A Fast Voltage Detection Method for Grid-tied Renewable Energy Generation Systems under Distorted Grid Voltage Conditions

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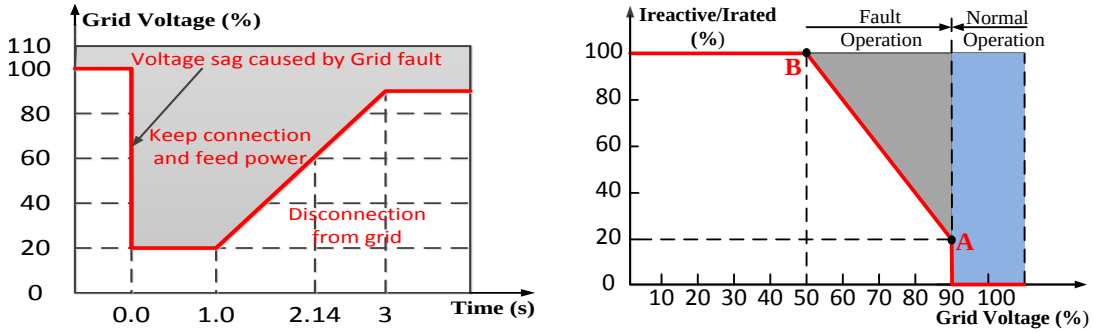
Abstract- A fast voltage detection method to assist with the low voltage ride-through (LVRT) operation of grid-tied renewable energy generation systems is proposed in this paper. It is designed to detect every phase voltage so that it can be applied in both three-phase and single-phase applications. The whole voltage detection approach consists of two stages, the pre-filtering stage and the voltage detection stage. In the pre-filtering stage, a cascaded delayed signal cancellation (CDSC) module and a low-pass filter are connected in series to filter low-order harmonics and high-frequency noises. For eliminating the low-order harmonics of interest, different types of CDSC methods are studied in detail. Subsequently, a new orthogonal signal generator (OSG) is built to calculate the voltage amplitude in the voltage detection stage. Finally, the proposed voltage detection method is verified by experimental results.

Index Terms—voltage detection, cascaded delayed signal cancellation, orthogonal signal generator, harmonic cancellation.

I Introduction

Along with the increasing penetration of distributed renewable energy generation systems, the grid stability and reliability are now facing significant challenges [1]. Especially, during the grid fault period, the behaviors of grid-tied converters have a significant impact on the grid stability. For instance, sudden disconnection of massive renewable power plants from the grid during voltage sag faults may trigger more severe problems than the initial event such as power outage and voltage flicker [2] [3]. Hence, many countries have enacted their grid codes to guide the operation of grid-tied renewable power systems [4] [5]. These new grid codes require grid-tied converters be capable of low voltage ride-through (LVRT) when suffering grid voltage sag.



(a) (b)

Fig. 1. LVRT requirements (a) China: Q/GDW 617-2011. (b) The E.ON code for LVRT.

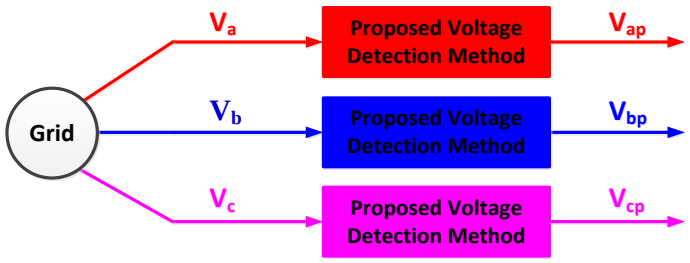
Fig. 1(a) shows the Chinese LVRT standard for large-capacity grid-tied photovoltaic (PV) inverters. As shown, PV inverters should stay connected to the grid in the shaded area. Besides, they are also required to provide reactive power for dynamic network support during the fault period and in the recovery process [6]. The E.ON code shown in Fig. 1(b) defines the amount of injected reactive current during LVRT. The injection of reactive power should be sufficiently fast, e.g., the PV system should deliver the required reactive power within 30 ms [7]. Moreover, faster detection of the voltage sag means that the grid-tied converter has more respond time, which is beneficial for the converter safety. Therefore, the voltage variation ratio should be detected as fast as possible.

Since the grid-tied converter is required to respond according to the variation of either line voltage or phase

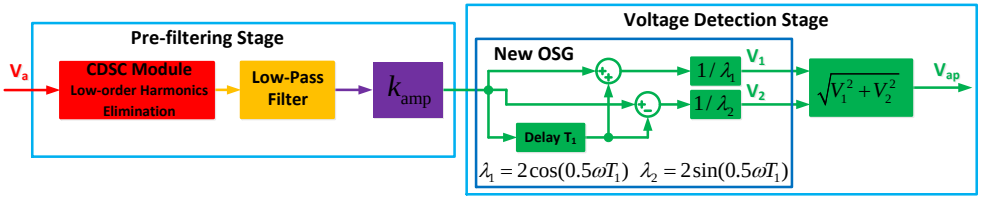
voltage [7], the adopted voltage detection method should have the capability of detecting each phase voltage. Consequently, conventional voltage detection approaches based on three-phase phase locked loop (PLL) such as DQ transformation method [8], cannot satisfy the new requirements. Several other voltage detection methods have been proposed in the literature, e.g., the RMS voltage detection [9], the peak voltage detection [10], and the discrete Fourier transform (DFT) [11] [12] [13], whose detection speed is too slow for LVRT operation. The peak voltage detection method maximally introduces half grid cycle delay, while both the RMS and FFT related methods induce one grid cycle delay [14]. Furthermore, for ensuring an accurate detection of the grid voltage under distorted conditions, the low-order harmonics and unbalanced variations of the grid voltage should be considered during the design. The current solutions are to either insert a digital filter into the PLLs [15] [16] [17], or use the positive and negative component separation methods [18] [19] to extract the fundamental voltage component for calculating the grid voltage. Note that, detecting each phase voltage separately with three independent single-phase PLLs is also valid for unbalanced voltage variations. However, as a matter of fact, the settling time of PLL related methods generally cannot be less than one grid cycle so that PLLs are not suitable for detecting the grid voltage variation ratio during LVRT operation. [14] presents a new detection method which is to detect both the maximum and zero voltage points. Its response time is affected by the position at which the voltage variation occurs, and the largest time delay is 10.1 ms.

To meet the requirement of LVRT operation, a new voltage detection scheme is designed for detecting the grid voltage variation ratio as fast as possible, while providing high detection accuracy under generally distorted conditions. In this work, every phase voltage is detected separately as shown in Fig. 2. Since the delayed signal cancellation (DSC) technique has the advantages of easy implementation and less computational burden [20] [21] [22], a cascaded DSC (CDSC) module is used to eliminate the low-order odd harmonics of the sampled grid voltage signal in the pre-filtering stage. In addition, a low-pass filter is employed to filter possible high-

frequency noises. Next, a new orthogonal signal generator (OSG) is built to calculate the voltage amplitude in the voltage detection stage. The main contribution of this paper is developing a new OSG with fast dynamic speed. Also, a new harmonic cancellation method is introduced. Finally, a fast and accurate detection of the grid voltage can be achieved with the proposed method.



(a)



(b)

Fig. 2. (a) The voltage detection approach for three-phase systems. (b) The proposed voltage detection method for each phase.

II Proposed Orthogonal Signal Generator (OSG) for Voltage Detection

Given the same detection principle of each phase voltage in Fig. 2, only the phase a $V_a(t) = V_{ap}\sin(\omega t)$, where V_{ap} is the voltage amplitude and ω is the angular frequency, is analyzed in this paper. Generally, an orthogonal signal V_β with respect to V_a can be generated with the OSG technique so that the voltage amplitude can be given by $V_{ap} = \sqrt{V_a^2 + V_\beta^2}$. The second order generalized integrator (SOGI) [23], the quarter-cycle delay [24], and the first-order differential method [25] [26], are three typical OSG methods. SOGI provides low computation burden and strong filtering capability. However, it gives a settling time of more than half of the fundamental period [27]. The quarter-cycle delay introduces a time delay of one fourth of the

fundamental period. Comparatively, the first-order differential method, which can derive the orthogonal signal in one sampling period, is the fastest OSG. As well known, higher accuracy of the first-order differential method requires higher sampling frequency, yet the high-frequency noise in the sampling process will be further amplified inevitably. To deal with these issues, a fast OSG algorithm, which is characterized by noise immunity and high accuracy in a wide range of sampling frequencies, is hereby proposed as

$$\begin{aligned} V_1(t) &= \frac{V_a(t)+V_a(t-T_1)}{\lambda_1} = \frac{V_{ap}\sin(\omega t)+V_{ap}\sin(\omega t-\omega T_1)}{2\cos(0.5\omega T_1)} = V_{ap}\sin(\omega t-0.5\omega T_1) \\ V_2(t) &= \frac{V_a(t)-V_a(t-T_1)}{\lambda_2} = \frac{V_{ap}\sin(\omega t)-V_{ap}\sin(\omega t-\omega T_1)}{2\sin(0.5\omega T_1)} = V_{ap}\cos(\omega t-0.5\omega T_1) \end{aligned} \tag{1}$$

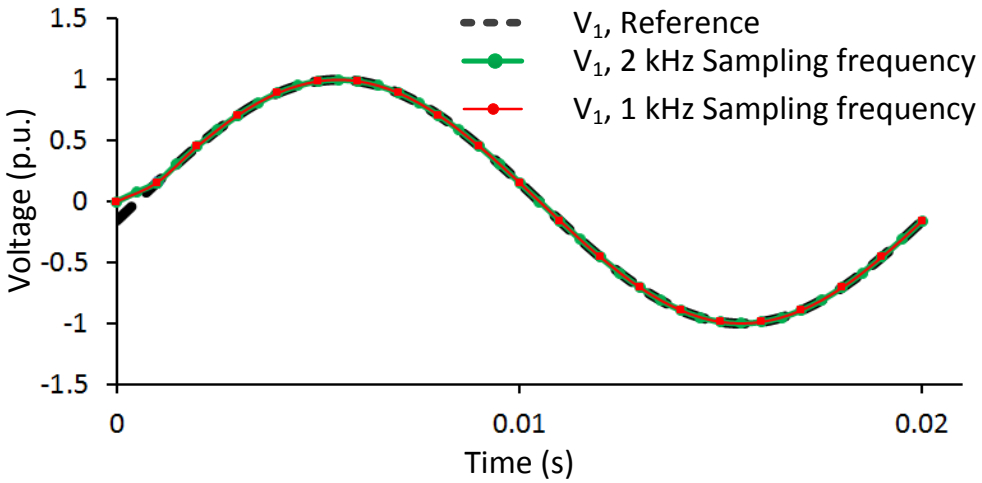
in which, T_1 is a predetermined delay time, and λ_1 and λ_2 are functions of T_1 and the grid frequency ω. Different from previous OSGs, the developed OSG creates an orthogonal frame of $V_{ap}\sin(\omega t-0.5\omega T_1)$ and $V_{ap}\cos(\omega t-0.5\omega T_1)$ instead of $V_{ap}\sin(\omega t)$ and $V_{ap}\cos(\omega t)$. It is worth noting that (1) is obtained by rigorous mathematical deduction without any approximation so that the accuracy of the proposed OSG is independent of the sampling frequency (see Fig. 3). From (1), the voltage amplitude can be achieved as $V_{ap}=\sqrt{V_1^2+V_2^2}$.

Note that T_1 is the only parameter which needs to be tuned in the proposed OSG. In what follows, the design considerations of T_1 are derived. Considering the high-frequency random noise V_x in the sampling process as $\tilde{V}_a(t)=V_a(t)+V_x(t)$, (1) can be rewritten as

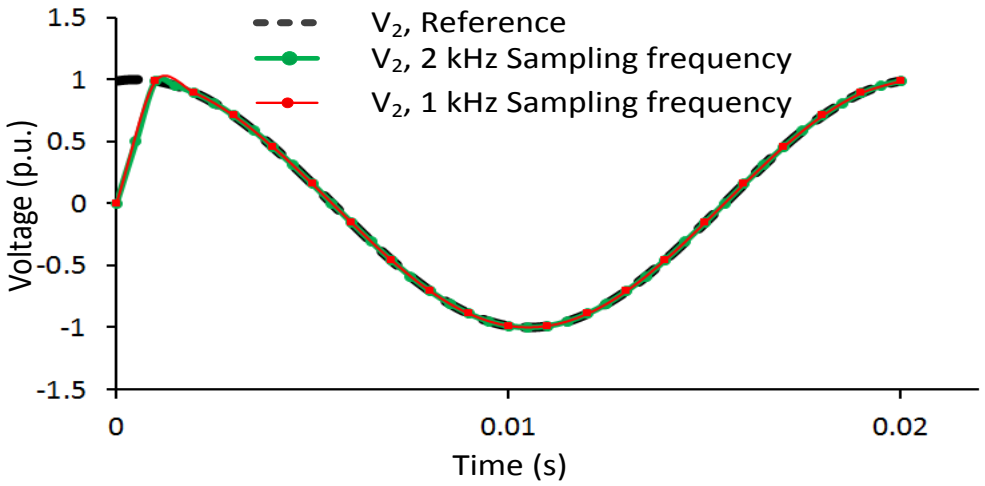
$$
\begin{aligned}
\tilde{V}_1(t) &= \frac{\tilde{V}_a(t)+\tilde{V}_a(t-T_1)}{2\cos(0.5\omega T_1)} = \frac{[V_{ap}\sin(\omega t)+V_x(t)]+[V_{ap}\sin(\omega t-\omega T_1)+V_x(t-T_1)]}{2\cos(0.5\omega T_1)} \\
&= V_{ap}\sin(\omega t-0.5\omega T_1)+\frac{V_x(t)+V_x(t-T_1)}{2\cos(0.5\omega T_1)} \\
&= V_{ap}\sin(\omega t-0.5\omega T_1)+V_{1n} \\
\tilde{V}_2(t) &= \frac{\tilde{V}_a(t)-\tilde{V}_a(t-T_1)}{2\sin(0.5\omega T_1)} = \frac{[V_{ap}\sin(\omega t)+V_x(t)]-[V_{ap}\sin(\omega t-\omega T_1)+V_x(t-T_1)]}{2\sin(0.5\omega T_1)} \\
&= V_{ap}\cos(\omega t-0.5\omega T_1)+\frac{V_x(t)-V_x(t-T_1)}{2\sin(0.5\omega T_1)} \\
&= V_{ap}\cos(\omega t-0.5\omega T_1)+V_{2n}
\end{aligned}
\tag{2}
$$

The physical quantities with superscript ~ in this paper indicate the existence of random noise. In (2)

$$
\begin{aligned}
|V_{1n}| &= \frac{|V_x(t)+V_x(t-T_1)|}{|2\cos(0.5\omega T_1)|} \le \frac{|V_x(t)|+|V_x(t-T_1)|}{|2\cos(0.5\omega T_1)|} \le \frac{|V_x|}{|\cos(0.5\omega T_1)|} = k_1|V_x| \\
|V_{2n}| &= \frac{|V_x(t)-V_x(t-T_1)|}{|2\sin(0.5\omega T_1)|} \le \frac{|V_x(t)|+|V_x(t-T_1)|}{|2\sin(0.5\omega T_1)|} \le \frac{|V_x|}{|\sin(0.5\omega T_1)|} = k_2|V_x|
\end{aligned}
\tag{3}
$$



(a) Generated Signal V_1.



(b) Generated signal V_2.

Fig. 3. Orthogonal signals constructed by the proposed OSG under different sampling frequencies.

where, k_1 and k_2 are the possible maximal noise amplification factors of the developed OSG in the worst condition. Since T_1 is designed below 0.25 grid periods for the sake of fast response, k_1 is smaller than k_2 so that k_2 is mainly considered during the tuning of T_1. Obviously, k_2 decreases remarkably and the response time increases linearly with the increased T_1. Consequently, it is necessary to find a good compromise between noise reduction and response speed. Industrial experience suggests that a noise amplification factor of 10 can fully meet the precision requirement in most cases [28]. Considering the required fast detection of voltage sags during LVRT applications, T_1 is set as 1 ms so that $k_1 = 1.01$ and $k_2 = 6.4$. Namely, the response time of the designed OSG is 1 ms in this work. The possible high-frequency noises can be rejected by a low-pass filter with 1 kHz cutoff frequency in the pre-filtering stage as shown in Fig. 2 (b).

Note that, (1) is derived on the premise of known grid frequency ω. Generally, the grid frequency is often measured with a PLL in grid-tied converters. Therefore, it is reasonable to assume the grid frequency is known for implementing the proposed OSG. The frequency ω for calculating λ_1 and λ_2 should only update after the PLL settles to a new steady state. Consequently, the dynamic process of the PLL in response to voltage variations (amplitude or phase angle jump) does not affect the performance of voltage detection. In practice,

the allowable variation range of the grid frequency is generally small in normal operation mode such as 0.2 Hz in China, which has negligible influence on the accuracy of the developed voltage detection method. Hence, this paper mainly focuses on the grid voltage variation cases.

III Proposed Voltage Detection Method under Distorted Conditions

To accurately detect the grid voltage under distorted conditions, a CDSC module is used to filter the sampled grid voltage signal before sending it to the voltage detection stage. The 5th, 7th, 11th and 13th harmonics are considered in this work because these harmonics are dominant low-order harmonics in the grid [14], [29]. It should be mentioned that this method is not restrictive, and can be extended to more harmonics.

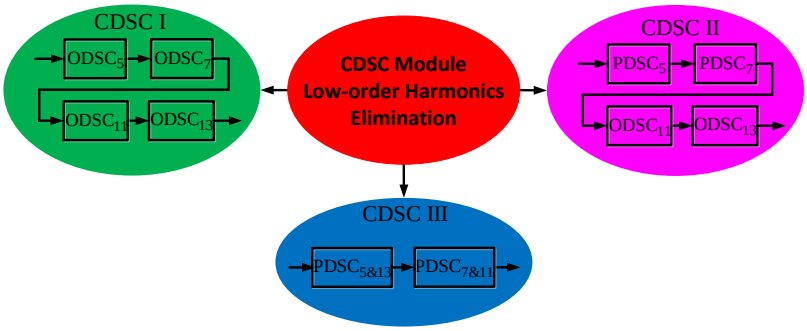


Fig. 4. Three types of CDSC methods for eliminating the 5th, 7th, 11th and 13th harmonics.

A. CDSC Method I

The CDSC method I (see Fig. 4) based on the original delayed signal cancellation (ODSC) [20] [21] [22] is used for cancelling the concerned harmonics. For the sake of simplicity, the grid voltage with only the nth odd harmonic as $V_a(t) = V_{ap}\sin(\omega t + \theta_1) + V_n \sin(n\omega t + \theta_n)$ is assumed for illustrating the operator $ODSC_n$. The output $ODSC_{no}$ of $ODSC_n$ is given by

$$\begin{aligned}\mathrm{ODSC_{no}}(t) &= V_a(t) + V_a(t-t_d) = V_a(t) + V_a(t-\frac{T_f}{2n}) \\ &= V_{ap}\sin(\omega t+\theta_1) + V_n\sin(n\omega t+\theta_n) + V_{ap}\sin(\omega t+\theta_1-\frac{\pi}{n}) + V_n\sin(n\omega t+\theta_n-\pi) \\ &= 2V_{ap}\cos(\frac{\pi}{2n})\sin(\omega t+\theta_1-\frac{\pi}{2n})\end{aligned} \tag{4}$$

in which, T_f is the fundamental period and t_d is the delay time. It is clear that the output does not contain the nth odd harmonic, while the fundamental component suffers from fixed amplitude and phase angle shift. Note that, the nth odd harmonic can be removed by $\mathrm{ODSC_n}$ only when $t_d = T_f/(2n)$. The total delay time of the CDSC Method I is $0.255T_f$, i.e., 5.1 ms for a 50 Hz power system (the grid frequency is assumed to be always 50 Hz in the following discussions).

B. CDSC Method II

We firstly introduce a proposed delayed signal cancellation (PDSC) operator $\mathrm{PDSC_n}$ for cancelling the nth odd harmonic. Similarly, the input $V_a(t) = V_{ap}\sin(\omega t+\theta_1) + V_n\sin(n\omega t+\theta_n)$ is used to illustrate the $\mathrm{PDSC_n}$ as

$$\begin{aligned}\mathrm{PDSC_{no}}(t) &= V_a(t) + V_a(t-t_d) - 2\cos(0.5n\omega t_d)V_a(t-0.5t_d) \\ &= V_{ap}\sin(\omega t+\theta_1) + V_n\sin(n\omega t+\theta_n) + V_{ap}\sin(\omega t+\theta_1-\omega t_d) + V_n\sin(n\omega t+\theta_n-n\omega t_d) \\ &\quad - 2\cos(0.5n\omega t_d)[V_{ap}\sin(\omega t+\theta_1-0.5\omega t_d) + V_n\sin(n\omega t+\theta_n-0.5n\omega t_d)] \\ &= 2[\cos(0.5\omega t_d)-\cos(0.5n\omega t_d)]V_{ap}\sin(\omega t+\theta_1-0.5\omega t_d)\end{aligned} \tag{5}$$

It is obvious that the nth odd harmonic is eliminated for any given $t_d > 0$. A close observation of (4) and (5) reveals that $\mathrm{ODSC_n}$ is a special case of $\mathrm{PDSC_n}$ with $t_d = T_f/(2n)$. Next, how to design $\mathrm{PDSC_n}$ for eliminating the nth odd harmonic with less time delay is given. Considering the high-frequency random noise V_x in the sampling process as $\tilde{V}_a(t) = V_a(t) + V_x(t)$, (5) can be rewritten as

$$\begin{aligned}\tilde{\mathrm{PDSC}}_{\mathrm{no}}(t) &= \tilde{V}_a(t) + \tilde{V}_a(t-t_d) - 2\cos(0.5n\omega t_d)\tilde{V}_a(t-0.5t_d) \\ &= 2[\cos(0.5\omega t_d)-\cos(0.5n\omega t_d)]V_{ap}\sin(\omega t+\theta_1-0.5\omega t_d) \\ &\quad + [V_x(t) + V_x(t-t_d) - 2\cos(0.5n\omega t_d)V_x(t-0.5t_d)]\end{aligned} \tag{6}$$

The ratio of the random noise to the amplitude of the fundamental component in (6) is defined as

$$F(t_d,n)=\frac{|V_x(t)+V_x(t-t_d)-2\cos(0.5n\omega t_d)V_x(t-0.5t_d)|}{|2[\cos(0.5\omega t_d)-\cos(0.5n\omega t_d)]V_{ap}|}$$
$$\le\frac{|V_x|+|V_x|+|2\cos(0.5n\omega t_d)||V_x|}{|2[\cos(0.5\omega t_d)-\cos(0.5n\omega t_d)]V_{ap}|}=k_3(t_d,n)\frac{|V_x|}{V_{ap}} \quad (7)$$

where $k_3(t_d,n)$ is termed as the possible maximal noise amplification factor of $PDSC_n$ in the worst case. While in $ODSC_n$

$$\tilde{ODSC}_{no}(t)=[\tilde{V}_a(t)+\tilde{V}_a(t-\frac{T_f}{2n})]=2V_{ap}\cos(\frac{\pi}{2n})\sin(\omega t+\theta_1-\frac{\pi}{2n})+[V_x+V_x(t-\frac{T_f}{2n})]$$
$$F(\frac{T_f}{2n},n)=\frac{|V_x+V_x(t-\frac{T_f}{2n})|}{|2\cos(\frac{\pi}{2n})V_{ap}|}\le\frac{|V_x|}{|\cos(\frac{\pi}{2n})|V_{ap}}=k_3(\frac{T_f}{2n},n)\frac{|V_x|}{V_{ap}} \quad (8)$$

Fig. 5 shows the relationship of the noise amplification factor versus the delay time. It is obvious that the noise amplification factor $k_3(t_d,n)$ of $PDSC_n$ decreases with the increased t_d in the shown range. In terms of LVRT operation, a faster detection of the grid voltage variation ratio is preferred. Therefore, k_3 is set to around 3 so that the total delay time of four cascaded $PDSC_n$ (n= 5, 7, 11, 13) operators is 3.43 ms, which is 1.67 ms less than that (5.1 ms) of the CDSC method I. However, the possible maximal noise amplification factor of such four PDSC blocks is 81, which may be not preferred in practice. Alternatively, the 5th and 7th harmonics are eliminated with $PDSC_5$ and $PDSC_7$, respectively, and the 11th and 13th harmonics are removed with $ODSC_{11}$ and $ODSC_{13}$, respectively, as shown in Fig. 4. This method provides 4 ms time delay with the total noise amplification factor of 9, and is called the CDSC method II.

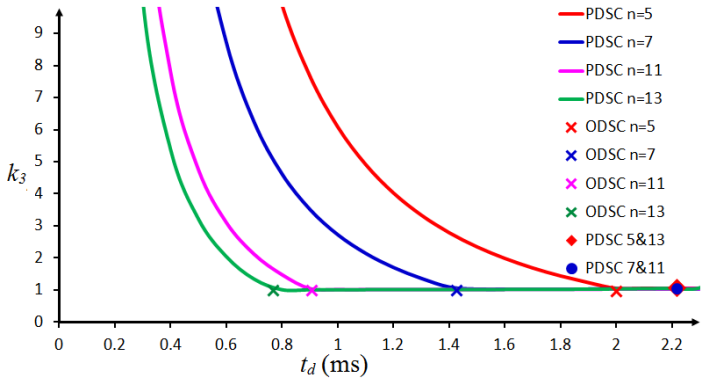


Fig. 5. The noise amplification factor versus the delay time.

C. CDSC Method III

In previous discussions, either $ODSC_n$ or $PDSC_n$ is designed to eliminate only the n^{th} odd harmonic so that four DSC blocks are needed for cancelling the 5^{th}, 7^{th}, 11^{th} and 13^{th} harmonics. In this section, a new operator $PDSC_{n\&m}$ with $t_d = 2T_f/(n+m)$ is used to remove the n^{th} and m^{th} odd harmonics (m>n) simultaneously, so that the number of cascaded blocks can be reduced by half, with the resulting reduced computation and delay time. The principle of $PDSC_{n\&m}$ is illustrated as follows:

$$\begin{aligned} V_a(t) &= V_{ap}\sin(\omega t+\theta_1)+V_n\sin(n\omega t+\theta_n)+V_m\sin(m\omega t+\theta_m) \\ \mathrm{PDSC}_{\mathrm{n\&mo}}(t) &= V_a(t)+V_a(t-t_d)-2\cos(0.5n\omega t_d)V_a(t-0.5t_d) \\ &= 2[\cos(0.5\omega t_d)-\cos(0.5n\omega t_d)]V_{ap}\sin(\omega t+\theta_1-0.5\omega t_d) \end{aligned} \tag{9}$$

To eliminate the 5^{th} and 13^{th} harmonics, t_d of $PDSC_{5\&13}$ should be $T_f/9$. Similarly, $PDSC_{7\&11}$ with $t_d = T_f/9$ can remove both the 7^{th} and 11^{th} harmonics. Therefore, only two cascaded blocks, $PDSC_{5\&13}$ and $PDSC_{7\&11,}$ are needed for eliminating the 5^{th}, 7^{th}, 11^{th}, and 13^{th} harmonics, and this method is named as the CDSC method III. With half number of the cascaded blocks, this approach can reduce the computational load compared with the CDSC I and II methods. In addition, the total delay time of the CDSC method III is 4.4 ms which is 0.7 ms less than that of the CDSC method I. From (7), the noise amplication factors of $PDSC_{5\&13}$ and $PDSC_{7\&11}$ can be derived as

$$\begin{aligned} k_3(\frac{T_f}{9},5) &= \frac{(1+|\cos(0.5n\omega t_d)|)}{|\cos(0.5\omega t_d)-\cos(0.5n\omega t_d)|} = \frac{(1+|\cos(\frac{5\pi}{9})|)}{|\cos(\frac{\pi}{9})-\cos(\frac{5\pi}{9})|} = 1.054,\ \mathrm{PDSC}_{5\&13} \\ k_3(\frac{T_f}{9},7) &= \frac{(1+|\cos(0.5n\omega t_d)|)}{|\cos(0.5\omega t_d)-\cos(0.5n\omega t_d)|} = \frac{(1+|\cos(\frac{7\pi}{9})|)}{|\cos(\frac{\pi}{9})-\cos(\frac{7\pi}{9})|} = 1.035,\ \mathrm{PDSC}_{7\&11} \end{aligned} \tag{10}$$

The noise amplification factors of the designed $PDSC_{5\&13}$ and $PDSC_{7\&11}$ are close to one, which means the CDSC method III has nearly the same noise rejection capability as the CDSC method I according to Fig. 5.

As analyzed above, due to the CDSC module, the fundamental component suffers from a fixed amplitude

shift, which is compensated by using a factor k_{amp} as shown in Fig. 2(b). The compensating factors of different CDSC methods are shown as

$$k_{amp} = \frac{1}{16\cos(\frac{\pi}{10})\cos(\frac{\pi}{14})\cos(\frac{\pi}{22})\cos(\frac{\pi}{26})} = 0.0686, \text{ CDSC I}$$

$$k_{amp} = \frac{1}{4[\cos(\frac{7\pi}{100}) - \cos(\frac{7\pi}{20})][\cos(\frac{9\pi}{200}) - \cos(\frac{63\pi}{200})]} \times \frac{1}{4\cos(\frac{\pi}{22})\cos(\frac{\pi}{26})} = 0.2021, \text{ CDSC II} \quad (11)$$

$$k_{amp} = \frac{1}{4[\cos(\frac{\pi}{9}) - \cos(\frac{5\pi}{9})][\cos(\frac{\pi}{9}) - \cos(\frac{7\pi}{9})]} = 0.1316, \text{ CDSC III}$$

TABLE I

Detection time comparison of different methods considering low-order harmonic distortion

Detection Method	FFT-based Methods [11]-[13]	PLL-based Methods [30] [31]	RMS Method [9]	Method [**Error! Bookmark not defined.**]	Proposed method		
					CDSC I	CDSC II	CDSC III
Detection Time	20 ms	> 20 ms	20 ms	5 - 10.1 ms	6.6 ms	5.5 ms	5.9 ms

D. Comparison with Previous Voltage Detection Methods

The detection time comparison between previous voltage detection methods, and the proposed ones with different harmonic cancellation methods is listed in Table I for the condition of three-phase unbalanced voltage drop with low-order harmonic distortion. The developed method can detect the voltage amplitude within 6.6 ms (CDSC I) or 5.5 ms (CDSC II) or 5.9 ms (CDSC III) when considering the 5^{th}, 7^{th}, 11^{th}, and 13^{th} harmonics. The detection time mentioned here is obtained considering both the pre-filtering stage and the voltage detection stage. It is worth mentioning that the detection time would increase slightly if more odd harmonics are considered. In terms of the detection time, the proposed methods are better than most of the previous methods

which can provide accurate voltage measurement under distorted conditions.

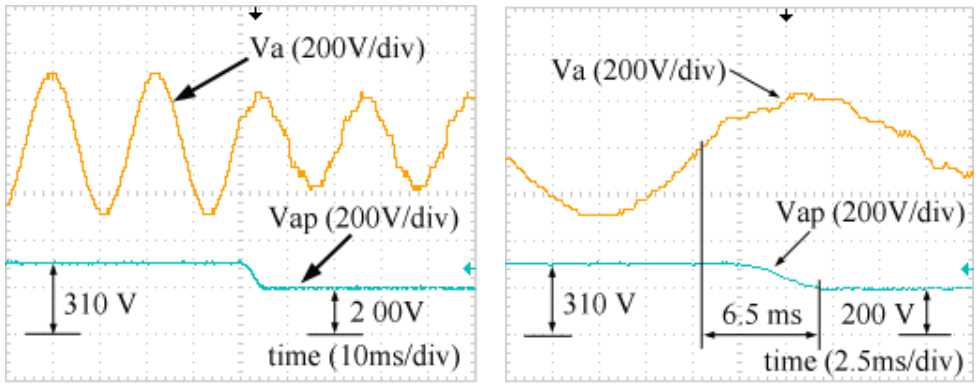
IV Experimental Results

The proposed voltage detection method is verified experimentally on a DSP chip TMS30F28335-based platform. All the operations are conducted with 10 kHz sampling frequency. The normal voltage amplitude is 310 V and the dropped voltage amplitude is set to 200 V. Along with the voltage amplitude drop, the 5^{th} (6%), 7^{th} (4.8%), 11^{th} (4%) and 13^{th} (3.2%) voltage harmonics are added for testing the harmonic rejection performance of the developed voltage detection method. The corresponding experimental results are shown in Fig. 5. It can be observed that the detection method with CDSC I, CDSC II or CDSC III, can fast detect the voltage amplitude even under distorted grid voltages. The response time of the approach with PDSC (CDSC II or CDSC III) is less compared to the one (CDSC I) based on ODSC. The achieved reduction of the delay time by using PDSC is limited in this paper, however, the freedom to design the time delay as well as the possibility to reduce the number of cascaded modules makes PDSC interesting for applications related to harmonics cancellation.

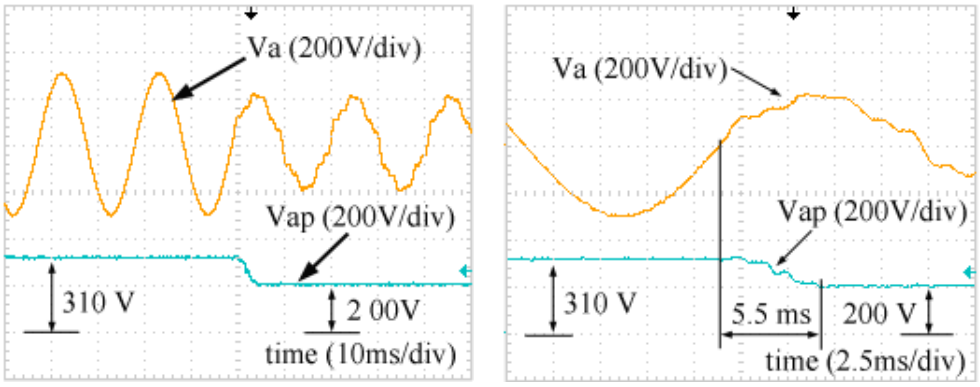
V Conclusions

This paper presents a fast voltage detection method to assist with the LVRT operation of grid-tied renewable energy generation systems. With the proposed approach, the amplitude of each phase voltage can be measured in a fast and accurate way under generally distorted conditions. Firstly, a new OSG with fast response speed is analyzed in detail. The benefit of adopting the new OSG is that the detection time of the grid voltage is significantly reduced. Secondly, based on DSC, a novel harmonic cancellation block is developed such that both the delay time and number of the cascaded DSC blocks for eliminating the low-order harmonics of interest

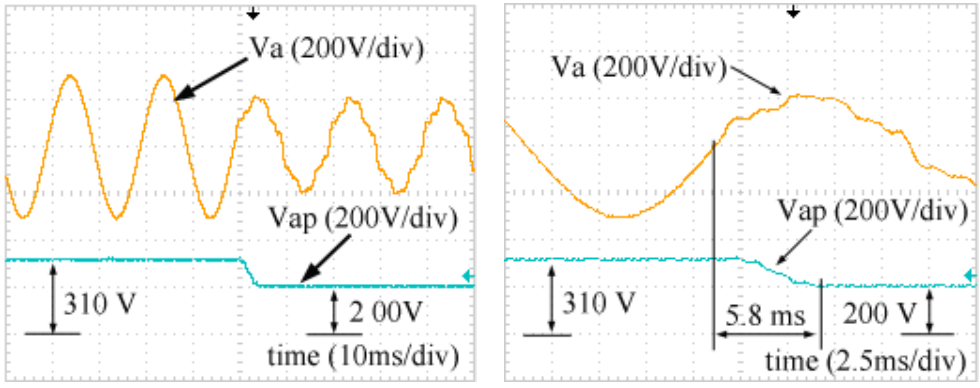
can be reduced. Finally, the presented voltage detection method is verified by experimental results.



(a) CDSC Method I



(b) CDSC Method II



(c) CDSC Method III

Fig. 5. Experimental results of the proposed voltage detection method.

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