Response to "Comment on 'Catastrophic degradation of the interface of epitaxial silicon carbide on silicon at high temperatures'" [Appl. Phys. Lett. 109, 196101 (2016)]

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(Received 13 October 2016; accepted 25 October 2016; published online 8 November 2016)

[http://dx.doi.org/10.1063/1.4967228]

Dimitrijev argues that the conclusions of our letter[1] are incorrect, based on two points. We summarize each criticism and respond point by point:

1. Dimitriev questions our conclusion that SiC is electrically shorted to Si based on the fact that the sheet resistance of the annealed SiC-Si system differs quantitatively from that of the pristine silicon substrate material.[2]

We have studied the temperature-dependent data resistivity of the as-grown and annealed 3C-SiC on Si (Fig. 1 of Ref. 1). As-grown n-SiC/p-Si showed limited n-type conduction as expected for an epitaxial SiC film on silicon, whereas the n-SiC/p-Si sample after annealing showed a resistance two orders of magnitude lower than the SiC layer. The conduction in the annealed sample appears dominated by p-type carriers, with a transition around ~25 K to n-type conduction similar to the non-annealed n-SiC/p-Si. This results clearly indicate the formation of a new parallel conduction path which is (1) p-type, (2) has higher mobility than SiC, and (3) freezes out around ~25 K; these aspects are all in agreement with the Si substrate acting as the new conduction channel. The author proposes no alternative conduction channel which could explain our observations (1)–(3). We do observe a quantitative change in the sheet resistance of the Si substrate, which we ascribe to a change in doping after annealing (Table I of Ref. 1). Notably, the mobility of the p-type conduction channel (273 cm^2/Vs) is very similar to that for the doped Si substrate (341 cm^2/Vs), again suggesting that the additional conduction channel is silicon.

In addition, we performed a simple experiment to verify unambiguously that, after annealing, the SiC is indeed electrically well connected to the silicon substrate.

The as-grown unintentionally n-type doped 3C-SiC(100) with thickness of 300 nm grown in-house on lowly doped 6 in. p-type Si(100) wafer at 1000 °C[1,3] was patterned into structures with 300 nm of aluminium contacts as shown in Fig. 1. For the electrical characterization, SiC/Si wafers were diced into 1 × 1 cm^2 fragments.

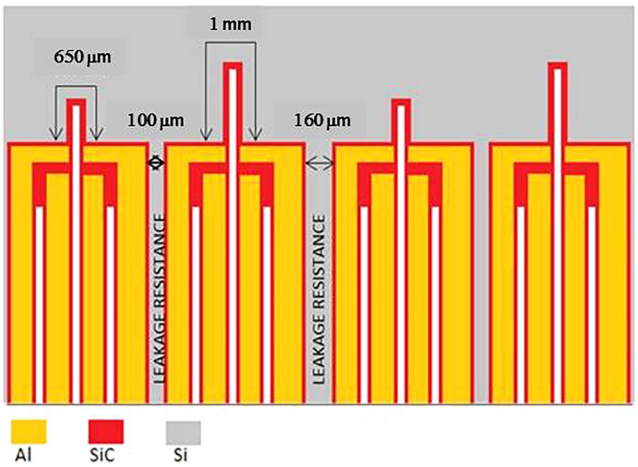

FIG. 1. Photolithographic pattern made on the SiC/Si for the electrical characterisation. (Courtesy of QMNC, Griffith University.)[4]

The current-voltage measurements were performed at room temperature to measure the SiC and silicon resistances (leakage) on the as-grown SiC(100) using a HP4145B semiconductor parameter analyser. Analogous samples were annealed at 1100 °C for 1 h. After an additional XeF_2 etching of silicon up to 14 μm in between the SiC structures, the electrical measurements were done at room temperature.

The as-grown SiC film indicates a factor of 30–50 difference in magnitude of the resistance of the SiC and the leakage through the silicon, as anticipated (Table I). However, after annealing, a major drop in all the SiC and leakage resistances to just a few kΩ is observed (Table I). This clearly indicates that separate thin-film SiC structures

TABLE I. SiC and silicon resistances (leakage) measured at room temperature for in-house SiC/Si(100) samples as-grown and after annealing at 1100 °C. The results are the averaged values from four measurements.

	As-grown	Annealed
R_{SiC} of 650 μm length (kΩ)	40	3
R_{SiC} of 1 mm length (kΩ)	70	4
$R_{leakage}$ across 100 μm (kΩ)	2000	1
$R_{leakage}$ across 160 μm (kΩ)	2000	1

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become electrically shorted through the silicon after annealing, fully supporting our report on the instability of the SiC/Si interface.[1]

2. The second point of the author's comment rejects the implications of our conclusions.[2]

Epitaxial SiC on Si could be used as a pseudo-substrate for the growth of functional layers such as graphene[5] and III-N materials,[6] for application as broad as electronic graphene devices and LEDs on silicon. Since these materials are generally grown at temperatures greater than 1000 °C, we believe it is important to consider the instability we discussed.

As to SiC on silicon for harsh environment operation, we only point out the potential for this failure mechanism to be initiated over time. A conclusive statement on the stability range of the 3C SiC-Si interface in harsh environments can be given exclusively by accurate bias-temperature-stress measurements that we can only encourage the community to investigate.

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