A thin film approach for SiC–derived graphene as an on-chip electrode for supercapacitors

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Abstract

We designed a nickel-assisted process to obtain graphene with sheet resistance as low as 80 Ω square^{-1} from silicon carbide films on Si wafers with highly enhanced surface area. The silicon carbide film acts as both a template and source of graphitic carbon, while, simultaneously, the nickel induces porosity on the surface of the film by forming silicides during the annealing process which are subsequently removed. As stand-alone electrodes in supercapacitors, these transfer-free graphene-on-chip samples show a typical double-layer supercapacitive behaviour with gravimetric capacitance of up to 65 F g^{-1}. This work is the first attempt to produce graphene with high surface area from silicon carbide thin films for energy storage at the wafer-level and may open numerous opportunities for on-chip integrated energy storage applications.

Key words: SiC, graphene, on-chip supercapacitors

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1. Introduction

An electrochemical capacitor, commonly known as a supercapacitor, has great potential as energy storage devices, as it has a prolonged service life and can be fully charged or discharged in just a few seconds [1]. Supercapacitors are capable of delivering an order of magnitude larger (10,000 Wkg^{-1}) power density more than lithium-ion batteries and two orders of magnitude higher (10 Whkg^{-1}) energy density than electrolytic capacitors [2]. Thus they show advances over commonly used energy storage devices such as lithium-ion rechargeable batteries, which have the undesirable characteristics of slow power output, and limited life cycles [3].

Carbon materials are low-cost and abundant in nature and they are one of the major active materials in supercapacitors to yield electrochemically stable double-layer capacitance [4, 5]. Carbide derived carbon (CDC) materials, a less known class of carbon, has attracted considerable attention in recent years due to their high surface area and tuneable pore structure [2, 6-8], leading to extensive research on CDC-based energy storage devices. For example, titanium carbide derived carbon (TiC-DC) and zirconium carbide derived carbon (ZrC-DC) powders show porous structure that plays a vital role in supercapacitor performance [9, 10].

Silicon carbide (SiC), mainly in powder form, has recently gained momentum for energy storage. The microstructure of SiC powders can be controlled by varying the synthesis conditions [11], hence tailoring the ion diffusion length [12]. SiC can tolerate extreme conditions and meet the critical energy storage requirements, such as high temperature, corrosive media, operation in high radiation exposure and ultra-high g-shock resilience [13]. These beneficial features opened up a window for SiC derived carbon (SiC-DC) based energy storage applications. SiC-DC powders obtained by halogenation have a high specific surface area and tuneable microstructure with a narrow pore size distribution [11]. However, the prepared SiC-DC powders via this approach are not viable for fabricating on-chip supercapacitors.

In our recent work, we demonstrated a Ni-Cu catalytic graphitisation technique to produce bilayer graphene from 3C-SiC, which is the cubic form of SiC and can be grown heteroepitaxially on Si wafers with sheet

resistance as low as 25 Ω square[-1] [14]. This wafer-level technology is readily scalable and can be used to fabricate thousands of microdevices simultaneously [15]. Therefore, it can be applied to micro-supercapacitors [16], but does not offer a high surface area for charge storage purposes. We will show that in order to enhance the suitability for on-chip energy storage, we need to create large surface area and high porosity in the underlying 3C-SiC film. Herein, we propose a novel approach to simultaneously prepare a few-layer graphene over an extremely rugged epitaxial 3C-SiC surface. It is known that nickel can be used to induce graphitisation on the surface of the silicon carbide at a rather low temperature [17], but this approach has subsequently been dismissed because it tends to be uncontrolled and not uniform, creating a pronounced topography on the surface. However, if this secondary and usually detrimental aspect of pitting and protrusions on the SiC surface caused by nickel–induced graphitisation happened in a controlled fashion, this process would provide an unparalleled advantage for energy storage applications. As a matter of fact, this process would simultaneously provide a highly conductive surface (graphene) over an enhanced and accessible surface area. In this work, we pursue this idea and we demonstrate a CDC methodology to synthesise continuous graphene layers with increased surface area and low sheet resistance. Preliminary results indicate the merit of using epitaxial SiC-derived graphene for on-chip energy storage, offering advantageous miniaturisation prospects for a number of integrated microsystems such as sensors and energy harvesters.

2. Experimental

An epitaxial 3C-SiC layer was firstly grown on a Si (100) wafer via a calcination process at 1000 °C with SiH_4 (99.9994%) and C_3H_6 (99.9999%) supplied alternatively into a customised, horizontal, hot wall, low-pressure chemical vapour deposition furnace [18]. An n-type, unintentional doping of 10^{16}–10^{17} cm^{-3} was observed after the growth of a crystalline 3C-SiC layer (~300 nm thick) on the silicon wafer [19]. The 3C-SiC/Si wafer acted as a template to accommodate graphitisation and was coated with a thin nickel film (~2 nm) by using a DC Ar$^+$ ion sputterer with a deposition current of 100 mA at a base pressure of 8×10^{-2} mbar.

The wafer was annealed for 2h by conventional furnace annealing (FA, temperature ramping at ~25 °C min^{-1}) or four minutes by rapid thermal annealing (RTA, temperature ramping at ~5 °C s^{-1}) in a N_2 atmosphere at 1000-1200 °C. The flow rate of N_2 was maintained at 20 sccm which was sufficient to exclude oxygen during the annealing process. The annealed wafers were etched by Freckle solution (70:10:5:5:10 – 85% H_3PO_4: Glacial acetic acid: 70% HNO_3: 50% HBF_4: H_2O) to remove nickel silicides and unreacted nickel. Samples with different annealing conditions are denoted as F_1 (1000 °C via FA), F_2 (1200 °C via FA), R_1 (1000 °C via RTA), and R_2 (1100 °C via RTA), respectively.

All the samples were characterized by Raman Spectroscopy on a Renishaw spectrometer with a laser excitation at 514 nm on four different sites of the surface. The chemical composition was determined by X-ray Photoelectron Spectrometry (XPS) in a ultrahigh vacuum system using a non-monochromatic Mg Kα (1253.6 eV) X-ray source (DAR 400, Omicron Nanotechnology), 300W incident angle at 65° to the sample surface, with a 125 mm hemispherical electron energy analyser (Sphera II, 7 channels detector, Omicron Nanotechnology). Photoelectron data were collected at a take-off angle of 90°. Survey scans were taken at analyser pass energy of 50 eV and high resolution scans at 20 eV. The survey scans were carried out with 0.5 eV steps and a dwell time of 0.2 s, whereas high-resolution scans were run with 0.2 eV steps and 0.2 s dwell time. The pressure in the analysis chamber during XPS scans was kept below 4.0×10^{-10} mbar. To investigate the surface morphology, samples were examined by Scanning Electron Microscopy (SEM) using a HITACHI SU70 tool. Transmission Electron Microscopy (TEM) was used to evaluate cross-sectional images of the samples. TEM samples were prepared using a Focused Ion Beam (FIB) lift-out technique. Prior to ion milling, the samples were protected with a 5keV e-beam deposited Pt cap to preserve the initial surface integrity. The samples were then prepared by FIB milling with a Ga ion beam at 30keV to a thickness of ~1 μm and then polished using an Ar ion beam at 500eV to remove the Ga ion damage and to obtain electron transparency for high resolution imaging. Then the samples were inserted into an FEI Titan Cs corrected TEM operated at 80keV. Atomic Force Microscopy (AFM) with a NT-MDT Integra spectra system was used to scan the surface texture on the samples. Sheet resistance of catalytic graphene formed on

3C-SiC/Si wafers, as well as the reference 3C-SiC/Si wafer, was measured using macroscopic Van der Pauw structures over 1×2 cm^2.

All samples (1×2 cm^2) were dried and directly assembled as working electrodes with an Ag/AgCl reference electrode and a platinum counter electrode in a three-electrode cell setup. The electrochemical tests were performed in a 3 M KCl aqueous electrolyte. The cyclic voltammetry (CV) tests were carried out at a voltage range of 0 to 0.8 V (against Ag/AgCl) on a Princeton Applied Research VersaSTAT 4 potentiostat unit. The scan rates ranged from 5, 10, 20, 50 to 100 mVs^{-1}. Electrochemical Impedance Spectroscopy (EIS) was performed on the same instrument at a frequency range of 100 kHz to 100 mHz with an alternating current amplitude of 10 mV. Galvanostatic charge and discharge performance was evaluated at current densities of 1-10 µA cm^{-2}, respectively on a Radiometer Analytical Voltalab 40 device.

3. Results and discussion

Material Characterization

Figure 1 demonstrates the mechanism to grow graphene on 3C-SiC/Si wafers. A thin layer (~2 nm) of nickel metal is firstly sputtered on a 3C-SiC/Si wafer, as shown in Figure 1. Nickel plays a crucial role in our approach to dissociate the Si-C bonds [20], forms nickel silicides and graphitic carbon [21], and simultaneously creates porosity on the surface of 3C-SiC/Si wafers. The released graphitic carbon (from the 3C-SiC) evolves not only at the SiC/Ni interface, but also in the surrounding silicides layers [22], and it evolves in crystalline form to produce graphene. The overall reaction to represent the synthesis routine can be simplified as follows:

$$y\text{Ni} + x\text{SiC} \rightarrow \text{Ni}_y\text{Si}_x + x\text{C (graphene)} \quad (1)$$
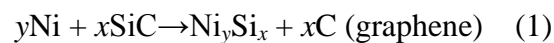
$$(\text{where } x,y = 1\text{-}2)$$

Silicides and unreacted nickel are etched by sonication in the Freckle solution with extreme care to retain the graphene layers on the SiC/Si wafer [17].

Raman spectroscopy is a powerful and non-destructive technique to assess the graphitic structure by comparing the D and G Raman bands. The G band (~1580 cm^{-1}) reveals the phonon vibration in the E_{2g} mode, while the D band (~1350 cm^{-1}) corresponds to the defects and disordered nature of sp^2 carbon network. The intensity ratio of D and G peak (I_D/I_G) attributes to the degree of reduction of sp^2 structure and defects [23]. A higher value of I_D/I_G indicates a more defective crystalline structure. SiC-DC powders processed by halogenation have a small pore size with a high value of I_D/I_G, indicating an abundance of defective sites [24]. In our approach, the metal-induced graphitized carbon (graphene) on 3C-SiC/Si wafer shows relatively low I_D/I_G values (0.7-1.2, Table 1), indicating low defectivity of the graphene.

High resolution XPS spectra of the C1s peak studied here are shown in Figure 2 for all samples, where the C1s peak is de-convoluted into two fitting peaks. The enriched graphene layer can be identified at ~285 eV as graphitic carbon, while the carbidic Si-C bonds are located at ~283 eV, attributed to the underlying 3C-SiC film. To quantitatively identify the number of produced graphene layers (*t*) on the 3C-SiC/Si wafer, the intensity ratio of the photoelectrons of graphene (N_G) and 3C-SiC (N_R, as a reference) peak in the high resolution XPS spectra is calculated as per the following equation [25], given the interlayer spacing of 3.35 Å for graphene [26].

$$\frac{N_G}{N_R} = \frac{T(E_G)\rho' C_G \lambda'(E_G)[1-\exp\left(-\frac{t}{\lambda'(E_G)}\right)]}{T(E_R)\rho C_R \lambda(E_R)\exp(-\frac{t}{\lambda(E_R)})} \cdot F \qquad (2)$$

where *T* represents the transmission function of the analyser; *E* stands for the kinetic energy of photoelectrons; ρ is the atomic density of the materials; *C* means the differential cross section; and λ refers to the inelastic mean free path from the TPP-2M formula [27]. Owning to photoelectron diffraction, a geometrical correction factor, *F*, is also included in the equation. The superscript ' indicates quantities referred to the graphene overlayer as opposed to the 3C-SiC bulk. By solving *t* from the equation, the number of graphene layers for each sample is determined to be 8.3, 13.7, 14.1, and 24.8 for F_1, F_2, R_1 and R_2, respectively, as recorded in Table 1.

Top-down SEM images (Figure 3) show that the initial surface of the pristine 3C-SiC (Figure 3(a)) possesses a high density of rectangular-shaped hillocks, which are the typical signature of stacking faults with two-fold symmetry on (100) surfaces [28]. The surface of all the graphene samples (Figure 3(b), (c), (d), and (e)) appears much rougher with a dense pitting pattern. This rugged morphology is a result of the diffusion of nickel into the 3C-SiC layer during annealing and the formation of localized silicide clusters that are subsequently etched away, as schematically shown in Figure 1. This phenomenon leads to a graphene layer with a larger surface area which, for the most part, conformally follows the 3C-SiC surface topology.

To further examine the morphology of the 3C-SiC film after graphitisation, a TEM analysis of sample F_2 is performed (Figure 4). The platinum capping layer deposited on top of the sample to preserve the surface under FIB has intruded into the SiC surface through surface pits, and the intrusion profile is highlighted with the dotted line in Figure 4, which represents therefore the actual SiC surface profile. Additionally, further away from the surface, several dark areas with a size within the range of ~30-50 nm are found, indicating also the presence of a component of pits that can be assimilated to open pore sites.

AFM images and line scan profiles of the graphene samples F_1, F_2, R_1, and R_2 over a scanning area of 20 μm×20 μm are shown in Figure 5. The AFM scan images (Figure 5(a), (c), (e), and (g)) indicate significant roughness for all samples, while the surface topography is further revealed by the line scan profiles (Figure 5(b),(d),(f), and (h)). As indicated in Table 1, F_1 has the smallest RMS roughness of ~23 nm, while F_2, R_1, and R_2 have relatively larger values of ~41, 66 and 70 nm, respectively. Note that the initial RMS roughness of the pristine bare 3C-SiC is ~3.8 nm.

Sheet resistance represents a measure of the resistance of a thin film of uniform thickness and is useful in the assessment of the conduction in thin films. The obtained graphene on 3C-SiC/Si yields sheet resistances varying over a large range according to the different annealing conditions, from 680 Ω square^{-1} down to 80 Ω square^{-1}, as shown in Table 1. All of these values represent a significant improvement over the untreated

reference 3C-SiC/Si layer with a sheet resistance of ~4-7×10³ Ω square⁻¹ [15], thanks to the presence of the graphene layers. Samples R_1 and F_2 show the lowest graphene sheet resistance (~80 Ω square⁻¹).

Electrochemical Analysis

CV curves of F_1, F_2, R_1, R_2 and reference 3C-SiC/Si samples at different sweep rates are exhibited in Figure 6(a)-(e). All electrodes present a rectangular shape, indicating a pre-dominant double-layer storage mechanism. Each electrode shows similar CV curves at various scanning rates, exhibiting high reversibility of the double-layer behaviour. Minor cathodic and anodic humps appear around ~0.2 V and they are most likely originating from Ni^{2+} impurity residues [14, 29], providing a minor pseudocapacitance component. All of the annealed samples have much higher responsive current densities along the voltage scan region, indicating a much higher capacitance over the reference 3C-SiC/Si, which delivers rather limited capacitance. The enhanced electrochemical behaviour for the annealed 3C-SiC/Si wafers is attributed to the grown graphene layers, which store ionic charge on their surface. The specific area capacitances (F cm⁻²) of F_1, F_2, R_1, R_2 and the reference 3C-SiC/Si samples versus scan rates are plotted in Figure 6(f). These are calculated from the CV curves against the apparent geometric electrode working area (2 cm²). R_1 exhibits the best capacitive performance. The area capacitance calculated for the lowest scan rate (5 mV s⁻¹) is 31.8, 37.5, 69.5, 34.4 and 6.2 μF cm⁻² for F_1, F_2, R_1, R_2 and reference 3C-SiC/Si, respectively. To convert the area capacitance (C_A, F cm⁻²) to gravimetric capacitance (C_G, F g⁻¹), we use the equation below:

$$C_G = \frac{C_A}{\frac{\rho_a}{N_A} \cdot M_C \cdot t} \quad (3)$$

where ρ_a is the atomic density of monolayer graphene (3.8×10¹⁵ atoms cm⁻²); N_A represents Avogadro's Constant (6.022×10²³ mol⁻¹); M_C is the molar mass of carbon (12.01 g mol⁻¹); and t is the number of graphene layers as obtained from Equation (2). The values of the area and gravimetric capacitance at a scan rate of 5 mV s⁻¹, as well as the sheet resistance, RMS roughness (Rq, nm), and the number of graphene layers measured via XPS of each sample are listed in Table 1.

The galvanostatic charge-discharge (GC) curves of F_1, F_2, R_1, R_2 and the reference 3C-SiC/Si electrodes are shown in Figures 7. All the curves show no obvious IR drops, suggesting low series resistances in these electrodes. Each graphene sample exhibits similar charge and discharge curves for the different current densities, indicative of a high reversibility. Distortions are found for R_1 and R_2 at ~0.4 V and they can be ascribed to the reactions of Ni^{2+} residues [14]. Note that we use similar Freckle etching time for all samples. R_1 and R_2 have a significantly higher surface roughness than the other samples, making a complete removal of Ni^{2+} residues more challenging. The R_1 electrode shows the longest discharge time for each current density, in agreement with the largest area capacitance among all the electrodes as per Table 1, which are calculated from the CV curves (Table 1). While at low current densities the charge/discharge times show more variations, at high current rates, the discharge times for R_2, F_1, and F_2 all converge to similar values, in line with the comparable area capacitances calculated from the CV curves.

Electrochemical Impedance Spectroscopy (EIS) is a prominent measure to assess the internal resistance of supercapacitors. Figure 8 shows the Nyquist plots of F_1, F_2, R_1, R_2 and the reference 3C-SiC/Si electrodes in a 3 M KCl electrolyte solution. The equivalent circuit model is also shown in the inset, where Rs is the electrolyte resistance (which includes the electrode resistance, the bulk electrolyte resistance and the resistance at the electrolyte/electrode interface); C_D is the double layer capacitance; R_{CT} is the charge transfer resistance; W is the Warburg impedance; and C_F is the Faradic pseudocapacitance [30]. All the Nyquist plots exhibit nearly vertical slopes in the low frequency region, indicating good capacitor behaviour of all the supercapacitor cells. The intercept of the real part axis at the high frequency region, as seen in the magnified view in the inset of Figure 8, is related to the electrolyte resistance (R_s) [31]. We found that all graphene samples have much smaller values of R_s than the reference 3C-SiC/Si, as expected, showing a highly improved bulk electrolyte resistance, in good agreement with their decreased sheet resistance. The diameter of the semicircle on the plot reveals the charge transfer resistance (R_{CT}); the reference 3C-SiC/Si has a larger semicircle than the other four catalytic graphene samples, indicative of a much larger R_{CT}, which is related to the low carrier doping and leads to limited capacitance. As graphene evolves on the 3C-SiC/Si wafers, the charge transfer resistance of the cell is further decreased, as evidenced by the presence of smaller

semicircles. These EIS results further confirm the improved conductivity of the supercapacitor cell with the catalytic graphene-on-chip electrodes, which deliver enhanced electrochemical performance compared to the reference bare 3C-SiC/Si electrode.

Final Discussion

As shown in Table 1, the synthesised graphene on SiC films plays a dual role in our on-chip supercapacitors – it reduces significantly the sheet resistance of the bare SiC and accumulates charges for double-layer capacitance. R_1 has the best electrochemical performance in terms of area capacitance (69.5 μF cm^{-2}) and gravimetric capacitance (65.0 F g^{-1}) among all samples. We credit this to its low sheet resistance (80 Ω square^{-1}), combined with the large RMS roughness (66 nm), which results in a larger surface area to facilitate charge storage on the graphene surface.

F_2 has a similar sheet resistance (80 Ω square^{-1}) to that of sample R_1, and a similar number of graphene layers, but its electrochemical performance is much poorer. We attribute this to its lower RMS roughness (41 nm), leading to a lower total surface area. R_2 has similar RMS roughness (70 nm vs. 66 nm) to R_1, but yields lower area capacitance and gravimetric capacitance. We ascribe this to its larger sheet resistance (236 Ω square^{-1}). It is worth noting that the merit of large RMS roughness of R_2 is suppressed by its large sheet resistance, giving a similar value of area capacitance to F_2. Sample F_1 shows the lowest area capacitance among the four graphene samples, likely due to the highest sheet resistance (680 Ω square^{-1}) combined to the smallest RMS roughness (23 nm).

In terms of graphene characteristics, we note that R_1, with ~14 graphene layers, delivers the best area and gravimetric capacitance, whereas R_2, with ~25 layers, shows the worst gravimetric capacitance, and F_1, with the fewest layers, yields the second best gravimetric capacitance. Thus it seems that a larger number of graphene layers does not correspond to a better electrochemical performance. This is an indication that only the few accessible graphene layers on top of the samples are essentially active in the double-layer charge storage, thus in determining the overall capacitance. In order to maximize the amount of accessible layers,

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the surface of graphene has to be as rugged as possible to create sufficient ion diffusion paths on the electrode. This means the synthesised graphene layers on SiC require a combination of low resistance and sufficiently high surface roughness to favorably make them accessible. A large increase in graphene layers like in the case of R_2 would demand further substantial increase in roughness to facilitate maximum accessibility of all available layers. Sample R_1 here demonstrates an optimal combination of surface roughness, graphene layer number and sheet resistance, to make the majority of graphene surface available for double-layer formation, showing the best performance among all samples.

We also conclude from Table 1 that the range of I_D/I_G values for the graphene obtained here do not correlate to either sheet resistance, or the electrochemical performance. They only correlate to the different synthesis conditions. Note also that the sheet resistance is most likely related to a complex combination of the number of layers, defectivity and discontinuities of graphene.

4. Conclusions

We demonstrate a process to simultaneously achieve graphene on 3C-SiC films on silicon and enhance greatly the surface area of such films by tailoring a nickel-assisted catalytic process. The obtained samples possess low sheet resistance thanks to the presence of graphene, and high surface area thanks to the creation of extensive roughening on the underlying 3C-SiC film. As stand-alone on-chip electrodes, they show typical supercapacitive behaviour with a specific capacitance of up to 65.0 F g^{-1} (or 69.5 µF cm^{-2}). We also indicate that the total accessible surface area and number of graphene layers is the key to high electrochemical performance. This new approach to the fabrication of electrodes for supercapacitors is transfer-free and can be performed at the wafer –level, and additionally it eliminates the need for conductive additives and binders that are typically used for electrochemical applications. By combining this approach with the patterning of graphene into an interdigitated structure as we proposed earlier [15], this technology can be used to create micro-supercapacitors on silicon chips in a simple and effective way.

Acknowledgments

References:

1. Simon, P. and Y. Gogotsi, *Materials for electrochemical capacitors.* Nature Materials, 2008. **7**(11): p. 845-854.
2. Miller, J.R. and P. Simon, *Materials science - Electrochemical capacitors for energy management.* Science, 2008. **321**(5889): p. 651-652.
3. Brodd, R.J., et al., *Batteries, 1977 to 2002.* Journal of the Electrochemical Society, 2004. **151**(3): p. K1-K11.
4. Notarianni, M., et al., *Graphene-based supercapacitor with carbon nanotube film as highly efficient current collector.* Nanotechnology, 2014. **25**(43).
5. Liu, J.Z., et al., *High performance all-carbon thin film supercapacitors.* Journal of Power Sources, 2015. **274**: p. 823-830.
6. Chmiola, J., et al., *Anomalous increase in carbon capacitance at pore sizes less than 1 nanometer.* Science, 2006. **313**(5794): p. 1760-1763.
7. Janes, A., et al., *Nanoscale fine-tuning of porosity of carbide-derived carbon prepared from molybdenum carbide.* Carbon, 2009. **47**(1): p. 23-29.
8. Tallo, I., et al., *Nanostructured carbide-derived carbon synthesized by chlorination of tungsten carbide.* Carbon, 2011. **49**(13): p. 4427-4433.
9. Gao, Y., et al., *High power supercapacitor electrodes based on flexible TiC-CDC nano-felts.* Journal of Power Sources, 2012. **201**: p. 368-375.
10. Dash, R.K., G. Yushin, and Y. Gogotsi, *Synthesis, structure and porosity analysis of microporous mesoporous carbon derived from zirconium carbide.* Microporous and Mesoporous Materials, 2005. **86**(1-3): p. 50-57.
11. Presser, V., M. Heon, and Y. Gogotsi, *Carbide-Derived Carbons - From Porous Networks to Nanotubes and Graphene.* Advanced Functional Materials, 2011. **21**(5): p. 810-833.
12. Chmiola, J., et al., *Effect of pore size and surface area of carbide derived carbons on specific capacitance.* Journal of Power Sources, 2006. **158**(1): p. 765-772.
13. Azevedo, R.G., et al., *A SiC MEMS resonant strain sensor for harsh environment applications.* Ieee Sensors Journal, 2007. **7**(3-4): p. 568-576.
14. Iacopi, F., et al., *A catalytic alloy approach for graphene on epitaxial SiC on silicon wafers.* Journal of Materials Research, 2015. **30**(5): p. 609-616.
15. Cunning, B.V., et al., *Graphitized silicon carbide microbeams: wafer-level, self-aligned graphene on silicon wafers.* Nanotechnology, 2014. **25**(32).
16. El-Kady, M.F. and R.B. Kaner, *Scalable fabrication of high-power graphene micro-supercapacitors for flexible and on-chip energy storage.* Nature Communications, 2013. **4**.
17. Escobedo-Cousin, E., et al., *Local solid phase growth of few-layer graphene on silicon carbide from nickel silicide supersaturated with carbon.* Journal of Applied Physics, 2013. **113**(11).
18. Phan, H.P., et al., *Thickness dependence of the piezoresistive effect in p-type single crystalline 3C-SiC nanothin films.* Journal of Materials Chemistry C, 2014. **2**(35): p. 7176-7179.

19. Wang, L., et al., *Growth of 3C–SiC on 150-mm Si(100) substrates by alternating supply epitaxy at 1000°C.* Thin Solid Films, 2011. **519**(19): p. 6443-6446.

20. Cao, Y., et al., *Effect of pre-treatment and nickel layer thickness on nickel silicide/silicon carbide contact.* Applied Surface Science, 2005. **241**(3-4): p. 392-402.

21. Ahmed, M., et al., *Graphene synthesis by thermal chemical vapor deposition using solid precursor.* Journal of Materials Science-Materials in Electronics, 2013. **24**(6): p. 2151-2155.

22. Gulpen, J.H., A.A. Kodentsov, and F.J.J. Vanloo, *Growth of Silicides in Ni-Si and Ni-Sic Bulk Diffusion Couples.* Zeitschrift Fur Metallkunde, 1995. **86**(8): p. 530-539.

23. Stankovich, S., et al., *Synthesis of graphene-based nanosheets via chemical reduction of exfoliated graphite oxide.* Carbon, 2007. **45**(7): p. 1558-1565.

24. Gogotsi, Y., et al., *Nanoporous carbide-derived carbon with tunable pore size.* Nature Materials, 2003. **2**(9): p. 591-594.

25. Rollings, E., et al., *Synthesis and characterization of atomically thin graphite films on a silicon carbide substrate.* Journal of Physics and Chemistry of Solids, 2006. **67**(9-10): p. 2172-2177.

26. Gupta, B., et al., *Evolution of epitaxial graphene layers on 3C SiC/Si (111) as a function of annealing temperature in UHV.* Carbon, 2014. **68**: p. 563-572.

27. Tougaard, S.

28. Iacopi, F., et al., *Orientation-dependent stress relaxation in hetero-epitaxial 3C-SiC films.* Applied Physics Letters, 2013. **102**(1).

29. Zhu, Y.Q., et al., *Ultrathin Nickel Hydroxide and Oxide Nanosheets: Synthesis, Characterizations and Excellent Supercapacitor Performances.* Scientific Reports, 2014. **4**.

30. Ren, B., et al., *Hollow NiO nanofibers modified by citric acid and the performances as supercapacitor electrode.* Electrochimica Acta, 2013. **92**: p. 197-204.

31. Kotz, R. and M. Carlen, *Principles and applications of electrochemical capacitors.* Electrochimica Acta, 2000. **45**(15-16): p. 2483-2498.

Table and Figures

 "A thin film approach for SiC–derived graphene as an on-chip electrode for supercapacitors",

M.Ahmed et al., submitted to Nanotechnology

Table 1. Measured sheet resistance, Raman I_D/I_G values, RMS roughness, number of graphene layers, area and gravimetric capacitance of F_1, F_2, R_1, R_2 and the reference 3C-SiC/Si samples

Samples	Sheet Resistance (Ω square^{-1})	Raman I_D/I_G	RMS Roughness (nm)	Number of Graphene Layers	Area Capacitance* ($\mu F\ cm^{-2}$)	Gravimetric Capacitance* ($F\ g^{-1}$)
F_1	680±10	1.2±0.1[#]	23±2	8.3±0.5	31.8±1.7	50.8
F_2	80±10	1.2±0.1	41±2	13.7±0.5	37.5±2.1	36.2
R_1	80±10	0.7±0.1	66±2	14.1±0.5	69.5±1.5	65.0
R_2	236±10	0.7±0.1	70±2	24.8±0.5	34.4±2.1	18.3
Reference 3C-SiC/Si	$4-7\times10^3$	N/A	3.8±0.8	N/A	6.2±0.9	N/A

*Capacitance obtained at a scan rate of 5 mV s^{-1}
[#] From variation over four sites per sample
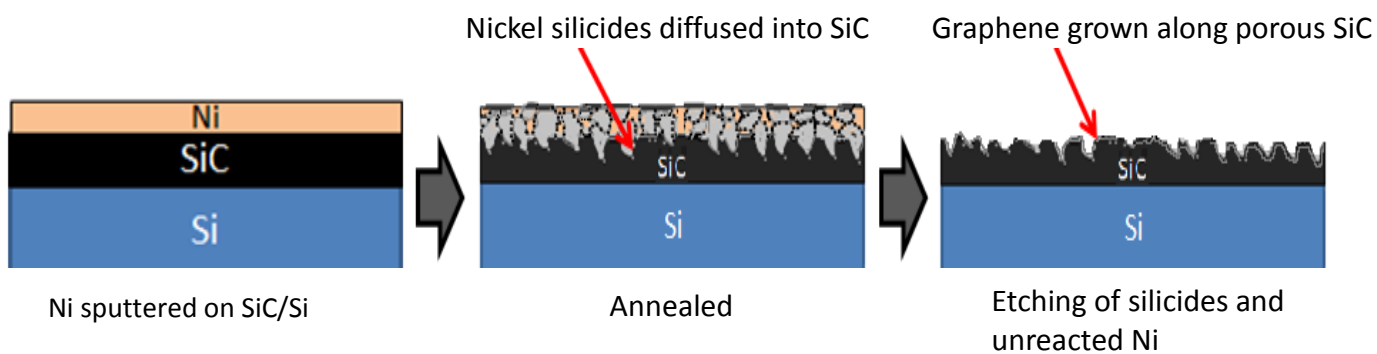
Figure 1. Schematic diagram of the synthesis procedures used to grow graphene on highly corrugated and porous 3C-SiC. First, Ni is sputtered on the 3C-SiC/Si wafer; followed by annealing and formation of silicides and graphitic carbon (graphene) at the 3C-SiC/metal interface; and finally the silicides and unreacted nickel metal are removed by metal etching Freckle solution to expose the graphene on porous 3C-SiC film.
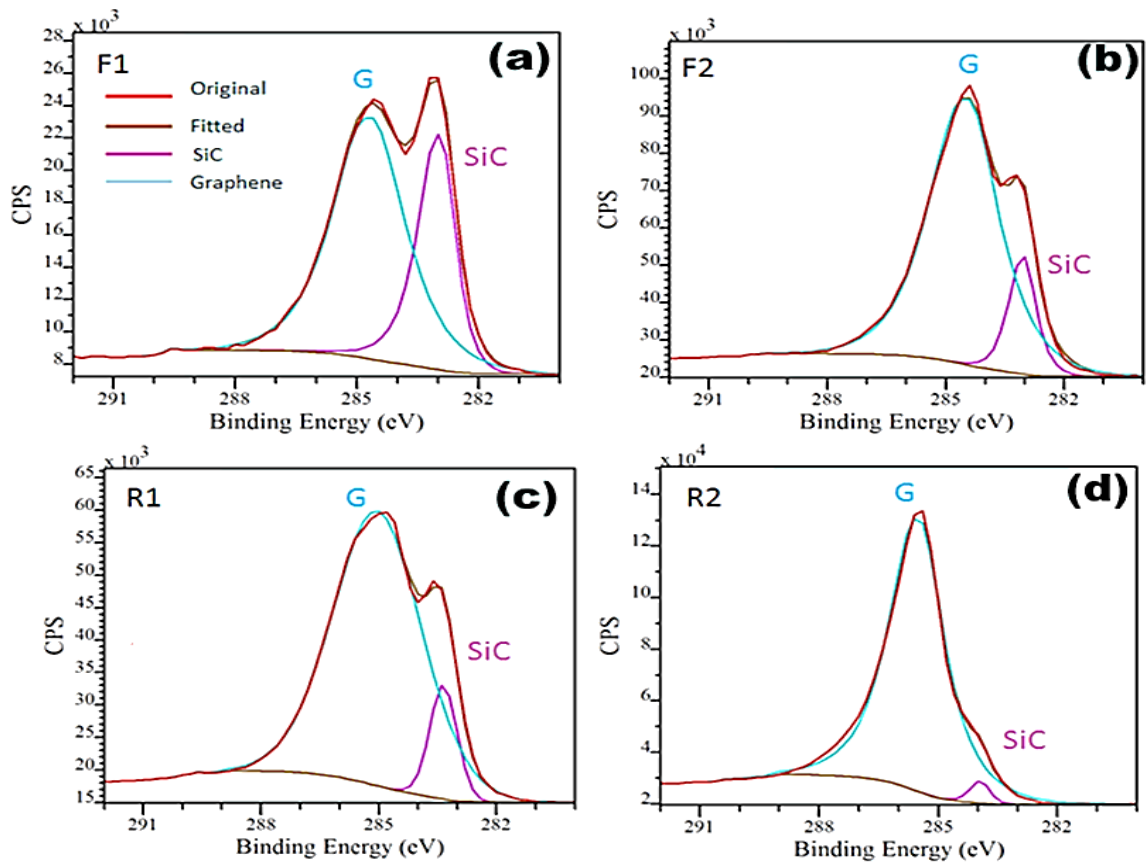
Figure 2. High-resolution XPS C1s spectra of (a) F$_1$, (b) F$_2$, (c) R$_1$ and (d) R$_2$ showing fitting of the graphene and 3C-SiC peaks.
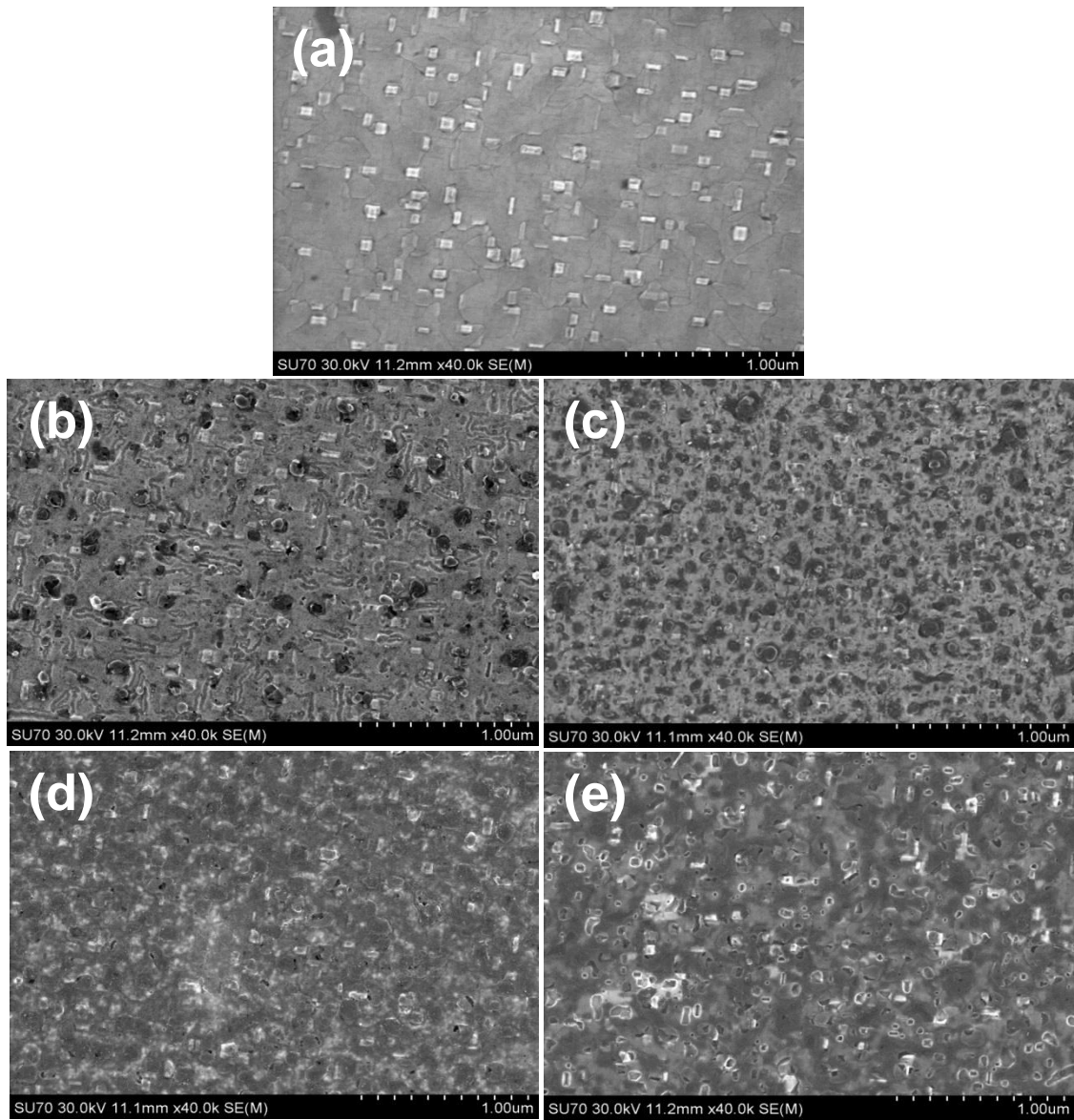
Figure 3. SEM images of (a) a reference pristine 3C-SiC film on Si, and the graphene samples (b) F_1, (c) F_2, (d) R_1 and (e) R_2. Note that extensive pitting is revealed after the nickel – assisted graphene formation.
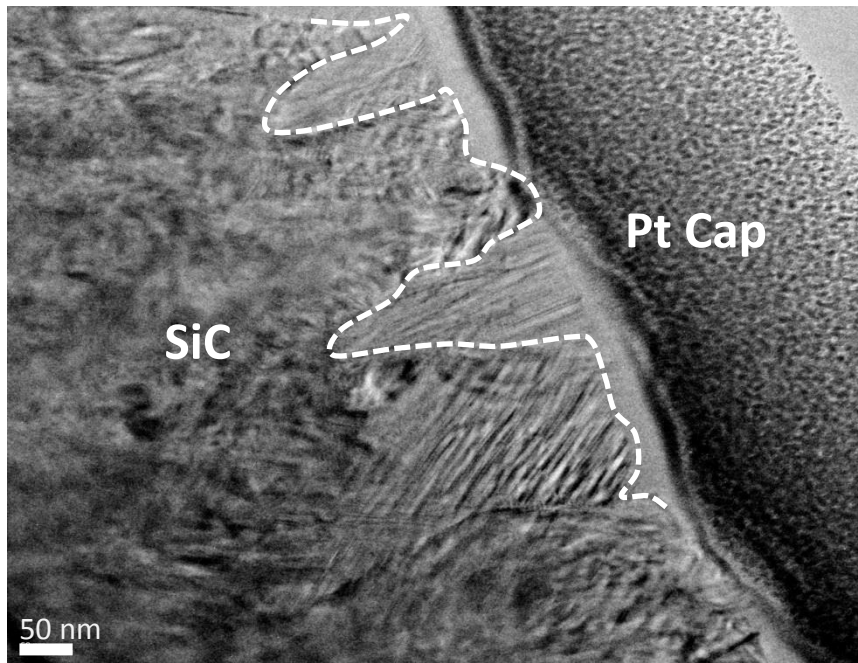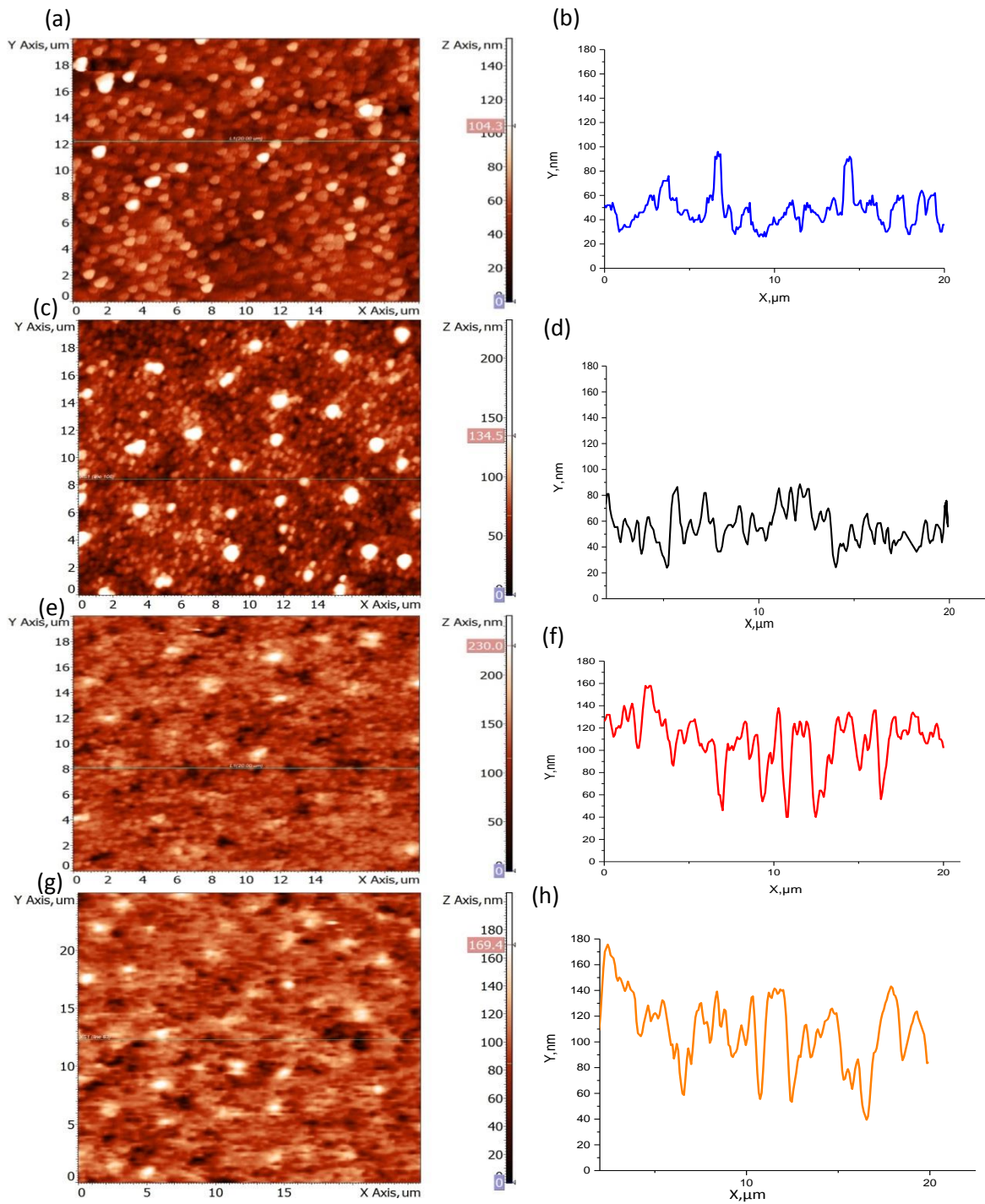
Figure 5. AFM images of (a) F_1, (c) F_2, (e) R_1 and (g) R_2, with their corresponding surface line scan profiles for (b) F_1, (d) F_2, (f) R_1 and (h) R_2. The changes in height indicate the degree of topography induced by the Ni graphitisation process.
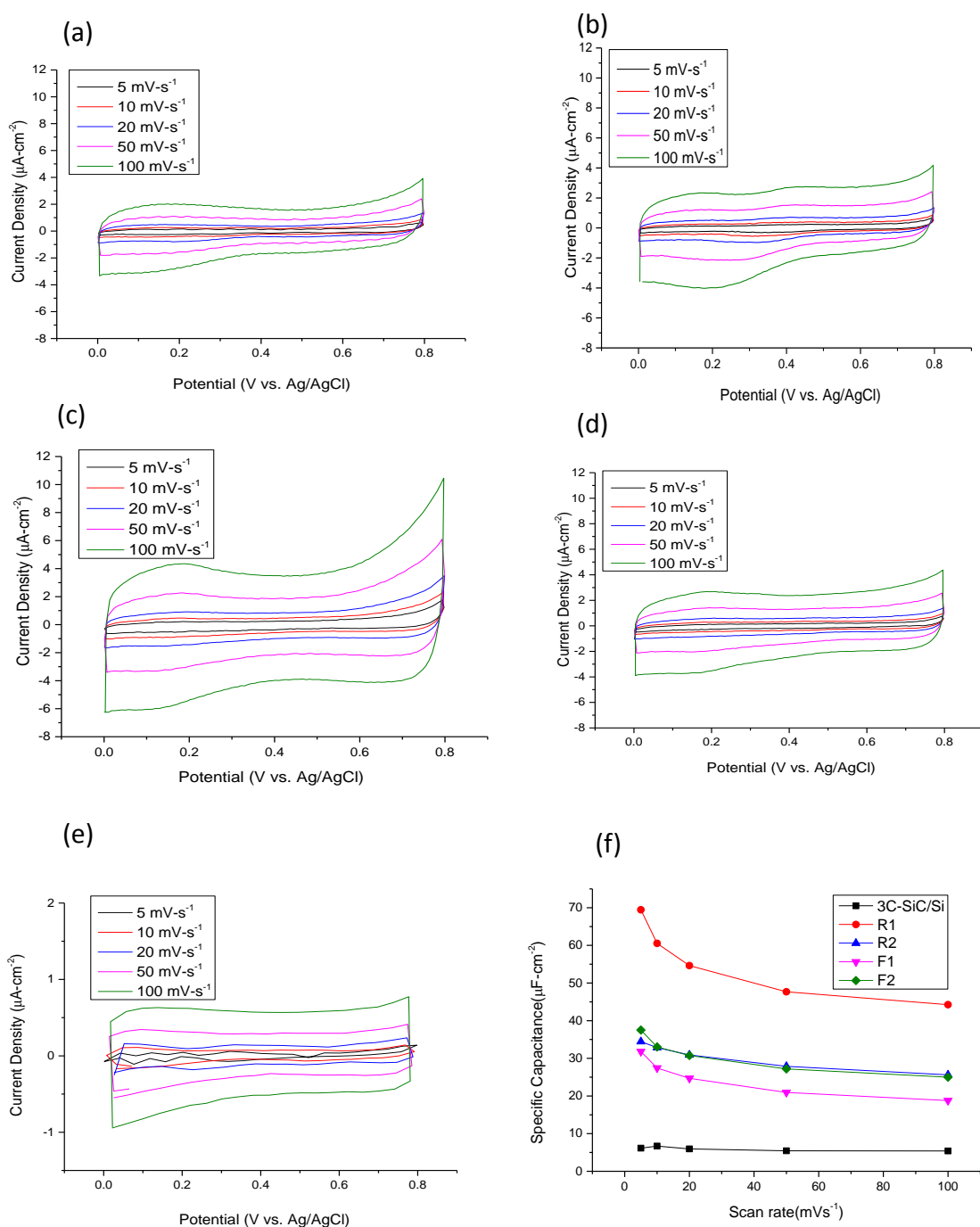
Figure 6. CV curves of (a) F_1, (b) F_2, (c) R_1, (d) R_2, and (e) reference 3C-SiC/Si samples in 3 M KCl at scan rates of 5-100 mV s^{-1} show rectangular shapes; (f) Capacitance vs. scan rates for all samples showing higher capacitances as compared to the reference 3C-SiC sample. Note that the current density axis for the reference sample in (e) is not to scale with the rest of the graphs because of the substantially smaller electrochemical performance.
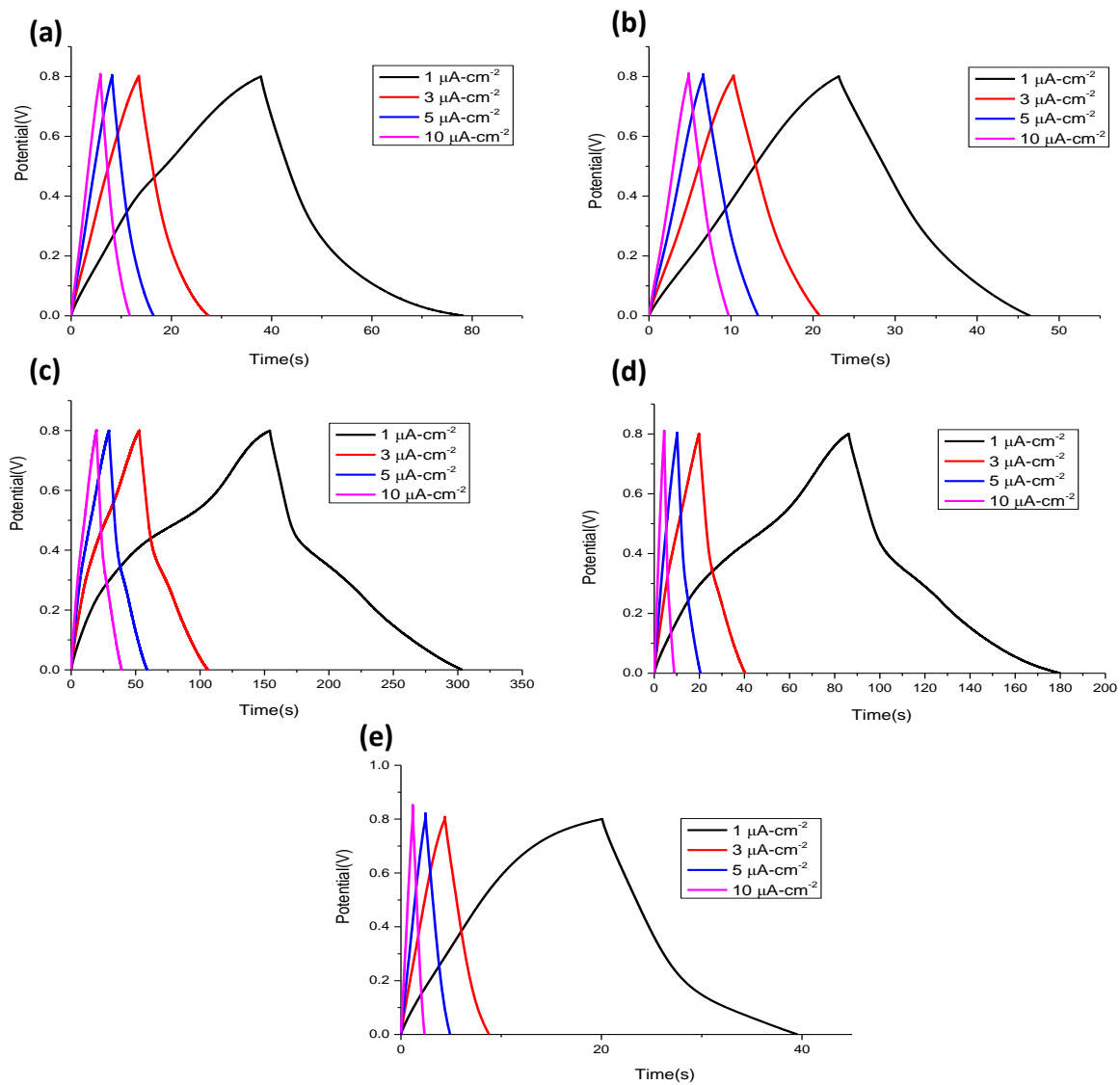
Figure 7. Galvanostatic charge-discharge curves of (a) F$_1$, (b) F$_2$, (c) R$_1$, (d) R$_2$, and (e) reference 3C-SiC/Si samples in 3 M KCl at current rates of 1-10μA cm^{-2} show reversible charge and discharge processes.
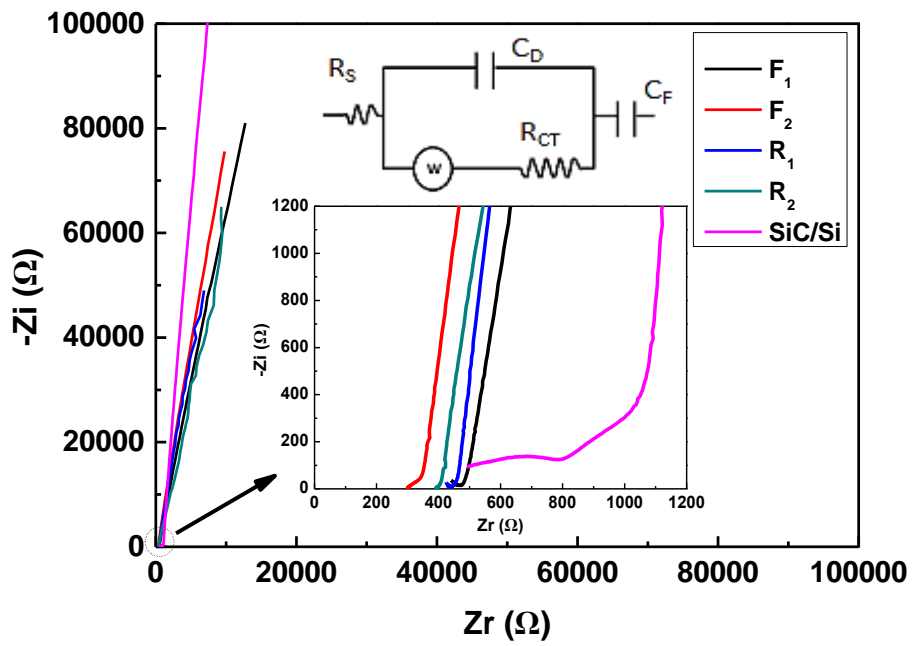
Figure 8. Nyquist plots for graphene samples F_1, F_2, R_1, R_2 and the reference 3C-SiC/Si sample. Inset shows the equivalent circuit and the magnified view of the Nyquist plots at the high frequency region.