A High Efficiency Transformerless PV Grid-Connected Inverter with Leakage Current Suppression

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Abstract—**This paper presents a new diode free freewheeling and common-mode voltage (CMV) clamping branches for single phase transformerless grid connected photovoltaic (PV) inverter for complete leakage current elimination and low conduction losses. In the past, various isolation techniques have been proposed for leakage current elimination in transformerless PV inverters. However, galvanic isolation only cannot completely eliminate leakage current due to that a resonant path is created by the switch junction capacitors, which also generate leakage current. The proposed freewheeling branch consists of four MOSFETs along with a clamping branch, which consists of two MOSFETs and a capacitor divider. The divider is connected to the DC side of the converter to keep constant CMV in the freewheeling path. As a result, the improved CMV clamping has been achieved for complete leakage current elimination. The unipolar sinusoidal pulse width modulation (SPWM) technique and modified HERIC topology with AC-decoupling for galvanic isolation is adopted for lower conduction losses. The proposed topology consists of only MOSFET in the freewheeling and clamping path which provides lower conduction losses compared with diode based topologies. The performances of the proposed topology in terms of common mode characteristics, leakage current, total harmonic distortion and conversion efficiency are analyzed and compared with H5, H6, HERIC and HBZBR topologies. The detail analyses are performed using MATLAB/Simulink and PSIM.**

***Index Terms*—inverters, leakage current suppression, common-mode voltage, photovoltaic systems.**

I. INTRODUCTION

Energy from renewable sources is becoming a common interest of research due to the rapid increase of energy demand and the exhaustion of global resources. Among renewable power sources, photovoltaic (PV) energy source is known as one great alternative all over the world due to the inexhaustible and pollution-free nature of solar power [1]. The integration of PV energy into the power grids is popular now. Therefore, efforts are being made to increase the percentage of energy sourced from PV energy into the grid [2]. However, what discourages PV system from expanding is the cost of the conversion systems due to expensive multi-winding transformer and filters in the grid connected inverter circuit. Therefore, it is important for a PV system to have a low cost and high efficiency grid connected inverter.

Photovoltaic inverter topologies can be classified into the transformerless inverter and the inverter with transformer. Generally, a high frequency and high efficiency transformer is used in the DC side or a low frequency bulky transformer is used in the AC side of the inverter to provide galvanic isolation for leakage current elimination and to avoid DC current injection into the grid. However, additional losses caused by the transformers in the inverter circuit deteriorate the overall system efficiency. Besides, the cost and size of the inverter increase due to use of the transformer. To overcome these problems, a research will be to design a transformerless grid-connected PV inverter. A direct path can be created between the PV module and the utility grid for a transformerless inverter due to nonisolation. As a result, the leakage current can flow from the PV system to the grid. In order to improve the safety and reliability of transformerless PV system, galvanic isolation is the main concern. A high leakage current is generated by the PV stray capacitance and the switch junction capacitance due to charging and discharging operation by the fluctuating common-mode voltage (CMV). According to VDE0126-1-1 standard, the leakage current flow from the PV system to the grid should be carefully handled [3-5].

In order to eliminate the leakage current of the transformerless grid connected inverter due to fluctuating common-mode voltage, a lot of in-depth research works have been conducted [3-10], where the new common mode clamping techniques and freewheeling branches have been proposed to generate constant common mode voltage and to separate the PV array from the grid in the freewheeling period. Several proposed topologies such as H5, H6, HERIC, oH5 and HBZVR can be divided into the AC bypass and the DC bypass based topology to disconnect the PV array and the utility grid in the freewheeling period. However, it is shown in the later section of this paper that the switch junction capacitances have unexpected influence on the leakage current generation. Based on the common-mode behavior of a transformerless inverter as explained in [6, 7], it is important to keep constant common mode voltage by using clamping branches instead of using only freewheeling branches to disconnect the PV module from the grid. Therefore, to completely eliminate the leakage current, common-mode clamping branches have been introduced in oH5 [8], H6 [9, 10], HBZVR [11] topologies, where oH5 and H6 are DC bypass based topology. It can be seen that AC bypass based topologies bring lower conduction losses compared with the DC bypass based topologies due to the minimum switch count in the conduction path during power transfer mode. Furthermore, HBZVR topology cannot completely eliminate the leakage current [3].

In this paper, the leakage current generation mechanism in the single phase transformerless PV inverters is briefly analyzed, and then a modified HERIC-D topology is proposed. The proposed topology consists of an active

common mode clamping branch to keep constant common mode voltage in the whole switching period. In addition, the freewheeling path is modified in the AC side of the inverter to bring the benefit of the low-loss AC bypass based method.

The rest of this paper is organized as follows. Section II describes the principle of leakage current generation in a typical transformerless inverter. In section III, the proposed topology structure and operation principles are described in details. Section IV presents the simulation results. Finally, in section V the conclusions are presented to summarize the findings.

II. Leakage Current Generation Principle

A. Common Mode Behavior

The common mode characteristics of a full bridge transformerless inverter for symmetrical filter inductor is explained in [12]. The typical single phase transformerless H5 voltage source inverter is illustrated in Fig. 1(a), which is used for defining common mode voltage and differential mode voltage and to explain the effect of switch junction capacitance for additional leakage current generation. According to the definition in [12], the common-mode voltage V_{CMV} and differential-mode voltage V_{DM} are as follows.

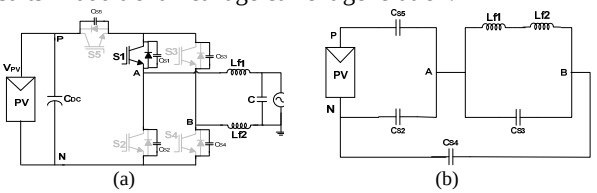
$$V_{CMV} = \frac{V_{AN} + V_{BN}}{2} \tag{1}$$

$$V_{DM} = V_{AN} - V_{BN} \tag{2}$$

where V_{AN} and V_{BN} are the voltages of terminals *A* and *B* to terminal *N*. The leakage current generation in a transformerless inverter depends on V_{AN}, V_{BN}, grid voltage, stray capacitance and filter inductance [12].

B. Switch Junction Capacitance Effect

The switch junction capacitors have unexpected influence to the leakage current generation in the transformerless inverter circuits. In this section, the DC decoupled based transformerless H5 inverter is used to explain the leakage current generation due to the switch junction capacitance effect [6] as shown in Fig. 1(a). During the positive half cycle of the grid voltage, the switches S1, S4 and S5 are in on-state in the power transfer mode while the switches S2 and S3 are in off-state. The switches S4 and S5 are turned off in the next stage to go into the freewheeling mode. However, the antiparallel diode of the switch S3 does not conduct to change the state into the freewheeling mode. As a result, the junction capacitors of the switches S4 and S5 are charged, and the junction capacitors of the switches S2 and S3 are discharged. The charging and discharging operations during freewheeling stage and equivalent circuit are shown in Fig. 1(a) and Fig. 1(b) respectively. The voltage V_{AN} increases due to charging operation while the voltage V_{BN} decreases due to discharging operation. As a result, the common mode voltage V_{CMV} is not constant due to charging and discharging operation, which results in additional leakage current generation.



(a) (b)

Fig. 1 (a) Transient operation of the typical H5 topology, (b) Equivalent circuit [6].

In addition, during the freewheeling operation mode, the switches S1 and S3 are in on-state while all other switches are in off-state. In this mode, terminals *A* and *B* are on floating state, and further a resonant path is formed. As a result, additional leakage current is generated due to high frequency resonant phenomenon occurring in the circuit.

III. Structure and Operation Principle

A. Structure of the Proposed Topology

AC decoupling network based HERIC transformerless inverter circuits do not consist of complete clamping ability. Therefore, additional leakage current is generated due to a resonant path which is created by the switch junction capacitors like H5 topology. In order to avoid resonance circuit to be formed due to floating operation and to maintain constant common-mode voltage by effective clamping, an active clamping circuit has been added. The proposed circuit topology and gate drive signals are shown in Fig. 2 and Fig. 3 respectively. Two clamping switches (S_a and S_b) have been inserted between the midpoints of the two freewheeling branches (S5-S6 or S7-S8) and the midpoint of the series bus capacitors, respectively.

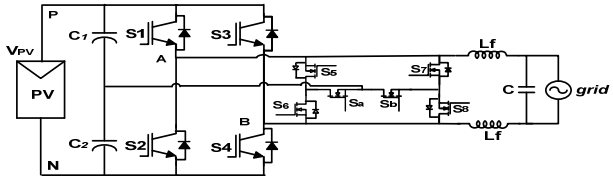


Fig. 2 Proposed topology.

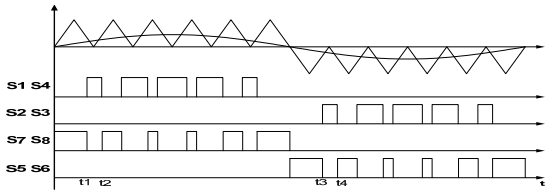


Fig. 3 Gate drive signals of the proposed topology

B. Operation Principles and Analysis

Mode 1: Refer to Fig. 3 and Fig. 4(a). At t_1, the switches S_1 and S_4 are turned on and all other switches are off. At this stage, power flows from the PV to the grid. The current i_L increases linearly until t_2 and flows through the switches S1, S4 and the filter inductor. The inductor current becomes

$$i_L(t) = \frac{V_{PV} - v_{grid}}{L}(t - t_1) \tag{3}$$

The common mode voltage (CMV) becomes

$$V_{CMV} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2}(V_{DC} + 0) = \frac{V_{DC}}{2} \tag{4}$$

Mode 2: Refer to Fig. 3 and Fig. 4(b). At t_2, the main switches S_1 and S_4 are turned off. The freewheeling path switches S_7 and S_8 are turned on to create a freewheeling path during positive half cycle. The current i_L decreases and freewheels through the switch S8 the antiparallel diodes of the switches S_7 and the grid. The inductor current becomes

$$i_L(t) = \frac{-v_{grid}}{L}(t - t_2) \tag{5}$$

The common mode voltage becomes

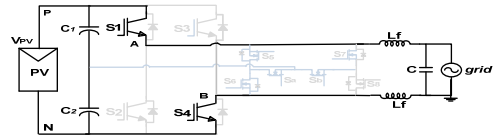
$$V_{CMV} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2}\left(\frac{V_{DC}}{2} + \frac{V_{DC}}{2}\right) = \frac{V_{DC}}{2} \tag{6}$$

Mode 3: Refer to Fig. 3 and Fig. 4(c). In this stage, the switches S_2 and S_3 are turned on and all other switches are off. At this stage, power flows from the PV to the grid. The current i_L increases linearly until t_5 and flows through the switches S_2, S_3 and the filter inductor. The inductor current becomes

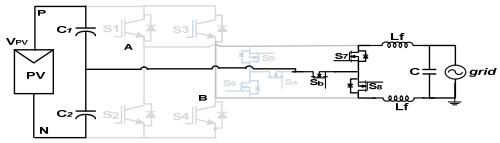
$$i_L(t) = \frac{V_{PV} - v_{grid}}{L}(t - t_3) \tag{7}$$

The common mode voltage becomes

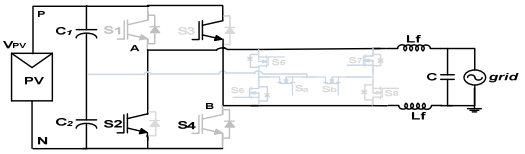
$$V_{CMV} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2}(0 + V_{DC}) = \frac{V_{DC}}{2} \tag{8}$$



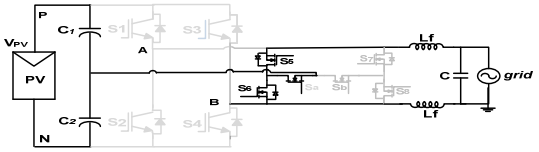
(a) Mode 1- conduction mode



(b) Mode 2- freewheeling mode



(c) Mode 3- conduction mode



(d) Mode 4- freewheeling mode

Fig. 4 Operation modes of the proposed topology

Mode 4: Refer to Fig. 3 and Fig. 4(d). At this stage, the main switches S_2 and S_3 are turned off. The freewheeling path switches S_5 and S_6 are turned on to create a freewheeling path during negative half cycle. The current i_L decreases and freewheels through the switch S6, antiparallel diodes of the switches S5 and the grid. The inductor current becomes

$$i_L(t) = \frac{-v_{grid}}{L}(t - t_4) \tag{9}$$

The common mode voltage becomes

$$V_{CMV} = \frac{V_{AN} + V_{BN}}{2} = \frac{1}{2}\left(\frac{V_{DC}}{2} + \frac{V_{DC}}{2}\right) = \frac{V_{DC}}{2} \tag{10}$$

It is clear that the V_{CMV} is completely clamped to half of the bus voltage during the entire switching period by turning on the active clamping switches.

C. Operation Principle of the Improved Clamping Branch

The clamping switch S_b and the bidirectional switches S5-S6 are turned on when the voltage of freewheeling path drops. Therefore, the common mode voltage is clamped to half of the DC-link voltage through midpoint voltage of the series bus capacitors, which can successfully eliminate the further leakage current generation by resonant circuit effect. Similarly, by turning-on the gate signals of the clamping switch S_a and bidirectional switches S7-S8 when the voltage of freewheeling path increases, the additional leakage current generation can be eliminated. In other words, when the freewheeling voltage is higher than the half of the DC-link voltage, the switch S_a is turned on to clamp the freewheeling path voltage to $V_{DC}/2$. The common-mode current flows through the clamping switch S_a. On the other hand, when the freewheeling path voltage is less than half of the DC-link voltage, the switch S_b is turned on to increase the freewheeling path voltage to $V_{DC}/2$. The common-mode current flows through the clamping switch S_b. As a result, constant CMV is achieved in the freewheeling path during all switching modes and the leakage current is completely eliminated.

IV. Results

In order to compare the overall performance of the proposed topology with existing H5, H6, HERIC and HBZBR topologies, simulation studies have been carried out using MATLAB/Simulink and PSIM with the same parameters. Figs. 5-10 show the simulation results of the output voltage, leakage current and common-mode voltage waveforms for different topologies. Refer to Fig. 5(a), V_{CMV} is not constant and large oscillations are observed up to 350 V for H5 topology. As a result, high leakage current is found as shown in Fig. 5(b). Refer to Fig. 6(a), large oscillations are also observed in CMV for HERIC topology. Therefore, the leakage current is not effectively eliminated as shown in Fig. 6(b). The existing HBZBR topology utilizes common mode clamping technique. However, oscillatory V_{CMV} is observed with the magnitudes up to 500 V as shown in Fig. 7(a). As a result, the leakage current is not completely eliminated which is shown in Fig. 7(b). Refer to Fig. 8(a) and Fig. 8(b), constant V_{CMV} and reduced leakage current are observed for H6 topology. However, four switches conduct during power transfer mode, which reduces the inverter efficiency.

In contrast, the proposed HERIC based inverter topology can effectively eliminate the leakage current during the entire switching period by clamping the common-mode voltage to the midpoint of the series bus capacitors using active clamping technique. The proposed inverter output voltage, output current, V_{CMV} and leakage current are shown in Figs. 9(a) to 10(b) respectively. The V_{CMV} is completely clamped to half of the bus voltage during the entire switching period by turning on the active clamping switches. Therefore, the leakage is eliminated. In addition, the galvanic isolation of the proposed inverter topology is achieved on the AC side of the inverter, which reduces the conduction losses compared with the DC-based galvanic isolation technique due to the reduced switch count in conduction at any switching interval. The output current flows through only two power switches in the freewheeling and power processing interval. The performance comparison among different topologies has been summarized in Table I for 2 kW output power to demonstrate the effectiveness of the proposed transformerless inverter topology. It is clear that the proposed topology gives the best overall performance.

V. Conclusions

A modified HERIC based topology with improved CMV clamping and freewheeling branches for transformerless grid connected inverter has been proposed in this paper. Besides, a comprehensive review, comparison and analysis of several

recently proposed single phase transformerless PV inverter topologies have been presented. The derived topology is an excellent candidate with improved conversion efficiency and minimized leakage current. The topology is obtained by adding six MOSFETS in the AC side of the converter which achieves lower conduction loss compared with other existing diode based topologies and DC-decoupling topologies. The performances of the derived topology in terms of common mode characteristics, leakage current, total harmonic distortion and efficiency are analyzed and compared with those of existing H5, H6, HERIC and HBZVR topologies. It can be concluded that the proposed topology provides the best performances and is suitable for transformerless single phase grid connected photovoltaic inverter.

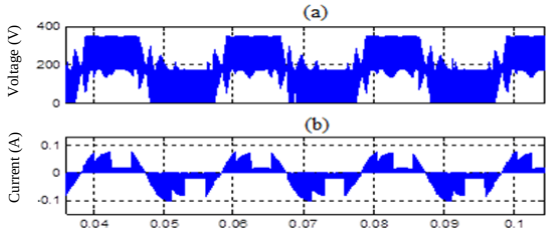


Fig. 5 H5 topology: (a) Common mode voltage, (b) leakage current.

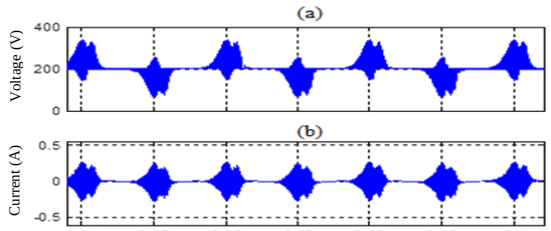


Fig. 6 HERIC topology: (a) Common mode voltage, (b) leakage current.

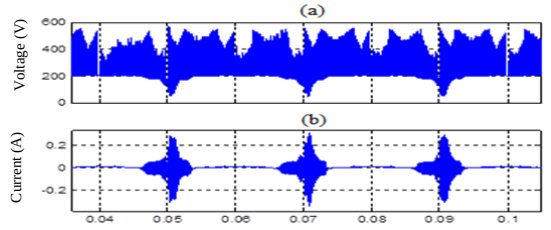


Fig. 7 HBZVR topology: (a) Common mode voltage, (b) leakage current.

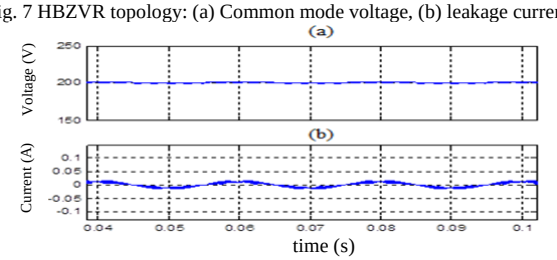


Fig. 8 H6 topology: (a) Common mode voltage, (b) leakage current.

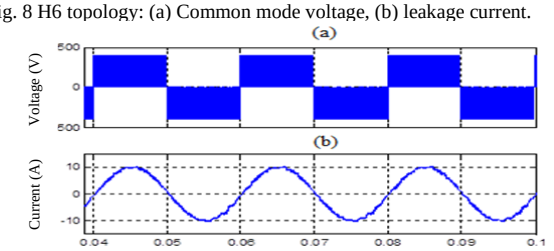


Fig. 9 Proposed topology: (a) Output voltage, (b) Output current,

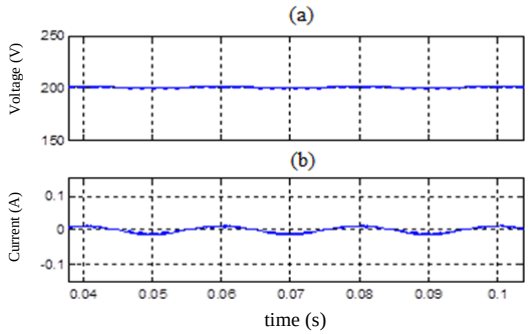


Fig. 10 Proposed topology: (a) Common mode voltage, (b) leakage current.

TABLE I
PERFORMANCE COMPARISON OF TRANSFORMERLESS INVERTER TOPOLOGIES

Topologies	H5	H6	HERIC	HBZVR	Proposed
Leakage current (mA, RMS)	33	7.7	75	19	7.7
Efficiency (%)	98.01	97.5	98.2	98.1	99
THD (%)	3.87	5	3.2	2.8	3.5
Switch count during power transfer mode	3	4	2	2	2
Active switch losses (W)	22.81	27.4	17.13	19.6	16.58

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