FPGA-Based Control of Modular Multilevel Converters: Modeling and Experimental Evaluation

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***Abstract*—In comparison with conventional two level converters, multilevel converters present lower switching losses, lower voltage stress on switching devices, lower common-mode voltages and better harmonic performance. Due to these remarkable features, nowadays the application of this technology covers a wide range, where high-quality voltages and currents are required. However, the multilevel converter requires a number of switching pulse width modulated (PWM) signals, which cannot be generated by using a single digital signal processor (DSP)/microcontroller because the available DSP at present only can provide about 12 PWM channels. In this instance, the field programmable gate array (FPGA) is the natural choice for multilevel converters. In addition, the most common software such as MATLAB/Simulink and Xilinx ISE Design Suite-based alternative design technique is used in this paper, which may reduce the developmental time and cost of the controller. The design and implementation of the switching controller, test platform, and experimental results are analyzed and discussed.**

Keywords—digital switching controller; FPGA; multilevel converters

I. INTRODUCTION

Multilevel converter can provide output voltage with more than three levels and this additional parameter can be used to control the quality of the output voltage waveform. Moreover, the switching frequency can be reduced to a low value with an increase in the number of voltage levels, making the converter more stable and reliable and making it possible to use low rated-voltage, technologically matured and commercially available low-cost semiconductor devices. Therefore, multilevel converter has recently become popular in medium- to high-voltage applications, e.g. tractions, renewable energy conversion, reactive power compensations, high-power rectifiers, and conveyor systems [1]–[5]. However, the multilevel converter requires a large number of pulse width modulated (PWM) gate signals, which depends on the number of levels. For example, a 3-phase *5*-level modular multilevel converter needs 24 PWM gate signals. Fig. 1 shows the power circuit of a 3-phase 5-level converter. The available digital signal processor (DSP)/microcontroller at present can only provide about 12 PWM gate signals, which are not adequate for multilevel converters [2]. Alternatively, the advanced field programmable gate array (FPGA) may provide multiple PWM gate signals according to the system requirements. Moreover, the DSP/microcontroller runs a sequential program in its microprocessor and FPGA runs all the operations in parallel with the clock pulse. Thus, the FPGA may update all gate pulses of the switching controller simultaneously. The ability of parallel operation makes the processing time independent of the number of converter levels. Therefore, the FPGA-based switching control technology could be the first choice for multilevel converters.

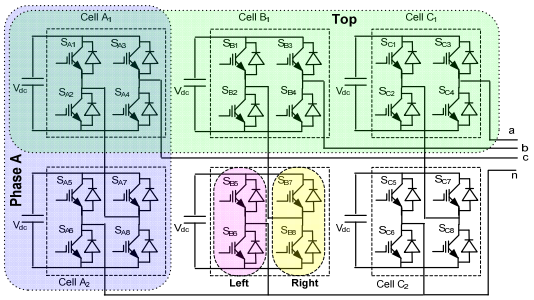

Fig. 1. Power circuit of a 3-phase modular 5-level converter.

Different vendors offer different design techniques and software environments for the modeling of control schemes with the FPGA technology. Allmost all of the available design techniques require costly special software. The uncommon software also increases the development time [6]. In this paper, the most common softwares such as the MATLAB and Xilinx ISE Design Suite are used, which may reduce the developmental time and cost of the control circuit. The simulation results from MATLAB/Simulink can be used to compare the performance of the control circuit in Xilinx ISE Design Suite environment. A switching control circuit for a modular 3-phase 5-level converter is designed with a Xilinx Spartan-3E XC3S500E FPGA. The developed controller is tested with a scaled down 1,200 V laboratory prototype modular 3-phase 5-level converter. The design and implementation of the control circuit, and the experimental results are analyzed and discussed. The design and implementation techniques may be useful for designing any other advanced power converter's switching control circuit.

II. MODELING OF CONTROL CIRCUIT

Two full-bridge cells are on each phase of a modular 5-level converter, as shown in Fig. 1. Each full-bridge cell requires two carrier signals; one for the left half-bridge and its inverted signal for the right half-bridge. One reference signal has to be compared with the two carrier signals. The carrier for each full-bridge cell on a particular phase leg is phase-shifted

by 90°. Fig. 2 shows the block diagram of the digital control circuit for a modular 5-level converter.

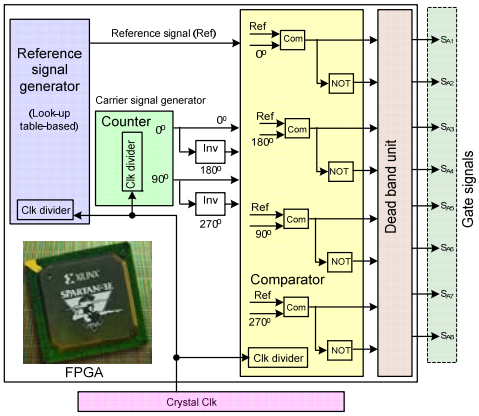

Fig. 2. Control circuit block diagram for a modular 5-level converter.

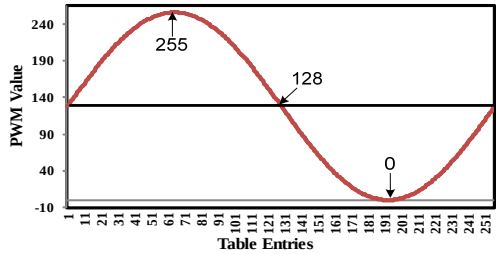

Fig. 3. Reference signal in ISim Simulator environment.

On each phase leg of a modular 5-level converter, there are four half-bridge cells in total. Only two carrier signals are required as the other two can be generated just by inverting them. Each phase of multilevel converter requires a reference signal, whose frequency is the same as the frequency of converter output voltage. The comparator block compares the carrier signal with the reference signal, and generates gate pulses with the consideration of reasonable deadband as required by switching devices, i.e. time required to switch on or off the insulated gate bipolar transistors (IGBTs). The FPGA board has a crystal which can be used for a clock source. The clock divider block reduces the clock frequency. In a single-phase 5-level converter, there are eight IGBTs, requiring eight gate pulses to control them. Four gate pulses can be generated by comparing four carrier signals with the relevant reference signal and the other four gate pulses can be generated by just inverting these four gate pulses with a consideration of reasonable deadband.

A. Reference Signal Generator

A look-up table (LUT) which has a set of memory locations containing the sampled values of analog reference signal is used to generate the sine reference signals. The sample value stored in the LUT can be calculated from [6]

$$S_{LUT}(n+1) = \frac{A}{2} + \frac{A}{2} \times \sin\left(\frac{360^o}{L_i} n + \psi\right) \quad (1)$$

where L_i is the number of entries for a cycle, A the amplitude of the output signal, ψ the phase angle, and n varies from 0 to L_i–1. If the peak value, A, is 255, and L_i 256, the decimal sample values of sine reference signals can be presented as shown in Fig. 3. In order to store the sample values, the decimal numbers are converted to hexadecimal numbers. A very high speed hardware description language (VHDL) code based program is used to create the LUT, which contains the sine reference signal. The following VHDL codes are used to create an LUT and assign 256 sampled values:

```
type memory is array (0 to 255) of std_logic_vector(15 downto
0);
constant Sine_Reference : memory := (
X"8000", X"8324", X"8647", X"896a", X"8c8b", X"8fab",
…….
X"6d38", X"7054", X"7374", X"7695", X"79b8", X"7cdb"
                                        );
```

The clock divider may determine the frequency of the reference signals. To generate a 50 Hz reference signal from 256 entries in LUT using an external crystal, the clock divider value k_R can be calculated from [6]

$$k_R = \frac{Crystal\_frequency}{256 \times 50Hz}. \quad (2)$$

The following VHDL codes may be used to model a clock divider:

```
clk_division : process (clk, clk_divider)
    begin
    if (clk = '1' and clk'event) then
    clk_divider <= clk_divider + 1;
    end if;
    slow_clk <= clk_divider(4);
end process;
```

After comparing the performance of the behavioral model of reference signal generator with MATLAB/Simulink results, a schematic symbol of reference signal generator is created.

B. Carrier Signal Generator

The triangular carrier signals are generated by 9-bit up-down counters. The frequency of the carrier signal should be much higher than that of reference signal. In this paper, 1,500 Hz and 50 Hz frequencies are considered for the carrier and reference signals, respectively. The clock divider value of the up-down counter is calculated from [6]

$$k_C = \frac{Crystal\_frequency}{2 \times 2^9 \times Switching\_frequency}. \quad (3)$$

In total four carrier signals are required for a modular 5-level converter. Only the 0° and 90° phase shifted carrier signals are required to generate as the 180° and 270° phase shifted carriers can be obtained just by inverting the 0° and 90° phase shifted carrier signals. The following VHDL codes are used to generate the 0° and 90° phase shifted 9-bit up-down counters, respectively:

```
signal D  : std_logic_vector(8 downto 0) := (others => '0');
signal D  : std_logic_vector(8 downto 0) := B"100000000";
```

The 0° phase shifted counter (Top_Counter_V_2) is used to generate gate pulse for the left leg IGBTs of top full-bridge cells and the 90° phase shifted counter (Bot_Counter_V_2) is used for IGBTs on the left legs of bottom full-bridge cells.

C. 180° Phase Shifter (Inverter) Unit

The 180° phase shifted counter is used to generate gate pulses for the right leg IGBTs of top cells and the 270° phase shifted counter is used for IGBTs on the right legs of bottom

cells. The following VHDL codes are used to model an 180^o phase shifter or inverter:

```
entity Inverter_9_Bits_V_2 is
        Port ( A : in  STD_LOGIC_VECTOR (8 downto 0);
               B : out  STD_LOGIC_VECTOR (8 downto 0));
    end Inverter_9_Bits_V_2;
    architecture Behavioral of Inverter_9_Bits_V_2 is
    begin
    B <= NOT A;
end Behavioral;
```

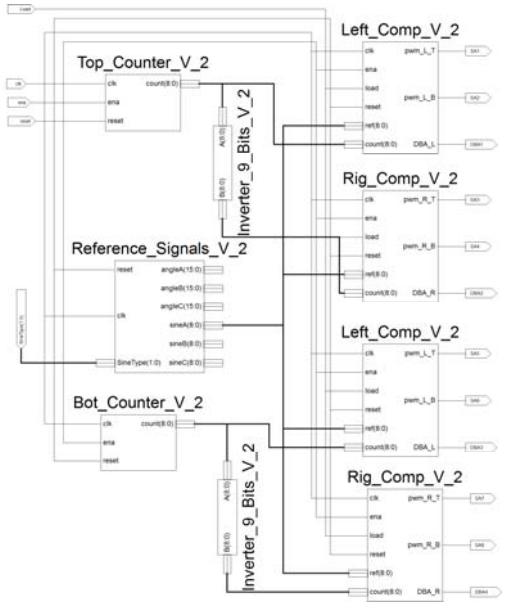

Fig. 4. Control circuit in the Project Navigator environment.

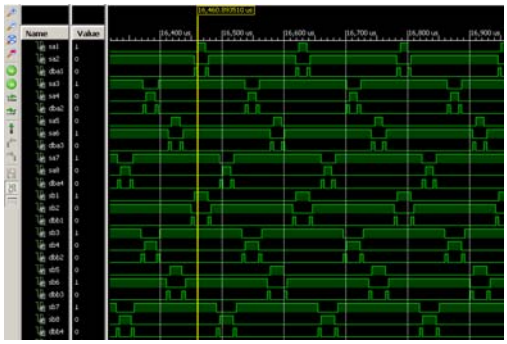

Fig. 5. Gate pules and deadbands in ISim Simulator environment.

D. Comparator Block

The comparator blocks compare the triangular carrier signals with the sine reference signals; whether the reference signal value is greater than or equal to the carrier signal value or the reference signal value is less than the carrier signal value. Each block provides a gate pulse for the top IGBT of the half-bridge cell. The inverted form of this gate pulse switches the bottom IGBT. In order to ensure the safe operation of IGBTs, a deadband is considered between the turning off of one IGBT and the turning on of the other IGBT on a half-bridge leg. One PWM signal is asserted when the carrier signal is greater than or equal to the reference signal plus half of the deadband and the other PWM signal is asserted when the carrier signal is less than the reference signal minus half of the deadband. The following VHDL codes are used to define and implement the deadband concept in ISim Simulator environment:

```
deadband:STD_LOGIC_VECTOR (8 DOWNTO 0) :=
B"000100000"
    top_cmp := conv_integer(compare_value) +
(conv_integer(deadband)/2);
    bot_cmp := conv_integer(compare_value) -
(conv_integer(deadband)/2);
```

The comparator and the PWM gate pulse generator with deadband are simulated by the ISim Simulator and performance are analyzed. A schematic symbol of comparator block is created from the VHDL program based behavioral model.

III. Behavioral Simulation of Control Circuit

A schematic-based switching control circuit is developed in the Project Navigator environment. The control circuit for a single-phase 5-level converter is shown in Fig. 4. The complete control circuit is simulated using the ISim Simulator with the created test bench file. The following VHDL codes may be used to create a test bench file:

```
load <= '1';
ena <= '1';
clk <= not clk after 10ns;
reset <= '0' after 50ns;

  tb : PROCESS (clk, reset)
  BEGIN
   --clk <= '0';
      --WAIT for ClockPeriod/2;
      --clk <= '1';
      --WAIT for ClockPeriod/2;
  END PROCESS;
```

The gate pulse waveforms and deadband wave forms are displayed on the waveform viewer. The gate pulses and deadband waveforms are depicted in Fig. 5. Through the waveform viewer, the performance of the controller is analyzed by comparing with the MATLAB/Simulink results. After analyzing the performance of the behavioral model of the switching control circuit with behavioral simulation, the model is ready for implementation.

IV. Experimental Validation

Synthesized-XST tool is used to synthesize the schematic model of switching control circuit. The input/output ports are assigned according to the available pin configuration of the Xilinx Spartan-3E FPGA development board with the PlanAhead tool. Switching and control signals are assigned to the top row connectors of the Hirose FX2 connector on the development board. The input signals, e.g. the load, enabling and reference type, are assigned to the available four slide switches on the board. The I/O Port Properties based I/O pins are assigned in the Xilinx ISE Design Suite 13.2 software environment. The pin number is entered in the site field in the I/O Port Properties tab when the I/O signal is selected. Once the PlanAhead is closed by selecting the Exit tab, a ucf file is added to the project, which contains the constraints.

The design Summary viewer reports timing constraints, pinout report, errors & warnings and other information. It is essential to check the pinout report carefully especially whether or not all signals have been assigned to the correct FPGA pins. After verification, a configuration bitstream is created for the model. The process tab Generate Programming File can be used to generate a bit file to program the FPGA. The FPGA board is connected with the PC through a standard USB cable on the USB based download/debug port of the test board. The FPGA is programmed using the iMPACT tool under the Configure Target Device process. During the programming process, the device xc3s500e is selected to program the FPGA.

The PWM gate pulses from the FPGA are 3.3 V, which is not enough to drive the IGBTs. Driver ICs TC4427A are used to increase the voltage level to 15 V. Through Hirose FX2 connector and ribbon cables the generated 3.3 V gate pulses are applied to the driver circuit. The experimental test platform is illustrated in Fig. 6. The gate pulses from FPGA and driver circuit are illustrated in Fig. 7. The measured switching frequency of the switching signals is 1,525 Hz, which well matches the theoretical result at 1,500 Hz. The output phase voltage is measured using Tektronix DPO 2024 digital phosphor oscilloscope as shown in Fig. 8. The phase voltage was found highly consistent with MATLAB/Simulink results. Three-phase line voltages were also measured and were found acceptable. Fig. 9 shows measured three-phase line voltage of a modular 5-level converter.

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Fig. 6. Photograph of the experimental test platform.

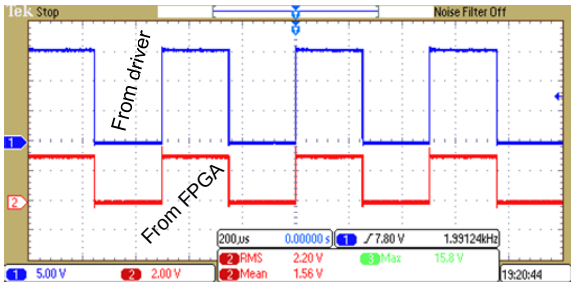

Fig. 7. Measured gate pulses from FPGA and driver circuit.

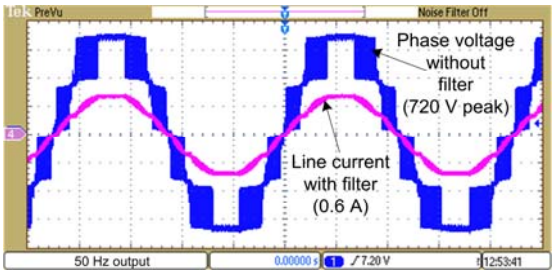

Fig. 8. Measured phase voltage and line current of a 5-level modular converter.

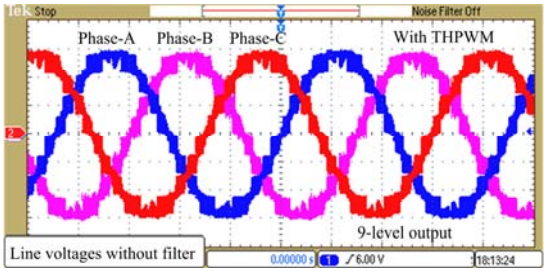

Fig. 9. Measured line voltages of a 3-phase 5-level modular converter.

V. Conclusion

During the behavioral modeling of the switching control circuit in Xilinx ISE Design Suite environment, the MATLAB/Simulink model and its response have been considered as the reference. Finally, the switching circuit has been implemented for experimental verification. The experimental results are found highly consistent with theoretical and MATLAB/Simulink results. This control scheme and design technique can be used for any other converter with minor modifications.

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