A Novel Diode-Clamped Modular Multilevel Converter with Simplified Capacitor Voltage Balancing Control

Abstract— **Multilevel converters have become very attractive for high voltage-level power conversion in renewable power generation applications. The converter topology is an important issue in the studies of multilevel converter. Many multilevel topologies have been developed, but few of them are qualified with capacitor voltage self-balancing capability. This paper proposes a novel diode-clamped modular multilevel converter (DCMMC) with simplified capacitor voltage balancing control. In this topology, low power rating diodes are used to clamp the capacitor voltages of the converter. Only the top sub-module in each arm of the converter requires capacitor voltage control. Consequently, very few voltage sensors are needed for voltage control and the control computation burden is reduced greatly when the quantity of the sub-modules is high. A simple voltage balancing control method with carrier phase-shifted (CPS) modulation strategy is developed for this topology. Experiments based on a laboratory prototype were carried out and the results validated the capacitor balancing performance of the proposed topology.**

Index Terms— **Multilevel converters, diode-clamped modular multilevel converter, capacitor voltage balancing.**

I. Introduction

HIGH voltage-level power conversion and transmission have become very popular for wind power and photovoltaic power generation, since the power scale of a wind farm or a photovoltaic power station is becoming larger and larger, even over hundreds of MWs. And high-voltage AC/DC or DC/AC converters are the basic elements in such applications. With low total harmonic distortion (THD) and low voltage stress on power switches the multilevel converter is a good choice for these applications.

Since 1980, multilevel converters have been developed extensively [1]-[6]. The most famous multilevel converter topologies are the neutral-point clamped (NPC), the flying-capacitor (FC) and the cascaded multilevel converters. It is easy to achieve a three- or five-level converter using the NPC or FC topology. However, numerous clamping diodes and capacitors are required when the voltage levels are high. Furthermore, the capacitor voltage balancing control is difficult and complicated [7]-[10].

With superior modularity and the least component requirement among various multilevel topologies, the cascaded H-bridge (CHB) multilevel converter seems to be the most suitable for medium-voltage active power conversion [11]-[16]. The voltage of the cells is maintained by isolated dc voltage source, which can be supplied by wind turbine generator, photovoltaic-cell, or windings of a multiwinding transformer, etc. However, the requirement of isolated dc voltage supplies and energy storage systems is the shortcoming in some applications. When the CHB converter is applied in reactive power conversion, e.g., STATCOM [17]-[20], the floating capacitor voltage balancing control becomes the most challenging issue.

Over the last decade the modular multilevel converter (MMC) topology as another kind of cascaded topology has gained growing attentions and found itself very attractive for medium/high-voltage applications [21]-[24]. Its modularity and scalability enable it to meet any voltage level requirement [25]-[27]. However, like the CHB topology, the capacitor voltage imbalance distributed in sub-modules (SMs) still remains. Many researchers concentrate on developing control and modulation strategies to solve the problem [27]-[39]. The most widely accepted voltage balancing strategy is based on a sorting method [27]. Li proposed an improved modulation method to balance the capacitor voltages [28]. The control systems rely on voltage sensors installed in all the SMs. In addition, extra switching actions [29] [30] or high execution frequency of voltage sorting algorithms [31] [32] are usually involved, and the situation will deteriorate when the number of SMs is high [33].

In 2001, Peng proposed a generalized multilevel converter [38], which can balance each capacitor voltage automatically without any additional circuits when applied in active or reactive power conversion. From this generalized multilevel converter topology, several other multilevel topologies can be derived including the diode-clamped, capacitor-clamped, cascaded H-bridge, Marx and modular multilevel topologies [39]. However, the quantity of components in the general multilevel converter is too high, which limits its applications in high voltage-level conversion. The Marx multilevel converter was proposed by Rodriguez and Leeb in [40], which can also realize voltage self-balancing at the price of extra active power switches compared with the MMC.

Based on the Marx and modular multilevel converters, this paper proposes a new type of multilevel topology in order to achieve a simplified capacitor voltage balancing method with modularity and good harmonic performance. In this topology, a low current rating diode and an inductor are used to replace the balancing switch installed in each cell of the Marx multilevel topology. We refer this new topology as the diode-clamped MMC (DCM2C). In this topology the number of voltage

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sensors is greatly reduced, and a very simple balancing control method is developed, avoiding high-frequency sorting algorithm and extra switching actions.

The rest of this paper is organized as follows. Section II introduces the DCM2C circuit topology and capacitor voltage balancing control method. The voltage drop distribution in the balancing circuit is then investigated in section III. The power losses and device requirement comparison of MMC and DCM2C are also discussed in this section. Experimental validations of the proposed DCM2C are presented in Section IV. A conclusion is made in section V.

II. Operation Principles of DCM2C

A. Topology of the proposed DCM2C

The generalized multilevel converter was proposed as a primary multilevel topology and many other multilevel topologies can be derived from it. Fig. 1 shows one phase leg of a five-level generalized multilevel converter and its basic cell circuit.

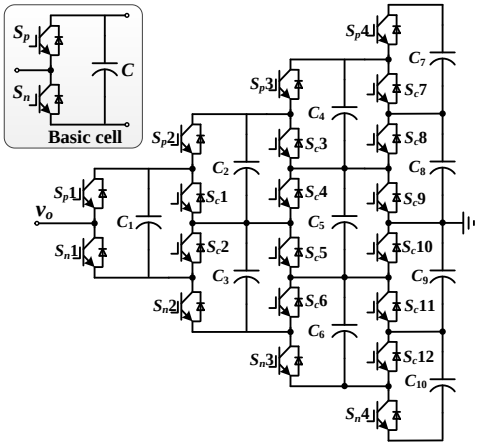


Fig. 1. Generalized multilevel converter (one phase leg, five-level).

The generalized multilevel topology maintains the five-level voltage output by switches S_{p1}-S_{p4} and S_{n1}-S_{n4}. Meanwhile the capacitor voltages are clamped by switches S_{c1}-S_{c12}. For example, when S_{c1} (S_{c2}) switches on, capacitor C_1 and C_3 (C_2) are connected in parallel. If a voltage deviation exists between the two capacitors, balancing current will arise and flow through the clamping switch.

The generalized multilevel topology is redundant and not suitable for practical applications. After removing the upper components, the MMC and the Marx multilevel converter can be obtained, as shown in Fig. 2 and Fig. 3. Compared with the MMC, the Marx multilevel converter uses an extra switch in each SM to realize the capacitor voltage balancing without the requirement of voltage sensors and complicated control methods [40]. Taking SM1 and SM2 as examples, according to superposition theorem, the balancing circuit and its simplified circuit are shown in Fig. 4. C_e is the equivalent capacitance and R_s is the equivalent resistance of power switch. The direction of the balancing current i_{S1} depends on the two capacitor voltage values. The state of switch S is determined by the states of power switch S_{c1} and S_{n2} (logical AND).

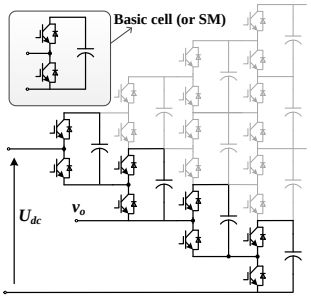


Fig. 2. Deriving MMC from the generalized multilevel topology.

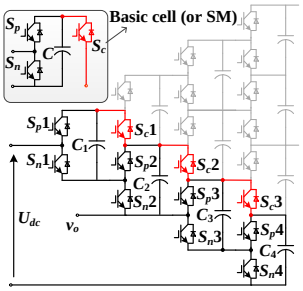


Fig. 3. Deriving Marx converter from the generalized multilevel topology.

In Fig. 4 the circuit parameters can be derived as follows,

$$\begin{cases} C_e = \dfrac{1}{2}C_1 = \dfrac{1}{2}C_2 \\ u_e = u_2 - u_1 \\ i_{S1} = \dfrac{u_e}{2R_s} \\ S = S_{n2} \,\&\, S_{c1} \end{cases} \tag{1}$$

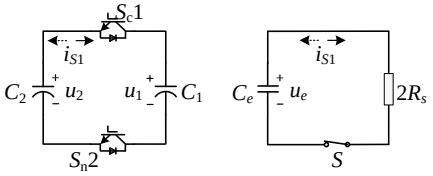


Fig. 4. Balancing diagrams of Marx multilevel converter. (a) Balancing circuit. (b) Simplified circuit.

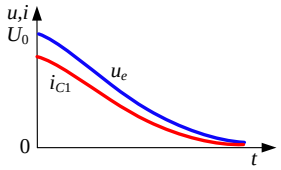


Fig. 5. Voltage and current curves during the charging or discharging process in the Marx multilevel converter.

Fig. 5 shows the voltage and current curves of the equivalent capacitor in the charging or discharging process. The initial value of u_e is U_0. Because R_s is usually very small, the initial amplitude of the balancing current can be large. If the voltage deviation between the neighboring capacitors is big, the balancing current will be very high. This is a common disadvantage of the traditional self-balancing multilevel converters.

Based on the Marx multilevel converter, this paper proposes an improved topology named as diode-clamped MMC

(DCM2C) to replace the extra switch with a low-current rating diode and an inductor, which are called the balancing-branch here. The inductor aims to suppress the peak current during the discharging process. The clamping diodes transfer energy in only one direction, and a simple control method is developed to balance all the capacitor voltages in each arm. The three-phase DCM2C topology is shown in Fig. 6. The balancing circuit and its simplified circuit of SM1 and SM2 in the DCM2C are derived in Fig. 7. The arm inductor L is used to limit the dc-side short-circuit current, meanwhile as a filter for the arm current.

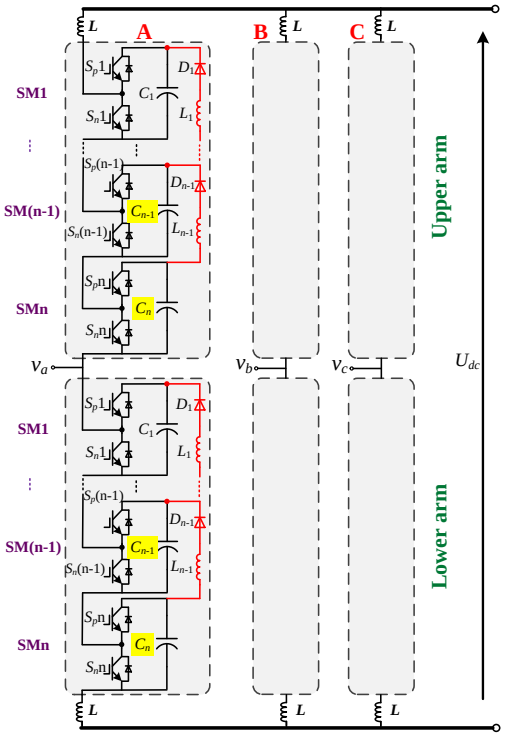


Fig. 6. The topology of three-phase DCM2C.

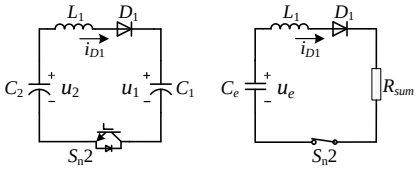


Fig. 7. Balancing diagrams of DCM2C. (a) Balancing circuit. (b) Simplified circuit.

Equation (2) shows the parameters in the simplified circuit. In this circuit only when $u_2 > u_1$, the balancing current i_{D1} can be generated. This means that the initial capacitor voltage u_e is positive. R_{sum} is the sum of the resistance, including R_s of the power switch, R_{di} of the clamping diode and R_{in} of the inductor.

$$\begin{cases} C_e = \dfrac{1}{2}C_1 \\ u_e = u_2 - u_1 \\ R_{sum} = R_s + R_{di} + R_{in} \\ i_{D1} = \dfrac{u_e}{R_e} \end{cases} \tag{2}$$

It can be seen that this is a second-order circuit. The differential equation and its roots, p_1 and p_2, are expressed as (3) and (4), respectively.

$$L_1 C_e \frac{d^2 u_e}{dt^2} + R_{sum} C_e \frac{du_e}{dt} + u_e = 0 \tag{3}$$

$$\begin{cases} p_1 = -\dfrac{R_{sum}}{2L_1} + \sqrt{\left(\dfrac{R_{sum}}{2L_1}\right)^2 - \dfrac{1}{L_1 C_e}} \\ p_2 = -\dfrac{R_{sum}}{2L_1} - \sqrt{\left(\dfrac{R_{sum}}{2L_1}\right)^2 - \dfrac{1}{L_1 C_e}} \end{cases} \tag{4}$$

According to (4), there could be two cases about the relations among the resistance, inductance and capacitance:

$$\left(\frac{R_{sum}}{2L_1}\right)^2 \geq \frac{1}{L_1 C_e} \Rightarrow R_{sum} \geq 2\sqrt{\frac{L_1}{C_e}} \tag{5}$$

$$\left(\frac{R_{sum}}{2L_1}\right)^2 < \frac{1}{L_1 C_e} \Rightarrow R_{sum} < 2\sqrt{\frac{L_1}{C_e}} \tag{6}$$

In the first case, p_1 and p_2 are negative real roots, and a non-oscillatory discharging process will appear. The voltage u_e and current i_{D1} are shown in Fig. 8 (a).

In the second case, p_1 and p_2 are conjugate complex roots, and a damped oscillation discharge process will appear. The voltage u_e and current i_{C1} are shown in Fig. 8 (b). The balancing current i_{D1} is unidirectional due to the clamping diode. When it drops to zero, the discharge process ends with a reversed voltage deviation u_d.

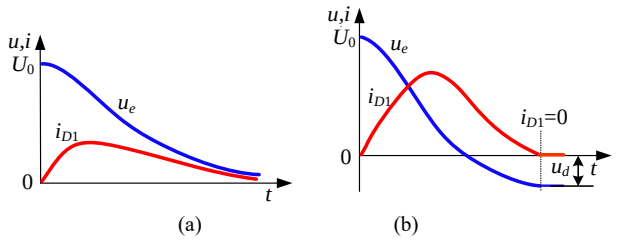


Fig. 8. The voltage and current diagrams of the equivalent capacitor during the discharge process. (a) Non-oscillatory discharge. (b) Damped oscillation discharge.

Fig. 8 illustrates the discharge process with the power switch S_{n2} staying on all the time. Actually with S_{n2} switching on and off alternately, current pulses will be generated and the two capacitor voltages will be balanced in several switching cycles. Fig. 9 shows the capacitor voltage and current diagrams along with the switching signals.

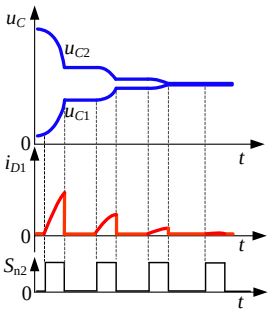


Fig. 9. The voltage and current diagram of the equivalent capacitor during the discharging process.

In each switching cycle when S_{n2} is on, D_1 and L_1 withstand a

voltage of u_{C2} - u_{C1}. If $u_{C2} > u_{C1}$, current i_{D1} will arise and the voltage deviation between the two capacitors will decrease. If $u_{C1} \geq u_{C2}$, no current will arise in the balancing circuit. In the topology of DCM2C the quantity of the cascaded SMs in an arm is n. If u_{Ci+1} is higher than u_{Ci}, C_i will be charged, absorbing energy from C_{i+1}. If u_{Ci+1} is lower than u_{Ci}, no energy transfer happens. As a result, the capacitor voltages of the whole arm will be

$$u_{C1} >= u_{C2} >= \cdots >= u_{Cn} \ . \tag{7}$$

B. *Capacitor voltage balancing control*

In the DCM2C topology, only one voltage sensor is required in each arm for the balancing control, which is installed in SM1. Six current sensors are installed in the upper arms and the lower arms respectively, and two voltage sensors are used to measure the load line-voltages. The upper arm currents, lower arm currents and load voltages are i_{uj}, i_{lj}, u_{ab} and u_{bc} respectively (j = a, b, c).

According to the relations of the arm current direction and the SM states, the capacitor states can be achieved as listed in Table I.

TABLE I
STATES OF CAPACITORS

Arm current direction	SM state	Capacitor state
Positive	On	Charged
	Off	Bypassed
Negative	On	Discharged
	Off	Bypassed

The control strategy for the proposed converter is shown in Fig. 10. The current control is carried out in the d-q coordinate system. u^*_d and u^*_q are the voltage references. The control variables V_j, j=a, b, c, are the modulation signals of the three phase-legs.

According to (7), the capacitor voltages of each arm are clamped in a descending order from SM_1 to SMn automatically. Assume D_{dc} is the dc component of the PWM duty cycles. The relation between the capacitor voltages and the dc bus voltage is

$$\sum_{i=1}^{n} D_{dc} \times u_{Ci,u} + \sum_{i=1}^{n} D_{dc} \times u_{Ci,l} = u_{dc} . \tag{8}$$

$u_{Ci,u}$ and $u_{Ci,l}$ are the capacitor voltages in the upper arm and lower arm respectively. When the unipolar modulation strategy is employed as shown in Fig. 10(d), D_{dc} is 0.5. Then

$$\sum_{i=1}^{n} u_{Ci,u} + \sum_{i=1}^{n} u_{Ci,l} = 2u_{dc} \ . \tag{9}$$

Furthermore, due to the symmetry of the modulation signals for the upper arm and the lower arm, the sum of the capacitor voltages of each arm should be

$$\sum_{i=1}^{n} u_{Ci,u} = \sum_{i=1}^{n} u_{Ci,l} = u_{dc} \ . \tag{10}$$

Combining equation (7) and (10), if the SM1 capacitor voltage is kept to be u_{dc}/n, then all the other capacitor voltages in this arm will be balanced as follows,

$$u_{Ci,u} = u_{Ci,l} = \frac{u_{dc}}{n} \ . \tag{11}$$

A closed-loop capacitor voltage control is carried out for each SM1, as shown in Fig. 10(b). The polarity of PI controller output depends on the direction of arm current, according to Table I.

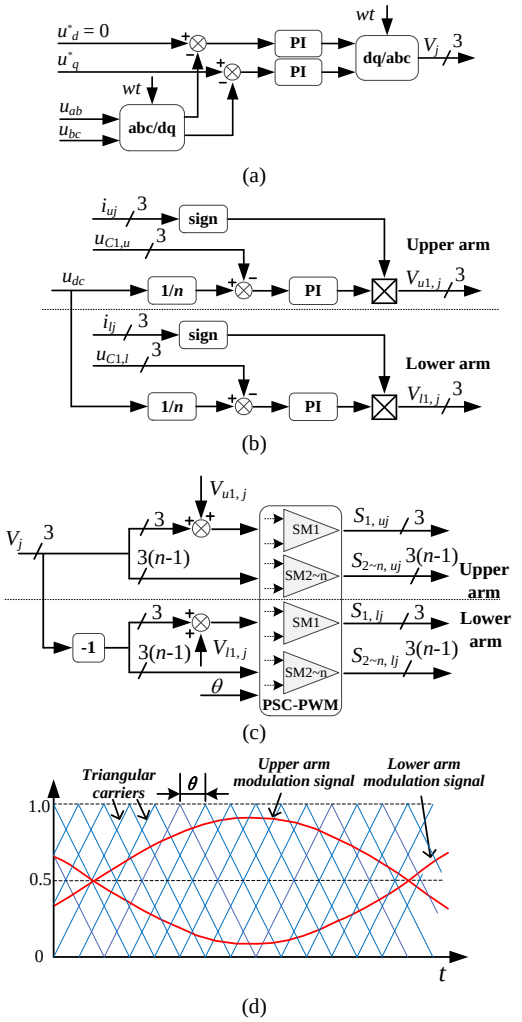


Fig. 10. Control block diagram of DCM2C as an inverter. (a) Load voltage control. (b) Capacitor voltage balancing control. (c) Switching signal generation. (d) PSC modulation.

The PSC-PWM is applied for switching signal generation, as shown in Fig. 10 (c). n triangular carriers with the frequency of f_s are assigned to the n SMs respectively. The SMs share one modulation signal except for SM1: 1) The control variables V_j are the common modulation signals for SM2-SMn. 2) The output of voltage controllers $V_{u1,j}$ plus V_j are the modulation signals for SM1. Fig. 10(d) shows the unipolar PSC-PWM diagram. The phase-shift angle θ is $2\pi/n$, and the upper arm modulation signal is opposite to that of the lower arm. The frequency of carriers is much higher than that of the modulation signals.

III. SPECIFIC CONSIDERATIONS FOR DCM2C

A. *Analysis of the balancing circuit*

In practical operation, both the clamping diode and switch

have the forward on voltage, which should be taken into account, especially when n is high. When the discharge process in Fig. 9 is over, u_{C1} is not always equal to u_{C2}. Fig. 11 shows the device voltage distribution after the balancing current drops to zero.

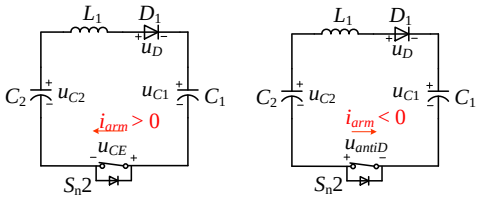


Fig. 11. The voltage distribution in balancing loop when: (a) $i_{arm} > 0$, (b) $i_{arm} < 0$.

The voltage drop across switch S_{n2} depends on the direction of the arm current. Thus the following cases should be discussed.

1) $i_{arm} > 0$: The positive current flows through the IGBT and the voltage drop equals the forward on voltage u_{CE}. u_D is the forward on voltage of the clamping diode. Fig. 11 (a) shows the voltage distribution diagram in this case. According to KVL the voltage equation of this circuit can be derived as follows,

$$u_{C2} = u_{C1} + u_D + u_{CE} \quad . \tag{12}$$

2) $i_{arm} < 0$: The negative current flows through the antiparallel diode in the switch and the voltage drop equals the diode forward on voltage u_{antiD}. Fig. 11 (b) shows the voltage distribution diagram in this case. The voltage equation of this circuit can be derived,

$$u_{C2} = u_{C1} + u_D - u_{antiD}. \tag{13}$$

The values of u_{CE} and u_{antiD} depend on the arm current and the electrical characteristics of the power devices. The value of u_D depends on the balancing current. The deviation between u_{C2} and u_{C1} can be described as follows,

$$u_{Dev} = u_{C2} - u_{C_1} \quad . \tag{14}$$

Substituting (14) into (13) yields the voltage deviation u_{Dev} as follows,

$$\begin{cases} u_{Dev} = u_D + u_{CE}, i_{arm} > 0 \\ u_{Dev} = u_D - u_{antiD}, i_{arm} < 0 \end{cases} \quad . \tag{15}$$

From (15), it can be seen that when i_{arm} is negative the capacitor voltage deviation can be lower than u_D, even eliminated by u_{antiD}.

In addition, the clamping diode should be fast diode, although its switching is softened by the inductor. Because the capacitor voltage deviation is very small in steady state, the current rating of the clamping diode is much lower than that of the main power switch. Generally the power flowing through the balancing circuit equals half of the power difference between the two SMs. Thus the current rating of the clamping diode can be very low, e.g. 10% of that of the main switch. High current pulses may appear in the recovery from a serious imbalance. However, the dynamic recovery process only lasts several switching cycles. Considering that the diode has high surge current withstanding capability, the clamping diodes current rating can still be much lower than that of the main switch. In practical applications the current rating of the diode and the inductor can be determined according to the analysis above.

Voltage deviation between two SMs reflects their power difference, which is mainly caused by the differences of switch losses, modulation and switching signal transfer delay. Adding up the power differences and considering the balanced SM voltage, the average current flowing through the diode and inductor can be derived. When selecting the clamping diode, this current value can be the reference of Average Forward Current I_F. Normally a current margin should be considered. The Maximum Peak Repetitive Reverse voltage value of the clamping diode, V_{RRM}, can be assured by referring to the SM voltage. Thus, the clamping diode selection can be carried out.

In a short time, normally several milliseconds, the clamping diode can suffer from a high current, which is named as the Non-Repetitive Forward Surge Current, I_{FSM}. The I_{FSM} can be obtained from the device datasheet. The current flowing through the diode cannot exceed I_{FSM}, or damage may happen. Therefore, the clamping inductance value should be large enough to suppress the diode current and make its peak value be lower than I_{FSM}. According to the equations of the second-order circuit, the clamping inductance value can be derived by referring to I_{FSM}, balanced SM voltage and switching frequency.

B. Discussion on DCM2C losses

The loss of MMC is consumed by the power switches, parasitic resistance and control circuits. Since the last two parts account for so small proportion of the total losses that they can be neglected, only the power switch loss is investigated.

The loss of power switch contains the IGBT loss P_T and antiparallel switch diode loss P_{aD}. P_T mainly contains the conduction loss P_{Tcon} and switch loss P_{Tsw}. P_{aD} mainly contains the conduction loss P_{aDcon} and recovery loss P_{aDrec}. Similarly the clamping diode loss P_{cD} also contains the conduction loss P_{cDcon} and recovery loss P_{cDrec}.

Then the total loss of a three-phase MMC can be expressed as follows,

$$\begin{aligned} P_{MMC} &= 12n \cdot (P_T + P_{aD}) \\ &= 12n \cdot [(P_{Tcon} + P_{Tsw}) + (P_{aDcon} + P_{aDrec})] \end{aligned} \quad . \tag{16}$$

Compared with MMC, the DCM2C has extra clamping diode loss. Hence, the total loss of DCM2C is

$$\begin{aligned} P_{DCM2C} &= P_{MMC} + 6(n-1) \cdot P_{cD} \\ &= 12n \cdot [(P_{Tcon} + P_{Tsw}) + (P_{aDcon} + P_{aDrec})] + \\ &\quad 6(n-1) \cdot (P_{cDcon} + P_{cDrec}) \end{aligned} \quad . \tag{17}$$

Generally, in the MMC a large proportion of total losses of an SM are the conduction losses of the IGBT and the antiparallel diode, and the total losses of the IGBT are always larger than that of the antiparallel diode [41]. The current flowing through the clamping diode is much lower than the arm current. Hence, the losses of clamping diode are also supposed to be much smaller than that of the IGBT. Then according to (16) and (17), the total losses of MMC and DCM2C are almost the same. The semiconductor losses in MMC can be potentially reduced to be 1% [27], so are the losses in DCM2C.

C. Device requirements of MMC and DCM2C

Table II lists the main device requirements of MMC and DCM2C. The quantity of SMs in each arm is n.

Regardless of the devices which possess the same cost in the two converters, such as the power switches and storage capacitors, the cost difference is mainly related to the clamping diodes, inductors, voltage sensors and capacitor voltage measuring circuit. The DCM2C requires more power diodes and inductors than the MMC, but much fewer voltage sensors and measuring circuits. Additionally, the current rating of the clamping diode and the inductor is much lower than that of the main switches.

TABLE II
COMPARISON OF MMC AND DCM2C

Topology	DCM2C	MMC
Voltage level	$2n$+1 (PSC_PWM)	$2n$+1 (PSC_PWM)
Switches	$12n$	$12n$
Capacitors	$6n$	$6n$
Clamping diodes	$6n$-6	0
Inductors	$6n$-6 clamping inductors + 6 arm inductors	6 arm inductors
Voltage sensors	6 for SM1s + 1for dc-bus	$6n$
Balancing control computation	very low	high

IV. EXPERIMENTAL RESULTS AND DISCUSSION

A three-phase DCM2C prototype has been developed for experiments, as shown in Fig. 12. The parameters are listed in Table III. The control unit is based on DSP (TMS320F28335) and FPGA (EP3C25F324), and as many as 80 optical fibers are used to transmit switching signals, communication and fault signals. Furthermore, a Tektronix scope TDS2024 is used to record the experimental data. In this section, several comparison experiments were carried out to investigate the features of this topology.

TABLE III
PARAMETERS OF THE PROTOTYPE

Items	Symbol	Values
Total number of SMs in each arm	n	6
dc-bus voltage	u_{dc}	600 V
SM capacitance	C	1100 μF
Capacitor voltage	u_C	100 V
Arm inductance	L	200 μH
Switching frequency	f_s	2 kHz
Clamping inductance	L_i	50 μH
Output frequency	f_O	100 Hz
Three-phase load	R_L	12 mH+10 Ω star-connecting

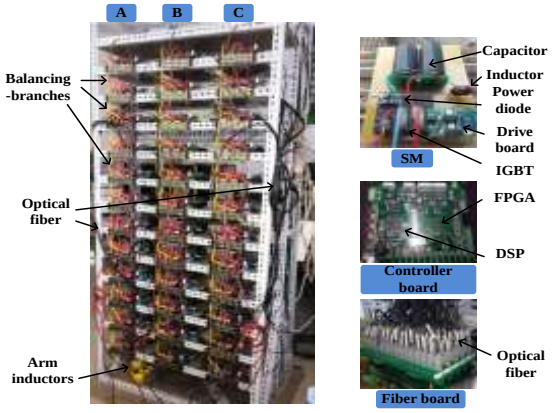


Fig. 12. Three-phase DCM2C prototype.

A. Experiment I: Voltage balancing verification and efficiency test

This experiment aims to validate the effectiveness of balancing-branches of DCM2C. Five relays are used in each arm and each relay is connected with the balancing-branch in series as shown in Fig. 13.

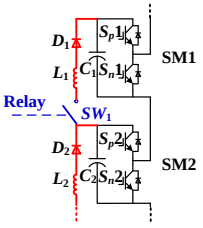


Fig. 13. Using relays to enable or disable the balancing-branches.

When the relays are closed, the balancing-branches are enabled, otherwise disabled. In order to make bigger differences of power losses of the SMs, two 2kΩ-resistors were connected to SM1 and SM6 of the upper arm in parallel with the capacitor and another two 2kΩ-resistors were connected to SM3 and SM4 of the lower arm. The converter started with the relay contacts closed and the capacitor voltages were all well balanced with the maximum capacitor voltage deviation lower than 3 V as shown in Fig. 14. When the relay contacts were opened at t_1 the capacitor voltages became unbalanced quickly until the relay contacts were closed again at t_2. The serious unbalanced capacitor voltages were balanced very quickly as shown in Fig. 14. The capacitor voltages of the upper arm are presented in Fig. 14 (a) and the capacitor voltages of the lower arm are presented in Fig. 14 (b). From the results it can be seen that the capacitor voltage balancing approach of DCM2C is effective.

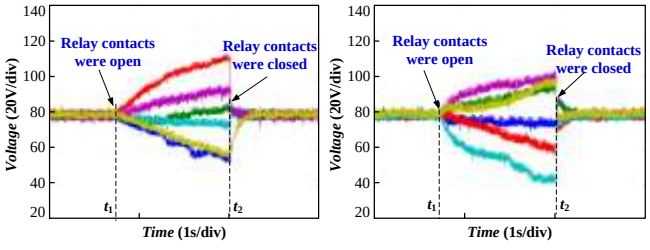


Fig. 14. Experimental results of capacitor voltages in phase a. (a) Upper arm,

u_{C1}~u_{C6}. (b) Lower arm, u_{C7}~u_{C12}.

Remove the 2kΩ-resistors attached to SMs and: 1) Keep the relay contacts open. The operation is similar to that of MMC, so the MMC efficiency based on this prototype can be worked out by calculating the input power and output power. 2) Keep the relay contacts closed and the DCM2C efficiency can be obtained. A three-phase resistance load was applied and Fig. 15 shows the MMC and DCM2C efficiency curves.

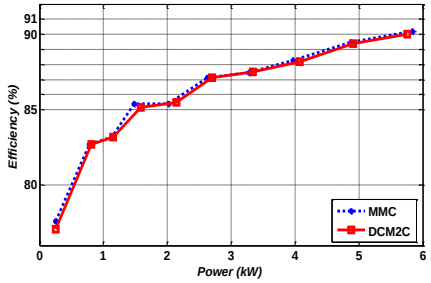


Fig. 15. MMC and DCM2C efficiency curves vs. power.

It can be seen that the DCM2C efficiency is close to that of MMC, and both rise as the output power increases. Limited by the power supply in lab, the dc voltage of an SM is only 100V, far from the maximum voltage of 900V. So the power cannot be very high and the efficiencies are both lower than 91% but still they show the rising trend.

B. Experiment II: Balancing process in detail

This experiment aims to investigate the balancing process with the switch on and off. A voltage deviation, as shown in Fig. 16, existed between SM2 and SM3. When S_n3 switched on, the balancing current pulse appeared with a voltage deviation decrease. When S_n3 switched off, the current dropped to zero. After about 7 ms the deviation was less than 1 V. The initial deviation was about 9 V and the first current peak was about 11 A. Generally the voltage deviation would not be that large in the steady operation.

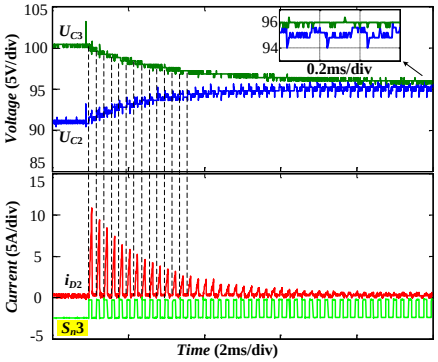


Fig. 16. Experimental waveforms of voltage and current with S_{32} switching on and off, including SM capacitor voltage u_{C2}, u_{C3} and current i_{D2}.

C. Experiment III: Test for balancing capability

An experiment was carried out to test the balancing capability of the DCM2C when the loss difference between the SMs is high. As shown in Fig. 17, a resistor is connected with the capacitor in parallel in one of the SMs of an arm. In this experiment, resistor R_P = 450 Ω is connected to one of the SMs. The output current of the converter is about 15 A (rms) and the reference capacitor voltage is 100 V. Hence, the consumed power in the resistor is 22 W and the power of each SM is about 475 W. In fact the power resistors connected in SM1 and SM6 represent the best and worst situations for balancing performance because of the direction of the diodes. The results in the two cases are presented in Fig. 18 (a) and (b) respectively.

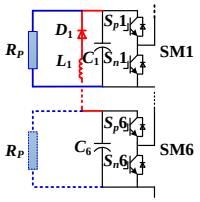


Fig. 17. Using R_P to be connected in SM_1or SM_6 to increase the loss difference.

As shown in Fig. 18, the capacitor voltage deviations between the maximum and minimum in (a) and (b) are about 5V and 7V respectively. The capacitor voltages can still be well balanced when the power difference between SMs is high.

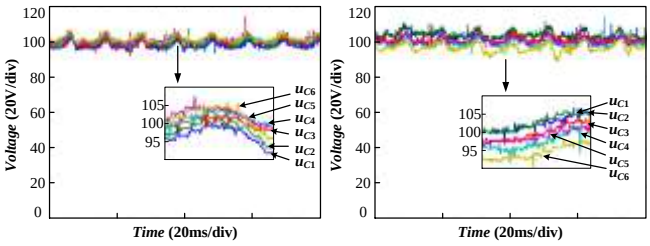
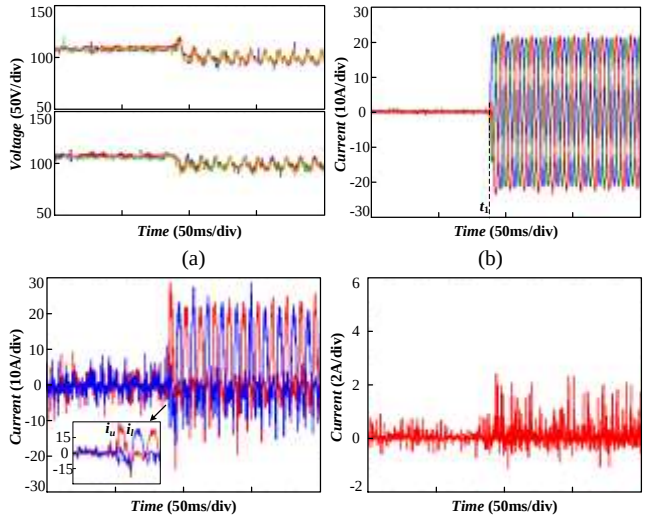


Fig. 18. Experimental results of capacitor voltages with discharging resistor employed. (a) R_P is connected in SM1. (b) R_P is connected in SM6.

D. Experiment IV: Influence of the main circuit current

The output change may affect the capacitor voltage balance, and an experiment of sudden load change has been carried out.



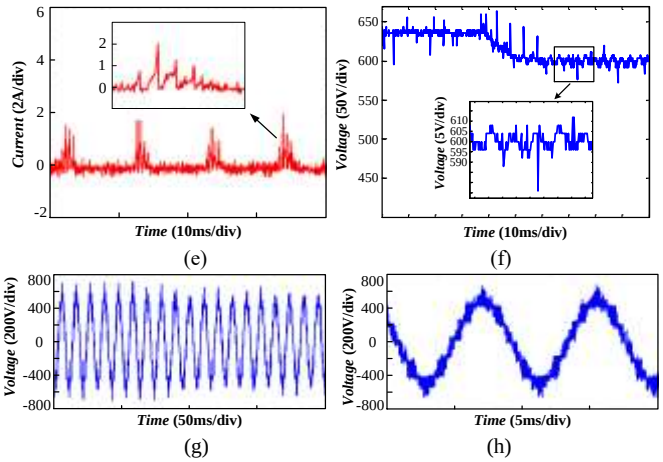


Fig. 19. Experimental waveforms of voltage and current with sudden increase of the load. (a) SM capacitor voltages u_{C1}~u_{C6}, u_{C7}~u_{C12}. (b) Load current i_a, i_b and i_c. (c) Arm current i_u, i_l. (d) Current i_{D1} through clamping diode D_1. (e) Enlarged current i_{D1} after putting the load into operation. (f) DC-bus voltage u_{dc}. (g) Load voltage u_{ab}. (h) Enlarged voltage u_{ab} after the load increased.

The converter started with no load and then the load was suddenly increased as shown in Fig. 19 (b). The capacitor voltage is about 107 V and the load current is about 15 A (rms). Fig. 19 (f) shows the DC-bus voltage when increasing the load. Because of the leakage inductance of the transformer, the output dc voltage of the rectifier circuits had a drop of about 40V. The output voltage of the converter is shown in Fig. 19 (g) and (h).When the load was increased, the capacitor voltage had a drop of about 7 V. After a short dynamic process, the average capacitor voltage was kept at 100 V with about 13 V peak-to-peak ripples, as shown in Fig. 19 (a). But the capacitor voltage deviation was lower than 3 V. Before the load increase the current flowing through the clamping diode was high frequency narrow pulses with amplitude of lower than 1 A (Fig. 19 (d)). This current became higher after the sudden increase of the load, but it was lower than 2A, far lower than the arm current (Fig. 19 (c)). And the average current of the clamping diode is even lower (Fig. 19 (e)). The results illustrate that the capacitor balancing performance can be well maintained in the process of load sudden change and the current of the clamping diode is far lower than that of the main switch. Therefore, the power rating of the clamping diode can be very low.

E. Experiment V: Operation with 50Hz and 20Hz

This experiment aims to validate the effectiveness of the proposed topology when it operates with 50Hz and 20Hz. The load is 15Ω+12mH, star-connection. Due to the limited channels of the scope, only some typical signals are sampled and displayed. Fig. 20 (a) and (b) show the waveforms with 50Hz and 20Hz operation, respectively.

Comparing the results, it can be noted that when the operation frequency is lower, the capacitor voltage ripples become larger. The voltage deviation between SM1 and SM6 also becomes bigger, but still within 5V. The amplitudes of currents flowing through the clamping diode D_1, D_3 and D_5 have no obvious variation, but the occurrence frequency of the current-bumps becomes lower. Due to the enlarged voltage deviation, the width of the bumps, which indicates the energy transfer process, becomes bigger. The experimental results illustrate that the proposed topology can excellently balance the capacitor voltages with variable frequency operation.

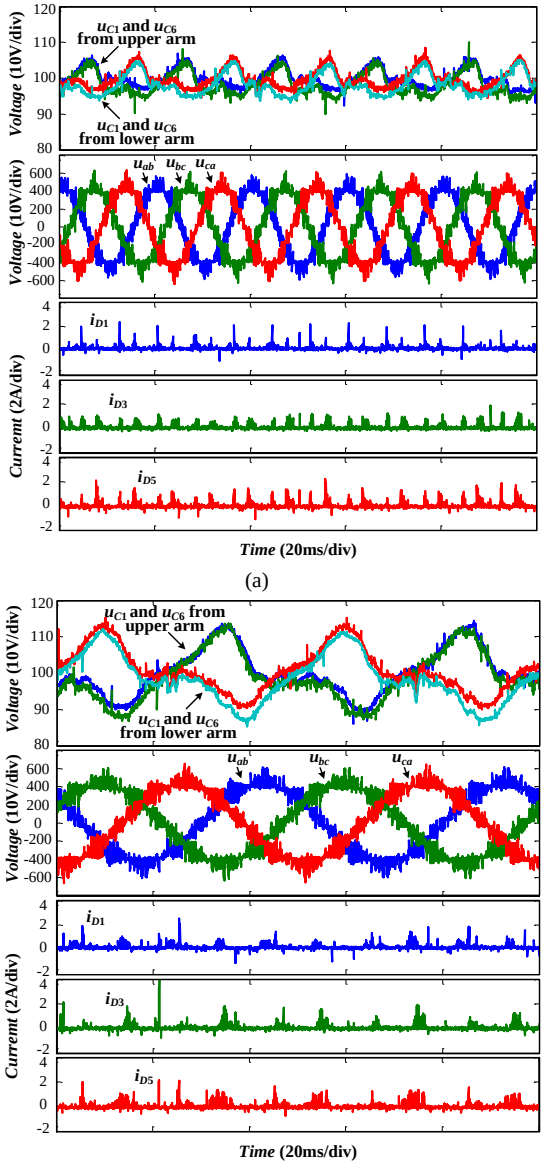


Fig. 20. Experimental waveforms of voltages and currents with: (a) 50Hz operation, and (b) 20Hz operation.

V. Conclusion

Low power rating clamping diode and inductors are used to replace the balancing switch in Marx multilevel converter in this paper, and the diode-clamped modular multilevel converter (DCM2C) is proposed. The capacitor voltage control of the converter is so simple that the computation burden is almost the same with that of the two-level converter. Furthermore, only seven voltage sensors are required in this novel converter topology with any quantity of SMs theoretically. In addition, the current rating of the clamping diodes and inductors is much lower than that of the main switches in the converter. Compared with the MMC structure, the DCM2C requires extra lower

current rating inductors and diodes but much fewer voltage sensors and simplified control circuits. The efficiency of DCM2C is only slightly lower than the MMC's efficiency because the extra losses of the clamping diodes are relatively small. The above proposals have been validated by experiments on a three-phase DCM2C prototype.

This converter can be used in high voltage and high power converting applications such as high voltage direct current transmission, wind power generation, and especially offshore wind power generation.

REFERENCES

[1] A. Nabae, *et al*., "A new neutral-point-clamped PWM inverter," *IEEE Trans., Ind. Appl*., vol. IA-17, pp. 518-523, 1981.

[2] P. M. Bhagwat and V. R. Stefanovic, "Generalized structure of a multilevel PWM inverter," *IEEE Trans. Ind. Appl*., vol. 19, no. 6, pp. 1057-1069, Nov./Dec. 1983.

[3] T. A. Meynard and H. Forch, "Multilevel conversion: high voltage chopper and voltage-source inverters," in *Proc. IEEE PESC*, 1992, pp. 397-403.

[4] M. Carpita and S. Tenconi, "A novel multilevel structure for voltage source inverter," in *Proc. EPE*, 1991, pp. 90-94.

[5] R. W. Menzies, P. Steomer, and J. K. Steinke, "Five level GTO inverters for large induction motor drives," in *Conf. Rec. IEEE IAS Annu. Meeting*, 1993, pp. 595-601.

[6] T. A. Meynard, M. Fadel, and N. Aouda, "Modeling of multilevel converters," *IEEE Trans. Ind. Electron*., vol. 44, no. 3, pp. 356-364, Jun. 1997.

[7] J. S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Trans. Ind. Appl*. vol. 32, no. 3, pp. 509-517, May/Jun. 1996.

[8] A. Bendre, G. Venkataramanan, *et al*., "Modeling and design of a neutral-point voltage regulator for a three-level diode-clamped inverter using multiple-carrier modulation," *IEEE Trans. Ind. Electron*., vol. 53, no. 3, pp. 718-726, Jun. 2006.

[9] B. T. Ooi, G. Hoos, and X. Huang, "Operation principles of shunt STATCOM based on 3-level diode-clamped converters," *IEEE Trans. Power Del*. vol. 14, no. 4, Oct. 1999.

[10] R. Stala, "A natural DC-link voltage balancing of diode-clamped inverters in parallel systems," *IEEE Trans. Ind. Electron*., vol. 60, no. 11, pp. 5008-5018, Nov. 2013.

[11] J. I. Leon, *et al*., "Unidimensional modulation technique for cascaded multilevel converters," *IEEE Trans. Ind. Electron*., vol. 56, no. 8, pp. 2981-2986, Aug. 2009.

[12] K. Anuradha, B. P. Muni, and A. D. Raj Kumar, "Control of cascaded H-bridge converter based DSTATCOM for high power applications," in *Proc. IEEE Power Electronics, Drives and Energy Systems*, 2006, pp. 1-6.

[13] S. Vazquez, J. I. Leon, *et al*., "DC-voltage-ratio control strategy for multilevel cascaded converters fed with a single dc source," *IEEE Trans. Ind. Electron*., vol. 56, no. 7, pp. 2513-2521, Jul. 2009.

[14] H. Sepahavand, J. Liao, M. Ferdowsi, and K. A. Corzine, "Capacitor voltage regulation in single-DC-source cascaded H-bridge multilevel converters using phase-shift modulation," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3619-3626, Sep. 2015.

[15] Z. Du, Knoxville, B. Ozpineci, L. M. Tolbert, and J. N. Chiasson, "Inductorless DC-AC cascaded H-bridge multilevel boost inverter for electric/hybrid electric vehicle applications," *IEEE Trans. Ind. Appl.* vol. 37, no. 2, pp. 603-608, Sep. 2007.

[16] L. Maharjan, S. Inoue, H. Akagi, and J. Asakura, "A transformerless battery energy storage system based on a multilevel cascaded PWM converter," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 4798-4804.

[17] W. Song and A. Huang, "Fault-tolerant design and control strategy for cascaded H-bridge multilevel converter-based STATCOM," *IEEE Trans. Ind. Electron*., vol. 57, no. 8, pp. 2700-2708, Aug. 2010.

[18] R. Xu, *et al.*, "A novel control method for transformerless H-bridge cascaded STATCOM with star configuration," *IEEE Trans. Power Electron*., vol. 30, no. 3, pp. 1189-1202, Apr. 2014.

[19] Z. Liu, B. Liu, S. Duan, and Y. Kang, "A novel DC capacitor voltages balance control method for cascaded multilevel STATCOM,"*IEEE Trans. Power Electron.*, vol. 56, no. 1, pp. 14-26, Jan. 2012.

[20] Y. Cheng, C. Qian, M. L. Crow, *et al*., "A comparison of diode-clamped and cascaded multilevel converters for a STATCOM with energy storage," *IEEE Trans. Ind. Electron*., vol. 53, no. 5, pp. 1512-1521, Oct. 2006.

[21] C. Gao, X. Jiang, Y. Li, Z. Chen, and J. Liu, "A DC-link voltage self-balance method for a diode-clamped modular multilevel converter with minimum number of voltage sensors," *IEEE Trans. Power Electron*., vol. 28, no. 5, pp. 2125-2139, May 2013.

[22] G. Bergna, E. Berne, *et al*., "An energy-based controller for HVDC modular multilevel converter in decoupled double synchronous reference frame for voltage oscillation reduction," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2360-2371, Jun. 2013.

[23] S. Debnath and M. Saeedifard, "Optimal control of modular multilevel converters for low-speed operation of motor drives," in *Proc. IEEE Appl. Power Electron. Conf. Expo*., 2014.

[24] M. Hiller, D. krug, R. Sommer, and S. Rohner, "A new highly modular medium voltage converter topology for industrial drive applications," in *Proc. 13th Euro. Conf. Power Electron. Appl*., 2009, pp. 1-10.

[25] N. Ahmed, *et al*., "HVDC supergrids with modular multilevel converters-the power transmission backbone of the future," in *Proc. Int. Conf. Syst., Signals Devices*, 2012, pp. 1-7.

[26] T. modeer, H. P. Nee and S. Norrga, "Loss comparison of different submodule implementations for modular multilevel converters in HVDC applications," in *Proc. Euro. Conf. Power Electron. Appl*., 2011, pp. 1-7.

[27] S. Debnath, *et al.*, "Operation, control and applications of the modular multilevel converter: a review," *IEEE Trans. Power Electron*., vol. 30, no. 1, pp. 37-53, Jan. 2015.

[28] Z. Li, P. Wang, H. Zhu, Z. Chu, and Y. Li, "An improved pulse width modulation method for chopper-cell-based modular multilevel converter," *IEEE Trans. Power Electron*., vol. 27 no. 8, pp. 3472–3481, Aug. 2012.

[29] J. Mei, B. Xiao, K. Shen, L. M. Tolbert, and J. Y. Zheng, "Modular multilevel inverter with new modulation method and its application to photovoltaic grid-connected generator," *IEEE Trans. Power Electron*., vol. 28, no. 11, pp. 5063–5073, Nov. 2013.

[30] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Del*., vol. 26, no. 3, pp. 2009-2017, Jul. 2011.

[31] K. Ilves, A. Antonopoulos, S. Norrga, and H.-P. Nee, "A new modulation method for the modular multilevel converter allowing fundamental switching frequency," *IEEE Trans. Power Electron*., vol. 27, no. 8, pp. 3482–3494, Aug. 2012.

[32] F. Deng and Z. Chen, "A control method for voltage balancing in modular multilevel converter," *IEEE Trans. Power Electron*., vol. 29, no. 1, pp. 66-76, Jan. 2014.

[33] S. Fan, K. Zhang, J. Xiong, and Y. Xue, "An improved control system for modular multilevel converters with new modulation strategy and voltage balancing control," *IEEE Trans. Power Electron*., vol. 30, no. 1, pp. 358-371, Jan. 2015.

[34] J. Bocker, B. Freudenberg, A. The, and S. Dieckerhoff, "Experimental comparison of model predictive control and cascaded control of the modular multilevel converter," *IEEE Trans. Power Electron*., vol. 30, no. 1, pp. 422-429, Jan. 2015.

[35] F. Deng and Z. Chen, "Voltage-balancing method for modular multilevel converters switched at grid frequency," *IEEE Trans. Ind. Electron*., vol. 62, no. 5, pp. 2835-2847, May 2015.

[36] K. Wang, Y. Li, Z. Zheng, and L. Xu, "Voltage balancing and fluctuation-suppression methods of floating capacitors in a new modular multilevel converter," *IEEE Trans. Ind. Electron*., vol. 60, no. 5, pp. 1943-1954, May 2013.

[37] A. Dekka, B. Wu, N. R. Zargari, and R. L. Fuentes, "A space-vector PWM based voltage balancing approach with reduced current sensors for modular multilevel converter," *IEEE Trans. Ind. Electron*., Early Access 2016.

[38] F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Trans. Ind. Appl*. vol. 37, no. 2, pp. 611-618, Mar./Apr. 2001.

[39] F. Z. Peng, W. Qian, and D. Cao, "Recent advances in multilevel converter/inverter topologies and applications," in *Proc. Int. Power Electronics Conf.*, 2010, pp. 492-501.

[40] J. I. Rodriguez and S. B. Leeb, "A multilevel inverter topology for

inductively coupled power transfer," *IEEE Trans. Power Electron*., vol. 21, no. 6, pp. 1607-1617, 2006.

[41] L. Yang, C. Zhao, and X. Yang, "Loss calculation method of modular multilevel HVDC converters," in *Proc. Electrical Power and Energy Conf*., 2011, pp. 97-101.