Development of a Direct Matrix Converter for Micro-grid Applications

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CERTIFICATE OF ORIGINALITY

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ABSTRACT

Matrix converter is a direct ac-ac converter topology which does not contain a dc-link passive component, unlike conventional ac-ac frequency converters. Electrolytic capacitors which are used as the energy storage component have a limited lifetime. They are also bulky and unreliable at very high temperatures. Matrix converter is able to generate controllable sinusoidal ac outputs regarding magnitude and frequency directly from an ac power supply. The other significant advantages offered by matrix converters are the capability of regeneration and adjustable input power factor.

The main objective of this thesis is design, implementation and the stability analysis of the matrix converter for power flow control applications in the context of the microgrids. In this regard, different applications with bidirectional or unidirectional power flow capabilities are considered as the case study. These include using the matrix converter as an interface link between a microgrid and the utility grid, between a variable frequency source such as wind turbine and the microgrid ac bus, and between a variable frequency load such as induction machine and microgrid ac bus.

As bidirectional power flow control between the utility grid and the microgrid is significantly affected by the stability issue, the stability analysis has become an essential part of this research. Details of the input filter design are presented due to the considerable effect of the filter components on the system stability. The effects of the system parameters on the matrix converter stability are investigated using the

small-signal model of the converter. Two methods of stability improvement using the damping resistor and the digital filter are studied in detail. In order to increase the efficiency of the converter, an optimum solution based on the combination of the damping resistor and the digital filter is suggested, and the performance of the proposed method is analyzed. The operation of the matrix converter as an interface between the utility and a microgrid for bidirectional active and reactive power flow control is studied in detail. To control the active and reactive bidirectional power flows, a vector-oriented control method is used.

Two main modulation strategies, the Venturini and space vector modulation, are analyzed and the simulation and experimental results are compared. Due to the better performance of the space vector modulation, this technique is selected for modulation of the designed matrix converter. Different current commutation methods are studied in detail and the simulation and experimental results of four-step semisoft current commutation are presented as the selected commutation method in this work.

Furthermore, a comprehensive simulation study is carried out to investigate the operation of the proposed strategies for modulation, protection, stabilisation and bidirectional power flow control of the matrix converter. To validate the proposed stability analysis and numerical simulations, a prototype direct matrix converter has been developed. The simulation results related to each of the research sections are confirmed through the experimental tests.

Contents

LIST OF SYMBOLS

q	Voltage gain
i_x, i_y, i_z	Instantaneous output currents, A
v_x, v_y, v_z	Instantaneous output voltages, V
i_A, i_B, i_C	Instantaneous input currents, A
L_f	Input filter inductance
C_f	Input filter capacitance
R_f	Resistance of the input filter inductance
ω_{coff}	Cut-off frequency of the input filter
ζ	The damping factor of the input filter
R_d	Damping resistance
R_s	Line resistance
L_s	Line inductance
L_l	Load inductance
R_l	Load resistance
C_c	Clamp capacitance
$\tilde{\beta}_i$	Phase angle of the input current vector
$\tilde{\alpha}_o$	Phase angle of the output voltage vector
$i_i(t)$	Instantaneous input current, A
$v_{si}(t)$	Instantaneous output voltages, V
$v_{im}(t)$	Input voltage amplitude, V

$I_{im}(t)$	Input current amplitude, A
$v_{om}(t)$	Output voltage amplitude, V
$I_{om}(t)$	Output current amplitude, A
P_i	Input power
P_o	Output power
φ_i	Input displacement angle
φ_o	Output displacement angle
PF_{in}	Input power factor
ω_i	Input angular frequency
ω_o	Output angular frequency
S_{kj}	Switching function of a single switch
m_{kj}	Duty cycle of the switch S_{kj}
t_{kj}	Conduction time of the switch S_{kj}
T_s	Switching period
$v_{o,ref}$	Output reference voltage
k_i	Input current sector
k_v	Output voltage sector
f_i	Input frequency
f_o	Output frequency
f_s	Switching frequency
$\vec{V_o}$	Output voltage space vector
$\vec{I_i}$	Input current space vector
P	Active power
Q	Reactive power

LIST OF ABBREVIATIONS

ac	alternative current
ac	direct current
ADC	Analog to Digital Converter
BBVSC	Back-to-Back Voltage Source Converter
CD	Current Direction
CSR	Current Source Rectifier
DB-VSI	Diode-Bridge Voltage Source Inverter
DAC	Digital to Analog Converter
DMC	Direct Matrix Converter
DSP	Digital Signal Processor
DSVM	Direct Space Vector Modulation
FCC	Forced Commutated Cycloconverter
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
IC	Integrated Circuit
IGBT	Insulated-Gate Bipolar Transistor
ILMC	Inverting Link Matrix Converter
IMC	Indirect Matrix Converter
ISVM	Indirect Space Vector Modulation
LPF	Low-Pass Filter

MC	Matrix Converter
NCC	Naturally Commutated Cycloconverter
OC	Over Current
OV	Over Voltage
PC	Personal computer
PCB	Printed Circuit Board
PF	Power Factor
PI	Proportional and Integral
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
RBIGBT	Reverse Blocking Insulated-Gate Bipolar Transistor
rms	root mean square
SMC	Sparse Matrix Converter
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
TL	Threshold Level
USMC	Ultra Sparse Matrix Converter
VHDL	Very high peed integrated circuit Hardware Description Language
VOC	Voltage Oriented Control
VSI	Voltage Source Inverter
VSMC	Very Sparse Matrix Converter
3LVSI	Three-Level Voltage Source Inverter
ZOH	Zero Order Hold

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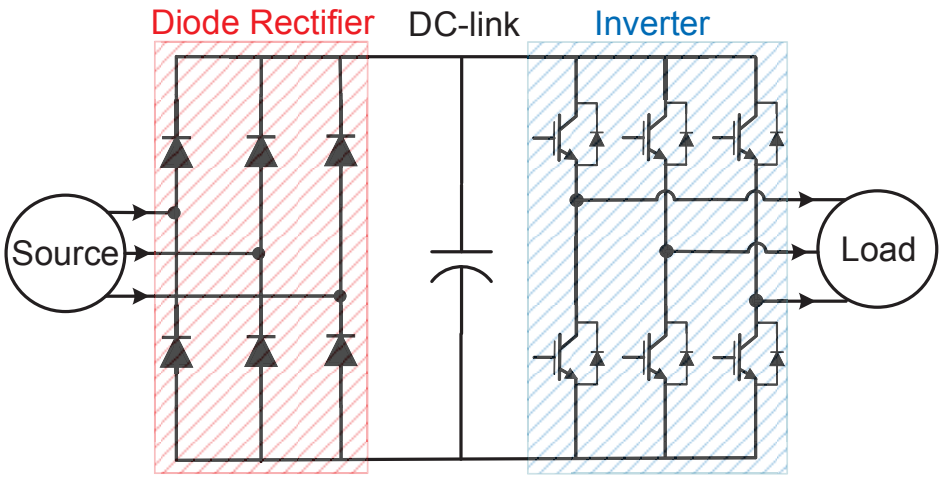
Chapter 1

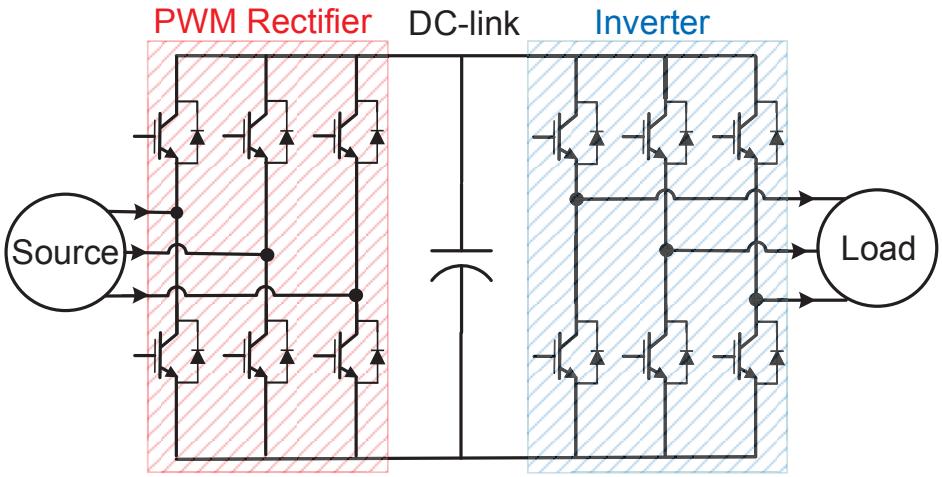
INTRODUCTION

1.1 Power Electronic Converters

Power electronic converters are utilised wherever electric power needs to be converted from alternative current (ac) to direct current (dc) or vice versa. They are also used for converting any level of dc to another level, and for converting frequency or amplitude of ac supplies. The primary task of power electronic converters including rectifiers (ac-dc), inverters (dc-ac), cycloconverters and MCs (ac-ac) and choppers (dc-dc), is supplying voltages and currents in a form that suit for user loads. Modern power electronic converters are involved in a wide range of applications like renewable energy conversion systems, vehicular technology and motor drives. Power converters include two fundamental modules which are the power stage, and the control stage [12]. The electronic circuit of the power stage is formed with high power handling semiconductor devices plus passive devices. Moreover, a digital electronic circuit controls the switching devices according to a specific strategy to obtain desirable quantities like voltages and currents at the input or output. Applications of the converters increased quickly since the first commercial power semiconductors were developed in the 1950s. This thesis is mainly focused on the MC as an ac-ac converter, so in the following text ac-ac converters are introduced. ac-ac converter topologies can be classified into two main categories, indirect and direct power converters. Next sections provide a brief review on the some of indirect



(a)



(b)

Figure 1.1: ac-ac indirect power converter, with the intermediate $dc-link$ stage a) With diode bridge on the supply side (DB-VSI) b) back-to-back voltage source converter (BBVSC)

and direct ac-ac converter topologies.

1.1.1 Indirect ac-ac power converter

The most common ac-ac converters are the indirect ac-ac power converters which consist of a rectifier at the supply side following by an inverter at the load side as shown in Figure 1.1. At first, the rectifier circuit converts the ac power of the input supply to dc power, and then, the dc voltage is converted back to an ac voltage by the inverter circuit. An intermediate dc-link interfaces the rectifier stage to

the inverter stage. These converters are able to generate controllable sinusoidal ac outputs regarding magnitude and frequency from an ac supply [13].

The scheme shown in Figure 1.1a represents the diode-bridge voltage source inverter (DB-VSI) topology that is suitable for ac drive applications, especially in the low- and medium-power range. This scheme is simple to implement and is a low-cost solution. Although, the input ac currents drawn by the rectifier side contain a large number of low-order harmonics that produces distortion in the input line voltages. This problem causes additional harmonic losses on the utility system and also has a negative impact on the other equipment connected to the input source. In addition, as the current direction of a diode rectifier cannot be reversed, the converter cannot be used in applications requiring a regenerative operation. Instead of the diode bridge, an IGBT bridge is used as the rectifier stage, and the converter is known as the back-to-back voltage source converter (BBVSC) that was introduced in 1978 [14] and is illustrated in Figure 1.1b. The PWM rectifier improves input current waveforms, and bidirectional power flow is possible as well [15]. Compared to the diode bridge, the PWM rectifier improves the input power factor, although it is more complicated and expensive. For reducing the voltage stresses of the semiconductors, a three-level voltage source converter (3LVSC) introduced by increasing the number of voltage levels as shown in Figure 1.2 [16]. The drawback of the 3LVSC is the number of active switches which is twice the DB-VSI.The complexity of the system increases more by replacing the diode bridge with a two level rectifier, however, the output voltages are smoother, and the voltage stress of the switches decrease by this method [16].

The above-mentioned ac-ac converters need a large energy storage element in the dc-link. Electrolytic capacitors which are used as the energy storage component have a limited lifetime. They are also bulky and unreliable at very high temperatures. In some applications like aerospace applications, these converters do not suit because of their size, weight and reliability. In order to eliminate the need for a bulky dc-link energy storage element, the direct ac–ac power conversion technology was introduced

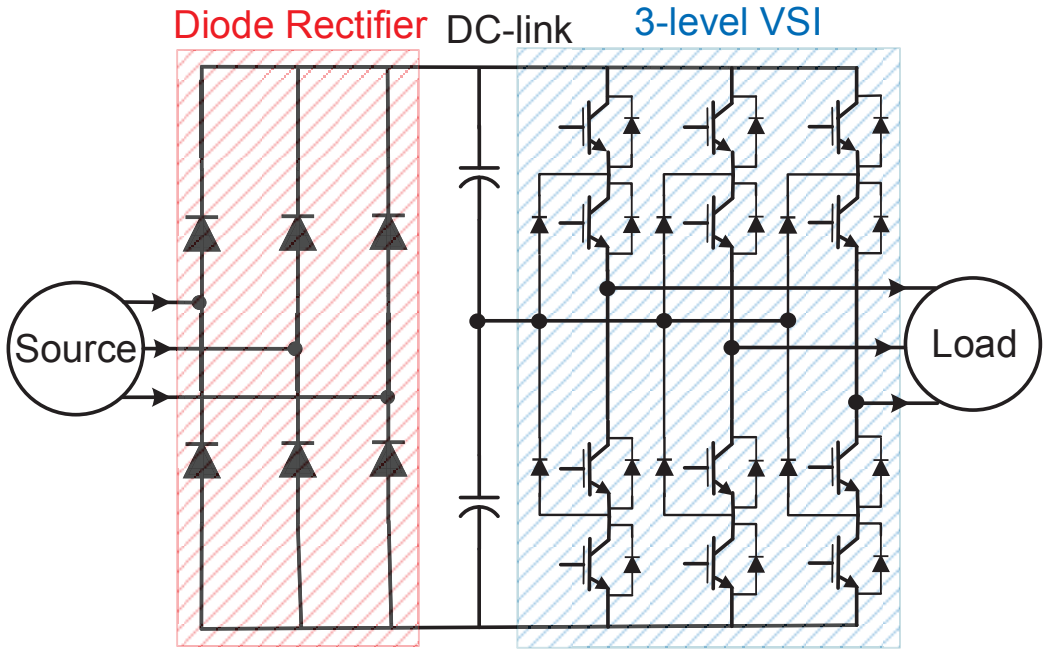


Figure 1.2: ac-ac indirect power converter, with the $dc-link$ stage and 3LVSI on the output side

as will be reviewed in the next section. In [17–21] comparisons between MC and back-to-back converter have been made.

1.1.2 Direct ac-ac power converter

As illustrated in the previous section, indirect ac-ac converters consisting of dc link elements, are heavy, large and subject to ageing. In the direct conversion schemes, ac-ac power conversion is carried out directly without the need of energy storage elements. The first semiconductor-based direct frequency converters were the cycloconverters which developed using the thyristors. In naturally commutated cycloconverter (NCC) the switches are naturally turned off by the voltages of the ac power supply. In this case, the input currents and output voltages are very distorted, the output frequency is lower than half of the input source frequency, input power factor is quite poor, and the voltage transfer ratio is less than unity [22]. Although, compared to the indirect ac-ac converters, NCC is more compact and

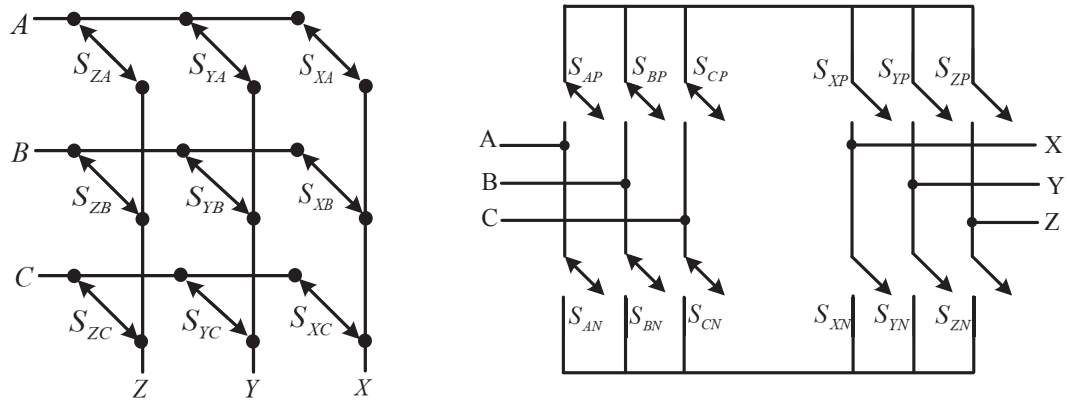


Figure 1.3: ac-ac direct power converters a) DMC b) IMC

allows bidirectional power flow. The NCCs are still used for high power levels which semiconductor devices like IGBTs are no longer applicable.

The forced commutated cycloconverter (FCC) or matrix converter (MC) developed by fully controlled power semiconductor devices. MCs provide the ability of transformation of amplitude and frequency of ac supplies, without an intermediate dc-link [23], although they still require passive components for the input filter and protection circuit. MCs are also able to generate sinusoidal supply currents and adjustable input power factor irrespective of the load [24]. Using high switching frequencies allow the output frequency to be higher than the input frequency. Fully controlled bi-directional switches enable the MCs to connect the input side and the output side directly without the energy storage element, and as a result, they have a more compact design and more lifetime [25–33].

The MC topologies can be classified as direct matrix converter(DMC) and indirect matrix converter (IMC) as presented in Figure 1.3 [34]. In case of the DMC, it includes nine bidirectional switches and each switch includes two IGBT switches connected in common-collector or common-emitter configurations. On the other hand, IMC includes six bidirectional switches in the rectifier stage and six IGBTs in the inverter stage as presented in Figure 1.4. The conventional converters for both schemes include 18 semiconductor switches and 18 diodes which the diodes can be

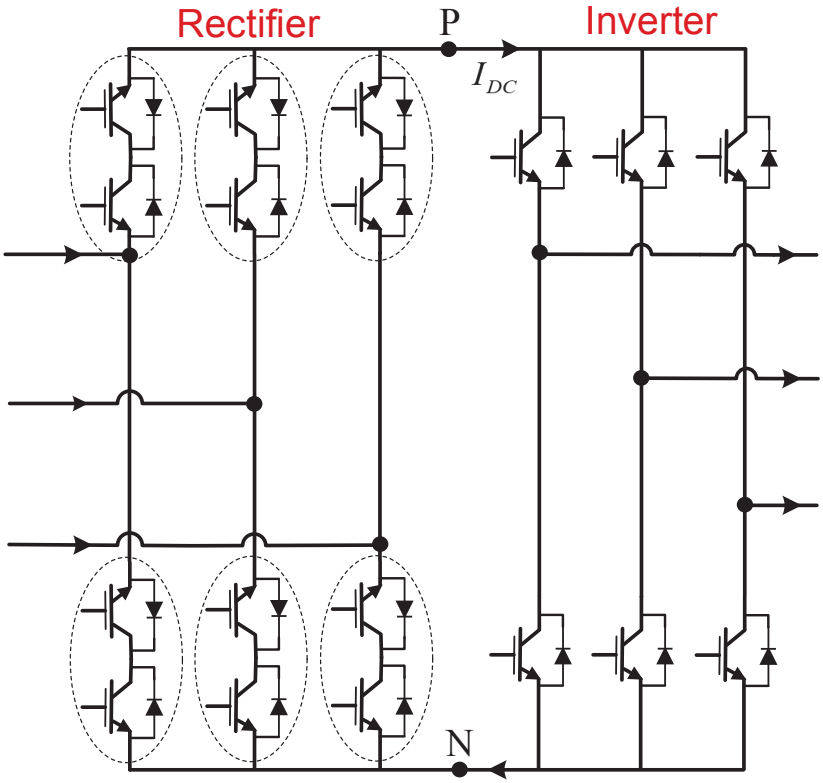


Figure 1.4: Schematic of the Indirect Matrix Converter (IMC)

included in the switches. The number of the switches can be reduced in IMC and denoted as Sparse Matrix Converter (SMC). There are different topologies of the SMCs including, Sparse, Inverting Link, Ultra Sparse,Very Sparse and as shown in Figures 1.5 to 1.8. For example, the three-phase SMC employs only 15 IGBTs, and this is reduced to 9 IGBTs in Ultra Sparse Matrix Converter (USMC) [35].

The basic configuration and control of three-phase DMC were introduced by Venturini [36–38] and consists of nine bidirectional switches as shown in Figure 1.3a. There are different modulation and control strategies for MCs including, pulse width modulation, direct torque control, predictive control, scalar techniques and some other methods [39].

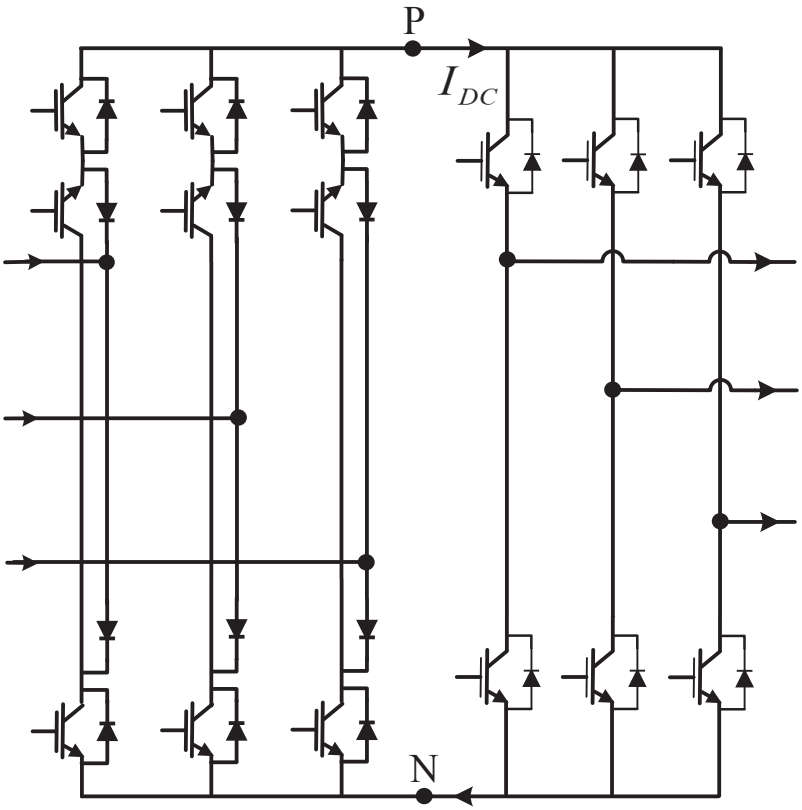


Figure 1.5: Schematic of the sparse matrix converter (SMC)

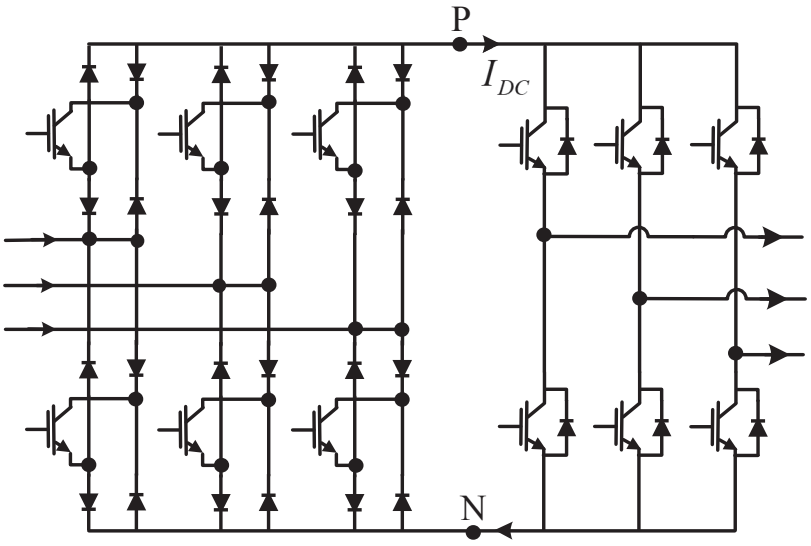


Figure 1.6: Schematic of the very sparse matrix converter (VSMC)

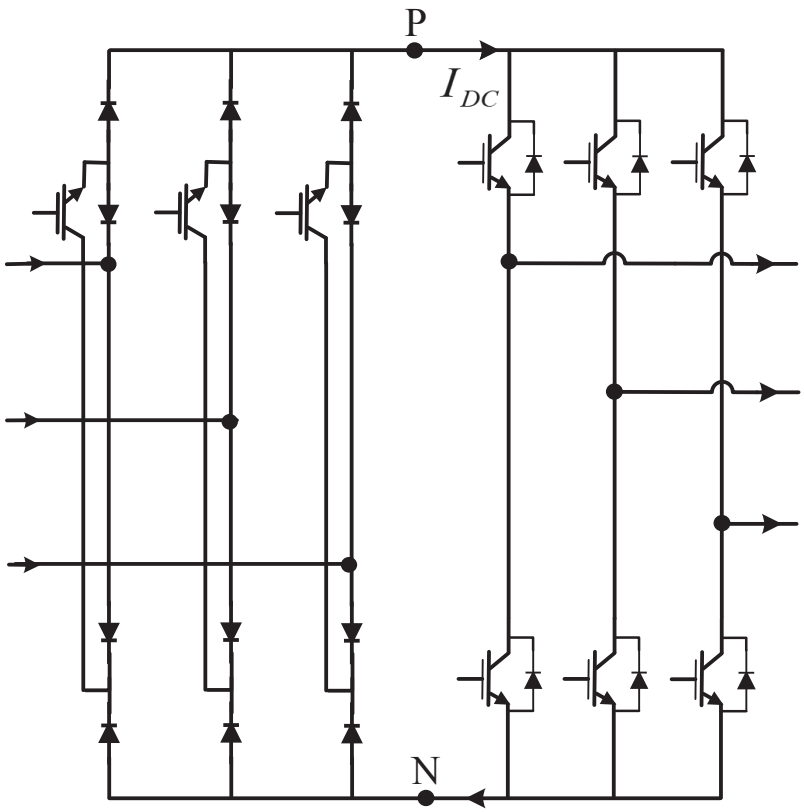


Figure 1.7: Schematic of the ultra sparse matrix converter (USMC)

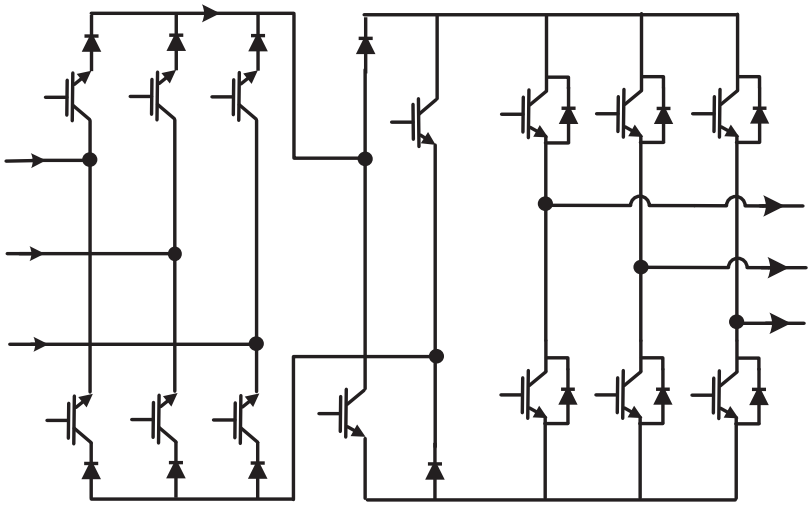


Figure 1.8: Schematic of the inverting link matrix converter(ILMC)

1.2 A Review on the Matrix Converter Applications in Microgrids

Matrix converters can be used in the microgrids in different applications. Some of the main applications recently proposed in the literature can be listed as follows.

1.2.1 Matrix converter as an interface link between the microgrid and the utility grid

A microgrid includes different distributed generations (DGs), storage units and the loads which are connected to a common dc or ac bus [40]. The energy consumers of the microgrid are usually residential, commercial and industrial users. Furthermore, the DG systems such as solar systems and wind turbine generators supply the loads, and batteries and flywheels are examples of the energy storage devices. The microgrid utilizes the different DGs and storage devices to provide a secure and reliable supply for the loads. However, it still needs to be connected to the utility grid to improve the energy supply reliability due to the intermittent nature of the most of the DG resources [40]. In addition, there is a possibility of bidirectional power flow between the microgrid and the main grid. This lets the utility grid to supply a portion of the microgrid energy demand in the case that the power generation is less than the load demand in the microgrid. Also, the surplus energy of the microgrid can be supplied to the utility grid when the power generation is more than the load demand in the microgrid.

The electrical connection point of the microgrid to the utility grid is known as the point of common coupling (PCC) [41]. In most of the cases, a converter is required at the PCC to control the power flow between the microgrid and the utility grid and also to adapt their features such as voltage level and frequency range. A proper topology of the converter in the PCC depends on the characteristics of the microgrid and the utility grid such as nominal voltage and frequency range. In the

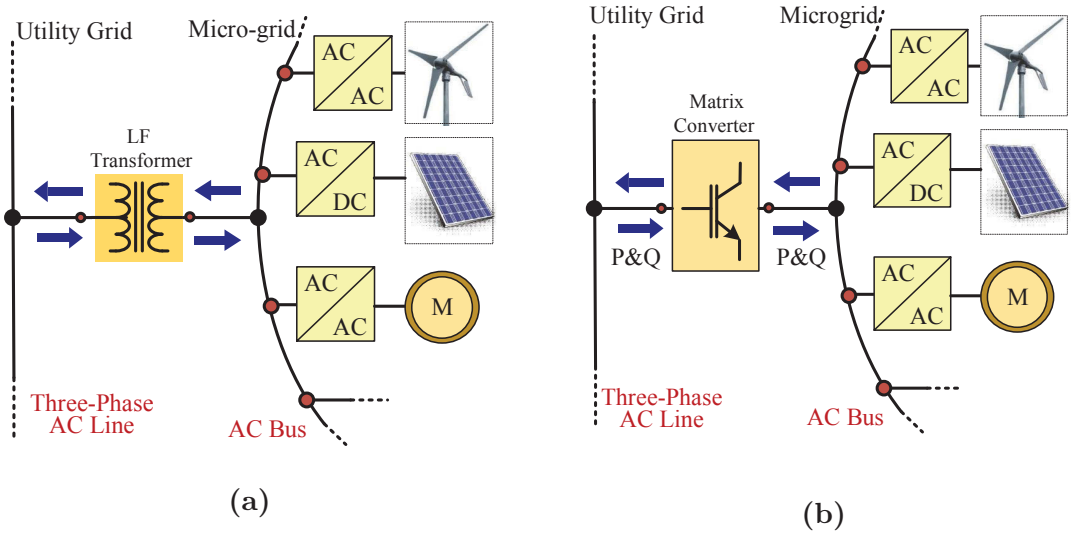


Figure 1.9: a) Using a transformer as an interface link between the microgrid and the utility grid at the PCC, b) Using a matrix converter as an interface link at the PCC

simplest case, it can be a simple low-frequency transformer with adjustable center taps. However, to control the power flows between the two grids, more complex systems such as solid-state-transformers (SSTs) or power electronics transformers (PETs) are feasible solutions [41–43].

To connect the microgrid to the utility grid, their parameters should be matched by using a proper interface link. The complexity of the link depends on the difference between the parameters of the grids such as voltage and frequency, and the required control features. In the simplest form a three-phase transformer with additional center tap voltage control can be used as the interface link as presented in Figure 1.9a. In this case, the transformer is used to match the voltage of the microgrid ac bus to the utility ac line. The microgrid frequency should be the same as that of the utility grid, and there is no power flow control between the grids. Furthermore, the microgrid ac bus needs to be synchronized to the grid when it is going to change from off-grid to the grid-connected operation mode.

In the case that the nominal voltage of the microgrid is slightly less than the utility grid, and there is a difference between the frequencies, a MC can be used as a feasible interface link as presented in Figure 1.9b. In this case, the power flow

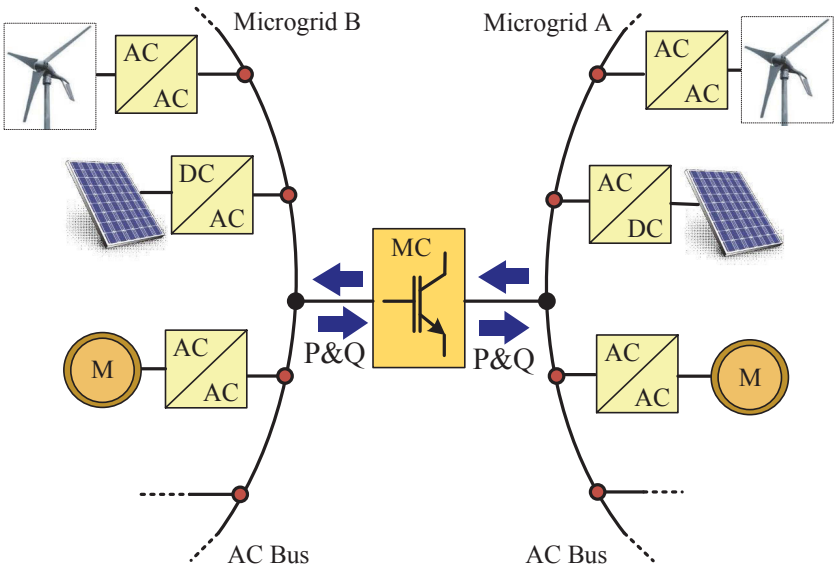


Figure 1.10: Application of the MC as a link between two microgrids

from the main grid to the microgrid can be controlled according to the microgrid requirements. On the other hand, the power flow from the microgrid to the utility grid can also be controlled. Furthermore, there is no need for synchronizing the grids at the transient time from the off-grid to the grid-connected condition. However, in the case of direct linked MC, the voltage level of the microgrid should be less than the utility grid due to the limited gain of the MC (less than 0.87). Although, the frequency of the microgrid and the utility grid can be the same or different. An example of such a microgrid is the airport microgrid where the DGs, storage devices and the loads are connected to a 400Hz common ac bus. The reason is that increasing the frequency reduces the size of the power electronic systems, electrical motors, and results in an increase in the cargo capacity. The standard voltage of the microgrid ac bus should be in the range of 115-200 V(rms). Therefore, a MC can be used in this application without any concern regarding the voltage gain limit [44].

Another example is using the MC as a link between two microgrids with different voltage levels and operating frequencies. Figure 1.10 shows two microgrids that are linked together at PCC using a MC. A bidirectional power flow between the microgrids is possible, however, it should be noted that the power can not be controlled

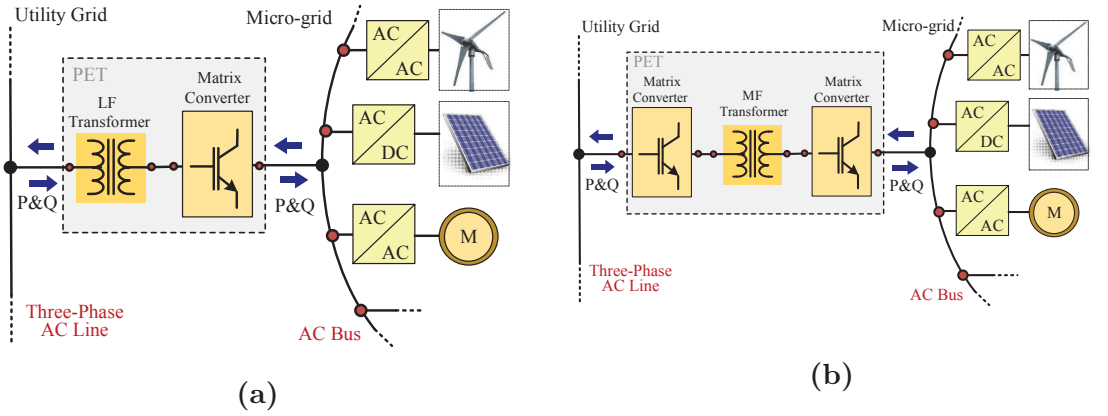


Figure 1.11: Application of the MC as a link between the utility grid and a microgrid, a) Using a MC with a low-frequency transformer, b) Using two MCs with a medium-frequency transformer

simultaneously at the both sides of the converter due to the lack of energy storage device in the MC topology.

Despite the mentioned advantages, the limitation in the MC voltage gain limits the application of this topology. Therefore, as a solution a low-frequency transformer can be used in series to the converter to change the voltage level according to the requirements and the converter is used to match the frequencies and control the power flow as presented in Figure 1.11a.

To reduce the system size, two MCs with a medium-frequency transformer can be used as presented in Figure 1.11b. In this case, the transformer size is reduced significantly due to the higher operating frequency. However, an extra converter is required which may increase the system cost. Such a structure is known as solid state transformer (SST) or power electronics transformer (PET).

The main advantage of using a PET at the PCC is bidirectional power flow control between the main grid and the microgrid. On the other hand, the ac bus frequency of the microgrid can be different from the utility grid. Furthermore, the transition from islanded mode to the grid-connected mode can be achieved without requiring a grid-frequency synchronization process. As a result, a faster and smoother transition is possible. Also, connection to the utility grid provides a degree of freedom to the microgrid to maintain a better power quality for the consumers in

terms of the frequency and voltage stability. Furthermore, more flexible marketing strategy and energy supply services are possible. On the other hand, the utility grid also can benefit from bidirectional power flow to the microgrid. The microgrid can actively assist the main grid to improve the power quality. For example, in the case of a frequency drop in the microgrid, the utility grid can assist the main grid by supplying the active power to the utility network. However, a power balance control between both networks is required to avoid the undesirable instabilities [45, 46]. For example, the active power flow from the utility grid to the microgrid in the peak demand hours may result in undesirable frequency change in the main grid and should be limited by the PET.

The main advantages of using a PET at the PCC over a low-frequency transformer can be listed as:

1. PET provides a controlled bidirectional power flow while in the case of the low-frequency transformer a bidirectional power flow without control is possible.

2. The voltage regulation and frequency control are achievable only by reactive and active power control in the grids. In the case of using a PET, the voltage and frequency regulations are maintained by controlling the active and reactive power transferred between the networks.

3. In the case of using a simple transformer, a grid synchronization is required when the microgrid is changing the status from islanded to grid-connected mode. However, in the case of using PET a smooth transition without using synchronization is possible.

4. The microgrid and the utility grid can have different frequencies in the case of using a PET, while in the case of the simple transformer, they should have the same frequency.

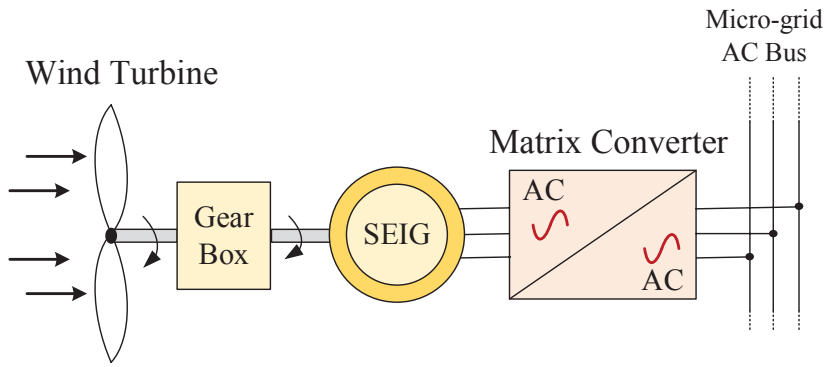


Figure 1.12: Application of the MC as an interface between a variable-frequency wind turbine generator or a high-frequency generator and the microgrid ac bus

1.2.2 Other applications of the matrix converters in the microgrids

MCs also can be used in other applications related to the microgrids as will be discussed in the next sections. These applications are generally in smaller scale compared to the application in PCC and are related to the connection of DGs with an ac output or ac loads to the common ac bus of the microgrid.

Applications of the matrix converter as a frequency regulator

MCs can be used as an interface between a variable-frequency wind turbine generator or a high-frequency generator and the microgrid ac bus as presented in Figure 1.12 [47, 48]. The conventional converters for this application, include an ac to dc stage such as diode or thyristor rectifier at the generator side followed by a grid-tied voltage source inverter. This structure imposes a large capacitor at the dc link which increases the size and weight of the converter and reduces the reliability. Furthermore, the current at the generator and grid sides are normally distorted and poor quality. Therefore, using the MCs is a feasible solution for this application. The main application of the MC, in this case, is to convert the wind energy at varying wind velocities and consequently the output frequency to the electric power with a constant frequency equal to the microgrid frequency. Compared to the conventional conversion systems, MC has a smaller size, provides high-quality currents at the

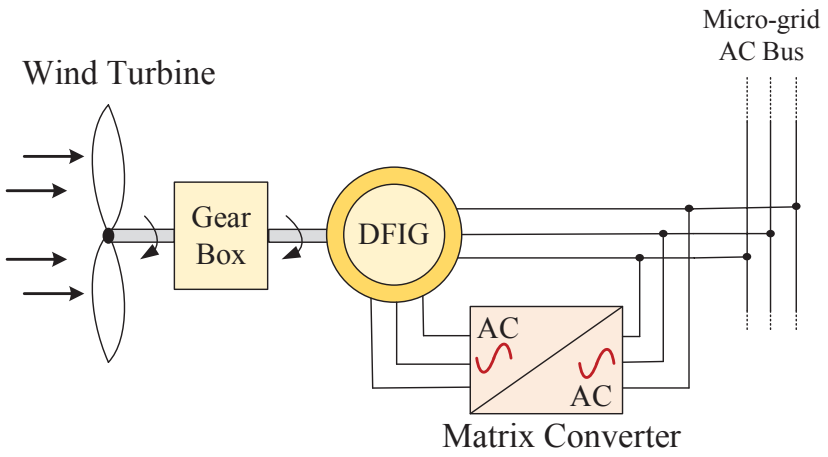


Figure 1.13: Application of the MC in doubly fed induction generators (DFIG) for variable speed generation systems

generator and grid sides, and does not need dc-link capacitors which increases the system reliability.

Application as a power electronic interface in wind power doubly fed induction generators

Another application of the MCs is in doubly fed induction generators (DFIG) for variable speed generation systems as presented in Figure 1.13 [49, 50]. As can be seen, the MC is used as an interface link between the microgrid ac bus and the rotor of DFIG. In this case, bidirectional power flow is achieved between the ac bus and the rotor which is used to adjust the current at the rotor and ac grid sides. Therefore, the active and reactive power supplied to the ac bus can be controlled independently of the generator speed. Based on this, the MC in this application is used to control the bidirectional power flow between the microgrid ac bus and the DFIG rotor.

Application as an interface link between microgrid ac bus and variable frequency load

In this case, MC is used as an interface between the microgrid ac bus and the ac load with variable frequency. The most common example of such an application is in ac

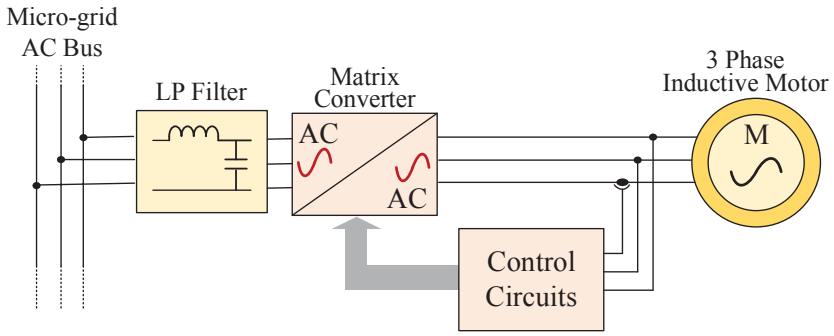


Figure 1.14: Application of the MC as an interface between the microgrid ac bus and the ac load with variable frequency

drive of induction machines as presented in Figure 1.14 [51–53]. In this application the MC is used to control both voltage and frequency of supplied voltage to the motor. Different control techniques such as mode-based predictive control (MPC), direct torque control (DTC) and so on can be used to control motor speed.

1.3 Motivation and Objectives of the Project

During the last four decades, the use of power electronics has been growing rapidly in the industry for various applications. Among the power electronic frequency converters, MCs, due to their advantages including bidirectional power flow, compactness and reliability are expected to have an increasing influence on the industry. MCs can be utilised for many applications like wind turbine, aerospace environments and electric vehicles [54]. As MCs offer a bidirectional power flow control with controllable input power factor and sinusoidal input and output currents, they can be used as a grid-connected converter to control the flow of power and convert it into a suitable AC form as required. They are particularly attractive for variable frequency wind and marine turbine generators and high-speed turbine generators in the context of microgrids [48, 55, 56].

The general motivation for this thesis is to determine the stability conditions of the MC as an interface between the utility grid and a microgrid for power flow control based on a detailed system stability analysis. The analysis mainly focused on

the two common active and passive stabilization methods proposed in the literature for bidirectional power flow control, considering the main effective parameters of the system including input and output filter elements, load and line impedances, and input and output frequencies. Furthermore, a combination of the digital low-pass filter as an active stabilization method, and the damping resistor as a passive stabilization method is suggested taking into account the efficiency performance and the THD standard limits. A detailed stability analysis of the MC for the proposed techniques is provided and their performance in terms of their efficiency, dynamic response and resultant overshoot in transients, and the quality of the input source current are compared. To do the stability analysis, the small signal model of the converter is derived for each method. The effect of the system parameters on the stability region and converter gain is briefly discussed. Some of the solutions for increasing the output power limit with a stable MC are investigated, and the obtained results are analyzed in aspects of the THDs of the input and output currents and power loss. On the other hand, along with the stability discussions, a solution is presented for increasing the efficiency of the converter, and the results are analyzed.

The proposed stabilization techniques are studied in the context of microgrid application. To evaluate the capability of different modulation methods, two well-known modulation methods of MCs, Venturini and SVM, are used, and the simulation and experimental tests are performed. Also, different commutation methods are studied in detail and a current direction based four-step semi-soft commutation method is carried out for the prototype DMC, and the experimental results are presented.

The theoretical analysis is validated by the simulations using PSIM, and is confirmed by experimental tests applying to the prototype DMC.

As a conclusion, the main objectives of this research can be listed as:

- Evaluation of the proposed solutions for stabilisation of the MC where its output is connected to a load or another source, and proposing the best method for increasing the input and output current quality and system efficiency.

- Controlling the active power exchange between the input source and load, or bidirectional power flow between the two sources.
- Designing a prototype DMC as an interface between the grid and a micro-grid.
- Analysis of the protection circuits and commutation methods to select the most reliable commutation strategy and protection for the prototype converter.
- Investigating some modulation strategies for DMC and IMC.

1.4 Thesis Outline

The structure of the thesis is divided into seven chapters. The main objective of each chapter is briefly discussed as follows:

Chapter 1 is an introduction to the thesis with a brief illustration of the ac-ac power converters. This chapter also presents the research motivations and outlines the main objectives of the research.

Chapter 2 gives a technology overview of the MC topologies with a general description of the MC fundamentals. The possible configurations of bidirectional switches are shown, and their advantages and drawbacks are discussed to select a proper configuration. The design of the input filter and the protection issues are also briefly investigated. The chapter also presents an overview of the current commutation techniques based on either the output currents or input voltages measurement.

Chapter 3 provides a detail study on the concept of the direct and indirect matrix converter topologies. This chapter presents two main modulation methods of the DMCs including Venturini and space vector modulation (SVM) that is followed by the simulation and experimental results, to show the effectiveness of the modulation strategies in controlling the converter. SVM method for IMC is also illustrated in detail, and the simulation results confirm similarities of the DMC and IMC.

Chapter 4 focuses on the hardware design of the prototype DMC designed for this project to validate the theoretical and simulation results. The overall structure of the prototype including power and control circuits, measurement and protection circuits and the other parts, are illustrated in detail.

Chapter 5 discusses the stability issues of the MCs. The importance of the input voltage measurement, input filter components and the other system parameters on the stabilisation of the MC system are reviewed in detail. The general solutions proposed for stability analysis of the DMC using the small signal modelling are studied in detail.

Chapter 6 investigates the unidirectional and bidirectional active and reactive power flow control in MCs using voltage-oriented control method. The impact of each proposed stabilisation method is analyzed, and their advantages and disadvantages are discussed. Then the best choice for reducing the power loss and also to obtain the maximum power for a stable MC system is introduced.

Chapter 7 summarises the research work and presents some suggestions for the future work.

Chapter 2

MATRIX CONVERTER FUNDAMENTALS AND PROTECTION TECHNIQUES

2.1 Introduction

The matrix converter is one of the semiconductor-based converters which has several attractive features. Basically, MCs have several advantages over traditional ac-ac converters including, sinusoidal waveforms in the input and output, bi-directional power-flow capability, fully controlled input power factor with the ability of unity power factor at the interface with the grid, without bulky and lifetime-limited dc-link capacitors. Although, they have some disadvantages which the most important one is limited output to input voltage transfer ratio that is less than unity ($q \leq 0.87$). On the other hand, in the absence of energy storage capacitors, MC is sensitive to the disturbances of the input voltage system.

In this chapter, a general description of the basic features of a three-phase to three-phase DMC including the basic MC technology and its protection issues are presented. First, the basic bidirectional switch configurations are introduced, and some integrated switch modules that have been designed for the power stage of the MC are presented. After that, some technical issues related to the input filter and

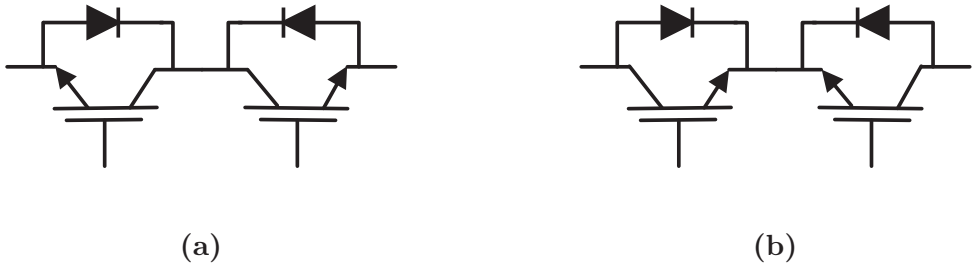


Figure 2.1: Back-to-back bidirectional switches configurations a) Common-collector b) Common-emitter

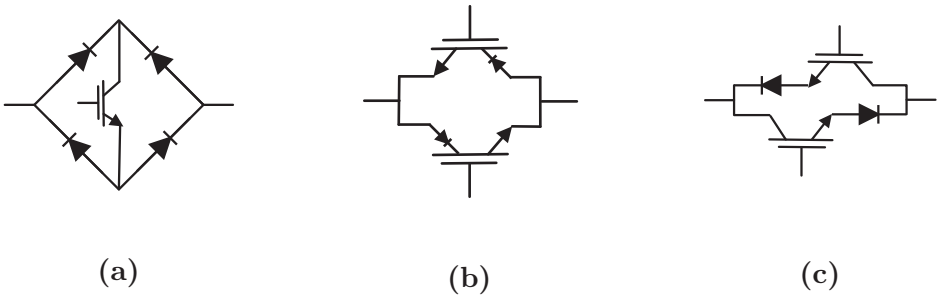


Figure 2.2: Other possible bidirectional switch arrangements a) Switch-diode bridge b) Antiparallel reverse blocking IGBTs (RBIGBTs) c) Switch and diode in series configuration

clamp circuit are investigated. Also, a notable part of the chapter is dedicated to the commutation techniques of the MC.

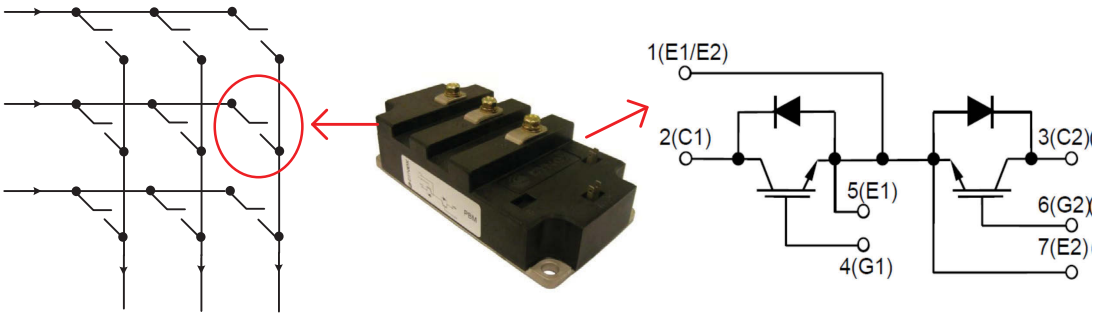


Figure 2.3: Package and the circuit configuration of Dynex IGBT bidirectional switch module [1,2]

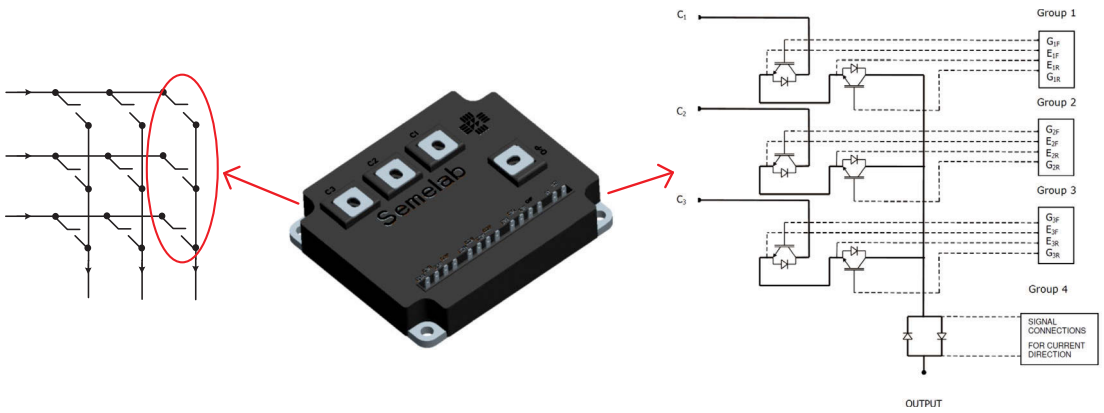


Figure 2.4: SEMELAB SML150MAT12 bidirectional module [3]

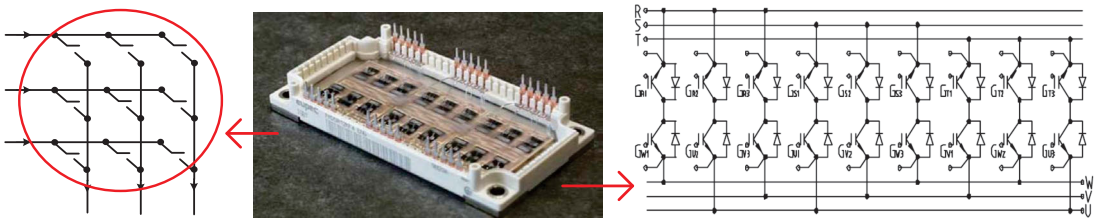


Figure 2.5: EconoMAC three-phase bidirectional switch module [4]

2.2 Bidirectional Switches

There are different bidirectional switch configurations as illustrated in Figures 2.1 and 2.2 using fully controllable semiconductors like IGBTs and RB-IGBTs. Back to back configurations shown in Figure 2.1 are the most popular bidirectional switches that are in common-collector or common-emitter arrangements and consist of two IGBTs with built-in fast recovery diodes. In these two configurations, the current can be controlled in both directions independently. The other switches presented in Figure 2.2 are not as popular as the previous ones because:

- The switch in Figure 2.2a is not applicable with some commutation methods as it contains only one active switch, and so its current cannot be controlled. Also, it has more components in the current path and conduction losses are increased.

- Although for the configuration presented in Figure 2.2b there is only one component conducting in the current path, the RBIGBTs characteristics are not as

known as IGBTs for MCs.

- The switch in Figure 2.2c consists four separated components against the ones with only two IGBTs with built-in diodes.

Also, some integrated switch modules have been designed for the power stage. Dynex Bi-Directional Switch modules [1,2] (DIM400PBM17-A000) and (DIM200MB S12-A000) are two bidirectional IGBT modules which are suitable for MC power stage. DIM400PBM17-A000 module designed for higher power (400A, 1.7 kV) and DIM200 MBS12-A000 module designed for lower power applications (200A, 1.3 kV). Each module contains one IGBT bidirectional switch as shown in Figure 2.3. SEMELAB SML150MAT12 bidirectional module [3] which is illustrated in Figure 2.4, contains three bidirectional switches which can be used for one of the output phases of the matrix converter. Another matrix converter module shown in Figure 2.5 is EconoMAC three-phase module build up by Siemens A&D in co-operation with Eupec as a laboratory prototype of a matrix converter [4]. It contains all nine bidirectional switches and can be used as the power stage of a 7.5kW matrix converter.

2.3 Input Filter

In general low-pass filters are needed at the input side and sometimes at the output terminals of the MCs to filter out the high-frequency harmonics generated by the switching process. The input filter is designed to prevent any switching frequency harmonics of the input currents from reaching the power supply and causing more distortions. Figure 2.6 shows an overall structure of the DMC with a low-pass input filter. The output filter may not be necessary for three-phase motor or RL loads.

Many literature addressed the input filter design of the switching power converters including MCs [57–64]. Different configurations of the input filter have been introduced, although the most practically used input filter considering the cost, weight and design simplicity is the low-pass LC filter. The schematic of the DMC including the LC input filter and a damping resistor in parallel with the inductor is

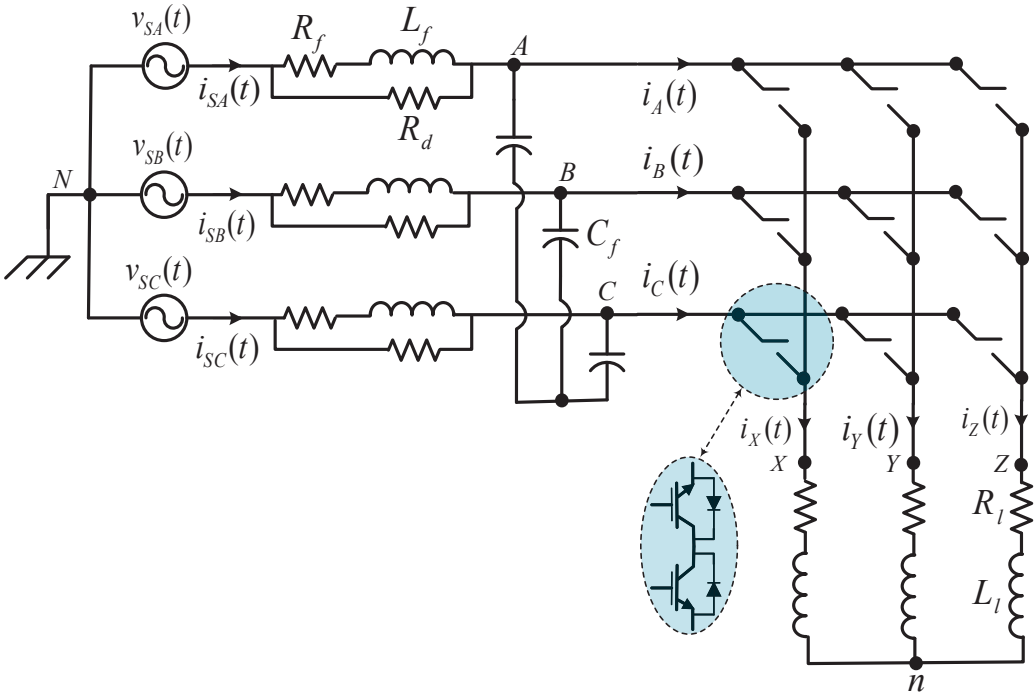


Figure 2.6: Basic power circuit of the DMC with the input filter and RL load

presented in Figure 2.6. To achieve higher attenuation at the switching frequency, two-level LC filter [65, 66] and more complicated filters such as the filter proposed in [60] can be used.

For convenient analysis of the three-phase second-order LC filter, a single-phase model of the filter can be considered when the three-phase input source and load are balanced as illustrated in Figure 2.7. The input filter interacts with the converter and, sometimes it causes degradation in the performance of the MC. On the other hand, because the harmonics of the input currents are near the switching frequency, so the filter parameters have to be selected such that to minimise these unwanted effects.

The cut-off frequency of the designed input filter must be sufficiently lower than the switching frequency. In order to have the highest voltage gain, the voltage drop on the filter inductance should be minimised. Also, by taking into account the minimum output power, the displacement power factor $cos(\varphi_i)$ should be maximised

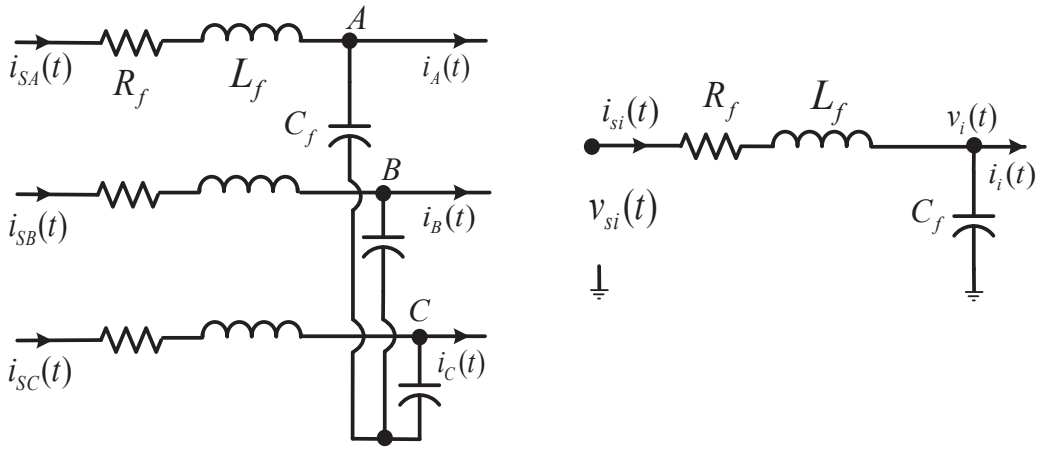


Figure 2.7: Second order LC filter, three-phase and single-phase

accordingly. One of the most important parameters of the MC is the input filter volume and weight as the matrix converter is considered as an all-silicon solution to the power conversion and does not need large passive components to save energy. Therefore, the input filter design should minimize the filter weight and volume [65] [27, 67, 68].

2.3.1 Design of the input filter

Considering Kirchhoff's voltage law for the simple LC low-pass filter presented in Figure 2.7, the MC input voltage is as follows [69]:

$$\begin{aligned} v_{si}(t) &= v_i(t) + L_f \frac{d\left(i_i(t) + C_f \frac{dv_i(t)}{dt}\right)}{dt} + R_f \left(i_i(t) + C_f \frac{dv_i(t)}{dt}\right) \\ \Leftrightarrow v_i(s) &= \frac{v_{si}(s) - (L_f s + R_f) i_i(s)}{L_f C_f s^2 + R_f C_f s + 1} \end{aligned} \tag{2.1}$$

where L_f, C_f and R_f are the inductance, capacitance and the internal resistance of the inductor respectively. Also, v_{si}, v_i, i_i are the input source voltage, and MC input voltage and current respectively. The input source current can be defined as:

$$
\begin{aligned}
i_{si}(t) &= i_i(t) + C_f \frac{dv_i(t)}{dt} \\
i_{si}(s) &= i_i(s) + sC_f v_i(s) \\
i_{si}(s) &= \frac{1}{L_f C_f s^2 + R_f C_f s + 1} i_i(s) + \frac{sC_f}{L_f C_f s^2 + R_f C_f s + 1} v_{si}(s)
\end{aligned}
\tag{2.2}
$$

By considering (2.1), and proper selection of the input filter parameters, matrix converter input voltages will be very similar to the source voltages. Also, from (2.2), it is clear that the input source current includes two parts, a filtered version of the MC input current and a filtered version of the input supply voltage. As mentioned above, the filter design should be such that the voltage drop on the inductor L_f is minimized and so $v_i(t) \approx v_{si}(t)$.

The cut-off frequency ω_{coff} and the damping factor ζ of the input filter, considering the single phase model of the filter presented in Figure 2.7 are defined as:

$$\omega_{coff} = \frac{1}{\sqrt{L_f C_f}} \tag{2.3}$$

$$\zeta = \frac{R_f}{2} \sqrt{\frac{C_f}{L_f}} \tag{2.4}$$

As unity input power factor ($\varphi_i = 0$) is favorite for gaining the maximum voltage transfer ratio, the maximum input displacement angle (φ_{im}) is obtained for the minimum output power $P_{o,min}$. The rated input power at unity input power factor and full load is defined by:

$$P_{i,n} = 3U_n I_n \tag{2.5}$$

where U_n and I_n are the rated input phase voltage and current of the MC. The maximum input filter capacitance then is defined as [70]:

$$C_f = \frac{P_{o,min} \tan(\varphi_{im})}{3\omega_i U_n^2} \tag{2.6}$$

In the case of the 7.5kW prototype matrix converter, for obtaining minimum input power factor $PF_{in} = 0.9$ at 10% rated power, considering the nominal input

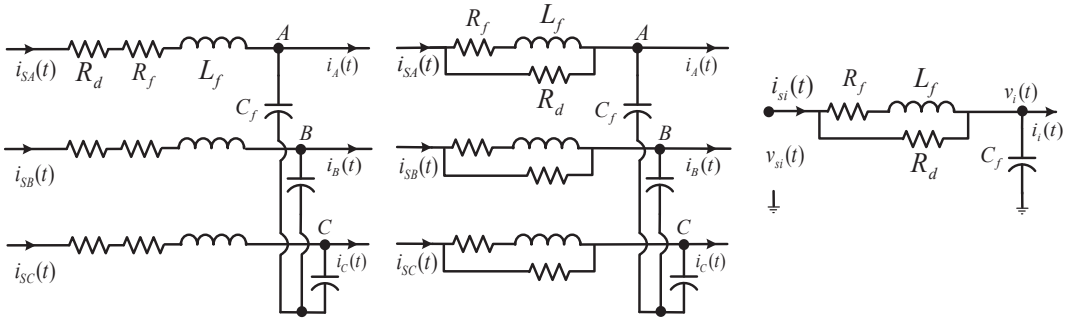


Figure 2.8: Second order LC filter with damping resistors a) In series with the inductors b) In parallel with the inductors c) Single-phase diagram for parallel damping resistor

phase voltage as 240V/50Hz, the maximum input filter capacitance is $6.7\mu F$. For the designed prototype, the selected capacitance is $6.6\mu F (3 \times 2.2\mu F$ film capacitor) [71].

For gaining the voltage transfer ratio, the voltage drop across the input filter inductance at the rated input current should be minimized [27] [70]:

$$\frac{\Delta U_n}{U_n} = 1 - \sqrt{1 - (\omega_i L_f)^2 \left(\frac{I_n}{U_n}\right)^2} \tag{2.7}$$

where ΔU_n is the voltage-drop on the filter inductance. Considering the apparent power of the capacitor (S_c) and the inductor (S_L) of the input filter as:

$$\begin{aligned} S_C &= \omega_i C_f U_n^2 \\ S_L &= \omega_i L_f I_n^2 \end{aligned} \tag{2.8}$$

It is possible to minimise the input filter weight and volume for the rated power as following:

$$\frac{S_L}{S_C} = \frac{L_f I_n^2}{C_f U_n^2} = \left(\frac{P_{i,n}}{3\omega_{coff} U_n^2 C_f}\right)^2 \tag{2.9}$$

By calculating the C_f using (2.6) and choosing the cut-off frequency ω_{coff} such that the input filter is able to attenuate the switching frequency, it is possible to find the filter inductance L_f using (2.3) or (2.9).

Since normally the resistance R_f of the inductor is less than 1Ω (less than 1% in pu scale), so the damping factor ξ is very small. The common LC filter as an input

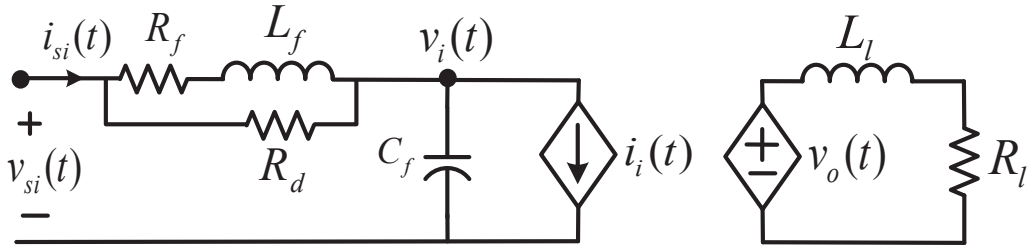


Figure 2.9: Per-phase equivalent scheme of direct matrix converter

filter, can be excited by the harmonics of the input current of the MC which is a PWM waveform, and cause instability not only in the power-up process but also, in the steady-state operation [64]. With the filter parameters ($C_f = 6.6\mu F$, $L_f = 3mH$ and $R_f = 0.1\Omega$), the resonant frequency is about 1131 Hz, and the damping factor is 11×10^{-3} which is very small. To increase the damping factor, it is possible to add damping resistors in series or in parallel with the filter inductance as illustrated in Figure 2.8. However, adding a damping resistance in series with the L-C input filter decreases the efficiency of the converter. It is better to add the damping resistance in parallel with L_f to increase the efficiency [22, 72], however the high-frequency harmonics of the input current can flow through the damping resistor to the input source current.

The matrix converter can be considered as a current sink in the input side and a voltage source in the output side as shown in Figure 2.9. By putting the damping resistors R_d in parallel with the input filter inductors, the input source current in (2.2) can be rewritten as:

$$
\begin{aligned}
i_{si}(s) &= i_i(s) + sC_f v_i(s) \\
i_{si}(s) &= \frac{R_d + R_f + sL_f}{R_d L_f C_f s^2 + (R_d R_f C_f + L_f)s + R_d + R_f} i_i(s) + \\
&\quad \frac{C_f L_f s^2 + C_f(R_d + R_f)s}{R_d L_f C_f s^2 + (R_d R_f C_f + L_f)s + R_d + R_f} v_{si}(s)
\end{aligned}
\tag{2.10}
$$

Moreover, the forward gain of the damped input filter is defined as follows:

$$\frac{v_i(s)}{v_{si}(s)} = \frac{i_{si}(s)}{i_i(s)} = \frac{L_f s + R_d + R_f}{R_d L_f C_f s^2 + (R_d R_f C_f + L_f)s + R_d + R_f} i_i(s) \tag{2.11}$$

Consequently, the cut-off frequency and damping factor can be obtained as:

$$\omega_{coff,d} = \sqrt{\frac{R_d + R_f}{R_d L_f C_f}} \tag{2.12}$$

$$\zeta_d = \frac{L_f + R_d R_f C_f}{2\sqrt{R_d L_f C_f (R_d + R_f)}} \tag{2.13}$$

As the resistor R_f compare to the R_d is very small, the cut-off frequency and also the damping factor for the input filter illustrated in Figure 2.8 can be approximately defined by [64]:

$$\begin{aligned} &R_f \ll R_d \qquad \Rightarrow \qquad \omega_{coff,d} = \omega_{coff} = \frac{1}{\sqrt{L_f C_f}} \\ &\zeta_d = \frac{1}{2R_d}\sqrt{\frac{L_f}{C_f}} \end{aligned} \tag{2.14}$$

In order to reduce the power loss caused by the damping resistors, if the converter remains stable in normal operation, they can be bypassed by using the bypass relays after power-up as illustrated in Figure 2.10 [27]. To design the parallel and series damping resistances the following conditions should be taken into account [27] [70]. For damping resistor in parallel with the filter inductance:

$$R_d \leq \omega_{coff}.L_f \tag{2.15}$$

which means the damping resistor has to be smaller than the reactance of the input filter inductor at the cut-off frequency. For example for the designed prototype DMC, $R_d \leq 21.32$. As R_d is smaller compare to the reactance of the input filter inductor in higher frequencies, the high-frequency harmonics of the current mostly flows through the damping resistor instead of the inductor, and this improves the

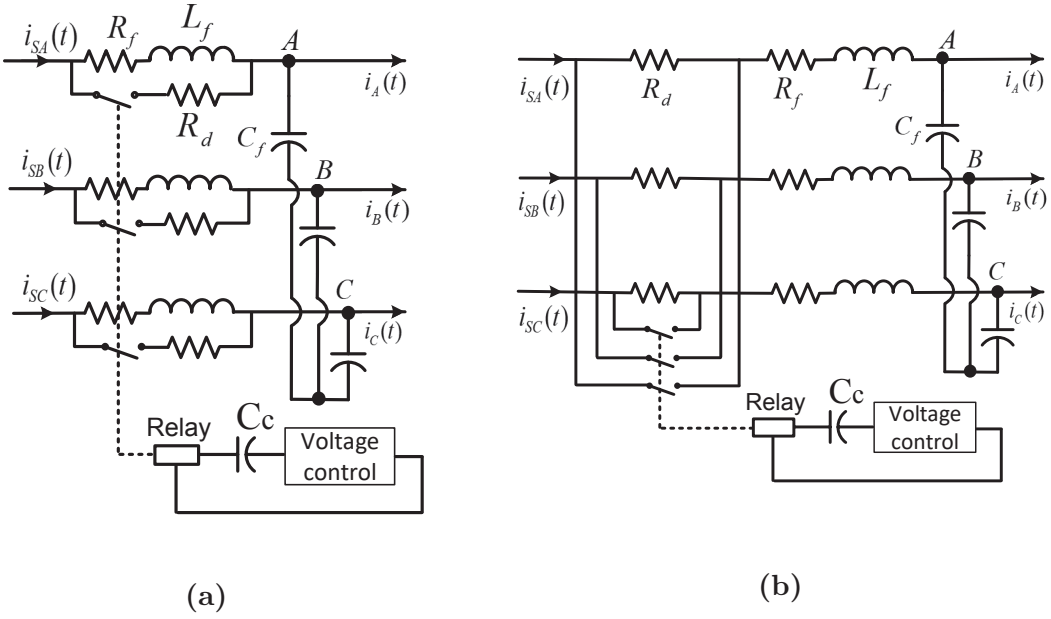


Figure 2.10: Second order LC filter with bypass relays for preventing of more power loss, and damping resistors a) in parallel b) in series with the inductors

input current waveforms during power-up.

In the case of series connected damping resistor the condition can be presented as:

$$R_d \geq 2\sqrt{\frac{L_f}{C_f}} \tag{2.16}$$

Figure 2.11 shows a comparison among bode diagrams of the damped input filter transfer function, with damping resistors in parallel with the filter inductors for different values of R_d. It can be seen that the cut-off frequency for $R_d = 20$ occurs at about 1100Hz that is close to the resonant frequency.

2.4 Clamp Circuit

Matrix converter is known as an all-silicon power converter and the dc-link capacitors which are bulky and reduce the converter lifetime are eliminated. However, MC still has some passive components in the input filter and the clamp circuit. On the other hand, elimination of the dc-link energy storage capacitor, causes the MC to be more

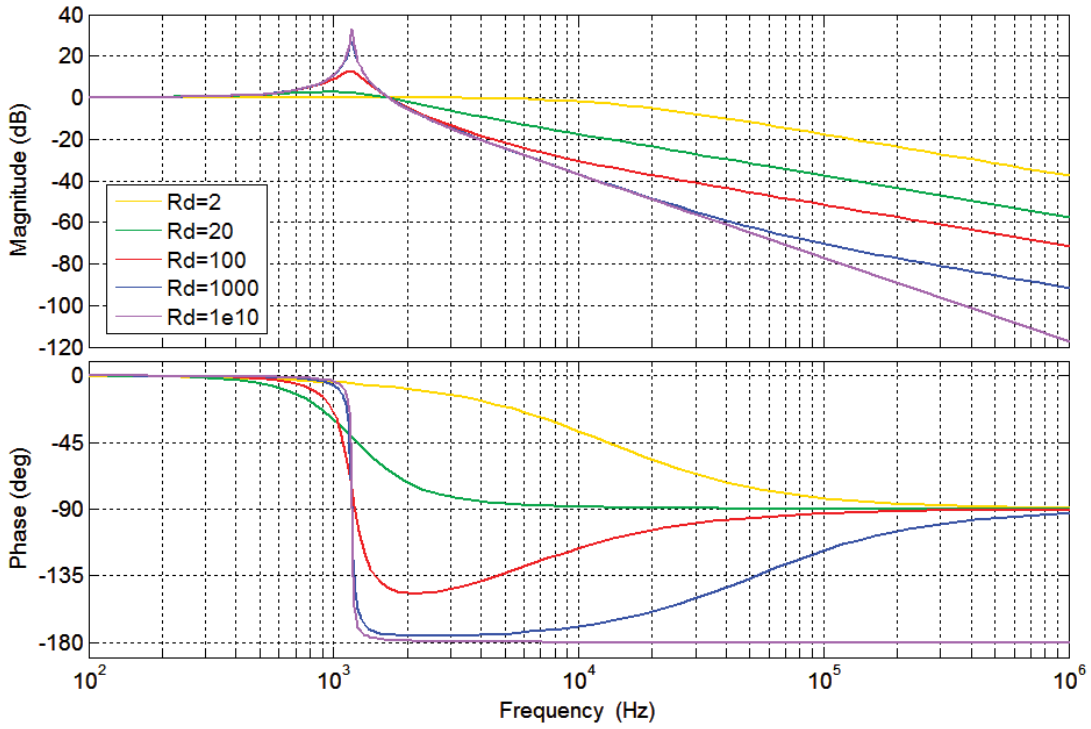


Figure 2.11: Comparison of the bode plots of the damped LC filter transfer function for different values of the damping resistor

sensitive and susceptible to disturbances.

A clamp circuit is a simple protection circuit which provides a freewheeling path to protect the converter against over-voltages caused by the forced shutdown of the converter or any other unpredictable disturbances. The circuit diagram of a simple clamp circuit connected to the input and output of the MC is shown in Figure 2.12 which includes two fast recovery diode bridges, a clamp capacitor C_c and a resistor R_c for discharging the capacitor. If any sudden shutdown happens to the converter for any reason or one of the switches fails or switches not being switched properly for commutation problem, the current will be able to flow through the clamp circuit and the clamp capacitor. By this way, any voltage spike that occurs due to the inductances can be stopped by the clamp capacitor that has been fully charged to the amplitude of the line voltage of the supply in normal operating conditions. Figure 2.13 illustrates the voltage across the clamp capacitor when the converter is

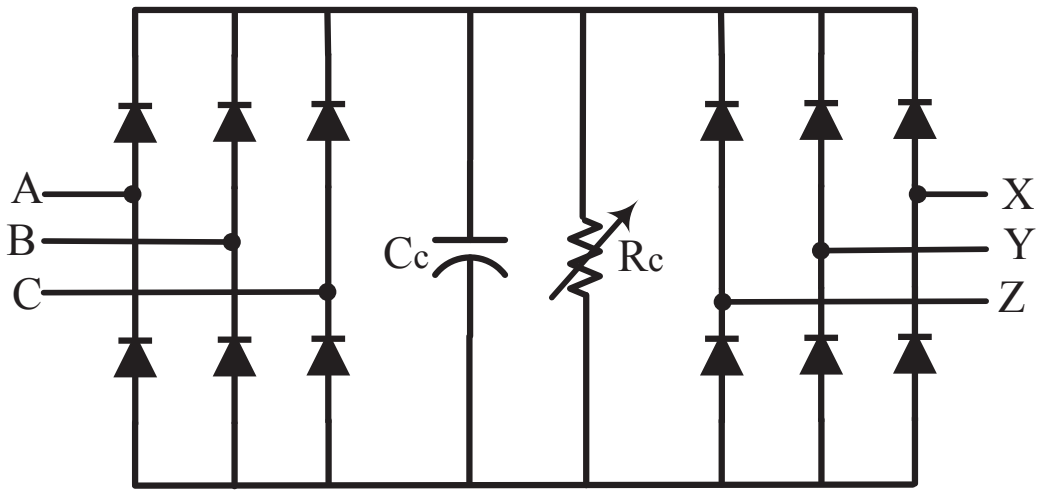


Figure 2.12: Circuit diagram of the voltage clamp used for converter protection against overvoltage spikes

shut down at 0.05s.

The total stored energy in a three-phase inductor that transfers to the clamp capacitor in the fault condition can be calculated by [73] :

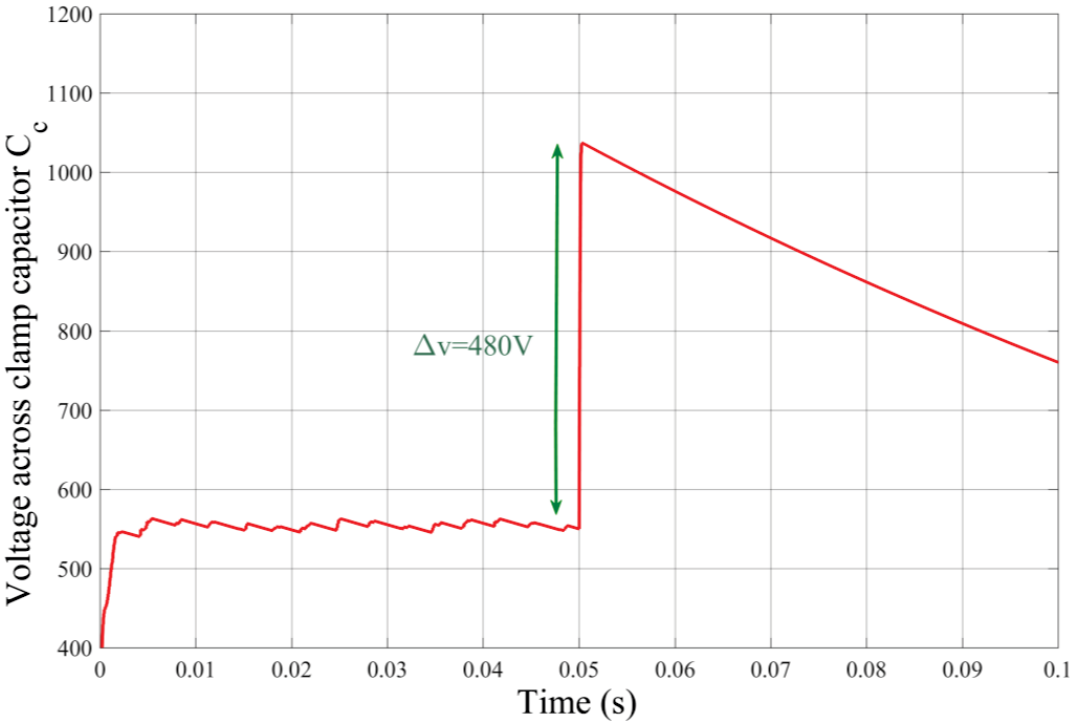
$$Q_L = \frac{1}{2}L_l(i^2_{X,rms} + i^2_{Y,rms} + i^2_{Z,rms}) = \frac{3}{4}L_l I^2_{om} \tag{2.17}$$

which $i_{j,rms}$ (j=X,Y,Z) is the output currant (rms), L_l is the load inductance, and I_{om} is the amplitude of the output current. As the initial value of the stored energy in the clamp capacitor is determined by the maximum input line voltage ($V_{C0} = V_{im,ll}$), so the maximum voltage across the clamp capacitor ($V_{C_c,max}$) after discharging the stored energy of the load can be defined by [73]:

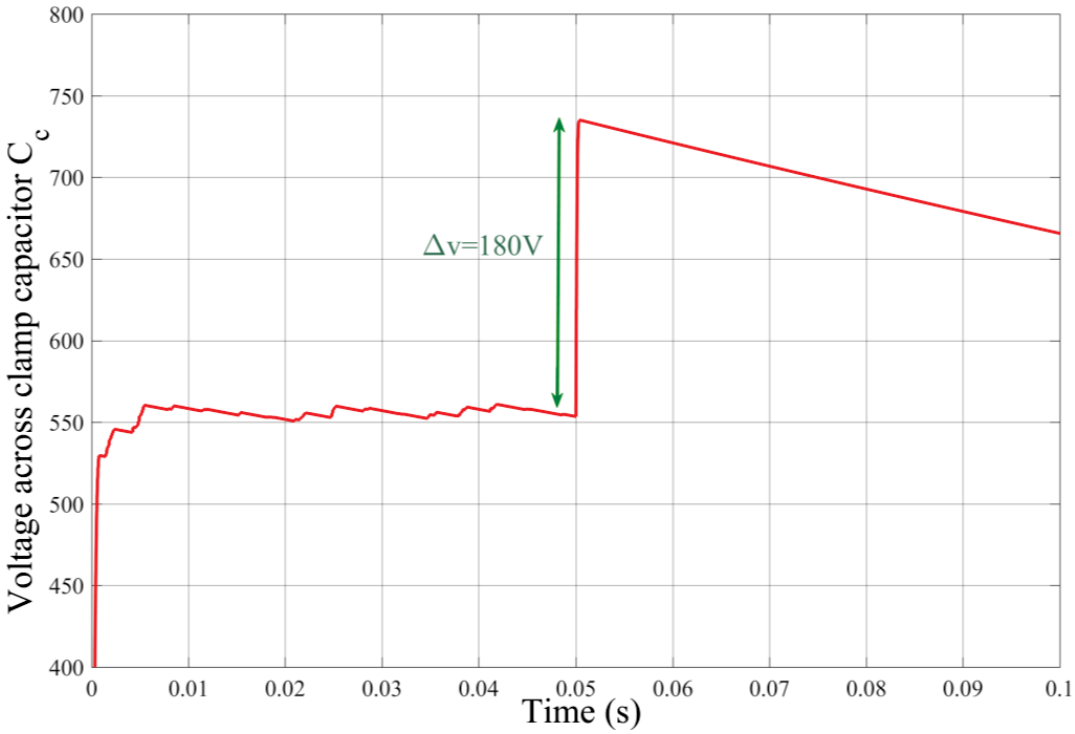
$$V_{C_c,max} = \sqrt{\frac{\frac{1}{2}C_c V^2_{C0} + Q_L}{\frac{1}{2}C_c}} = \sqrt{\frac{\frac{1}{2}C_c V^2_{im,ll} + \frac{3}{4}L_l I^2_{om}}{\frac{1}{2}C_c}} \tag{2.18}$$

where C_c is the clamp capacitor and is calculated by:

$$C_c = \frac{\frac{3}{2}L_l I^2_{om}}{V^2_{C_c,max} - V^2_{im,ll}} \tag{2.19}$$



(a)



(b)

Figure 2.13: Voltage across clamp capacitor when a) $C_c = 3.2\mu F$ b) $C_c = 10\mu F$

Table 2.1: Matrix converter simulation parameters

Input voltage	Input filter	output load	clamp circuit
$V_{si,peak} = 300V$	$C_f = 6.6\mu F$	$R_l = 10\Omega$	$C_c = 3.2\mu F$
$f_i = 50Hz$	$L_f = 3mH$	$L_l = 6mH$	$R_c = 50k\Omega$
		$f_o = 50Hz$	

In the case of using an induction motor, the load inductance is $L_l = L_{\delta s} + L_{\delta r}$ (the total motor leakage inductance) and $I_{om} = I_s$ that I_s is the maximum amplitude of the stator current. Therefore, to design the clamp capacitor by considering the switches characteristics, the maximum acceptable voltage and current should be taken into account.

As can be seen in Figure 2.13, in normal conditions the clamp capacitor charges to the maximum input line voltage and at the shutdown time the voltage across the capacitor steps up. It can be observed that the voltage surge for smaller capacitance is more than the larger capacitance. The system parameters are presented in Table 2.1.

Figures 2.14b and 2.14d show the output phase voltage and common-mode voltage which include a big voltage spike at the time of the forced shutdown when there is no clamp circuit. On the other hand, Figures 2.14a and 2.14c illustrate the reduction of the over-voltage by utilising a clamp circuit. The results for the input and output currents are shown in Figure 2.15. As can be seen, there is no important difference between the waveforms with and without clamp circuit.

2.5 Safe Commutation Techniques For DMCs

All the existing switching devices have a non-ideal characteristic, and there is a delay in switching during turn-on and off. Normally the delay during turn-off is more than the delay of the turn-on, and when two switches are changing their states these delays cause them to be 'on' at the same time, and a short circuit happens. To ensure the safe switching and to prevent the large current flows through the switches during the short circuits, a commutation strategy is required.

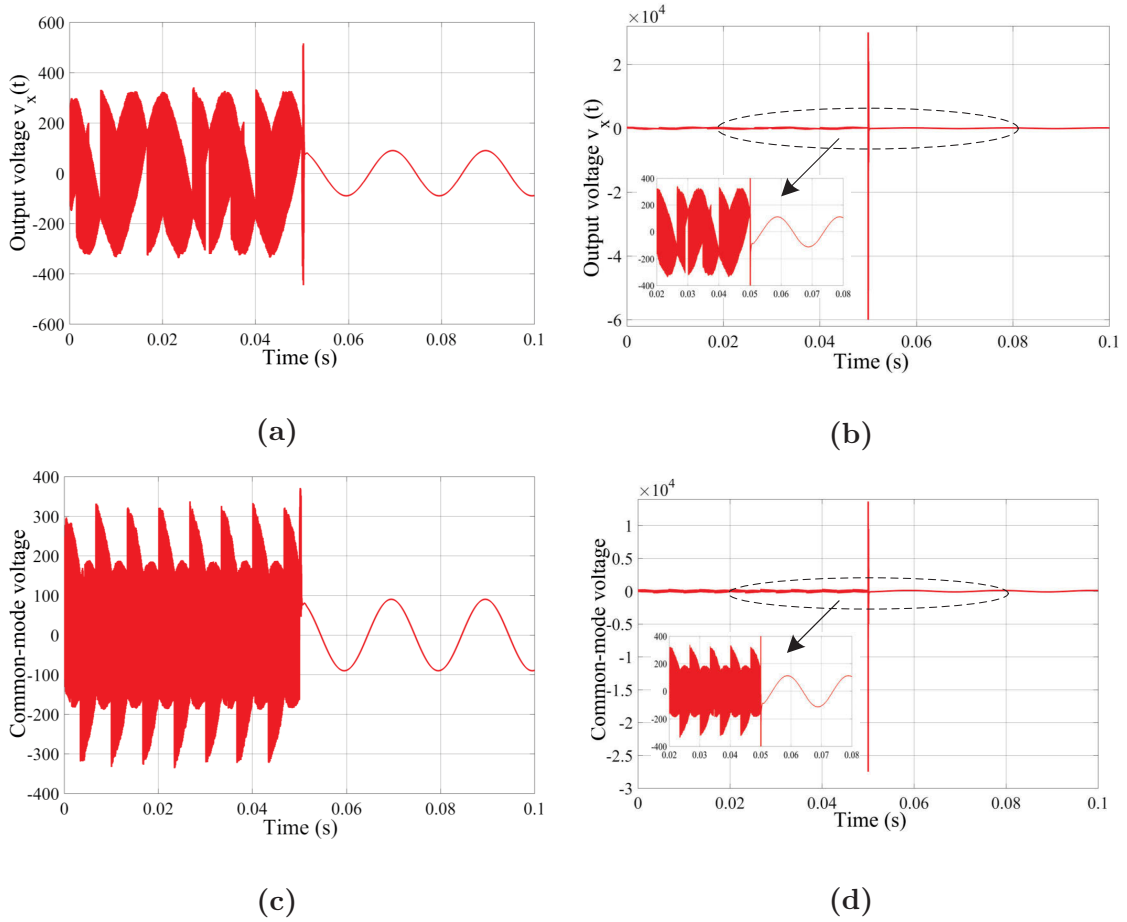


Figure 2.14: a) Output voltage $v_x(t)$ with clamp circuit, b) Output voltage $v_x(t)$ without clamp circuit, c) Common-mode voltage with clamp circuit, and d) Common-mode voltage without clamp circuit

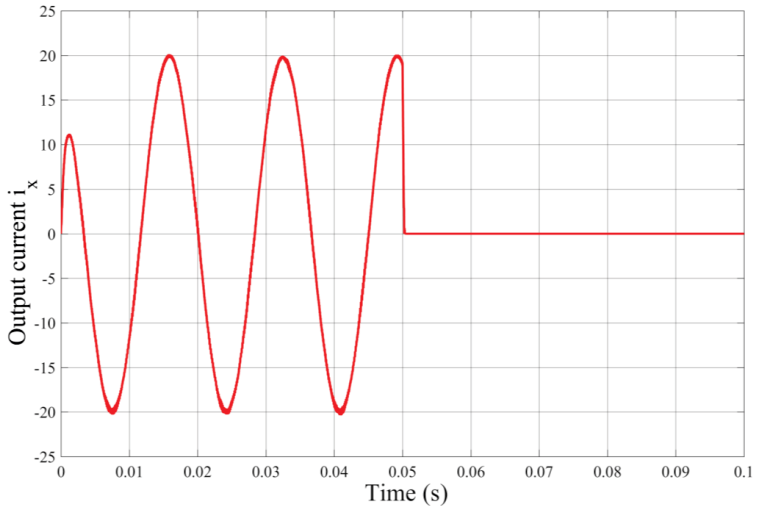
For all of the modulation methods of the DMC, two basic rules must be considered [69]:

1) For avoiding the input short circuit, there must not be more than one input phase connected to one output phase.

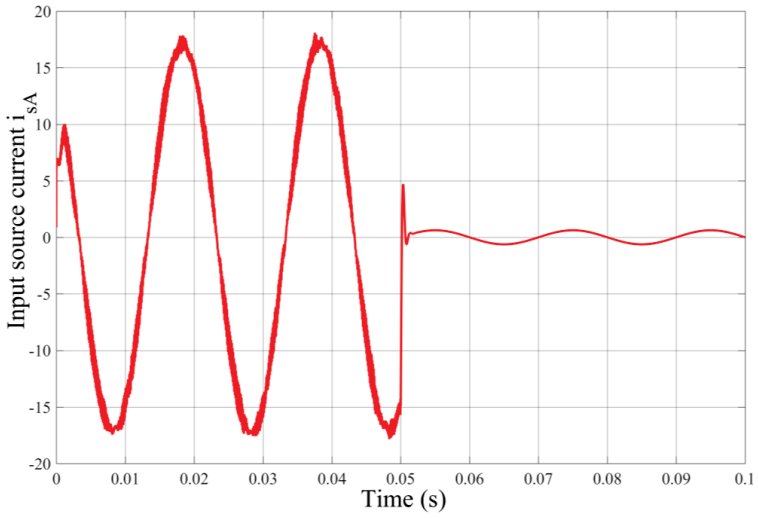
2) For avoiding the output open circuit, all the switches connected to any output phase cannot be left open at the same time.

To illustrate the current commutation problem in MCs, Figure 2.16 shows a simple matrix converter with two-phase input source and a single-phase load. When the input source voltage $v_{SA}(t) > v_{SB}(t)$, switch S11 is 'on' and S12 is 'off', and the current direction is as indicated in Figure 2.16, otherwise, when $v_{SA}(t)$ is less

(a)



(b)



(c)

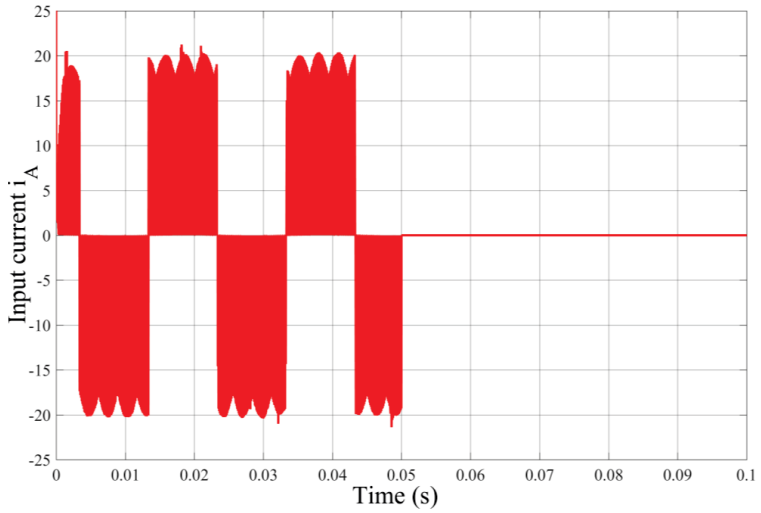


Figure 2.15: Input and output currents with clamp circuit, where a) Output current $i_x(t)$, b) Input source current $i_{sA}(t)$, and c) Input current $i_A(t)$

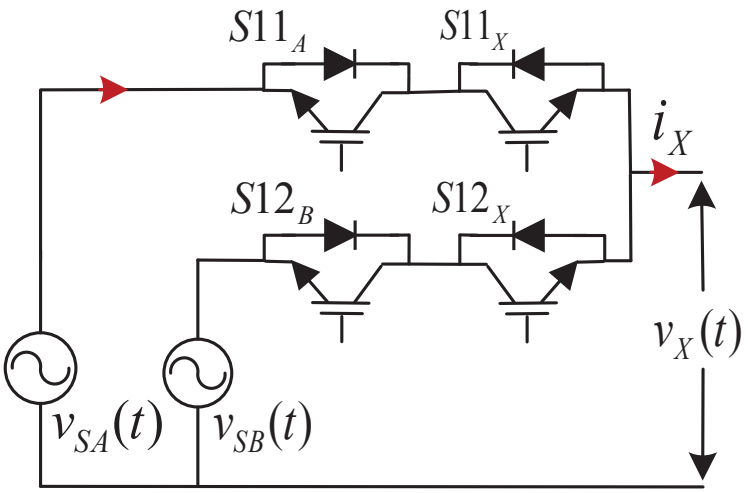


Figure 2.16: Matrix converter with two-phase input source and single-phase load

than $v_{SB}(t)$, S11 is 'off', S12 is 'on' and the current direction is the opposite of the previous direction. As the bidirectional switches are IGBT transistors which include antiparallel diodes, due to the direction of the transistors and diodes when both of the switches are 'on', current can flow in both directions. However, when both of the switches are 'off' at the same time, no current will flow through the bidirectional switches.

The common-collector and common-emitter back-to-back arrangements in Figure 2.1 are commonly used in matrix converters and are the most popular switching configurations. The one-step [74], two-step and four-step commutations are the commutation methods which are applied to these bidirectional switch configurations. They can operate based on the output current direction or the input voltage polarity [75–77]. Also, there is another method based on both output current direction and the input voltage polarity. These commutation methods were suggested for direct matrix converter in the late 1980s [78, 79] however, they can be applied to IMCs as well. The commutation process is performed by a programmable logic device like FPGA which consists of programmable logic components and interconnections that can operate in parallel [80].

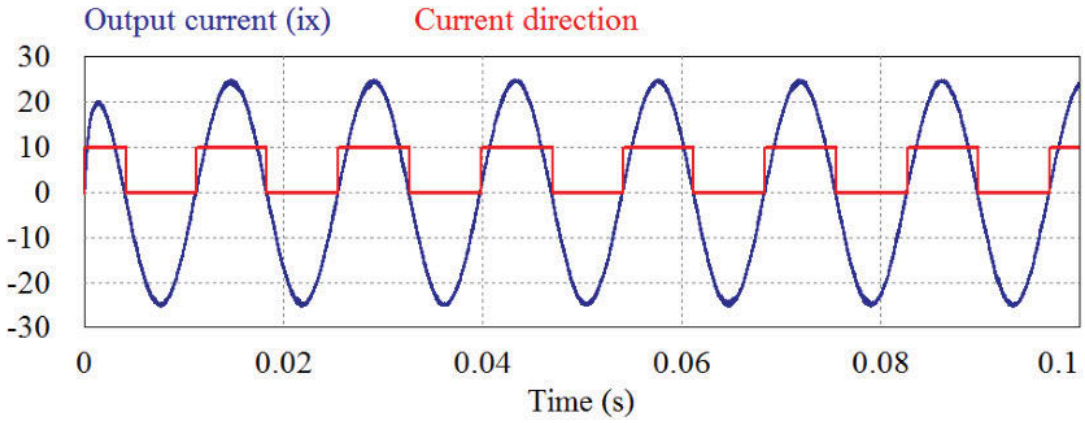


Figure 2.17: Simulation results of the output current direction

In the case of the indirect matrix converter (IMC), as it includes two separate stages, rectifier and inverter, with different circuit configurations, each stage needs a different commutation strategy. In rectification stage which includes six bidirectional switches, as there is no natural freewheeling path, different methods of commutation like two-step or four-step commutations can be applied. However, for the inversion stage which does not include bidirectional switches, the diodes that are connected in anti-parallel with the switches act as freewheeling paths. So the energy stored in the load can always be discharged even when none of the switching devices are gated. As a result, it is possible to apply the dead time commutation strategy in the inverter stage by introducing a time gap between the incoming and the outgoing switches [65] [81, 82]. During the time gap both of the mentioned switches are 'off' and so there is no short-circuit in the imaginary dc-link. Although the dead-time commutation can be applied to the rectification as well, it needs protection circuits like clamp circuits and snubbers.

2.5.1 Output current direction based four-step semi-soft commutation method

The four-step commutation is one of the first commutation methods proposed based on the knowledge of the output current direction. Figure 2.17 shows the simulation

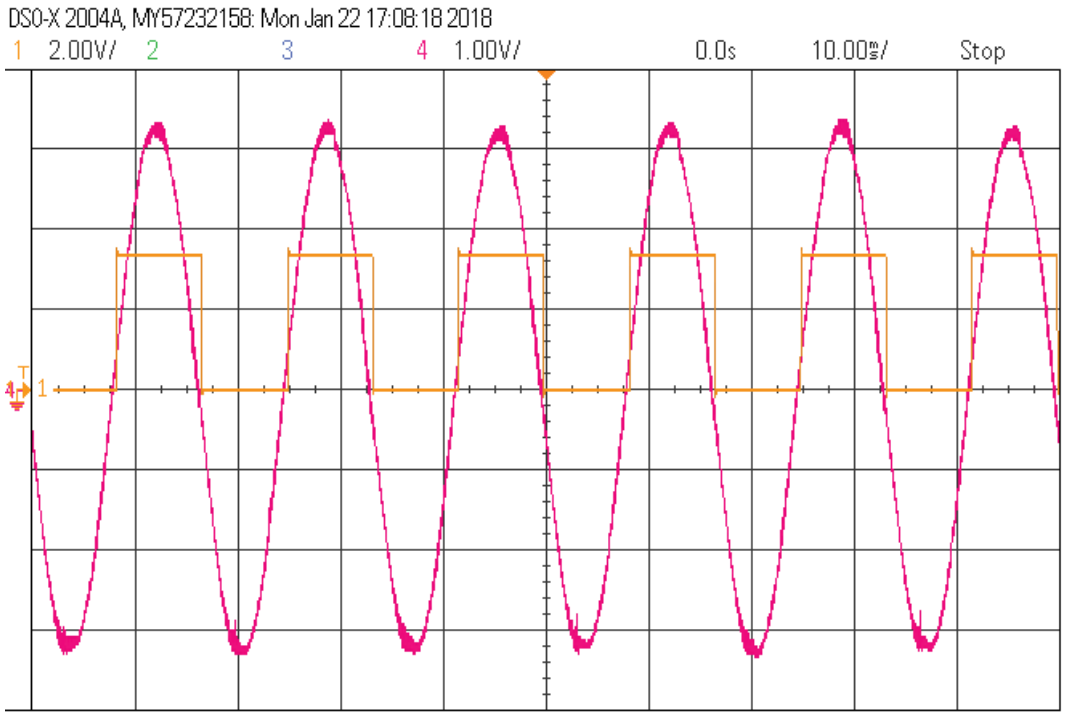


Figure 2.18: Experimental result of the output current i_y and its direction

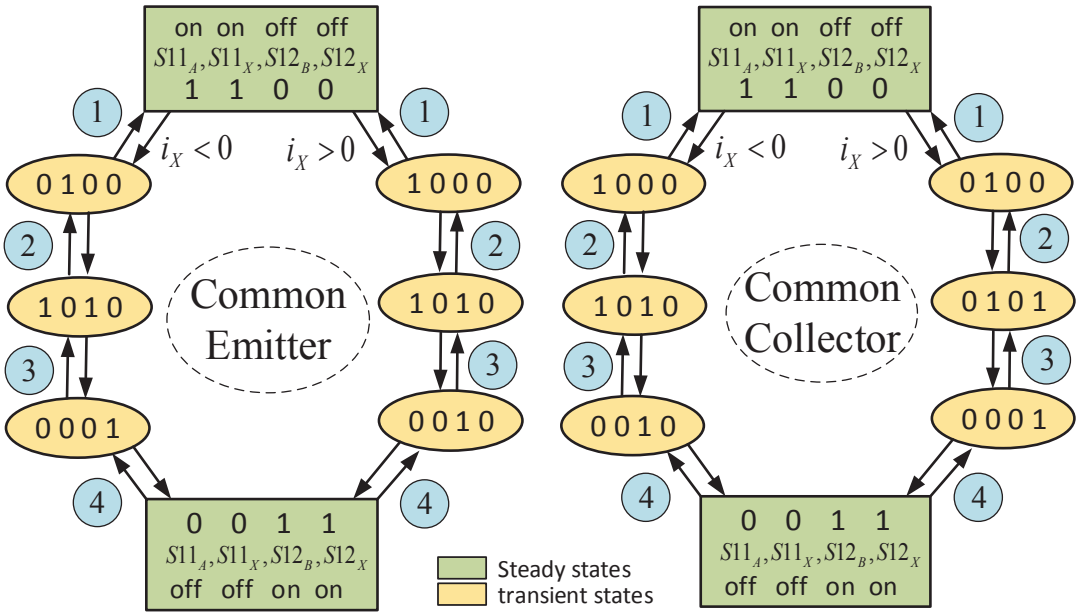


Figure 2.19: State diagram of the soft-switching four-step commutation strategy for both switch cell arrangements

results of the output current direction and Figure 2.18 presents the experimental result. As illustrated in Figure 2.19 both of the IGBTs in the bidirectional switches are 'on' during the steady state and in four individual steps the current transfers to the other bidirectional switch. Figure 2.20 illustrates the common-collector arrangement when S11 is 'on' and S12 is 'off' and, the current flow is in the direction $i_X > 0$. When commutation is needed from S11 to S12, the current sign is used to determine the non-conducting device in the outgoing bidirectional switch which in this case is $S11_A$. Thus, $S11_A$ is turned 'off' in the first step. As there is no current flow through $S11_A$, the output current is not interrupted.

Then the second step is turning 'on' the device that will be conducting ($S12_x$) in the incoming switch S12. In this step depending on the magnitudes of v_{SA} and $v_{SB}(t)$ the current can flow through $S12_X$. If $v_{SA}(t) > v_{SB}(t)$ the load current will flow in S11 otherwise it will flow through S12 and, there is no short circuit.

The third step is to turn 'off' the originally conducting switch $S11_X$ that it forces the current to flow through the incoming switch if it did not happen in the second step because S11 is 'off' entirely. Finally, the fourth step is turning on the other device $S11_B$ in the incoming switch which by this way the current can flow in both directions. Each step occurs after a short time (short enough) to complete the process of turning 'on' or 'off' the needed switch. Figure 2.21 shows the timing diagram of the commutation for both current directions $i_X > 0$ and $i_X < 0$ when the switching arrangement is common-collector. As can be observed the experimental result presented in Figure 2.22 confirms the above-mentioned timing diagram. Also, for common-emitter arrangement, this process is illustrated in Figure2.20. The state diagram of the illustrated steps is shown in Figure 2.19 for both switch cell arrangements of common-collector and common-emitter and both directions under the assumption that initially S11 is 'on' and S12 is 'off'. When the current direction is opposite ($i_X < 0$) these steps are different as demonstrated in Figure 2.23. Four-step commutation process for one output phase is shown in Figure 2.24 for the common-collector arrangement.

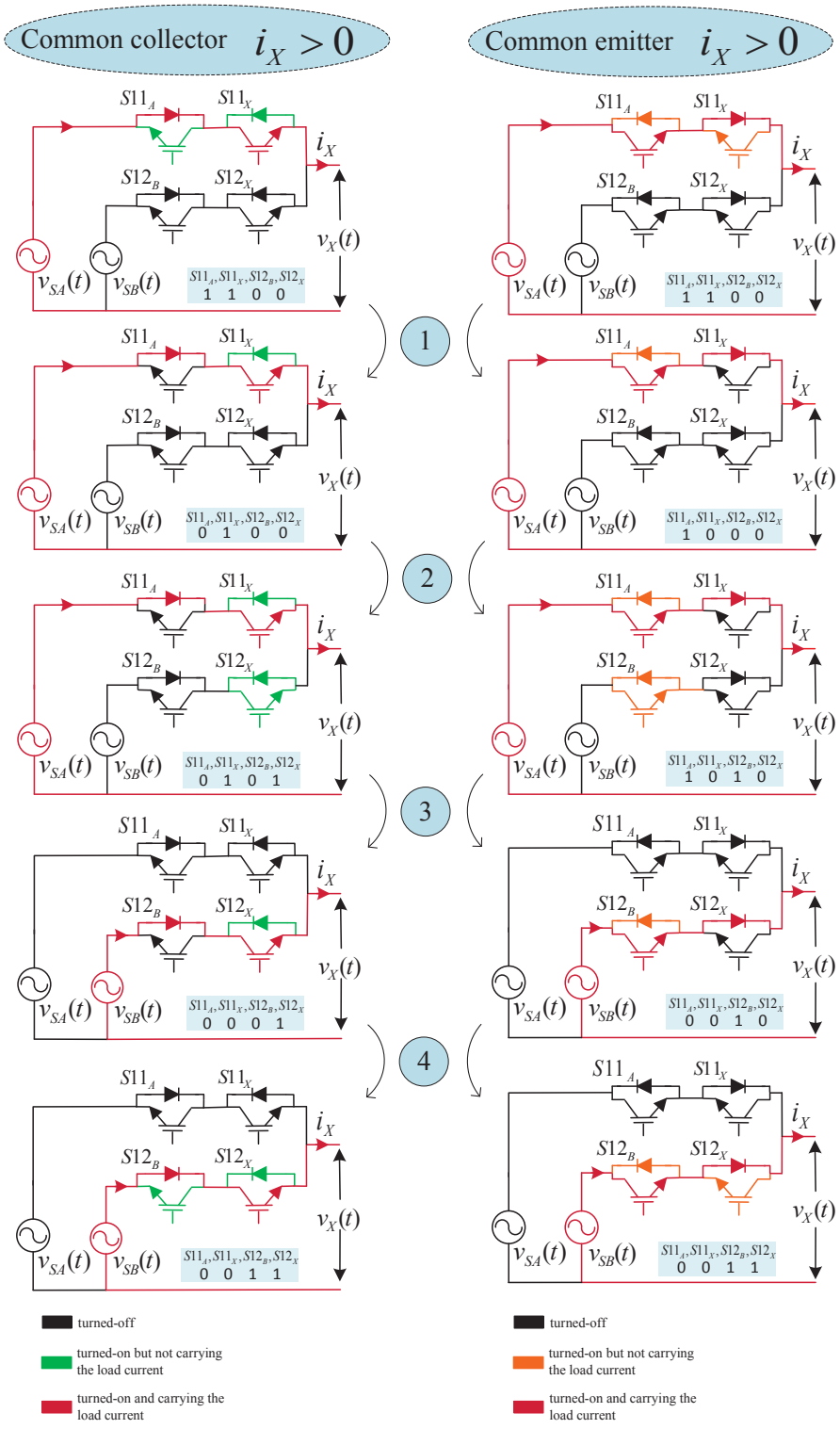


Figure 2.20: Four step semi-soft commutation of the bidirectional switches for a two-phase to single-phase DMC, when the current direction is toward the load $i_x > 0$ (common-collector and common-emitter modes)

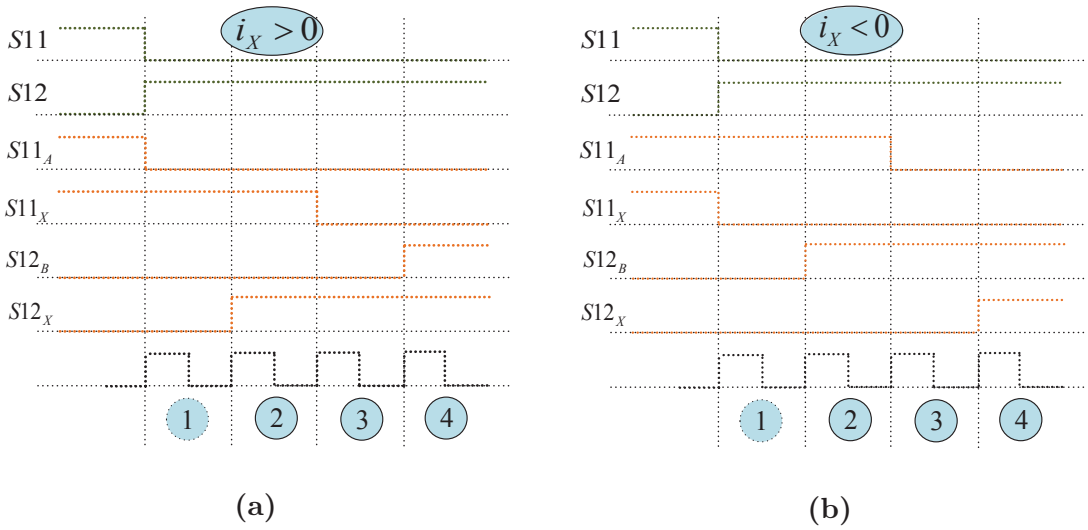


Figure 2.21: Timing diagram of the four-step commutation strategy for common-collector switch cell arrangement, where a) $i_x > 0$, and b) $i_x < 0$

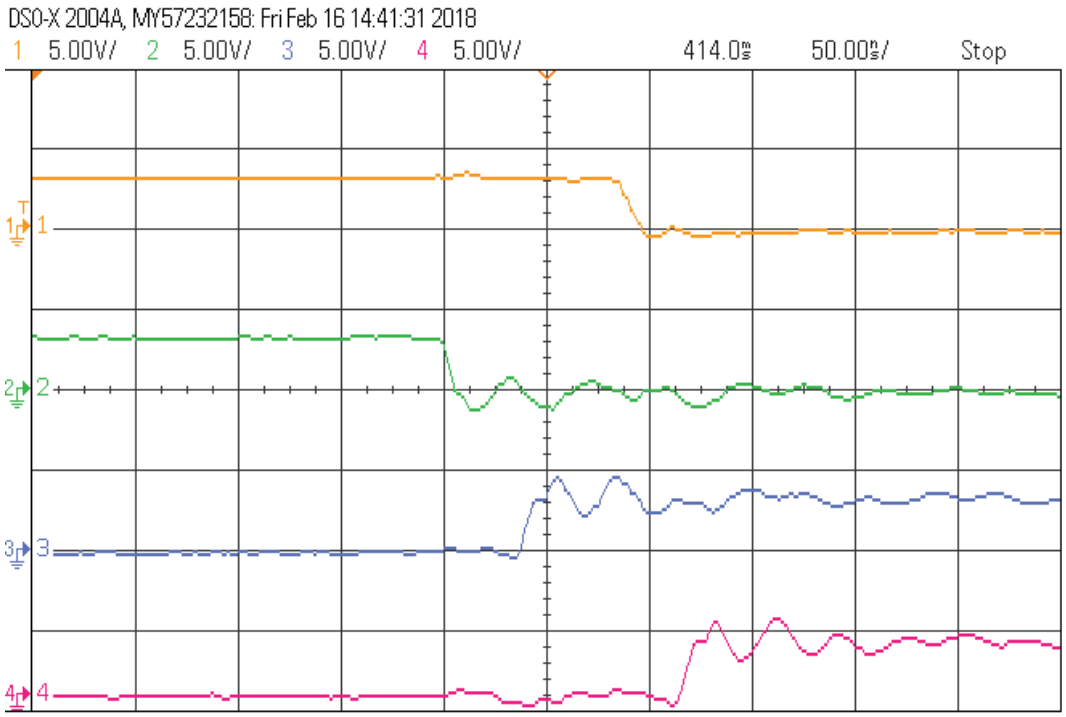


Figure 2.22: Experimental result of the four-step semi-soft commutation

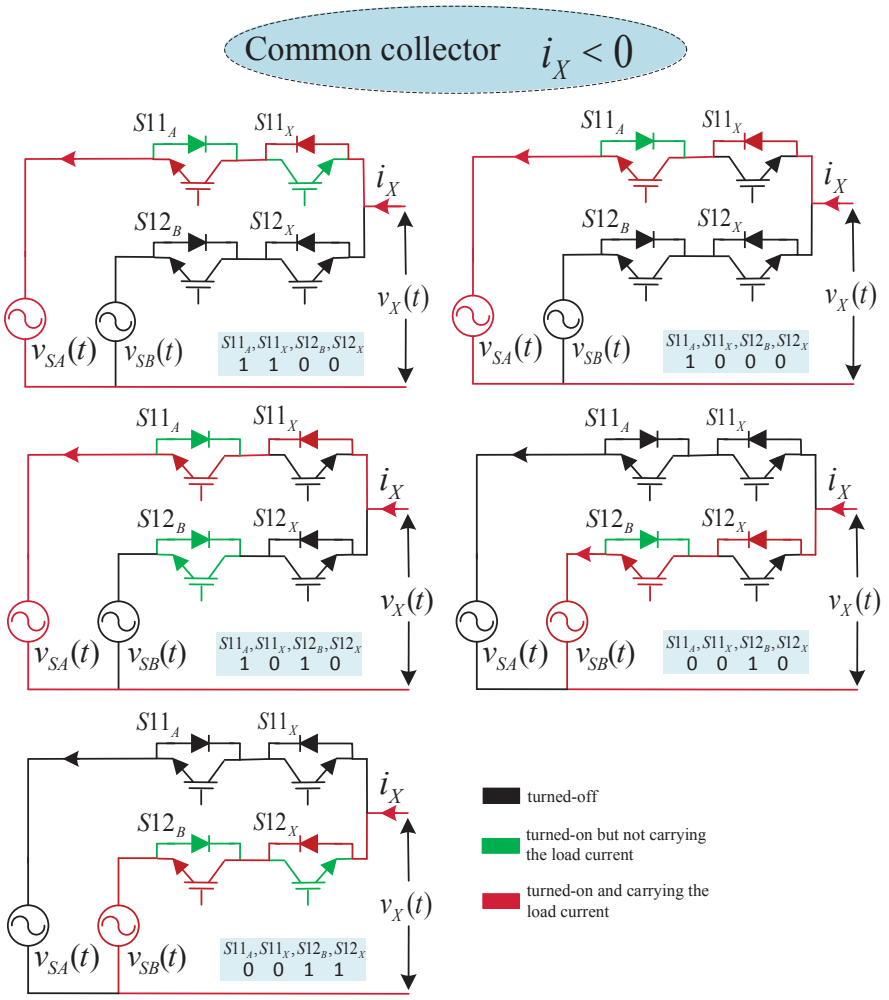


Figure 2.23: Four-step semi-soft commutation of the bidirectional switches for a two-phase to single-phase DMC when the current direction is from the load (common-collector)

The current commutation can occur in the second step if $v_{SB}(t) > v_{SA}(t)$ and as a result turning 'off' the switch S11 is soft because both of its devices are turned 'off' when carrying no current. In this case, turning on the $S12_X$ is hard as it is turned on when carries the current. But if in the second step $v_{SB}(t) > v_{SA}(t)$, bidirectional switch S11 will turn 'off' completely in the third step while $S11_X$ carries the current and current commutation happens at the third step. In this case, $S11_X$ has a hard turn 'off' but turning on the $S12_X$ is soft as there is no current flow through it. That is why the current based 4-step commutation is a semi-soft commutation [65]. As the chance of reverse bias is 50%, so there will be 50% reduction in the average

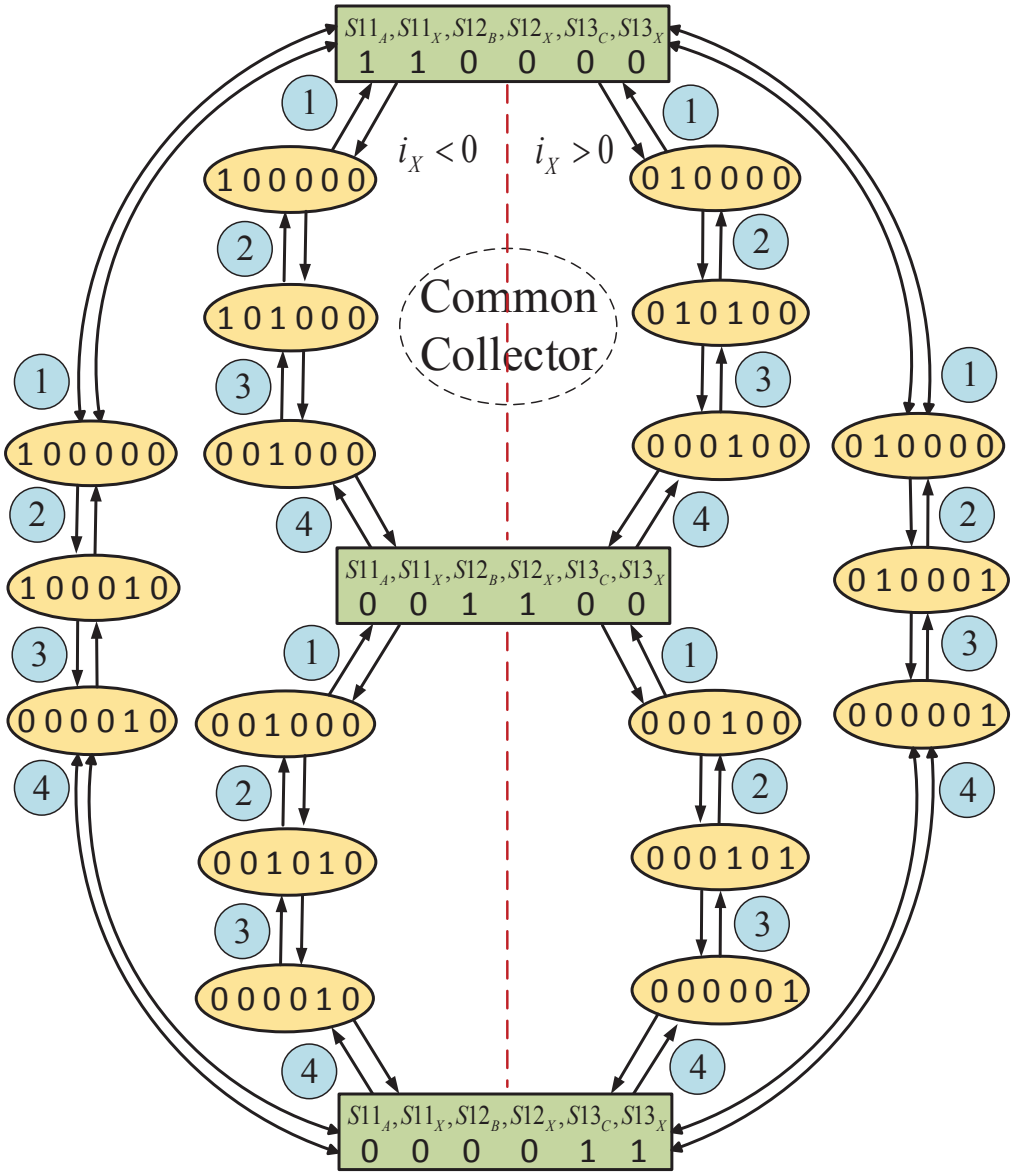


Figure 2.24: State diagram of the semisoft-switching four-step commutation strategy for a three-phase to single-phase DMC

switching losses by using the semi-soft commutation.

The illustrated commutation technique relies on the output current direction which flows through the conducted bidirectional switch, and this knowledge is important as it defines which IGBT carries the current and which one is idle. The current direction defines the switching order. Current sensing using the existing

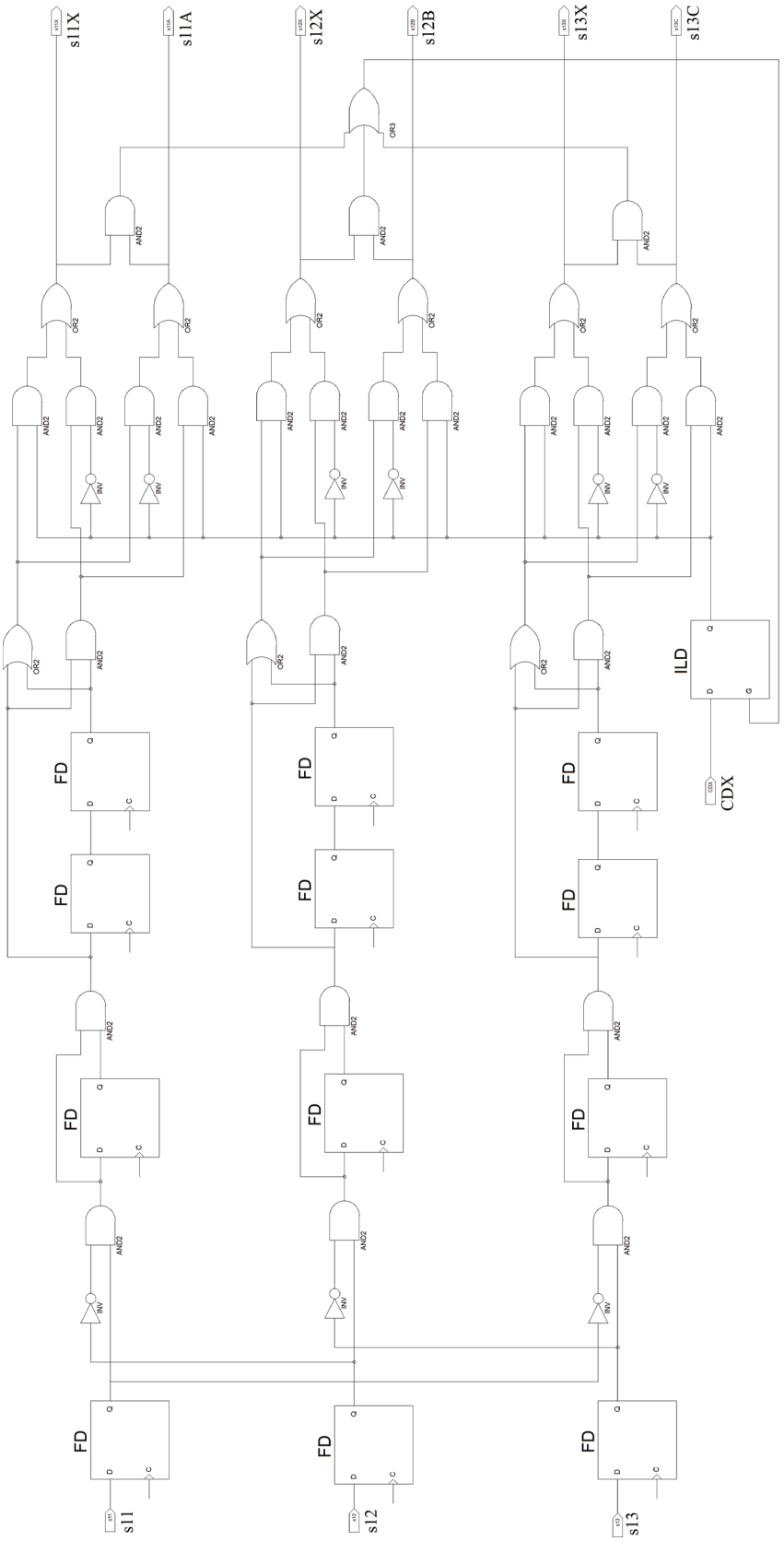


Figure 2.25: Schematic of the four-step commutation strategy for a three-phase to single-phase DMC using the logic elements [5]

sensors like Hall effect ones is difficult at very low current levels or when the current crossing the zero level while is distorted. In these situations the result of the current direction detection is inaccurate, and it causes an open circuit in the output path. The over-voltage caused by the output open circuit can be handled using a clamp circuit and snubbers as it happens at very low currents. Also, there are some other techniques proposed to solve this problem. Some of them have different solution for detecting the current direction like the method presented in [83] that uses the voltage sign across the bidirectional switches to determine the current direction and allows the current direction detection at very low current levels. In this method, it needs the measurement of the voltage drop across the IGBTs of the conducting bidirectional switch. When any of the IGBTs carries the current, the voltage polarity and value is different compare to the nonconducting IGBT. By comparing the voltage drop across the two IGBTs in the conducting bidirectional switch, the current direction can be found more accurately. Also, for very low current levels, it is possible to switch to the dead-time commutation.

If current direction changes during the commutation steps, it can result in the wrong switching order. To overcome this issue, the current sign information can be latched during the commutation process. Latching the information about the output current direction can cause a short interruption in the current but, as the current is close to zero, it does not cause any problem using the clamp circuit. Figure 2.25 illustrates a simple implementation of the soft-switching four-step commutation strategy for one output phase(X) [5].

2.5.2 Two-step semi-soft commutation method

The illustrated current-based four-step commutation strategy allows the output current to flow in both directions automatically as the method turns on both of the IGBTs of the conducting bidirectional switch. By considering the current direction, at any current commutation of two bidirectional switches, there are two nonconductive IGBTs which do not carry the current, and the turn-on and turn-off

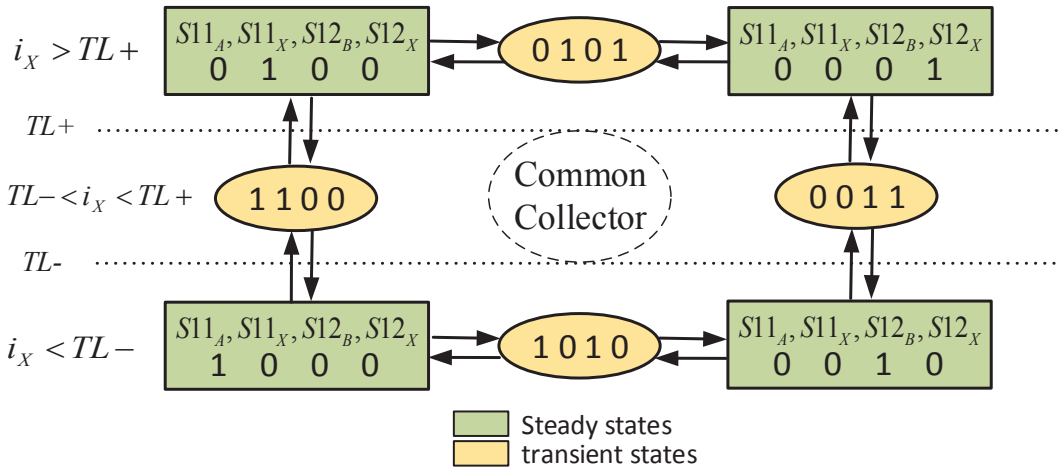


Figure 2.26: State diagram of the current-direction based two-step commutation strategy for two bidirectional switches

operations of them are almost useless. Two steps of the four-step commutation for turning 'on' and 'off' the non-conductive switches slow down the switching process and by reducing the number of steps the commutation process will be faster.

In the threshold two-step commutation as illustrated in [83], just the conducting IGBT is switched 'on' and the other one which does not carry the current stays 'off' until the current direction changes. Figure 2.26 shows the state diagram of the two-step commutation strategy. In the steady state, as can be seen in Figure 2.26, only one IGBT of four IGBTs in Figure 2.16 is 'on' and when a current commutation is needed from S11 to S12, first the conducting IGBT of the incoming bidirectional switch turns on and at the second step the conducting IGBT of the outgoing bidirectional switch turns off. Thus, after the two steps, there is only one conducting IGBT among the four IGBTs.

In step one if $v_{SB}(t) > v_{SA}(t)$ the current commutation happens in the first step and turning on the IGBT in the incoming switch is hard and consequently turning off the IGBT in the outgoing switch is soft. If in the first step $v_{SA}(t) > v_{SB}(t)$, the opposite happens and in both of the cases there is one hard switching and one soft, and so this commutation is a semi-soft commutation.

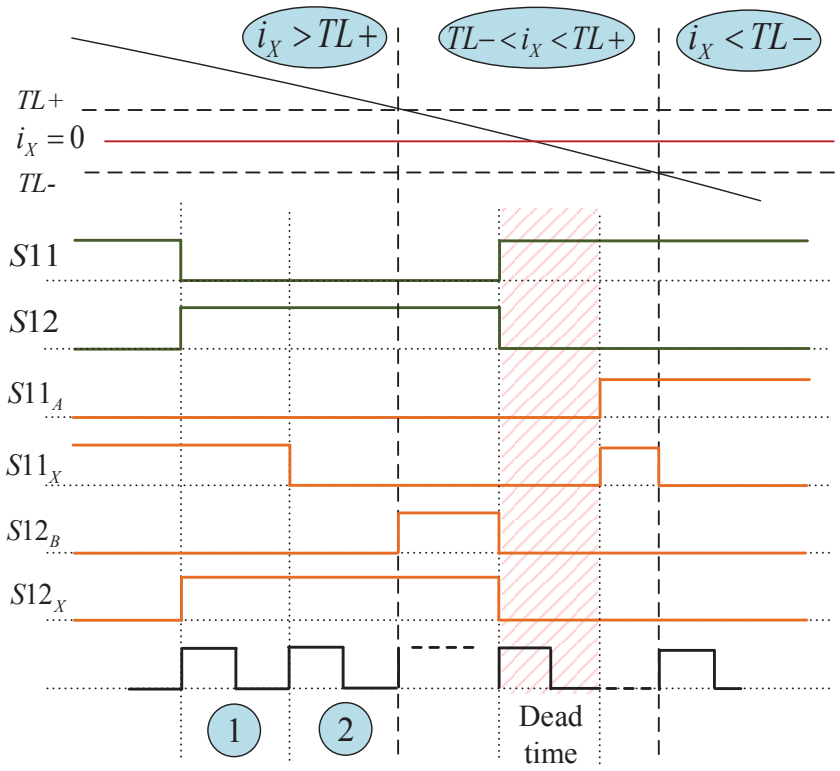


Figure 2.27: Timing diagram of the current direction based two-step commutation when the commutation is needed within the threshold levels

In order to have bidirectional current flow, knowing the accurate current direction is necessary. However, because of the ripples caused by PWM, the detection process of output current zero-crossing is difficult. So two threshold levels near zero are considered (TL+ and TL-), and when the output current crosses one of the threshold levels, the other IGBT in the conducting switch is turned on as well, and so within the two threshold levels both of the IGBTs of the conducting bidirectional switch are 'on'. When the output current crosses the other threshold level, the non-conducting IGBT is switched off as explained by the timing diagram in Figure 2.28.

However, as presented in the timing diagram in Figure 2.28, there is no current commutation between the bidirectional switches within the threshold levels ($TL- < i_x < TL+$). The current direction is unknown within these levels because of the ripples, and so defining the incoming and outgoing IGBTs is impossible, and as a

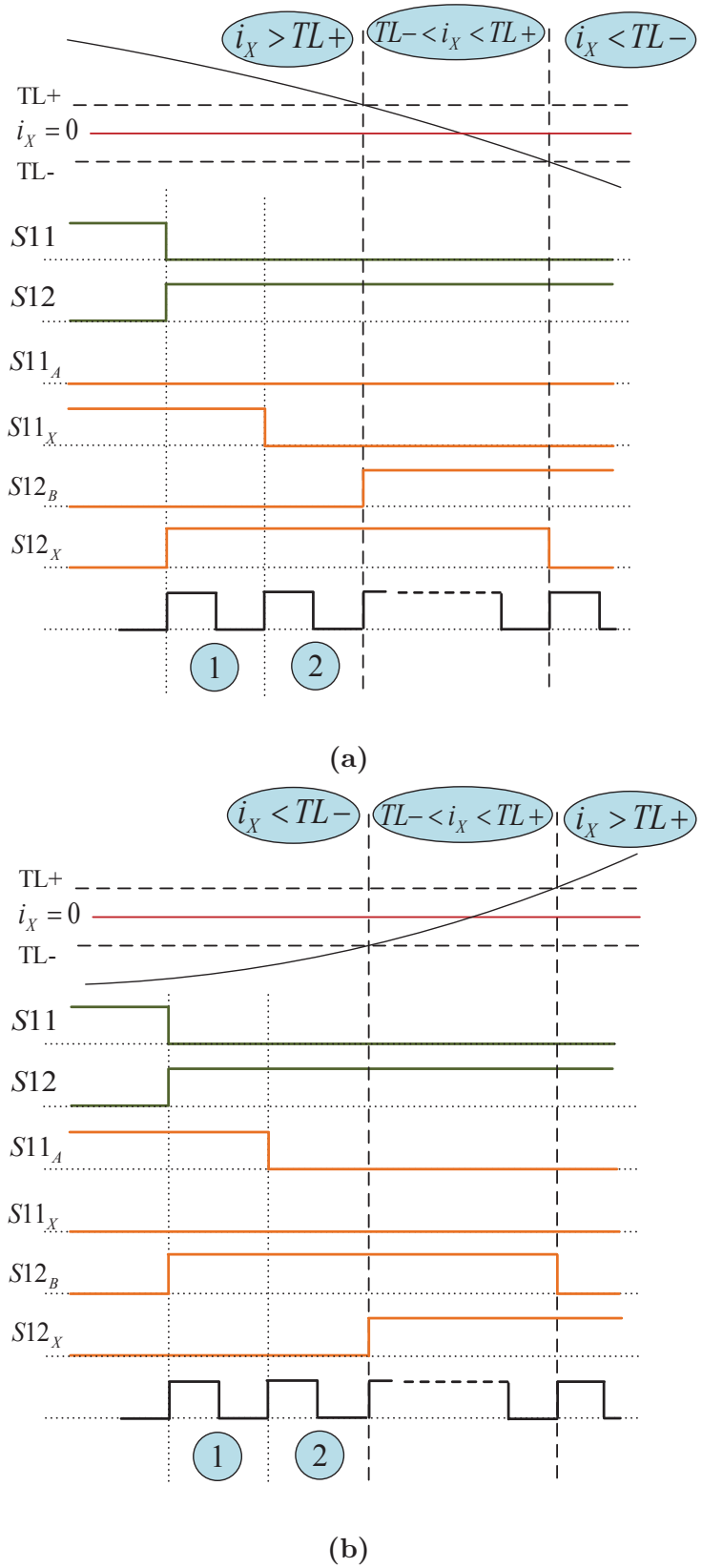


Figure 2.28: Timing diagram of two-step commutation for common-collector switch cell arrangement a) $i_x > 0$ b) $i_x < 0$

result, current commutation cannot carry out correctly within the threshold levels. It is possible to perform the commutation within the threshold levels using a dead time when the current commutation is required as illustrated in Figure 2.27. So, having the clamping circuit and snubbers across the switches are necessary.

2.5.3 Overlap current commutation method

This simple commutation strategy has two steps as is illustrated by the timing diagram in Figure 2.29a [83]. When a current commutation is needed, first the IGBTs of the incoming bidirectional switch are switched 'on' at the same time and at the second step the IGBTs of the outgoing bidirectional switch are turned 'off'. Figure 2.29b shows the state diagram of the commutation.

Although in this method the output phases are always connected, and so allows bidirectional current flow, two of the input supply phases are shorted together for a moment. This problem can be solved by increasing the supply inductance to limit the input current during the short circuit, but as the inductors are heavy and expensive, the solution causes extra cost and weight in the converter [83].

2.5.4 Dead-time current commutation method

In this commutation similar to the overlap method, the current commutation happens in two steps, but when a current commutation is needed, first both of the IGBTs of the outgoing switch are switched off, and in the second step the IGBTs of the incoming switch are turned on simultaneously [83] as shown in the state diagram of Figure 2.30b. There is a dead-time between the two steps as illustrated by the timing diagram in Figure 2.30a.

Now the problem is the dead time that within that moment the output phases are open circuited. To solve the problem the switches need snubbers to overcome the generated over-voltage spikes. The energy loss and increasing the converter volume are the disadvantages of this strategy.

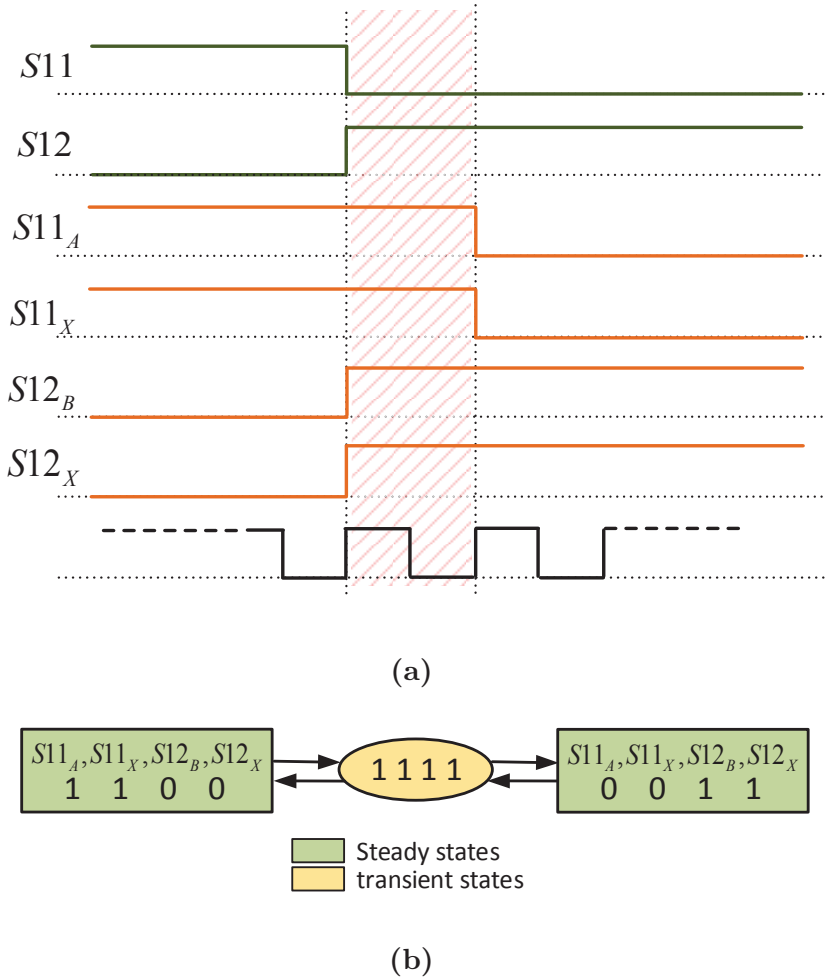


Figure 2.29: Overlap current commutation, where a) Timing diagram, and b) state diagram

2.5.5 Input voltage polarity based commutation method

Similar to the output current sign based four-step commutation, this strategy is a semi-soft four-step commutation technique, but it relies on the knowledge of the polarity of the input source voltages for a safe current commutation [78]. According to this strategy, the conducting and nonconducting IGBTs of the bidirectional switches are determined using the input voltage polarity. Referring to Figure 2.16 for the presented current direction, when the current commutation is needed, at first the input voltages polarity must be determined.

Based on the state diagram illustrated in Figure 2.31, for current commutation

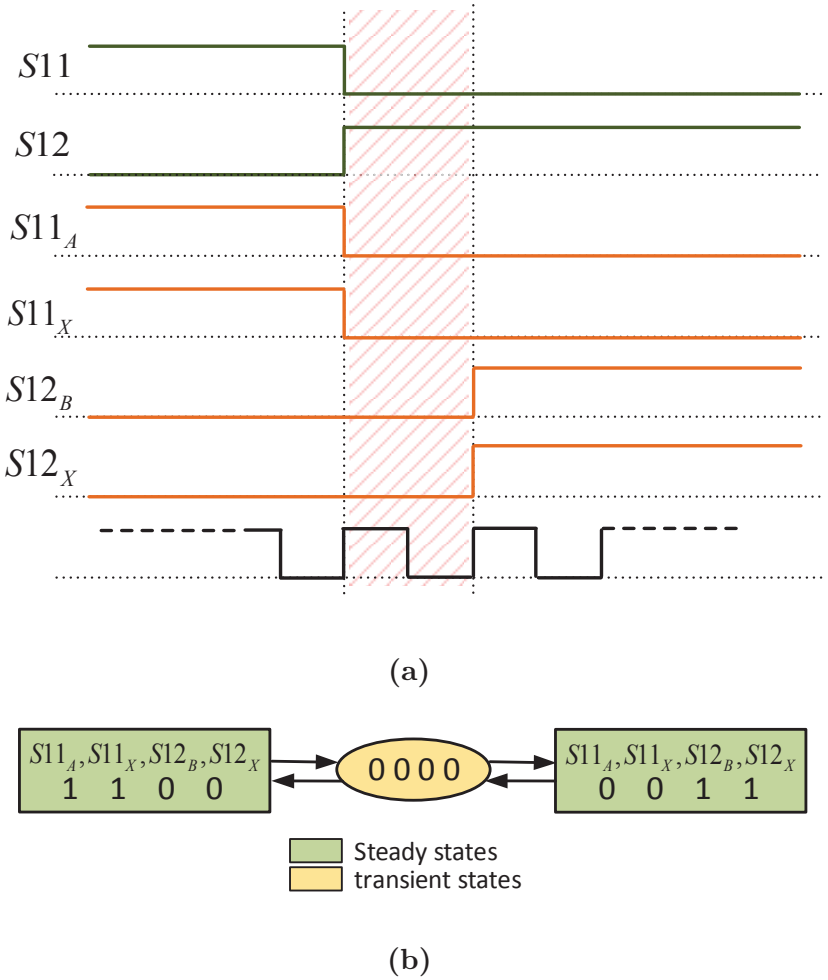


Figure 2.30: Dead-time current commutation, where a) Timing diagram, and b) state diagram

from S11 to S12, when $v_{SA}(t) > v_{SB}(t)$, at the first step the conducting IGBT in the incoming switch ($S12_X$) is turned on. Because of the voltage polarity, the current commutation does not happen at this step and so turning on $S12_X$ is soft. At the second step, the conducting IGBT ($S11_X$) of the outgoing bidirectional switch (S11) is switched off, and it forces the current to flow in the incoming switch (S12), so that the current commutation occurs at this time. At this step due to the current flow in $S11_X$, it is a hard turn-off. The nonconducting IGBT ($S12_B$) in the incoming switch is turned on at the third step to allow the bidirectional current flow and finally at the last step ($S11_A$) which is the nonconducting device in the outgoing switch can

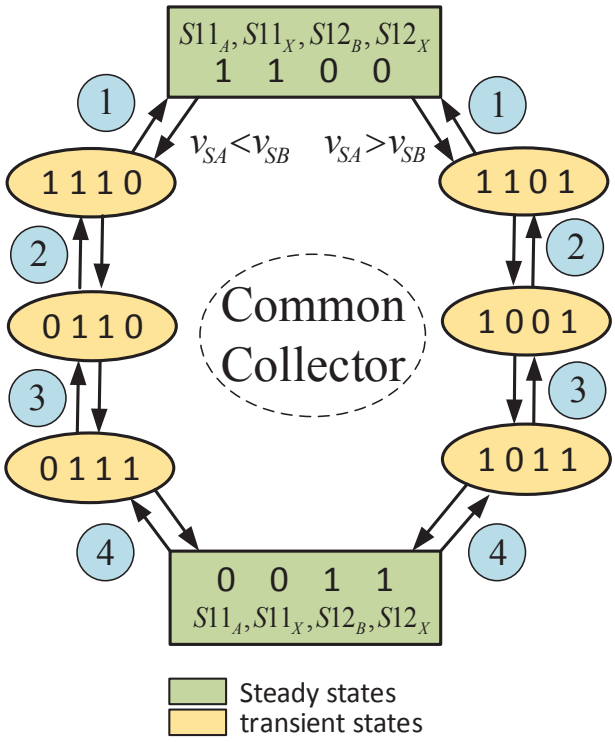
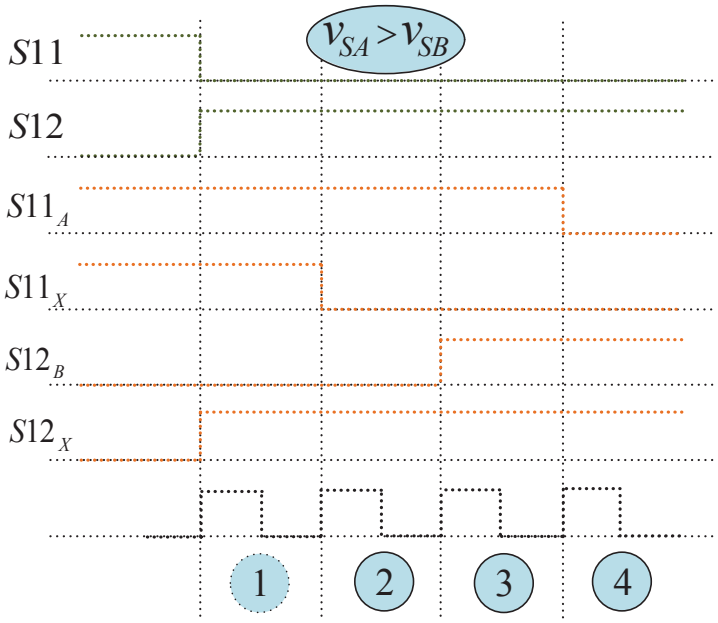


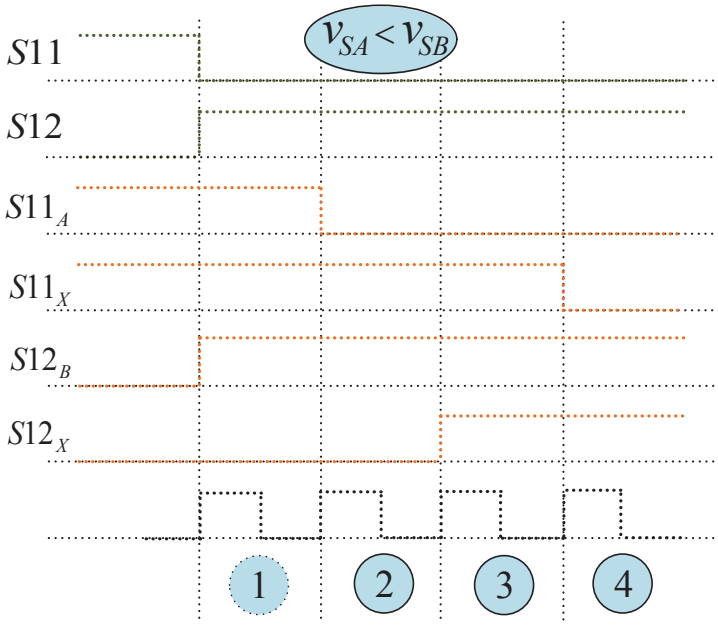
Figure 2.31: State diagram of the voltage-polarity based four-step commutation strategy for two bidirectional switches

be turned off to complete the process. Turning on $S12_B$ and turning off $S11_A$ both are soft as none of them carries the current at that time. In the similar way, the current commutation when $v_{SA}(t) < v_{SB}(t)$ can be analyzed as demonstrated by the state diagram presented in Figure 2.31. Figure 2.32 shows the timing diagram of the commutation for both $v_{SA}(t) > v_{SB}(t)$ and $v_{SA}(t) < v_{SB}(t)$ when the current commutes from S11 to S12.

Input voltage polarity based four-step commutation is a safe method for current commutation between two bidirectional switches if the polarity of the input voltages is measured correctly. Otherwise due to the wrong selection of the IGBTs a short circuit is formed because it causes two bidirectional switches to be turned on simultaneously. Therefore like the current direction-based commutation strategy which needs a reliable measurement of the output current, the voltage sign-based method requires accurate measurement of the input voltage. Although, in the



(a)



(b)

Figure 2.32: Timing diagram of the voltage-polarity based four-step commutation strategy for common-collector switch cell arrangement, where a) $v_{SA} > v_{SB}$, and b) $v_{SA} < v_{SB}$

voltage polarity-based commutation method the bidirectional current path always exists, the precise detection of voltage polarity is difficult near zero crossing, and as a result, the short-circuiting of the input and discharging the filter capacitors are destructive for the semiconductors. Unlike the current-sign based techniques which overvoltage caused by the output open circuit occurred at the very low currents near zero, and could be handled using clamp circuits, the input short circuit and the generated over current are still harmful to the converter.

If voltage polarity changes during the commutation steps, unlike the current direction based commutation, the information about the voltage polarity cannot be latched during the commutation steps as it causes a short circuit in the input and overcurrent happens. The input voltage polarity information must be changed when the polarity changes, and if an open circuit happens, the resultant overvoltage can be handled by using the clamp circuit. An input voltage polarity based two-step commutation method has been proposed in [84] by eliminating two steps of the illustrated commutation strategy.

2.6 Conclusion

The basic parts of the MC technology such as the input filter, protection circuits and bidirectional switches have been presented in this chapter. Some bidirectional switch modules designed and manufactured by some companies have been introduced as a solution for the commercial MC. Also, the problem of the input filter design for the MC has been explained using passive elements, although an optimised design of the MC input filter is a quite difficult task. In order to maintain the high input power factor, the filter capacitance has to be minimised. On the other hand, to meet the required attenuation specifications, the filter inductance has to be increased, but the impedance interaction between the input filter and the converter should be controlled to achieve the system stability.

In order to design a stable and reliable power converter some protection schemes

for protecting the MC against the overvoltage and the overcurrent that might be destructive for the semiconductor devices are presented. The commutation methods are studied in detail. By using these techniques the commutations is performed in steps, avoiding short-circuit and open-circuit situations as the bidirectional switch configurations do not provide safe operation automatically. These strategies are based on either the relative magnitude of the commutating voltages or the direction of the output current. Some details on the implementation of the four-step commutation strategy on a programmable logic device have been given by a schematic diagram using the flip-flops and logic gates.

Although commutation strategies prevent overvoltage spikes in the bidirectional switches in normal conditions, freewheeling path is still needed to safely commutate the output current, when the output is disconnected due to an emergency shutdown of the converter. Thus, a clamp circuit made up of a capacitor connected to all input and output lines through two diodes bridges is proposed that can protect the bidirectional switches from the surges coming from the input and output sides.

Chapter 3

MODULATION METHODS, SIMULATIONS AND EXPERIMENTAL RESULTS

3.1 Introduction

Modulation is one of the main issues of the converters including MCs. Open-loop control strategies of MCs are the modulation methods which control the converter to generate the desired reference waveform. On the other hand, Closed-loop control strategies include a combination of both, modulation and control of the output (or input) parameters like current, voltage or power. Different modulation methods for direct and indirect matrix converters have been introduced in the literature [36–39, 67, 69, 85–95]. The modulation methods determine how the bidirectional switches which arranged to connect the input phases to the output legs can be switched. Every modulation method should generate sinusoidal input currents and be able to control the input power factor. Also, it should control the magnitude and frequency of the output voltages. This chapter will investigate some of the common modulation methods of MCs. The performance of each method will be analyzed by using the simulation models. Also, some experimental tests have been carried out on a prototype direct matrix converter which has been designed for this purpose, and the numerical results have been verified by the experimental tests. At first, the basics of Alesina-Venturini method are introduced, followed by the simulation

and experimental results. After that, the Alesina-Venturini optimum method is reviewed in brief. Then, space vector modulation (SVM) for DMCs is presented in detail based on direct space vector modulation (DSVM) and indirect space vector modulation (ISVM) strategies.

For all modulation methods a set of sinusoidal input voltages and an assumed set of output currents are considered as following:

$$V_i(t) = \begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix} = \begin{bmatrix} V_{im}\cos(\omega_i t) \\ V_{im}\cos(\omega_i t - \frac{2\pi}{3}) \\ V_{im}\cos(\omega_i t - \frac{4\pi}{3}) \end{bmatrix} \tag{3.1}$$

$$I_o(t) = \begin{bmatrix} i_X(t) \\ i_Y(t) \\ i_Z(t) \end{bmatrix} = \begin{bmatrix} I_{om}\cos(\omega_o t - \varphi_o) \\ I_{om}\cos(\omega_o t - \varphi_o - \frac{2\pi}{3}) \\ I_{om}\cos(\omega_o t - \varphi_o - \frac{4\pi}{3}) \end{bmatrix} \tag{3.2}$$

where V_{im} and ω_i are the input voltage amplitude and angular frequency, ω_o and φ_o are the output angular frequency and displacement angle. The modulation problem is finding a modulation matrix such that the input currents and output voltages are:

$$I_i(t) = \begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} = \begin{bmatrix} I_{im}\cos(\omega_i t - \varphi_i) \\ I_{im}\cos(\omega_i t - \varphi_i - \frac{2\pi}{3}) \\ I_{im}\cos(\omega_i t - \varphi_i - \frac{4\pi}{3}) \end{bmatrix} \tag{3.3}$$

$$V_o(t) = \begin{bmatrix} v_X(t) \\ v_Y(t) \\ v_Z(t) \end{bmatrix} = \begin{bmatrix} V_{om}\cos(\omega_o t) \\ V_{om}\cos(\omega_o t - \frac{2\pi}{3}) \\ V_{om}\cos(\omega_o t - \frac{4\pi}{3}) \end{bmatrix} \tag{3.4}$$

where φ_i is the input displacement angle. If q is the voltage gain, the output voltage amplitude is:

$$V_{om} = qV_{im} \tag{3.5}$$

Therefore, the output line voltages are:

$$\begin{bmatrix} v_{XY}(t) \\ v_{YZ}(t) \\ v_{ZX}(t) \end{bmatrix} = \begin{bmatrix} V_{om}\cos(\omega_o t + \frac{\pi}{6}) \\ V_{om}\cos(\omega_o t + \frac{\pi}{6} - \frac{2\pi}{3}) \\ V_{om}\cos(\omega_o t + \frac{\pi}{6} - \frac{4\pi}{3}) \end{bmatrix} \tag{3.6}$$

3.2 Alesina-Venturini Modulation Method

This high-frequency switching strategy which was proposed by Alesina and Venturini in 1980 [38] [36], controls the MC using a direct transfer function method. They presented this AC/AC converter as a matrix of bidirectional switches and named it as 'Matrix Converter'. In this modulation approach, the output voltages are calculated directly by multiplication of the modulation matrix with the input voltages. The method was further modified to increase the voltage transfer ratio from 0.5 to 0.866.

The output voltage waveforms are composed of samples of the input voltages with a sampling rate much higher than input and output frequencies. The instantaneous relationships between input and output quantities are:

$$\begin{bmatrix} v_X(t) \\ v_Y(t) \\ v_Z(t) \end{bmatrix} = \begin{bmatrix} S_{XA} & S_{XB} & S_{XC} \\ S_{YA} & S_{YB} & S_{YC} \\ S_{ZA} & S_{ZB} & S_{ZC} \end{bmatrix} \begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix} \tag{3.7}$$

$$\begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} = \begin{bmatrix} S_{XA} & S_{YA} & S_{ZA} \\ S_{XB} & S_{YB} & S_{ZB} \\ S_{XC} & S_{YC} & S_{ZC} \end{bmatrix} \begin{bmatrix} i_X(t) \\ i_Y(t) \\ i_Z(t) \end{bmatrix} \tag{3.8}$$

The switching function of a single switch is defined as [67]:

$$S_{kj} = \begin{cases} 1 & switch\, S_{kj}\, on \\ 0 & switch\, S_{kj}\, off \end{cases} \tag{3.9}$$

$$\sum_{j=A,B,C} S_{kj}(t) = 1 \quad , k = \{X, Y, Z\} \tag{3.10}$$

It means that only one switch per columns must be closed at any instant to prevent input terminals from short-circuiting. On the other hand, because of inductive nature of the load, the output current should not be interrupted suddenly, so at least one switch of each column must be closed [67] [69]. Figure 3.1 shows the switching pattern of the *kth* output phase in Venturini method. The duty cycle of the switch S_{kj} represented as $m_{kj}(t)$ can be defined as:

$$m_{kj}(t) = \frac{t_{kj}}{T_s} \qquad j = \{A, B, C\},\ k = \{X, Y, Z\}, \quad 0 \leq m_{kj}(t) \leq 1 \tag{3.11}$$

$$T_s = t_{kA} + t_{kB} + t_{kC} \tag{3.12}$$

where t_{kj} is the conduction time of switch $S_{kj}(t)$ during the switching period T_s. The design aim is to define $m_{kj}(t)$ such that the resultant three output phase voltages in (3.4) match closely the desired three-phase reference voltages. The low-frequency transfer matrix is defined by:

$$M(t) = \begin{bmatrix} m_{XA} & m_{XB} & m_{XC} \\ m_{YA} & m_{YB} & m_{YC} \\ m_{ZA} & m_{ZB} & m_{ZC} \end{bmatrix} \tag{3.13}$$

The operation of the system can be modeled by an average model when the swtching frequency is significantly higher than the input and output frequencies. In this manner, the average value of each switching function equals with its duty cycle. The low-frequency component (mean value calculated over one sampling interval) of the *kth* output phase voltage and output voltage vector are respectively as the following:

$$\bar{v}_{kN} = \begin{bmatrix} \frac{t_{kA}}{T_s} & \frac{t_{kB}}{T_s} & \frac{t_{kC}}{T_s} \end{bmatrix} \begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix} \tag{3.14}$$

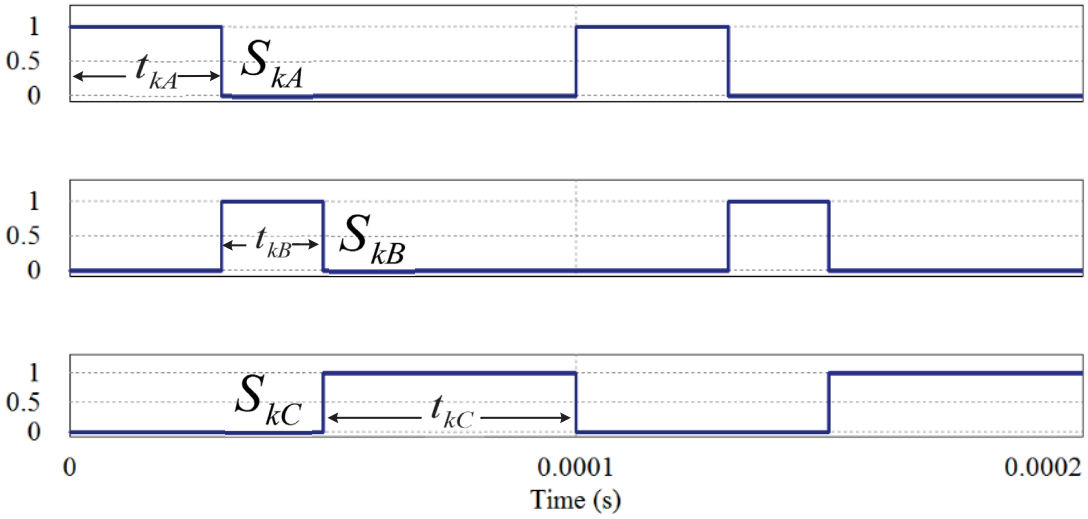


Figure 3.1: Switching pattern of the *kth* output phase in Venturini method

$$\bar{V_o} = M(t).V_i(t) \tag{3.15}$$

And the low-frequency input current vector using the transpose of the matrix $M(t)$ is:

$$\bar{I_i} = M^T.I_o(t) \tag{3.16}$$

There are two modulation matrixes $M(t)$, the first one results the same phase displacement angle at the input and output ($\varphi_i = \varphi_o$), but the second one gives reversed phase displacement ($\varphi_i = -\varphi_o$) [36, 38, 67]:

$$M_1 = \frac{1}{3}\begin{bmatrix} 1+2q\cos(\omega_m t) & 1+2q\cos(\omega_m t-\frac{2\pi}{3}) & 1+2q\cos(\omega_m t-\frac{4\pi}{3}) \\ 1+2q\cos(\omega_m t-\frac{4\pi}{3}) & 1+2q\cos(\omega_m t) & 1+2q\cos(\omega_m t-\frac{2\pi}{3}) \\ 1+2q\cos(\omega_m t-\frac{2\pi}{3}) & 1+2q\cos(\omega_m t-\frac{4\pi}{3}) & 1+2q\cos(\omega_m t) \end{bmatrix}$$

$$\omega_m = (\omega_o - \omega_i) \tag{3.17}$$

$$M_2 = \frac{1}{3}\begin{bmatrix} 1+2q\cos(\omega_m t) & 1+2q\cos(\omega_m t-\frac{2\pi}{3}) & 1+2q\cos(\omega_m t-\frac{4\pi}{3}) \\ 1+2q\cos(\omega_m t-\frac{2\pi}{3}) & 1+2q\cos(\omega_m t-\frac{4\pi}{3}) & 1+2q\cos(\omega_m t) \\ 1+2q\cos(\omega_m t-\frac{4\pi}{3}) & 1+2q\cos(\omega_m t) & 1+2q\cos(\omega_m t-\frac{2\pi}{3}) \end{bmatrix}$$

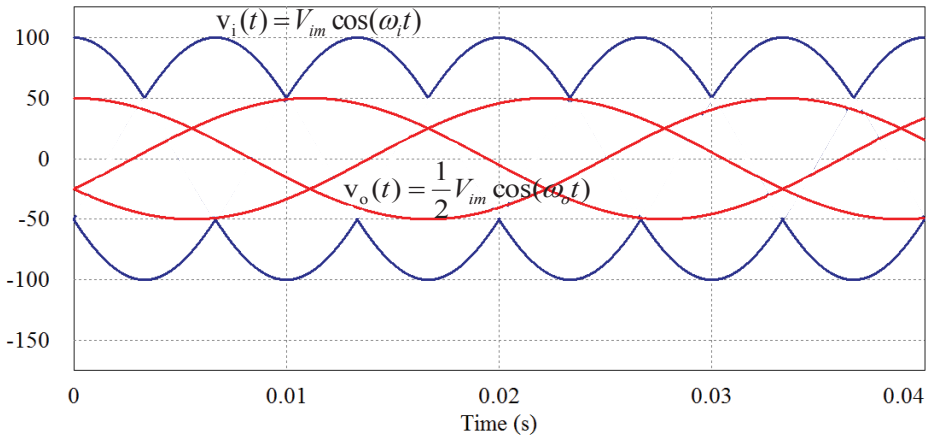


Figure 3.2: Sinusoidal output voltages ($\bar{v}_{kN}$), fitting into input three-phase voltages

$$\omega_m = -(\omega_o + \omega_i) \tag{3.18}$$

For input displacement factor control these two solutions should be combined. In case of practical implementation, duty cycles can be defined directly in terms of the input voltages and the reference output voltages with unity displacement factor as the following:

$$m_{kj}(t) = \frac{t_{kj}}{T_s} = \frac{1}{3}\left[\ 1 + 2\frac{v_j(t)\bar{v}_{kN}(t)}{V_{im}^2}\ \right] \quad j = \{A, B, C\}, k = \{X, Y, Z\} \tag{3.19}$$

The desired output reference voltages should ensure that the maximum voltage transfer ratio is obtained. To achieve this, the reference output voltage waveform must remain within an envelope formed by the three-phase input voltages at any time, as shown in Figure 3.2. Thus, the maximum achievable output-to-input voltage ratio is restricted to 0.5.

3.2.1 Alesina-Venturini optimised method

As the voltage gain (q) of the converter using the Venturini method cannot exceed from 0.5, for increasing the voltage gain to $q = \sqrt{3}/2 = 0.866$, Venturini proposed adding a proportion of the third harmonic components of the output and input frequencies, resulting in the following expression [39]:

$$V_o(t) = \begin{bmatrix} v_X(t) \\ v_Y(t) \\ v_Z(t) \end{bmatrix} = V_{om} \begin{bmatrix} \cos(\omega_o t) - \frac{1}{6}\cos(3\omega_o t) + \frac{1}{2\sqrt{3}}\cos(3\omega_i t) \\ \cos(\omega_o t - \frac{2\pi}{3}) - \frac{1}{6}\cos(3\omega_o t) + \frac{1}{2\sqrt{3}}V_{im}\cos(3\omega_i t) \\ \cos(\omega_o t - \frac{4\pi}{3}) - \frac{1}{6}\cos(3\omega_o t) + \frac{1}{2\sqrt{3}}V_{im}\cos(3\omega_i t) \end{bmatrix} \quad (3.20)$$

The optimised Venturini algorithm, including displacement factor control, in Venturini's paper [37] is rather complex and appears unsuited for real-time implementation [25, 96, 97]. By assuming that having a unity input power factor, solving for the modulation matrix M(t) then gives the following form which is applicable for real-time implementation [67]:

$$\begin{aligned} m_{kj}(t) = \frac{t_{kj}}{T_s} = \frac{1}{3}\left[\ 1 + 2\frac{v_j(t)\bar{v}_{kN}(t)}{V_{im}^2} + \frac{4q}{3\sqrt{3}}sin(\omega_i t + \beta_j)sin(3\omega_i t)\ \right] \\ j = \{A, B, C\}, k = \{X, Y, Z\} \quad \beta_j = 0, \frac{2\pi}{3}, \frac{4\pi}{3} \end{aligned} \quad (3.21)$$

For controlling the input displacement factor a phase shift can be added to $v_j(t)$ in (3.21) after input measurement, but power factor not equal to unity, reduces the voltage gain [67].

3.2.2 Simulation results of Alesina-Venturini and its optimised method

Figure 3.3 shows the results of Alesina-Venturini modulation method for the system characteristics mentioned in Table 3.4 and output reference voltage $v_{o,ref} = 195V(line - line)$, which means voltage gain is about 0.48. As can be seen the THDs of the input source and output currents (3.28% and 2.33% respectively) are under 5% and input power factor is very close to unity ($PF_i = 0.967$). Also, output phase voltage v_{xn} and common mode voltage have been presented to be compared with other modulation methods.

Figure 3.4 illustrates the results of Alesina-Venturini optimum modulation method. The simulation results are for output reference voltages $v_{o,ref} = 200V$ (line-line) ($q \approx 0.5$) and $v_{o,ref} = 300V$ (line-line) ($q \approx 0.75$). With regard to the input cur-

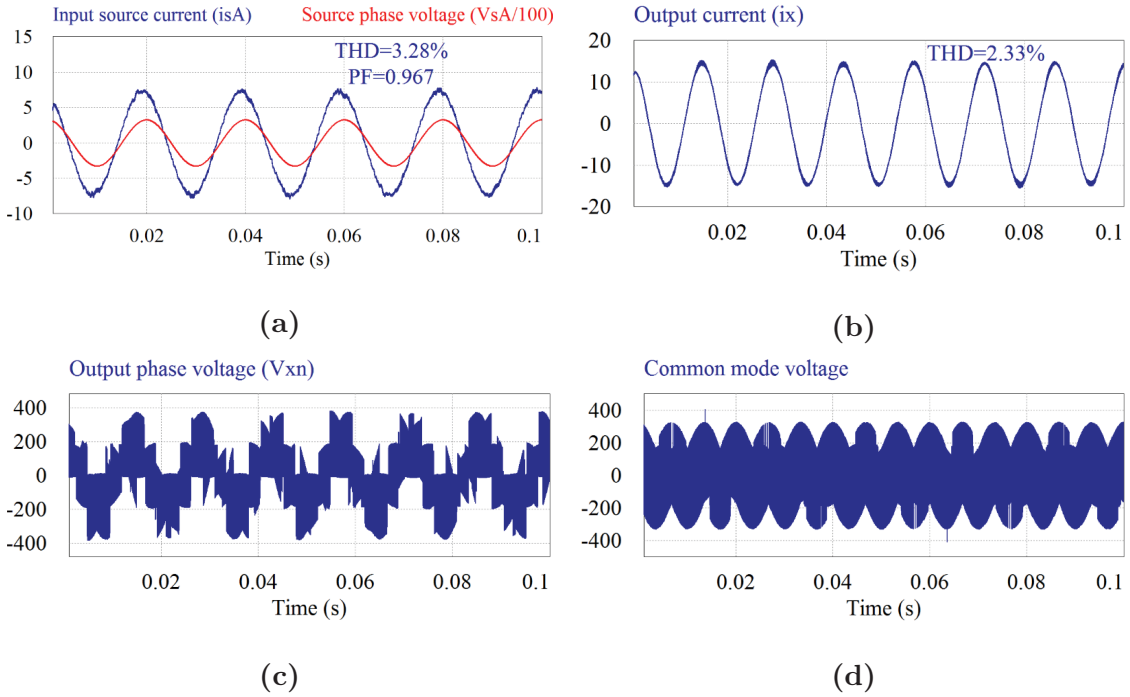


Figure 3.3: Simulation results of Alesina-Venturini method for output reference voltage $v_{o,ref} = 195V(line - line)$, where a) Input source current and voltage of phase (A), b) Output current i_x, c) Output phase voltage v_{xn}, and d) Common mode voltage

rents, it can be noted that for the optimised strategy the waveforms are in sinusoidal form but, even for voltage gain about 0.5 (Figure 3.4a) THD is relatively high. It is also worth noting that in the case of $v_{o,ref} = 300V$, THDs of both input source current and output current are too high, although the input power factor is close to unity. So, although Alesina-Venturini optimised modulation method raised the maximum input-output voltage transfer ratio to 0.867 the currents have significant distortion.

3.3 Space Vector Modulation Method

There are different modulation strategies to synthesise the output reference voltages from the input voltages and the input currents from output currents. One of the most preferred modulations for MCs is the Space Vector Modulation (SVM) because of the better harmonic performance using different switching strategies. There are

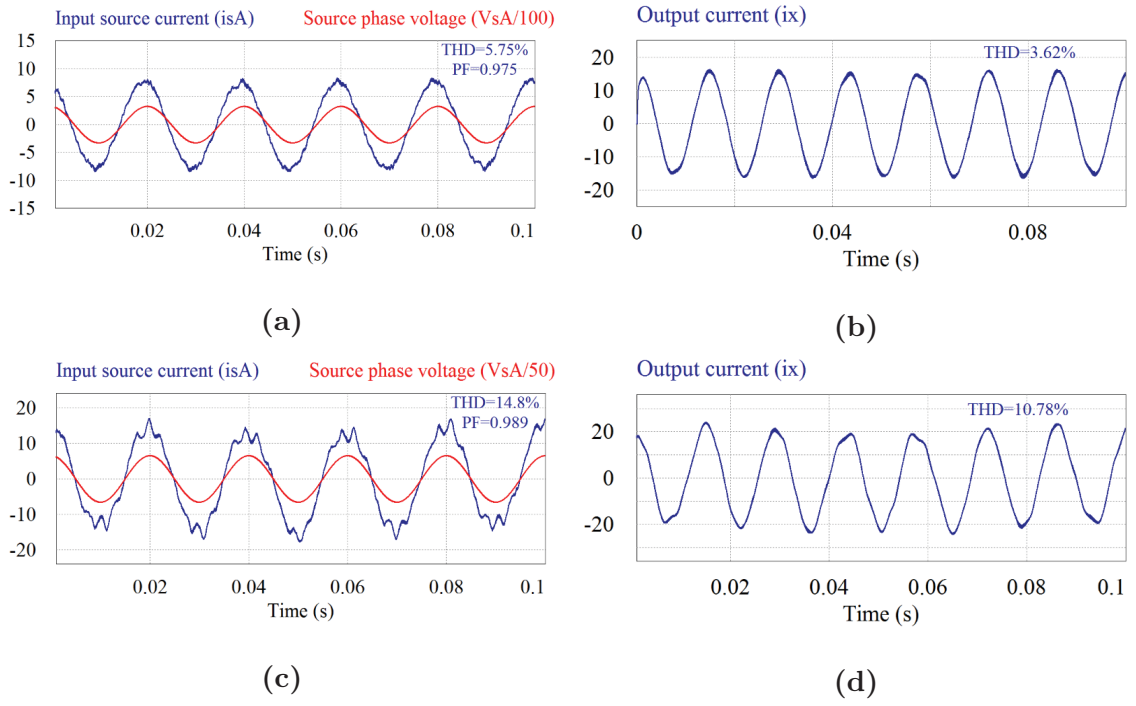


Figure 3.4: Simulation results of Alesina-Venturini optimised method, where a and c) Input source current and voltage of phase (A) when output reference voltage is $v_{o,ref} = 200V$ and $v_{o,ref} = 300V$ (line-line), and b and d) Output current i_x when output reference voltage $v_{o,ref} = 200V$ and $v_{o,ref} = 300V$ (line-line), respectively

two versions of SVM known as, direct SVM (DSVM) and indirect SVM (ISVM). The ISVM for controlling of the MC was first proposed by Huber and Borojevic in 1989 [85]. This method is based on the instantaneous space vectors of the input currents and output voltages. It utilises the rectifier-inverter concept and considers the MC as a two-stage converter. later in 1993, Casadei, Tani *et al.* proposed DSVM strategy which unlike ISVM, does not make use of any imaginary dc-link and the output voltages are directly generated from the input voltages [86].

This section focuses on matrix converter modulation strategies based on SVM. By means of a simulated model, the performance of these methods has been analyzed under the balanced and sinusoidal voltage source. Also, the numerical results have been verified by experimental tests using the matrix converter prototype.

3.3.1 Direct space vector approach

Direct space vector modulation provides independent control of the magnitude and frequency of the output voltages and generates sinusoidal input currents with full control of the displacement angle. As the inductive loads have the low-pass filtering behaviour, the output currents are sinusoidal too. The SVM modulation method is based on space vectors to present three-phase time-variant quantities such as voltage and current in a complex plane [87] [88] [98].

When the three phase of input source are purely sinusoidal and symmetric, and they have a constant angular frequency, the time-varying values of the input currents and the output voltages of the MC, shown in Figure 2.6, can be transformed into the space vectors in a two-axis coordinate as following:

$$\vec{I_i} = \frac{2}{3}[i_A(t) + i_B(t)e^{\frac{j2\pi}{3}} + i_C(t)e^{\frac{j4\pi}{3}}] = I_{im}e^{j(\omega_i t - \varphi_i)} \tag{3.22}$$

$$\vec{V_o} = \frac{2}{3}[v_X(t) + v_Y(t)e^{\frac{j2\pi}{3}} + v_Z(t)e^{\frac{j4\pi}{3}}] = V_{om}e^{j(\omega_o t)} \tag{3.23}$$

where $\vec{I_i}$ and $\vec{V_o}$ are the input current and the output voltage space vectors as shown in Figure 3.5.

A DMC with nine bidirectional switches involves $2^9 = 512$ switching states, but Considering the rules of avoiding input short circuit and output open circuit, to avoid over-voltage spikes, there are only 27 safe switching combinations for a DMC as presented in Table 3.1. Among the 27 switching states, in the first 18 states, three output phases are connected to only two input phases at any duty cycle. For example, considering state(-5), the output voltage space vector can be obtained as the following:

$$\begin{bmatrix} v_X(t) \\ v_Y(t) \\ v_Z(t) \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix} \times \begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix} \tag{3.24}$$

Table 3.1: Safe switching configurations of DMC and the output voltage and the input current vectors associated with them

states	XYZ	ON switches	$\lvert\vec{v}_o\rvert$	α_o	$\lvert\vec{i}_i\rvert$	β_i
+1	ABB	S11,S22,S32	$2/3\ v_{AB}(t)$	0	$2/\sqrt{3}\ i_X$	$-\pi/6$
-1	BAA	S12,S21,S31	$-2/3\ v_{AB}(t)$	0	$-2/\sqrt{3}\ i_X$	$-\pi/6$
+2	BCC	S12,S23,S33	$2/3\ v_{BC}(t)$	0	$2/\sqrt{3}\ i_X$	$\pi/2$
-2	CBB	S13,S22,S32	$-2/3\ v_{BC}(t)$	0	$-2/\sqrt{3}\ i_X$	$\pi/2$
+3	CAA	S13,S21,S31	$2/3\ v_{CA}(t)$	0	$2/\sqrt{3}\ i_X$	$7\pi/6$
-3	ACC	S11,S23,S33	$-2/3\ v_{CA}(t)$	0	$-2/\sqrt{3}\ i_X$	$7\pi/6$
+4	BAB	S12,S21,S32	$2/3\ v_{AB}(t)$	$2\pi/3$	$2/\sqrt{3}\ i_Y$	$-\pi/6$
-4	ABA	S11,S22,S31	$-2/3\ v_{AB}(t)$	$2\pi/3$	$-2/\sqrt{3}\ i_Y$	$-\pi/6$
+5	CBC	S13,S22,S33	$2/3\ v_{BC}(t)$	$2\pi/3$	$2/\sqrt{3}\ i_Y$	$\pi/2$
-5	BCB	S12,S23,S32	$-2/3\ v_{BC}(t)$	$2\pi/3$	$-2/\sqrt{3}\ i_Y$	$\pi/2$
+6	ACA	S11,S23,S31	$2/3\ v_{CA}(t)$	$2\pi/3$	$2/\sqrt{3}\ i_Y$	$7\pi/6$
-6	CAC	S13,S21,S33	$-2/3\ v_{CA}(t)$	$2\pi/3$	$-2/\sqrt{3}\ i_Y$	$7\pi/6$
+7	BBA	S12,S22,S31	$2/3\ v_{AB}(t)$	$4\pi/3$	$2/\sqrt{3}\ i_Z$	$-\pi/6$
-7	AAB	S11,S21,S32	$-2/3\ v_{AB}(t)$	$4\pi/3$	$-2/\sqrt{3}\ i_Z$	$-\pi/6$
+8	CCB	S13,S23,S32	$2/3\ v_{BC}(t)$	$4\pi/3$	$2/\sqrt{3}\ i_Z$	$\pi/2$
-8	BBC	S12,S22,S33	$-2/3\ v_{BC}(t)$	$4\pi/3$	$-2/\sqrt{3}\ i_Z$	$\pi/2$
+9	AAC	S11,S21,S33	$2/3\ v_{CA}(t)$	$4\pi/3$	$2/\sqrt{3}\ i_Z$	$7\pi/6$
-9	CCA	S13,S23,S31	$-2/3\ v_{CA}(t)$	$4\pi/3$	$-2/\sqrt{3}\ i_Z$	$7\pi/6$
0_1	AAA	S11,S21,S31	0	—	0	—
0_2	BBB	S12,S22,S32	0	—	0	—
0_3	CCC	S13,S23,S33	0	—	0	—
syn1	ABC	S11,S22,S33	V_{im}	$\omega_i t$		
syn2	ACB	S11,S23,S32	V_{im}	$-\omega_i t$		
syn3	BAC	S12,S21,S33	V_{im}	$-\omega_i t + 2\pi/3$		
syn4	BCA	S12,S23,S31	V_{im}	$\omega_i t + 4\pi/3$		
syn5	CAB	S13,S21,S32	V_{im}	$\omega_i t + 2\pi/3$		
syn6	CBA	S13,S22,S31	V_{im}	$-\omega_i t + 4\pi/3$		

$$
\begin{aligned}
\vec{V_o}[-5] =& \frac{2}{3}[v_X(t) + v_Y(t)e^{\frac{j2\pi}{3}} + v_Z(t)e^{\frac{j4\pi}{3}}] \\
=& \frac{2}{3}[v_B(t) + v_C(t)e^{\frac{j2\pi}{3}} + v_B(t)e^{\frac{j4\pi}{3}}] \\
=& \frac{2}{3}[V_{im}\cos(\omega_i t - \frac{2\pi}{3}) + V_{im}\cos(\omega_i t - \frac{4\pi}{3})e^{\frac{j2\pi}{3}} + V_{im}\cos(\omega_i t - \frac{2\pi}{3})e^{\frac{j4\pi}{3}}] \\
=& -\frac{2\sqrt{3}V_{im}\sin(\omega_i t)}{3}e^{\frac{j2\pi}{3}} \\
=& -\frac{2}{3}v_{BC}(t)e^{\frac{j2\pi}{3}}
\end{aligned}
\tag{3.25}
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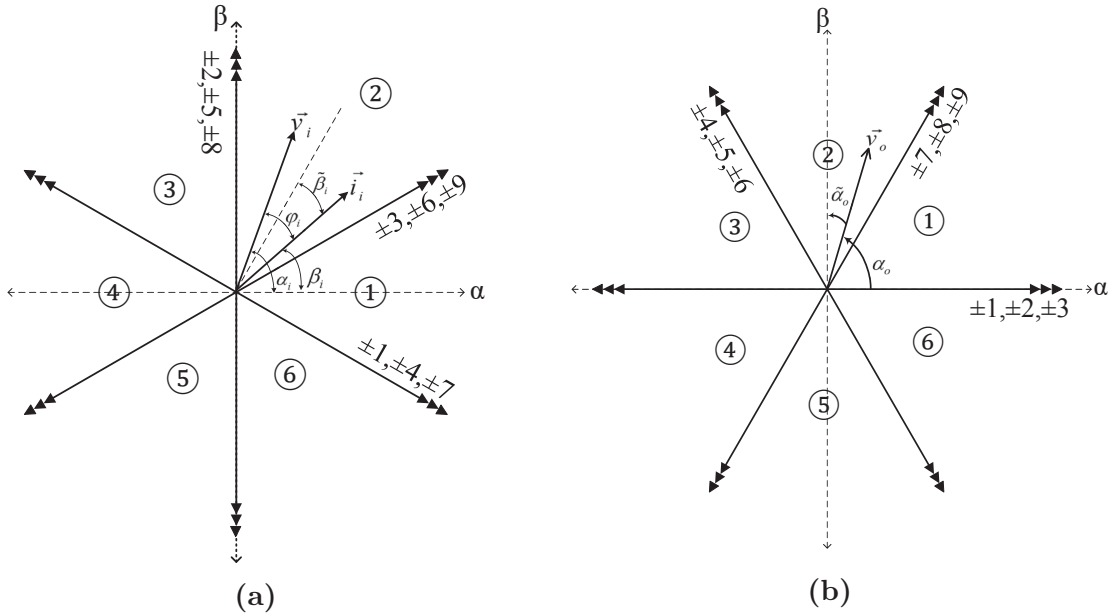


Figure 3.5: Complex space vector for active configurations a) Input current switching vectors b) Output voltage switching vectors

and the input current space vector can be found similarly as:

$$\vec{I}_i[-5] = -\frac{2}{\sqrt{3}} i_Y(t) e^{j\frac{\pi}{2}} \tag{3.26}$$

As can be seen the angles are constant, but the amplitudes depend on the instantaneous values of the input line voltages and output currents and vary with the time. This group of 18 states with fixed directions and variable amplitudes are called "active vectors". In the other three states that are "zero vectors", all output phases are connected to the same input phase voltage and therefore, have zero amplitude and angle. For example, considering the first zero vector as:

$$\begin{bmatrix} v_X(t) \\ v_Y(t) \\ v_Z(t) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix} \times \begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix} \tag{3.27}$$

The output voltage space vector can be found as:

$$\begin{aligned}\vec{V_o}[0_1] &= \frac{2}{3}[v_X(t) + v_Y(t)e^{\frac{j2\pi}{3}} + v_Z(t)e^{\frac{j4\pi}{3}}] \\ &= \frac{2}{3}[v_A(t) + v_A(t)e^{\frac{j2\pi}{3}} + v_A(t)e^{\frac{j4\pi}{3}}] \\ &= \frac{2}{3}[V_{im}\cos(\omega_i t) + V_{im}\cos(\omega_i t)e^{\frac{j2\pi}{3}} + V_{im}\cos(\omega_i t)e^{\frac{j4\pi}{3}}] \\ &= 0\end{aligned} \tag{3.28}$$

Except for these 21 configurations, there are 6 synchronous configurations that each output phase voltage connects to a different input voltage. For example, considering the following output phase voltage vector in the complex space vector plane:

$$\begin{bmatrix} v_X(t) \\ v_Y(t) \\ v_Z(t) \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix} \tag{3.29}$$

The output voltage space vector can be obtained as:

$$\begin{aligned}\vec{V_o}[syn1] &= \frac{2}{3}[v_X(t) + v_Y(t)e^{\frac{j2\pi}{3}} + v_Z(t)e^{\frac{j4\pi}{3}}] \\ &= \frac{2}{3}[v_A(t) + v_B(t)e^{\frac{j2\pi}{3}} + v_C(t)e^{\frac{j4\pi}{3}}] \\ &= \frac{2}{3}[V_{im}\cos(\omega_i t) + V_{im}\cos(\omega_i t - \frac{2\pi}{3})e^{\frac{j2\pi}{3}} + V_{im}\cos(\omega_i t - \frac{4\pi}{3})e^{\frac{j4\pi}{3}}] \\ &= V_{im}[\cos(\omega_i t) + j\sin(\omega_i t] \\ &= V_{im}e^{j\omega_i t}\end{aligned} \tag{3.30}$$

These 6 combinations represent rotating vectors with constant amplitudes but variable directions. The results for all 27 switching configurations are summarised in Table 3.1. According to this table, both the input current and the output voltage active vectors can be expressed in six different directions, with the magnitudes depending upon the output line currents and input line voltages respectively shown in Figure 3.5.

The conventional DSVM method can be applied to the DMC using the active

Table 3.2: Four "active configurations" selected for any combinations of k_i, k_v

Ki \ Kv	1				2				3				4				5				6			
1	+9	-7	-3	+1	-6	+4	+9	-7	+3	-1	-6	+4	-9	+7	+3	-1	+6	-4	-9	+7	-3	+1	+6	-4
2	-8	+9	+2	-3	+5	-6	-8	+9	-2	+3	+5	-6	+8	-9	-2	+3	-5	+6	+8	-9	+2	-3	-5	+6
3	+7	-8	-1	+2	-4	+5	+7	-8	+1	-2	-4	+5	-7	+8	+1	-2	+4	-5	-7	+8	-1	+2	+4	-5
4	-9	+7	+3	-1	+6	-4	-9	+7	-3	+1	+6	-4	+9	-7	-3	+1	-6	+4	+9	-7	+3	-1	-6	+4
5	+8	-9	-2	+3	-5	+6	+8	-9	+2	-3	-5	+6	-8	+9	+2	-3	+5	-6	-8	+9	-2	+3	+5	-6
6	-7	+8	+1	-2	+4	-5	-7	+8	-1	+2	+4	-5	+7	-8	-1	+2	-4	+5	+7	-8	+1	-2	-4	+5
	I	II	III	IV	I	II	III	IV	I	II	III	IV	I	II	III	IV	I	II	III	IV	I	II	III	IV

and zero vectors of the input current and the output voltage [89]. Depending on the input current sector k_i and output voltage sector k_v, there are 36 switching sequences which have been mentioned in Table 3.2. The next step is selecting four suitable active configurations for any combination of input current and output voltage sectors according to the Table 3.2. For example, if both input current and output voltage vectors are in sector 2, the active switching configurations are +5, -6, -8, +9. To achieve the output reference voltage and complete the sampling period T_s, one or more (up to three) zero configuration is applied. In the case of applying just one zero configuration, five switching configurations generate the switching pattern for each switching period T_s. Selecting the zero configuration and the order of the active configurations are very important to reduce the number of switchings in each switching period [90].

For example, if $k_i = k_v = 2$, the switching configurations are +5, -6, -8 and +9. It means that for a switching period T_s the outputs X,Y,Z are connected to the inputs A,B and C in five steps: CBC, CAC, BBC, AAC, 0_n where n=1,2,3. Selecting the zero configuration 0_1 and switching sequence as following for a switching period T_s, minimises the number of switchings as the shift from one switching configuration to the other one is performed by changing only one switch:

-8	+5	-6	+9	0_1
BBC	CBC	CAC	AAC	AAA
III	I	II	IV	0

Figure 3.6 shows the connected switches in the switching pattern using one zero vector. Any switching pattern indicates the order of the switching configurations

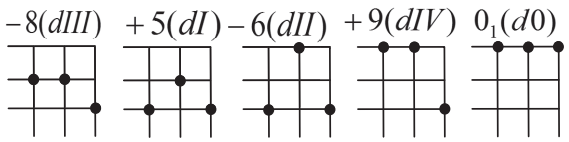


Figure 3.6: Connected switches in case of using one zero configuration

and the number of the applied zero vectors. The switching sequence with three zero configurations can be shown in seven steps as following and Figure 3.7 shows the connected switches.

0_2	-8	+5	0_3	-6	+9	0_1
BBB	BBC	CBC	CCC	CAC	AAC	AAA
0/3	III	I	0/3	II	IV	0/3

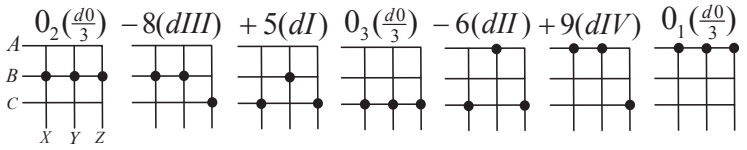


Figure 3.7: Connected switches in case of using three zero configurations

Figure 3.8 illustrates the difference between THD of the input source current and output current using the switching pattern with one or three zeros. The system characteristics are presented in Table 3.4 and the time step of the simulation is $1\mu s$. As can be seen in the diagram, there is no important difference between THDs of the input source current although, the switching pattern with three zeros presented less THD in the output current [95]. Also, Figure 3.9 shows that input power factor varies similarly in both switching patterns and using one or three zero vectors does not have any effect on the input power factor.

The order of the active switching combinations depends on the number of the sectors k_i and k_v. If $k_i + k_v$ is even then this order is III, I, II, IV, but if $k_i + k_v$ is odd, the order is I, III, IV, II.

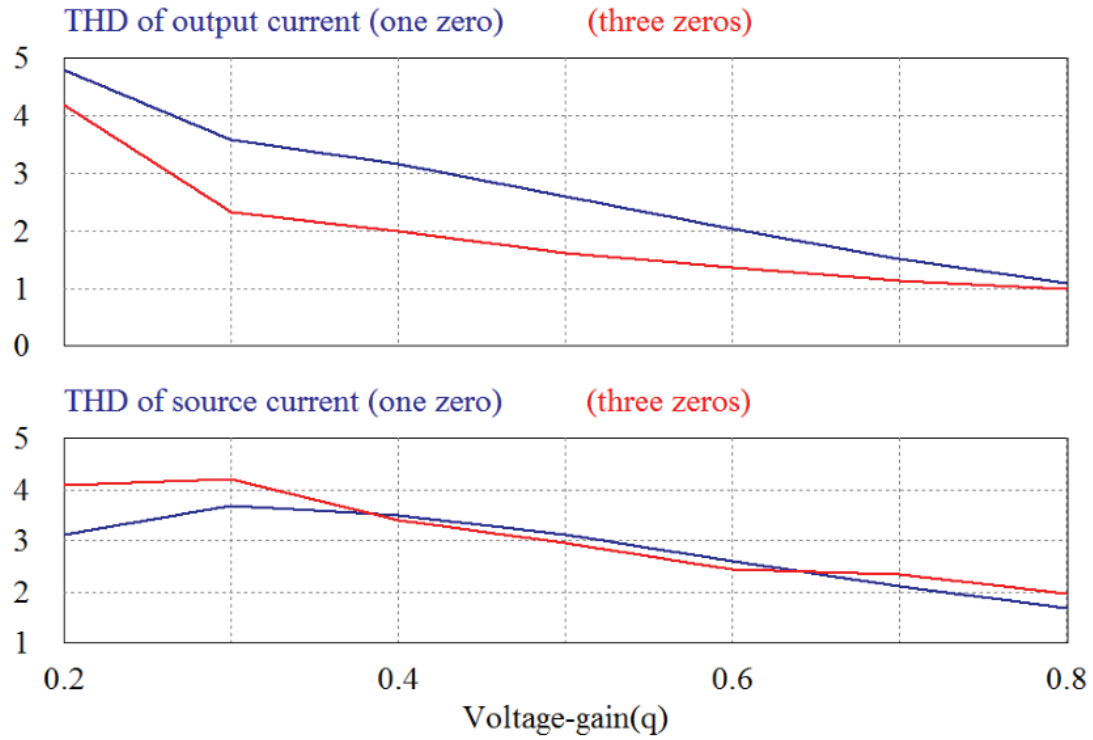


Figure 3.8: THD of the input source current and the output current using the switching pattern with one and three zeros

Considering Table 3.1, for any switching configurations, the output voltage has a specific amplitude and angle. In order to generate the output reference voltage with arbitrary amplitude and frequency, each output phase connects to the three input phases for a specific time duration. It means that for a switching sequence with switching period T_s, each switching configuration has a specific time duration $(t_0, t_1, t_2, t_3, t_4)$. Figures 3.10 and 3.11 illustrate how symmetrically distributed switching pulses are generated and the same results has been shown in Figure 3.12 for the simulated model. The duty cycle of the switching configurations are calculated as:

$$d_I = \frac{t_1}{T_s} = \frac{2}{\sqrt{3}} q \frac{\cos(\tilde{\alpha}_o - \frac{\pi}{3}) \cos(\tilde{\beta}_i - \frac{\pi}{3})}{\cos \varphi_i} \tag{3.31}$$

$$d_{II} = \frac{t_2}{T_s} = \frac{2}{\sqrt{3}} q \frac{\cos(\tilde{\alpha}_o - \frac{\pi}{3}) \cos(\tilde{\beta}_i + \frac{\pi}{3})}{\cos \varphi_i} \tag{3.32}$$

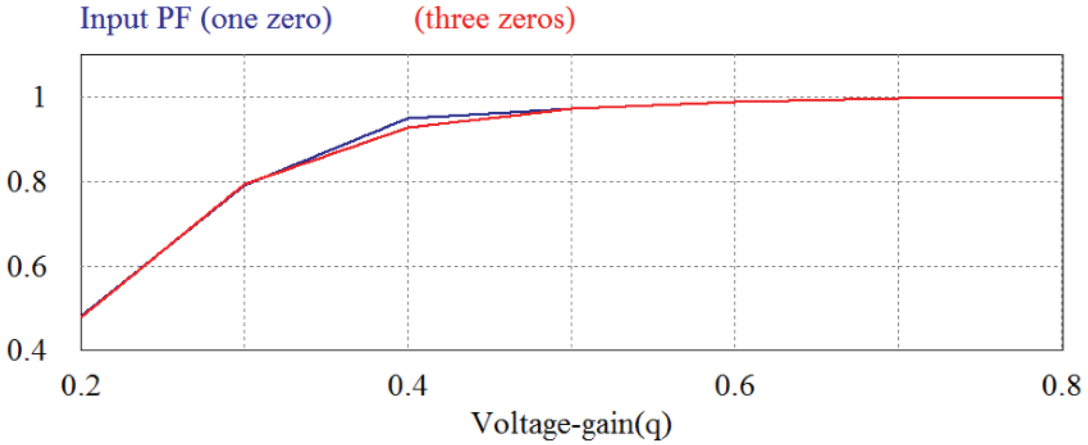


Figure 3.9: Input power factor using the switching pattern with one and three zeros

$$d_{III} = \frac{t_3}{T_s} = \frac{2}{\sqrt{3}} q \frac{\cos(\tilde{\alpha}_o + \frac{\pi}{3}) \cos(\tilde{\beta}_i - \frac{\pi}{3})}{\cos \varphi_i} \tag{3.33}$$

$$d_{IV} = \frac{t_4}{T_s} = \frac{2}{\sqrt{3}} q \frac{\cos(\tilde{\alpha}_o + \frac{\pi}{3}) \cos(\tilde{\beta}_i + \frac{\pi}{3})}{\cos \varphi_i} \tag{3.34}$$

$$d_0 = \frac{t_0}{T_s} = 1 - (d_I + d_{II} + d_{III} + d_{IV}) \tag{3.35}$$

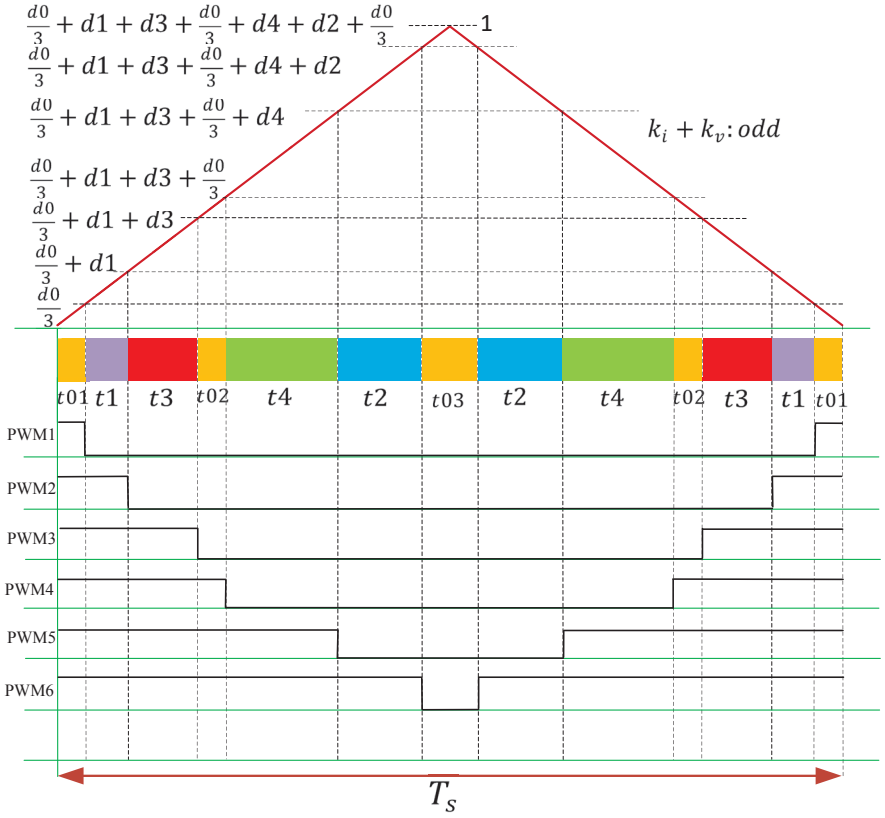
$$q = \frac{V_{om}}{V_{im}} \leq \frac{\sqrt{3}}{2} \cos \varphi_i \tag{3.36}$$

where $\tilde{\beta}_i$ and $\tilde{\alpha}_o$ are the phase angles of the input current and the output voltage vectors respectively with referred to the bisecting line of the corresponding sector as illustrated in Figure 3.5 ($-\frac{\pi}{6} < \tilde{\alpha}_o < +\frac{\pi}{6}$, $-\frac{\pi}{6} < \tilde{\beta}_i < +\frac{\pi}{6}$) [89] and the output voltage space vector can be defined accordingly as:

$$\vec{V_o} = d_I \vec{V_1} + d_{II} \vec{V_2} + d_{III} \vec{V_3} + d_{IV} \vec{V_4} + d_0 \vec{V_0} \tag{3.37}$$

For switching pattern with three zero vectors, the duty cycle d_0 is divided equally among them. For example for output phase X and $k_i = k_v = 2$, the following switches are connected for the specific times as presented in Table 3.3:

(a)



(b)

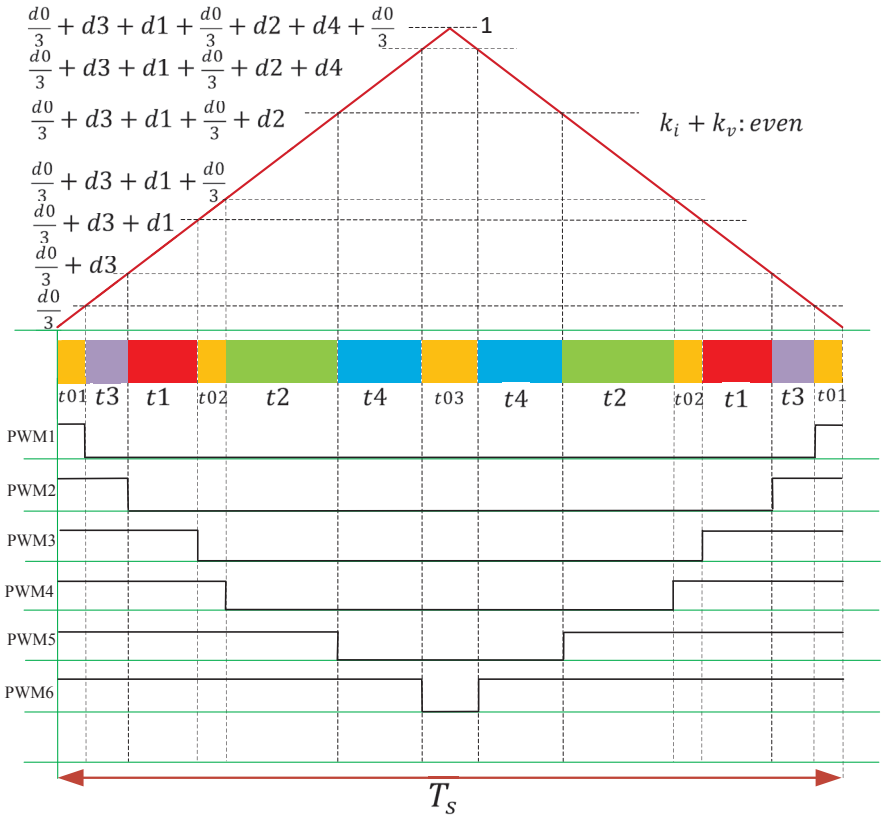


Figure 3.10: Generation of symmetrically distributed switching pulses, where a) When $k_i + k_v$ is odd, and b) When $k_i + k_v$ is even

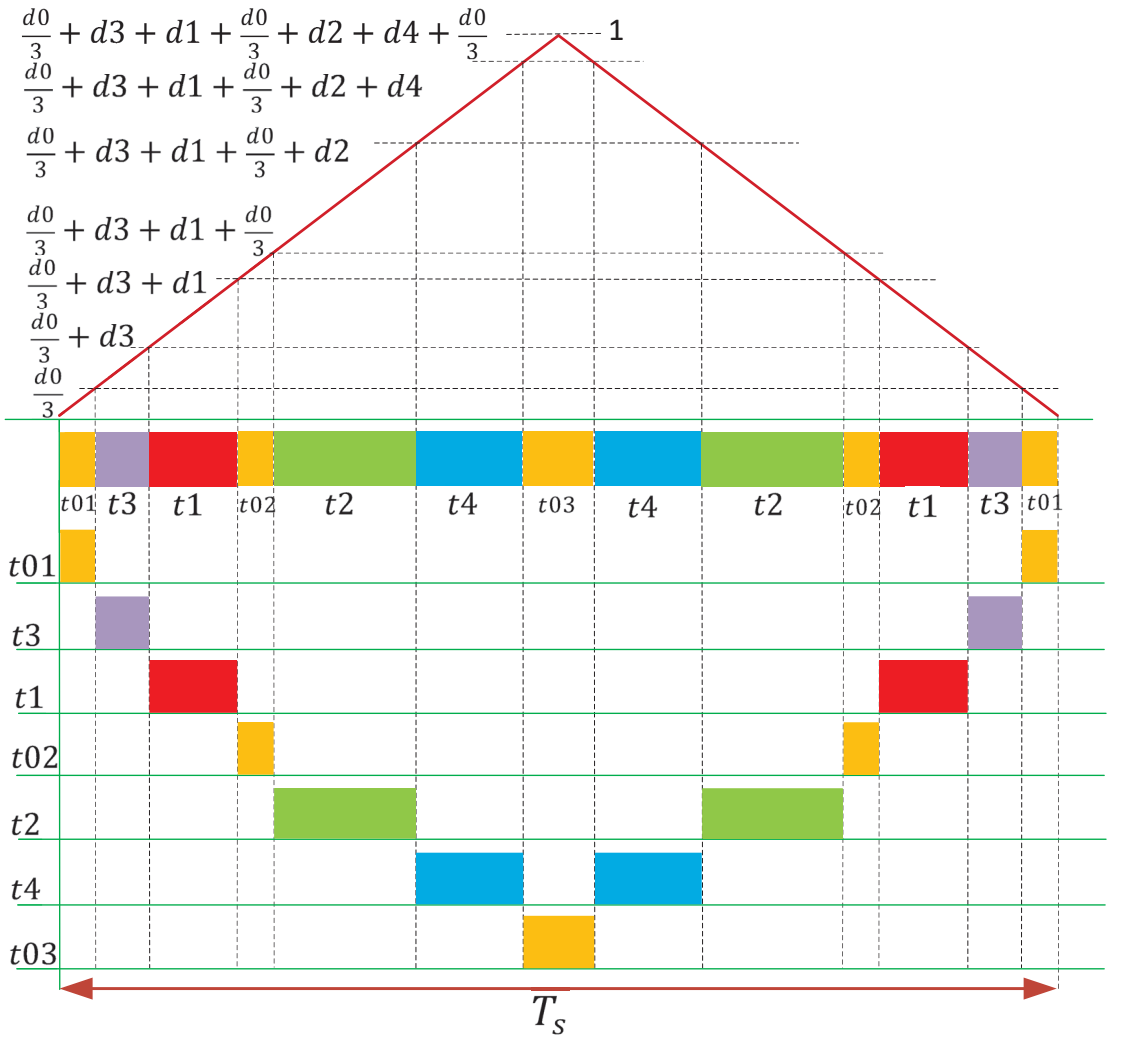


Figure 3.11: Generation of symmetrically distributed switching pulses, time duration of each switching configuration for a switching sequence with period T_s When $k_i + k_v$ is even

Table 3.3: Connected switches and their connecting time durations when $k_i = k_v = 2$

output phases	XYZ	XYZ	XYZ	XYZ	XYZ	XYZ	XYZ
input phases	BBB	BBC	CBC	CCC	CAC	AAC	AAA
ON switches	S12,S22,S32	S12,S22,S33	S13,S22,S33	S13,S23,S33	S13,S21,S33	S11,S21,S33	S11,S21,S31
time durations	$\frac{t_0}{3}$	t_3	t_1	$\frac{t_0}{3}$	t_2	t_4	$\frac{t_0}{3}$

According to the above mentioned details, following stages are required to implement a SVM method for DMC:

- Computing the switching-times using (3.31) to (3.35).

Table 3.4: Matrix converter simulation parameters

Input source	Input filter	Output load	Frequencies
$V_{si} = 400V(ll, rms)$	$C_f = 6.6\mu F$	$R_l = 10\Omega$	$f_i = 50Hz$
$L_s = 0.4mH$	$L_f = 3mH$	$L_l = 6mH$	$f_o = 70Hz$
$R_s = 0.5\Omega$	$R_d = 5\Omega$		$f_s = 10kHz$

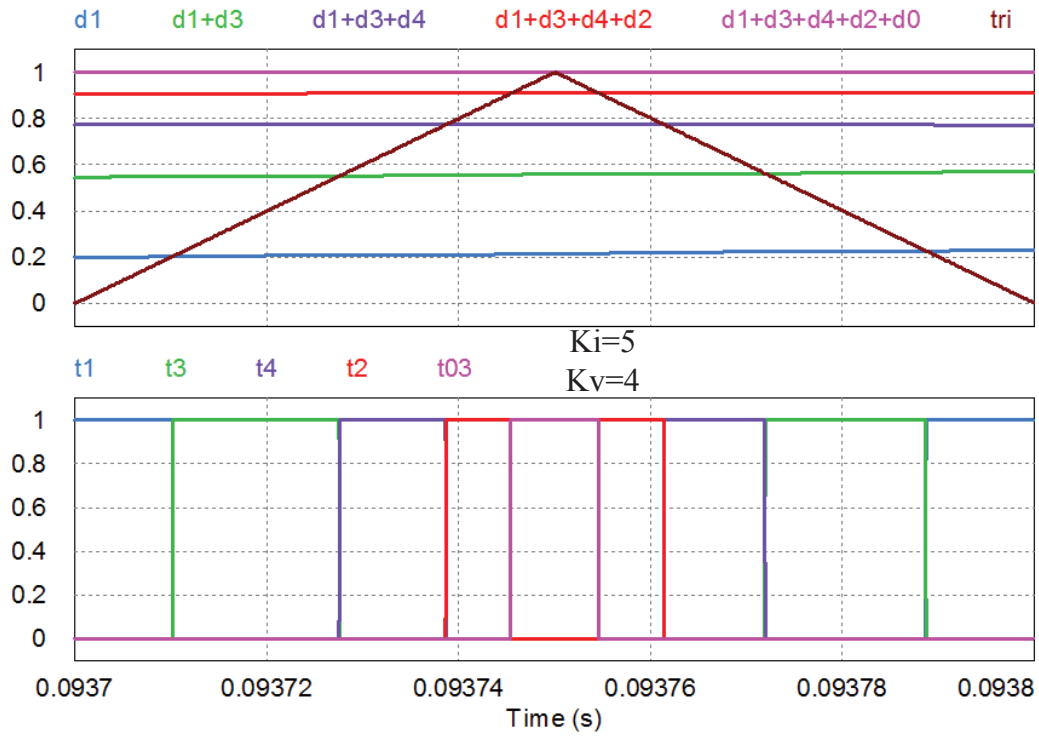
- Converting the switching-times into PWM switching pulses.
- Distributing the switching pulses to the bidirectional switches according to the switching patterns.

3.3.2 Simulation and experimental results of DSVM

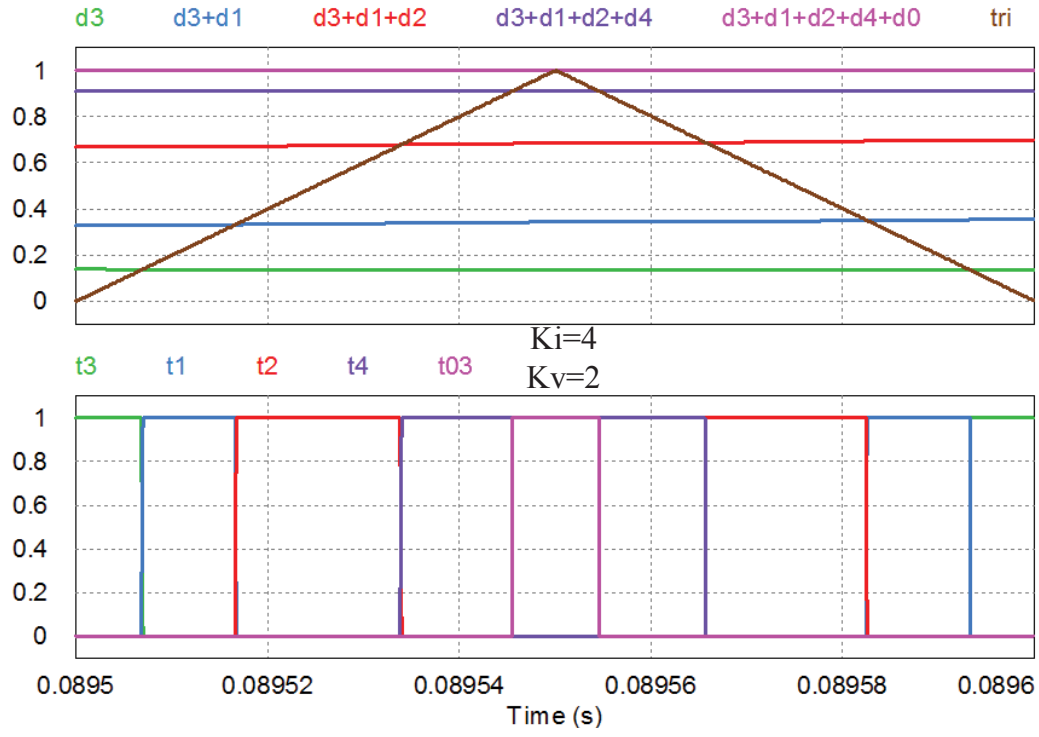
The model of the DMC shown in Figure 2.6 with a three-phase Y-connected R-L load, has been simulated using PSIM, based on the specifications presented in Table 3.4. The parameters of IGBT switches are selected close to the real ones and simulation time step is $2\mu s$. The simulation results using DSVM are presented in the following figures. Figure 3.13 shows the three-phase output current and the frequency spectrum of i_x when the output reference voltage is $v_{o,ref} = 330V(line - line)$. It can be seen that harmonics are introduced at integer multiples of the switching frequency $f_s = 10kHz$ and their sidebands. The output currents are sinusoidal due to the inductive load, and its THD is about 1.14%.

The same results are obtained for input source current as illustrated in Figure 3.14. By using the low-pass RLC filter, the switching frequency harmonics are filtered out, and a set of sinusoidal, balanced input currents is obtained at the supply side. The THD of the input source current is about 2.51% that the low THD of the input source and output currents are due to the high voltage gain $q \cong 0.83$. As the output current, the harmonics of the input source currents are around the integer multiples of the switching frequency and their sidebands.

The relation of the voltage gain, input power factor and THD of the currents have been studied through simulation. Figure 3.17 presents the source and output currents with the input source phase voltage and output reference voltage respec-



(a)



(b)

Figure 3.12: Simulation results of time duration of each switching configuration for a switching sequence with period T_s When $k_i + k_v$ is: a) odd, and b) even

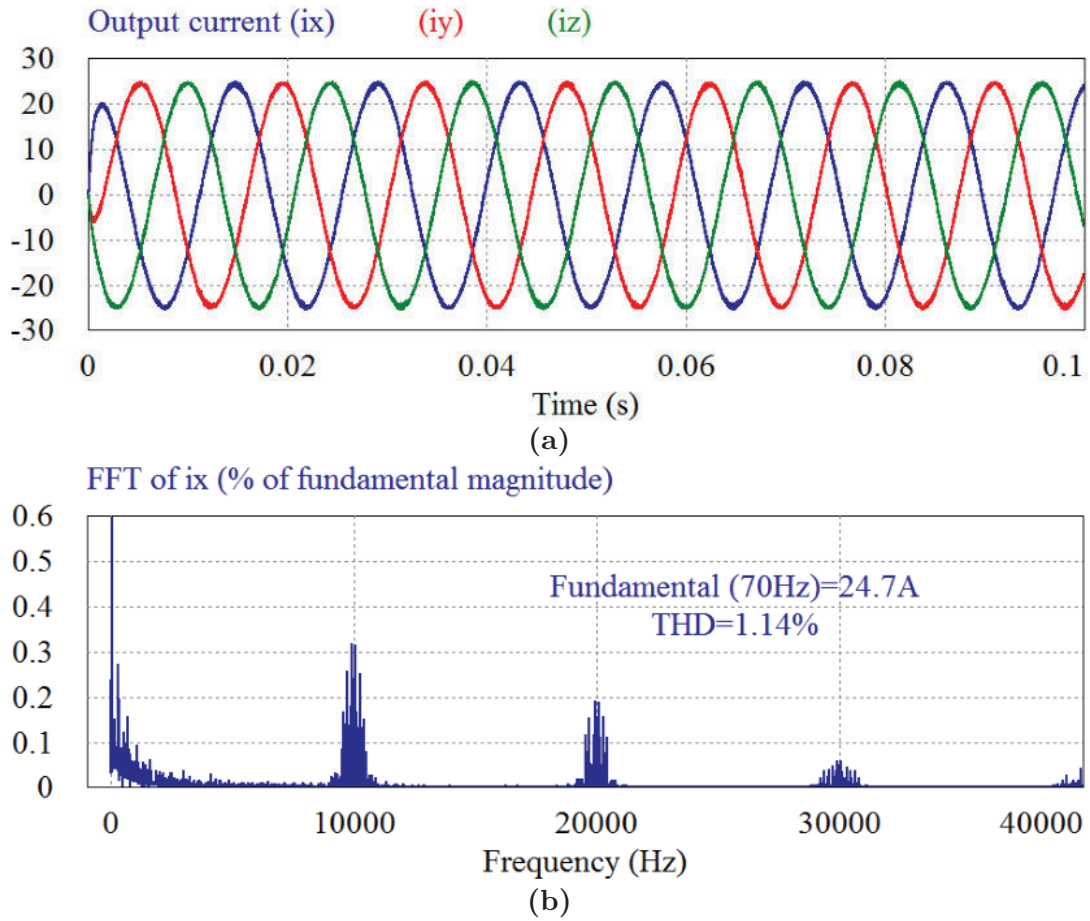


Figure 3.13: Simulation results of DSVM when $v_{o,ref} = 330V(L-to-L)$, where a) Three-phase output currents, and b) Frequency spectrum of i_x

tively for three different $v_{o,ref}$, 330V, 200V, and 80V. As can be seen for voltage gains around 0.83, 0.5 and 0.2, the THD of the input source current and the output current increase to (2.51, 1.14), (4.11, 2.72) and (5.47, 6.21) respectively and input power factor decreases from 0.999 to 0.972 and 0.48. The angle between the output reference voltage and generated current remains constant and does not depend on the voltage gain. The other results of the simulation are presented in Figures 3.15 and 3.16, including output phase voltage v_{xn} and its spectrum, input phase voltage of the converter v_A, output line voltage v_{xy}, output phase voltage with respect to the input neutral point v_{xN}, and common mode voltage v_{nN}. Also, Figure 3.18 shows the results for lower output frequency $f_o = 30Hz$.

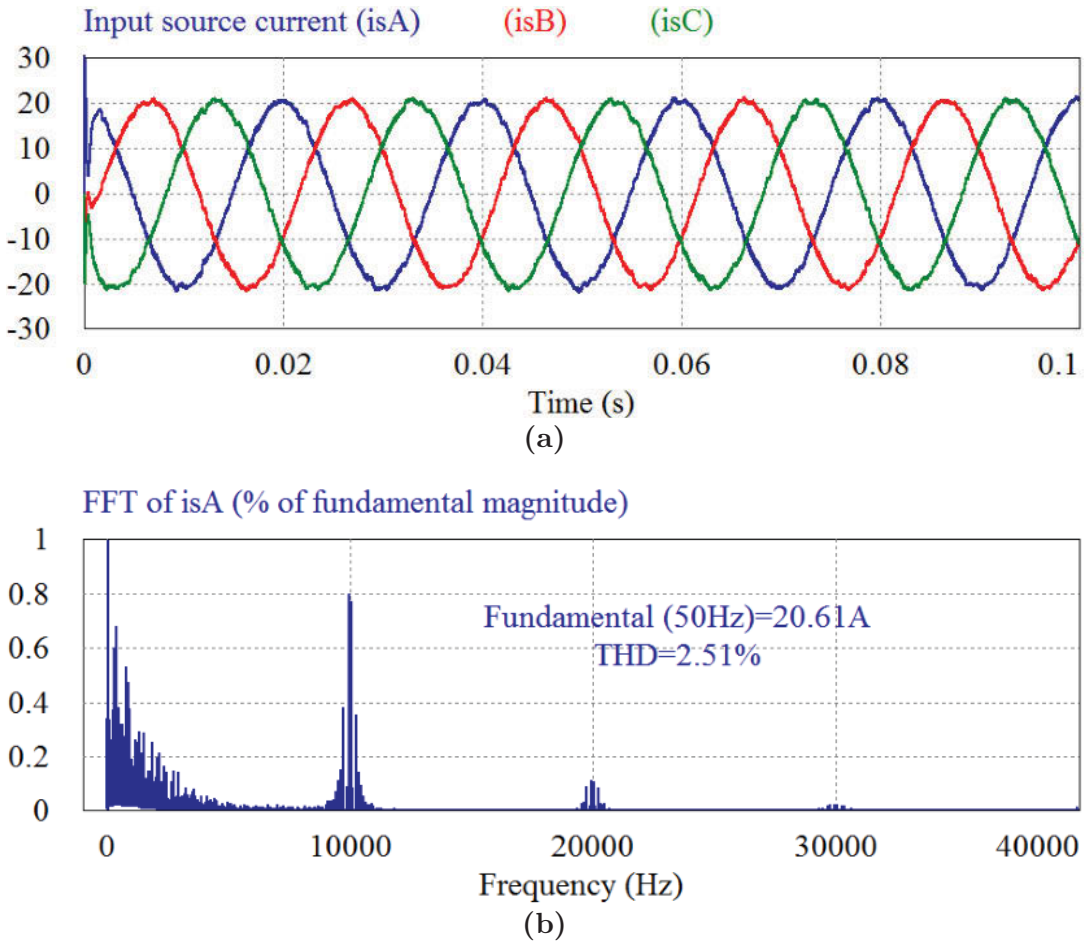
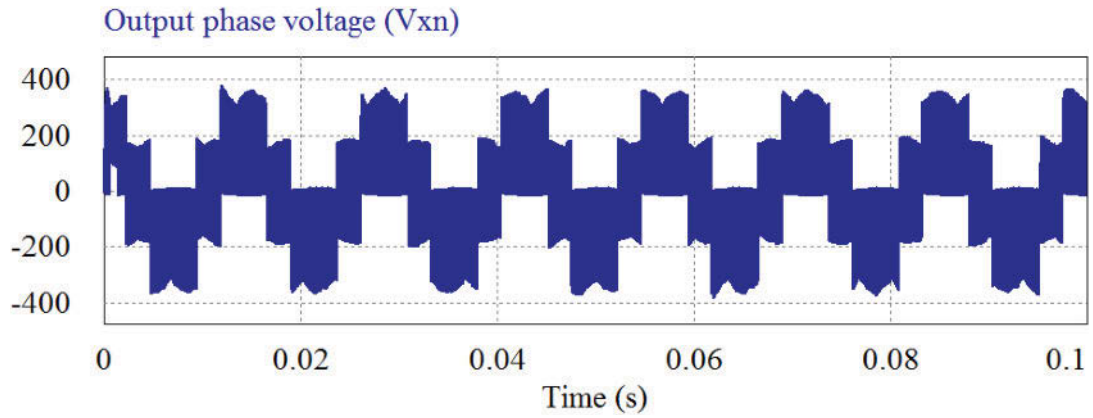
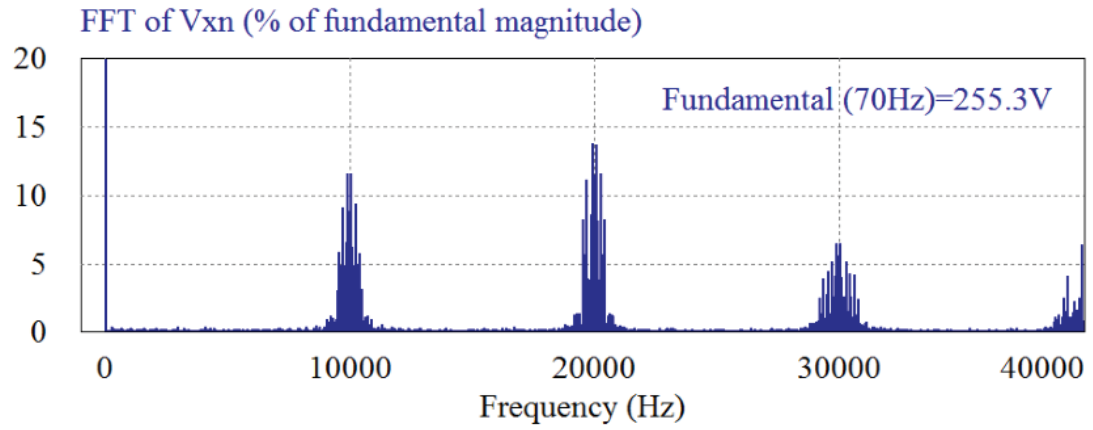


Figure 3.14: Simulation results of DSVM with $v_{o,ref} = 330V(L-L)$, where a) Three-phase input source currents, and b) Frequency spectrum of i_{sA}

The performance of the DSVM strategy in terms of the input and output currents quality have been verified through the experimental tests carried out on the designed prototype direct matrix converter. The prototype DMC characteristics are mentioned in the next chapter, and the passive load parameters are $R_l = 12\Omega$ and $L_l = 6mH$. The switching frequency is $f_s = 10kHz$. A DSOX2004A KEYSIGHT oscilloscope and a TCPA300 current probe from Tektronix have also been used for measurements. Figure 3.19 shows the three-phase input source currents and the frequency spectrum of i_{sB}. AS can be seen, harmonics are introduced at integer multiples of the switching frequency $f_s = 10kHz$ and the sidebands of all these frequencies. Figure 3.20 shows the ability of the converter to generate output wave-



(a)



(b)

Figure 3.15: Simulation results of DSVM with $v_{o,ref} = 330V(L-L)$, where a) Output phase voltage v_{xn}, and b) Frequency spectrum of v_{xn}

forms with frequencies higher (70Hz) or less (50Hz) than the input source frequency (50Hz) and in the other experimental figures $f_o = 60Hz$. Figure 3.21 illustrates the effect of the voltage gain on the quality of the input and output currents and the input power factor. As is presented, for the voltage gain about 0.5, the currents are more distorted, and the percentage of the harmonic components in the currents decreases by increasing the converter gain. On the other hand, it can be seen in Figure 3.22a that the input power factor is almost equal to unity as the input displacement angle measured by the oscilloscope is about 5°. The slight leading displacement of the input current is due to the effect of the input LC filter. Figure 3.23a shows the three-phase output currents which are sinusoidal due to the inductive load. With

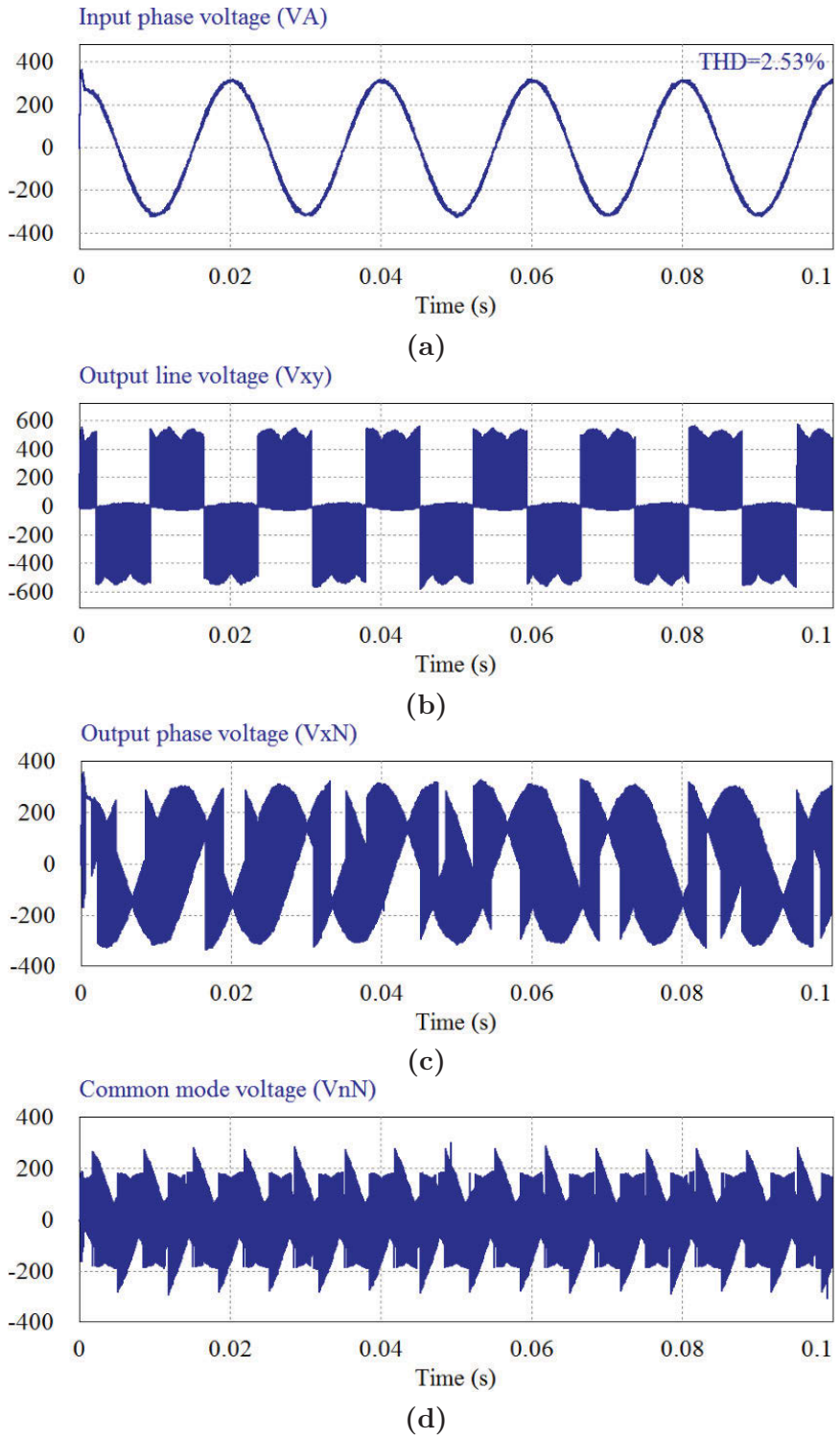


Figure 3.16: Simulation results of DSVM with $v_{o,ref} = 330V(L-L)$, where a) Input phase voltage v_A, b) Output line voltage v_{xy}, c) Output phase voltage with respect to the input neutral point v_{xN}, and d) Common mode voltage

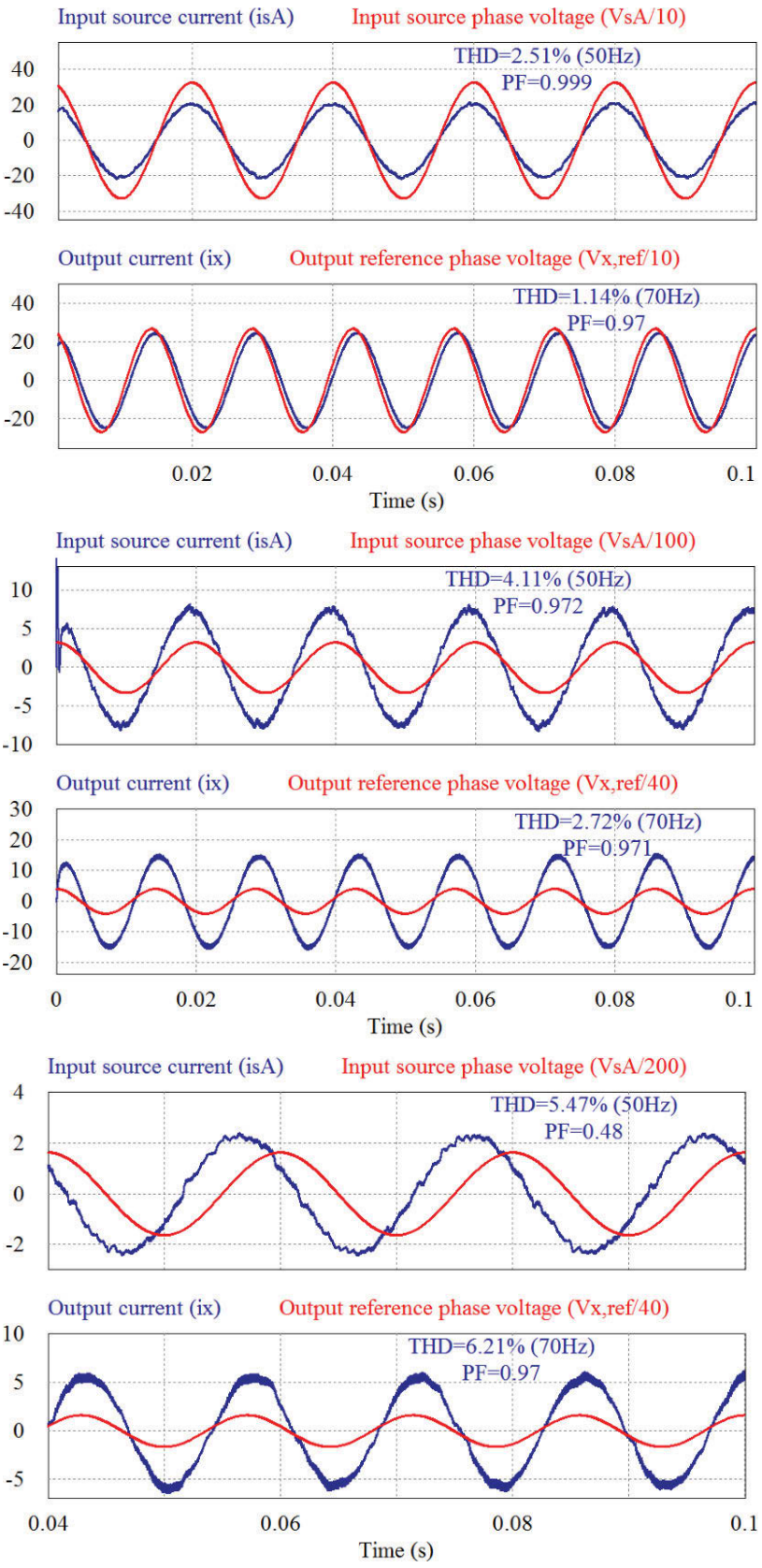


Figure 3.17: Simulation results when output reference voltage (line-line) is: a) $v_{o,ref} = 330V$, b) $v_{o,ref} = 200V$, and c) $v_{o,ref} = 80V$

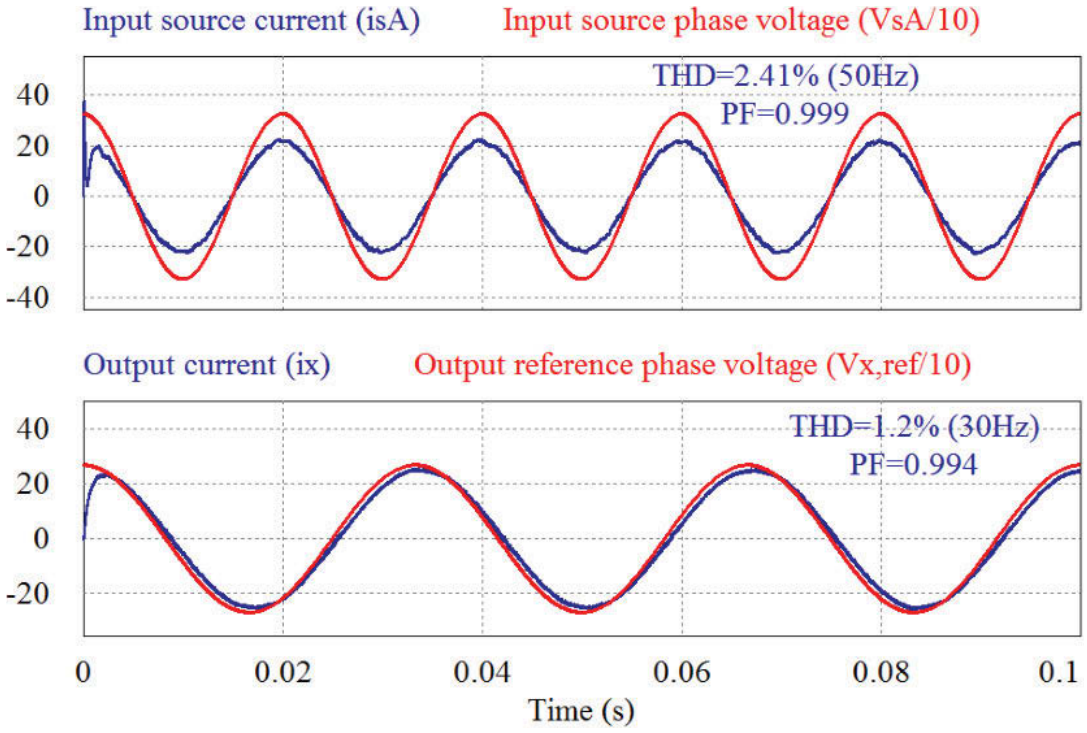
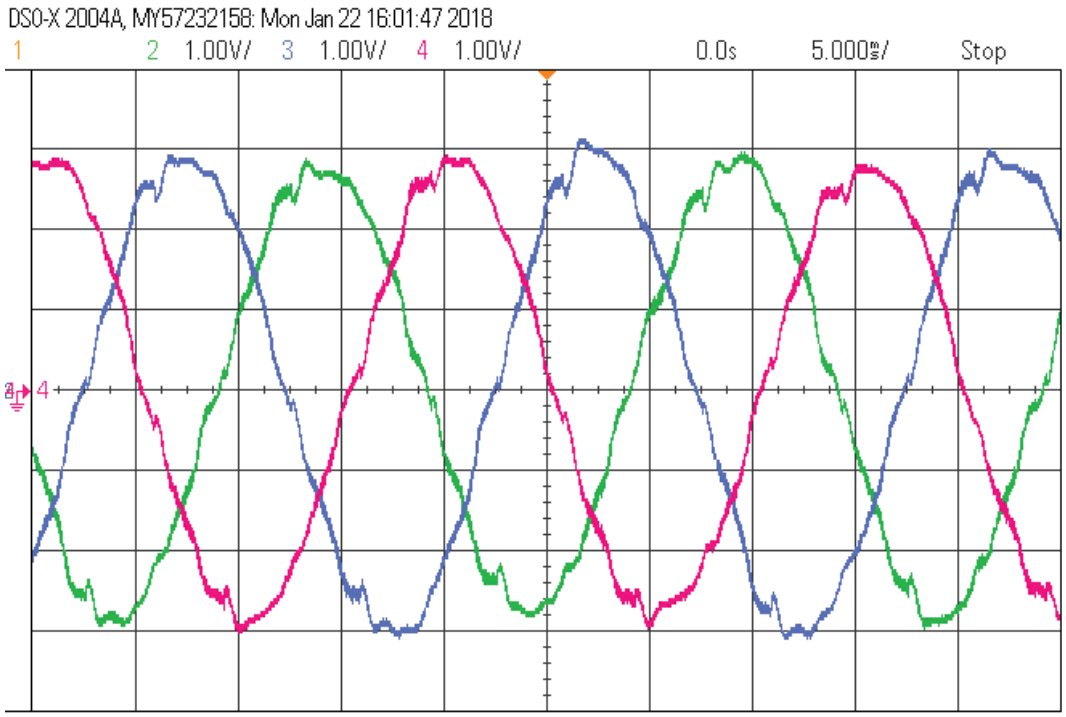


Figure 3.18: Simulation results of DSVM with $v_{o,ref} = 330VL - L$ and $f_o = 30Hz$

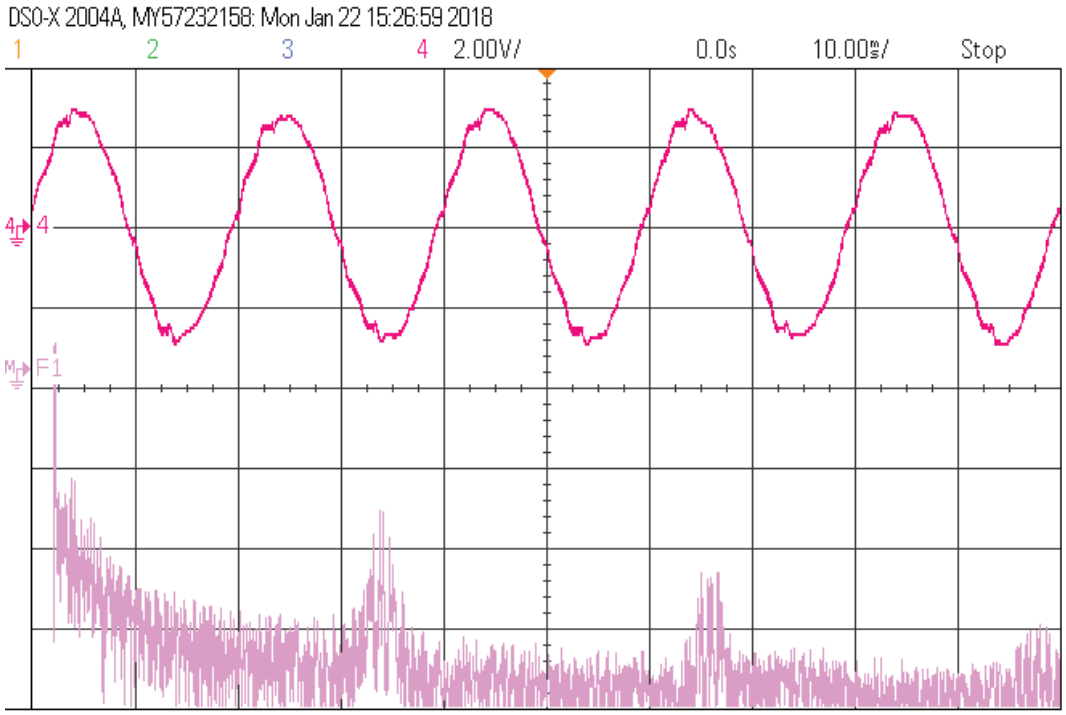
regard to Figure 3.23b, the harmonics of the output current are at integer multiples of the switching frequency. Also, the output phase voltage v_{yN}, line-to-line voltage v_{xy} and their frequency spectrum have been presented in Figure 3.24 that are in good accordance with the simulation ones.

3.3.3 Indirect space vector approach

The indirect conversion method for the MC was firstly introduced by Huber and Borojevic in 1989 [85]. The indirect matrix converter (IMC) divides the modulation process of the matrix converter into the two stages of rectifier with six bidirectional switches and inverter with six unidirectional switches, as shown in Figure 3.25. Based on this technique, the three-phase input voltages are rectified to a virtual dc-link voltage and then, using this imaginary dc voltage, the voltage source inverter stage generates the desired output voltages. As mentioned before one of the most preferred modulations for MCs is the Space Vector Modulation (SVM) because of

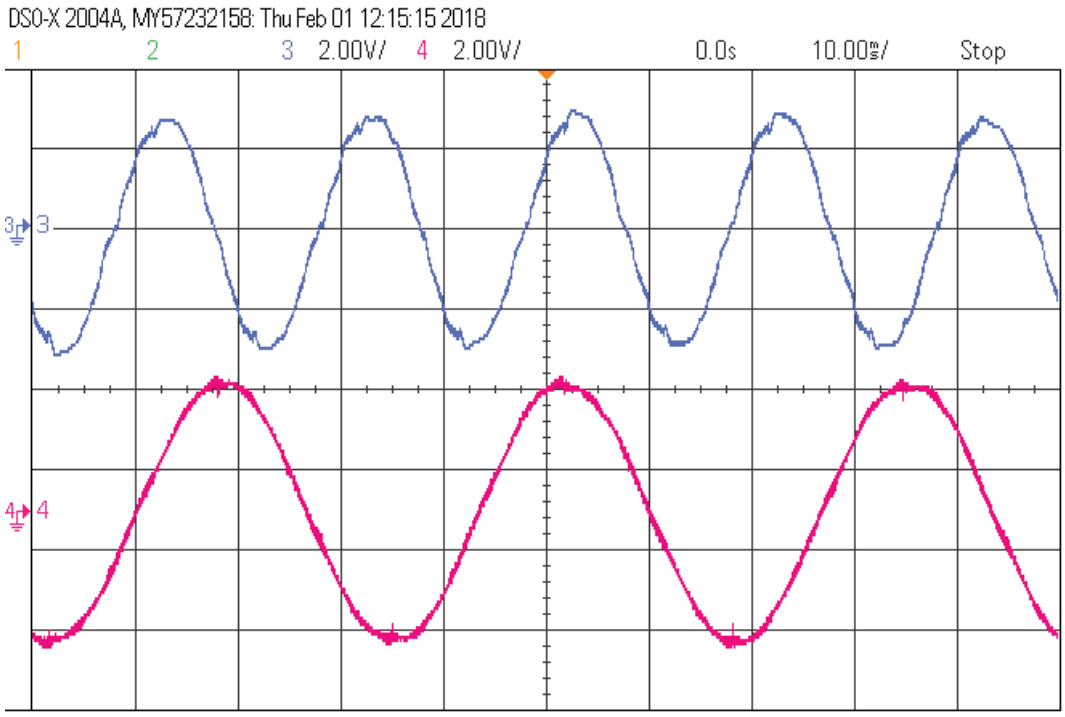


(a)

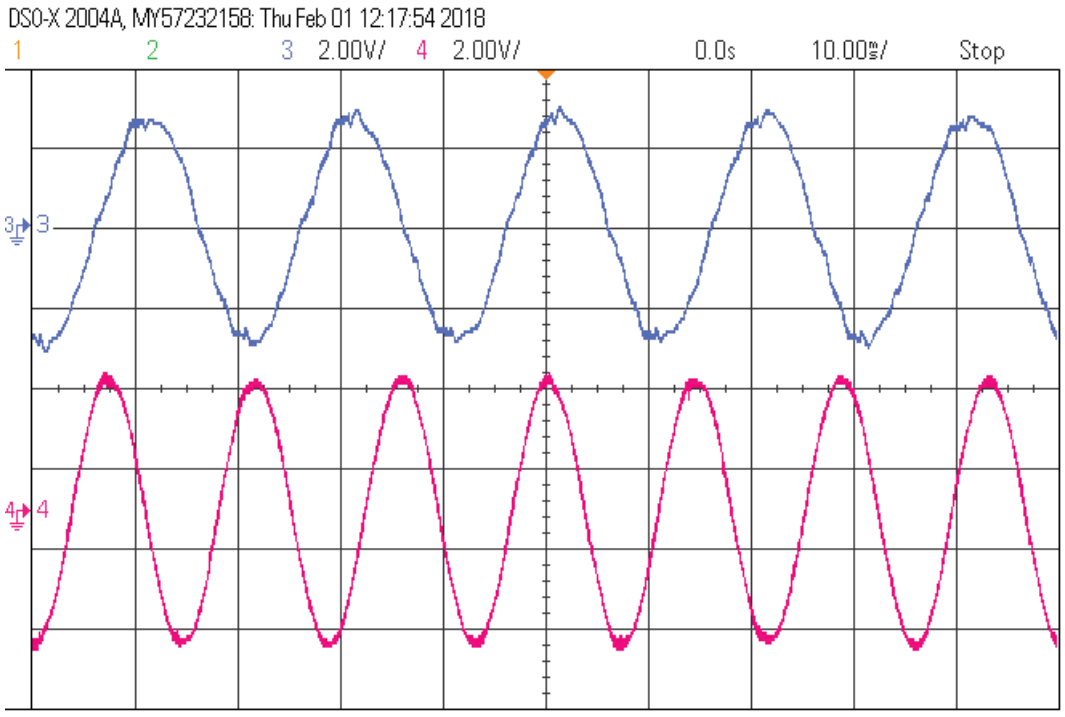


(b)

Figure 3.19: Experimental results of DSVM when $q = 0.86, f_i = 50Hz, f_o = 60Hz$, where a) Three-phase input source currents, and b) Input source current i_{sB} and its frequency spectrum

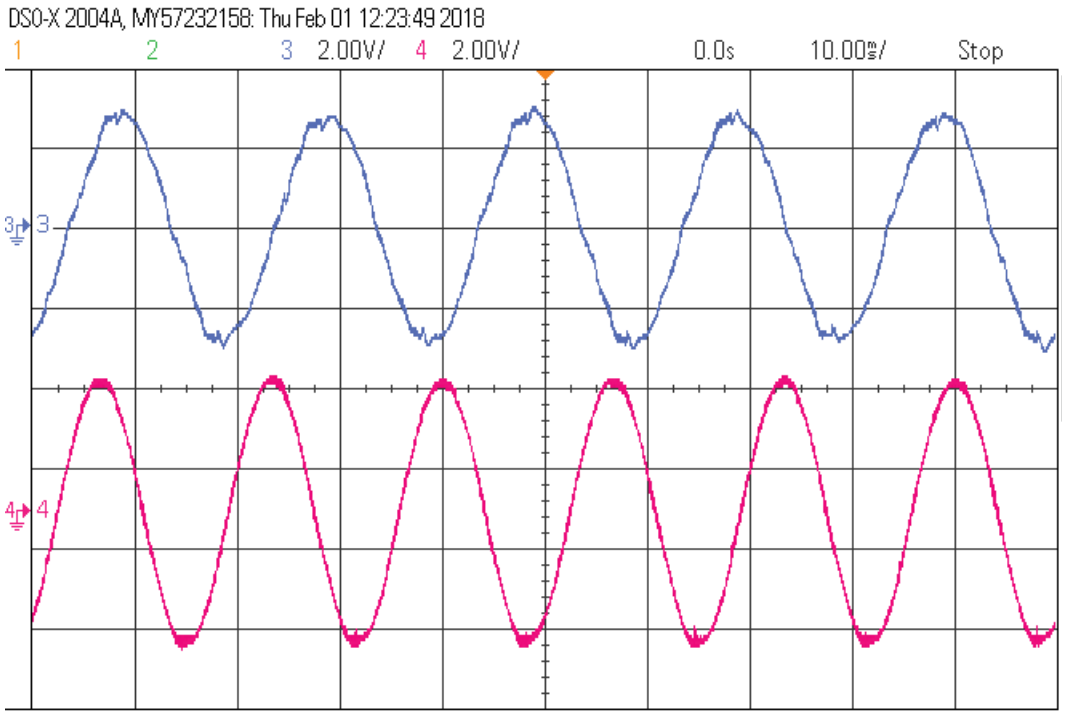


(a)

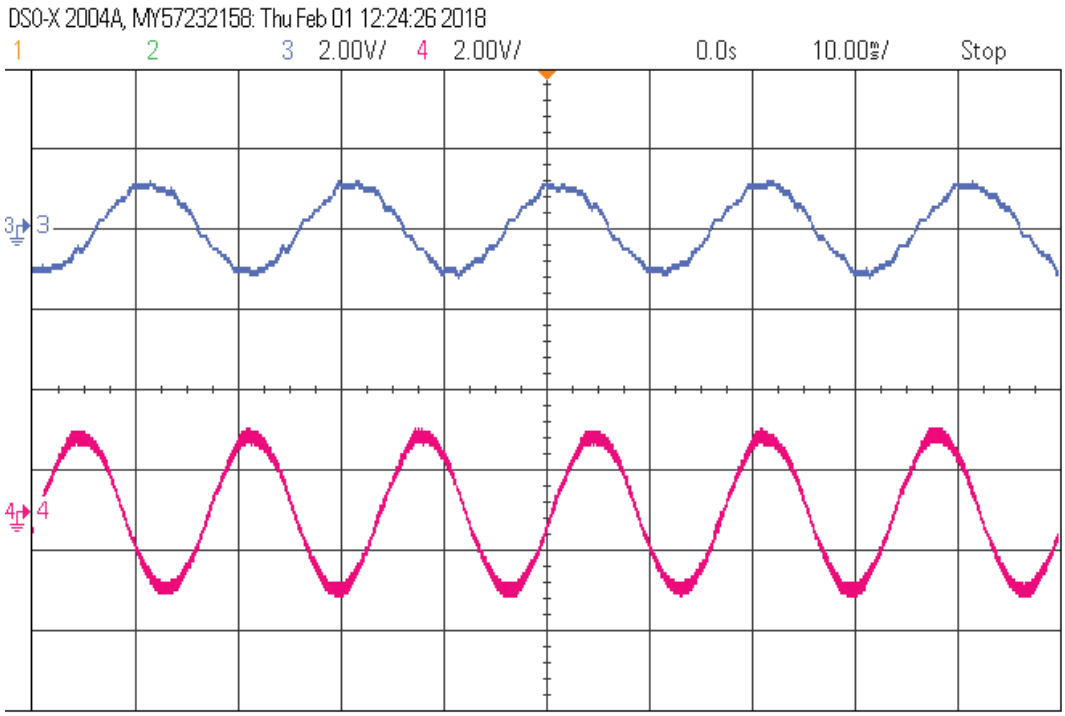


(b)

Figure 3.20: Experimental results of DSVM, input source current i_{sB} and output current i_y when $q = 0.86$ and $f_i = 50Hz$, where a) $f_o = 30Hz$, and b) $f_o = 70Hz$

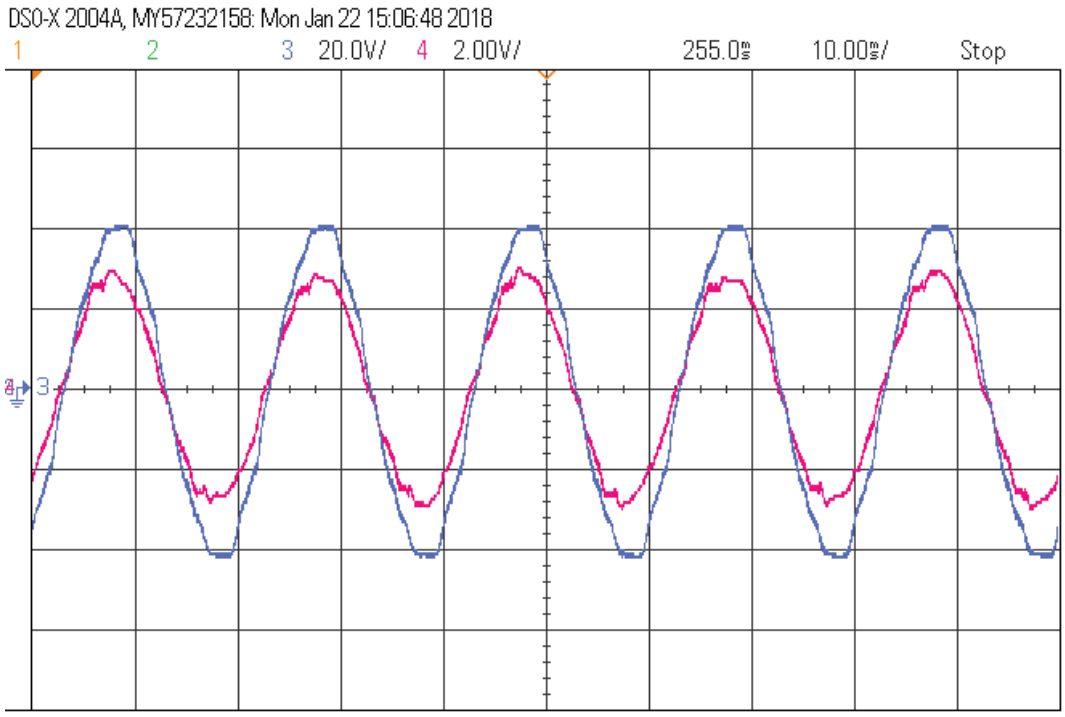


(a)

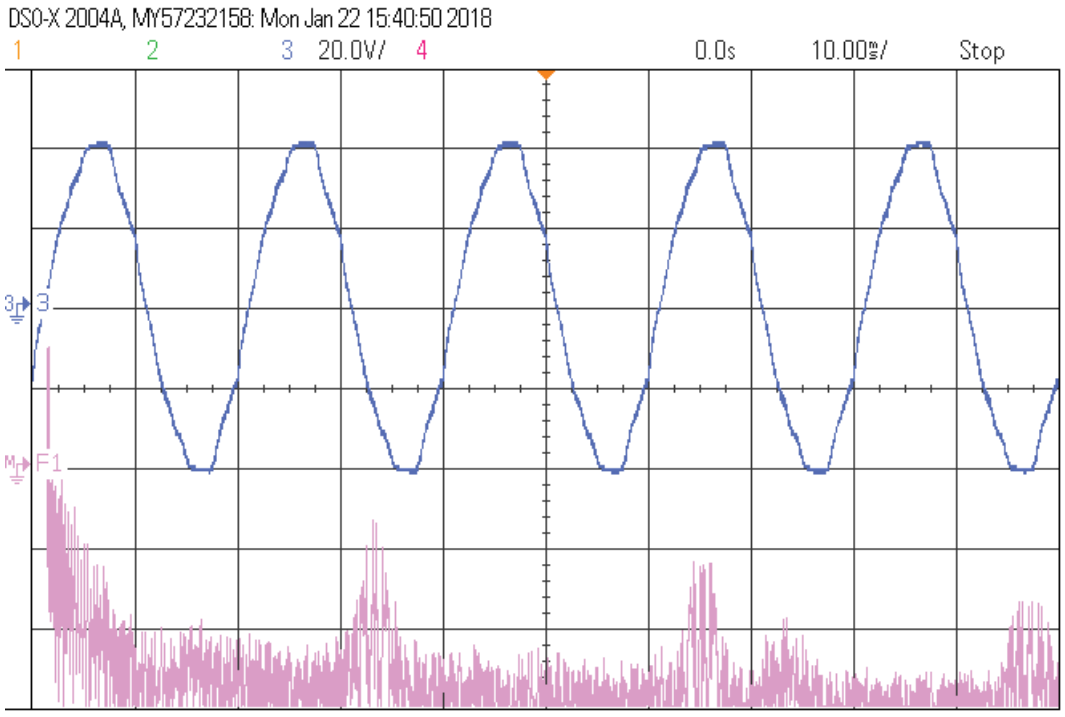


(b)

Figure 3.21: Experimental results of DSVM, input source current i_{sB} and output current i_y when $f_i = 50Hz$ and $f_o = 60Hz$, where a) $q = 0.86$, and b) $q = 0.5$

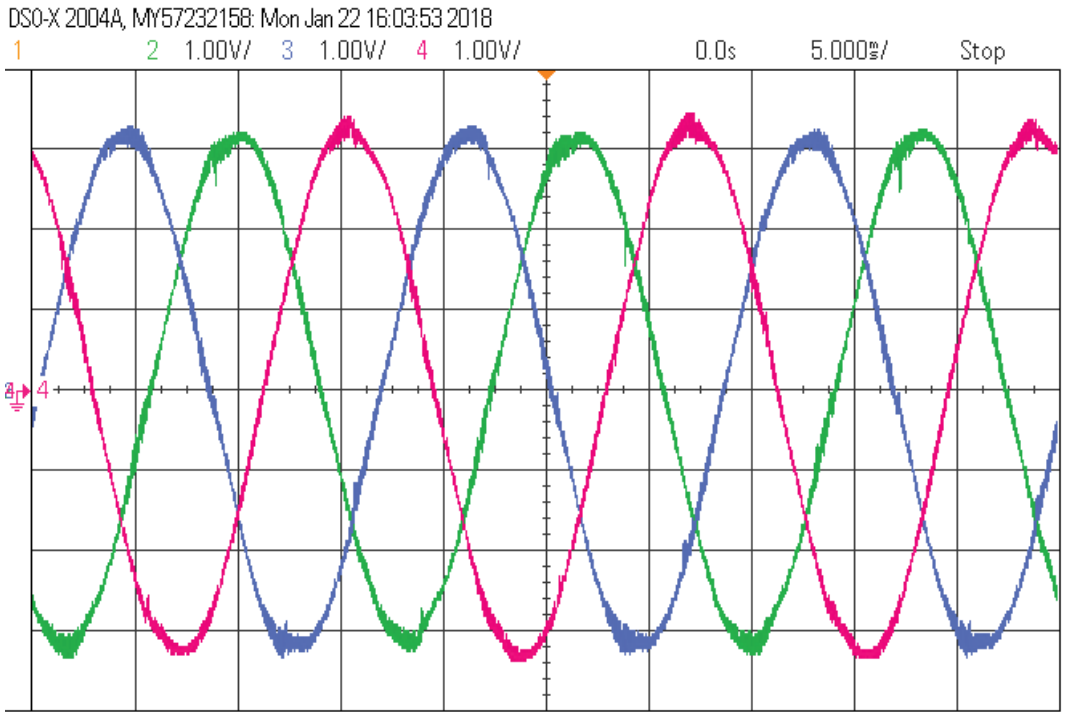


(a)

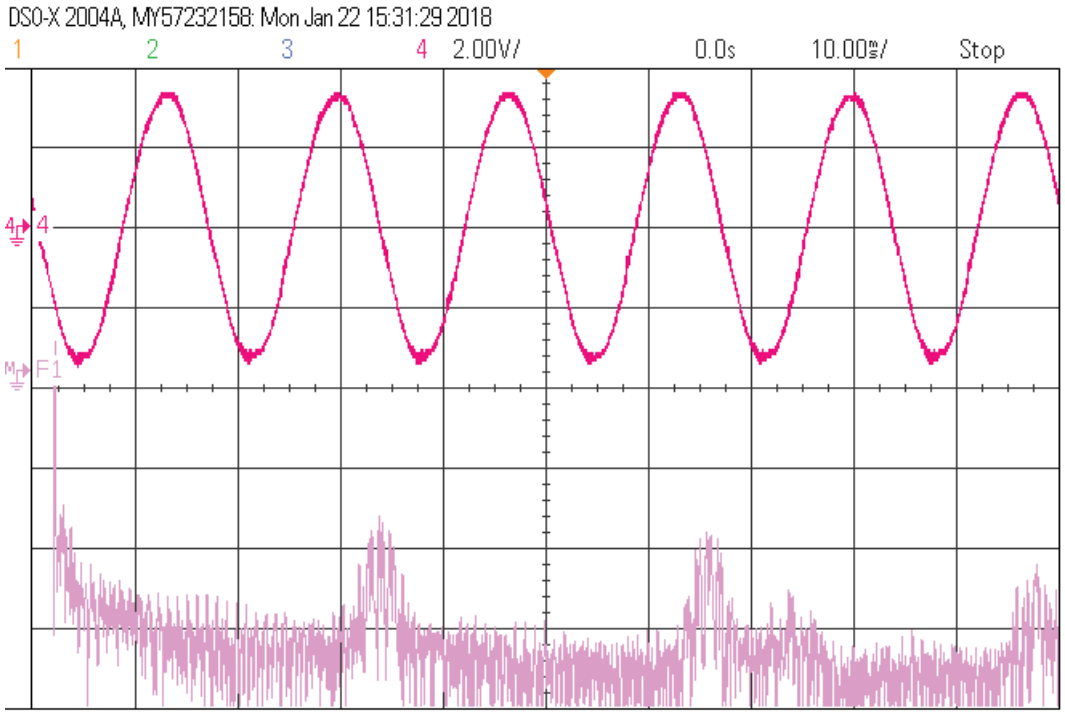


(b)

Figure 3.22: Experimental results of DSVM, when $q = 0.86$, $f_i = 50Hz$ and $f_o = 60Hz$, where a) input source current and voltage i_{sB} and v_{sB}, and b) input source voltage v_{sB} and its frequency spectrum

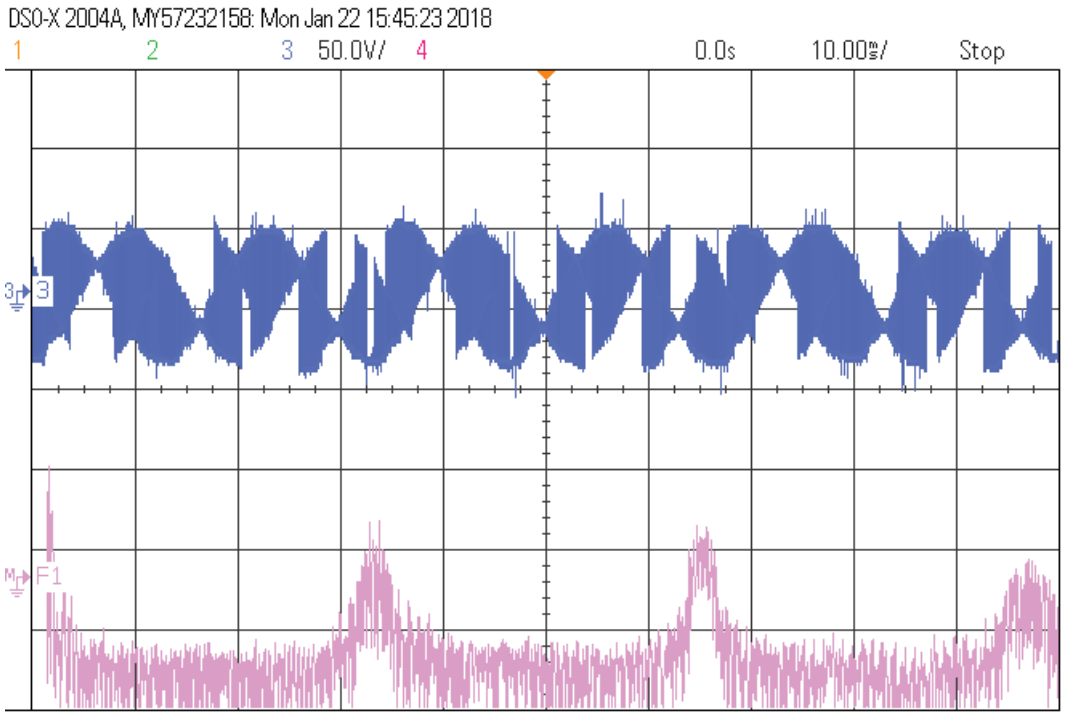


(a)

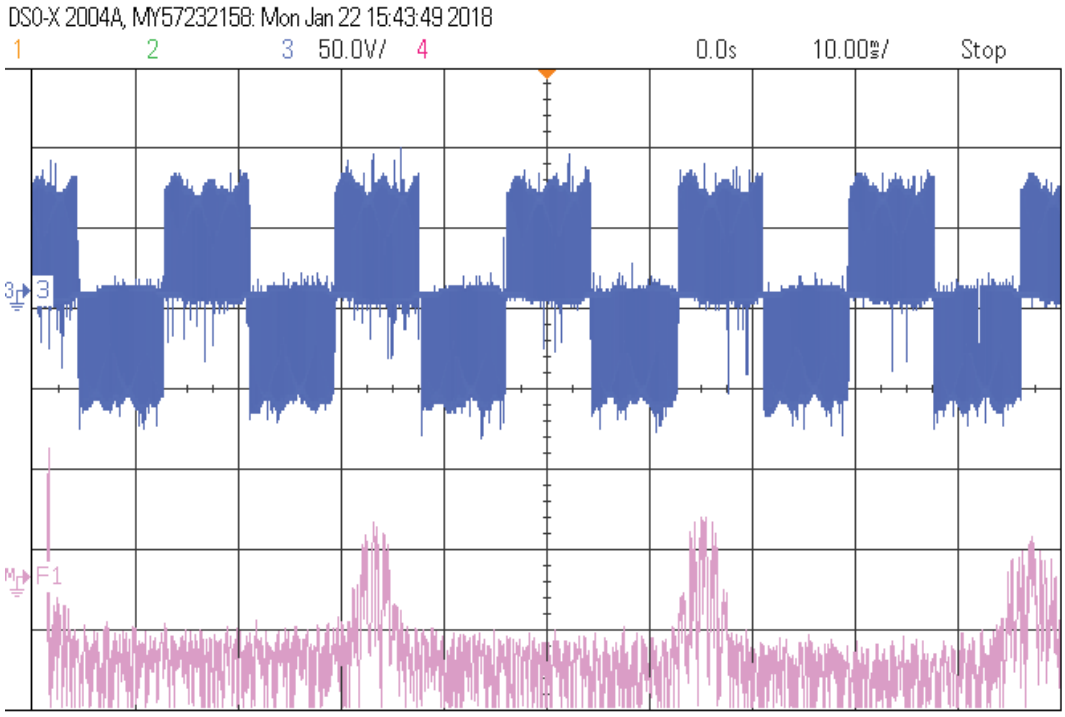


(b)

Figure 3.23: Experimental results of DSVM when $q = 0.86, f_i = 50Hz and f_o = 60Hz$, where a) Three-phase output currents, and b) Output current i_y and its frequency spectrum



(a)



(b)

Figure 3.24: Experimental results of DSVM when $q = 0.86, f_i = 50Hz and f_o = 60Hz$, where a) Output phase voltage v_{yN} and its spectrum, and b) Output line-to-line voltage v_{xy} and its spectrum

the better harmonic performance using different switching strategies. The converter control stage generates and applies indirect SVM (ISVM) control signals to the power switches in order to obtain the desired input current and output voltage waveforms. The number of switching commutations and consequently the switching losses in each switching period depends on the number and position of the zero configurations used in the switching pattern. It also has some effect on the ripples of the input and output voltages and currents. Figure 3.26 shows a schematic diagram of the conventional IMC. A second-order low-pass input filter is located between the input three-phase voltage source and the rectifier stage to eliminate the current harmonics injected into the source. The rectifier and the inverter stages are synthesised independently, and then the results are combined to produce the modulation for the entire matrix converter [91–93]. Compare to the DSVM, ISVM is easier to understand and also it is possible to apply different well-established algorithms of the inverter to IMCs.

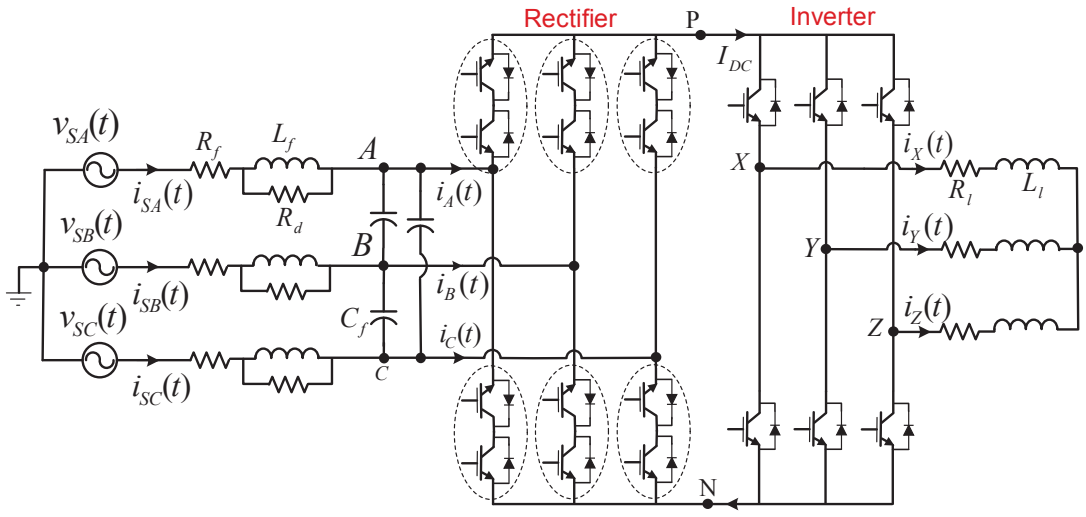


Figure 3.25: IMC with an RLC filter and a three-phase RL load

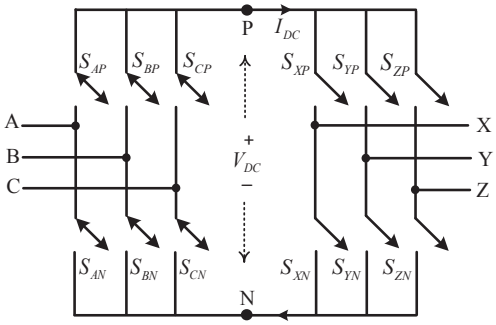


Figure 3.26: The schematic diagram of ideal IMC

By splitting the transfer matrix of the MC into the product of the transfer matrixes of a rectifier and an inverter, the control of the input current and output voltage is decoupled as following:

$$\begin{bmatrix} S_{XA} & S_{YA} & S_{ZA} \\ S_{XB} & S_{YB} & S_{ZB} \\ S_{XC} & S_{YC} & S_{ZC} \end{bmatrix} = \begin{bmatrix} S_{XP} & S_{XN} \\ S_{YP} & S_{YN} \\ S_{ZP} & S_{ZN} \end{bmatrix} \begin{bmatrix} S_{AP} & S_{BP} & S_{CP} \\ S_{AN} & S_{BN} & S_{CN} \end{bmatrix} = \\ \begin{bmatrix} S_{XP}.S_{AP} + S_{XN}.S_{AN} & S_{XP}.S_{BP} + S_{XN}.S_{BN} & S_{XP}.S_{CP} + S_{XN}.S_{CN} \\ S_{YP}.S_{AP} + S_{YN}.S_{AN} & S_{YP}.S_{BP} + S_{YN}.S_{BN} & S_{YP}.S_{CP} + S_{YN}.S_{CN} \\ S_{ZP}.S_{AP} + S_{ZN}.S_{AN} & S_{ZP}.S_{BP} + S_{ZN}.S_{BN} & S_{ZP}.S_{CP} + S_{ZN}.S_{CN} \end{bmatrix} \tag{3.38}$$

The instantaneous output phase voltages can be determined as below:

$$\begin{bmatrix} v_X(t) \\ v_Y(t) \\ v_Z(t) \end{bmatrix} = \begin{bmatrix} S_{XP} & S_{XN} \\ S_{YP} & S_{YN} \\ S_{ZP} & S_{ZN} \end{bmatrix} \begin{bmatrix} S_{AP} & S_{BP} & S_{CP} \\ S_{AN} & S_{BN} & S_{CN} \end{bmatrix} \begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix} \tag{3.39}$$

3.3.4 The rectifier stage

The rectifier stage is controlled to provide sinusoidal input currents with unity input power factor [90]. By assuming the rectifier stage as a stand-alone current source rectifier (CSR), the dc-link voltage V_{DC} can be derived by using the rectifier transfer matrix multiplied by the input voltages. Also, the input currents can be represented

Table 3.5: Valid switching combinations for the rectifier stage and its respective generated input current vectors

input current space vectors	$\lvert\overrightarrow{I}_i\rvert$	$\angle\overrightarrow{I}_i(\beta_i)$	connected switches
$\overrightarrow{I}_{i1}$	$\frac{2}{\sqrt{3}}I_{DC}$	$-\frac{\pi}{6}$	S_{AP}, S_{BN}
$\overrightarrow{I}_{i2}$	$\frac{2}{\sqrt{3}}I_{DC}$	$\frac{\pi}{6}$	S_{AP}, S_{CN}
$\overrightarrow{I}_{i3}$	$\frac{2}{\sqrt{3}}I_{DC}$	$\frac{\pi}{2}$	S_{BP}, S_{CN}
$\overrightarrow{I}_{i4}$	$\frac{2}{\sqrt{3}}I_{DC}$	$\frac{5\pi}{6}$	S_{AN}, S_{BP}
$\overrightarrow{I}_{i5}$	$\frac{2}{\sqrt{3}}I_{DC}$	$-\frac{5\pi}{6}$	S_{AN}, S_{CP}
$\overrightarrow{I}_{i6}$	$\frac{2}{\sqrt{3}}I_{DC}$	$-\frac{\pi}{2}$	S_{BN}, S_{CP}

by using the transposed transfer matrix of the rectifier and I_{DC} such as:

$$\begin{bmatrix} v_P \\ v_N \end{bmatrix} = \begin{bmatrix} S_{AP} & S_{BP} & S_{CP} \\ S_{AN} & S_{BN} & S_{CN} \end{bmatrix} \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} \tag{3.40}$$

$$\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \begin{bmatrix} S_{AP} & S_{AN} \\ S_{BP} & S_{BN} \\ S_{CP} & S_{CN} \end{bmatrix} \begin{bmatrix} I_{DC+} \\ I_{DC-} \end{bmatrix} \tag{3.41}$$

where I_{DC} is the dc-link current shown in Figures 3.25 and 3.26.

In purpose of avoiding short circuit at the input source, only nine switching combinations are permitted in the rectifier stage and presented as non-zero vectors shown in Table 3.5.

For example, in Figure 3.29 the closed switches in the rectifier stage are S_{AP} and S_{CN}. The virtual dc-link P-N is connected to the input phase voltages v_A and v_C at this instant and therefore the input current vector $\vec{I_{i2}}$ is obtained by using the

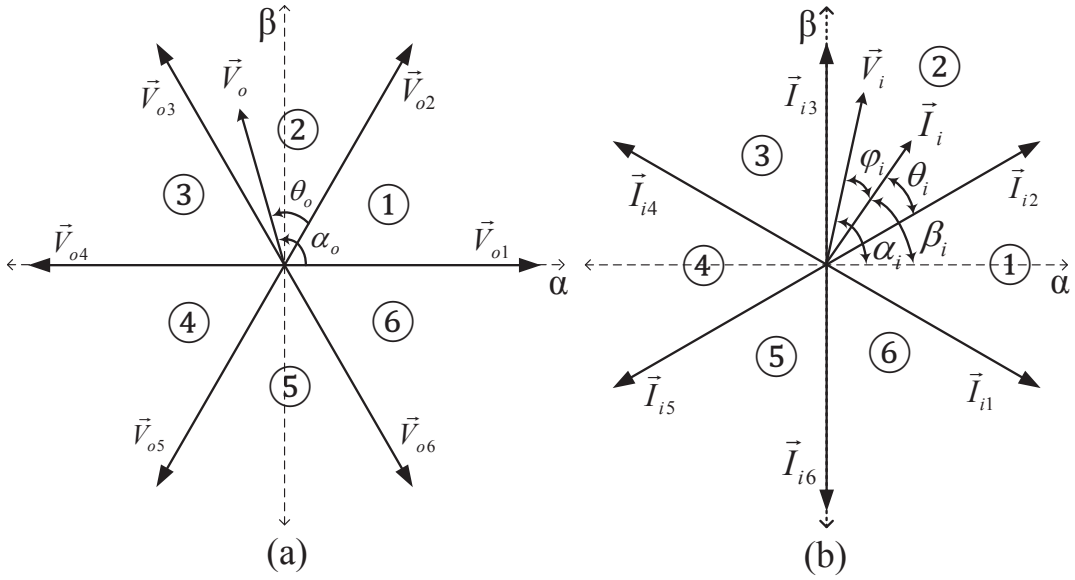


Figure 3.27: IMC space vectors of a) The output voltage b) The input current

space vector transformation:

$$\begin{aligned}\vec{I_{i2}} &= \frac{2}{3}[i_A(t) + i_B(t)e^{\frac{j2\pi}{3}} + i_C(t)e^{\frac{j4\pi}{3}}] \\ &= \frac{2}{3}(I_{DC} + 0.e^{\frac{j2\pi}{3}} - I_{DC}.e^{\frac{j4\pi}{3}}) \\ &= \frac{2}{\sqrt{3}}e^{j\frac{\pi}{6}}\end{aligned} \tag{3.42}$$

According to the six vectors mentioned in Table 3.5 with fixed directions, Figure 3.27 illustrates the input current vectors formed by the valid switching combinations of the rectifier stage. Any arbitrary input current vector within a sector of the current hexagon can be synthesised by two adjacent input current switching vectors ($\overrightarrow{I}_{i2}$, $\overrightarrow{I}_{i3}$) as shown in Figure 3.28b. The proportion between two adjacent vectors determines the direction of the current reference vector. Therefore the reference input current vector, for a switching period T_s is synthesised as:

$$\begin{aligned}\vec{I_i} &= d_\gamma \vec{I_\gamma} + d_\delta \vec{I_\delta} \\ &= d_\gamma \vec{I}_{i2} + d_\delta \vec{I}_{i3}\end{aligned} \tag{3.43}$$

where d_γ and d_δ are resectively the duty cycles of the adjacent vectors $\vec{I_\gamma}$ and $\vec{I_\delta}$

within the switching interval T_s. Considering the triangle $\triangle ABC$ in Figure 3.28b, the duty cycles d_γ and d_δ are calculated as following:

$$\begin{aligned} \frac{\sin(\angle BAC)}{|d_\delta \vec{I}_{i3}|} &= \frac{\sin(\angle ACB)}{|d_\gamma \vec{I}_{i2}|} = \frac{\sin(\angle ABC)}{|\vec{I}_i|} \\ \frac{\sin(\theta_i)}{d_\delta(\frac{2}{\sqrt{3}} I_{DC})} &= \frac{\sin(\frac{\pi}{3} - \theta_i)}{d_\gamma(\frac{2}{\sqrt{3}} I_{DC})} = \frac{\sin(\frac{2\pi}{3})}{|I_i|} \end{aligned} \tag{3.44}$$

$$d_\gamma = \frac{t_\gamma}{T_s} = m_c \sin(\frac{\pi}{3} - \theta_i) \tag{3.45}$$

$$d_\delta = \frac{t_\delta}{T_s} = m_c \sin(\theta_i) \tag{3.46}$$

$$d_{0I} = 1 - (d_\gamma + d_\delta) \tag{3.47}$$

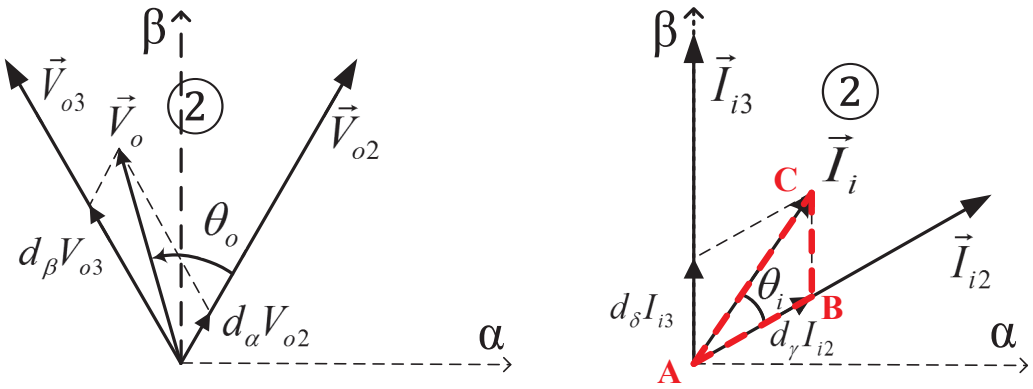
$$m_c = \frac{|\vec{I}_i|}{I_{DC}} \tag{3.48}$$

where t_γ and t_δ are the time durations of the adjacent switching vectors. m_c is the modulation index of the rectifier ($0 \leq m_c \leq 1$), and θ_i indicates the angle of the input current vector within the sector. As the input voltages are considered as the input reference instead of the input currents, the input displacement angle φ_i as shown in Figure 3.27 can be defined as:

$$\begin{aligned} \varphi_i &= \alpha_i - \beta_i \\ \beta_i &= \alpha_i - \varphi_i \end{aligned} \tag{3.49}$$

As an example, in figure 3.27 which input reference current is located in sector 2, the adjacent vectors are $\vec{I}_{i2} and \vec{I}_{i3}$ and connected switches are (S_{AP}, S_{CN}) and (S_{BP}, S_{CN}), so that the instantaneous input currents and the dc-link voltage are as following:

$$\begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = d_\gamma \vec{I}_{i2} + d_\delta \vec{I}_{i3} = (d_\gamma \begin{bmatrix} 1 & 0 \\ 0 & 0 \\ 0 & 1 \end{bmatrix} + d_\delta \begin{bmatrix} 0 & 0 \\ 1 & 0 \\ 0 & 1 \end{bmatrix}) \begin{bmatrix} I_{DC+} \\ I_{DC-} \end{bmatrix} \tag{3.50}$$



(a) **(b)**

Figure 3.28: Synthesising the output reference voltage and input current vectors by two adjacent space vectors in a given sector

$$\begin{bmatrix} v_P \\ v_N \end{bmatrix} = (d_\gamma \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix} + d_\delta \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}) \begin{bmatrix} v_A \\ v_B \\ v_C \end{bmatrix} \tag{3.51}$$

As MCs do not have any energy storage element, the input power and the dc power are equal at any instant. In normal condition, the input voltages are balanced sinusoidal voltages. Therefore,

$$\begin{aligned} P_{in} &= P_{DC} \\ \frac{3}{2} V_{im} I_{im} \cos(\varphi_i) &= V_{DC} I_{DC} \end{aligned} \tag{3.52}$$

As a result, the average dc-voltage generated by the rectifier stage is calculated by:

$$V_{DC} = \frac{3}{2} m_c V_{im} \cos(\varphi_i) \tag{3.53}$$

The maximum dc-voltage level is $\frac{3}{2}V_{im}$, as m_c and power factor $\cos(\varphi_i)$ are assumed unity to have the maximum gain for the converter.

Table 3.6: Valid switching combinations for the inverter stage and its respective generated output voltage vectors

output voltage space vectors	$\lvert\overrightarrow{V}_o\rvert$	$\angle\overrightarrow{V}_o(\alpha_o)$	connected switches
$\overrightarrow{V}_{o1}$	$\frac{2}{3}V_{DC}$	0	S_{XP}, S_{YN}, S_{ZN}
$\overrightarrow{V}_{o2}$	$\frac{2}{3}V_{DC}$	$\frac{\pi}{3}$	S_{XP}, S_{YP}, S_{ZN}
$\overrightarrow{V}_{o3}$	$\frac{2}{3}V_{DC}$	$\frac{2\pi}{3}$	S_{XN}, S_{YP}, S_{ZN}
$\overrightarrow{V}_{o4}$	$\frac{2}{3}V_{DC}$	π	S_{XN}, S_{YP}, S_{ZP}
$\overrightarrow{V}_{o5}$	$\frac{2}{3}V_{DC}$	$-\frac{2\pi}{3}$	S_{XN}, S_{YN}, S_{ZP}
$\overrightarrow{V}_{o6}$	$\frac{2}{3}V_{DC}$	$-\frac{\pi}{3}$	S_{XP}, S_{YN}, S_{ZP}
$\overrightarrow{V}_0$	0	-	S_{XP}, S_{YP}, S_{ZP} *or* S_{XN}, S_{YN}, S_{ZN}

3.3.5 The inverter stage

In order to find the relationship between the output voltages and the dc-link, the inverter stage is considered as a conventional two-level voltage inverter. So the conventional SVM for VSI can be applied to the inverter stage. The inverter stage should generate sinusoidal output voltages with controllable amplitude and frequency. To avoid the open circuit at the load side, and short circuit in dc-link, only eight switching combinations are permitted in the rectifier stage as listed in Table 3.6. Therefore, in each leg of the inverter, one and only one switch must be connected, or:

$$S_{jP} + S_{jN} = 1 \qquad j \in X, Y, Z \tag{3.54}$$

Figure 3.27 illustrates the six non-zero output voltage vectors formed by the valid switching combinations of the voltage source inverter.

The output phase voltages of the inverter can be determined using the transfer

matrix of the inverter stage as following:

$$\begin{bmatrix} v_X \\ v_Y \\ v_Z \end{bmatrix} = \begin{bmatrix} S_{XP} & S_{XN} \\ S_{YP} & S_{YN} \\ S_{ZP} & S_{ZN} \end{bmatrix} \begin{bmatrix} v_P \\ v_N \end{bmatrix} \tag{3.55}$$

Similarly, the dc-link current I_{DC} is derived by the transpose of the inverter transfer matrix:

$$\begin{bmatrix} I_{DC+} \\ I_{DC-} \end{bmatrix} = \begin{bmatrix} S_{XP} & S_{YP} & S_{ZP} \\ S_{XN} & S_{YN} & S_{ZN} \end{bmatrix} \begin{bmatrix} i_X \\ i_Y \\ i_Z \end{bmatrix} \tag{3.56}$$

As can be seen in Figure 3.28a the output reference voltage vector $\vec{V_o}$ can be synthesised by two adjacent space vectors in a given sector as:

$$\vec{V_o} = d_\alpha \vec{V_\alpha} + d_\beta \vec{V_\beta} \tag{3.57}$$

where d_α and d_β are the duty cycles of the vectors $\vec{V_\alpha}$ and $\vec{V_\beta}$ respectively, which can be calculated in the same method of the rectifier:

$$d_\alpha = \frac{t_\alpha}{T_s} = m_v \sin(\frac{\pi}{3} - \theta_o) \tag{3.58}$$

$$d_\beta = \frac{t_\beta}{T_s} = m_v \sin(\theta_o) \tag{3.59}$$

$$d_{0V} = \frac{t_0}{T_s} = 1 - (d_\alpha + d_\beta) \tag{3.60}$$

$$m_v = \frac{\sqrt{3} V_{om}}{V_{DC}} \tag{3.61}$$

where m_v is the modulation index of the inverter stage ($0 \leq m_v \leq 1$), θ_o is the angle of the vector $\vec{V_o}$ within the sector and d_{0V} is the duty cycle of the zero voltage vector $\vec{V_o}$.

For example, in Figure 3.28a which output reference vector is in sector 2, the dc-link current and output voltages are:

$$\begin{aligned} \vec{V_o} &= d_\alpha \vec{V}_\alpha + d_\beta \vec{V}_\beta \\ &= d_\alpha \vec{V}_{o2} + d_\beta \vec{V}_{o3} \\ \begin{bmatrix} v_X \\ v_Y \\ v_Z \end{bmatrix} &= (d_\alpha \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 0 & 1 \end{bmatrix} + d_\beta \begin{bmatrix} 0 & 1 \\ 1 & 0 \\ 0 & 1 \end{bmatrix}) \begin{bmatrix} v_P \\ v_N \end{bmatrix} \end{aligned} \tag{3.62}$$

$$\begin{bmatrix} I_{DC+} \\ I_{DC-} \end{bmatrix} = (d_\alpha \begin{bmatrix} 1 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} + d_\beta \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_X \\ i_Y \\ i_Z \end{bmatrix} \tag{3.63}$$

The output power equals the dc-link power at any instant as there is no energy storage element in the converter:

$$\begin{aligned} P_{DC} &= P_{out} \\ V_{DC} I_{DC} &= \frac{3}{2} V_{om} I_{om} \cos(\varphi_o) \end{aligned} \tag{3.64}$$

Therefore, the average value of the virtual dc-link current I_{DC} is determined as:

$$I_{DC} = \frac{\sqrt{3}}{2} m_v I_{om} \cos(\varphi_o) \tag{3.65}$$

where V_{om} and I_{om} are the peak values of the output phase voltage and the output current respectively, and φ_o is the output displacement angle.

3.3.6 Indirect space vector modulation for the entire matrix converter

The correct modulation pattern combines the switching states of the rectifier and inverter stages in such a way that the desired input and output waveforms can be obtained. The displacement factor is controlled to zero to obtain the maximum

Table 3.7: Valid switching combinations of the rectifier stage

k_i	sw_γ	sw_δ
1	$S_{AP}S_{BN}$	$S_{AP}S_{CN}$
2	$S_{AP}S_{CN}$	$S_{BP}S_{CN}$
3	$S_{BP}S_{CN}$	$S_{AN}S_{BP}$
4	$S_{AN}S_{BP}$	$S_{AN}S_{CP}$
5	$S_{AN}S_{CP}$	$S_{BN}S_{CP}$
6	$S_{BN}S_{CP}$	$S_{AP}S_{BN}$

Table 3.8: Valid switching combinations of the inverter stage

k_v	sw_α	sw_β
1	$S_{XP}S_{YN}S_{ZN}$	$S_{XP}S_{YP}S_{ZN}$
2	$S_{XP}S_{YP}S_{ZN}$	$S_{XN}S_{YP}S_{ZN}$
3	$S_{XN}S_{YP}S_{ZN}$	$S_{XN}S_{YP}S_{ZP}$
4	$S_{XN}S_{YP}S_{ZP}$	$S_{XN}S_{YN}S_{ZP}$
5	$S_{XN}S_{YN}S_{ZP}$	$S_{XP}S_{YN}S_{ZP}$
6	$S_{XP}S_{YN}S_{ZP}$	$S_{XP}S_{YN}S_{ZN}$

voltage transfer ratio and also for reducing the switching number and consequently the switching loss, the zero vectors are produced only on the inverter stage. On the other hand, the rectifier modulation index m_c is often fixed to unity and to adjust the overall voltage transfer gain of the IMC, the inverter modulation index m_v is considered variable. Tables 3.7 and 3.8 illustrate the valid switching combinations for the rectifier and inverter stages according to the sector of the input current and output voltage vectors respectively. Combination of the switching states of the rectifier and inverter stages depends on the sectors that input current and output voltage vectors are in.

The double sided switching pattern using one zero state is illustrated in Table 3.9 when the summation of the input and output hexagon sectors is odd or even [69] [90] [94, 95]. The zero switching sequence and its duty cycle can be expressed as:

$$Sw_0 = \begin{cases} 111 & k_i \; 'even' \\ 000 & k_i \; 'odd' \end{cases} \tag{3.66}$$

$$d_0 = 1 - (d_\gamma d_\beta + d_\gamma d_\alpha + d_\delta d_\alpha + d_\delta d_\beta) \tag{3.67}$$

Table 3.9: The switching pattern of the IMC using one zero vector

$k_i + k_v$ 'odd'					
Rectifier switching	sw_γ		sw_δ		
Rectifier switching duty cycles	$d_\gamma(d_\alpha + d_\beta)$		$1 - d_\gamma(d_\alpha + d_\beta)$		
Inverter switching	sw_β	sw_α	sw_α	sw_β	sw_0
Inverter switching duty cycles	$d_\gamma d_\beta$	$d_\gamma d_\alpha$	$d_\delta d_\alpha$	$d_\delta d_\beta$	d_0
$k_i + k_v$ 'even'					
Rectifier switching	sw_γ		sw_δ		
Rectifier switching duty cycles	$d_\gamma(d_\alpha + d_\beta)$		$1 - d_\gamma(d_\alpha + d_\beta)$		
Inverter switching	sw_α	sw_β	sw_β	sw_α	sw_0
Inverter switching duty cycles	$d_\gamma d_\alpha$	$d_\gamma d_\beta$	$d_\delta d_\beta$	$d_\delta d_\alpha$	d_0

The double sided switching pattern including three zero vectors is presented in Table 3.10 when the sum of the input and output hexagon sectors is odd or even. The zero switching sequences and their duty cycles are defined as:

$$Sw_{0a} = \begin{cases} 111 & k_i\ 'even' \\ 000 & k_i\ 'odd' \end{cases} \tag{3.68}$$

$$Sw_{0b} = \begin{cases} 000 & k_i\ 'even' \\ 111 & k_i\ 'odd' \end{cases} \tag{3.69}$$

$$\begin{aligned} d_{0v} &= 1 - (d_\alpha + d_\beta) \\ d_{0I} &= 1 - (d_\gamma + d_\delta) \end{aligned} \tag{3.70}$$

Figure 3.29 illustrates the operating approach of the DMC deduced from IMC. The modulation algorithm for DMC can be obtained from indirect modulation approach by substituting the virtual dc-link voltages v_P and v_N in (3.55) by (3.40),

Table 3.10: The switching pattern of the IMC using three zero vectors

$k_i + k_v$ 'odd'									
Rectifier switching	sw_γ				sw_δ				sw_δ
Rectifier switching duty cycles	d_γ				d_δ				d_{0I}
Inverter switching	sw_{0a}	sw_β	sw_α	sw_{0b}		sw_α	sw_β	sw_{0a}	sw_{0a}
Inverter switching duty cycles	$\frac{1}{2}d_\gamma d_{0v}$	$d_\gamma d_\beta$	$d_\gamma d_\alpha$	$\frac{1}{2}d_\gamma d_{0v}$	$\frac{1}{2}d_\delta d_{0v}$	$d_\delta d_\alpha$	$d_\delta d_\beta$	$\frac{1}{2}d_\delta d_{0v}$	d_{0I}
$k_i + k_v$ 'even'									
Rectifier switching	sw_γ				sw_δ				sw_δ
Rectifier switching duty cycles	d_γ				d_δ				d_{0I}
Inverter switching	sw_{0a}	sw_α	sw_β	sw_{0b}		sw_β	sw_α	sw_{0a}	sw_{0a}
Inverter switching duty cycles	$\frac{1}{2}d_\gamma d_{0v}$	$d_\gamma d_\alpha$	$d_\gamma d_\beta$	$\frac{1}{2}d_\gamma d_{0v}$	$\frac{1}{2}d_\delta d_{0v}$	$d_\delta d_\beta$	$d_\delta d_\alpha$	$\frac{1}{2}d_\delta d_{0v}$	d_{0I}

and the result is illustrated in (3.39). The duty cycles of the DSVM using the ISVM with unity input power factor are calculated as:

$$\begin{aligned}
d_{\alpha\gamma} &= d_\alpha d_\gamma = m_v \sin(\frac{\pi}{3} - \theta_o)\sin(\frac{\pi}{3} - \theta_i) \\
d_{\alpha\delta} &= d_\alpha d_\delta = m_v \sin(\frac{\pi}{3} - \theta_o)\sin(\theta_i) \\
d_{\beta\gamma} &= d_\beta d_\gamma = m_v \sin(\theta_o)\sin(\frac{\pi}{3} - \theta_i) \\
d_{\beta\delta} &= d_\beta d_\delta = m_v \sin(\theta_o)\sin(\theta_i) \\
d_0 &= 1 - (d_\gamma d_\beta + d_\gamma d_\alpha + d_\delta d_\alpha + d_\delta d_\beta)
\end{aligned} \tag{3.71}$$

3.3.7 Simulation results of the indirect matrix converter

The model of the indirect matrix converter shown in Figure 3.26 has been simulated using PSIM. Figure 3.31 shows the simulation results for an indirect matrix converter when $f_i = 50$, $f_o = 40$, $v_{s,ll,rms} = 400V$, $v_{o,ref} = 320V$ and the load and input filter parameters are the same as the DMC that mentioned before. Referring to Figure

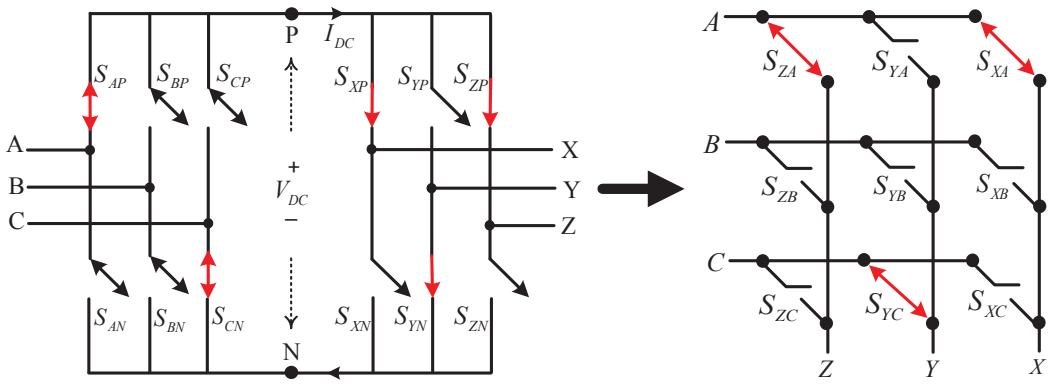


Figure 3.29: Graphical representation of the switch states of IMC and its equivalent circuit in DMC

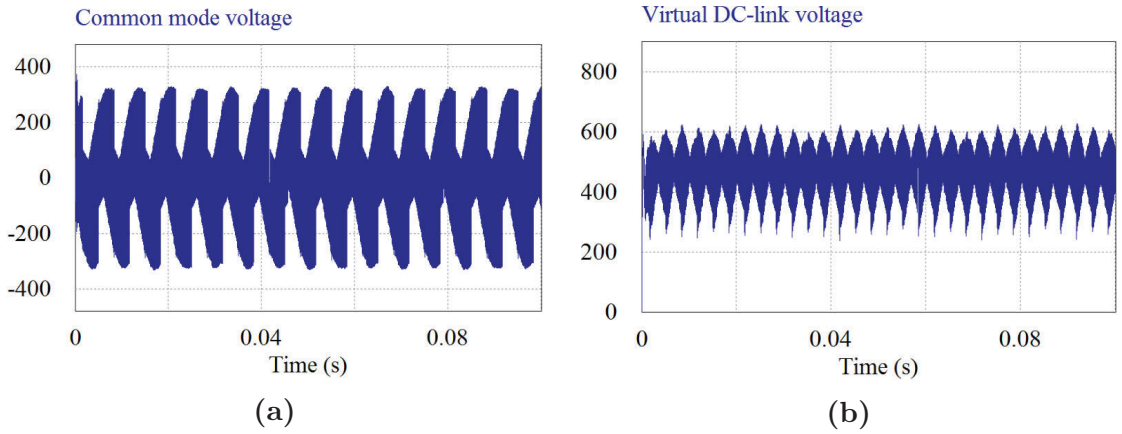


Figure 3.30: Simulation results of IMC, where a) Common mode voltage, and b) Virtual dc-link voltage V_{DC}

3.31h, the input current i_A has significant high-frequency harmonics which can be eliminated by using an appropriate low-pass LC filter, so that a sinusoidal, balanced input current is obtained at the supply side, as shown in Figure 3.31a. Therefore IMC can generate sinusoidal input and output currents like DMC. The inductive property of the load generates sinusoidal output currents from the output voltages generated by the inverter stage. Also, the input filter has such a role for smoothing the input current that returns to the input source.

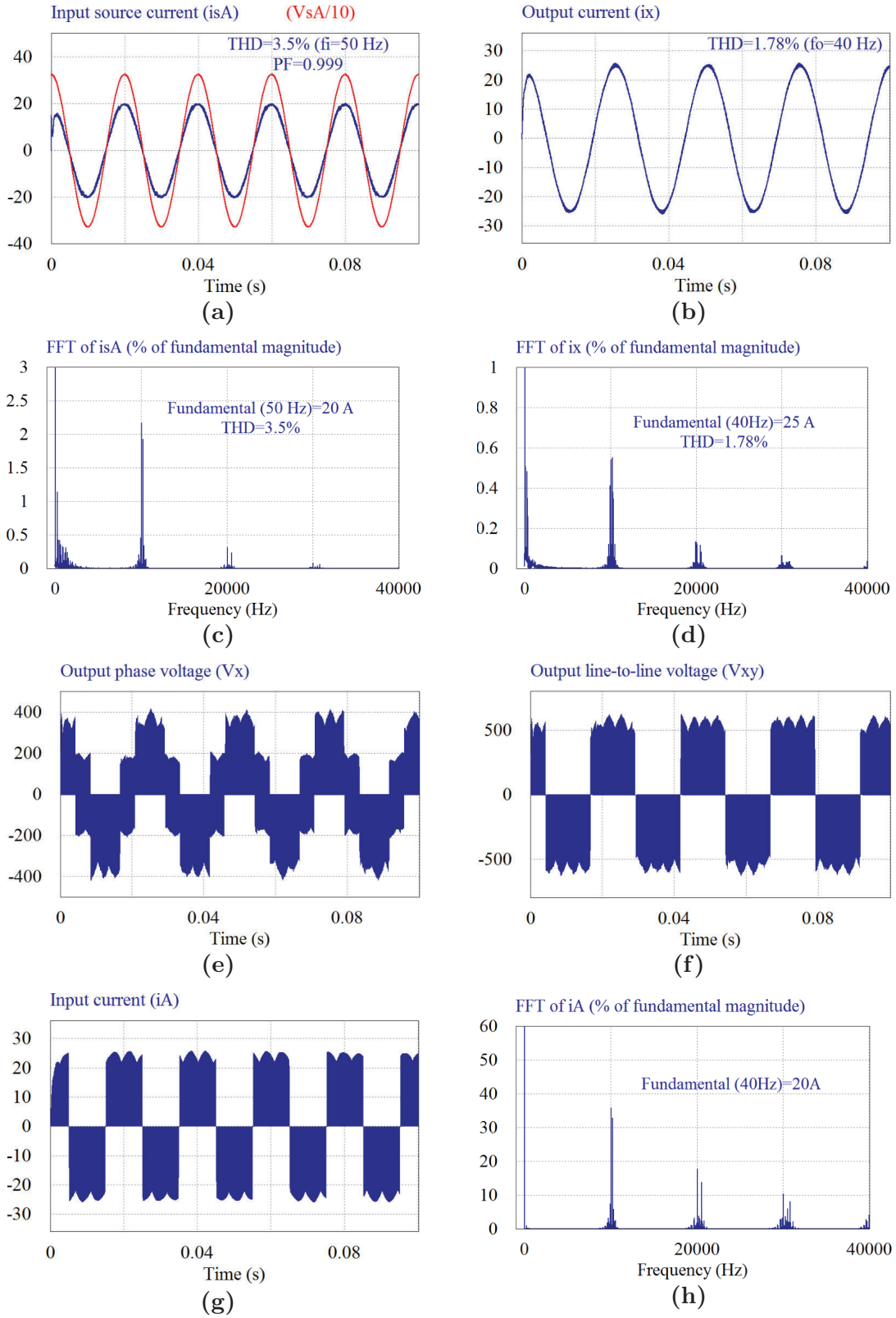


Figure 3.31: Simulation results of IMC, where a) Input source current and voltage i_{sA} and v_{sA}, b) Output current i_x, c) Frequency spectrum of i_{sA}, d) Frequency spectrum of i_x, e) Output phase voltage v_x, f) Output line-to-line voltage v_{xy}, g) Input current i_A, and h) Frequency spectrum of input current i_A

3.4 Conclusion

In this chapter, the basics of direct matrix converter and indirect matrix converter technologies and their modulation schemes have been reviewed. Three modulation strategies for controlling DMC including Alesina-Venturini modulation method, Alesina-Venturini optimum method and direct space vector modulation have been presented. All strategies operate in order to keep at any instant the input current space vector in phase with the input voltage vector that means instantaneous unity input power factor. The performance of these three modulation strategies has been analyzed in detail and verified by numerical simulations. The quality of the waveforms has been evaluated by the criteria of total harmonic distortion (THD). Then some of the modulation strategies have been implemented on a direct matrix converter prototype which has been designed for this project. The collected experimental results confirmed the validity of analysis and show good agreement with the numerical results. Also, ISVM has been performed on a simulated IMC, and according to the simulation and experimental results, both direct and indirect schemes are able to generate high-quality sinusoidal input and output currents. Although there is no experimental results for IMC to compare the results with DMC results, the simulation results show that there is no significant difference between the two structures. Finally, it has been found from the results that, space vector modulation is preferred to the other ones due to the higher voltage gain and lower harmonic distortions. In the case of the Alesina-Venturini optimised method, although it improves the voltage gain from 0.5 to 0.87, the THD of the input and output currents are too high.

Chapter 4

DESIGN AND IMPLEMENTATION OF A DIRECT MATRIX CONVERTER PROTOTYPE

4.1 Introduction

This chapter presents the basics of the prototype implementation of the DMC which has been developed to validate the simulation results presented in the thesis. At first, the overall structure of the prototype is described in brief, and then each part is explained in more details. As shown in Figure 4.1, the DMC prototype consists of four main parts: the power circuit with gate drivers, measurement and protection circuits, control platform, clamp circuit and input filter.

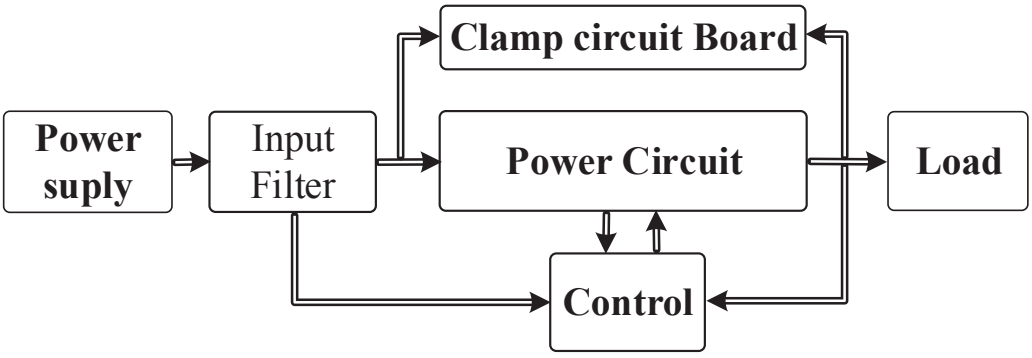


Figure 4.1: Block diagram of the overall structure of the designed DMC

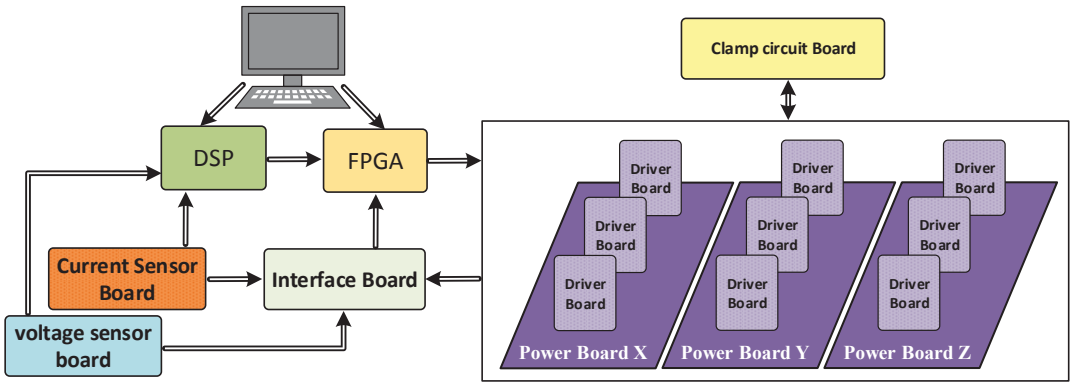


Figure 4.2: Block diagram of the overall structure of the control plan

Figure 4.2 shows a simplified block diagram of the DMC prototype. The general overview explains that the converter consists of the following main parts:

1. The power section includes the power modules, driver boards, input filter and a clamp circuit.

2. Voltage and current sensor boards and protection circuits.

3. Control section consists of the FPGA, the DSP and a PC.

More details of each part will be explained in the following sections.

4.2 The Power Module

The schematic of the power module is shown in Figure 4.3. The main parts of the power module of the DMC are the bidirectional switches which are based on the common-collector configuration of the IGBTs as demonstrated in Figure 4.4b. The power circuit consists of three separated PCB boards on the three heat-sinks, each of which consists of six IGBTs (IRG7PH42UD1-EP) containing an antiparallel connected diode (rated current 30A and voltage 1200V at 100℃ temperature as shown in Figure 4.4a), snubber circuit for each switch, three on-board drivers (VLA567-01R) and three filter capacitors.

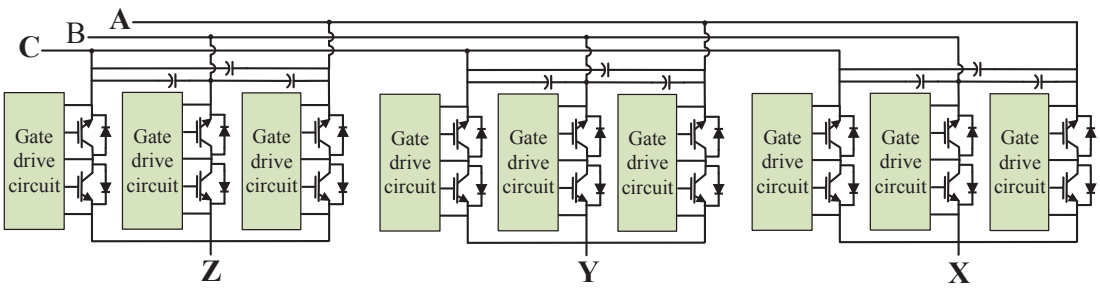
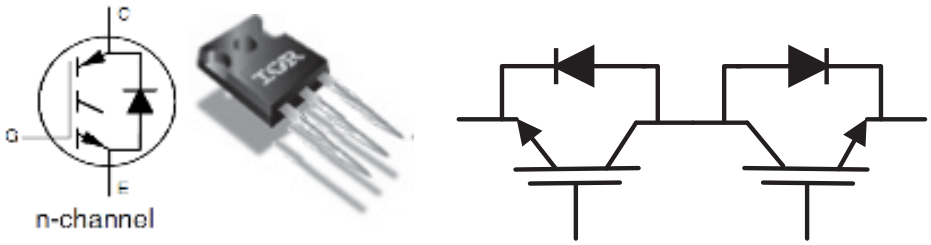


Figure 4.3: The schematic of the power module with driver boards



(a) **(b)**

Figure 4.4: IGBT switch, where a) TO-247ADIRG7PH42UD1-EP, and b) Schematic of a single bidirectional-switch

As there should be three delta-connected capacitors in the input filter, for better decoupling of the converter from the input side and minimising the effect of the parasitic inductances, each filter capacitor is split into three capacitors and connected directly to the bidirectional switches on each board [71]. All of the nine bidirectional switches have a filter capacitor in the input, and three input filter inductors with damping resistors are located between the input three-phase AC supply and the power boards.

As the traditional electrolytic capacitors have limited lifetime so, they replace with film capacitors. It was possible to build the power module using a large multi-layered printed circuit board but separating them into three PCB, each for one output phase is more convenient for fixing possibly damaged components.

4.3 Gate Drive Circuits

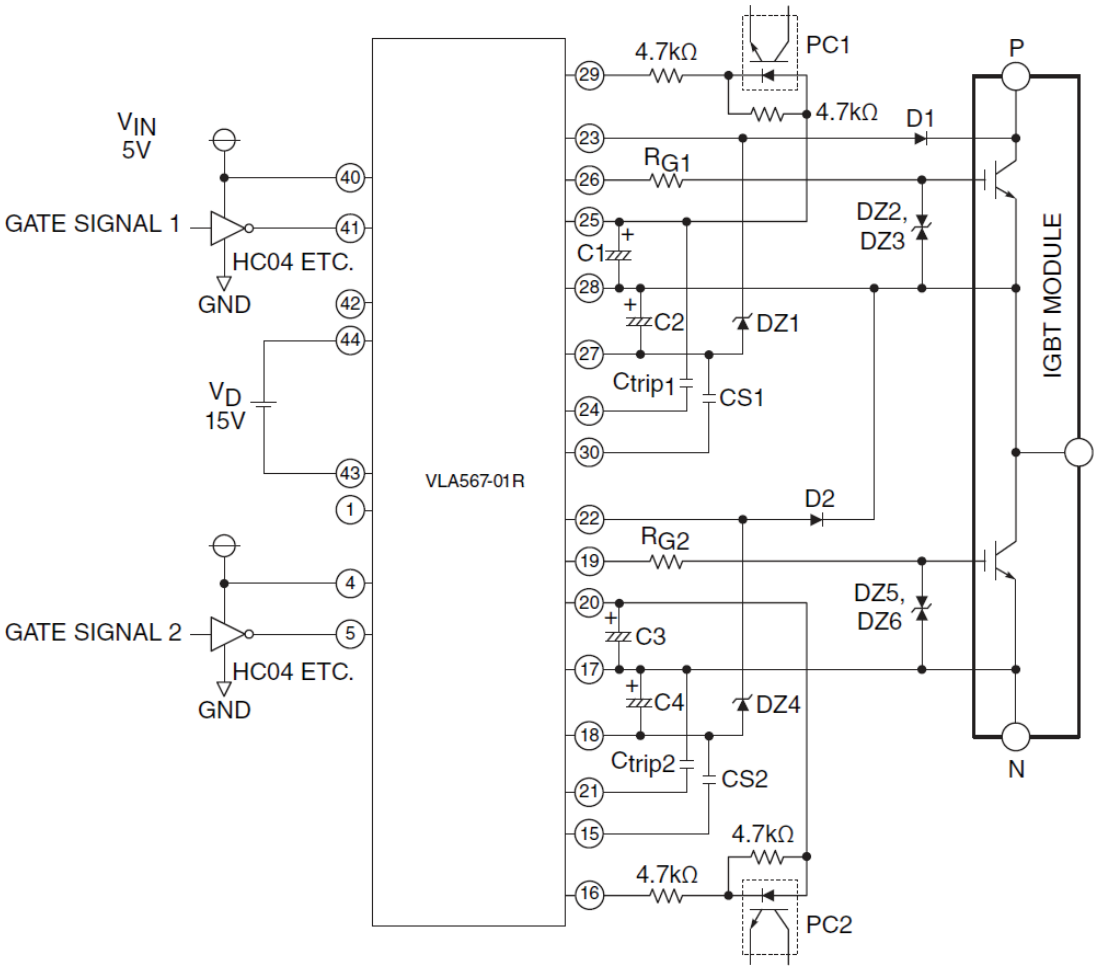
The driver board is designed to drive the IGBTs as the bidirectional switches on the power boards. The drive signals are applied to the switches through a hybrid integrated circuit (IC), VLA567-01R made by Powerx as shown in figure 4.5b. Each IC can drive two IGBTs at the same time (one bidirectional switch) and because it has a built-in isolated dc-dc converter required for the gate drive, so that it can be used in both, the common-collector and common-emitter configurations for bidirectional switches. The isolation voltage between each input and between input and output is 2500 Vrms. Figure 4.5a shows the circuit diagram of the driver board using VLA567-01R driver integrated circuit, and Figure 4.6 presents the outline drawing and circuit diagram of the IC [6]. Although Figure 4.5a shows the switch configuration for a leg of an inverter, it can drive a bidirectional switch too.

To protect the switches from failure under short circuit condition, the collector to emitter voltage should be monitored continuously. The driver IC includes a built-in short circuit protection that provides gate lockout to maintain a reverse bias for a predetermined time (T_{trip}) after the short circuit detection. A controlled time (T_{trip}) to detect the short circuit should be predetermined by a capacitor (C_{trip}). When the collector voltage is high, and the applied input voltage to the gait stays ON for a time longer than (T_{trip}), the IC will recognise the condition as a short circuit and consequently reduce the gate voltage. The flowchart of the short circuit detection process is presented in Figure 4.7 [6].

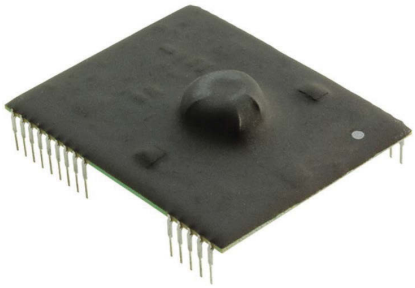
To achieve the minimum distance between the switches and gate drive signals each gate driver board is placed as close as possible to the power board. Figure 4.8 presents a photograph of the power boards with the driver boards.

4.4 Interface Board

The interface board is designed to link the FPGA to the protection circuits and driver boards. The output voltage level of the DSP is compatible with the FPGA,



(a)



(b)

Figure 4.5: Driver integrated circuit, where a) Schematic of the driver board using VLA567-01R driver integrated circuit, and b) VLA567-01R driver integrated circuit [6]

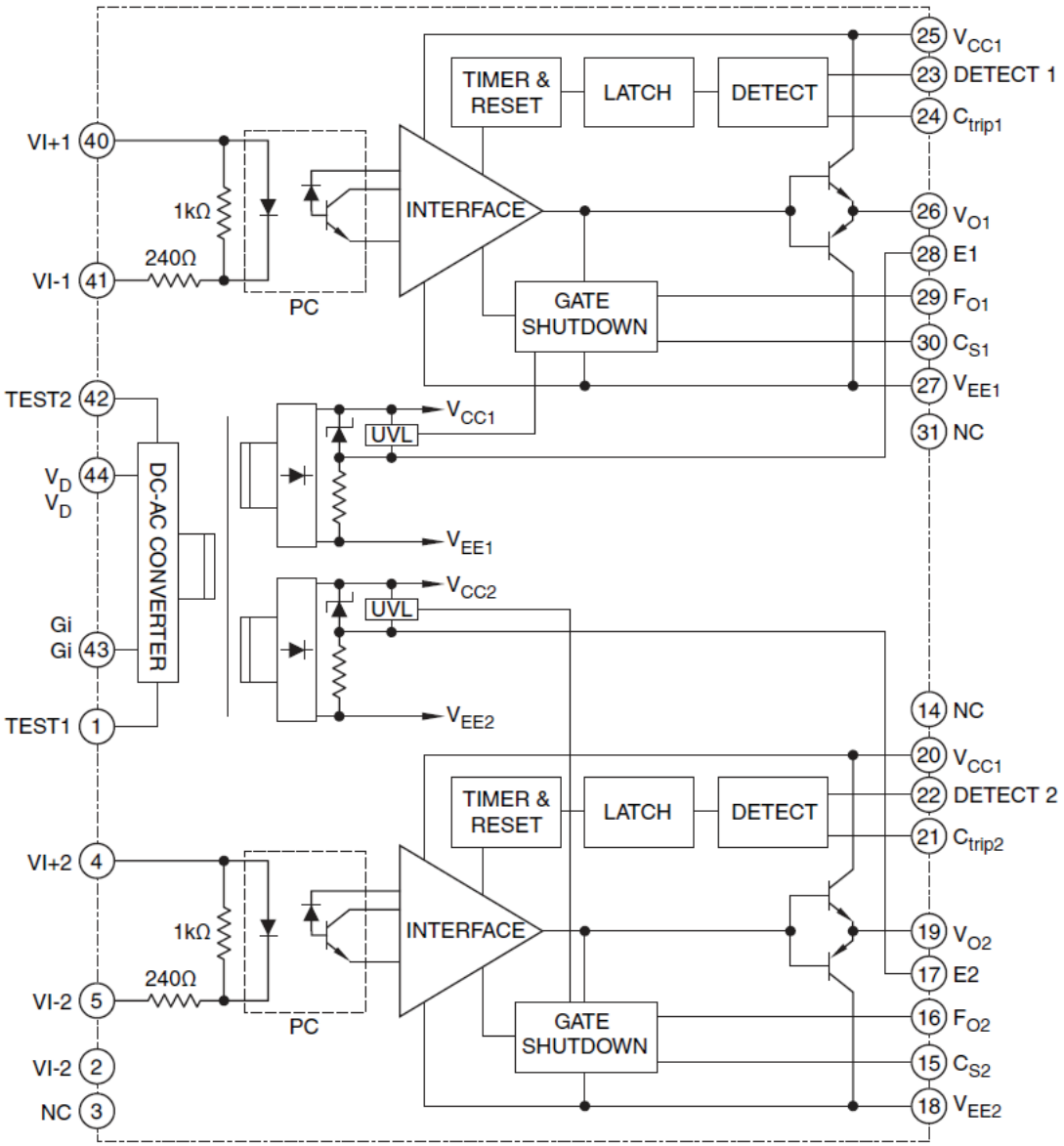


Figure 4.6: Outline drawing and circuit diagram of VLA567-01R [6]

and both are 3.3 V, so that the DSP output signals can be connected to the input connector of the FPGA without converting the logic level. However, the level conversion is necessary for connecting the outputs of the current and voltage protection boards to the FPGA as their output voltages are 5V and from FPGA to the driver boards.

The SN74LVC16T245 16-bit dual-supply bus transceiver with configurable voltage translation is used for the level shifting. It uses two separate configurable power

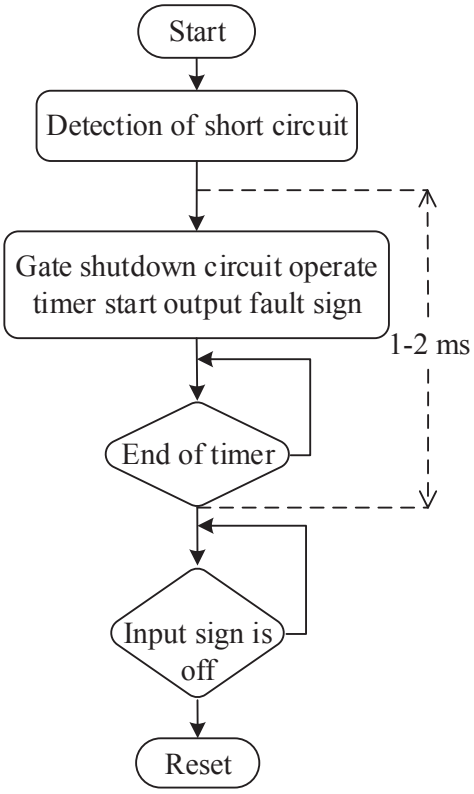


Figure 4.7: Operation flowchart on detecting short circuit [6]

supply from 1.65 to 5.5 and allows for low-voltage bidirectional translation between 3.3 V and 5 V. The incoming protection signals (overvoltages, overcurrents, short circuits and current directions) to the FPGA should be level shifted to 3.3V. On the other hand, the FPGA output PWM signals should be stepped up to 5V before connecting to the driver boards. It also buffers the PWM gate-drive signals using the 74HCT2G04 dual inverter which provides two inverting buffers for each driver board.

4.5 Input Filter

The input current THD should be limited to the standard level. A single-stage LC filter with the incorporation of damping in the form of resistors in parallel with the inductors is used to provide the required attenuation with the arrangement demonstrated in Figure 4.9. As the damping ratio of the LC filter is not enough for

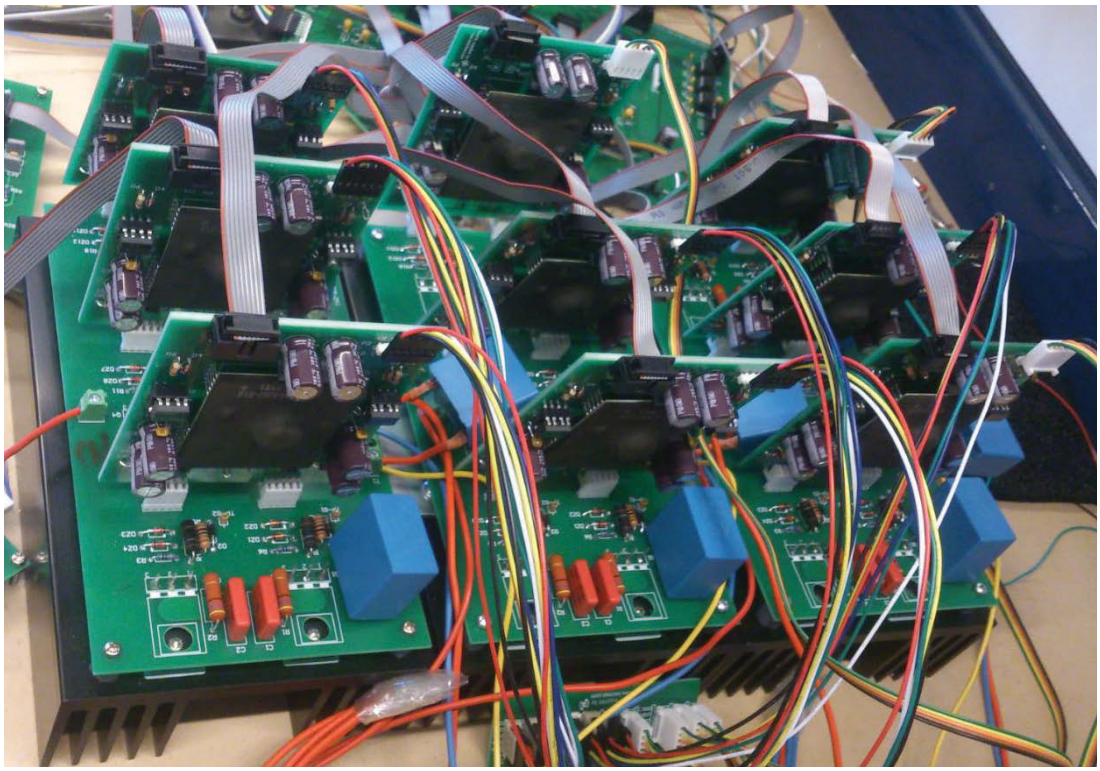


Figure 4.8: Photograph of the power boards with the driver boards on them

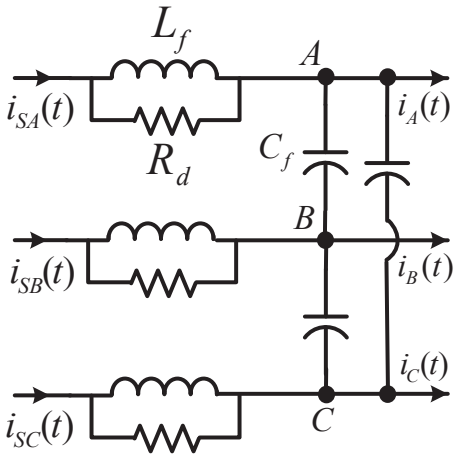


Figure 4.9: Schematic of the input filter circuit with damping resistors in parallel with the filter inductances

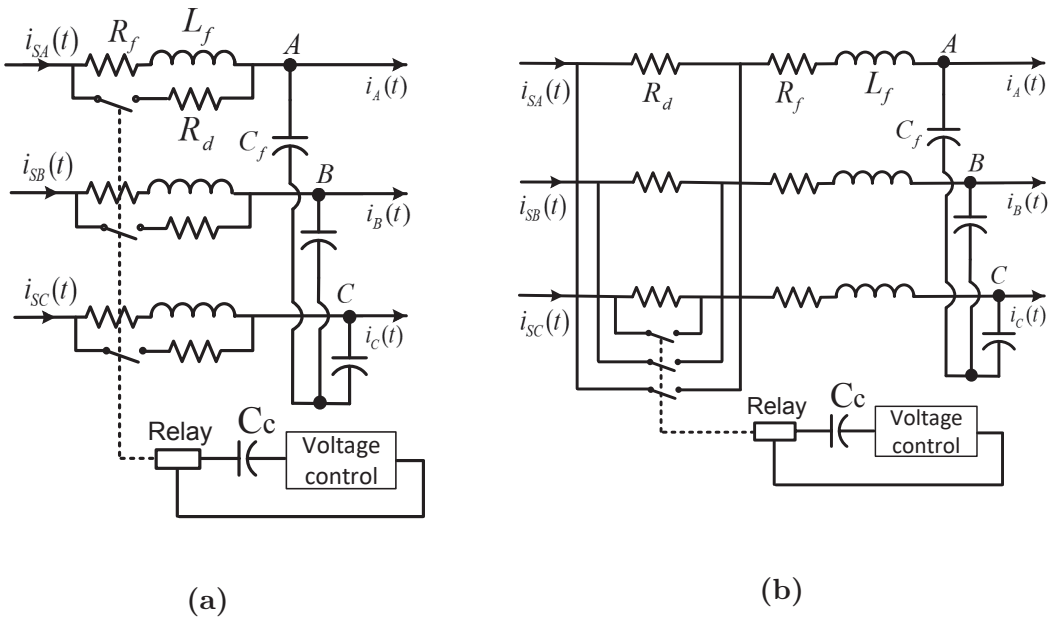


Figure 4.10: Second order LC filter with bypass relays for preventing of more power loss, and damping resistors, where a) in parallel, and b) in series with the inductors

fast and safe power-up, and when a voltage step is applied to the MC, it causes a transient over-voltage level and oscillation that can lead to instability. The inductors should be damped using three parallel or series resistors with the filter inductance. In order to reduce the power loss caused by the damping resistors, they can be bypassed by using the bypass relays as illustrated in Figure 4.10 [70] [27]. The damping resistors are used because input currents are possible at some operating points, to contain a harmonic close to the cut-off frequency of the filter and cause the converter to be unstable.

For the prototype converter, three star-connected $6.6\mu F$ capacitors (split into three star-connected $2.2\mu F$ for each power board) are used which are connected in series with a set of three inductances of approximately 3 mH each, to produce a cut-off frequency of about 1.13kHz. This resonant frequency is well below the switching frequency (10 kHz), and so this filter can effectively filter out the harmonics caused by switching, while the phase shift caused by the filter is close to zero over the input frequency range. The input displacement factor is still close to unity. The damping resistor can be found according to the (2.15), which should be less than 21.32Ω.

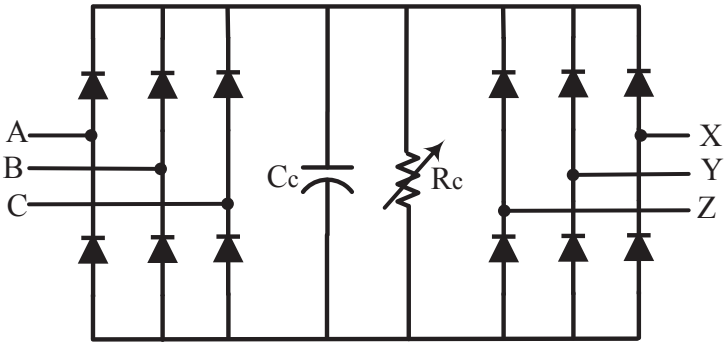


Figure 4.11: Schematic of the clamp circuit

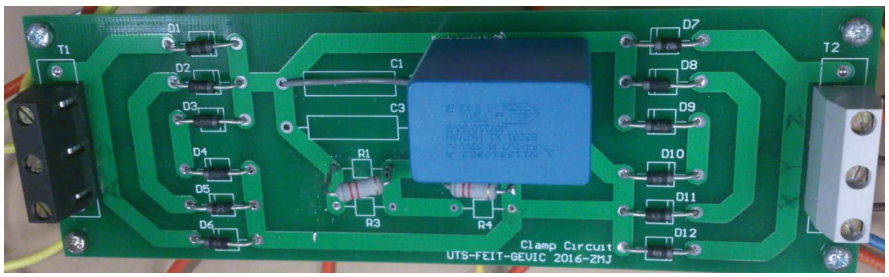


Figure 4.12: Photograph of the clamp circuit

4.6 Clamp Circuit

The clamp circuit includes two rectifier bridges using six fast recovery diodes, a clamp capacitor and a parallel resistor and protects the MC against over currents or over voltages on both input and output sides of the converter. Figure 4.11 shows the schematic of a typical clamp circuit. In the case of an R-L load, the energy stored in the inductances and in the case of an induction motor the energy stored in the leakage inductances cause an over voltage during converter shutdown if there is no discharge way. On the other hand, line perturbations can case over voltages on the grid side [27]. As shown in Figure 4.12 the clamp circuit for this prototype is built on a separate PCB and connected to the input and output sides of the MC to limit the over-voltage level on both supply and load sides.

In normal conditions the clamp capacitor charges to the maximum input line voltage. Under a fault condition which an error signal is generated by any protection circuits and the FPGA sends turn off command to the drivers to shut down all the

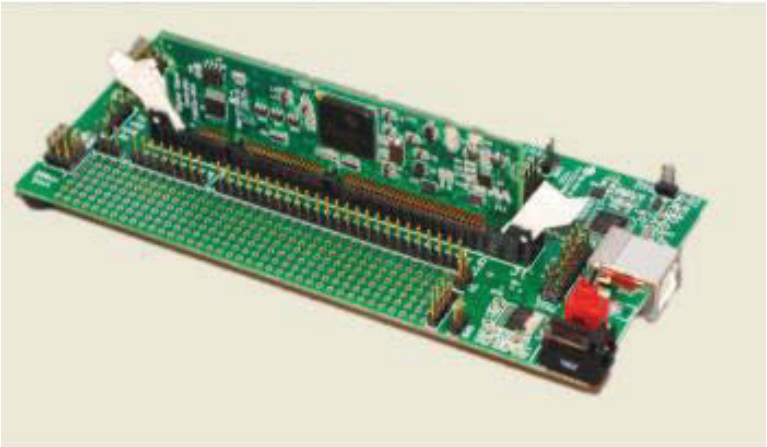


Figure 4.13: TMS320F28335 Experimenter Kit [7]

switches at the same time, the clamp circuit is the way for discharging the load energy.

It can be seen from 2.19, for designing the clamp capacitor by considering the switches characteristics, the maximum acceptable voltage and current should be determined. In this prototype IRG7PH42UD1-EP IGBT switches have $V_{CE,max} = 1200V$ and $I_{nominal} = 30A$. Assuming the converter current limit about 20 A and maximum voltage of the clamp capacitor $V_{C_c,max} = 1200V$, L_l=6 mH, $V_{im,ll} = \sqrt{2} * 400V = 565V$, C_c becomes 3.2 μF.

4.7 Matrix Converter Control

The control unit comprises of a digital signal processor (DSP) board and a field programmable gate array (FPGA) board. The modulation calculations and control functions are performed by the DSP as the main processing unit. In this prototype, the TMS320F28335 Experimenter Kit manufactured by Texas Instruments is used as the central processor. A fast processor is required due to the relatively intensive mathematics of every switching cycle of a MC with the short time scales for performing the calculations. Operating at 150 MHz, the TMS320F28335 DSP offers sufficient processing capability required for this application. The processor features 18 PWM channels with high-resolution capability, 512 KB integral flash, a 150 MIPS

processing core with floating point support and 12-bit, 12.5 MSPS analogue to digital converter (ADC). The C2000 experimenter kit facilitates real-time in-system programming and debugging using an isolated XDS100 JTAG emulator for connection to the PCB via USB port and header pins access to key micro-controller signals. Also, the code composer studio (CCS) is the required software for programming and debugging the DSP using a PC. Figure 4.13 shows the TMS320F28335 Experimenter Kit.

The DSP handles the following tasks:

1. Creating the output voltage reference in the case of R-L load and open loop control.

2. Converting three-phase input voltages, output current and reference voltages to digital quantities by ADC.

3. Determining the instantaneous locations of the input and output voltage vectors and generating the sector codes of $K_i and K_v$ and also the angle of each vector in the related sector.

4. Calculating the duty cycles $d_0, ..., d_4$ according to the voltage gain and instantaneous angles.

5. Transferring the PWM signals to the FPGA.

The output signals of the DSP board are connected to the power circuit through a Xilinx spartan6-LX150T development board (manufactured by AVNET) which includes a Xilinx-spartan6 FPGA as presented in Figure 4.14. This kit has the FPGA processor mounted on a PCB with the required memory and associated peripherals that allow it to be connected to a PC through a JTAG cable and used with ISE Design Suite 14.6. Figure 4.15 shows the main components of the FPGA development board.

The Spartan-6 LX150T development board provides expansion capabilities for customised user application daughter cards and interfaces over two low pin count

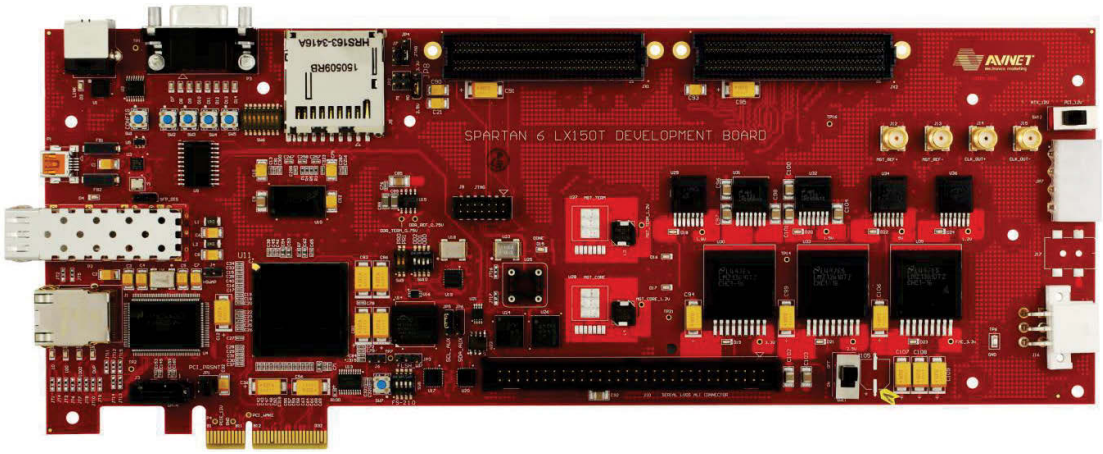


Figure 4.14: XILINX Spartan-6 LX150T Development Board used for this prototype [8]

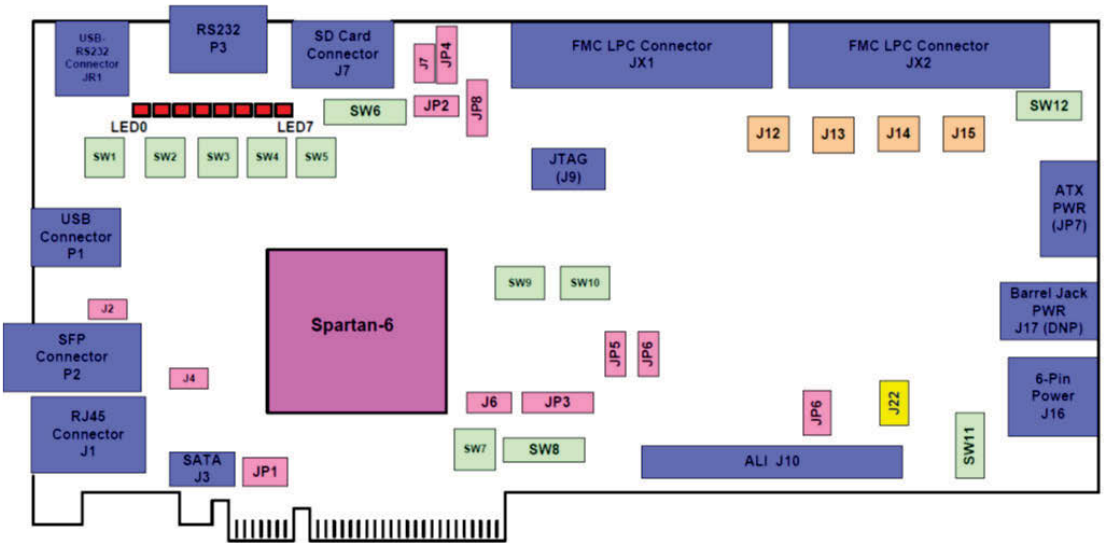


Figure 4.15: XILINX Spartan-6 LX150T development board main components [8]

(LPC) FPGA Mezzanine Card (FMC) expansion connectors. The LPC connectors on the development board have populated 160 of the 400 possible positions of HPC (High Pin Count) version of the connector. The FMC defines the LPC interface to be a 160-pin connector arranged in a 4×40 array. Figure 4.16 explains the installation of the mezzanine card to FMC Connector [9].

The most important function of the FPGA is the commutation process and generating the gate control signals for bidirectional switches. The gate control signals are applied to the gate drivers through the interface board. The concept of the 4-step commutation method has been explained in previous sections. By using the VHDL

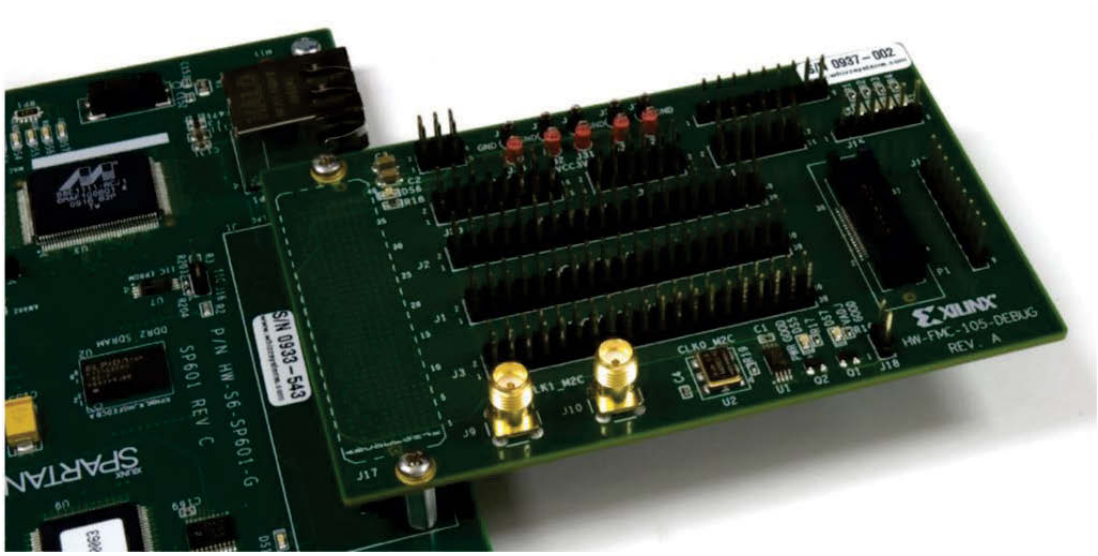


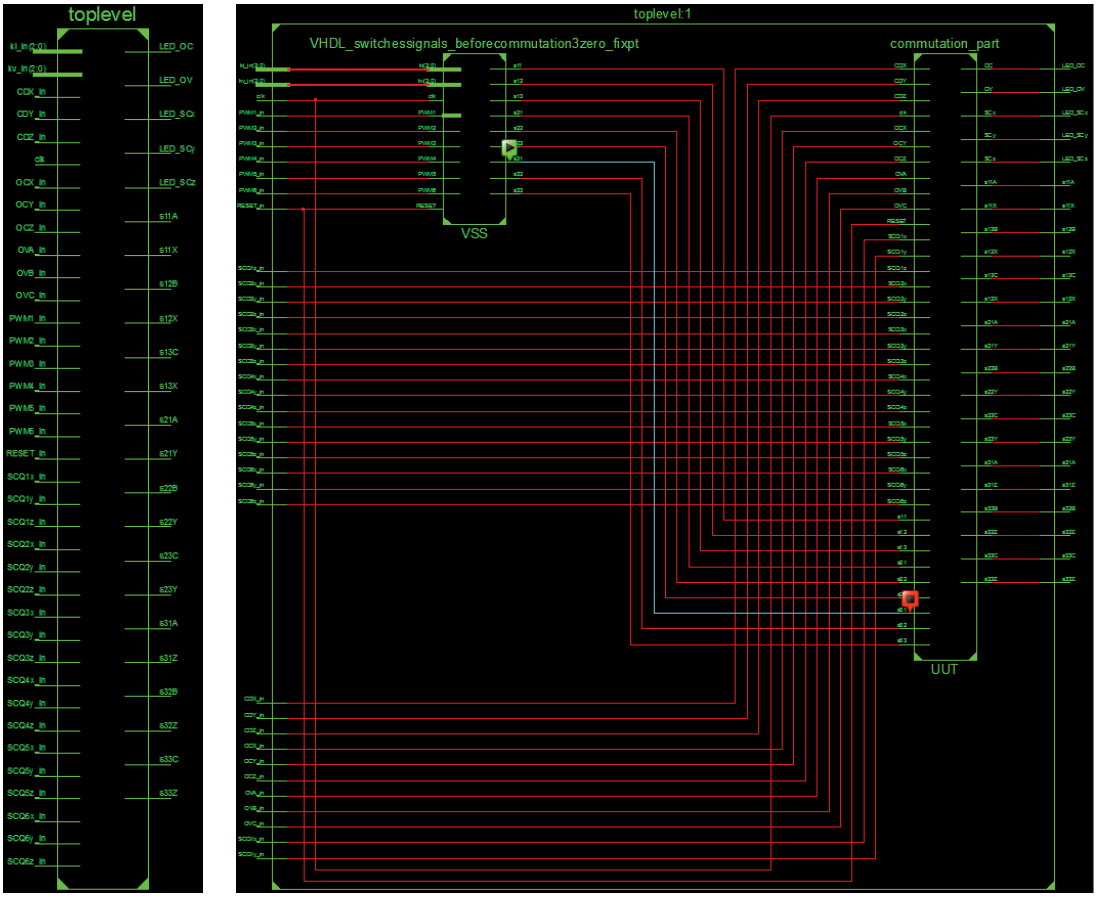
Figure 4.16: Installation of Mezzanine Card to Board FMC Connector [9]

(very high speed integrated circuit hardware description language), logic gates and state machines for 4-step commutation strategy can be programmed into the FPGA. An FPGA consists of programmable logic components and interconnections. The architecture of FPGA is parallel; it means that different parts of the implemented control algorithm in an FPGA can be executed in parallel so that the execution time is very short [80]. Therefore due to the fast computational capability of FPGAs, it is reasonable to put a part of the modulation algorithm as well as the commutation process in the FPGA to increase the performance of the control part and reduce the DSP load. On the other hand, the commutation process needs to be performed simultaneously and in parallel for the active switching devices. Figures 4.17b shows the top-level block of the control algorithm in the FPGA.

According to the Figure 4.18 which illustrates the overall control structure of the converter, the FPGA board handles the following tasks:

1. Receiving PWM signals, sector codes of the current and voltage space vectors from DSP and creating nine switching pulses for bidirectional switches.

2. Performing the current commutation process using the switching pulses and current-direction signals and generating 18 switching pulses for driver boards.



(a) **(b)**

Figure 4.17: The control algorithm in the FPGA, where a) Top-level block, and b) Inside the top-level block

3. Turning off all the switches if there is any fault condition considering the over-voltage, over-current and short-circuit signals from protection circuits.

4.8 Measurement and Protection Circuits

The measurement circuits comprise of current transducers, voltage transducers, over-voltage and over-current protection circuits and current direction detection circuits. The voltage transducers and over-voltage protection circuits are mounted on one PCB board, and the current direction measurement and protection circuits are

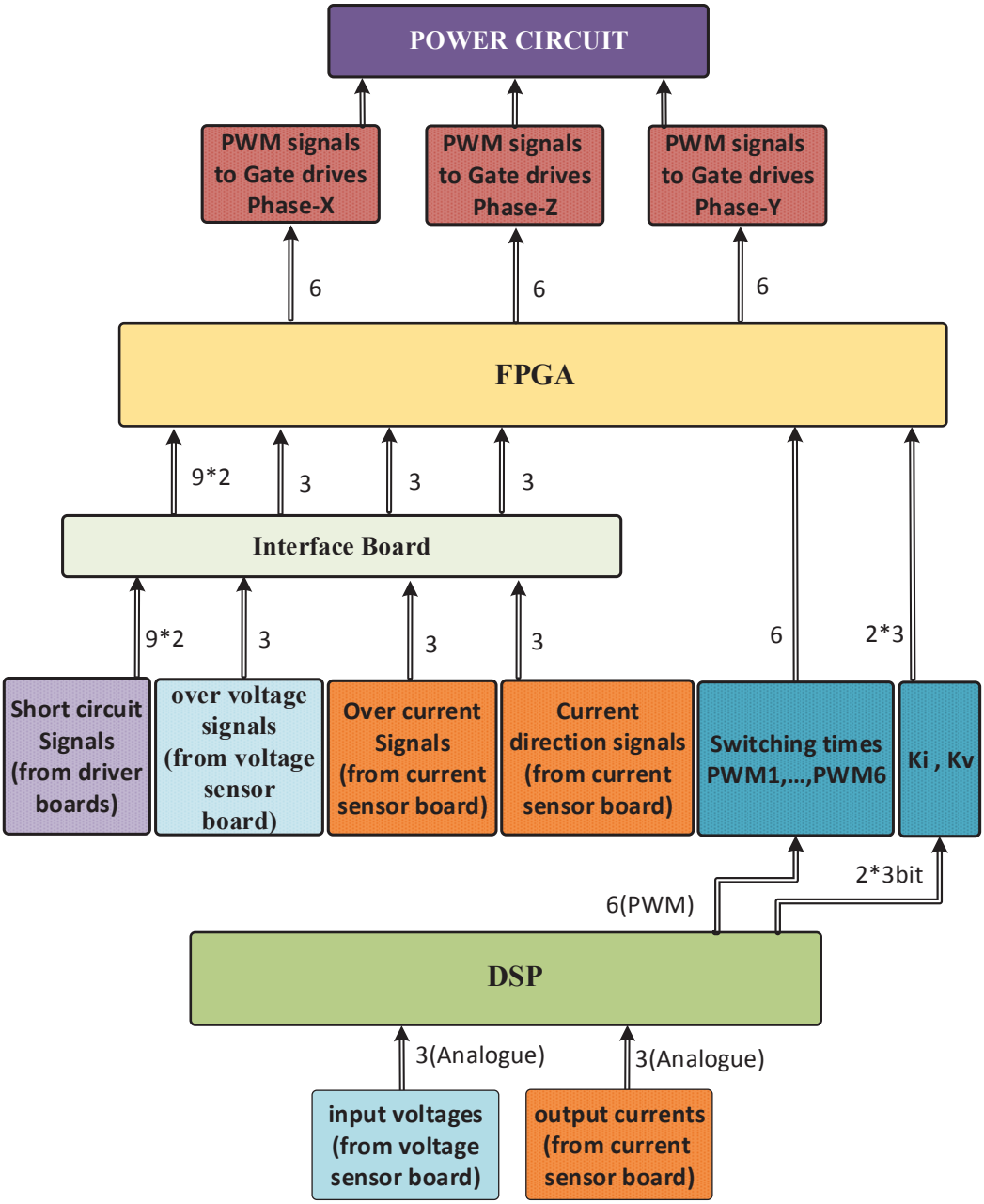


Figure 4.18: Overall structure of the control platform

placed on another PCB board. The separated PCBs are due to the difference between voltage and current levels of the measuring signals, noise sensitivity of the components and easier maintenance if any failure happens. The current transducers also are assembled on a different PCB to reduce the distortions in the measured

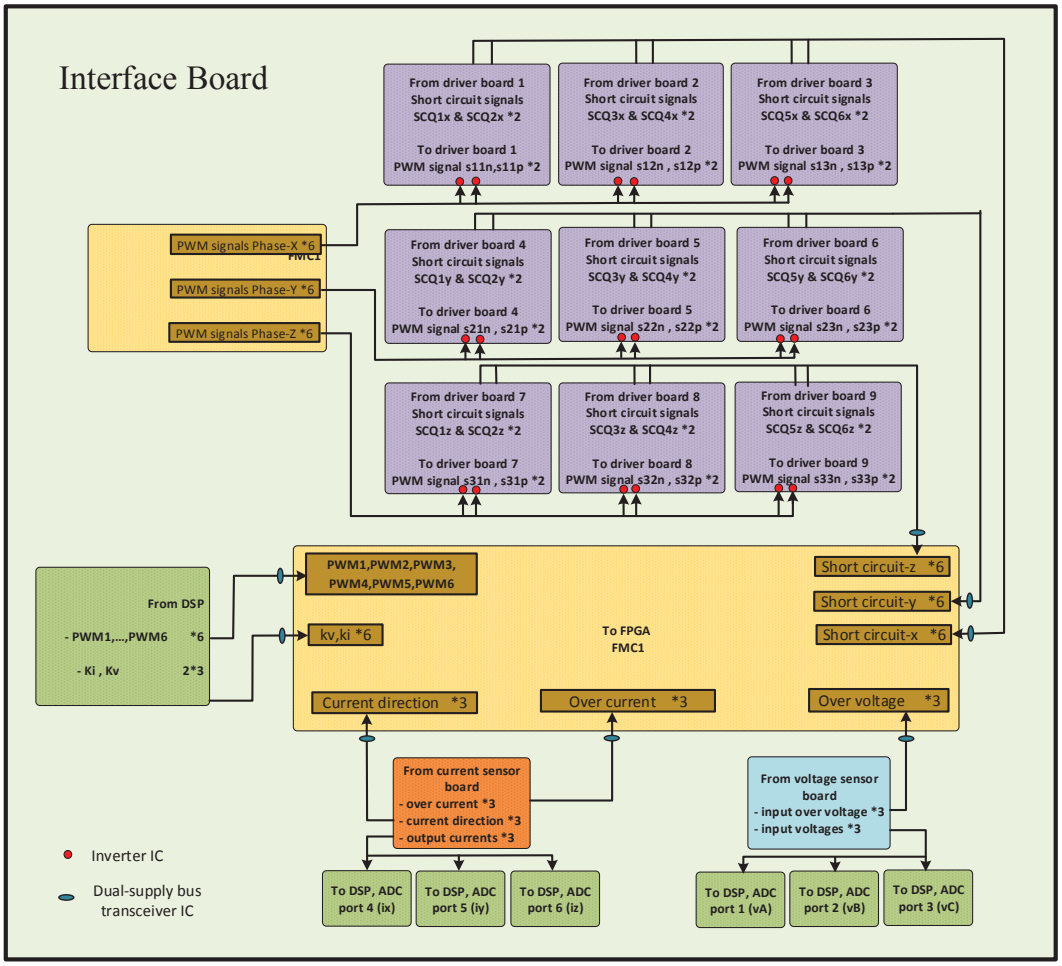


Figure 4.19: Overall structure of the interface board

currents. Each one of these circuits will be reviewed in more detail in following.

4.8.1 Input voltage measurement and protection circuits

According to the SVM strategy, the reference angle of the input current space vector is required to determine the duty cycles and switching sequences. On the other hand, to reach the unity input power factor, the generated input currents are synchronised with the input voltages, and the input phase voltages should be measured to determine the angle and sector of the input current space vector. For this purpose, the LEM voltage-transducer, LV 25-P, is used as shown in Figure 4.20 that is suitable for measuring nominal voltages from 10 to 500V. For voltage measurement

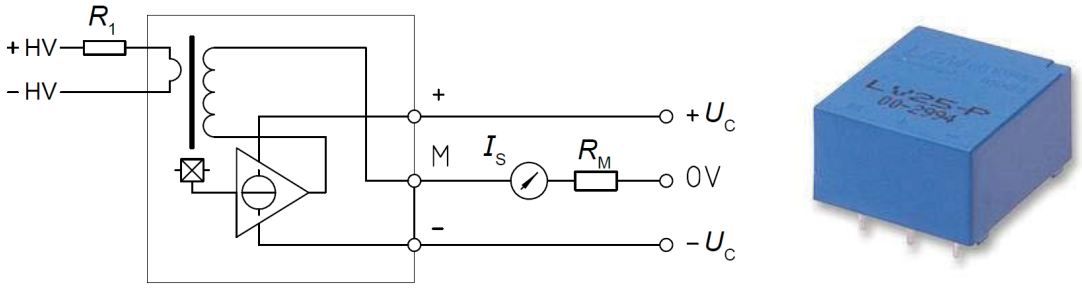


Figure 4.20: Voltage transducer LV 25-P [10]

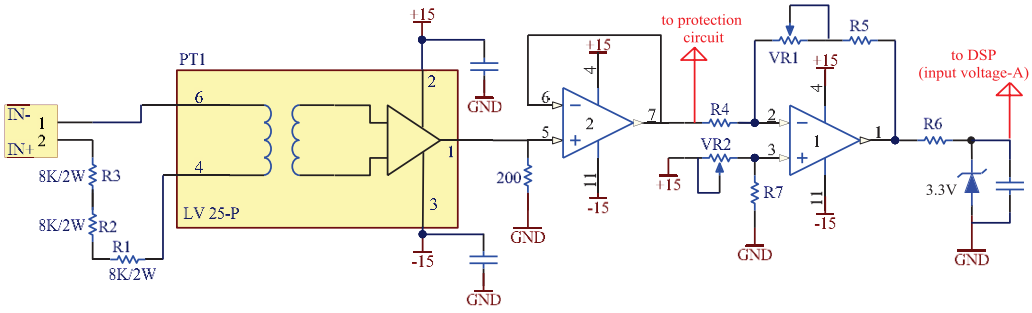


Figure 4.21: Schematic of the voltage measurement circuit

using this Hall effect transducer, a current proportional to the measured voltage must be passed through an external resistor (R1) which is installed in series with the primary circuit of the transducer as shown in the schematic diagram of Figure 4.20. The primary resistor R1 should be calculated to obtain the transducer's optimum accuracy. Therefore the nominal voltage should be measured corresponds to a primary nominal current rms of 10 mA. To measure the input voltage 240V(rms), $R1 = 240V/10mA = 24k\Omega, 2.4W$ ($3 \times 8k\Omega, 2W$ has been utilized). As the secondary nominal rms current is 25mA, considering the conversion ratio 2500:1000, the output of the transducer is a voltage proportional to the current passing through the resistor R_m [10].

After measuring the voltage using the voltage transducers, the measured voltages which are connected to the ADC of the DSP must be between 0V to 3.3V. As shown in Figure 4.21, using amplifier OP4227, the output signals meet the required

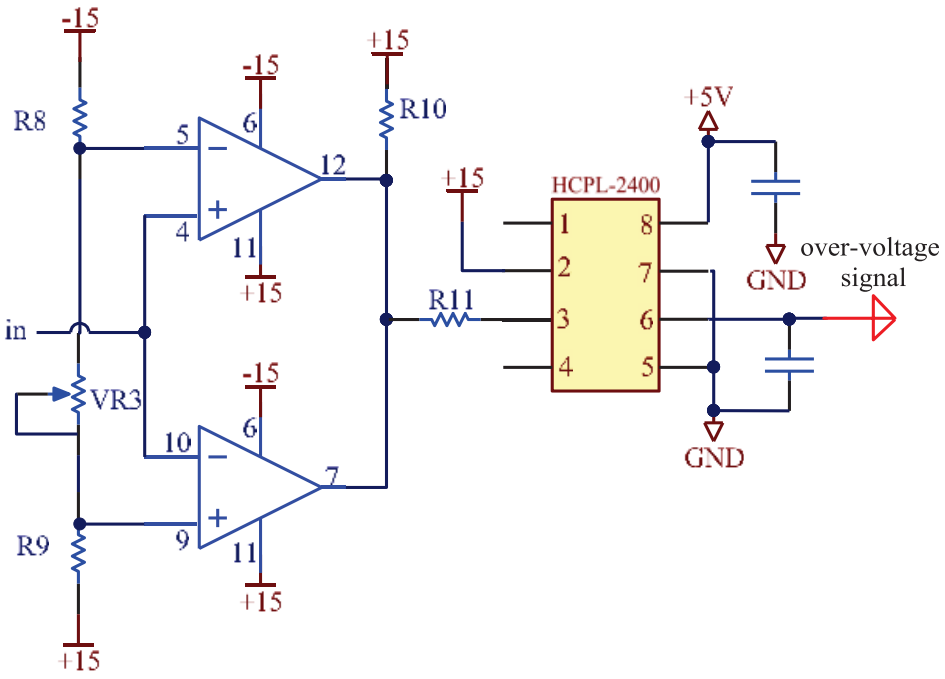


Figure 4.22: Schematic of the over-voltage protection circuit

level for DSP. Also by a window comparator using LT119A (dual comparator IC) the over-voltage (OV) fault signals are generated as well. For monitoring the fault signals in the FPGA, three HCPL-2400 optocouplers are used to convert the voltage level to +5V and then they are applied to the FPGA through interface board after level shifting to 3.3V. The isolation between the analogue and digital circuits is performed by using the optocouplers as presented in Figure 4.22. Zener diode with cut off voltage 3.3V is used to clamp the voltage to the safe level for DSP. Figure 4.23 shows a picture of the voltage measurement circuit board that has been built for the prototype.

4.8.2 Output current measurement

To measure the output currents, the inline current transducer LEM, LTSR 25-NP is used as shown In Figure 4.25 [11]. The output of the transducer is a voltage

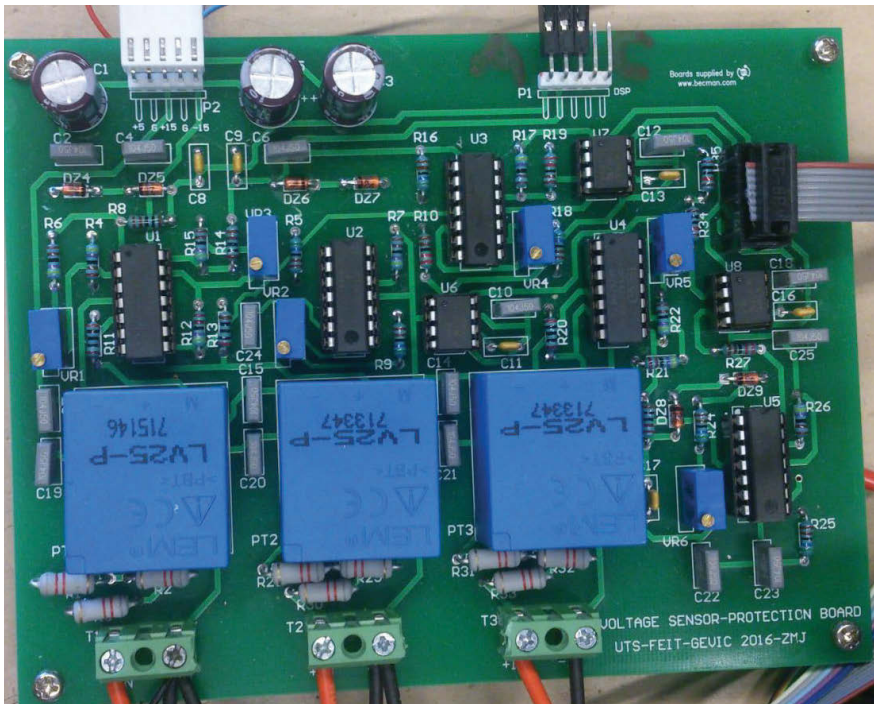
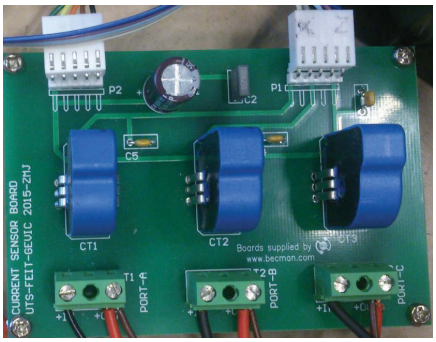
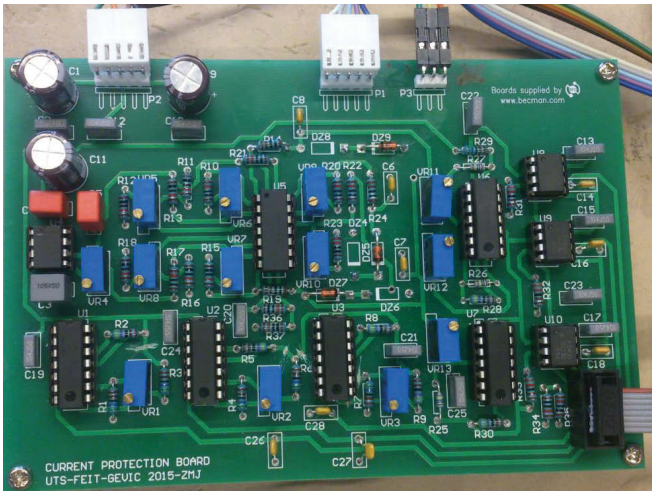


Figure 4.23: The voltage measurement and protection board



(a)



(b)

Figure 4.24: Prototype current measurement board, where a) Current sensor board, and b) Current measurement and protection circuits

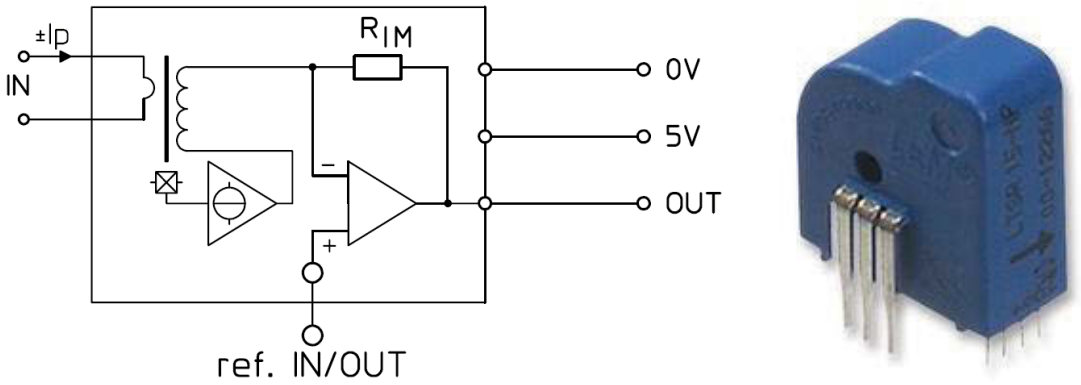


Figure 4.25: Current transducer LTSR 25-N [11]

between 0.5 to +4.5V proportional to the measured current as illustrated in Figure 4.26, so the output voltage for zero input current is +2.5V [11]. This offset should be cancelled out using a voltage reference generated by IC MAX6225 and amplifier OP4227. The amplified output of the op-amp then is fed into a non-inverting comparator with hysteresis to determine the current direction (CD) at any instance, as the 4-step commutation is used for this prototype. An optocoupler is used to reduce the CD voltage level to 0-5V and to provide the electrical isolation between the measurement circuit and the control platform. The schematic diagram of the output current measurement and current direction detection circuit of this prototype are illustrated in Figure 4.28.

On the other hand, to ensure protection against over-current, the output currents should be continuously monitored by a circuit that generates over-current (OC) fault signals. The schematic diagram of the over-current protection circuit is shown in Figure 4.27. The OC signals are sent to the FPGA through the interface board. Figure 4.24 shows a picture of the current sensor and current measurement boards.

4.9 Conclusion

The basics of the hardware design and implementation of power and control boards of the DMC have been presented in this chapter. A 7.5 kW laboratory prototype

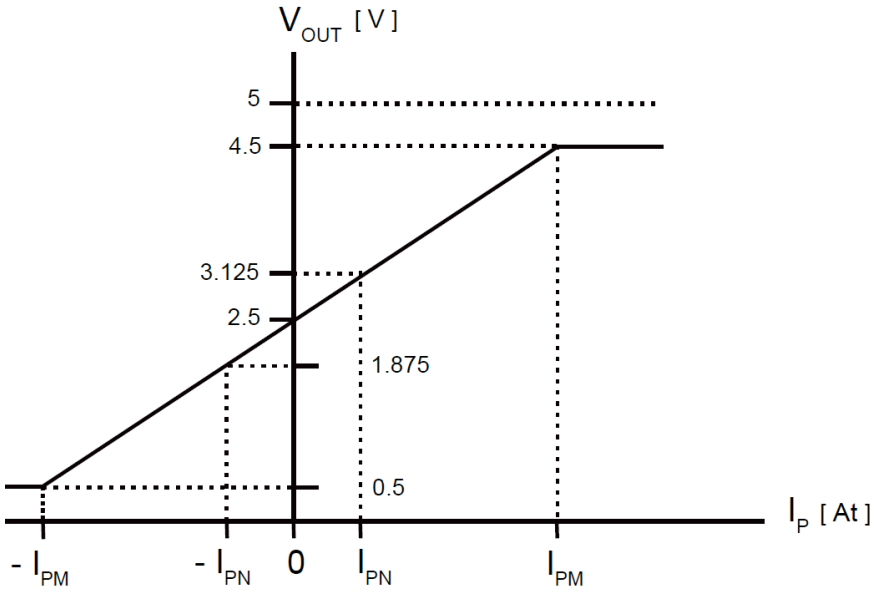


Figure 4.26: Input-output characteristic of the current transducer LTSR 25-N [11]

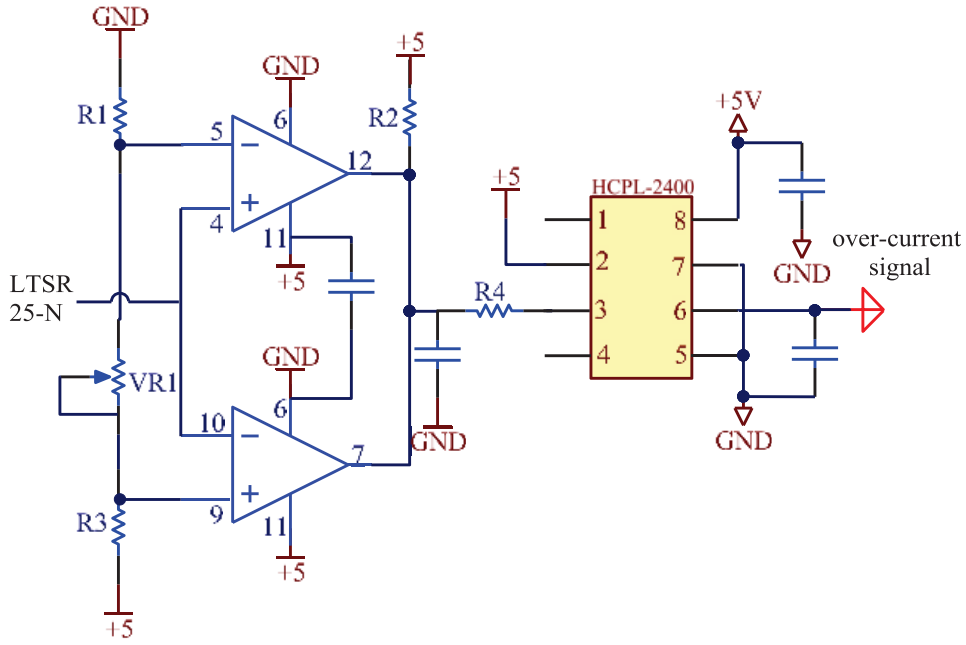


Figure 4.27: Schematic of the over-current protection circuit

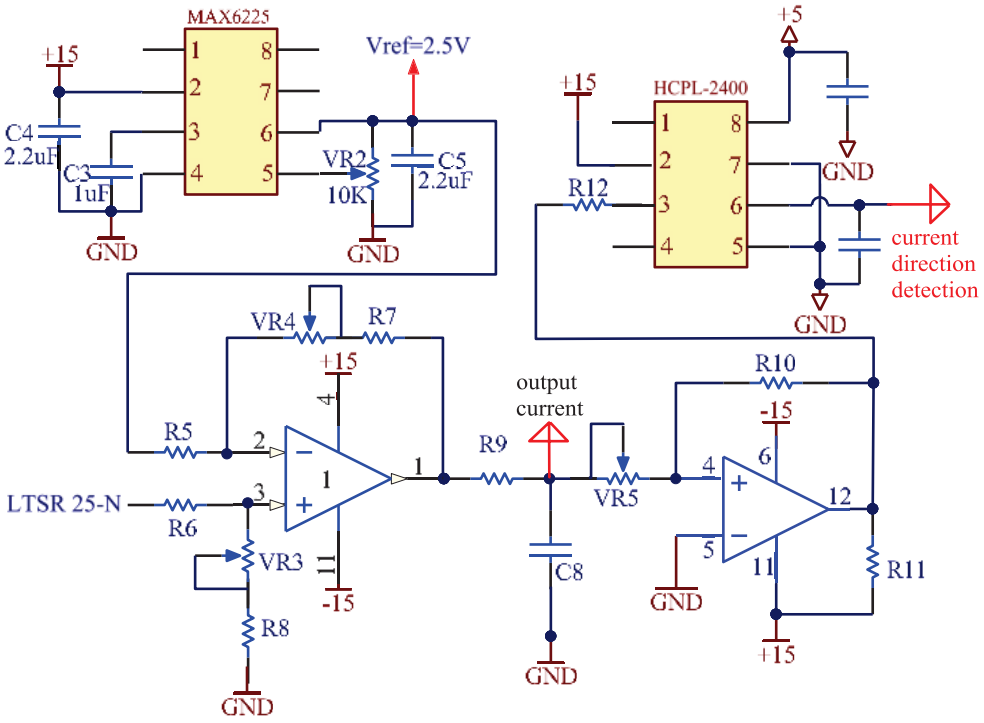


Figure 4.28: Current direction measurement circuit

has been designed and implemented in order to verify the operation of the modulation and control methods presented in the other chapters of the thesis. The prototype has been designed as identically as possible to the structures illustrated in the simulation models to assure a reliable comparison between the simulation and experimental results, although the simulation results are more close to the ideal results because of the non-ideal characteristics of the real components, circuits and instruments. As presented in the other chapters the experimental results are in agreement with the simulation results. The results verify that the designed DMC operates as expected and it can generate high-quality input and output currents and output voltage waveforms.

The design and construction of the DMC prototype used for micro-grid applications has been illustrated in detail. The power circuit is built up with eighteen IGBTs in common-collector configuration for bidirectional switches and also the in-

put filter capacitors are placed on the power boards. The current direction based four-step commutation is applied for safe operation of the bidirectional switches in FPGA, so 18 switching signals are generated by the VHDL programming in the FPGA to perform the four-quadrant operation effectively. Also, the control panel includes a DSP for performing the modulation and control calculations. The input filter is a simple low-pass LC filter with the damping resistors in parallel with the filter inductors that the procedure for designing an effective filter is illustrated to obtain sinusoidal input currents at the supply side. The voltage and current measurement and protection circuits and also the clamp circuit as an over-voltage protection circuit are explained in detail.

Chapter 5

STABILITY ANALYSIS OF THE MATRIX CONVERTER

5.1 Introduction

The demand for environment-friendly sustainable energy resources has increased significantly over the past decades due to the energy crisis and environmental pollution [99]. The major renewable energy sources, such as the solar and wind, however, are intermittent, resulting in poor power quality. This problem can be effectively solved by adopting the concept of smart microgrids, which integrate the renewable power generation, energy storage, and consumption closely through intelligent communication and control strategies. On the other hand, for the integration of multiple renewable power sources such as wind turbines into the microgrid, the ac-dc-ac power converters are commonly used [40,100]. These converters, though highly matured in technology, are bulky and less reliable, especially at relatively high capacity. On the other hand, matrix converters (MCs) can be used in the microgrids with common ac bus as an interface between the ac components and the grid or between the microgrid and utility grid, in order to eliminate the energy storage element, to increase the converter lifetime and to have a more compact converter [31, 55].

MCs are known as a direct-type power converter as the output phases can be connected to any input phase without energy storage elements. In all structures of

the MCs, installing an input filter is necessary to mitigate the switching harmonics and to improve the quality of the input currents [22, 27, 65]. In general, a simple low-pass LC filter is used at the input of MCs, as shown in Fig. 5.1. However, as stated in [59, 66, 101, 102], one of the instability potentials of the MCs is the input filter due to the negative input impedance of the converter at low frequencies. The instability caused by the input filter depends on the different items such as closed-loop control method, switching strategy and converter topology [72, 103, 104] as is explained in the next sections.

Some research works have been conducted on the stability problem of the MC to assure its normal stable operation for the maximum voltage gain [72, 103, 105–109]. One of the proposed approaches for increasing the output power limit is to add a parallel damping resistor to the input filter inductance. In this regard, analytical and numerical approaches have been used to determine the stability limit equations by linearizing the system state equations [72, 102]. The other popular method is to use a digital low-pass filter, to filter out the measured input voltage [103, 106, 107]. The filtered input voltages are used for calculating the duty cycles of the switching configurations required for the modulation process. The positive effect of filtering of input voltage vector angle on the stability region of the MC is presented in [107] and [108]. The stability analysis using a digital input PLL with magnitude filtering of the input voltage vector that is, in fact, a combination of angle filter with an infinite time constant and magnitude filter is studied in [108]. Another method to improve the MC stability is based on the virtual harmonic damper algorithm by constructing a correction term to increase the input impedance of the MC in motor and generator modes [109].

In addition, there are some practical issues that influence the stability of the converter. One of them is the digital implementation of the modulation strategy by discrete time operation of processors due to the limited precision of their arithmetic unit and the quantization of data and coefficients [108]. Furthermore, the digital implementation of the control algorithm by digital controllers introduces a switching

period delay that can affect the stability of the system as explained in [106] and [108]. In [106], the positive effects of the converter power losses on the system stability is illustrated by using a simplified model of the converter taking into account the converter power losses (switching and conduction losses). It is shown that the conduction power loss can increase the voltage transfer ratio limit.

The stability issue also depends on the input voltage measurement technique. If the voltage sensors are mounted before the input filter, across the three-phase input voltage source, the measured voltage is different from the actual voltage fed into the MC. This is because of the impedance of the filter inductor, especially in case of high currents. As the modulation strategy and calculation of the duty cycles are based on the voltage fed to the converter, it causes an error in the output results, and affects the output performance. To measure the actual voltage across the input of the MC, the voltage sensors should be installed after the input filter [103].

This chapter presents a detailed study of input filter interaction on performance and stability of the DMC. At first, the stability problem of the system is analysed by developing the mathematical model of the converter and the small-signal model. Then stabilisation of the system is studied with utilising the parallel damping resistor and also the digital input filter as two common solutions for the stability problem. The effect of each system parameter on the stability is presented in detail using the graphs plotted in MATLAB.

5.2 Stability Analysis of the MC

To investigate the stability of the converter, a DMC with a set of three-phase RL load as shown in Figure 5.1 is used. The duty cycles of the switching configurations are calculated by the instantaneous values of the voltages across the input filter capacitors. Figure 5.2 shows a single-phase model of the input low-pass LC filter, where R_s and L_s are the line resistance and inductance respectively. R_f is the internal resistance of the input filter inductor which is ideally considered as zero

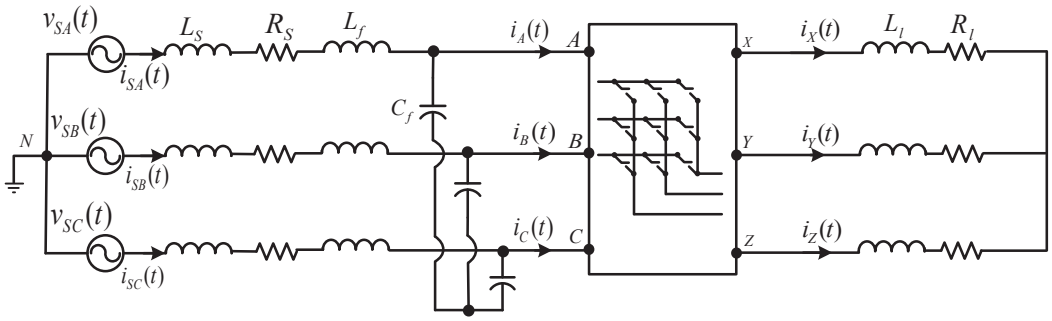


Figure 5.1: Schematic of the DMC with LC input filter and RL load

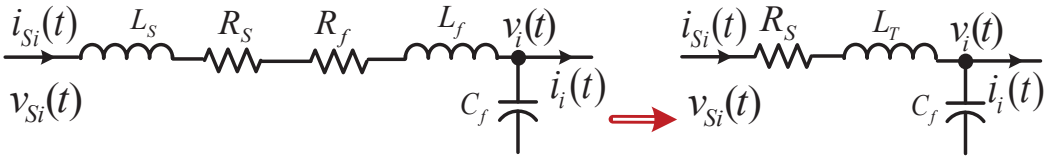


Figure 5.2: The single-phase model of the input low-pass LC filter

and C_f and L_f are the input filter capacitance and inductance respectively. The mathematical modelling of the MC is on the basis of the state-space averaging method which considers the average values of the voltages and currents as state variables over a switching interval while the effects of the switching harmonics are neglected.

5.2.1 Developing the mathematical model

Considering Figure 5.1, the input and output equations in the stationary reference frame using the space vector notation are:

$$\frac{d\vec{i}_{si}(t)}{dt} = -\frac{R_s}{L_T}\vec{i}_{si}(t) - \frac{1}{L_T}\vec{v}_i(t) + \frac{1}{L_T}\vec{v}_{si}(t) \tag{5.1}$$

$$\frac{d\vec{v}_i(t)}{dt} = \frac{1}{C_f}\vec{i}_{si}(t) - \frac{1}{C_f}\vec{i}_i(t) \tag{5.2}$$

$$\frac{d\vec{i}_o(t)}{dt} = -\frac{R_l}{L_l}\vec{i}_o(t) + \frac{1}{L_l}\vec{v}_o(t) \tag{5.3}$$

where $L_T = L_s + L_f$ and $R_f \simeq 0$ as shown in Figure 5.2. The variable, with a "$\vec{}$" over it, represents its corresponding space vector. There are two methods to find the input-output relationships:

1) Utilizing the equations of the input-output relationships of the voltages and currents of the matrix converter as illustrated in [110].

2) Considering the equality of the input and output powers by ignoring the switching loss as presented in [72].

According to the first suggested method, the equations representing the input-output relationships of the matrix converter are as following [110]:

$$\vec{v}_o(t) = \frac{3}{2}[\vec{v}_i(t)\vec{m}_i^*(t) + \vec{v}_i^*(t)\vec{m}_d(t)] \tag{5.4}$$

$$\vec{i}_i(t) = \frac{3}{2}[\vec{i}_o(t)\vec{m}_i(t) + \vec{i}_o^*(t)\vec{m}_d(t)] \tag{5.5}$$

where $\vec{m}_d(t)$ and $\vec{m}_i(t)$ are the duty-cycles space vectors defined by:

$$\vec{m}_d(t) = \frac{\vec{v}_{or}(t)\vec{\psi}(t)}{3[\vec{v}_i(t)\cdot\vec{\psi}(t)]} \tag{5.6}$$

$$\vec{m}_i(t) = \frac{\vec{v}_{or}^*(t)\vec{\psi}(t)}{3[\vec{v}_i(t)\cdot\vec{\psi}(t)]} \tag{5.7}$$

and the * sign shows the complex conjugate of the vector, and $\vec{v}_{or}(t)$ is the output reference voltage vector. $\vec{\psi}(t)$ is the modulation vector when the input current vector is modulated along the arbitrary space vector $\vec{\psi}(t)$ to have the desired angle between the input current and voltage space vectors as following [72] [89]:

$$\vec{i}_i(t)\cdot j\vec{\psi}(t) = 0 \tag{5.8}$$

Considering φ_i as the displacement angle between the input current and voltage

space vectors then:

$$\vec{\psi}(t) = \vec{v}_i(t)e^{-j\varphi_i} \tag{5.9}$$

For unity input power factor, φ_i is considered equal to zero, which means the input current is modulated along the input voltage space vector and so, $\vec{m}_d(t)$ and $\vec{m}_i(t)$ can be simplified as follows:

$$\varphi_i = 0 \qquad \Rightarrow \qquad \vec{\psi}(t) = \vec{v}_i(t) \tag{5.10}$$

$$\begin{aligned} \vec{m}_d(t) &= \frac{\vec{v}_{or}(t)\vec{v}_i(t)}{3[\vec{v}_i(t)\cdot\vec{v}_i(t)]} \\ &= \frac{\vec{v}_{or}(t)\vec{v}_i(t)}{3[\frac{1}{2}(\vec{v}_i(t)\vec{v}_i^*(t)+\vec{v}_i^*(t)\vec{v}_i(t))]} \end{aligned} \tag{5.11}$$

$$\vec{m}_d(t) = \frac{\vec{v}_{or}(t)}{3\vec{v}_i^*(t)} \tag{5.12}$$

$$\begin{aligned} \vec{m}_i(t) &= \frac{\vec{v}_{or}^*(t)\vec{v}_i(t)}{3[\vec{v}_i(t)\cdot\vec{v}_i(t)]} \\ &= \frac{\vec{v}_{or}^*(t)\vec{v}_i(t)}{3[\frac{1}{2}(\vec{v}_i(t)\vec{v}_i^*(t)+\vec{v}_i^*(t)\vec{v}_i(t))]} \end{aligned} \tag{5.13}$$

$$\vec{m}_i(t) = \frac{\vec{v}_{or}^*(t)}{3\vec{v}_i^*(t)} \tag{5.14}$$

The nonlinear equations for the input side in a synchronous reference frame rotating at the supply angular frequency ω_i for the MC shown in Figure 5.1 are as following:

$$\frac{d\vec{i}_{si}(t)}{dt} = -(\frac{R_s}{L_T} + j\omega_i)\vec{i}_{si}(t) - \frac{1}{L_T}\vec{v}_i(t) + \frac{1}{L_T}\vec{v}_{si}(t) \tag{5.15}$$

$$\frac{d\vec{v}_i(t)}{dt} = \frac{1}{C_f}\vec{i}_{si}(t) - j\omega_i\vec{v}_i(t) - \frac{1}{C_f}\vec{i}_i(t) \tag{5.16}$$

Also, the nonlinear equation for the output side in a synchronous reference frame rotating at the angular frequency ω_o is:

$$\frac{d\vec{i}_o(t)}{dt} = -(\frac{R_l}{L_l} + j\omega_o)\vec{i}_o(t) + \frac{1}{L_l}\vec{v}_o(t) \tag{5.17}$$

The resultant equations (5.12) and (5.14) - (5.17) are further used to drive the small-signal model of the MC based on the method presented in [72, 103] as illustrated in the next section.

5.2.2 Small-Signal Model

As the fundamental model of the system is normally nonlinear, a state-space model is developed based on linearising the model around the steady-state operating point. For this purpose, at first, the steady-state operating point should be defined. In steady state conditions, when the three-phase input supply voltage and output reference voltage are balanced and sinusoidal, and the space vector of the input voltage and output reference voltage are along the d-axis ($\alpha_i = \alpha_o = 0$), the space vectors of these three-phase voltages are as follows:

$$\begin{aligned} \vec{v}_i(t) &= \vec{V}_i e^{j\omega_i t} = V_{im} e^{j\alpha_i} e^{j\omega_i t}\Big|_{\alpha_i=0} = V_{im} e^{j\omega_i t} \\ \vec{v}_{or}(t) &= \vec{V}_{or} e^{j\omega_o t} = V_{or} e^{j\alpha_o} e^{j\omega_o t}\Big|_{\alpha_o=0} = V_{or} e^{j\omega_o t} \end{aligned} \tag{5.18}$$

So in steady-state operating point, all the variables expressed in their synchronous reference frames rotating at a specific angular speed can be assumed as constant values as following:

$$\vec{V}_i = V_{im} \tag{5.19}$$

$$\vec{V}_{or} = V_{or} \tag{5.20}$$

$$q = \frac{V_{or}}{V_{im}} \tag{5.21}$$

$$\vec{M}_d = \frac{q}{3} \tag{5.22}$$

$$\vec{M}_i = \frac{q}{3} \tag{5.23}$$

$$\vec{I}_o = \frac{qV_{im}}{\vec{Z}_l} \tag{5.24}$$

To find the small-signal model of the system, the deviation variable Δx which is the perturbation of the variable x from its steady-state operating point is added. The small-signal equations of the system linearised around the steady-state operating point then can be defined as follows:

$$\frac{d\Delta\vec{i}_{si}(t)}{dt} = -(\frac{R_s}{L_T} + j\omega_i)\Delta\vec{i}_{si}(t) - \frac{1}{L_T}\Delta\vec{v}_i(t) + \frac{1}{L_T}\Delta\vec{v}_{si}(t) \tag{5.25}$$

$$\frac{d\Delta\vec{v}_i(t)}{dt} = \frac{1}{C_f}\Delta\vec{i}_{si}(t) - j\omega_i\Delta\vec{v}_i(t) - \frac{1}{C_f}\Delta\vec{i}_i(t) \tag{5.26}$$

$$\frac{d\Delta\vec{i}_o(t)}{dt} = -(\frac{R_l}{L_l} + j\omega_o)\Delta\vec{i}_o(t) + \frac{1}{L_l}\Delta\vec{v}_o(t) \tag{5.27}$$

Assuming the balanced and sinusoidal three-phase output reference voltage, $\Delta\vec{v}_{or}(t) = 0$, (5.12), (5.14) and consequently (5.4) and (5.5) considering the small signal variations, can be written as follows:

$$\begin{aligned}\Delta\vec{m}_d(t) &= \frac{1}{3}\frac{\Delta\vec{v}_{or}(t)\vec{V}^*_{im} - \vec{V}_{or}\Delta\vec{v}^*_i(t)}{(\vec{V}^*_{im})^2} \\ &= -\frac{q}{3V_{im}}\Delta\vec{v}^*_i(t)\end{aligned} \tag{5.28}$$

$$\begin{aligned}\Delta\vec{m}_i(t) &= \frac{1}{3}\frac{\Delta\vec{v}^*_{or}(t)\vec{V}^*_{im} - \vec{V}^*_{or}\Delta\vec{v}^*_i(t)}{(\vec{V}^*_{im})^2} \\ &= -\frac{q}{3V_{im}}\Delta\vec{v}^*_i(t)\end{aligned} \tag{5.29}$$

$$\begin{aligned}\Delta\vec{v}_o(t) &= \frac{3}{2}\left[\Delta\vec{v}_i(t)\vec{M}^*_i + \Delta\vec{v}^*_i(t)\vec{M}_d + V_{im}\Delta\vec{m}^*_i(t) + V_{im}\Delta\vec{m}_d(t)\right] \\ &= \frac{q}{2}\Delta\vec{v}_i(t) + \frac{q}{2}\Delta\vec{v}^*_i(t) - \frac{q}{2}\Delta\vec{v}_i(t) - \frac{q}{2}\Delta\vec{v}^*_i(t) \\ &= 0\end{aligned} \tag{5.30}$$

$$\begin{aligned}\Delta\vec{i}_i(t) &= \frac{3}{2}\left[\Delta\vec{i}_o(t)\vec{M}_i + \Delta\vec{i}^*_o(t)\vec{M}_d + \vec{I}_o\Delta\vec{m}_i(t) + \vec{I}^*_o\Delta\vec{m}_d(t)\right] \\ &= \frac{q}{2}\Delta\vec{i}_o(t) + \frac{q}{2}\Delta\vec{i}^*_o(t) - \frac{q^2}{2\vec{Z}_l}\Delta\vec{v}^*_i(t) - \frac{q^2}{2\vec{Z}^*_l}\Delta\vec{v}^*_i(t) \\ &= \frac{q}{2}\Delta\vec{i}_o(t) + \frac{q}{2}\Delta\vec{i}^*_o(t) - \frac{q^2R_l}{|\vec{Z}_l|^2}\Delta\vec{v}^*_i(t)\end{aligned} \tag{5.31}$$

where $\vec{Z}_l = R_l + j\omega_o L_l$. For modelling and control design it is very convenient to transform three-phase variables into rotating d-q coordinates. Therefore the space vectors of the input voltage $\vec{v}_i(t)$ and output reference voltage $\vec{v}_{or}(t)$ are decomposed into d-q reference frame:

$$\begin{aligned} \vec{v}_i(t) &= [v_{i(d)}(t) + jv_{i(q)}(t)]e^{j\omega_i t} \\ \vec{v}_{or}(t) &= [v_{or(d)}(t) + jv_{or(q)}(t)]e^{j\omega_o t} \end{aligned} \tag{5.32}$$

Assuming the balanced and sinusoidal three-phase input supply voltage and output reference voltage, $\Delta\vec{v}_{si}(t) = 0$ and $\Delta\vec{v}_{or}(t) = 0$, (5.30) and (5.31) can be decomposed into d-q components as:

$$\begin{aligned} \Delta v_{o(d)}(t) &= 0 \\ \Delta v_{o(q)}(t) &= 0 \end{aligned} \tag{5.33}$$

$$\begin{aligned} \Delta i_{i(d)}(t) &= q\Delta i_{o(d)}(t) - \frac{q^2 R_l}{|\vec{Z}_l|^2}\Delta v_{i(d)}(t) \\ \Delta i_{i(q)}(t) &= \frac{q^2 R_l}{|\vec{Z}_l|^2}\Delta v_{i(q)}(t) \end{aligned} \tag{5.34}$$

Moreover, the final state equations can be obtained by decomposing (5.25)-(5.27) into d-q components, and considering (5.33) and (5.34) as following:

$$\begin{aligned} \frac{d\Delta i_{si(d)}(t)}{dt} &= -\frac{R_s}{L_T}\Delta i_{si(d)}(t) + \omega_i \Delta i_{si(q)}(t) - \frac{1}{L_T}\Delta v_{i(d)}(t) \\ \frac{d\Delta i_{si(q)}(t)}{dt} &= -\omega_i \Delta i_{si(d)}(t) - \frac{R_s}{L_T}\Delta i_{si(q)}(t) - \frac{1}{L_T}\Delta v_{i(q)}(t) \end{aligned} \tag{5.35}$$

$$\begin{aligned} \frac{d\Delta v_{i(d)}(t)}{dt} &= \frac{1}{C_f}\Delta i_{si(d)}(t) + \frac{q^2 R_l}{C_f|\vec{Z}_l|^2}\Delta v_{i(d)}(t) + \omega_i \Delta v_{i(q)}(t) - \frac{q}{C_f}\Delta i_{o(d)}(t) \\ \frac{d\Delta v_{i(q)}(t)}{dt} &= \frac{1}{C_f}\Delta i_{si(q)}(t) - \omega_i \Delta v_{i(d)}(t) - \frac{q^2 R_l}{C_f|\vec{Z}_l|^2}\Delta v_{i(q)}(t) \end{aligned} \tag{5.36}$$

$$\begin{aligned} \frac{d\Delta i_{o(d)}(t)}{dt} &= -\frac{R_l}{L_l}\Delta i_{o(d)}(t) + \omega_o \Delta i_{o(q)}(t) \\ \frac{d\Delta i_{o(q)}(t)}{dt} &= -\omega_o \Delta i_{o(d)}(t) - \frac{R_l}{L_l}\Delta i_{o(q)}(t) \end{aligned} \tag{5.37}$$

Table 5.1: System Parameters for Numerical Analysis

Input parameters	Input filter parameters	output parameters
$V_{i,rms} = 240V$	$C_f = 6\mu F$	$R_l = 10\Omega$
$L_s = 0.4mH$	$L_f = 0.6mH$	$L_l = 6mH$
$R_s = 0.5\Omega$	$f_i = 50Hz$	$f_o = 70Hz$

Consequently, the state equations of the linearised system around the steady-state operating point are obtained using (5.35)-(5.37) as:

$$\frac{d\Delta X}{dt} = A\Delta X \tag{5.38}$$

where ΔX and A are defined as:

$$\Delta X = \begin{bmatrix} \Delta i_{si(d)}(t) & \Delta i_{si(q)}(t) & \Delta v_{i(d)}(t) & \Delta v_{i(q)}(t) & \Delta i_{o(d)}(t) & \Delta i_{o(q)}(t) \end{bmatrix}^T \tag{5.39}$$

$$A = \begin{bmatrix} -\frac{R_s}{L_T} & \omega_i & \frac{-1}{L_T} & 0 & 0 & 0 \\ -\omega_i & -\frac{R_s}{L_T} & 0 & \frac{-1}{L_T} & 0 & 0 \\ \frac{1}{C_f} & 0 & k_1 & \omega_i & -\frac{q}{C_f} & 0 \\ 0 & \frac{1}{C_f} & -\omega_i & -k_1 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{R_l}{L_l} & \omega_o \\ 0 & 0 & 0 & 0 & -\omega_o & -\frac{R_l}{L_l} \end{bmatrix} \tag{5.40}$$

$$k_1 = \frac{q^2 R_l}{C_f |\vec{Z}_l|^2}$$

In the following section using matrix A, a numerical approach is illustrated for stability analysis of the system.

5.2.3 Numerical approach for stability analysis

The eigenvalues of matrix A are numerically analysed to find the stability limit of the system. For this purpose, the dominant eigenvalue should be find which is the closest eigenvalue to the imaginary axis. This evaluation is carried out for different

amounts of voltage transfer ratio q, to find the limit value of q which causes the system remains stable. The positive real part of the dominant eigenvalue means that the system is unstable. For the system parameters defined in Table 5.1, Figures 5.3 and 5.4 illustrate the effects of some parameters of the system on the stability limit. According to the figures the stability limit depends on the different parameters of the system and to show the effect of each parameter, it is changed in a particular range while the other parameters are kept constant as illustrated in Table 5.1.

Figure 5.3a shows the positive effect of increasing the filter capacitance C_f while Figure 5.3b illustrates the positive effect of decreasing the filter inductance. It means that the system remains stable for larger voltage gains by increasing C_f or decreasing L_f although the capacitance raise is more effective. As demonstrated in Figure 5.4a, higher input frequency f_i permits larger voltage gain q in the stability region. The output frequency f_o has no noticeable effect on that. Also rising the line resistance R_s increases the stability limit as shown in Figure 5.4b, but obviously adding a resistance in series with R_s causes efficiency reduction and loss increment. So, instead of increasing R_s, a parallel damping resistor is added to the filter inductance that will be explained later. As explained in the input filter design section, filter parameters should be selected in a way that cause minimum displacement angle between voltage and current of the input source. It is not possible to change these parameters in a wide range, and a suitable method should be carried out to increase the stability limit.

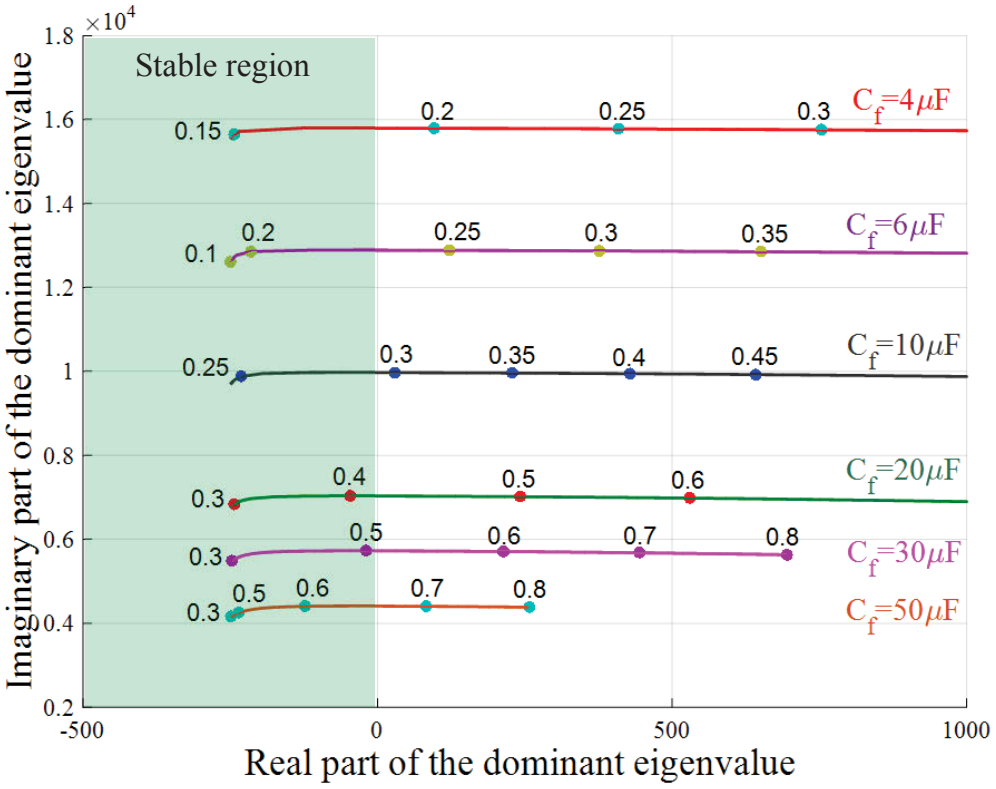
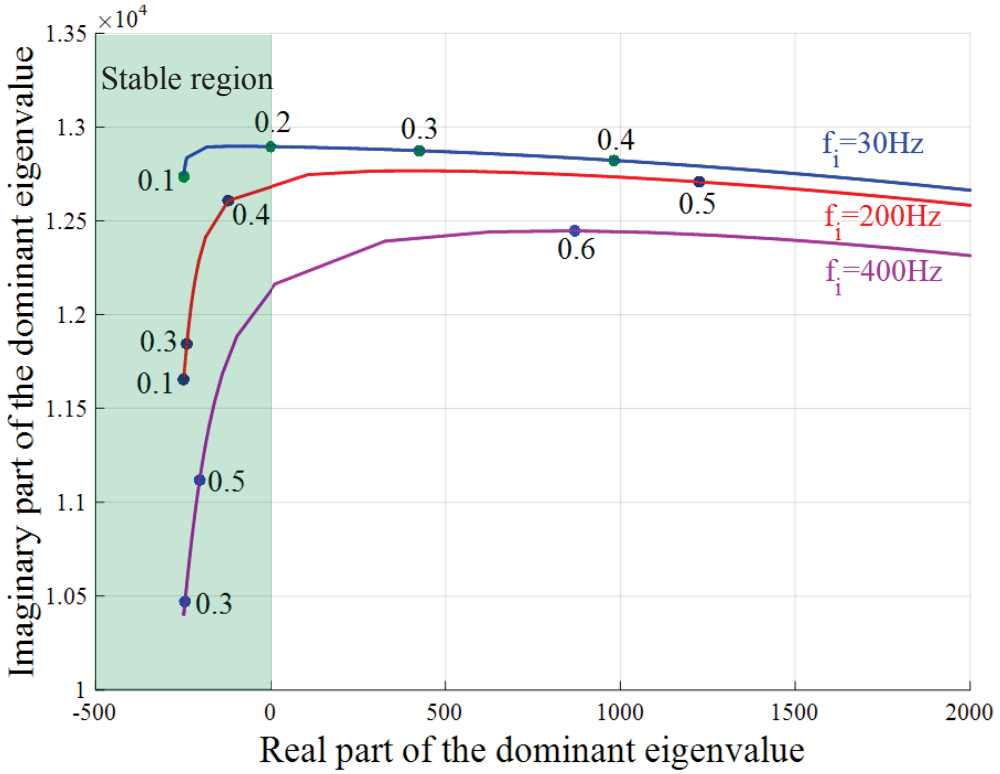
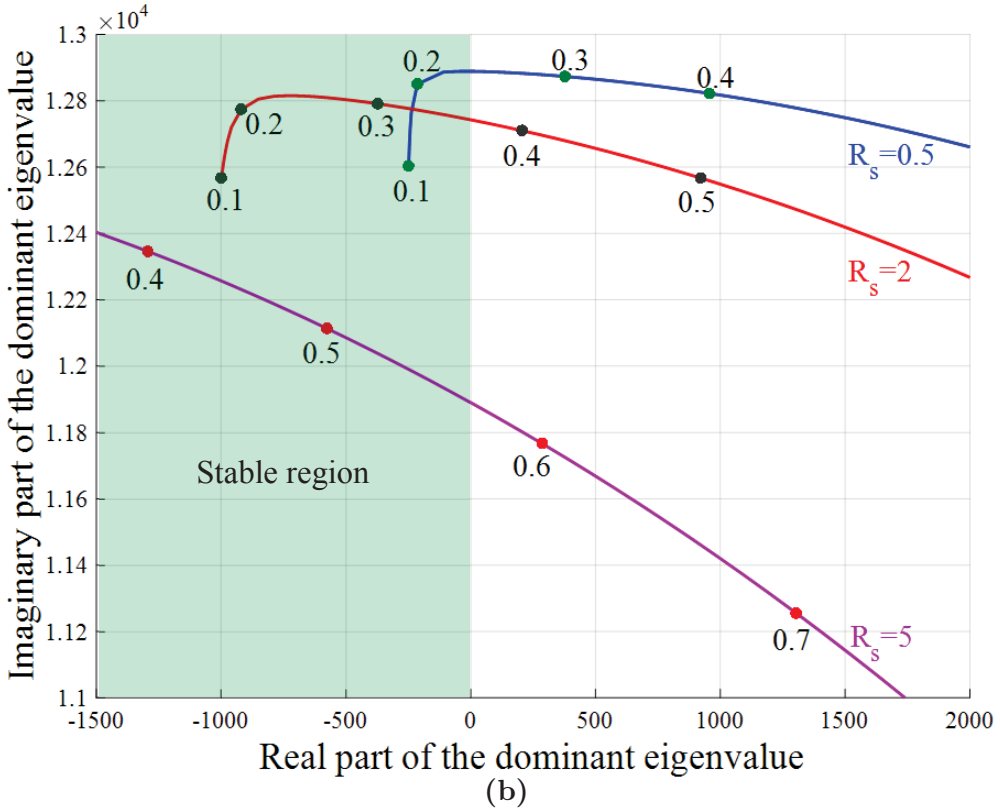


Figure 5.3: Position of the dominant eigenvalue of the state matrix A in the complex plane as a function of the voltage gain q, where a) For different values of C_f, and b) For different values of L_T



(a)



(b)

Figure 5.4: Position of the dominant eigenvalue of the state matrix A in the complex plane as a function of the voltage gain q, where a) For different values of f_i, and b) For different values of R_s

5.2.4 Stability analysis for maximum output power

Instead of voltage gain q, it is possible to evaluate the converter stability according to the maximum output power [72]. As the matrix converter has no internal energy storage, by ignoring the switching loss, the instantaneous input and output powers are equal:

$$p_i(t) = \frac{3}{2}\vec{v}_i(t) \cdot \vec{i}_i(t) = \frac{3}{4}[\vec{v}_i^*(t)\vec{i}_i(t) + \vec{v}_i(t)\vec{i}_i^*(t)] = p_o(t) \tag{5.41}$$

In order to have the desired angle φ_i between the input current and voltage, the input current vector is modulated along the arbitrary space vector $\vec{\psi}(t) = \vec{v}_i(t)e^{-j\varphi_i}$ so that [72] [89]:

$$\begin{aligned}
&\vec{i}_i(t) \cdot j\vec{\psi}(t) = 0 \\
&\vec{\psi}(t) = \vec{v}_i(t)e^{-j\varphi_i} \\
&\vec{i}_i(t) \cdot j\vec{v}_i(t)e^{-j\varphi_i} = 0 \\
&\frac{1}{2}\left[\vec{i}_i^*(t)\left(j\vec{v}_i(t)e^{-j\varphi_i}\right) + \vec{i}_i(t)\left(j\vec{v}_i(t)e^{-j\varphi_i}\right)^*\right] = 0 \\
&j\vec{i}_i^*(t)\vec{v}_i(t)e^{-j\varphi_i} = -\vec{i}_i(t)\left(-j\vec{v}_i^*(t)e^{j\varphi_i}\right) \\
&\vec{i}_i^*(t)\vec{v}_i(t) = \frac{\vec{i}_i(t)\vec{v}_i^*(t)e^{j\varphi_i}}{e^{-j\varphi_i}}
\end{aligned} \tag{5.42}$$

Thus, the relationship between the input current and output power using (5.41) and (5.42) is as following:

$$\begin{aligned}
p_o(t) =& \frac{3}{4}\left[\vec{v}_i^*(t)\vec{i}_i(t) + \frac{\vec{i}_i(t)\vec{v}_i^*(t)e^{j\varphi_i}}{e^{-j\varphi_i}}\right] \\
=& \frac{3}{4}\vec{v}_i^*(t)\vec{i}_i(t)\left[\frac{e^{-j\varphi_i} + e^{j\varphi_i}}{e^{-j\varphi_i}}\right] \\
=& \frac{3}{4}\vec{v}_i^*(t)\vec{i}_i(t)\left[\frac{2\cos(\varphi_i)}{e^{-j\varphi_i}}\right] \\
\vec{i}_i(t) =& \frac{2}{3}\frac{p_o(t)e^{-j\varphi_i}}{\vec{v}_i^*(t)\cos(\varphi_i)}
\end{aligned} \tag{5.43}$$

Therefore, (5.16) can be rewritten as:

$$\frac{d\vec{v}_i(t)}{dt} = \frac{1}{C_f}\vec{i}_{si}(t) - j\omega_i\vec{v}_i(t) - \frac{2p_o(t)e^{-j\varphi_i}}{3C_f\vec{v}_i^*(t)\cos(\varphi_i)} \tag{5.44}$$

In steady state conditions which explained before, as $\frac{d\vec{v}_i(t)}{dt} = \frac{d\vec{i}_{si}(t)}{dt} = 0$, by substitution of the variable parameters with the constant values, the maximum exchangeable power between the source and load in case of $\varphi_i = 0$ is obtained as [72]:

$$P_{s1}, P_{s2} = \frac{3V_s^2.\left[-R_s \mp \sqrt{R_s^2 + eq1}\right]}{4eq_1} \tag{5.45}$$

where $eq_1 = \omega_i^2\left[L_T\left(1 - \omega_i^2 L_T C_f\right) - R_s^2 C_f\right]^2$ and $P_{s1} < P_o < P_{s2}$. P_{s1} is the maximum power in the regenerative mode and P_{s2} is for the motor mode. To find the maximum output power which keeps the system stable, the state equations of the small-signal model of the system are needed. So, (5.15) and (5.44) are linearised around the steady state operating point which mentioned before. The small-signal equation $\vec{i}_i(t)$ in (5.43) and as a result, the small-signal equation of (5.44) is as following:

$$\Delta\vec{i}_i(t) = \frac{2p_o(t)e^{-j\varphi_i}}{3\cos(\varphi_i)}\frac{-\Delta\vec{v}_i^*(t)}{V_{im}^2} \tag{5.46}$$

$$\frac{d\Delta\vec{v}_i(t)}{dt} = \frac{1}{C_f}\Delta\vec{i}_{si}(t) - j\omega_i\Delta\vec{v}_i(t) - \frac{2p_o(t)e^{-j\varphi_i}}{3C_f\cos(\varphi_i)}\frac{-\Delta\vec{v}_i^*(t)}{V_{im}^2} \tag{5.47}$$

The d-q decomposition of (5.47) is:

$$\begin{aligned}
\frac{d\Delta v_{i(d)}(t)}{dt} &= \frac{1}{C_f}\Delta i_{si(d)}(t) + \omega_i\Delta v_{i(q)}(t) \\
&\quad + \frac{2p_o(t)}{3C_f V_{im}^2\cos\varphi_i}\left(\cos\varphi_i\Delta v_{i(d)}(t) - \sin\varphi_i\Delta v_{i(q)}(t)\right) \\
\frac{d\Delta v_{i(q)}(t)}{dt} &= \frac{1}{C_f}\Delta i_{si(q)}(t) - \omega_i\Delta v_{i(d)}(t) \\
&\quad - \frac{2p_o(t)}{3C_f V_{im}^2\cos\varphi_i}\left(\cos\varphi_i\Delta v_{i(q)}(t) + \sin\varphi_i\Delta v_{i(d)}(t)\right)
\end{aligned} \tag{5.48}$$

Using (5.35), (5.48) and (5.37) the state equation of the small-signal model of the

system is as following:

$$\frac{d\Delta X}{dt} = A_1 \Delta X \tag{5.49}$$

where ΔX and A_1 are defined as:

$$\Delta X = \begin{bmatrix} \Delta i_{si(d)}(t) & \Delta i_{si(q)}(t) & \Delta v_{i(d)}(t) & \Delta v_{i(q)}(t) & \Delta i_{o(d)}(t) & \Delta i_{o(q)}(t) \end{bmatrix}^T \tag{5.50}$$

$$A_1 = \begin{bmatrix} -\frac{R_s}{L_T} & \omega_i & -\frac{1}{L_T} & 0 & 0 & 0 \\ -\omega_i & -\frac{R_s}{L_T} & 0 & -\frac{1}{L_T} & 0 & 0 \\ \frac{1}{C_f} & 0 & -K_p & K_p \tan(\varphi_i) + \omega_i & 0 & 0 \\ 0 & \frac{1}{C_f} & K_p \tan(\varphi_i) - \omega_i & K_p & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{R_l}{L_l} & \omega_o \\ 0 & 0 & 0 & 0 & -\omega_o & -\frac{R_l}{L_l} \end{bmatrix} \tag{5.51}$$

$$K_p = -\frac{2p_o}{3C_f V_{im}^2}$$

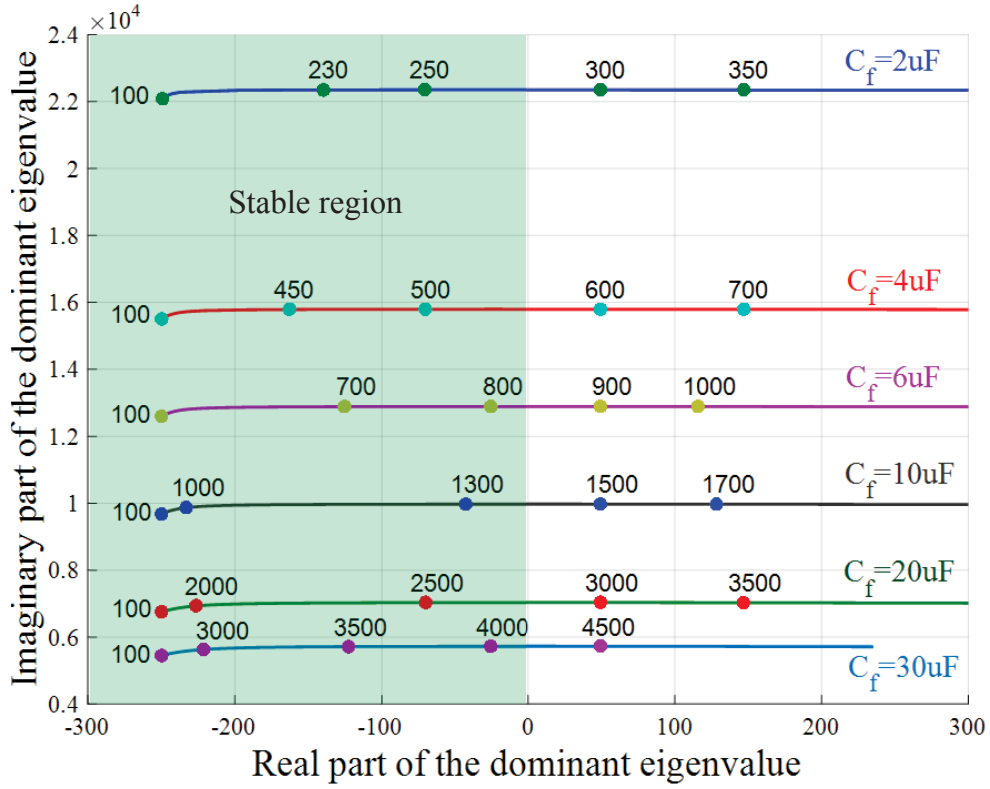
By analysing the eigenvalues of matrix A_1, the stability condition is obtained as following [72]:

$$\begin{aligned} p_1 &= \frac{3}{2} V_{im}^2 C_f |\cos\varphi_i| \sqrt{\frac{R_s^2}{L_T^2} + 4\omega_i^2} \\ -p_1 &< p_o < p_1 \end{aligned} \tag{5.52}$$

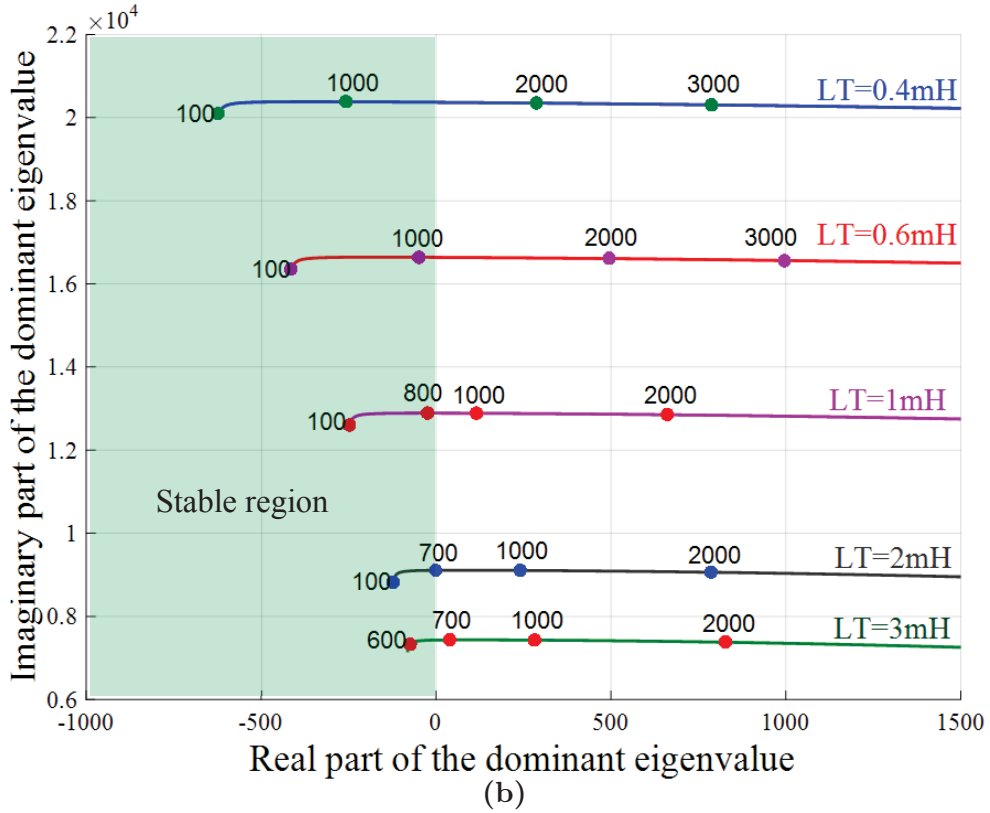
which p_1 is the maximum output power while the converter is still stable. For example, with the system defined in Table 5.1, the maximum output power equals to 832.53W that is in agreement with the results illustrated in Figure 5.5a with $C_f = 6\mu F$ and Figure 5.5b with $L_T = 1mH$.

Equation (5.52) shows that the output power of the MC is a function of the system parameters. In the same conditions, the maximum output power is obtained at unity input power factor, and this is not dependent on the switching frequency. To increase the output power limit, the filter capacitance should be increased while the filter inductance should be decreased as far as it does not lead to a reduction of the input power factor. The switching behaviour has not been considered in the

state equations, so it is not possible to analyse the effect of the switching harmonics on the stability behaviour of the system. Also, the bigger line resistance R_s has a positive effect on increasing the output power limit. The best method for increasing the damping factor of the filter is adding a damping resistance in parallel with the inductances of the input filter. A series damping resistance decreases the efficiency of the converter, but a parallel damping resistance only allows the high-frequency harmonics of the input current to pass through. Figures 5.5 and 5.6 show the effect of the mentioned parameters on the maximum output power limit of a stable system. As can be observed, larger capacitance and smaller inductance of the input filter leads to a stable system with higher output power. Same results can be obtained by increasing the input frequency f_i or line resistance R_s according to Figure 5.6, although these parameters are not always under control.

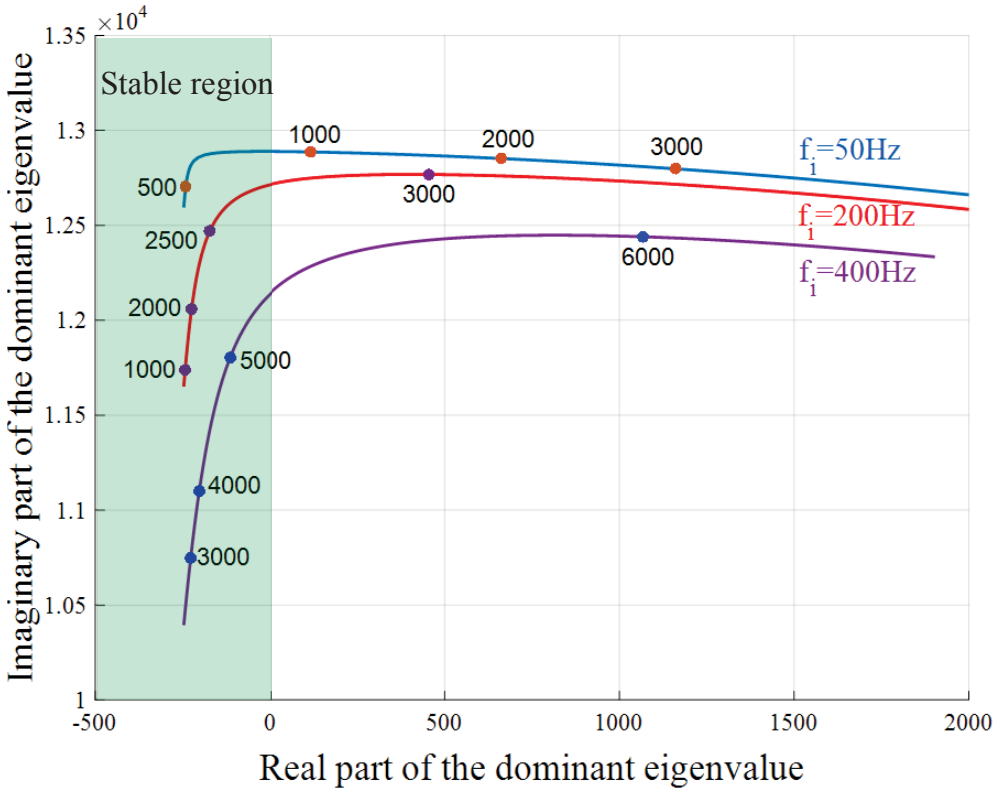


(a)

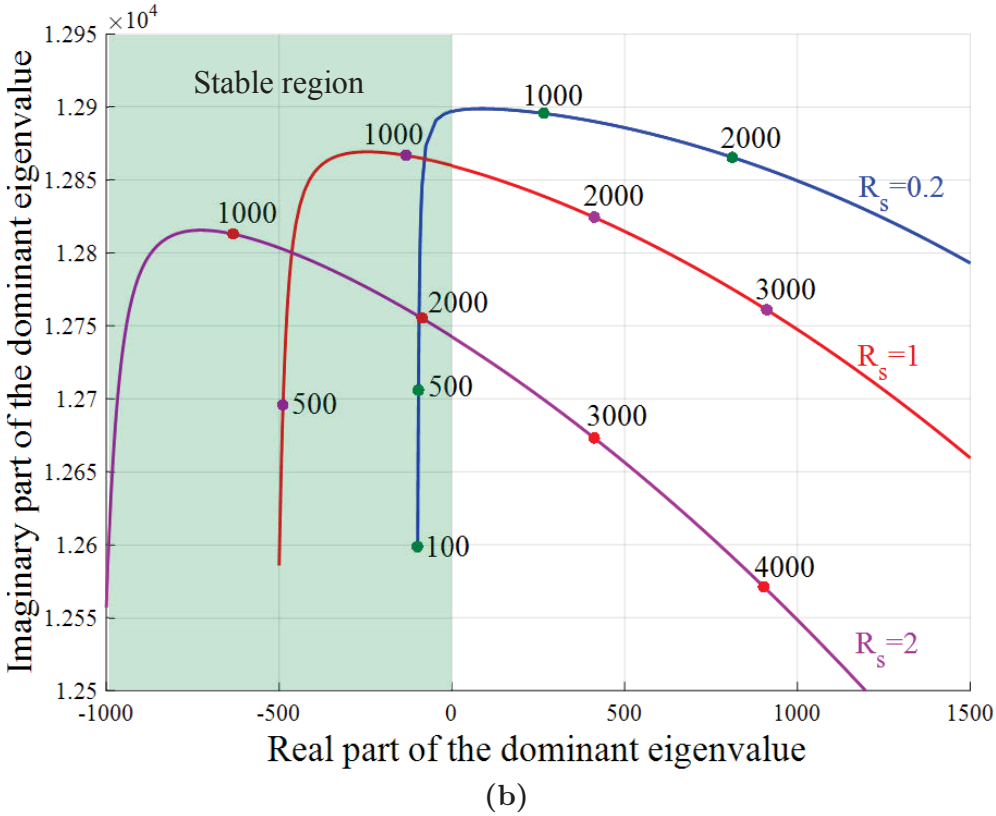


(b)

Figure 5.5: Position of the dominant eigenvalue of the state matrix A in the complex plane as a function of the output power p_o, where a) For different values of C_f, and b) For different values of L_T



(a)



(b)

Figure 5.6: Position of the dominant eigenvalue of the state matrix A in the complex plane as a function of the output power p_o, where a) For different values of f_i, and b) For different values of R_s

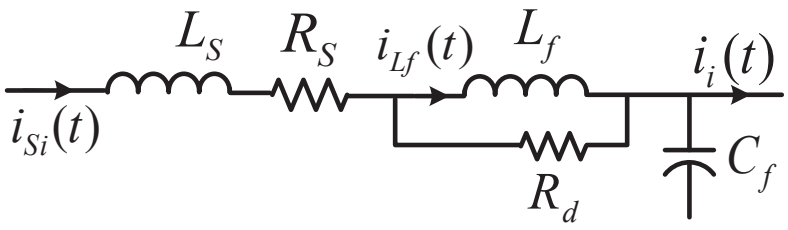


Figure 5.7: Schematic of the low-pass LC filter with the parallel damping resistor

5.3 Stability Analysis of the MC With Damping Resistor

As explained before, one of the effective methods for increasing the output power limit of a stable MC is adding the parallel damping resistors to the input filter inductances as shown in Figure 5.7 [72] [102]. As the resistance of the filter inductor is very small, it can be neglected ($R_f = 0$). The stability analysis using the small-signal model of the system for linearising the state equations around the steady-state operating point is carried in the same way as without damping resistor method.

The nonlinear equations of the input of the MC with a parallel damping resistor R_d, in a synchronous reference frame rotating at the angular frequency ω_i, can be written as:

$$\frac{d\vec{i}_{si}(t)}{dt} = -(\frac{R_s + R_d}{L_s} + j\omega_i)\vec{i}_{si}(t) + \frac{1}{L_s}\vec{v}_{si}(t) - \frac{1}{L_s}\vec{v}_i(t) + \frac{R_d}{L_s}\vec{i}_{Lf}(t) \tag{5.53}$$

$$\frac{d\vec{i}_{Lf}(t)}{dt} = \frac{R_d}{L_f}\vec{i}_{si}(t) - \left(\frac{R_d}{L_f} + j\omega_i\right)\vec{i}_{Lf}(t) \tag{5.54}$$

The output equation is as mentioned in (5.17). As the system is nonlinear, in order to study the stability of the converter, the small-signal model of the system is derived for linearising the system model around the steady-state operating point. All the variables in steady state operating point are defined as mentioned before in (5.19)-(5.24). The small-signal equations of the input can be defined as:

$$\frac{d\Delta\vec{i}_{si}(t)}{dt} = -(\frac{R_s + R_d}{L_s} + j\omega_i)\Delta\vec{i}_{si}(t) + \frac{1}{L_s}\Delta\vec{v}_{si}(t) - \frac{1}{L_s}\Delta\vec{v}_i(t) + \frac{R_d}{L_s}\Delta\vec{i}_{Lf}(t) \quad (5.55)$$

$$\frac{d\Delta\vec{i}_{Lf}(t)}{dt} = \frac{R_d}{L_f}\Delta\vec{i}_{si}(t) - \left(\frac{R_d}{L_f} + j\omega_i\right)\Delta\vec{i}_{Lf}(t) \quad (5.56)$$

After decomposing into d-q components, the equations in a synchronous reference frame rotating at the supply angular frequency ω_i are as following:

$$\begin{aligned}
&\frac{d\Delta i_{si(d)}(t)}{dt} = \\
&\frac{1}{L_s}\Delta v_{si(d)}(t) - \frac{R_s + R_d}{L_s}\Delta i_{si(d)}(t) + \omega_i\Delta i_{si(q)}(t) - \frac{1}{L_s}\Delta v_{i(d)}(t) + \frac{R_d}{L_s}\Delta i_{Lf(d)}(t) \\
&\frac{d\Delta i_{si(q)}(t)}{dt} = \\
&\frac{1}{L_s}\Delta v_{si(q)}(t) - \frac{R_s + R_d}{L_s}\Delta i_{si(q)}(t) - \omega_i\Delta i_{si(d)}(t) - \frac{1}{L_s}\Delta v_{i(q)}(t) + \frac{R_d}{L_s}\Delta i_{Lf(q)}(t)
\end{aligned} \quad (5.57)$$

$$\begin{aligned}
\frac{d\Delta i_{Lf(d)}(t)}{dt} &= \frac{R_d}{L_f}\Delta i_{si(d)}(t) - \frac{R_d}{L_f}\Delta i_{Lf(d)}(t) + \omega_i\Delta i_{Lf(q)}(t) \\
\frac{d\Delta i_{Lf(q)}(t)}{dt} &= \frac{R_d}{L_f}\Delta i_{si(q)}(t) - \frac{R_d}{L_f}\Delta i_{Lf(q)}(t) - \omega_i\Delta i_{Lf(d)}(t)
\end{aligned} \quad (5.58)$$

As $\Delta\vec{v}_{si}(t) = 0$, the d-q components of the $\Delta v_i(t)$ are as (5.48), and the state equations for the output side are obtained as (5.37), so the state equation of the small-signal model of the system is as following [72]:

$$\frac{d\Delta X_d}{dt} = A_{d1}\Delta X_d \quad (5.59)$$

$$X_d = \begin{bmatrix} i_{si(d)}(t) & i_{si(q)}(t) & v_{i(d)}(t) & v_{i(q)}(t) & i_{Lf(d)}(t) & i_{Lf(q)}(t) & i_{o(d)}(t) & i_{o(q)}(t) \end{bmatrix}^T \quad (5.60)$$

$$A_{d1} = \begin{bmatrix} -\frac{R_s+R_d}{L_s} & \omega_i & \frac{-1}{L_s} & 0 & \frac{R_d}{L_s} & 0 & 0 & 0 \\ -\omega_i & -\frac{R_s+R_d}{L_s} & 0 & \frac{-1}{L_s} & 0 & \frac{R_d}{L_s} & 0 & 0 \\ \frac{1}{C_f} & 0 & -K_p & K_p \tan\varphi_i + \omega_i & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_f} & K_p \tan\varphi_i - \omega_i & K_p & 0 & 0 & 0 & 0 \\ \frac{R_d}{L_f} & 0 & 0 & 0 & -\frac{R_d}{L_f} & \omega_i & 0 & 0 \\ 0 & \frac{R_d}{L_f} & 0 & 0 & -\omega_i & -\frac{R_d}{L_f} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{R_l}{L_l} & \omega_o \\ 0 & 0 & 0 & 0 & 0 & 0 & -\omega_o & -\frac{R_l}{L_l} \end{bmatrix}$$

$$K_p = -\frac{2po}{3C_f V_{im}^2} \tag{5.61}$$

Also, it is possible to do the stability analysis for maximum voltage gain q. For this purpose instead of the (5.48), (5.36) should be considered. As a result, the state equations are:

$$\frac{d\Delta X}{dt} = A_{d2}\Delta X_d \tag{5.62}$$

$$A_{d2} = \begin{bmatrix} -\frac{R_s+R_d}{L_s} & \omega_i & \frac{-1}{L_s} & 0 & \frac{R_d}{L_s} & 0 & 0 & 0 \\ -\omega_i & -\frac{R_s+R_d}{L_s} & 0 & \frac{-1}{L_s} & 0 & \frac{R_d}{L_s} & 0 & 0 \\ \frac{1}{C_f} & 0 & K_1 & \omega_i & 0 & 0 & -\frac{q}{C_f} & 0 \\ 0 & \frac{1}{C_f} & -\omega_i & -K_1 & 0 & 0 & 0 & 0 \\ \frac{R_d}{L_f} & 0 & 0 & 0 & -\frac{R_d}{L_f} & \omega_i & 0 & 0 \\ 0 & \frac{R_d}{L_f} & 0 & 0 & -\omega_i & -\frac{R_d}{L_f} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{R_l}{L_l} & \omega_o \\ 0 & 0 & 0 & 0 & 0 & 0 & -\omega_o & -\frac{R_l}{L_l} \end{bmatrix}$$

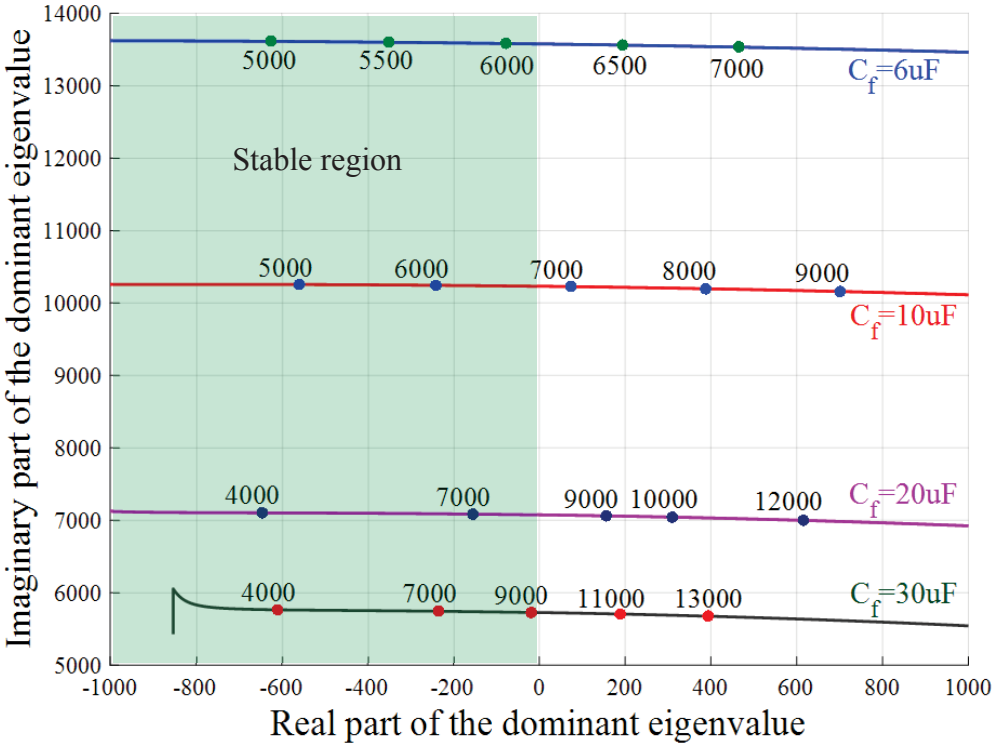
$$K_1 = \frac{q^2 R_l}{C_f |\vec{Z}_l|^2} \tag{5.63}$$

The resultant equations (5.59)-(5.63) can be further used for stability analysis of the system in a numerical approach as will be discussed in the next section.

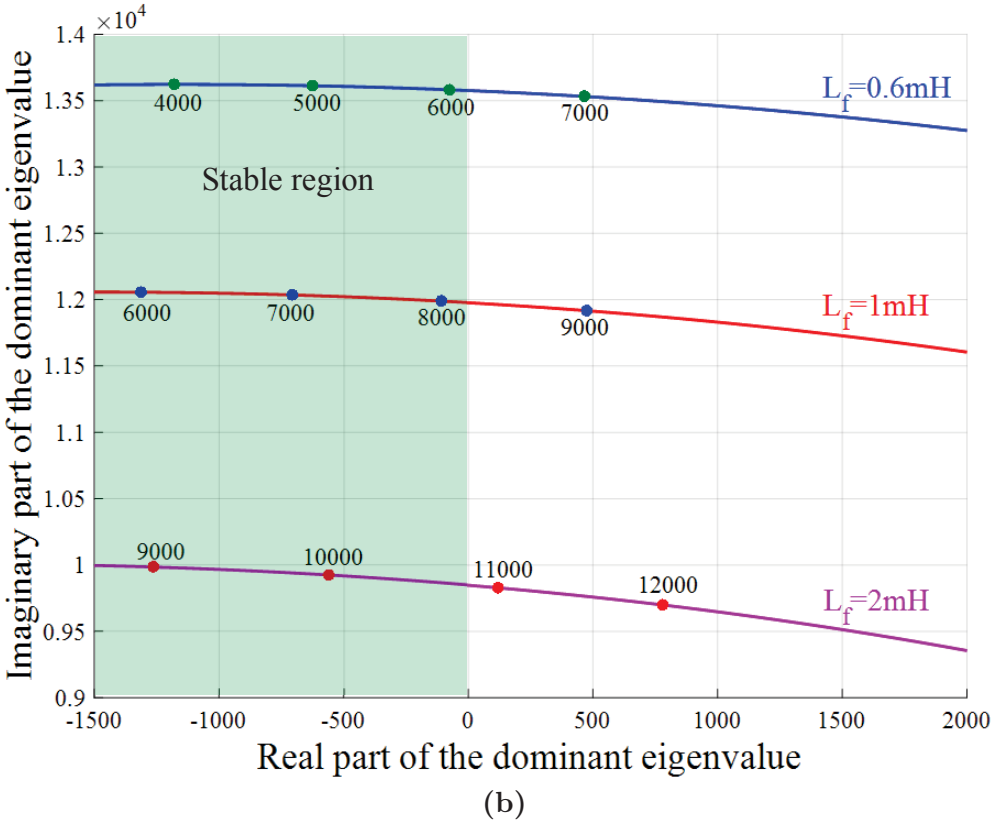
5.3.1 Numerical approach for stability analysis of the MC with the damping resistor

The stability of the system can be developed using a numerical approach. Again the position of the real part of the dominant eigenvalues of matrix A_{d1} and A_{d2} are considered as the criterion for stability. As far as the real part of the dominant eigenvalue is negative the system is stable, and when it closes to the imaginary axis the system starts to oscillate, and if it gets positive, the system will get unstable.

As shown in Figures 5.8-5.11, input filter parameters affect the position of the dominant eigenvalue and as a result, affect the system stability. The system parameters in this analysis, are the same parameters in Table 5.1. As illustrated in Figures 5.8 and 5.11 increasing the filter capacitance and inductance raises the limits of output power and voltage gain while without damping resistor, L_f has the opposite effect. Figures 5.9 and 5.10 illustrate the effect of damping resistor R_d on the limit of the output power and voltage gain. As can be seen, small values of R_d, result in the higher output power and voltage gain limits although, there is a limitation for reducing the damping resistor and an optimal value of R_d can be found for each case of system parameters. For the mentioned system parameters when $R_d = 4\Omega$ the system with voltage gain 0.7 and output power 8 kW is stable but when $R_d = 3\Omega$ it is not stable anymore for these values. Furthermore, it should be considered that smaller parallel damping resistance allows the high-frequency harmonics of the input current to pass through more. The effects of the other system parameters like input and output frequencies and line resistance are similar to the results mentioned in the previous section.



(a)



(b)

Figure 5.8: Position of the dominant eigenvalue of the state matrix A_{d1} in the complex plane as a function of the output power *po* with $R_d = 10\Omega$, where a) For different values of C_f, and b) For different values of L_f

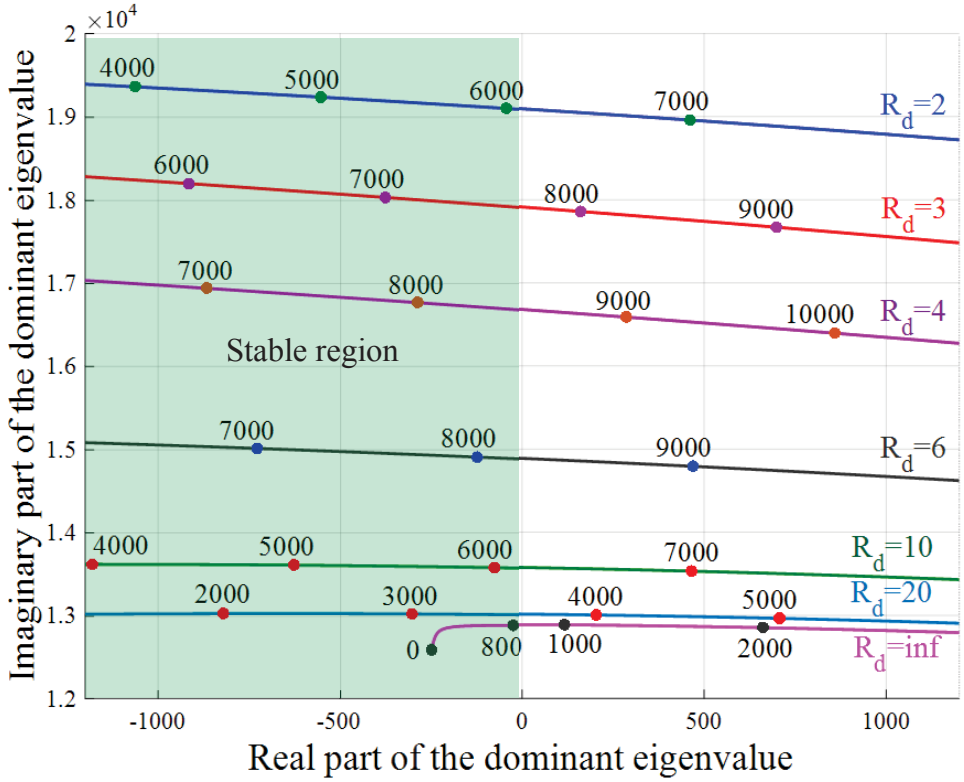


Figure 5.9: Position of the dominant eigenvalue of the state matrix A_{d1} in the complex plane as a function of the output power p_o for different values of R_d

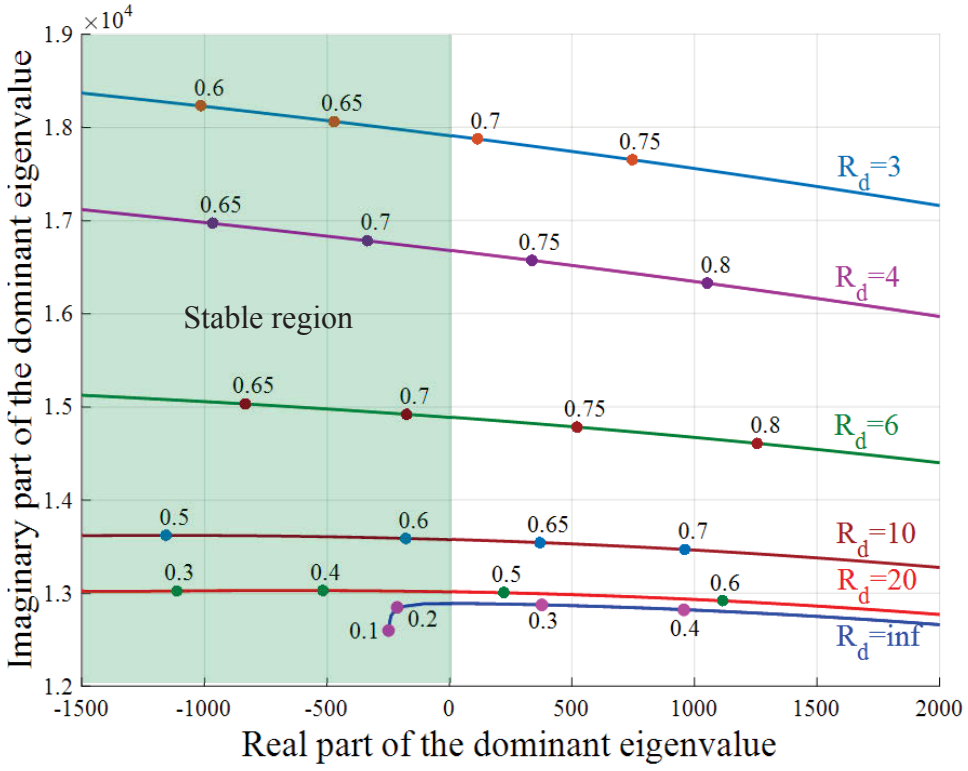
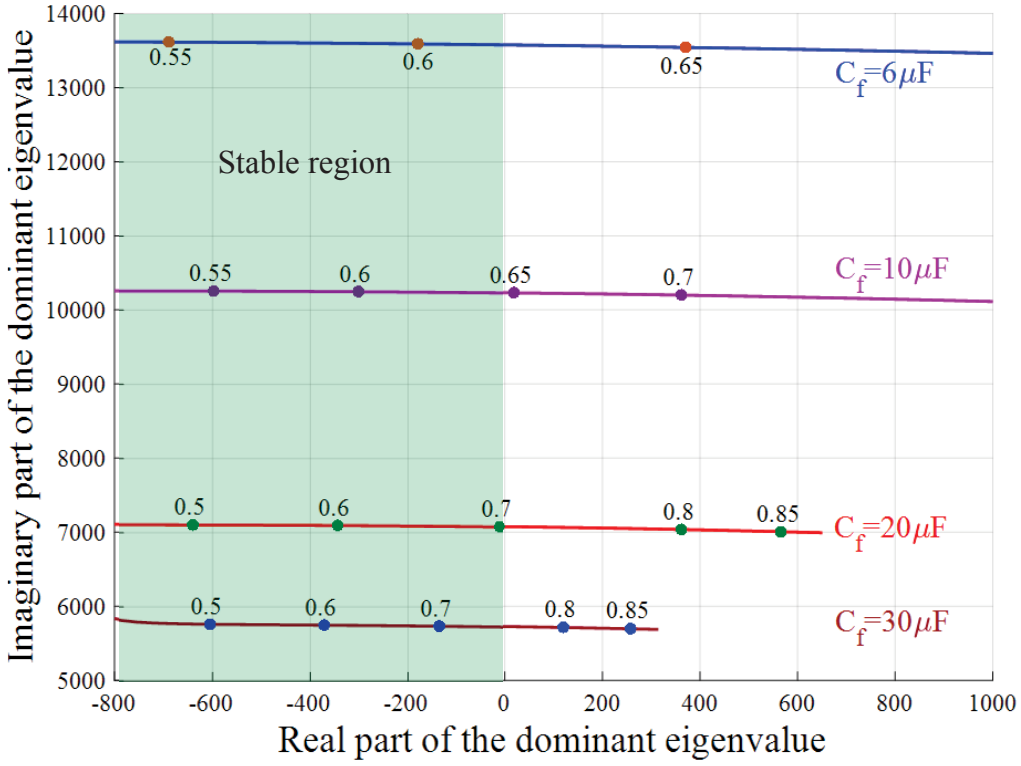
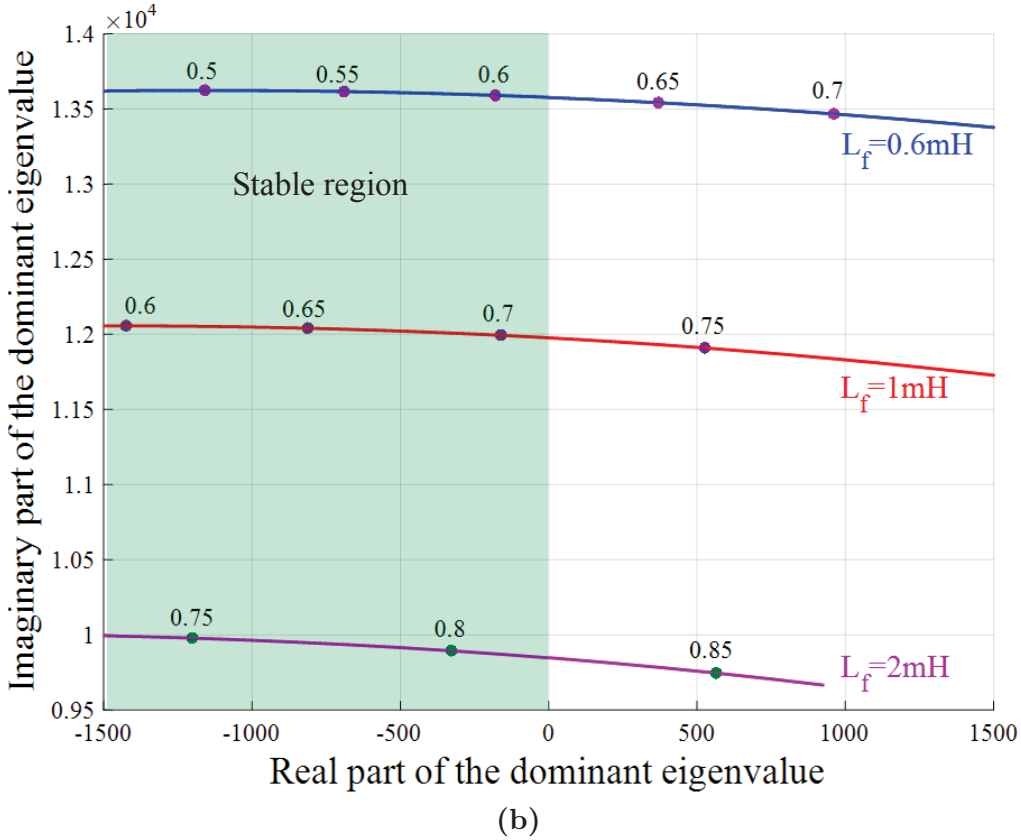


Figure 5.10: Position of the dominant eigenvalue of the state matrix A_{d2} in the complex plane as a function of the voltage gain q for different values of R_d



(a)



(b)

Figure 5.11: Position of the dominant eigenvalue of the state matrix A_{d2} in the complex plane as a function of the voltage gain q with $R_d = 10\Omega$, where a) For different values of C_f, and b) For different values of L_f

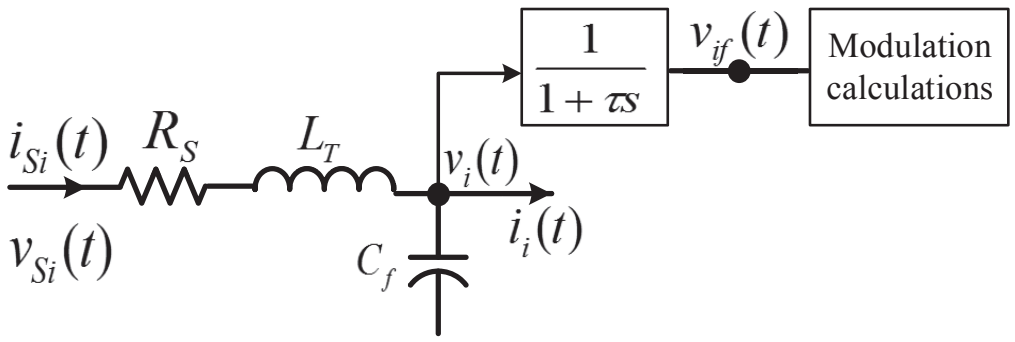


Figure 5.12: Block diagram of the single-phase input filter with a digital low-pass filter

5.4 Stability of the MC With Digital Low-Pass Input Filter

There is another method for improving the output power limit by using a digital low-pass filter that filters the amplitude of the measured input voltage [106] [103] [107]. The filtered input voltages are used for calculating the duty cycles of the switching configurations required for modulation process as shown in Figure 5.12.

The equations for the input and output of the MC, are as mentioned before in (5.15)-(5.17) and the relationship for the digital input low-pass filter referring to Figure 5.12 is [103]:

$$\frac{d\vec{v}_{if}(t)}{dt} = \frac{1}{\tau}\vec{v}_i(t) - \frac{1}{\tau}\vec{v}_{if}(t) \tag{5.64}$$

where $\vec{v}_{if}(t)$ is the output voltage of the digital filter and τ is the filter time constant. The modulation vector is defined in such a way that the input current vector is in phase with the filtered input voltage vector:

$$\vec{\psi}(t) = \vec{v}_{if}(t)e^{-j\varphi_i}\Big|_{\varphi_i=0} = \vec{v}_{if}(t) \tag{5.65}$$

Now $\vec{m}_d(t)$ and $\vec{m}_i(t)$ are defined as following to show the relationship between the filtered input voltage and output reference voltage vectors [103]:

$$\vec{m}_d(t) = \frac{\vec{v}_{or}(t)}{3\vec{v}^*_{if}(t)} \tag{5.66}$$

$$\vec{m}_i(t) = \frac{\vec{v}^*_{or}(t)}{3\vec{v}^*_{if}(t)} \tag{5.67}$$

To do the stability analysis, the state equations of the system are linearised around the steady-state operating point in a similar way to previously discussed sections. All the variables in steady state operating point are defined as mentioned before in (5.19)-(5.24). Also, as $\vec{V}_i = V_{im}$, considering (5.64), variable $\vec{v}_{if}(t)$ in steady state operating point is $\vec{V}_{if} = V_{im}$ and the above equations lead to the following small signal equations:

$$\Delta\vec{m}_d(t) = \frac{1}{3}\frac{\Delta\vec{v}_{or}(t)\vec{V}^*_{if} - \vec{V}_{or}\Delta\vec{v}^*_{if}(t)}{(\vec{V}^*_{if})^2}\bigg|_{\substack{\Delta\vec{v}_{or}(t)=0 \\ \vec{V}_{or}=qV_{im}}} \Rightarrow\ \Delta\vec{m}_d(t) = -\frac{q}{3V_{im}}\Delta\vec{v}^*_{if}(t) \tag{5.68}$$

$$\Delta\vec{m}_i(t) = \frac{1}{3}\frac{\Delta\vec{v}^*_{or}(t)\vec{V}^*_{if} - \vec{V}^*_{or}\Delta\vec{v}^*_{if}(t)}{(\vec{V}^*_{if})^2}\bigg|_{\substack{\Delta\vec{v}^*_{or}(t)=0 \\ \vec{V}^*_{or}=qV_{im}}} \Rightarrow\ \Delta\vec{m}_i(t) = -\frac{q}{3V_{im}}\Delta\vec{v}^*_{if}(t) \tag{5.69}$$

As a result, the small signal equations of the output voltage and input current space vectors can be obtained as following:

$$\begin{aligned}\Delta\vec{v}_o(t) &= \frac{3}{2}\left[\Delta\vec{v}_i(t)\vec{M}^*_i + \Delta\vec{v}^*_i(t)\vec{M}_d + V_{im}\Delta\vec{m}^*_i(t) + V_{im}\Delta\vec{m}_d(t)\right] \\ &= \frac{q}{2}\Delta\vec{v}_i(t) + \frac{q}{2}\Delta\vec{v}^*_i(t) - \frac{q}{2}\Delta\vec{v}_{if}(t) - \frac{q}{2}\Delta\vec{v}^*_{if}(t)\end{aligned} \tag{5.70}$$

$$\begin{aligned}\Delta\vec{i}_i(t) &= \frac{3}{2}\left[\Delta\vec{i}_o(t)\vec{M}_i + \Delta\vec{i}^*_o(t)\vec{M}_d + \vec{I}_o\Delta\vec{m}_i(t) + \vec{I}^*_o\Delta\vec{m}_d(t)\right] \\ &= \frac{q}{2}\Delta\vec{i}_o(t) + \frac{q}{2}\Delta\vec{i}^*_o(t) - \frac{q^2}{2\vec{Z}_l}\Delta\vec{v}^*_{if}(t) - \frac{q^2}{2\vec{Z}^*_o}\Delta\vec{v}^*_{if}(t) \\ &= \frac{q}{2}\Delta\vec{i}_o(t) + \frac{q}{2}\Delta\vec{i}^*_o(t) - \frac{q^2R_l}{|\vec{Z}_l|^2}\Delta\vec{v}^*_{if}(t)\end{aligned} \tag{5.71}$$

$$\frac{d\Delta\vec{v}_{if}(t)}{dt} = \frac{1}{\tau}\Delta\vec{v}_i(t) - \frac{1}{\tau}\Delta\vec{v}_{if}(t) \tag{5.72}$$

moreover, the resultant equations are transformed to the d-q reference frame as:

$$\begin{aligned}\Delta v_{o(d)}(t) &= q\Delta v_{i(d)}(t) - q\Delta v_{if(d)}(t)\\ \Delta v_{o(q)}(t) &= 0\end{aligned} \tag{5.73}$$

$$\begin{aligned}\Delta i_{i(d)}(t) &= q\Delta i_{o(d)}(t) - \frac{q^2 R_l}{|\vec{Z}_l|^2}\Delta v_{if(d)}(t)\\ \Delta i_{i(q)}(t) &= \frac{q^2 R_l}{|\vec{Z}_l|^2}\Delta v_{if(q)}(t)\end{aligned} \tag{5.74}$$

Finally, in steady state conditions, assuming $\Delta\vec{v}_{si}(t) = 0$, the d-q components of the small-signal equations of the linearised system around the steady state operating point are:

$$\begin{aligned}\frac{d\Delta v_{i(d)}(t)}{dt} &= \frac{1}{C_f}\Delta i_{si(d)}(t) + \omega_i \Delta v_{i(q)}(t) - \frac{q}{C_f}\Delta i_{o(d)}(t) + \frac{q^2 R_l}{C_f|\vec{Z}_l|^2}\Delta v_{if(d)}(t)\\ \frac{d\Delta v_{i(q)}(t)}{dt} &= \frac{1}{C_f}\Delta i_{si(q)}(t) - \omega_i \Delta v_{i(d)}(t) - \frac{q^2 R_l}{C_f|\vec{Z}_l|^2}\Delta v_{if(q)}(t)\end{aligned} \tag{5.75}$$

$$\begin{aligned}\frac{d\Delta i_{o(d)}(t)}{dt} &= \frac{q}{L_l}\Delta v_{i(d)}(t) - \frac{R_l}{L_l}\Delta i_{o(d)}(t) + \omega_o \Delta i_{o(q)}(t) - \frac{q}{L_l}\Delta v_{if(d)}(t)\\ \frac{d\Delta i_{o(q)}(t)}{dt} &= -\omega_o \Delta i_{o(d)}(t) - \frac{R_l}{L_l}\Delta i_{o(q)}(t)\end{aligned} \tag{5.76}$$

$$\begin{aligned}\frac{d\Delta v_{if(d)}(t)}{dt} &= \frac{1}{\tau}\Delta v_{i(d)}(t) - \frac{1}{\tau}\Delta v_{if(d)}(t)\\ \frac{d\Delta v_{if(q)}(t)}{dt} &= \frac{1}{\tau}\Delta v_{i(q)}(t) - \frac{1}{\tau}\Delta v_{if(q)}(t)\end{aligned} \tag{5.77}$$

and the state equations of the system using the digital input filter are defined as [103]:

$$\frac{d\Delta X_f}{dt} = A_f \Delta X_f \tag{5.78}$$

$$\Delta X_f = \begin{bmatrix}\Delta i_{si(d)} & \Delta i_{si(q)} & \Delta v_{i(d)} & \Delta v_{i(q)} & \Delta i_{o(d)} & \Delta i_{o(q)} & \Delta v_{if(d)} & \Delta v_{if(q)}\end{bmatrix}^T \tag{5.79}$$

$$A_f = \begin{bmatrix} -\frac{R_s}{L_T} & \omega_i & \frac{-1}{L_T} & 0 & 0 & 0 & 0 & 0 \\ -\omega_i & -\frac{R_s}{L_T} & 0 & \frac{-1}{L_T} & 0 & 0 & 0 & 0 \\ \frac{1}{C_f} & 0 & 0 & \omega_i & -\frac{q}{C_f} & 0 & K_f & 0 \\ 0 & \frac{1}{C_f} & -\omega_i & 0 & 0 & 0 & 0 & -K_f \\ 0 & 0 & \frac{q}{L_l} & 0 & -\frac{R_l}{L_l} & \omega_o & -\frac{q}{L_l} & 0 \\ 0 & 0 & 0 & 0 & -\omega_o & -\frac{R_l}{L_l} & 0 & 0 \\ 0 & 0 & \frac{1}{\tau} & 0 & 0 & 0 & -\frac{1}{\tau} & 0 \\ 0 & 0 & 0 & \frac{1}{\tau} & 0 & 0 & 0 & -\frac{1}{\tau} \end{bmatrix} \tag{5.80}$$

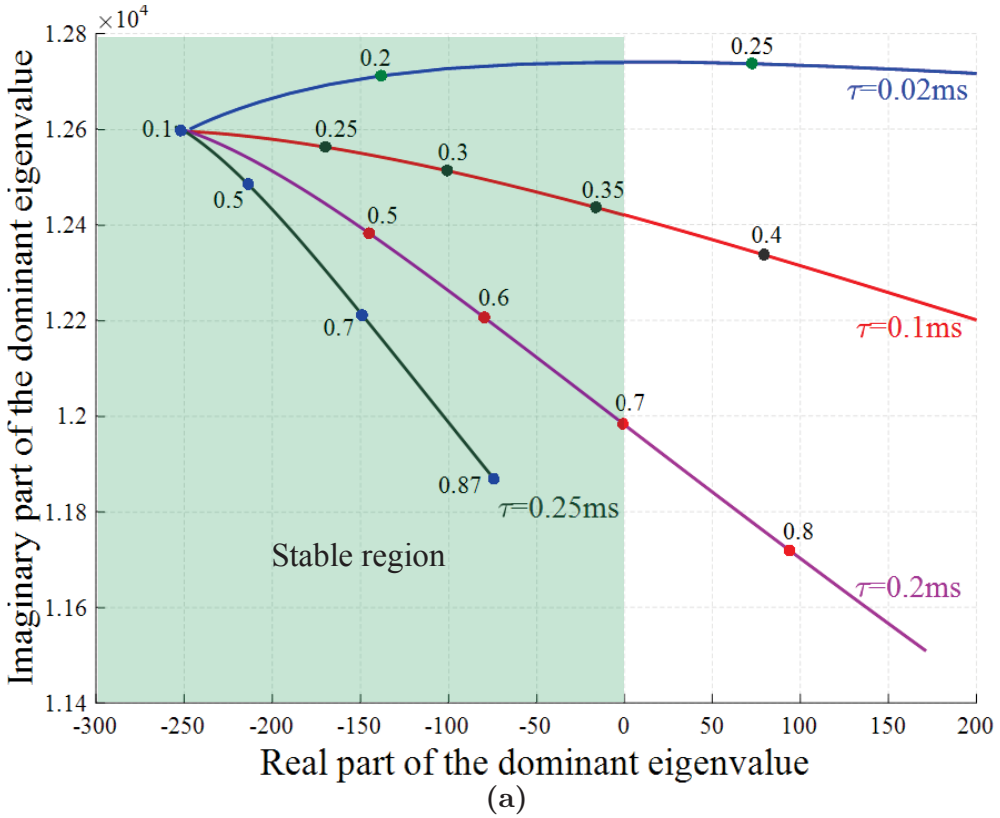
where:

$$K_f = \frac{q^2 R_l}{C_f |\vec{Z}_l|^2} \tag{5.81}$$

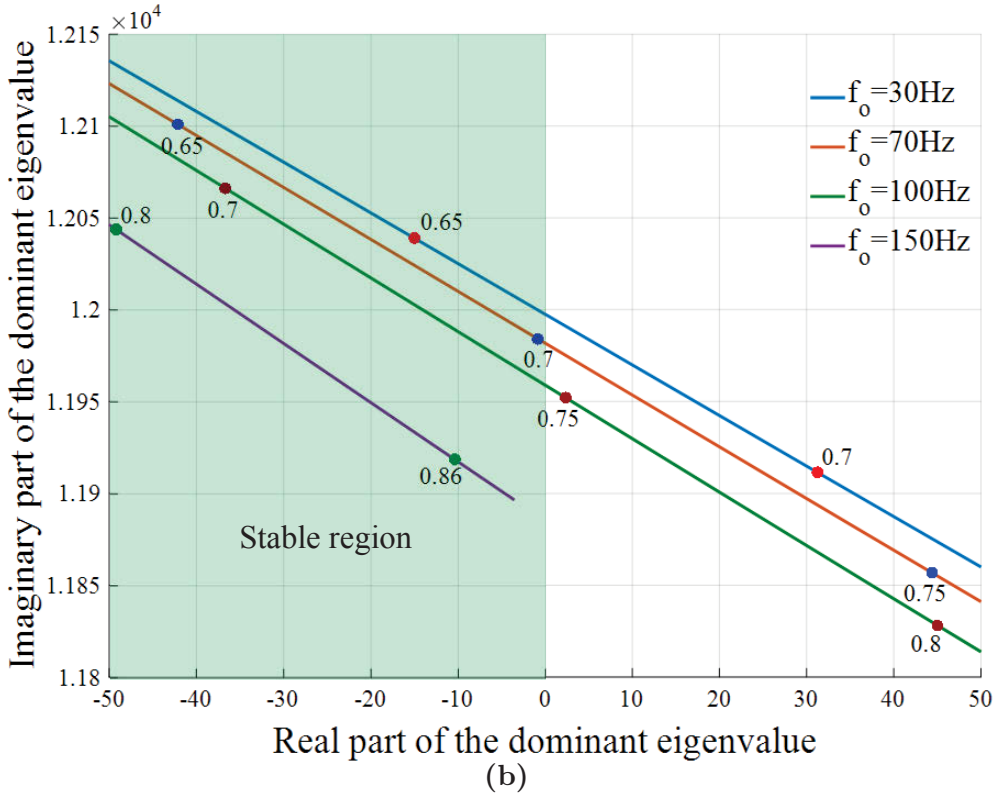
Similar to the previous sections, the resultant matrix A_f is utilised for numerical stability analysis in the next section.

5.4.1 Numerical approach for stability analysis of the MC with digital input filter

As before the position of the real part of the dominant eigenvalues of matrix A_f is considered as the criterion for stability. Figure 5.13a shows the effect of the digital filter time constant τ and output frequency f_o on the stability of the system. For the system parameters mentioned in Table 5.1 as expected, increasing the filter time constant helps the system to stay stable for higher voltage gains. Also rising the output frequency has a positive effect on the stability, so that for $f_o = 150Hz$ with $\tau = 0.2ms$ system stays stable for maximum voltage gain while for presented lower frequencies it is unstable. According to the results illustrated in Figure 5.14 about the input filter parameters, larger values of capacitance and smaller inductance cause increment in the system stability limit.



(a)



(b)

Figure 5.13: Position of the dominant eigenvalue of the state matrix A_f in the complex plane as a function of the voltage gain q, where a) For different values of τ, and b) For different values of f_o when $\tau = 0.2ms$

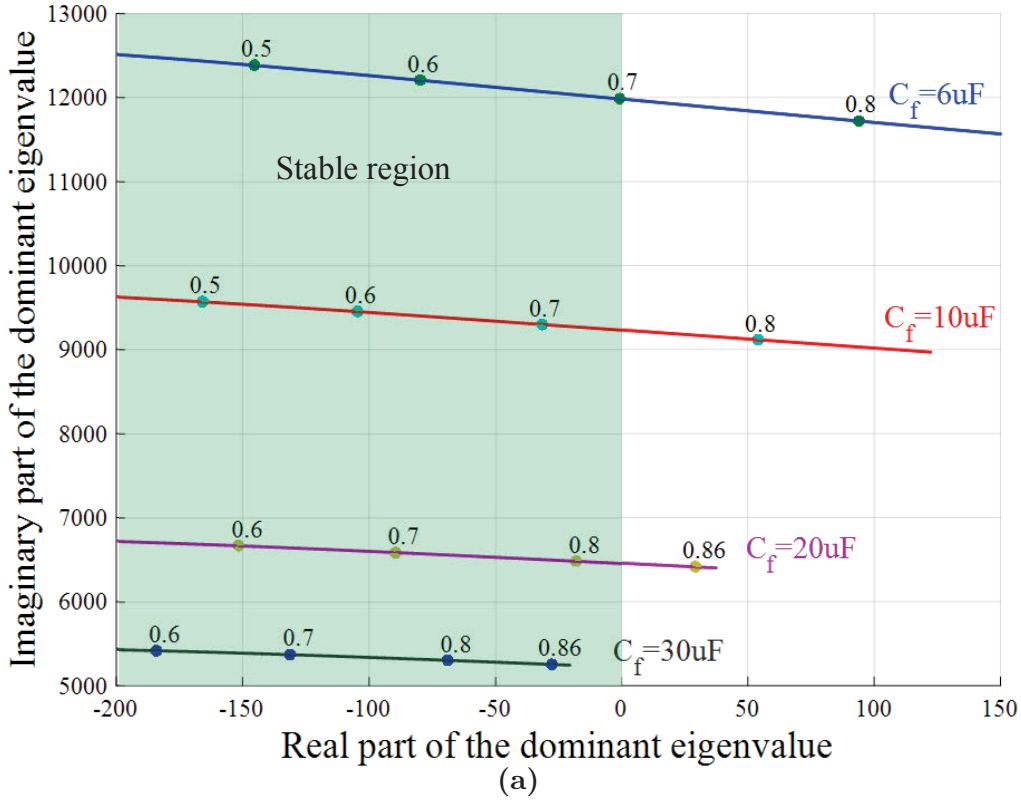


Figure 5.14: Position of the dominant eigenvalue of the state matrix A_f in the complex plane as a function of the voltage gain q when $\tau = 0.2ms$, where a) For different values of C_f, and b) For different values of L_f

5.5 Conclusion

In this chapter, the stability of the DMC system including DMC, the input filter and a star connected R-L load has been analysed. The basics of the mathematical model of the system and its small-signal model have been presented to show the impacts of the system parameters on the stability. A theoretical investigation was carried out on the two solutions for improving the stability of the system, adding a damping resistor or a digital filter. A numerical approach has been used by evaluating the position of the real part of the dominant eigenvalue of the matrix that describes the system. The dominant eigenvalue of the matrix can be defined as a function of the voltage gain or the output power, it is possible to find the approximate range of the maximum voltage gain or the maximum output power that keeps the system stable. Although the effect of each system parameter on the stability has been illustrated separately on a diagram to show their particular impact on the stability problem, it is possible to adjust some of them like filter parameters, to increase the stability limit. In both stabilisation methods, increasing the input filter capacitance C_f causes an increment in the stability region. However, in case of the input filter inductance L_f, it has a different effect. In the damping resistor adding strategy, increasing the inductance helps to the system stabilisation while with the digital filter method, reduction of the inductance has such a positive effect. It can be found all the system parameters have more or less an effect on this problem, but some of them are more effective and controllable.

Chapter 6

BIDIRECTIONAL POWER FLOW CONTROL

6.1 Introduction

As MCs offer a bidirectional power flow control with controllable input power factor and sinusoidal input and output currents, they can be used as a grid-connected converter to control the flow of power and convert it into a suitable AC form as required. MCs are particularly attractive for variable frequency wind and marine turbine generators and high-speed turbine generators [48, 55, 56]. For MCs, on the output side the voltage and current amplitude and frequency, and in the input side, the power factor or current amplitude can be controlled. Although it is not possible to control the input and output variables simultaneously because the converter cannot store energy, and controlling any variable at one side is at the expense of some effects on the other side.

When the output variables of the power electronic converters are tightly regulated, the converter behaves as a constant power load (CPL) which presents a negative incremental input resistance. The negative incremental resistance of the CPLs can destabilize the input LC filter and the system [111, 112] depending on the system parameters. Although, the instability related to the negative input resistance depends on the system parameters and can be improved by changing the

input filter parameters, however, this is often undesirable and not recommended. The input filter is usually designed in order to satisfy the EMC requirements and provide attenuation at the switching frequency. The current fed into the grid should have high quality considering upper limits on the source current total harmonic distortion (THD) levels. As the MC is known as an all-silicon converter and does not require large energy storage components, the size of the input filter components should be minimized, and the input displacement factor is set at unity. Therefore, the instability needs to be eliminated by different logical methods.

A large amount of research work has been done on destabilizing effects of CPLs in multi-converter power electronic systems, DC-DC and AC-DC converters and different strategies have been proposed to overcome this problem [111–113]. However, in the case of MCs, stability analysis is not widely studied, and more research work needs to be done in this field. There are different methods for stabilizing the converters. Adding the damping resistor in parallel with the filter inductor is the basic approach for MC stabilization [72, 102]. As the inherent damping factor of the LC filter is negligible, adding the damping resistors can reduce the input current oscillation. However, the main drawback of this method is a large amount of dissipation. Loss-free resistors are another solution using extra power electronic elements like inductors and switches which are complicated and need extra components [114, 115]. Active techniques are another alternative for stabilization without adding extra elements. The active methods are implemented by modifying the controller, with adding a negative input resistance compensator or using additional algorithms [103, 106–109, 113]. At this strategy, the input impedance of the converter is modified by applying a correction term in the feedback loop. In [109], the converter stability is achieved by constructing different correction terms for modifying the input admittance of the MC, using additional algorithms in each direction of power flow. Also, the measured input voltage can be filtered out using a digital low-pass filter before applying to the modulation section and calculating the duty cycles. The digital filter can be applied for filtering the amplitude of the input

voltages [103, 106, 107] or the angle of the input voltage vector [107, 108].

The analysis presented in this chapter is focused on the bidirectional power-flow ability of the MC with a concentration on improving the stability issue for a better efficiency, considering the EMC standards [65]. The proposed converter is used as an interface between a microgrid and the utility grid. The renewable sources, loads and storage devices are connected to a common ac bus through voltage conversion blocks in the microgrid. The active and reactive power flows are going to be controlled in both directions independently between the microgrid and utility grid, while the system remains stable for the whole operating range. The modulation strategy is the space vector modulation (SVM) technique with an output current control loop based on the voltage oriented control (VOC) strategy. Compared to the previous stabilization techniques, this paper suggests a combination of virtual harmonic damper using a digital lowpass filter and passive damping using damping resistors. The suggested technique includes the advantages of the both methods in terms of the power loss and undesirable transient. In addition, it is shown that the number of branch-switch-overs (BSOs) and commutation process can affect the overall system stability. Further discussions are provided in order to show how the clock frequency of the programable logic device for commutation process, and the number of BSOs can affect the stability voltage gain limit. The proposed stability technique is applied to a typical system presented in Fig. 5.1, and the theoretical analysis based on a state variable average model is presented. The stability of the system is evaluated by numerical simulations and experimental tests.

6.1.1 System stabilisation using the damping resistor

As explained before in the previous chapter, the eigenvalues of the state space matrix can be used as stability criteria. The space matrix A_{d2} (5.63), which is a function of the system parameters, has been analyzed, and when its dominant eigenvalue is negative, the converter remains stable. The following figures explain the effects of

Table 6.1: Matrix converter system parameters for stability analysis

Input source	Input filter	output load
$V_{i,rms} = 240V$	$C_f = 6\mu F$	$R_l = 10\Omega$
$L_s = 0.4mH$	$L_f = 0.6mH$	$L_l = 6mH$
$R_s = 0.5\Omega$	$f_i = 50Hz$	$f_o = 70Hz$

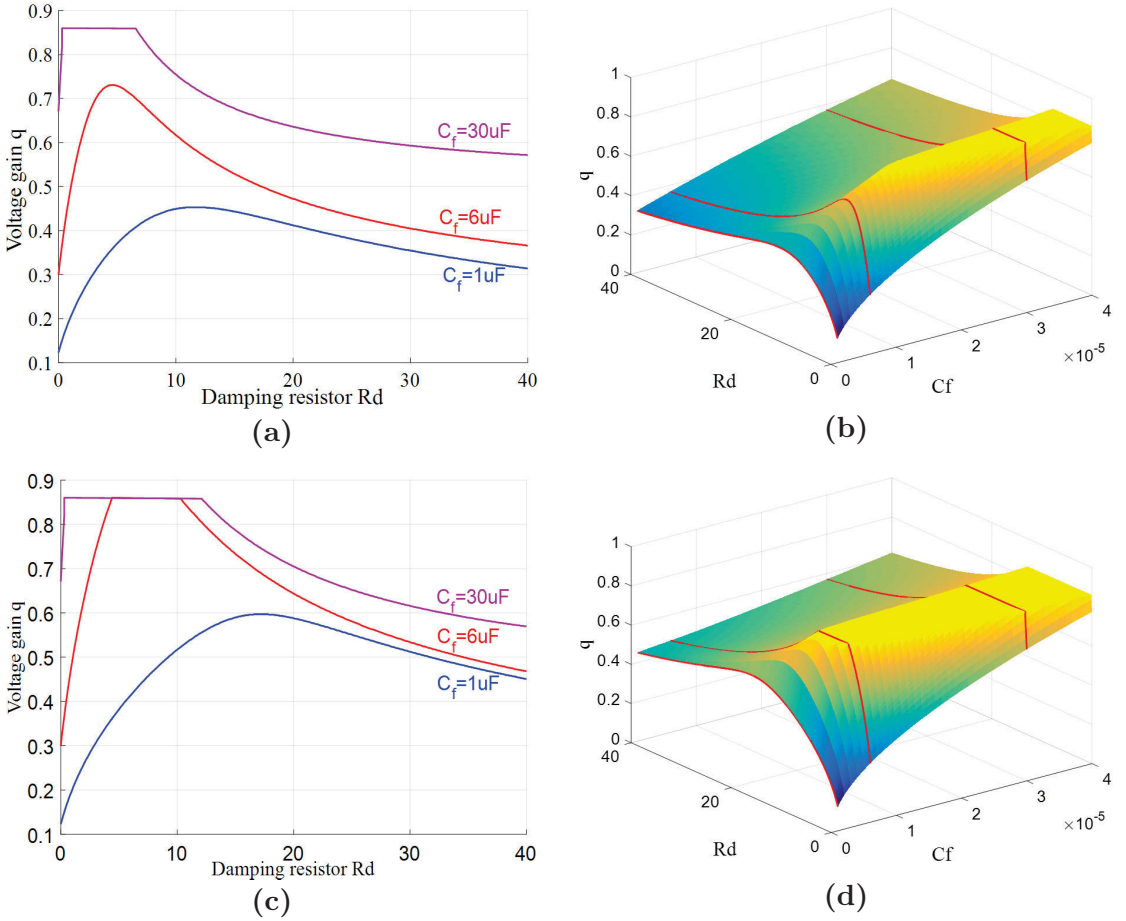
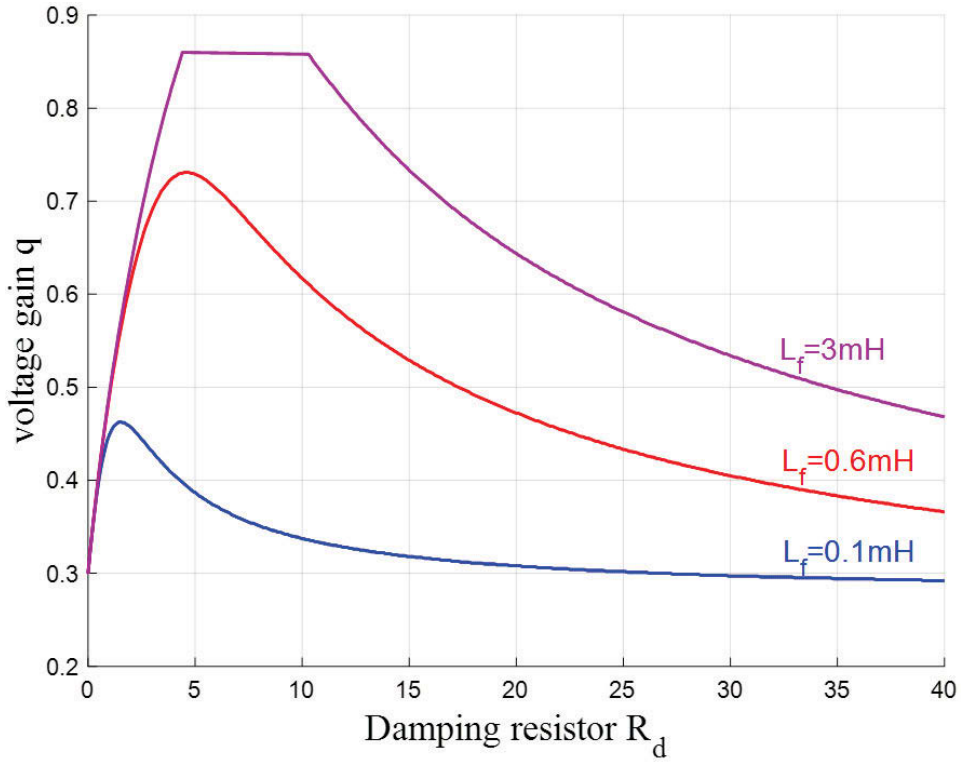
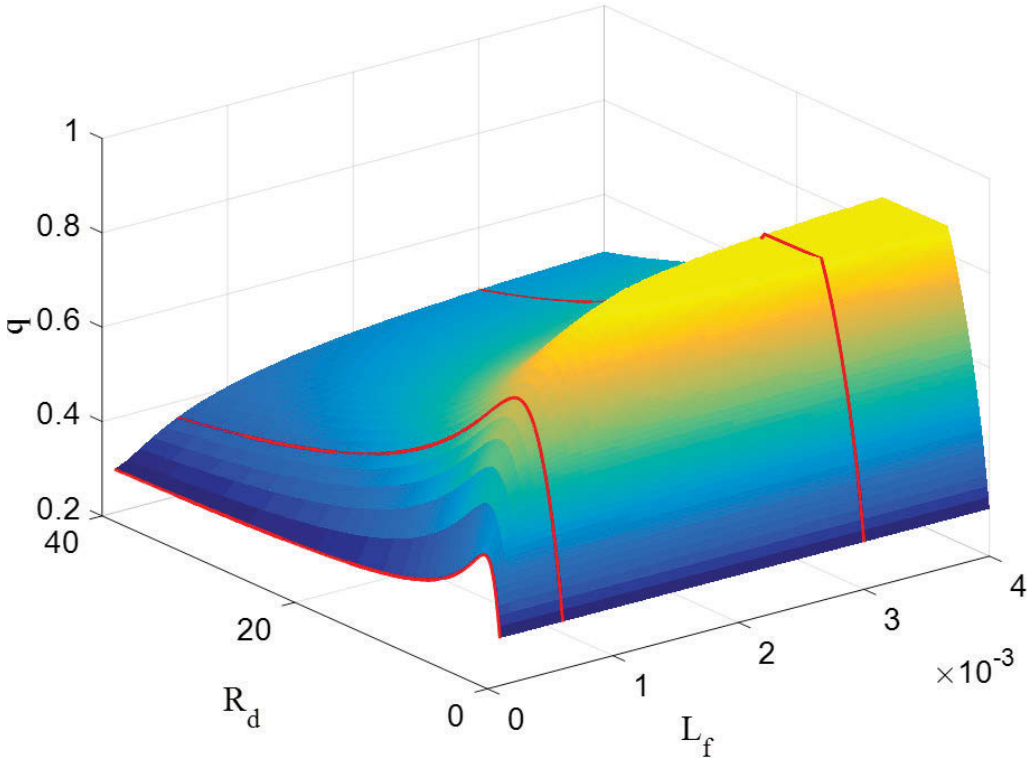


Figure 6.1: Stability region of the DMC system, voltage gain 'q' against damping resistor R_d, where a) For three different filter-capacitance C_f when $L_f = 0.6mH$, b) 3D graph of the case (a), c) For three different filter capacitance C_f when $L_f = 3mH$, and d) 3D graph of the case (c)

different parameters of the system on the stability issue. Figure 6.1 illustrates the stability region of the system when the damping resistor R_d is used as the solution for system instability. The figure shows the maximum voltage gain against the damping resistor R_d for different filter capacitances. The DMC system parameters referred to Figure 2.6 are presented in Table 6.1, and the figure illustrates the results for

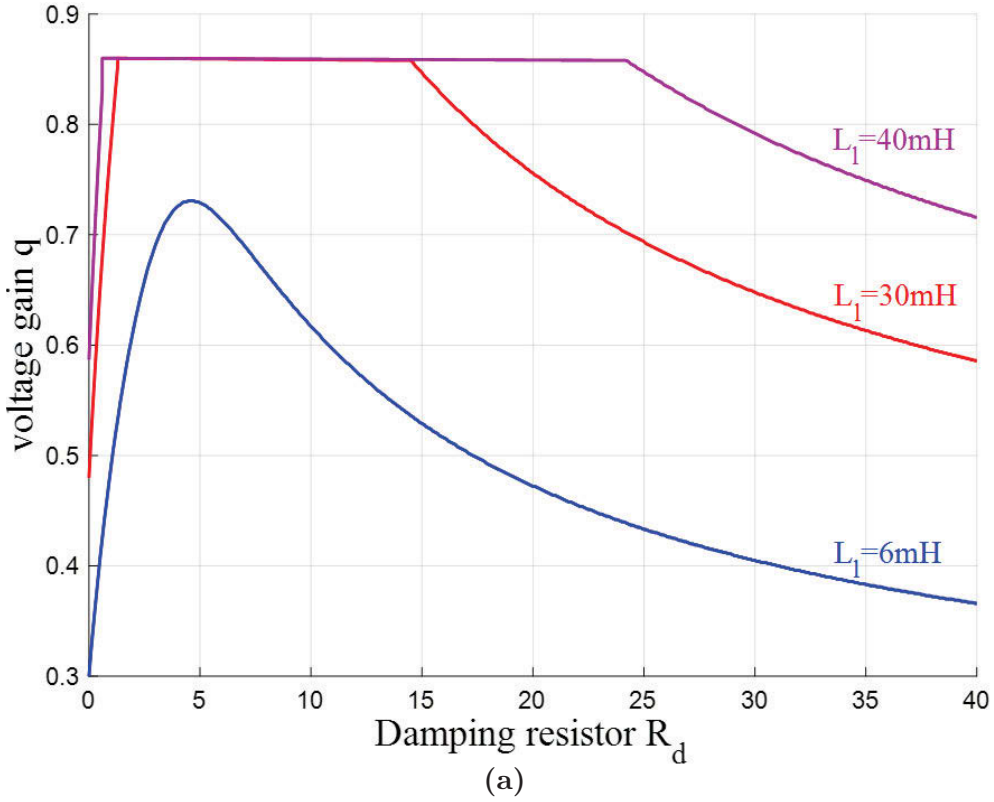


(a)

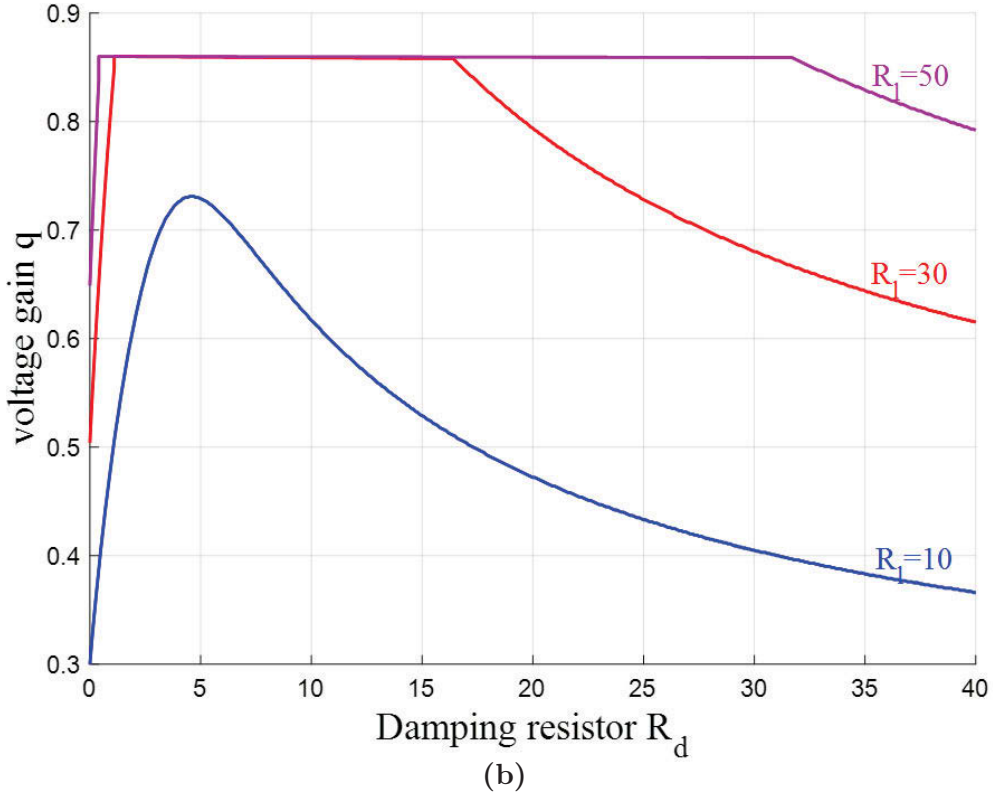


(b)

Figure 6.2: Stability region of the DMC system, voltage gain 'q' against damping resistor R_d, where a) For three different filter inductance L_f, and b) 3D graph of the case (a)

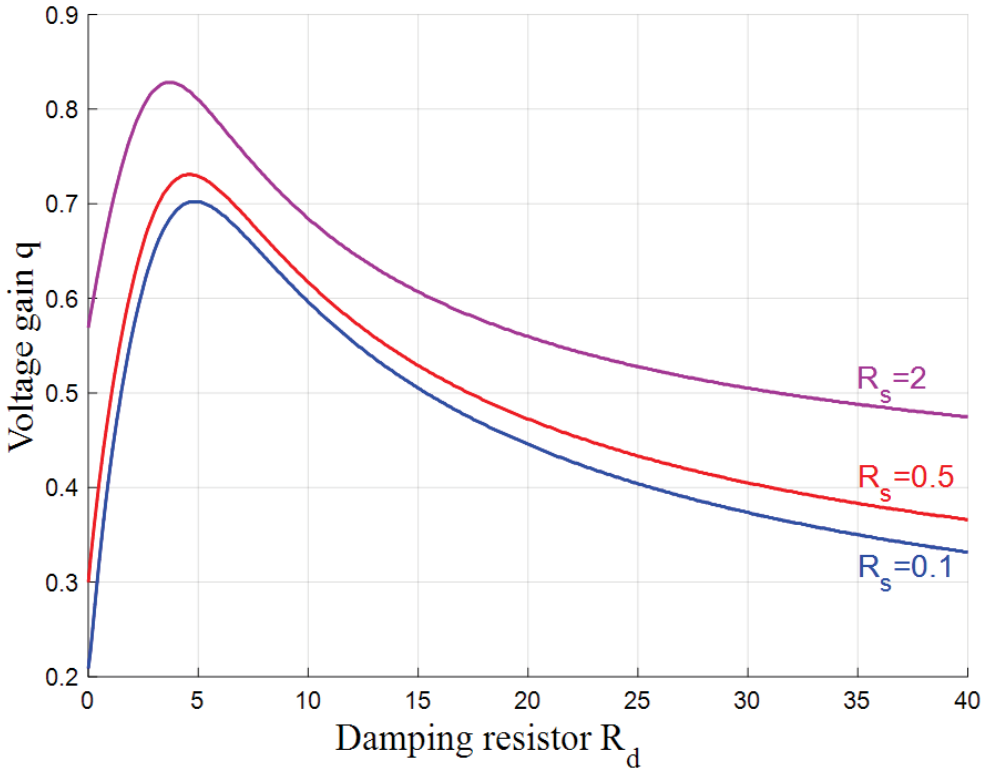


(a)

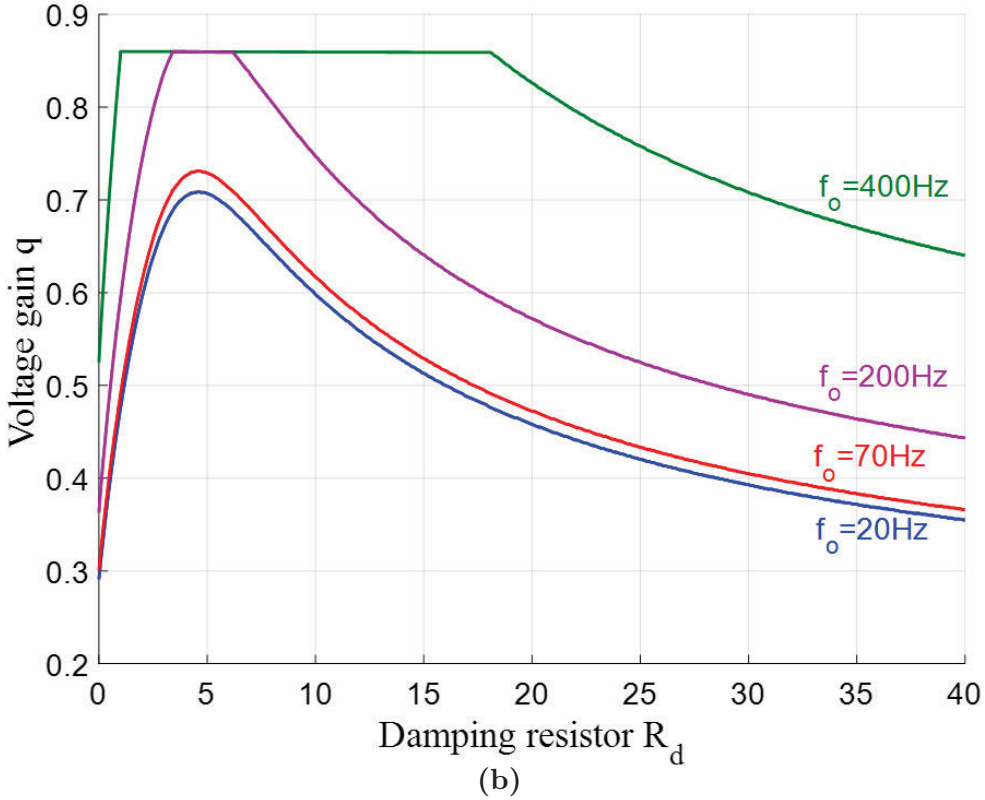


(b)

Figure 6.3: Stability region of the DMC system, voltage gain 'q' against damping resistor R_d, where a) For different values of the load inductance L_l, and b) For different values of the load resistance R_l



(a)



(b)

Figure 6.4: Stability region of the DMC system, voltage gain 'q' against damping resistor R_d, where a) For different values of the line resistor R_s, and b) For different values of the output frequency f_o

two different filter inductances, 0.6mH and 3mH. The stability region is under the curves, and above the curves the system becomes unstable. As can be observed, in the same conditions, increasing the filter inductance, expands the stability region. On the other hand, as shown in Figures 6.1d and 6.1c, for example when $C_f = 6\mu F$ and $L_f = 3mH$, to have the maximum voltage gain 0.86, R_d can be selected between 5Ω and 10Ω and as the smaller damping resistance can transfer the output distortions to the input source, it is better to put the higher resistance in parallel with the filter inductances. Also, for some filter capacitances, the voltage gain cannot reach to the maximum value (0.86), and C_f should be increased to improve the system stability.

On the other hand, increasing the inductance of the input filter also increases the stability region of the converter as demonstrated in Figure 6.2. Therefore, it is possible to have a stable system with the mentioned parameters in Table 6.1 by increasing the filter inductance and proper value of the damping resistance. Based on Figure 6.3, the load parameters have significant effects on the converter performance, and larger resistance or inductance on the load side improves the stability. Input source and line resistance (R_s) and output frequency (f_o) are the other parameters which have slight effects on this problem as shown in Figure 6.4. It can be seen that the stability region slightly increases for higher output frequency and source resistance. Obviously although changing some of the parameters like (R_s), (f_o), load variables and so on can change the stability performance, these are not the parameters that can be controlled to stabilise the system. The filter parameters are the only variables which can be designed to improve the system stability.

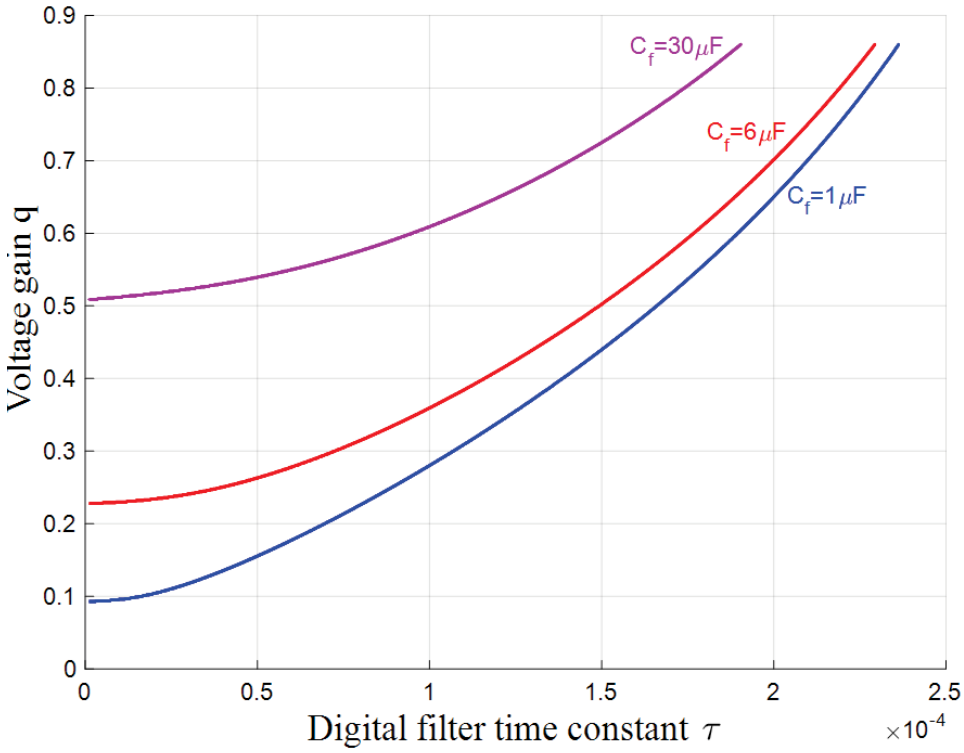
6.1.2 Improving the stability using the digital filter

Filtering the amplitude of the measured input voltage for modulation process is another solution for MC stability problem [103] [107]. It can be carried out using a digital low-pass filter in the digital signal processor which is utilised for modulation and control process. The following figures have been obtained based on the eigenvalues of matrix A_f in (5.80) which the dominant eigenvalue shows the stability

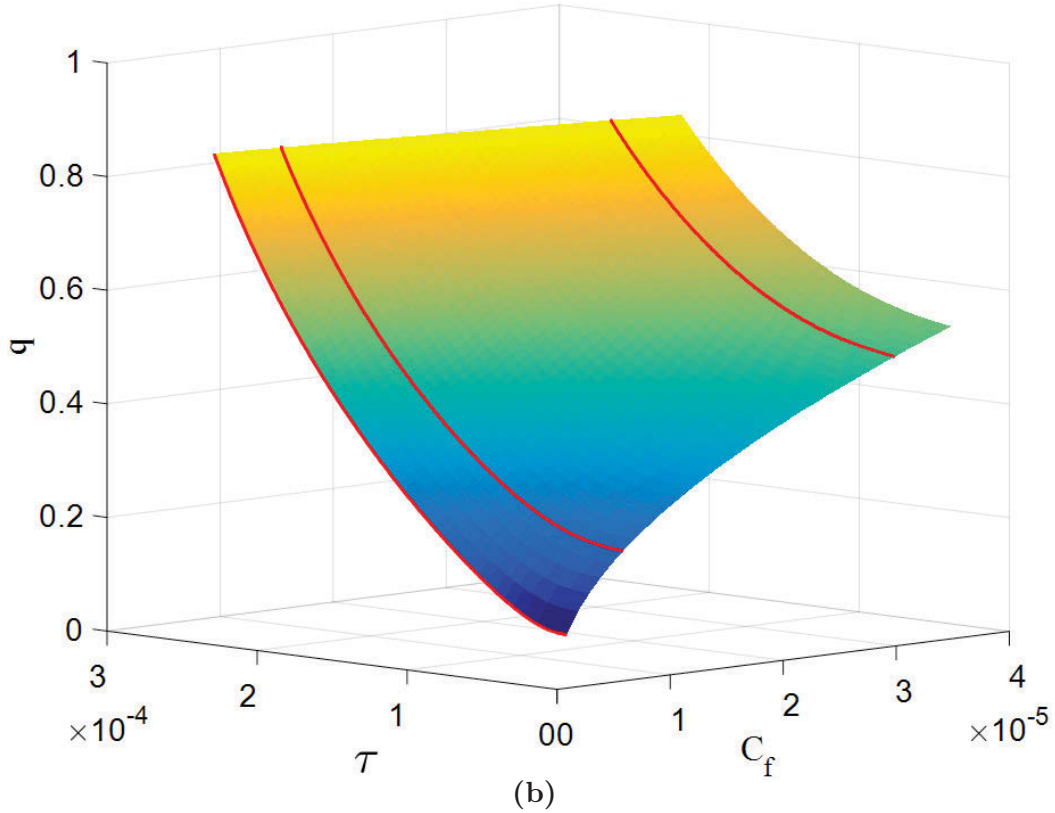
margin. The area under the 3D-planes and the graphs are the stability areas. Here again increasing the filter capacitance, C_f expands the stability region as illustrated in Figure 6.5. As can be seen in Figure 6.5, again increasing the filter capacitance has a noticeable effect on improvement of the stability. However, unlike the stabilisation using damping resistor, decreasing the filter inductance causes the system remains stable for higher voltage gains as shown in Figure 6.6. For any value of the filter parameters, there is a special digital filter time constant that permits the maximum voltage gain. Also Figures 6.7 and 6.8 illustrate the effects of the load parameters, the input line resistance and the output frequency on the system stability. Increasing the load inductance and resistance, output frequency and line resistance increases the stability region and for having the maximum voltage gain, a smaller time constant τ is needed. As an example, Figure 6.7a shows that for $L_l = 6mH$ the filter time constant τ should be around 0.23ms to reach the maximum voltage gain in the stable region, while for $L_l = 60mH$ it reduces to about 0.08ms.

6.2 System Stabilisation by Applying a Combination of the Damping Resistance and Digital Input Filter

As discussed before, the parallel damping resistance method is the most common strategy to make sure a MC stays stable for the whole range of the voltage gain. On the other hand, the damping resistor allows the high-frequency harmonics of the input current to pass through, and so the smaller damping resistance causes the more THD of the source current even without a closed loop control. Also, the power loss of the small damping resistances is the other issue which should be considered. Adding a digital input filter for smoothing the measured input voltage is another strategy which does not include any extra power loss. On the other hand, as illustrated in [103] the high-frequency disturbances of the input voltage can be reflected on the output side proportional to the filter time constant. It means that

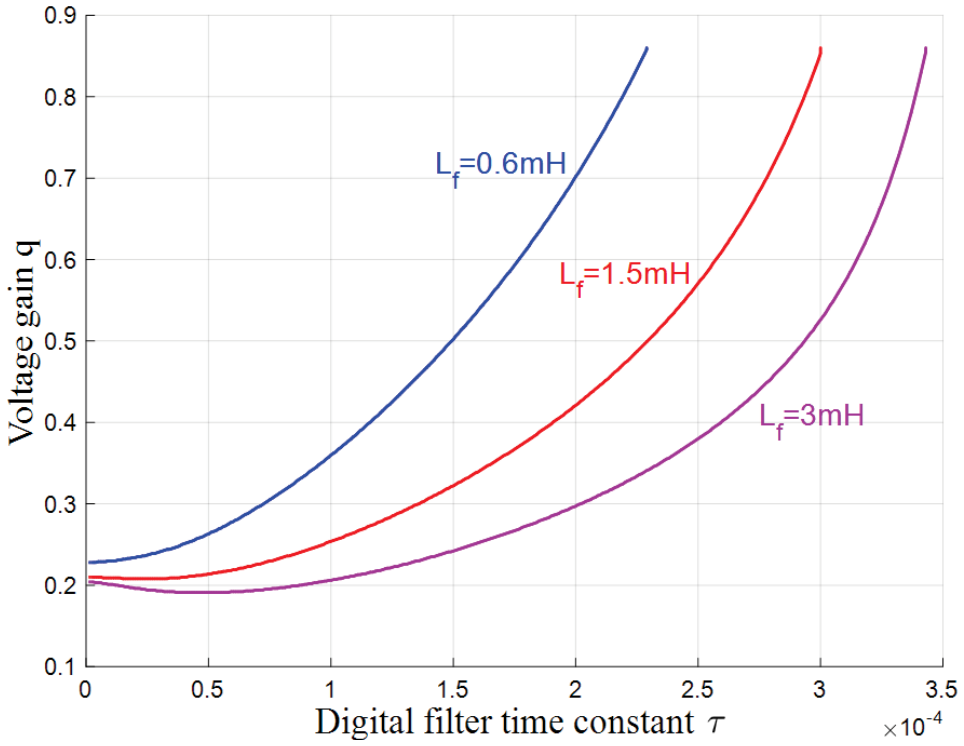


(a)

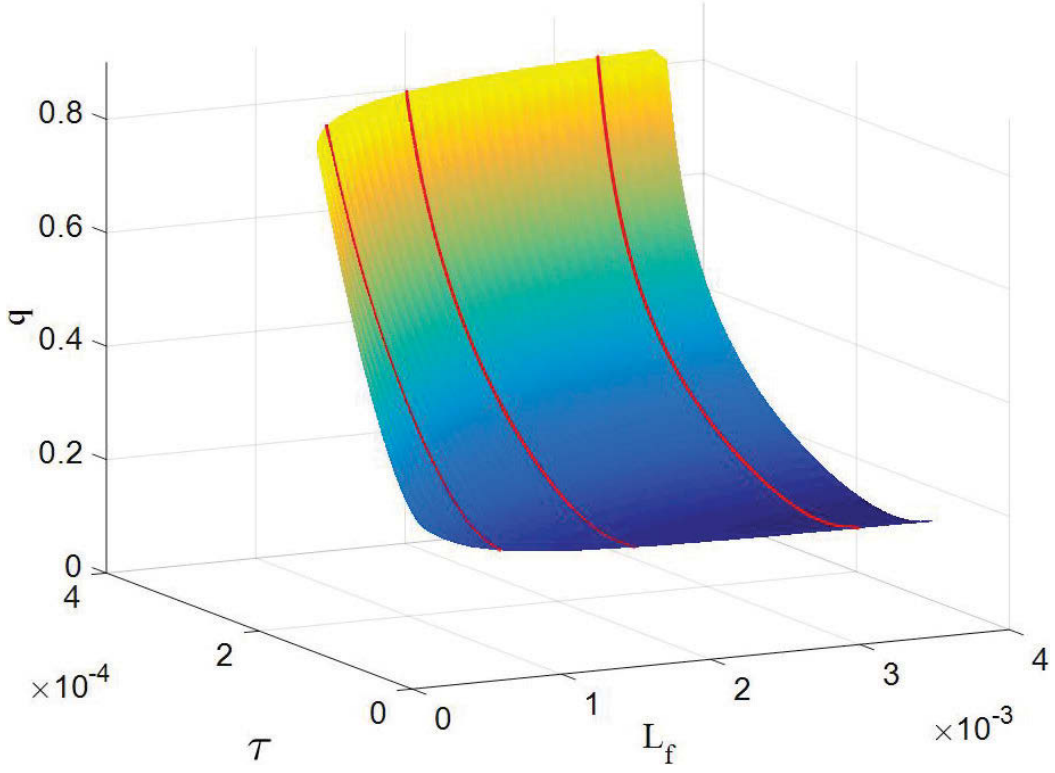


(b)

Figure 6.5: Stability region of the DMC system, voltage gain 'q' against input digital filter time constant τ, where a) For three different filter capacitance C_f, and b) 3D graph of the case (a)

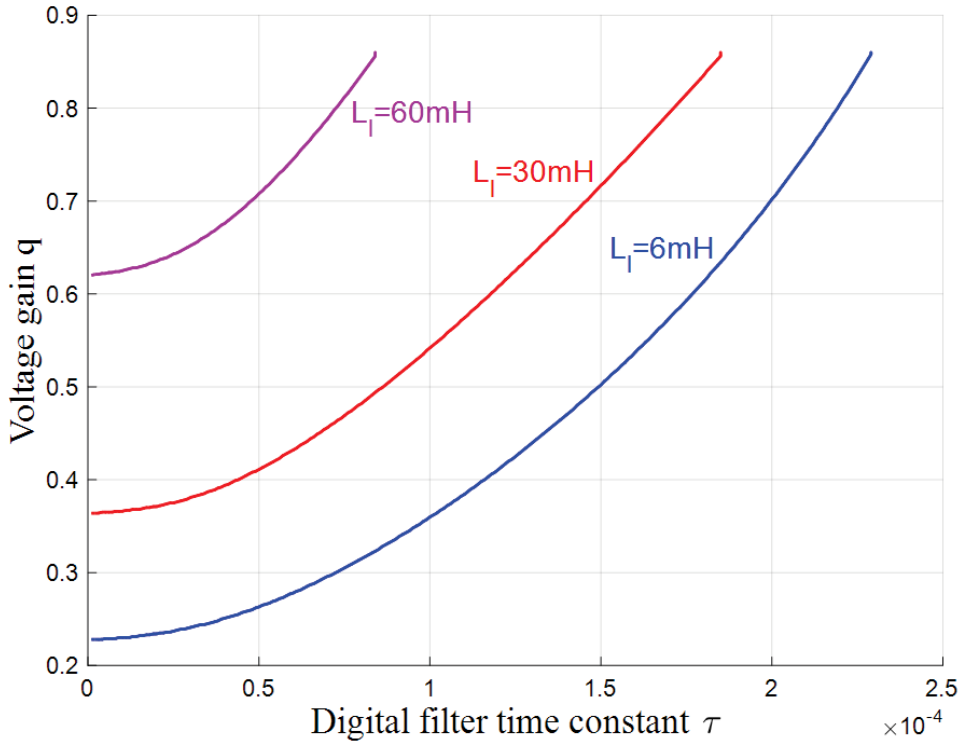


(a)

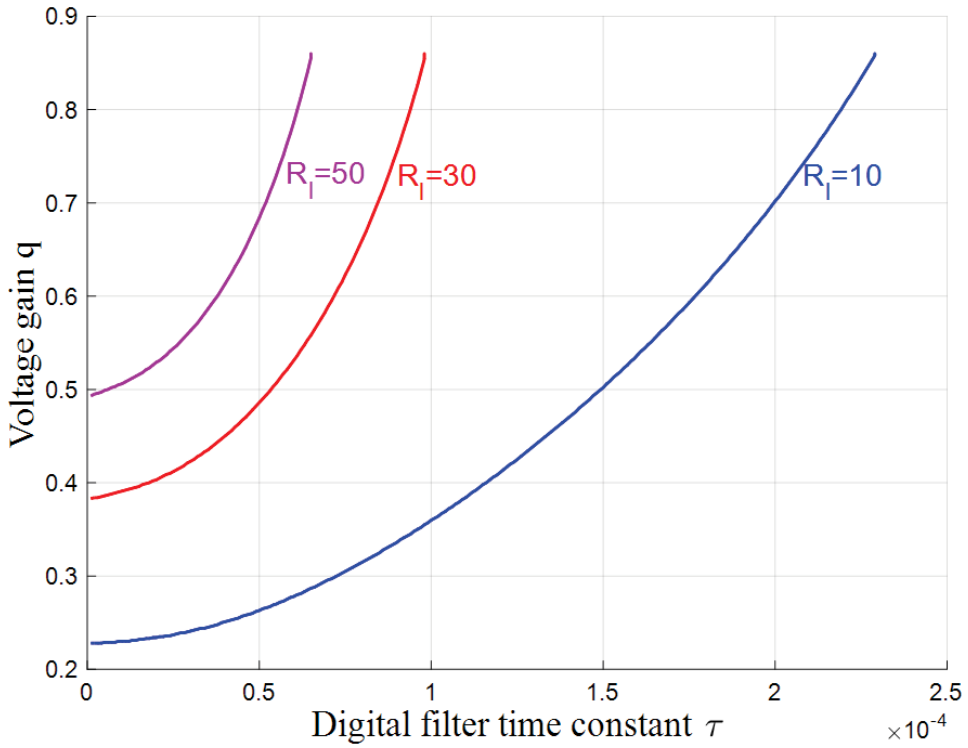


(b)

Figure 6.6: Stability region of the DMC system, voltage gain 'q' against input digital filter time constant τ, where a) For three different filter inductance L_f, and b) 3D graph of the case (a)

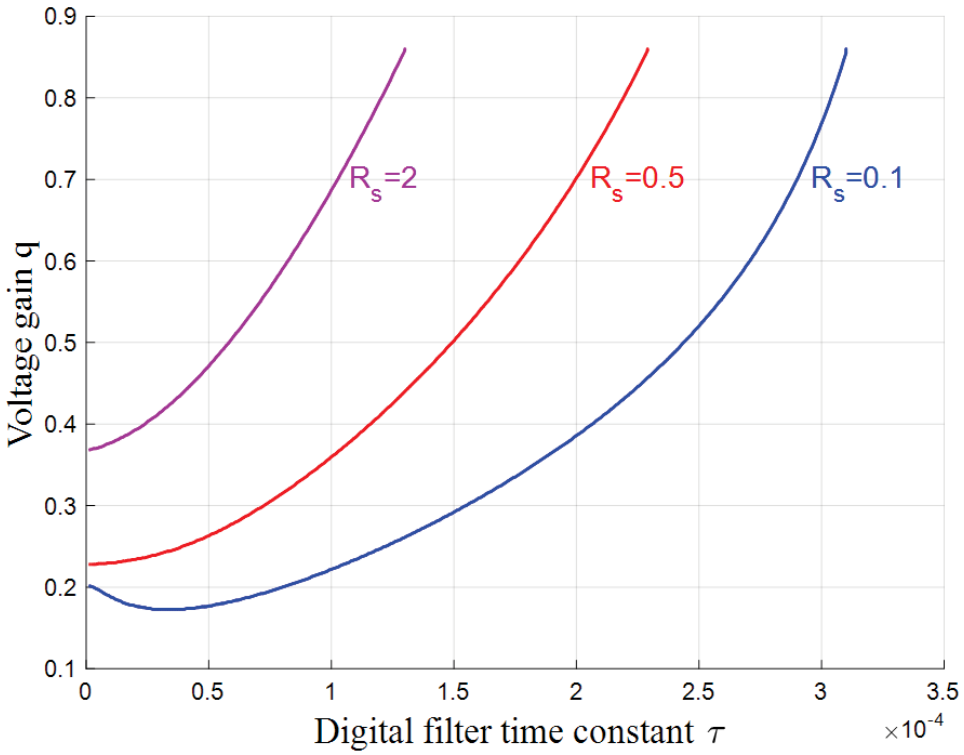


(a)

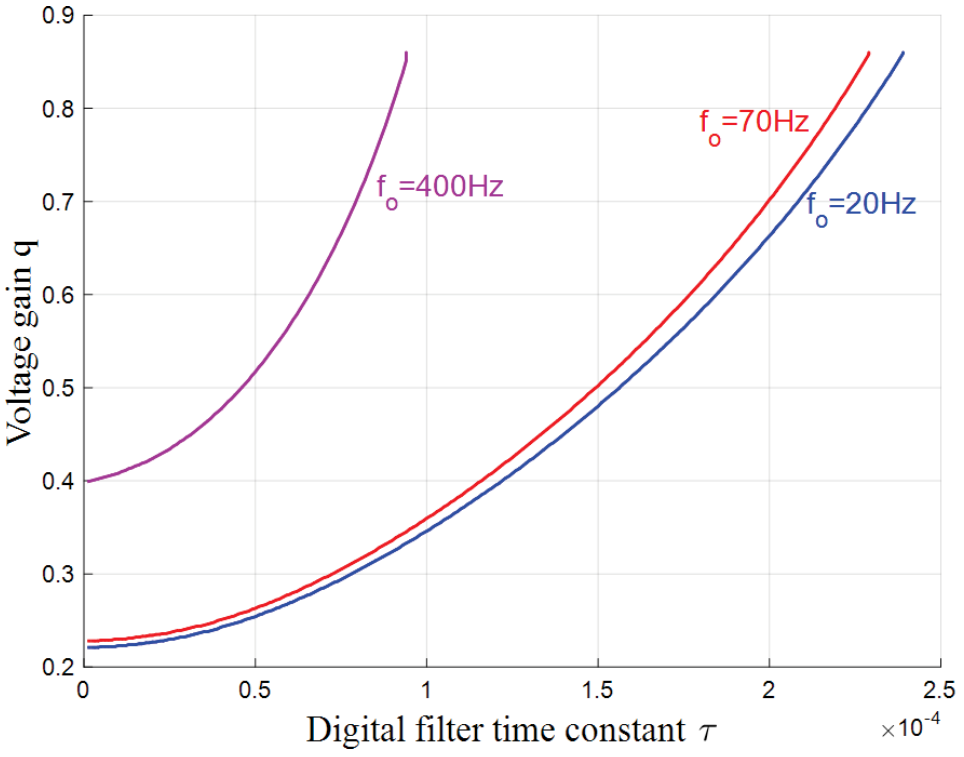


(b)

Figure 6.7: Stability region of the DMC system, voltage gain 'q' against input digital filter time constant τ, where a) For different values of the load inductance L_l, and b) For different values of the load resistance R_l



(a)



(b)

Figure 6.8: Stability region of the DMC system, voltage gain 'q' against input digital filter time constant τ, where a) For different values of the line resistance R_s, and b) For different values of the output frequency f_o

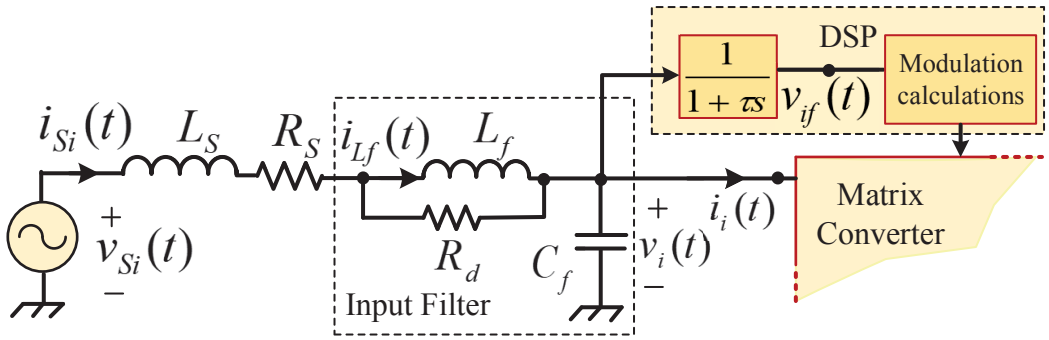


Figure 6.9: Block diagram of one of the input phases with a digital low-pass filter and the damping resistor

by increasing τ for attenuating the low-frequency harmonics of the input voltage, the high-frequency harmonics of the input voltage transfers to the output side.

In the following, a strategy using a combination of the two solutions is presented to take advantage of both and to reduce their disadvantages. In other words, by increasing the damping resistance and decreasing the digital filter time constant, it is possible to reduce the power loss while the system remains stable for the whole range of the voltage gain.

Referring to Figure 6.9, the nonlinear equations for the input side in a synchronous reference frame rotating at the supply angular frequency ω_i are:

$$\frac{d\vec{i}_{si}(t)}{dt} = -(\frac{R_s + R_d}{L_s} + j\omega_i)\vec{i}_{si}(t) + \frac{1}{L_s}\vec{v}_{si}(t) - \frac{1}{L_s}\vec{v}_i(t) + \frac{R_d}{L_s}\vec{i}_{Lf}(t) \tag{6.1}$$

$$\frac{d\vec{v}_i(t)}{dt} = \frac{1}{C_f}\vec{i}_{si}(t) - j\omega_i\vec{v}_i(t) - \frac{1}{C_f}\vec{i}_i(t) \tag{6.2}$$

$$\frac{d\vec{i}_{Lf}(t)}{dt} = \frac{R_d}{L_f}\vec{i}_{si}(t) - \left(\frac{R_d}{L_f} + j\omega_i\right)\vec{i}_{Lf}(t) \tag{6.3}$$

$$\frac{d\vec{v}_{if}(t)}{dt} = \frac{1}{\tau}\vec{v}_i(t) - \frac{1}{\tau}\vec{v}_{if}(t) \tag{6.4}$$

and their small-signal equations can be defined based on the method presented in [72, 103] as follows:

$$\frac{d\Delta\vec{i}_{si}(t)}{dt} = -(\frac{R_s + R_d}{L_s} + j\omega_i)\Delta\vec{i}_{si}(t) + \frac{1}{L_s}\Delta\vec{v}_{si}(t) - \frac{1}{L_s}\Delta\vec{v}_i(t) + \frac{R_d}{L_s}\Delta\vec{i}_{Lf}(t) \quad (6.5)$$

$$\frac{d\Delta\vec{v}_i(t)}{dt} = \frac{1}{C_f}\Delta\vec{i}_{si}(t) - j\omega_i\Delta\vec{v}_i(t) - \frac{1}{C_f}\Delta\vec{i}_i(t) \quad (6.6)$$

$$\frac{d\Delta\vec{i}_{Lf}(t)}{dt} = \frac{R_d}{L_f}\Delta\vec{i}_{si}(t) - \left(\frac{R_d}{L_f} + j\omega_i\right)\Delta\vec{i}_{Lf}(t) \quad (6.7)$$

$$\frac{d\Delta\vec{v}_{if}(t)}{dt} = \frac{1}{\tau}\Delta\vec{v}_i(t) - \frac{1}{\tau}\Delta\vec{v}_{if}(t) \quad (6.8)$$

by decomposing the small-signal equations (6.5) and (6.7) into d-q components:

$$\begin{aligned}
&\frac{d\Delta i_{si(d)}(t)}{dt} = \\
&\frac{1}{L_s}\Delta v_{si(d)}(t) - \frac{R_s + R_d}{L_s}\Delta i_{si(d)}(t) + \omega_i\Delta i_{si(q)}(t) - \frac{1}{L_s}\Delta v_{i(d)}(t) + \frac{R_d}{L_s}\Delta i_{Lf(d)}(t) \\
&\frac{d\Delta i_{si(q)}(t)}{dt} = \\
&\frac{1}{L_s}\Delta v_{si(q)}(t) - \frac{R_s + R_d}{L_s}\Delta i_{si(q)}(t) - \omega_i\Delta i_{si(d)}(t) - \frac{1}{L_s}\Delta v_{i(q)}(t) + \frac{R_d}{L_s}\Delta i_{Lf(q)}(t)
\end{aligned} \quad (6.9)$$

$$\begin{aligned}
\frac{d\Delta i_{Lf(d)}(t)}{dt} &= \frac{R_d}{L_f}\Delta i_{si(d)}(t) - \frac{R_d}{L_f}\Delta i_{Lf(d)}(t) + \omega_i\Delta i_{Lf(q)}(t) \\
\frac{d\Delta i_{Lf(q)}(t)}{dt} &= \frac{R_d}{L_f}\Delta i_{si(q)}(t) - \frac{R_d}{L_f}\Delta i_{Lf(q)}(t) - \omega_i\Delta i_{Lf(d)}(t)
\end{aligned} \quad (6.10)$$

The modulation vector is defined in such a way that the input current vector is in phase with the filtered input voltage vector [72] [89]:

$$\vec{\psi}(t) = \vec{v}_{if}(t)e^{-j\varphi_i} \quad (6.11)$$

$$\varphi_i = 0 \qquad \Rightarrow \qquad \vec{\psi}(t) = \vec{v}_{if}(t) \quad (6.12)$$

Now $m_d(t)$ and $m_i(t)$ are defined as follows to show the relationship between the filtered input voltage vector $\vec{v}_{if}(t)$ and output reference voltage vector $\vec{v}_{or}(t)$ [103,

106]:

$$\vec{m}_d(t) = \frac{\vec{v}_{or}(t)}{3\vec{v}^*_{if}(t)} \tag{6.13}$$

$$\vec{m}_i(t) = \frac{\vec{v}^*_{or}(t)}{3\vec{v}^*_{if}(t)} \tag{6.14}$$

The small-signal equations can be linearised around the steady-state operating point as follows:

$$\begin{aligned} \Delta\vec{m}_d(t) &= \frac{1}{3}\frac{\Delta\vec{v}_{or}(t)\vec{V}^*_{if} - \vec{V}_{or}\Delta\vec{v}^*_{if}(t)}{(\vec{V}^*_{if})^2} \\ \Delta\vec{v}_{or}(t) &= 0 \quad and \quad \vec{V}_{or} = qV_{im} \\ \Delta\vec{m}_d(t) &= -\frac{q}{3V_{im}}\Delta\vec{v}^*_{if}(t) \end{aligned} \tag{6.15}$$

$$\begin{aligned} \Delta\vec{m}_i(t) &= \frac{1}{3}\frac{\Delta\vec{v}^*_{or}(t)\vec{V}^*_{if} - \vec{V}^*_{or}\Delta\vec{v}^*_{if}(t)}{(\vec{V}^*_{if})^2} \\ \Delta\vec{v}^*_{or}(t) &= 0 \quad and \quad \vec{V}^*_{or} = qV_{im} \\ \Delta\vec{m}_i(t) &= -\frac{q}{3V_{im}}\Delta\vec{v}^*_{if}(t) \end{aligned} \tag{6.16}$$

Now using (6.15) and (6.16) the small signal equations of the output voltage and input current space vectors and their d-q components are obtained as follows:

$$\begin{aligned} \Delta\vec{v}_o(t) &= \frac{3}{2}\left[\Delta\vec{v}_i(t)\vec{M}^*_i + \Delta\vec{v}^*_i(t)\vec{M}_d + V_{im}\Delta\vec{m}^*_i(t) + V_{im}\Delta\vec{m}_d(t)\right] \\ &= \frac{q}{2}\Delta\vec{v}_i(t) + \frac{q}{2}\Delta\vec{v}^*_i(t) - \frac{q}{2}\Delta\vec{v}_{if}(t) - \frac{q}{2}\Delta\vec{v}^*_{if}(t) \end{aligned} \tag{6.17}$$

$$\begin{aligned} \Delta\vec{i}_i(t) &= \frac{3}{2}\left[\Delta\vec{i}_o(t)\vec{M}_i + \Delta\vec{i}^*_o(t)\vec{M}_d + \vec{I}_o\Delta\vec{m}_i(t) + \vec{I}^*_o\Delta\vec{m}_d(t)\right] \\ &= \frac{q}{2}\Delta\vec{i}_o(t) + \frac{q}{2}\Delta\vec{i}^*_o(t) - \frac{q^2}{2\vec{Z}_l}\Delta\vec{v}^*_{if}(t) - \frac{q^2}{2\vec{Z}^*_l}\Delta\vec{v}^*_{if}(t) \\ &= \frac{q}{2}\Delta\vec{i}_o(t) + \frac{q}{2}\Delta\vec{i}^*_o(t) - \frac{q^2R_l}{|\vec{Z}_l|^2}\Delta\vec{v}^*_{if}(t) \end{aligned} \tag{6.18}$$

$$\begin{aligned} \Delta v_{o(d)}(t) &= q\Delta v_{i(d)}(t) - q\Delta v_{if(d)}(t) \\ \Delta v_{o(q)}(t) &= 0 \end{aligned} \tag{6.19}$$

$$\begin{aligned}\Delta i_{i(d)}(t) &= q\Delta i_{o(d)}(t) - \frac{q^2 R_l}{|\vec{Z}_l|^2}\Delta v_{if(d)}(t)\\ \Delta i_{i(q)}(t) &= \frac{q^2 R_l}{|\vec{Z}_l|^2}\Delta v_{if(q)}(t)\end{aligned} \tag{6.20}$$

Finally, the state equations can be obtained as:

$$\begin{aligned}\frac{d\Delta v_{i(d)}(t)}{dt} &= \frac{1}{C_f}\Delta i_{si(d)}(t) + \omega_i \Delta v_{i(q)}(t) - \frac{q}{C_f}\Delta i_{o(d)}(t) + \frac{q^2 R_l}{C_f|\vec{Z}_l|^2}\Delta v_{if(d)}(t)\\ \frac{d\Delta v_{i(q)}(t)}{dt} &= \frac{1}{C_f}\Delta i_{si(q)}(t) - \omega_i \Delta v_{i(d)}(t) - \frac{q^2 R_l}{C_f|\vec{Z}_l|^2}\Delta v_{if(q)}(t)\end{aligned} \tag{6.21}$$

$$\begin{aligned}\frac{d\Delta i_{o(d)}(t)}{dt} &= \frac{q}{L_l}\Delta v_{i(d)}(t) - \frac{R_l}{L_l}\Delta i_{o(d)}(t) + \omega_o \Delta i_{o(q)}(t) - \frac{q}{L_l}\Delta v_{if(d)}(t)\\ \frac{d\Delta i_{o(q)}(t)}{dt} &= -\omega_o \Delta i_{o(d)}(t) - \frac{R_l}{L_l}\Delta i_{o(q)}(t)\end{aligned} \tag{6.22}$$

$$\begin{aligned}\frac{d\Delta v_{if(d)}(t)}{dt} &= \frac{1}{\tau}\Delta v_{i(d)}(t) - \frac{1}{\tau}\Delta v_{if(d)}(t)\\ \frac{d\Delta v_{if(q)}(t)}{dt} &= \frac{1}{\tau}\Delta v_{i(q)}(t) - \frac{1}{\tau}\Delta v_{if(q)}(t)\end{aligned} \tag{6.23}$$

The state space equation of the small-signal model of the system is as following:

$$\frac{d\Delta X_c}{dt} = A_c \Delta X_c \tag{6.24}$$

where X_c and A_c are defined as:

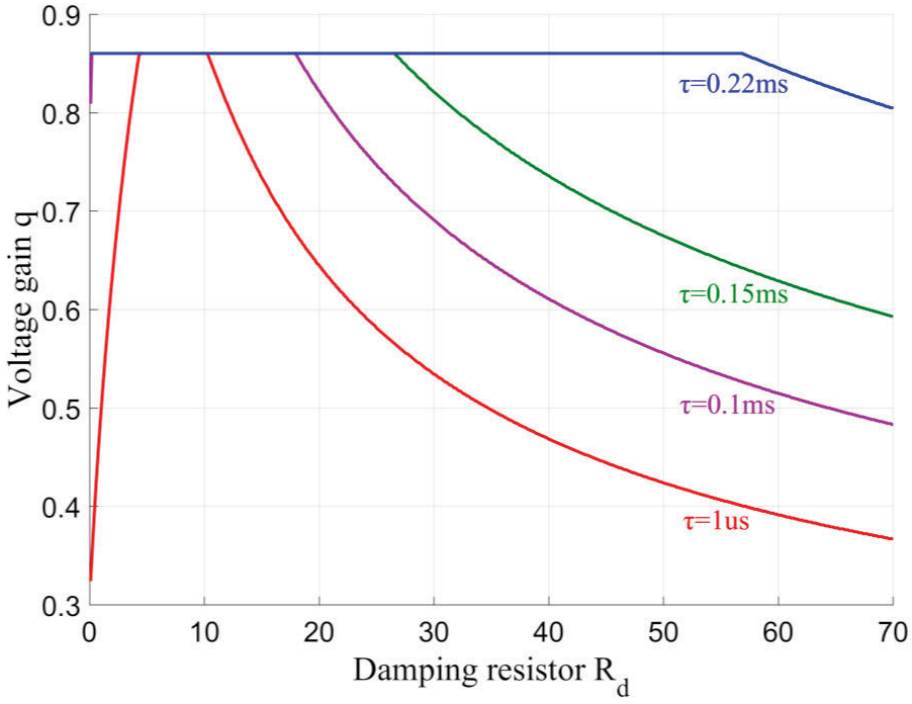
$$X_c = \begin{bmatrix} i_{si(d)} & i_{si(q)} & v_{i(d)} & v_{i(q)} & i_{Lf(d)} & i_{Lf(q)} & v_{if(d)} & v_{if(q)} & i_{o(d)} & i_{o(q)} \end{bmatrix}^T \tag{6.25}$$

$$A_c = \begin{bmatrix} k & \omega_i & -\frac{1}{L_s} & 0 & \frac{R_d}{L_s} & 0 & 0 & 0 & 0 & 0 \\ -\omega_i & k & 0 & -\frac{1}{L_s} & 0 & \frac{R_d}{L_s} & 0 & 0 & 0 & 0 \\ \frac{1}{C_f} & 0 & 0 & \omega_i & 0 & 0 & k_1 & 0 & -\frac{q}{C_f} & 0 \\ 0 & \frac{1}{C_f} & -\omega_i & 0 & 0 & 0 & 0 & -k_1 & 0 & 0 \\ \frac{R_d}{L_f} & 0 & 0 & 0 & -\frac{R_d}{L_f} & \omega_i & 0 & 0 & 0 & 0 \\ 0 & \frac{R_d}{L_f} & 0 & 0 & -\omega_i & -\frac{R_d}{L_f} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{\tau} & 0 & 0 & 0 & -\frac{1}{\tau} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{\tau} & 0 & 0 & 0 & -\frac{1}{\tau} & 0 & 0 \\ 0 & 0 & \frac{q}{L_l} & 0 & 0 & 0 & -\frac{q}{L_l} & 0 & -\frac{R_l}{L_l} & \omega_o \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\omega_o & -\frac{R_l}{L_l} \end{bmatrix} \tag{6.26}$$

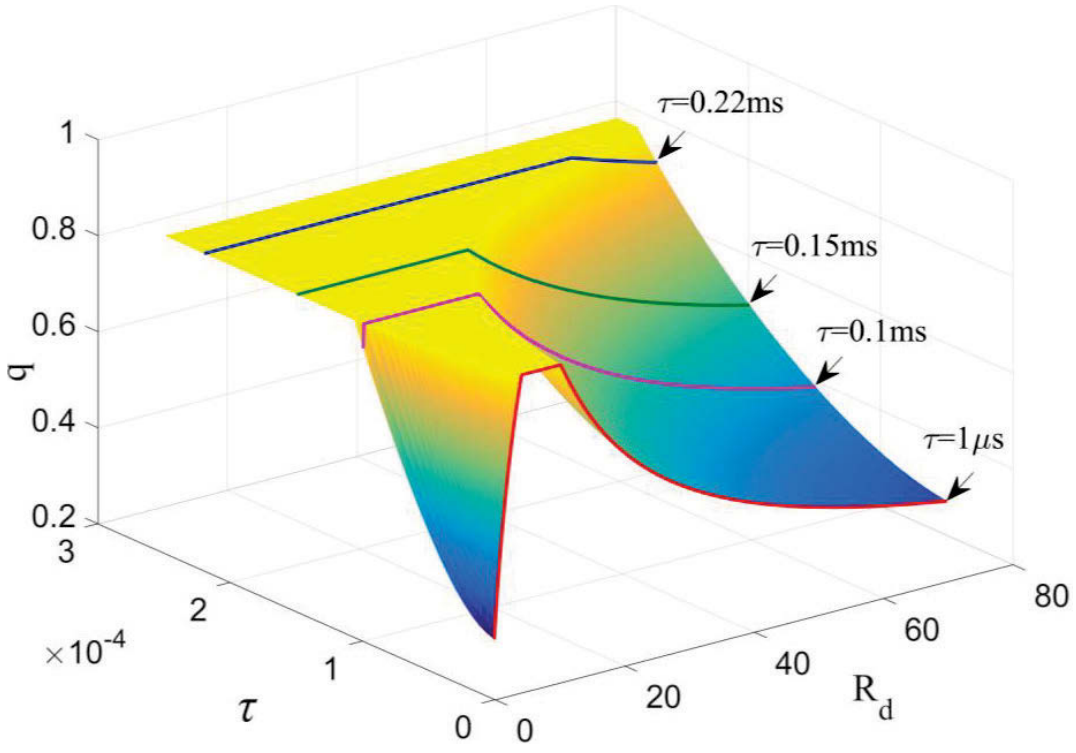
where k and k_1 are as following:

$$\begin{aligned} k &= -\frac{R_s + R_d}{L_s} \\ k_1 &= \frac{q^2 R_l}{C_f |\vec{Z}_l|^2} \end{aligned} \tag{6.27}$$

By analyzing the eigenvalues of matrix A_c, the stability limit of the system can be find like the previous chapter, and the results are illustrated in the following figures. Figures 6.10 and 6.11 show the effects of the damping resistor and digital filter time constant on the stability of the system. The parameters of the system are presented in Table 6.3. Adding the damping resistors causes the required τ to be small. For each particular value of τ, there is a range of R_d which keeps the system stable for any voltage gain. Therefore, it is possible to increase the damping resistance by using a digital filter with smaller time constant τ. For example, when $\tau = 0.22ms$ the appropriate range of R_d is up to 55Ω while for $\tau = 1\mu s$ the damping resistor can be selected between about 5Ω to 10Ω. In the next sections, unidirectional and bidirectional power-flow control is presented which for stabilisation of the system the illustrated strategies is applied, and the results are compared.



(a)



(b)

Figure 6.10: Stable region of the DMC system, voltage gain 'q' against R_d, where a) For different values of τ, and b) 3D graph of the case (a)

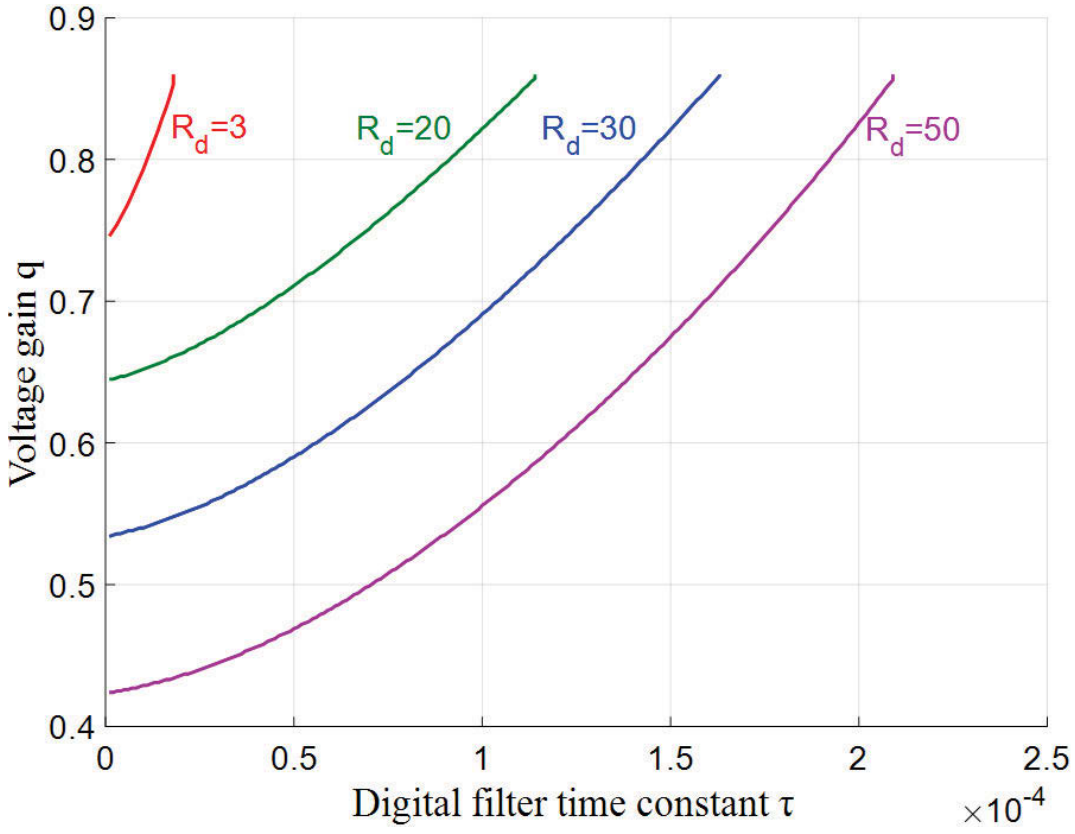


Figure 6.11: Stable region of the DMC system, voltage gain 'q' against digital filter time constant τ for different values of damping resistor R_d

6.3 Unidirectional Power Flow Control

When the three-phase input source and output load are symmetrical and balanced, the instantaneous apparent power in the d-q coordinate system is:

$$S = V.I^* = (V_d + jV_q)(I_d - jI_q) \tag{6.28}$$

The active and reactive powers P and Q which are the real and imaginary parts of the apparent power can be obtained as follows:

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} V_d & V_q \\ V_q & -V_d \end{bmatrix} \times \begin{bmatrix} I_d \\ I_q \end{bmatrix} \tag{6.29}$$

As the source voltage is balanced and symmetrical, with considering its space vector along the d axis, $V_q = 0$, and therefore:

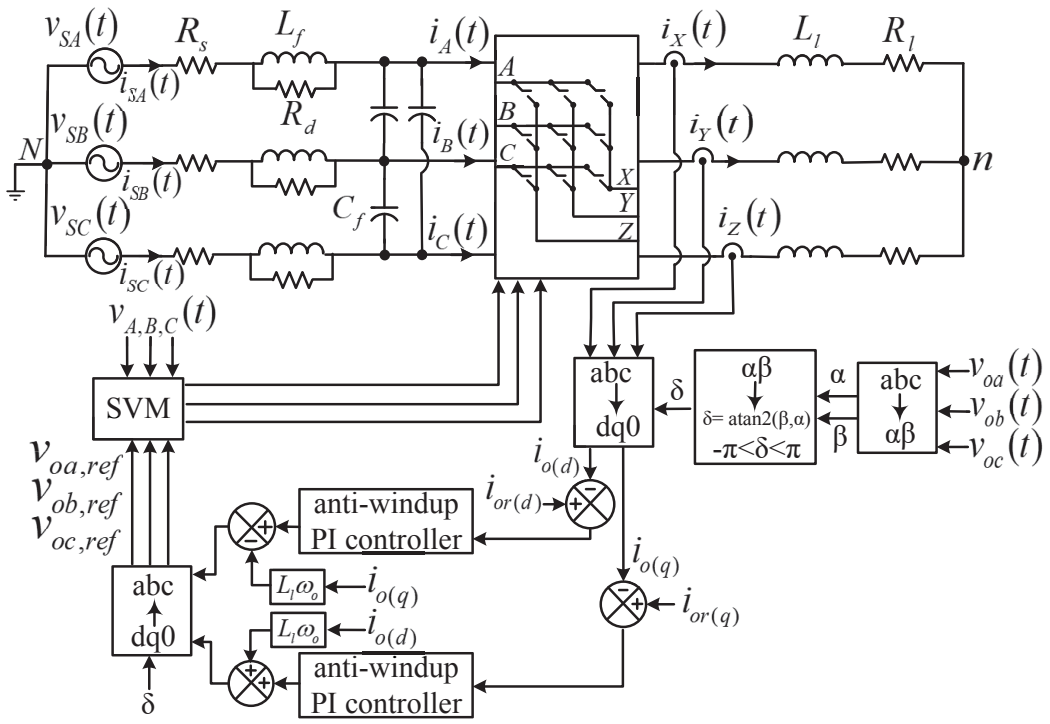


Figure 6.12: Unidirectional output power control using the voltage oriented control

$$P = V_d I_d \tag{6.30}$$

$$Q = -V_d I_q \tag{6.31}$$

It means that in purpose of controlling the active and reactive power and power flow direction, I_d and I_q should be controlled. Figure 6.12 illustrates the closed-loop output current control that is investigated for controlling the output power delivered to a star-connected three-phase RL load.

Digital implementation and discrete nature of PWM is accounted for in the simulation by adding the Zero-Order-Hold (ZOH) blocks. Also, the additional delay caused by the digital controller can be considered using a unit delay (z^{-1}) [108].

Table 6.2: The results of the unidirectional power flow for different values of R_d (switching pattern with one zero vector)

	$R_d = 5\Omega$		$R_d = 8\Omega$		$R_d = 10\Omega$	
$i_{x,peak}$	17A	24A	17A	24A	17A	24A
$THD(i_x)\%$	2.38	1.13	2.33	1.2	2.34	1.2
$THD(i_{sA})\%$	3.25	2.05	3.02	2.38	3	2.62
PF_{in}	0.986	0.999	0.986	0.999	0.986	0.999

6.3.1 Unidirectional power flow control with damping resistor R_d

As illustrated before in Figure 6.2, for maximum voltage gain, R_d should be approximately between 5Ω to 10Ω. Table 6.2 illustrates the results of THDs of the input and output currents, and the input power factor for three different values of R_d and two output currents. As can be seen, in this range of resistance, for higher current (24A) and as a result, for higher voltage gain, PF_{in} and THD of the input and output currents are better than the results for 17A. Although the results for all three selected resistances are very close, larger damping resistance improves the THD of the input current for lower currents slightly, while for higher currents the result is the opposite. So it is logical to select a resistance in the middle of the range like 8Ω. The d-q components of the output current as the reference, are adjusted on $i_{x(q)} = 0$ and $i_{x(d)}$ steps up from 17A to 24A.

Figure 6.13 shows that without damping resistor R_d, system is unstable while in Figure 6.14 with $R_d = 5\Omega$ it stays stable.

In the case of switching pattern with three zeros, as it can be seen in Figure 6.15, for example, using the damping resistor $R_d = 8\Omega$ results in instability in the system, but anti-windup PI controller makes it stable again. Also, the results for three zero switching pattern when $R_d = 5\Omega$ with a normal PI controller is shown in Figure 6.16. As a result, anti-windup PI controller does not have any effect on the THD of the currents, but in some cases, it helps the system to remain stable, so anti-windup PI controller is a better choice for stability problem.

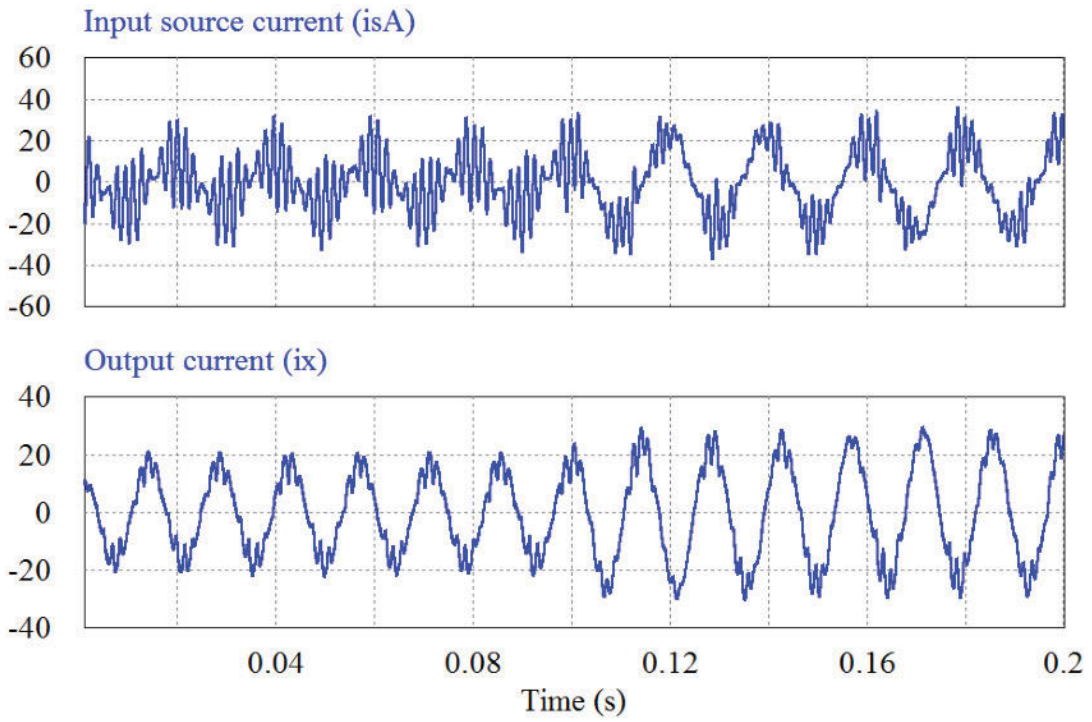


Figure 6.13: Waveforms of the input source current and the output current for the unidirectional power flow, without applying any stabilisation method

Table 6.3: Matrix converter system parameters for stability analysis

Input source	Input filter	Output load	Frequencies
$V_{si} = 400V(ll, rms)$	$C_f = 6.6\mu F$	$R_l = 10\Omega$	$f_i = 50Hz$
$L_s = 0.4mH$	$L_f = 3mH$	$L_l = 6mH$	$f_o = 70Hz$
$R_s = 0.5\Omega$			$f_s = 10kHz$

Comparison between Figures 6.14 and 6.16 shows that for lower voltage gains the switching pattern with three zero vectors causes less THD for the output current but the results for the input current is opposite.

6.3.2 Unidirectional power flow control with digital input filter

According to Figure 6.6, for the system parameters mentioned in Table 6.3, digital filter time constant τ should be about 0.35 ms to system stays stable for maximum voltage gain. However, as it can be seen in Figure 6.17a, the system is unstable

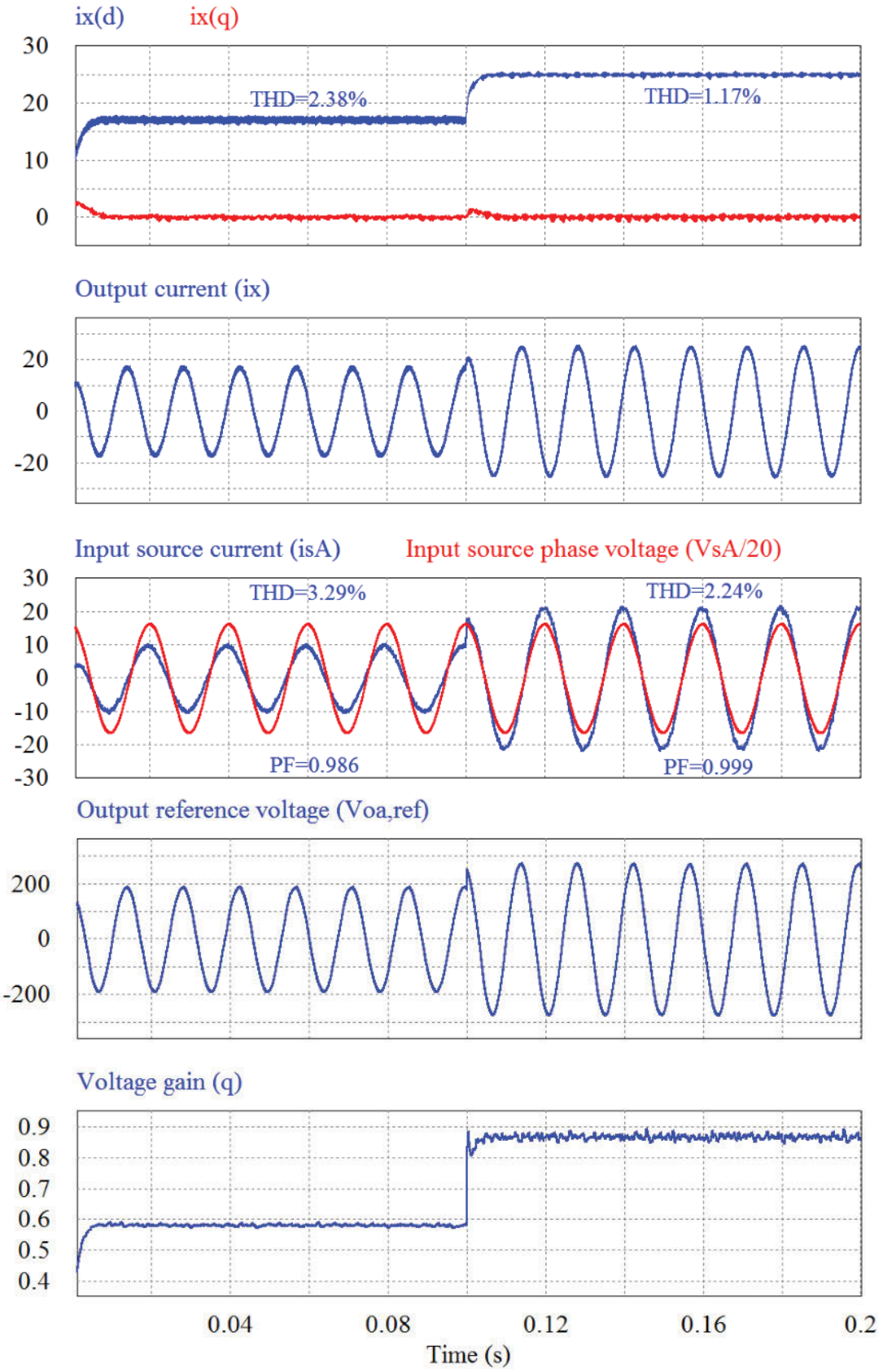


Figure 6.14: The input and output waveforms for unidirectional power flow control with $R_d = 5\Omega$

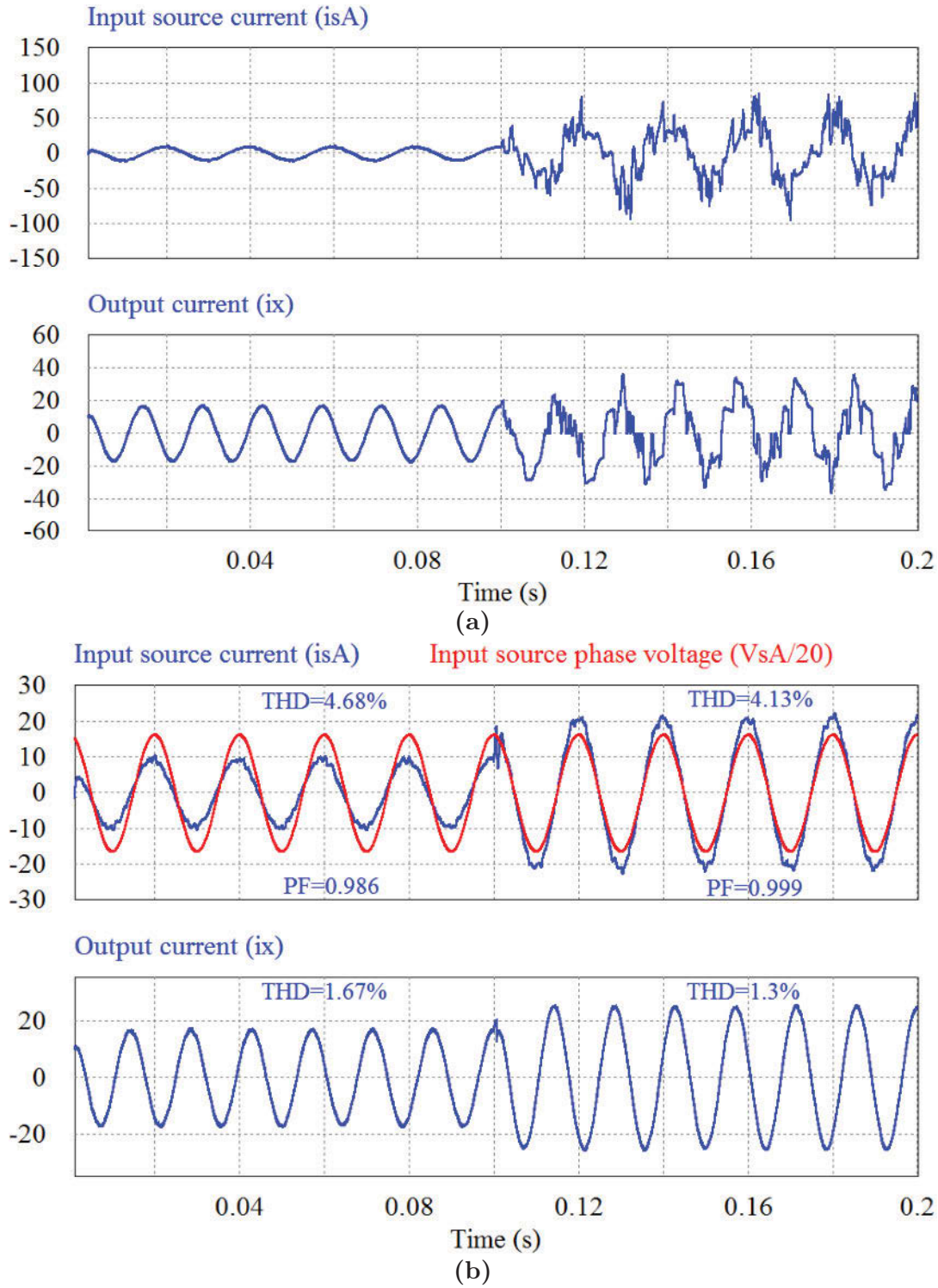


Figure 6.15: Waveforms of the input source current and the output current for the unidirectional power flow control, with $R_d = 8\Omega$ and switching pattern using three zero vectors, where a) With normal PI controller, and b) With anti-windup PI controller

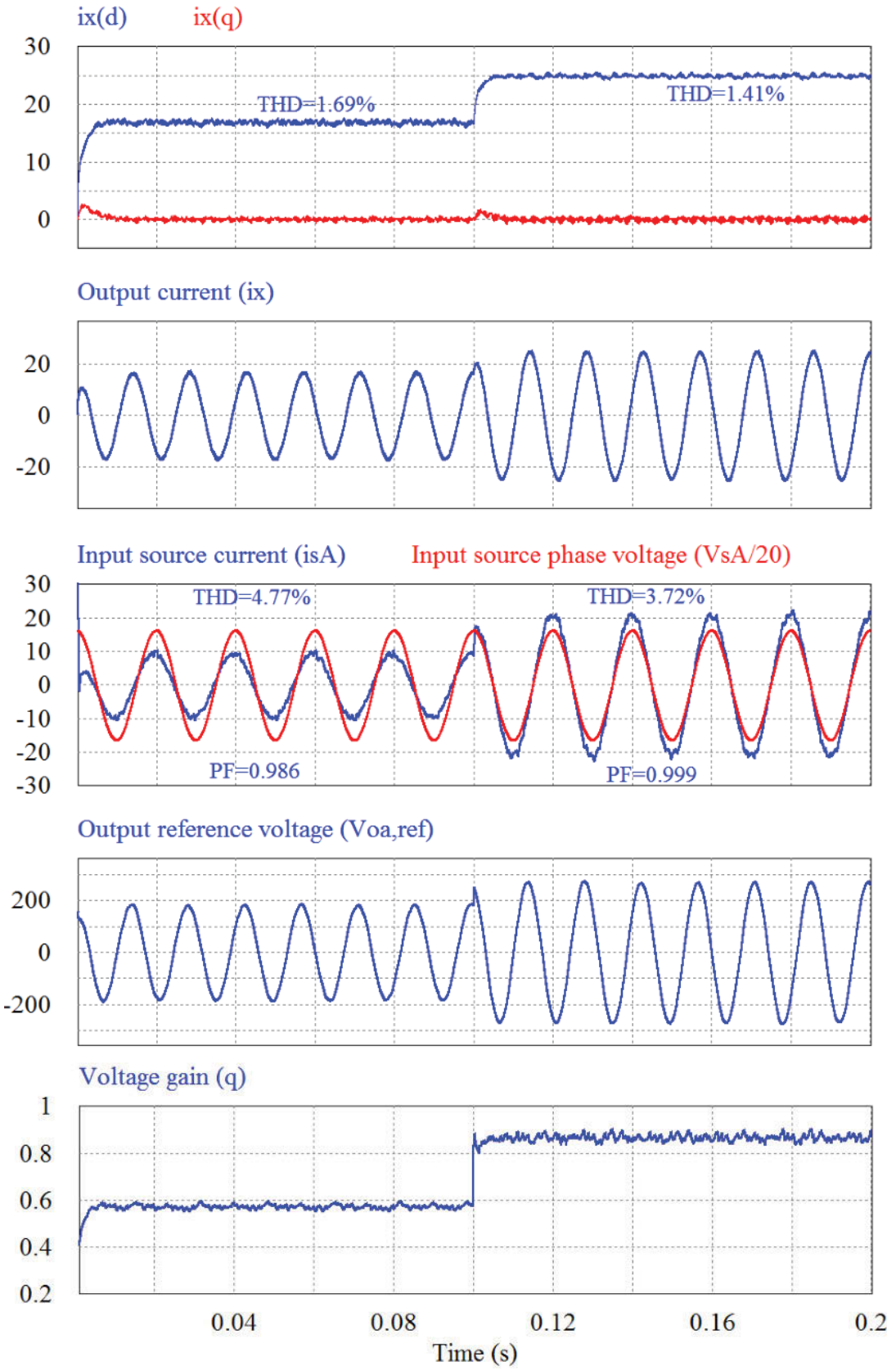


Figure 6.16: The input and output waveforms for unidirectional power flow control with $R_d = 5\Omega$, switching pattern using three zero vectors and conventional PI controllers

for lower voltage gain. On the other hand, Figure 6.17b shows that with the same conditions for switching frequency $f_s = 5kHz$, the system stays stable although THDs of the currents are high. Increasing the filter time constant to 0.5ms causes better results as illustrated in Figure 6.17c, but the larger time constant does not improve the results for the whole range of voltage gain. Also, high values of τ cause the input disturbances to transfer to the output side [103].

6.3.3 Unidirectional power flow control with a combination of the damping resistor and digital input filter

Comparing the results of the two methods mentioned above shows that the damping resistor solution provides better results in the case of THD of the input and output currents and the transient oscillations. However, damping resistor causes power loss while digital filter does not have this disadvantage, and when the damping resistor is small, the power loss will increase because a portion of the input current flows through the damping resistor. Figure 6.19a illustrates the waveform of the current in one of the damping resistors, and the instantaneous and average power loss when $R_d = 5\Omega$. In this case, the power loss for the three damping resistors is about 25.5 W and 116 W for output currents 17A and 24A respectively.

In order to reduce the power loss, damping resistors have to be increased and to solve the stability problem, one solution is a combination of the damping resistor and the digital filter. According to Figure 6.11, for the maximum voltage gain, the time constant about $\tau = 0.21ms$ is needed when $R_d = 50\Omega$. Although the system stays stable for this time constant of the digital filter, by increasing the time constant, THD of the input current is reduced. Figure 6.19b shows the damping resistor current and the power loss caused by one $R_d = 50\Omega$ when the digital filter time constant is $\tau = 0.5ms$. The other results have been shown in Figure 6.18 in order to compare the results when only the damping resistor is utilised or when only the digital filter is used. The combination of the damping resistor and the digital filter provides better results in the case of stability, power loss and transient

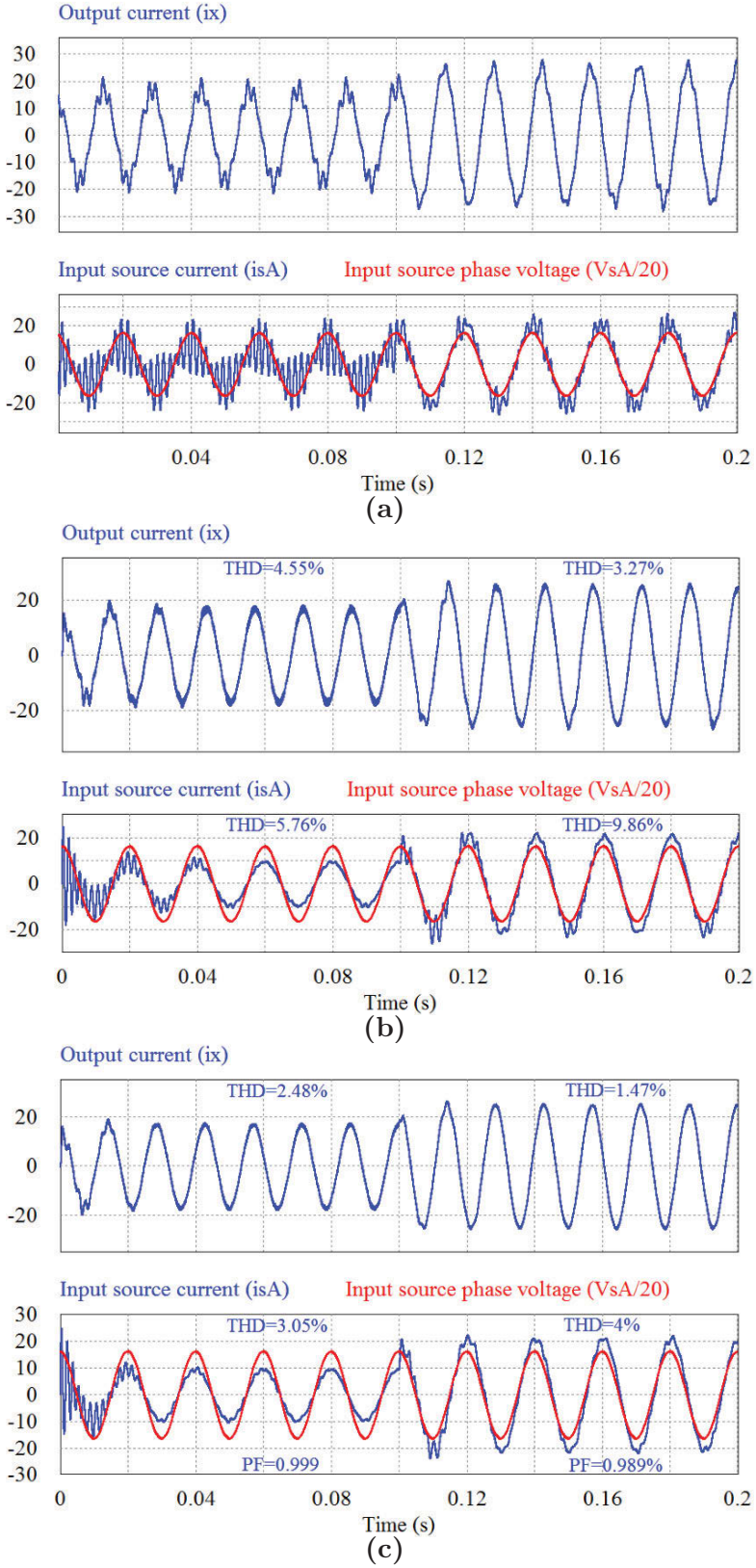


Figure 6.17: Waveforms of the output and input source currents for unidirectional power flow control with switching pattern using one zero vector and digital filter with time constant, where a) $\tau = 0.35ms$, switching frequency $f_s = 10kHz$, b) $\tau = 0.35ms$ and switching frequency $f_s = 5kHz$, and c) $\tau = 0.5ms$ and switching frequency $f_s = 10kHz$

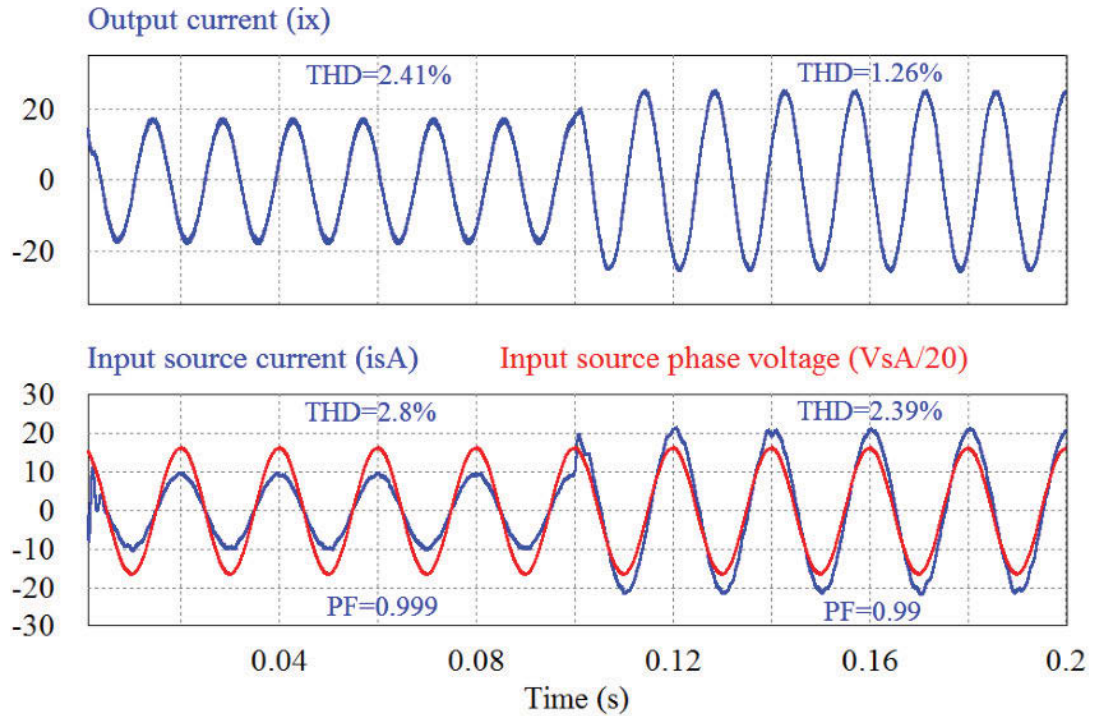


Figure 6.18: Waveforms of the output and input source currents for unidirectional power flow control with switching pattern using one zero vector, damping resistor $R_d = 50\Omega$ and the digital filter time constant $\tau = 0.5ms$

oscilations.

6.3.4 Experimental results for unidirectional active power flow control

The power flow control and the stability improvement approaches are verified on a 7.5kW three-phase DMC, with a switching frequency 10 kHz. Figure 6.20 shows the control results of the output current when the output reference current $i_{or(d)}$ steps from 4A to 7A and the damping resistor is $R_d = 5\Omega$. Also, Figure 6.21 presents the same results for the damping resistor $R_d = 47\Omega$ and a digital input filter with the time constant $0.5ms$. The load is a star connected R-L with $R_l = 12\Omega$ and $L_l = 6mH$, and the input filter parameters are $C_f = 6.6\mu F$, $L_f = 3mH$. In order to show the phase difference between the output current and the output reference voltage, the input source is used as the output reference voltage as well. As can be seen, when $i_{or(q)} = 0$ and $i_{or(d)}$ steps from 4A to 7A, the output current and reference voltage are in phase which means that the output power has been controlled to be

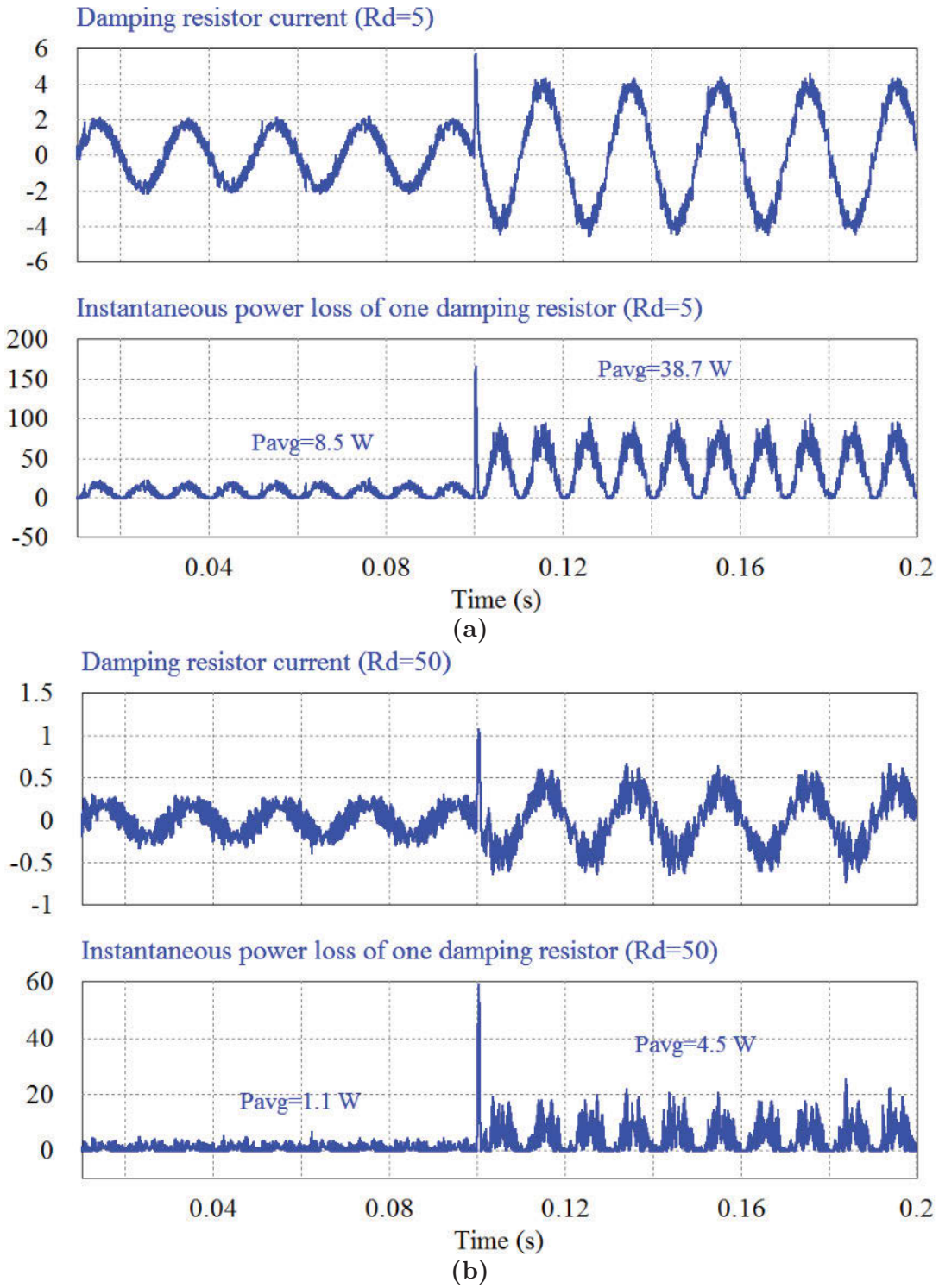


Figure 6.19: Waveforms of the current and instantaneous power loss in a damping resistor for the unidirectional active power-flow control, where a) Using only the damping resistor, $R_d = 5\Omega$, and b) Using the damping resistor $R_d = 50\Omega$ and digital filter $\tau = 0.5ms$

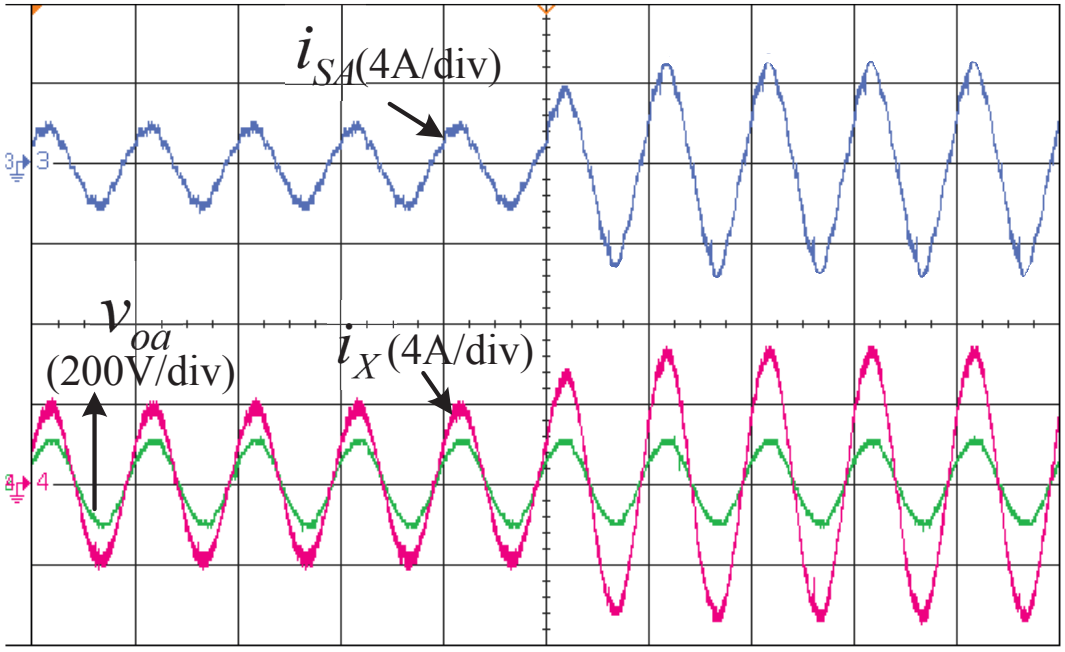


Figure 6.20: Experimental results for unidirectional active power flow control with $R_d = 5\Omega$, $ior(q) = 0$ and $ior(d)$ steps up from 4A to 7A

completely active. Another oscilloscope Tektronix DPO2024 is used for collecting the data of the waveforms and the data is processed using PSIM. For both of the damping resistors, the system is stable, and the THDs of the input and output currents are very close. For the output reference current $i_{or(d)} = 7A$, the measured THD of the output current is around 2% for both of the damping resistors, and the input current THD is about 6%. The experimental results confirm the simulation results that increasing the damping resistor along with the input digital filter can reduce the power loss while does not affect the THD.

6.4 Bidirectional Power Flow Control

Electricity generated by a micro-grid can have variable frequency and amplitude, and for exchanging the power with the utility grid, a power conditioning converter is needed to meet the required amplitude and frequency. As illustrated in Figure 6.22, DMC can be considered as an interface between the main grid and a micro-grid. In this figure the three-phase sources V_s and V_o represents the main grid and

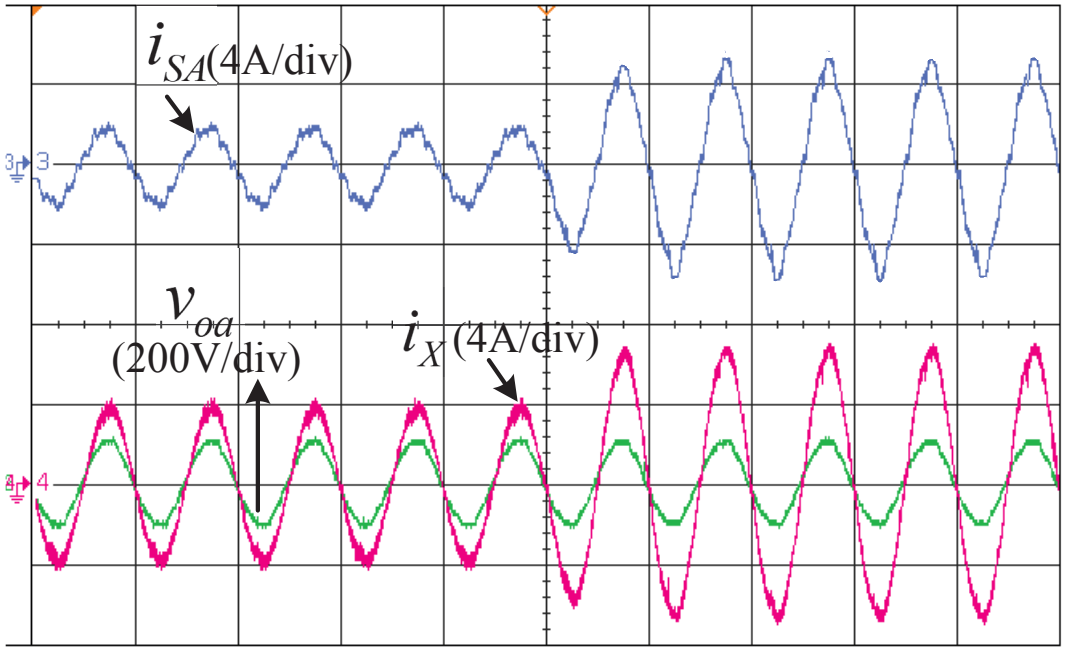


Figure 6.21: Experimental results for unidirectional active and reactive power flow, with $R_d = 47\Omega$ and $\tau = 0.5ms$, where a) $ior(q) = 0$ and $ior(d)$ changes from 4A to 7A, and b) $ior(d) = 0$ and $ior(q)$ changes from 4A to 7A

Table 6.4: System parameters for bidirectional power flow control

Input source voltage	400V, $f_i = 50Hz$
Output source voltage	230V, $f_o = 70Hz$
Input line impedance	$L_s = 0.4mH, R_s = 0.5\Omega$
Input filter	$L_f = 0.6mH, C_f = 12.6\mu F$
Switching frequency	$f_s = 10kHz$
output filter	$L_l = 6mH$
Simulation time step	$1\mu s$

microgrid respectively. In general, a PWM rectifier followed by a PWM inverter including a dc-link or a back-to-back voltage source converter are utilised for this purpose. In order to eliminate the use of an energy storage element as the dc-link and increase the converter lifetime and to have a more compact converter, a MC can be utilised instead of the conventional converters.

On the other hand, to have the needed output active and reactive power in both directions, the stability problem must be considered especially for the maximum output power. As the output of the MC is connected to a voltage source with

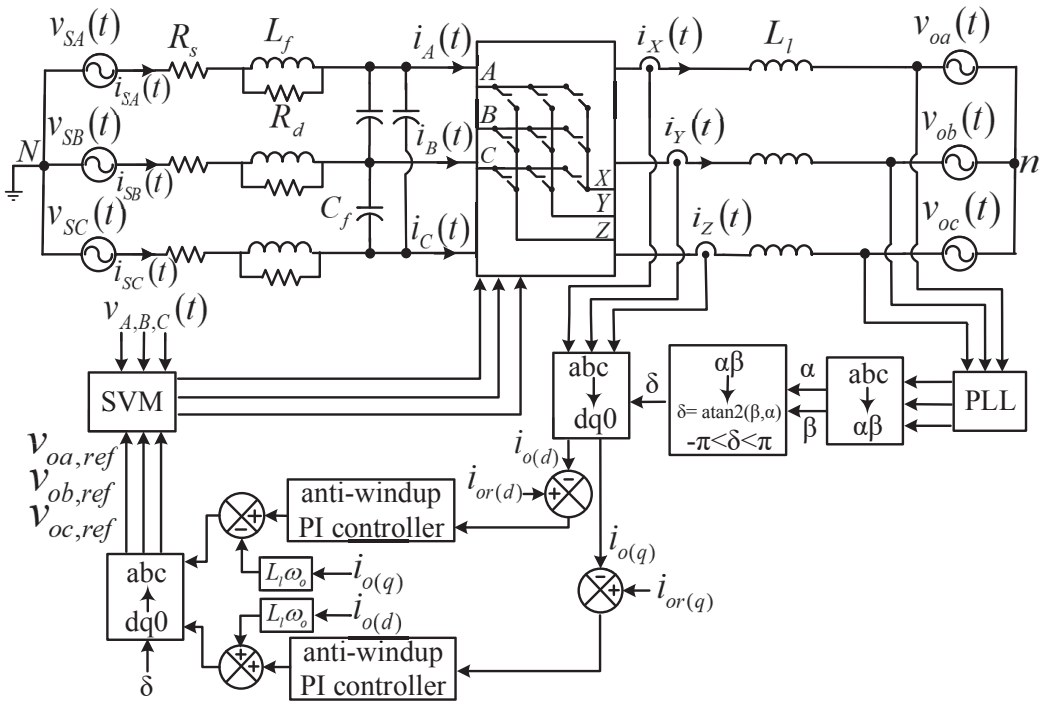


Figure 6.22: Bidirectional active and reactive output power flow control using the VOC method

the almost zero impedance, stabilisation of the system is more difficult. The main goals of the investigation are the stability of the system for maximum voltage gain, power-up performance of the system, reduction of the THD of the input and output currents, and input power factor close to unity. In this section, the three methods for stabilisation of the MC and their performances are analyzed. In all the methods, in the case of the bidirectional active power flow, the output current ($i_{or(d)}$) increases from 16A to 51A from input to the output side, and 16A to 80A from output to the input side. For the reactive power control, ($i_{or(q)}$) increases from 16A to 32A from the input to the output and from 16A to 48A from the output to the input. The system parameters are presented in Table 6.4.

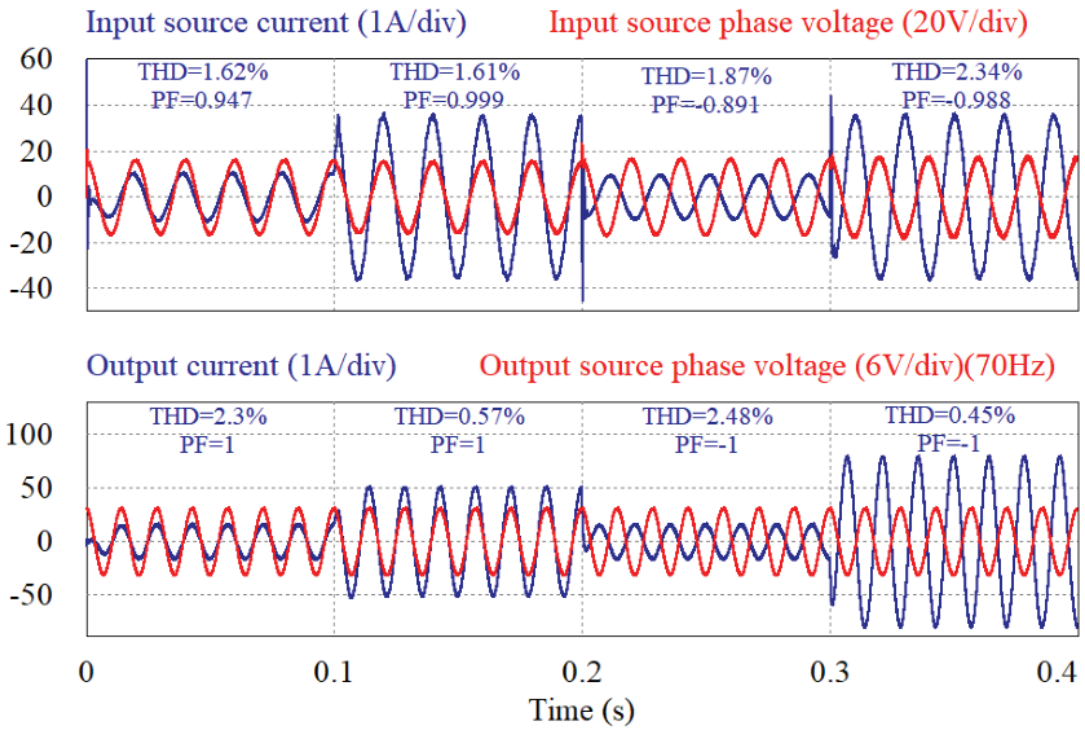


Figure 6.23: Waveforms of the input source current and output current for bidirectional active power-flow with $R_d = 3\Omega$

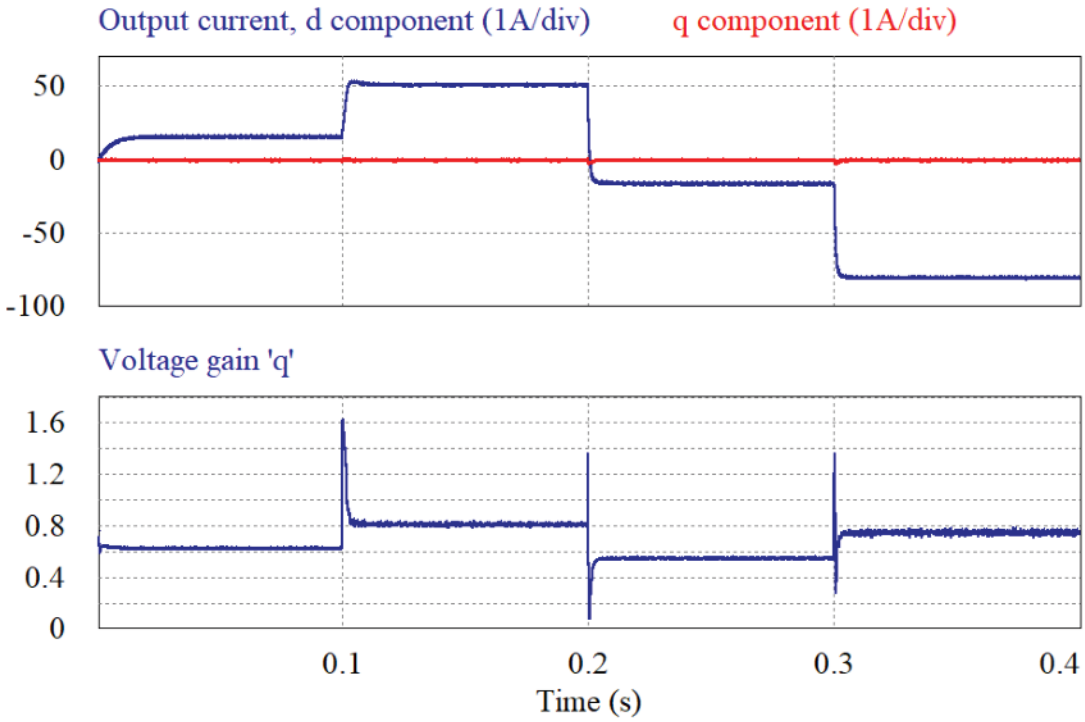


Figure 6.24: d-q components of the output current and voltage gain for bidirectional active power-flow, with $R_d = 3\Omega$

6.4.1 Bidirectional power flow control with damping resistor R_d

In damping resistor method, for the system parameters presented in Table 6.4, the damping resistors should be decreased to $R_d = 3\Omega$ for lower THD of the input current. The simulation results of the input source current and the output current shown in Figure 6.23 illustrates the system performance when the active power flows in both directions. During the time 0-0.2s the active power flows from the input to the output side and during the interval 0.2–0.4s it flows in the opposite direction from the output to the input. In fact for controlling the active power, the d component of the output reference current ($i_{or(d)}$) is controlled. As can be seen in Figure 6.24, $i_{or(d)}$ is set to be $16A$ before $t = 0.1s$ and during the interval 0.1-0.2s is changed to 51 A to control the active power from the input to the output. Then $i_{or(d)}$ is set to be -16A and steps up to -80A during the times 0.2-0.3s and 0.3-0.4s respectively to control the active power from the output to the input side. These currents are selected to show the MC behaviour in different voltage gains as presented in Figure 6.24. It can be seen that the input and output currents follow the references quickly, and THD of the input and output currents are in the acceptable range. The applied PI controllers are anti-windup PI controllers and the limiters help the system to remain stable and also by selecting the appropriate upper and lower limits, it reduces the overshoot at the step change time.

In the simulation circuit, the parameters of the IGBT switches match the parameters of the physical devices. Figure 6.26 presents the sent and received active power from the two sources. It is obvious that the absorbed power is less than the generated power by each of the voltage sources because of the resistances and switching loss. Figure 6.27 shows the current and the instantaneous and average power in one of the damping resistors.

For controlling the reactive output power, $i_{or(q)}$ is adjusted to step from 16A to 32A at $t = 0.1s$ for reactive power flow control from input to the output, and then

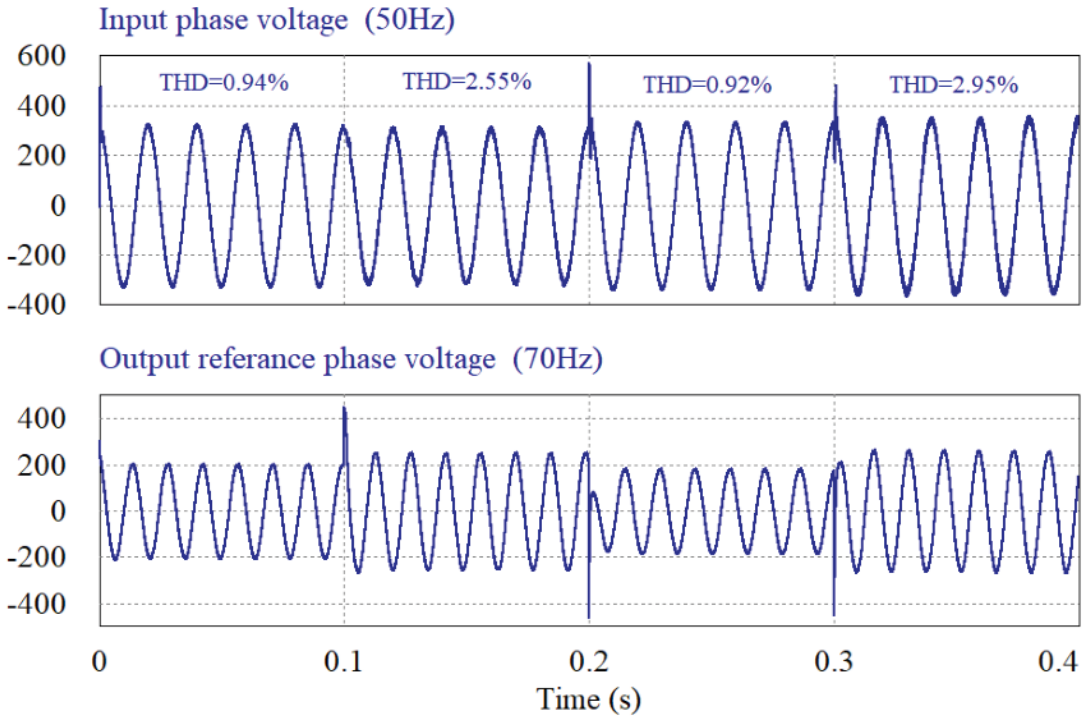


Figure 6.25: Waveforms of the input voltage and output reference voltage for bidirectional active power-flow, with $R_d = 3\Omega$

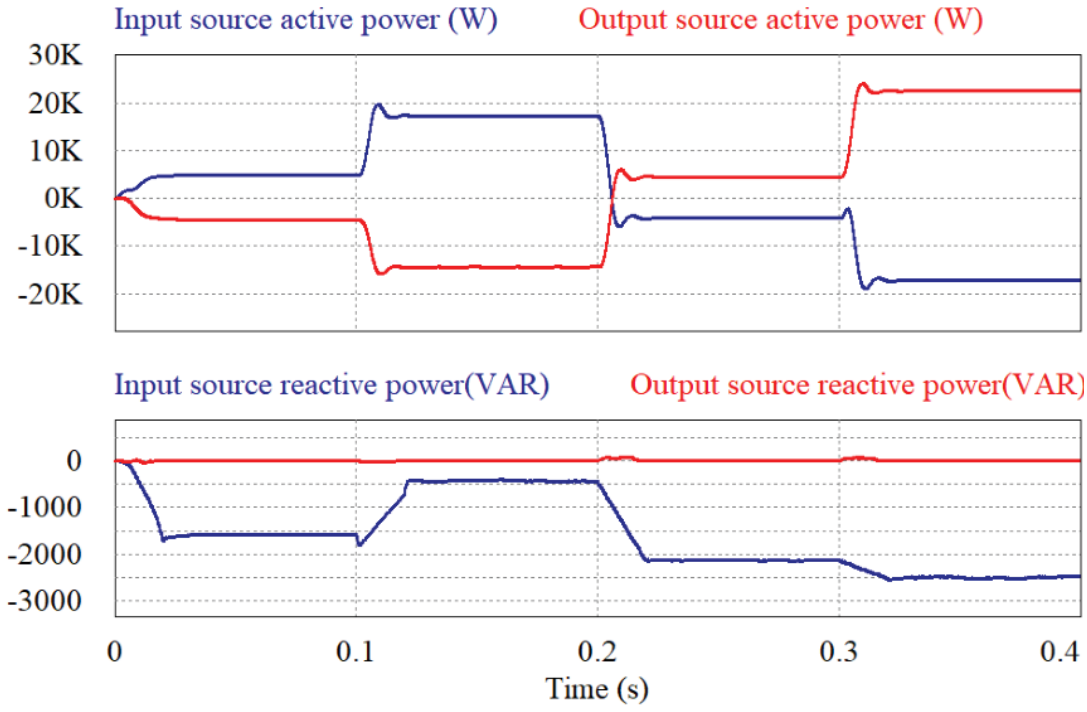


Figure 6.26: The input and output sources active and reactive powers for bidirectional active power-flow control, with $R_d = 3\Omega$

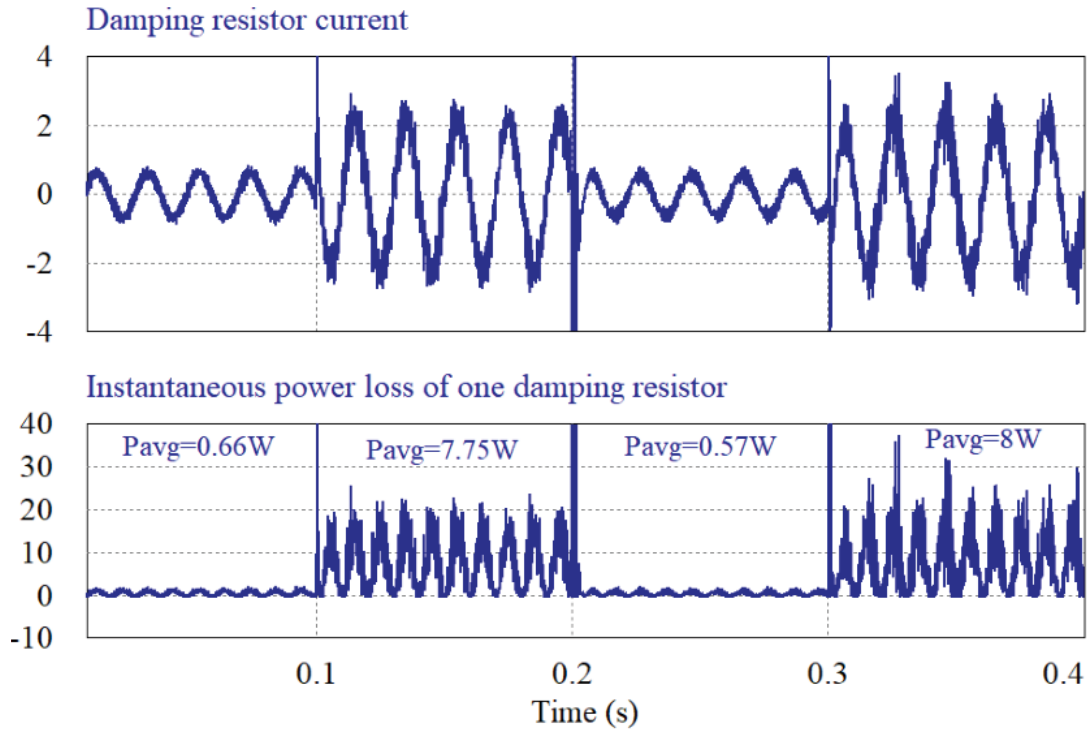


Figure 6.27: Waveform of the current and instantaneous power loss in a damping resistor ($R_d = 3\Omega$) for the bidirectional active power-flow control.

it steps to -16A and -48A at $t = 0.2s$ and $t = 0.3s$ respectively for controlling the reactive power flow from the output to the input side as shown in Figure 6.28. As can be seen, the references are tracked quickly, and as presented in Figure 6.29 the output current lags the output source voltage by about 90° from 0-0.2s, and then it leads the voltage by 90° from 0.2-0.4s. Figure 6.30 illustrates the active and reactive powers of both input and output sources. As can be observed, the active power of the output source is almost zero, and the active power of the input source is very small that is related to the power loss of the circuit, and that is why the input source current shown in Figure 6.29 is very low. Also, Figure 6.31 presents the input voltage of the MC and the output reference phase voltage generated by the control circuit. It should be noted that the simulation time-step represents one clock cycle in the FPGA in the experimental tests [116]. Considering the turn-off and turn-on times of the IGBTs, the FPGA clock frequency is selected 25MHz for a proper commutation. The time-step of the simulation should be adjusted to $4\mu s$ until the

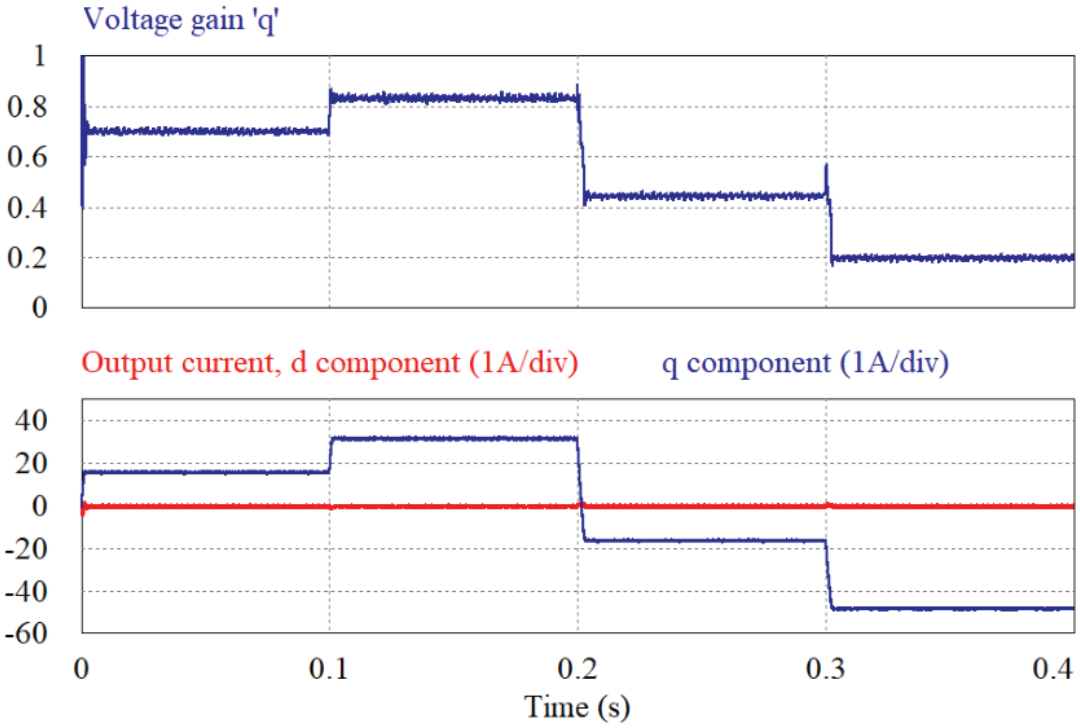


Figure 6.28: The voltage gain and d-q components of the output current for bidirectional reactive power-flow, with $R_d = 3\Omega$

simulation results be comparable with the experimental results. Compared to the Figure 6.23, the results shown in Figure 6.32 illustrates the impact of increasing the time-step on THD of the input and output currents for bidirectional active power flow.

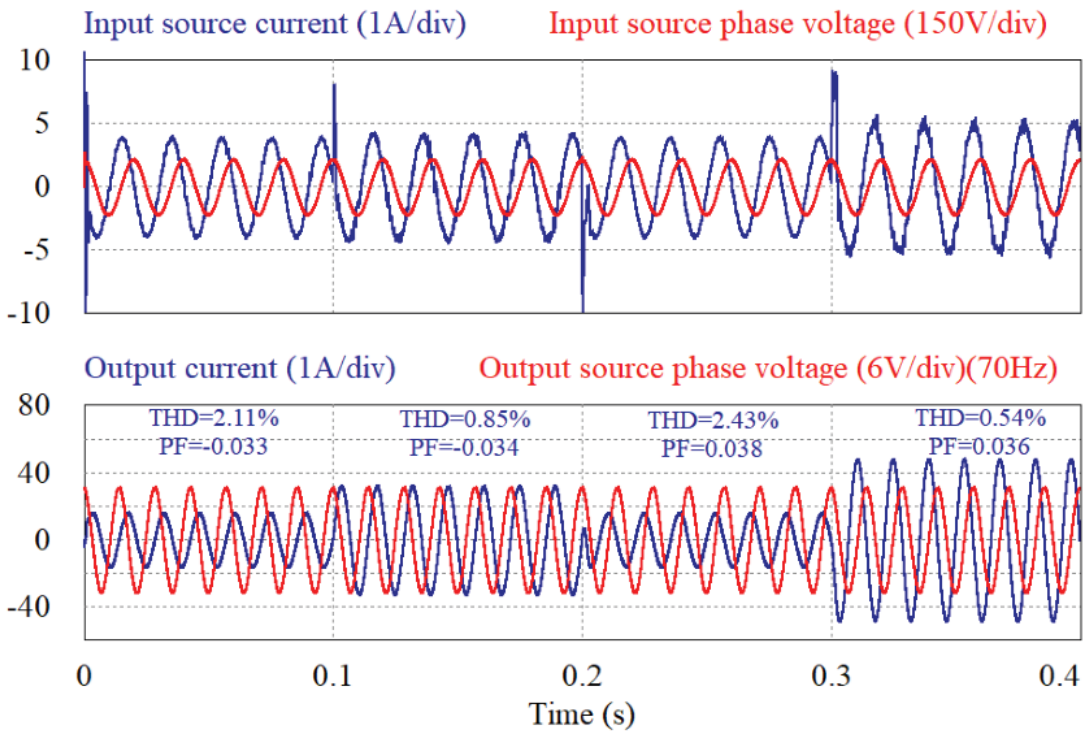


Figure 6.29: The input source current and output current for bidirectional reactive power-flow, with $R_d = 3\Omega$

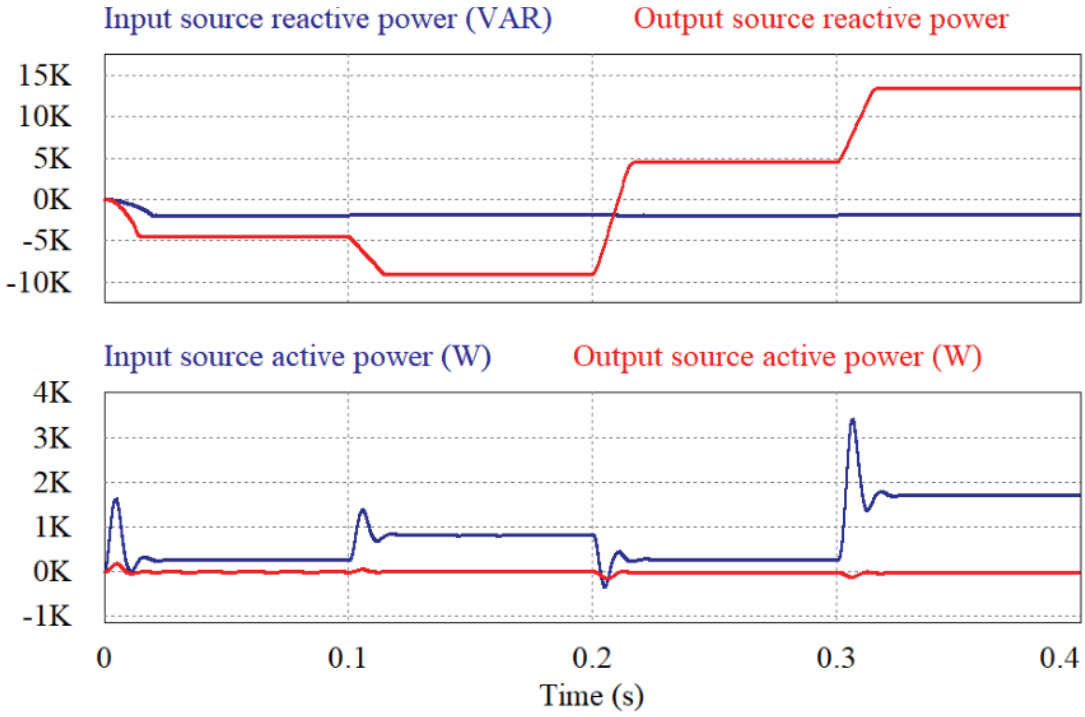


Figure 6.30: The input and output sources reactive and active powers for bidirectional reactive power-flow, with $R_d = 3\Omega$

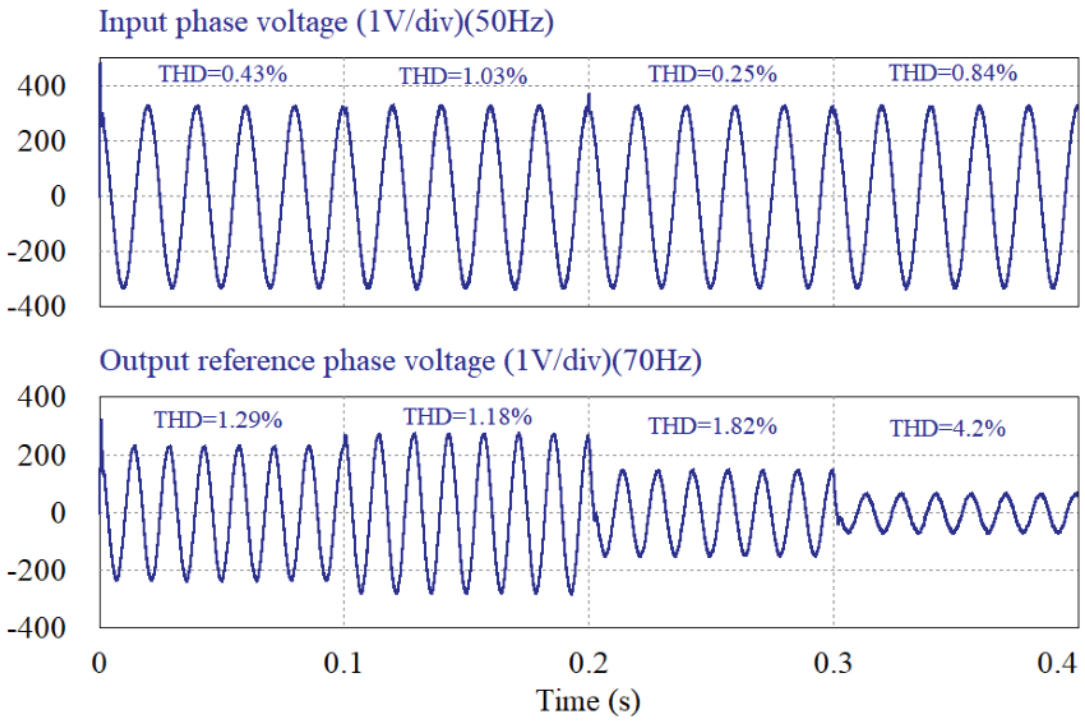


Figure 6.31: The input voltage of the MC and output reference phase voltage for bidirectional reactive power-flow, with $R_d = 3\Omega$

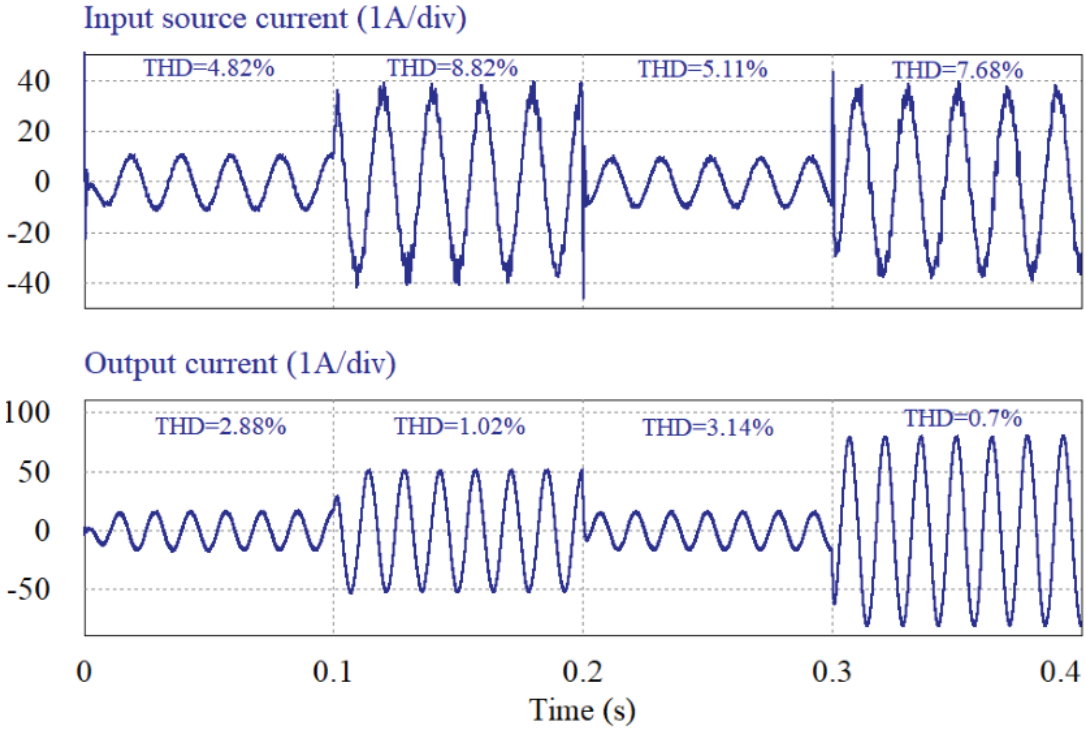


Figure 6.32: The input source current and output current for bidirectional active power-flow, with $R_d = 3\Omega$ and simulation time-step $4\mu s$

6.4.2 Bidirectional power flow control with digital input filter

In this section, the simulation results related to the digital filter method are presented. Figure 6.33 shows the input source and output currents. In contrast to the damping resistor method, the power-up problem has increased whenever a voltage step is applied. This problem is reduced by increasing the damping factor of the input filter [27]. In the case of the THDs of the input and output currents, there is no considerable difference between the two methods. The d-q components of the output current and the voltage gain illustrated in Figure 6.34 show that the references are tracked quickly. The input phase voltage of the MC and the generated output reference voltage are presented in Figure 6.35. The results are very close to the damping resistor method except for the step change times. The bidirectional reactive power test has been carried out, and the results are illustrated in Figures 6.36 to 6.38. As mentioned before, the FPGA clock frequency is adjusted on 25MHz which means that to compare the experimental results with the simulation, the time-step should be $4\mu s$. As can be seen in Figure 6.39, the system is unstable for the time interval 0.3-0.4s and for the other steps THDs of the currents are much higher than that of the damping resistor with the same conditions, specially for the input source current. As a result, in the experimental tests in order to keep the system stable, using the damping resistor strategy is preferred to the digital filter method.

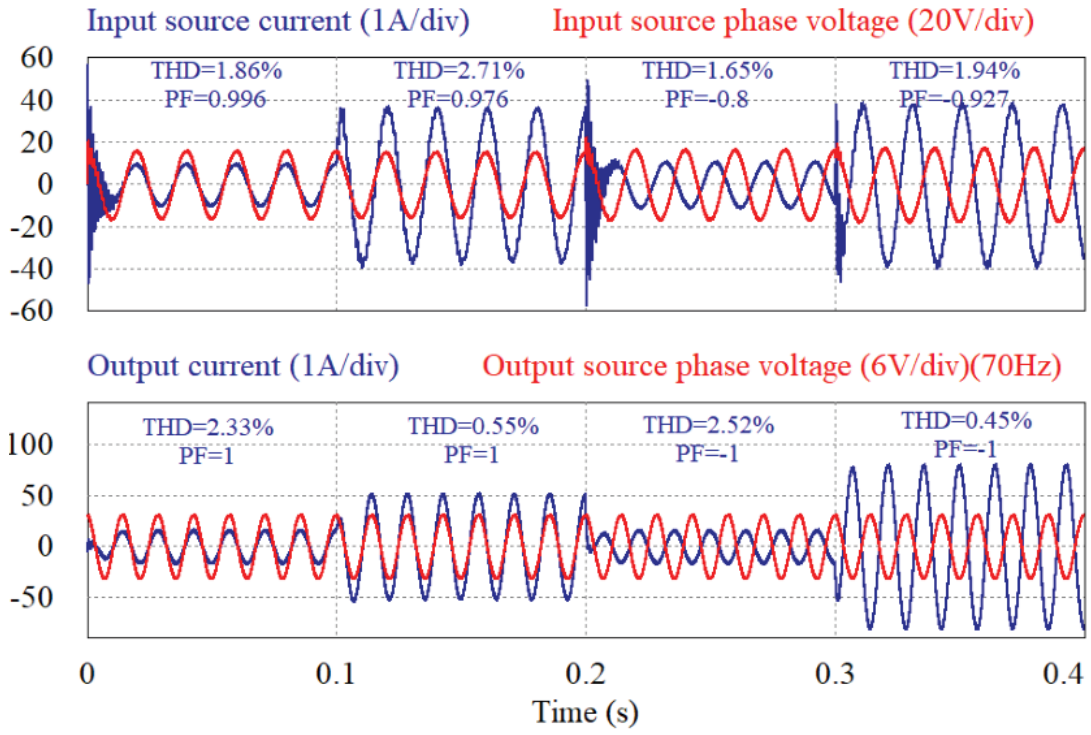


Figure 6.33: Input source current and output current for bidirectional active power-flow, with digital input filter $\tau = 0.8ms$

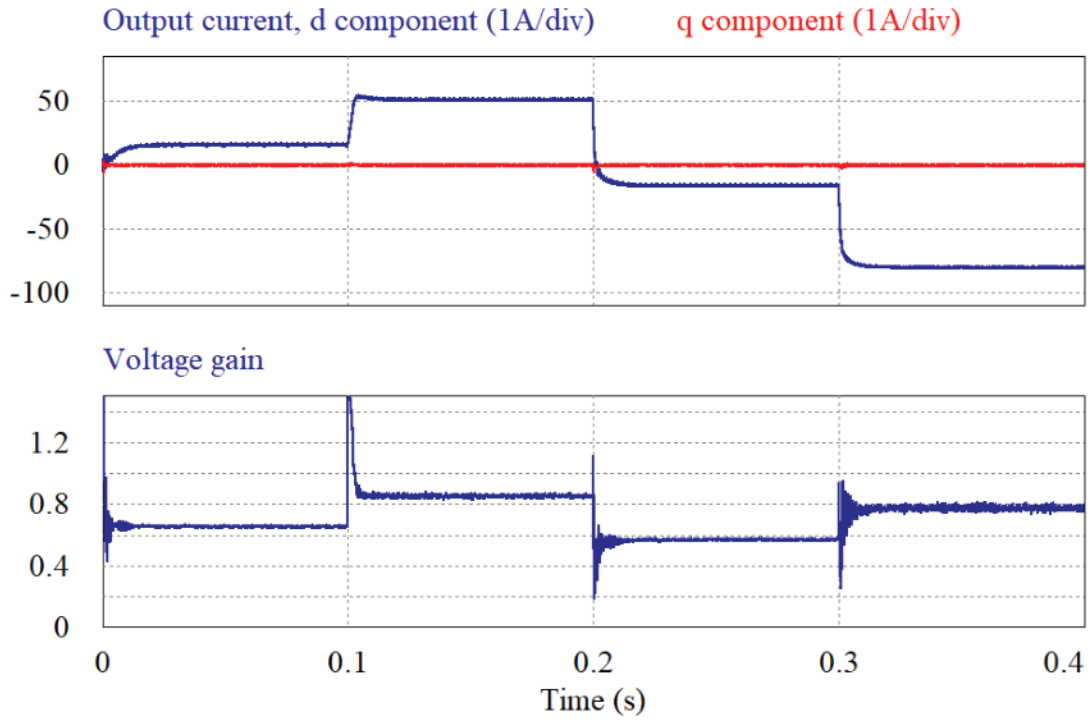


Figure 6.34: d-q components of the output current and voltage gain 'q' for bidirectional active power-flow, with digital input filter $\tau = 0.8ms$

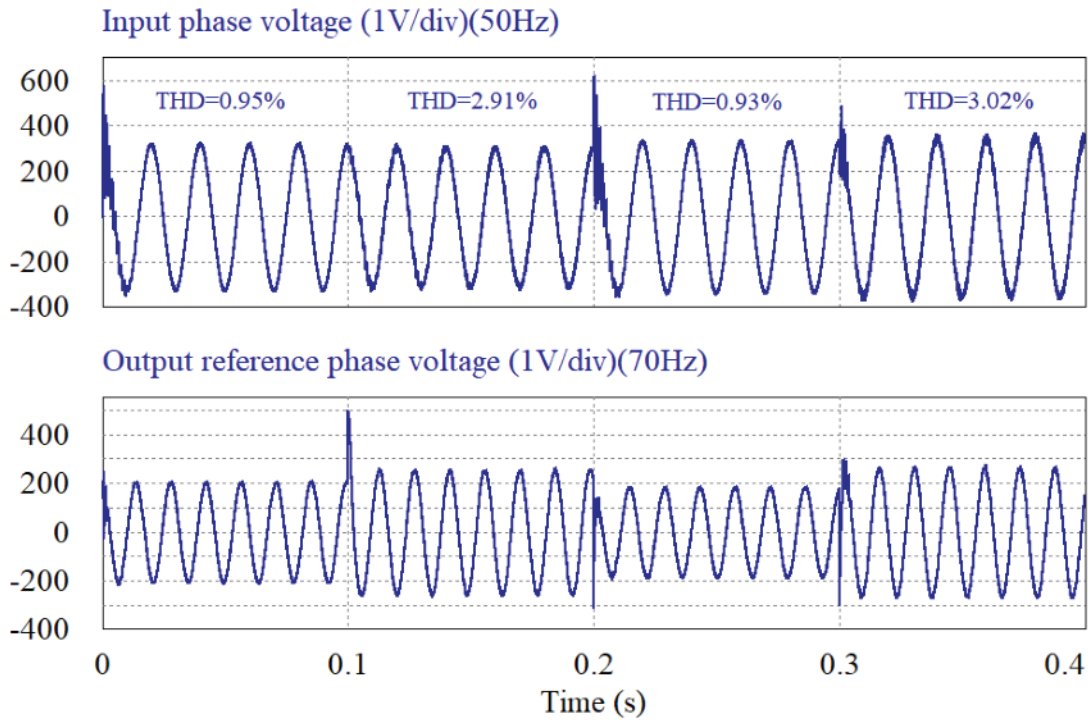


Figure 6.35: Input voltage and output reference voltage for bidirectional active power-flow, with digital input filter $\tau = 0.8ms$

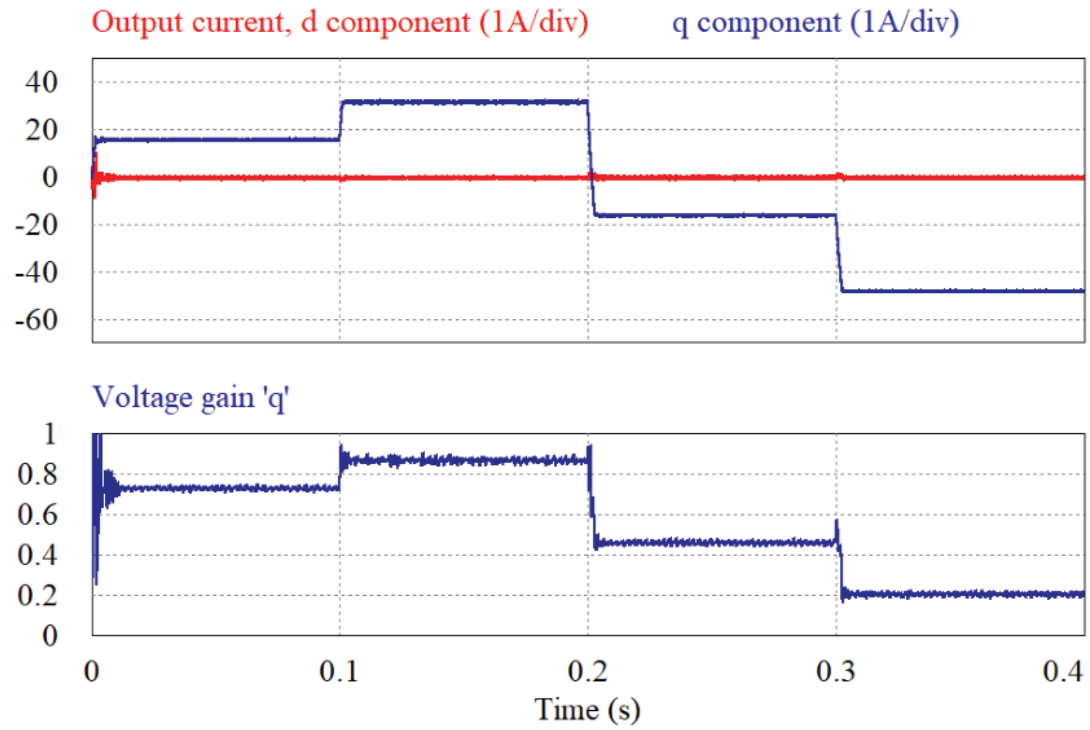


Figure 6.36: d-q components of the output current and voltage gain 'q' for bidirectional reactive power-flow, with digital input filter $\tau = 0.8ms$

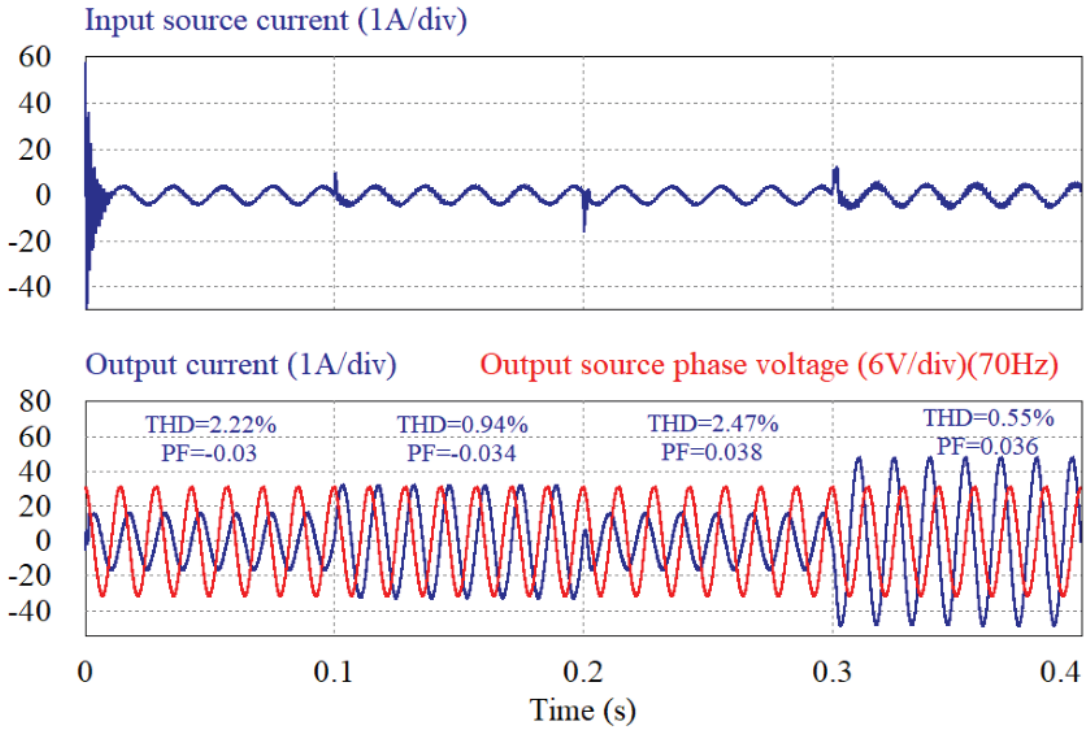


Figure 6.37: The input source current and output current for bidirectional reactive power-flow, with digital input filter $\tau = 0.8ms$

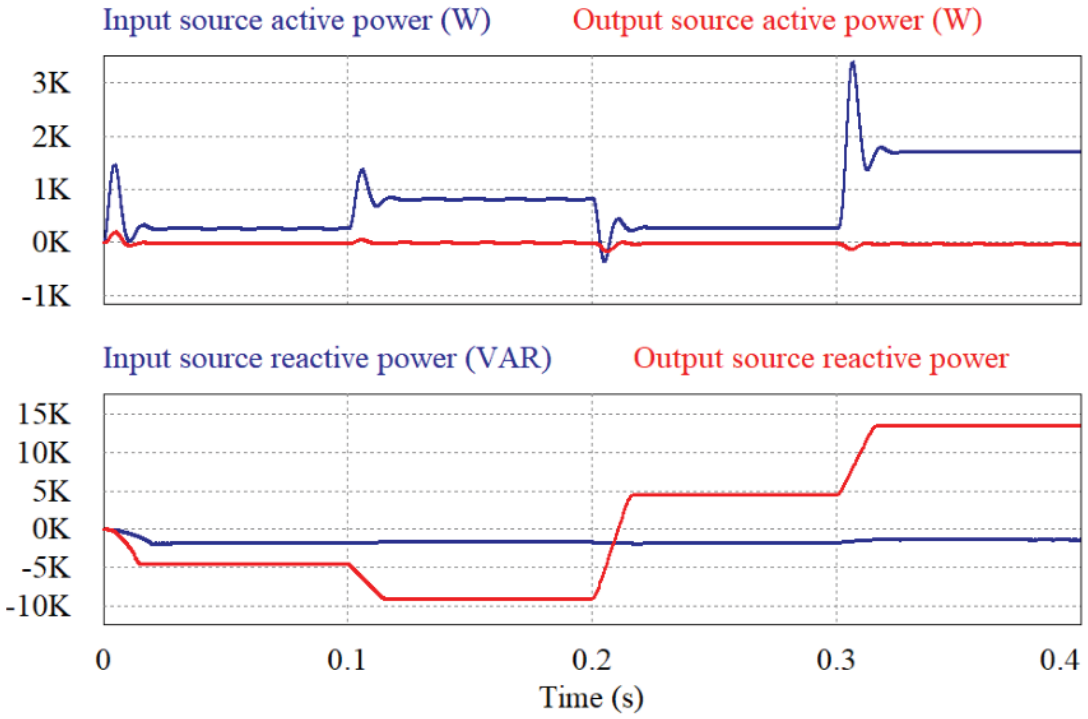


Figure 6.38: The input and output sources active and reactive powers for bidirectional reactive power-flow, with digital input filter $\tau = 0.8ms$

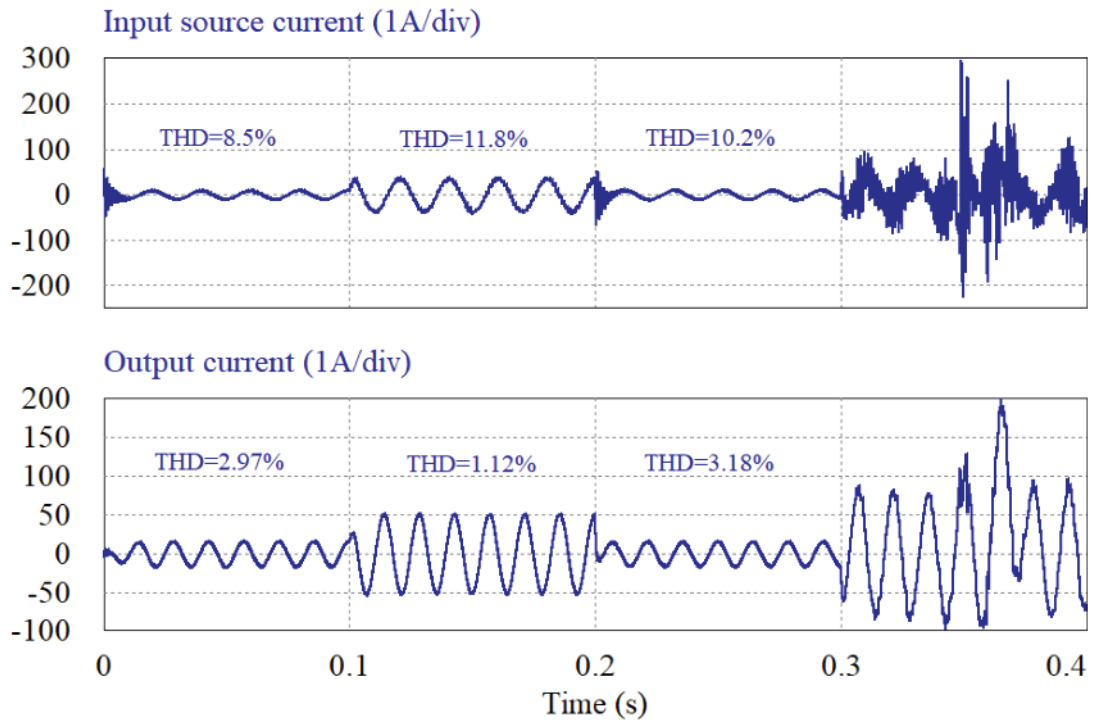


Figure 6.39: The input source current and output current for bidirectional active power-flow, with digital input filter $\tau = 0.8ms$ and time-step $4\mu s$

6.4.3 Bidirectional power flow control using a combination of the damping resistor and the digital input filter stabilisation methods

As illustrated in the unidirectional section, it is possible to decrease the power loss of the damping resistors by increasing the damping resistance. As the larger damping resistance cause the instability, the digital filter with a small time constant is utilised. Figures 6.40 and 6.41 show the results of this method for $R_d = 10\Omega$ and $\tau = 0.2ms$ with time-step $1\mu s$ and $4\mu s$ respectively. In the case of the THD and input PF, this strategy has similar results to the damping resistor method. Compare to $R_d = 3\Omega$, the damping resistor current is about half, and the power loss is around one third as shown in Figure 6.42. Furthermore, the power-up at the step times is much better than applying only the digital filter. Also, despite increasing the damping resistance, the converter remains stable for the whole range of the voltage gain.

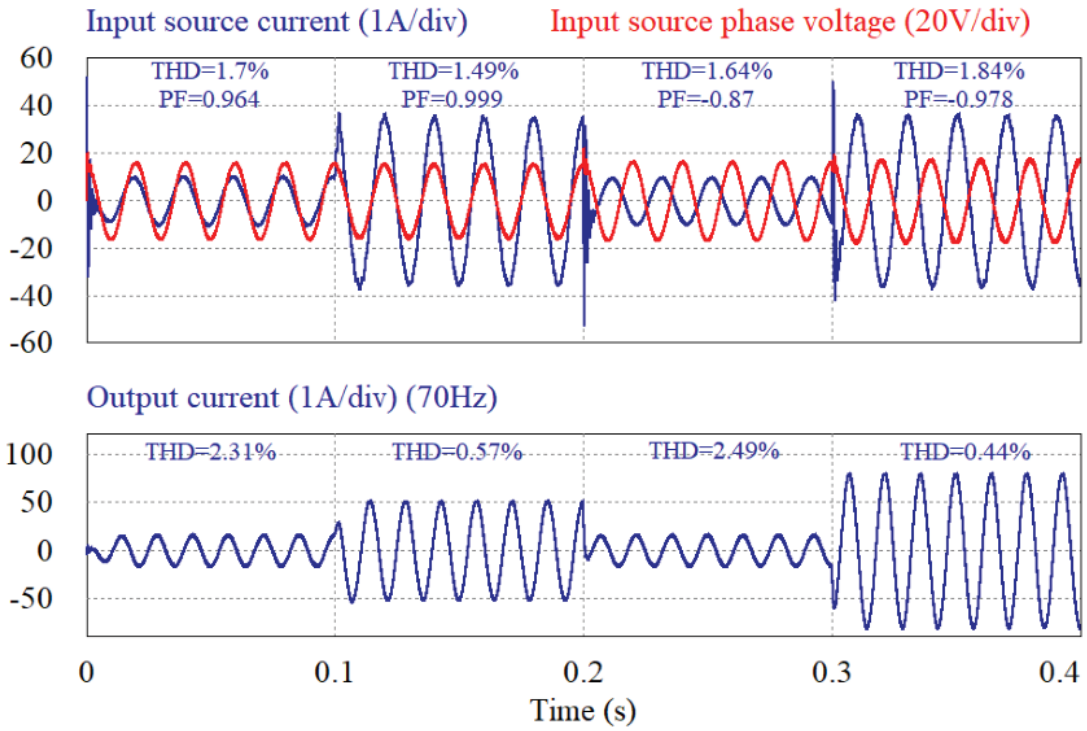


Figure 6.40: The input source current and output current for bidirectional active power-flow, with the combination of the damping resistor $R_d = 10\Omega$ and the digital input filter $\tau = 0.2ms$

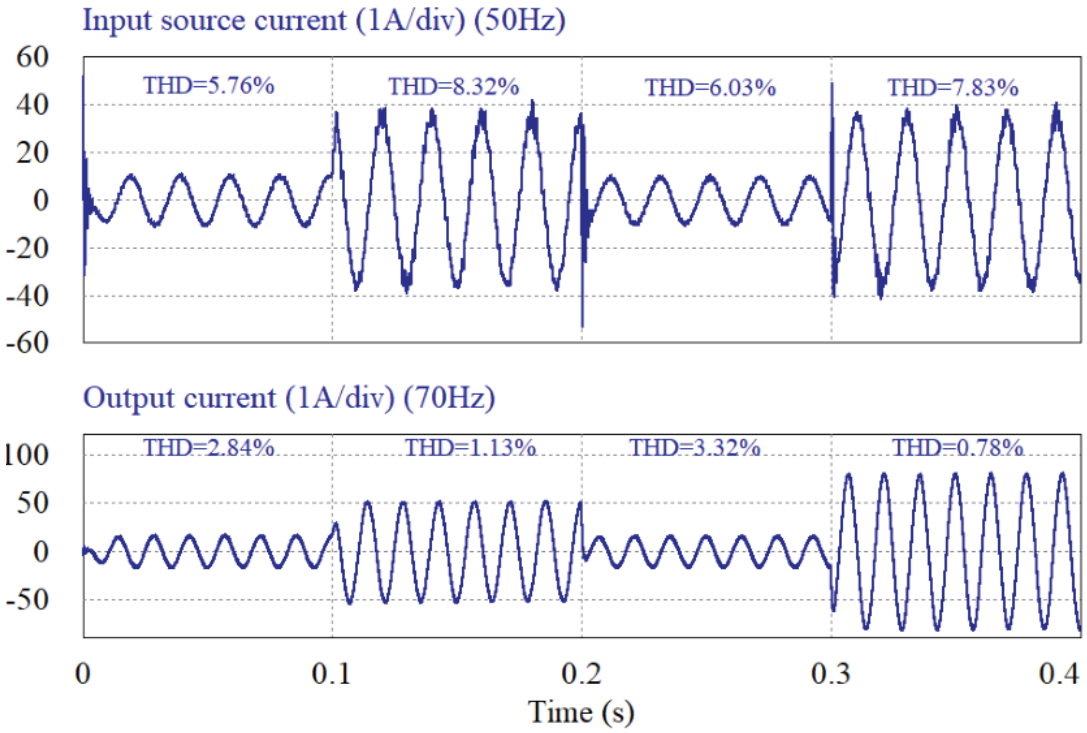


Figure 6.41: The input source current and output current for bidirectional active power-flow, with the combination of the damping resistor $R_d = 10\Omega$ and the digital input filter $\tau = 0.2ms$ when time-step is $4\mu s$

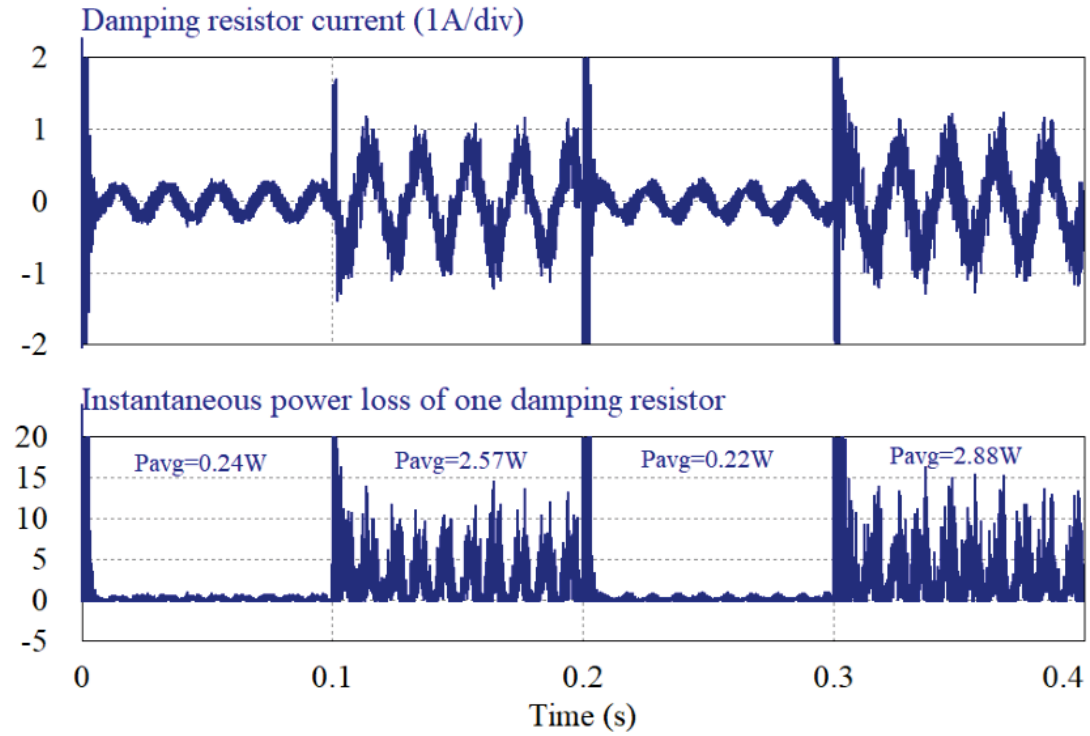


Figure 6.42: Waveform of the current and instantaneous power loss in a damping resistor for the bidirectional active power-flow control. Stabilisation method is a combination of the damping resistor $R_d = 10\Omega$ and the digital input filter $\tau = 0.2ms$, when time-step is $4\mu s$

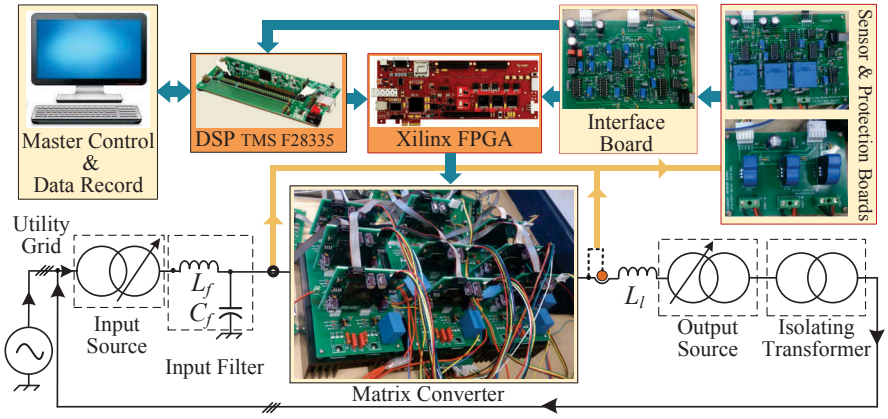


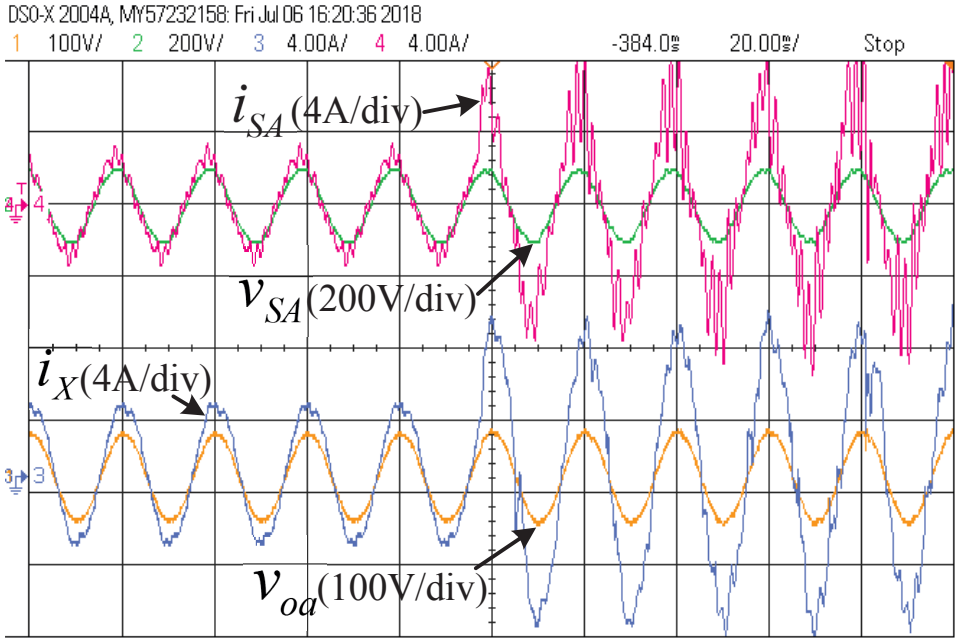
Figure 6.43: Schematic of the designed system for the experimental test of the MC bidirectional power flow using utility grid

6.4.4 Experimental results of bidirectional power flow control

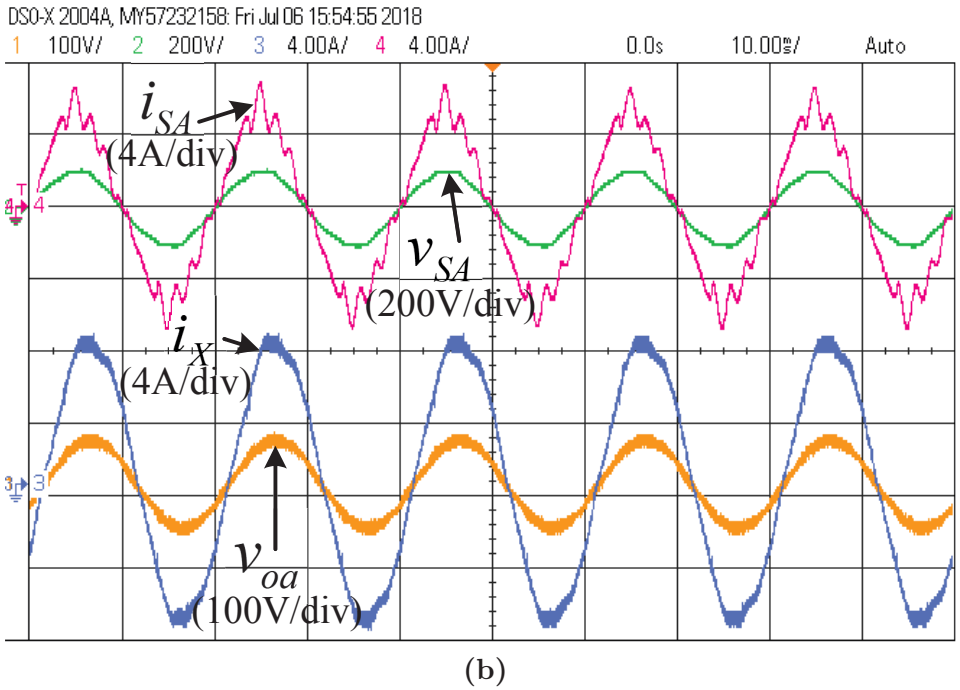
In order to experimentally test the bidirectional power flow control, the utility grid is used for both input and output sources using one isolation transformer and two

variable transformers as illustrated in Fig. 6.43. By this plan, it is possible to adjust the input and output voltage amplitudes separately, although the frequencies are the same ($f_i = f_o = 50Hz$). The input filter parameters are: $C_f = 6.6\mu F$ and $L_f = 3mH$, and an inductance $L_l = 6mH$ is used as the output filter. The input source phase voltage is adjusted to 72 V-rms, the output source voltage to 43 V-rms and the switching frequency (f_s) to 10kHz.

Fig. 6.44a shows the transition from stable to unstable operation when $i_{or(d)}$ jumps from $4A$ to $8A$ without applying any stabilization strategy. In Fig. 6.44b the system shows stable behavior for $i_{or(d)} = 8A$ when the large damping resistor $R_d = 47\Omega$ is used to make the system stable, but as can be seen, the input current is distorted. The experimental results in the case of using a combination of the digital filter and damping resistor are presented in Fig. 6.45. The test is carried out with $R_d = 47\Omega$ and digital filter time constant $\tau = 0.2ms$. Fig. 6.45a presents the input and output currents for bidirectional active power control. The d-component of the output reference current $i_{or(d)}$ is adjusted to change from $8A$ to $-8A$. As can be seen, at first, the input and output currents and voltages are in phase, and then the phase between them is changed to 180° when output reference current changes to $-8A$. In Fig. 6.45b, the same results are presented for bidirectional reactive power control by changing $i_{or(q)}$ from $8A$ to $-8A$. The output voltage at first leads the current by about 90° and then lags it by 90°. The frequency spectrums of the input and output currents for bidirectional active power flow control is presented in Fig. 6.46. It can be seen that harmonics are introduced at the integer multiples of the switching frequency $f_s = 10kHz$ and at the side bands of these frequencies. Fig. 6.47 shows the active and reactive bidirectional power flow when only the input digital filter with $\tau = 0.5ms$ is applied. The transient oscillation can be seen when $i_{or(d)}$ jumps from $4A$ to $8A$, although, as the current step is not large, it is negligible. The results in the case of using only a small damping resistor $R_d = 3\Omega$ is presented in Fig. 6.48. When the current is controlled from the output to the input side, the combination method presents less distortion for the input source current. As

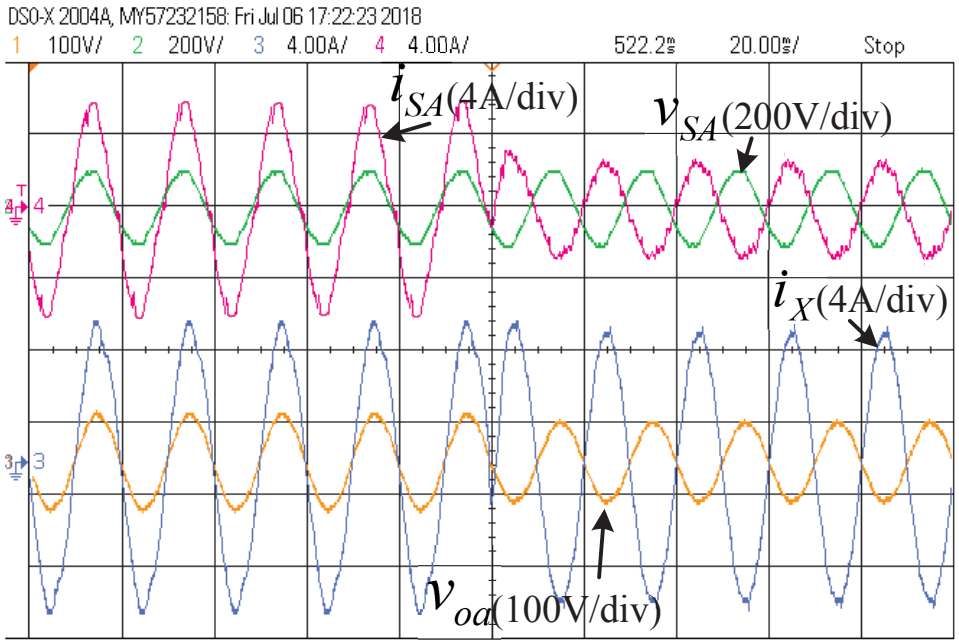


(a)

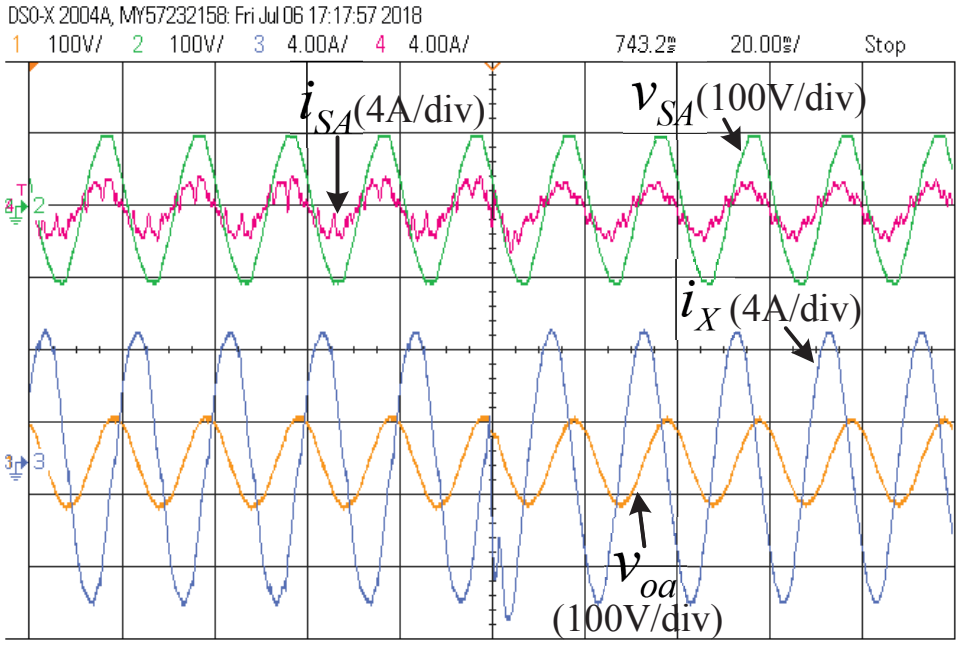


(b)

Figure 6.44: Experimental results for bidirectional active power control, input and output currents and voltages a) Without applying any stabilization method b) By adding only the large damping resistor $R_d = 47\Omega$

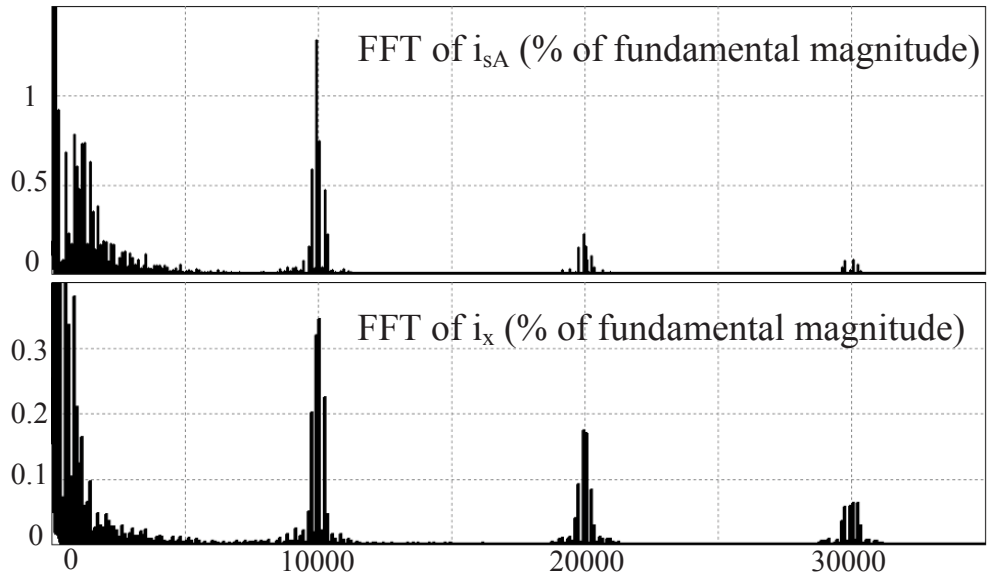


(a)

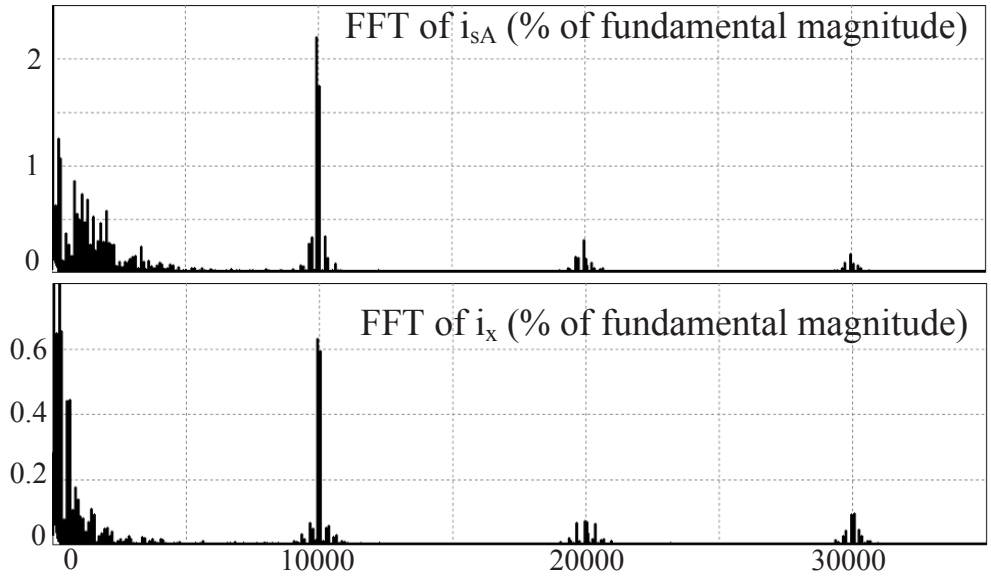


(b)

Figure 6.45: Experimental results for bidirectional power-flow control, input and output currents and voltages, using the combination method, with $R_d = 47\Omega$ and $\tau = 0.2ms$ a) Active power control b) Reactive power control



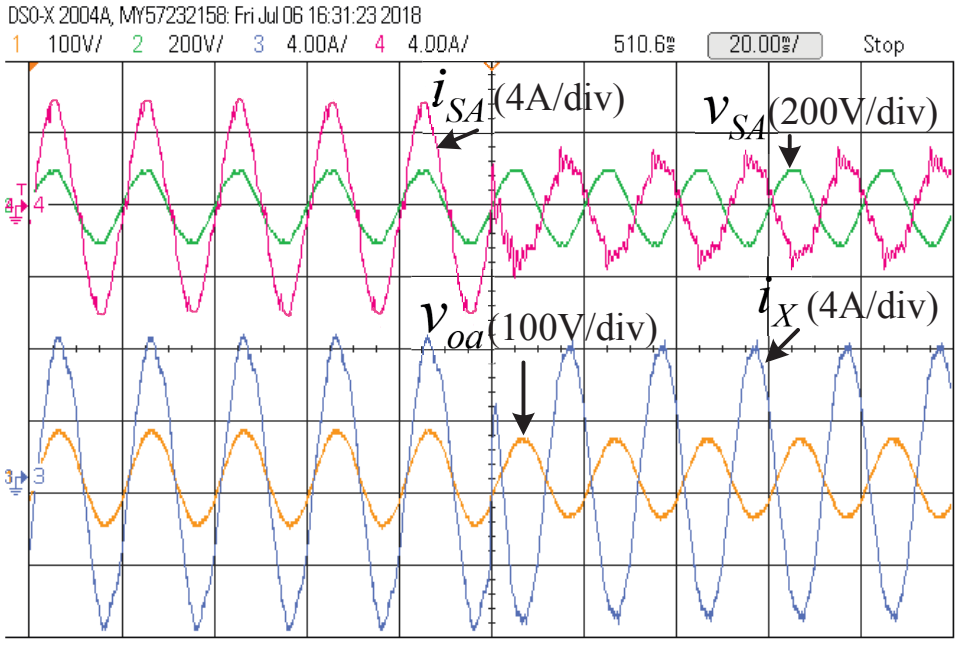
(a)



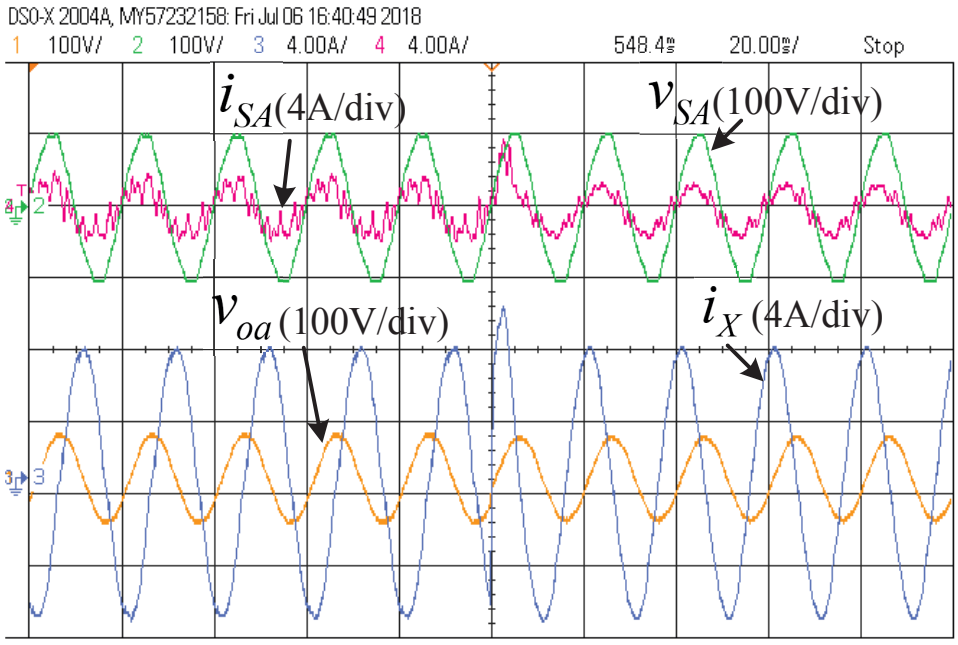
(b)

Figure 6.46: FFT of the input and output currents, for bidirectional active power flow control, a) From the input to the output side b) From the output to the input side

explained before, in experimental tests because of the clock frequency effect of the FPGA, the anti-windup PI controllers are used to help the stability of the system in high voltage gains.

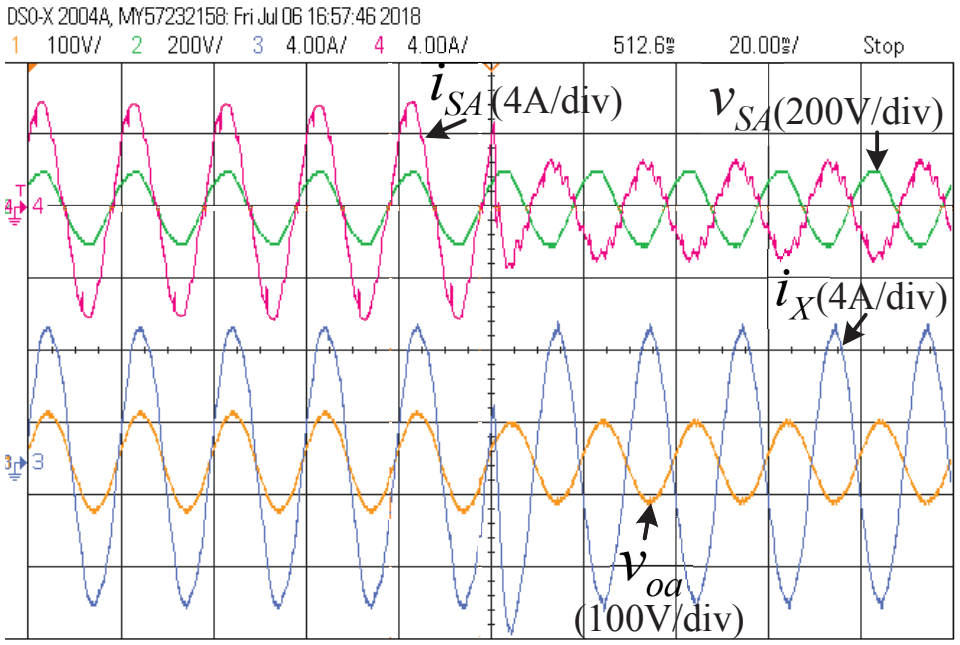


(a)

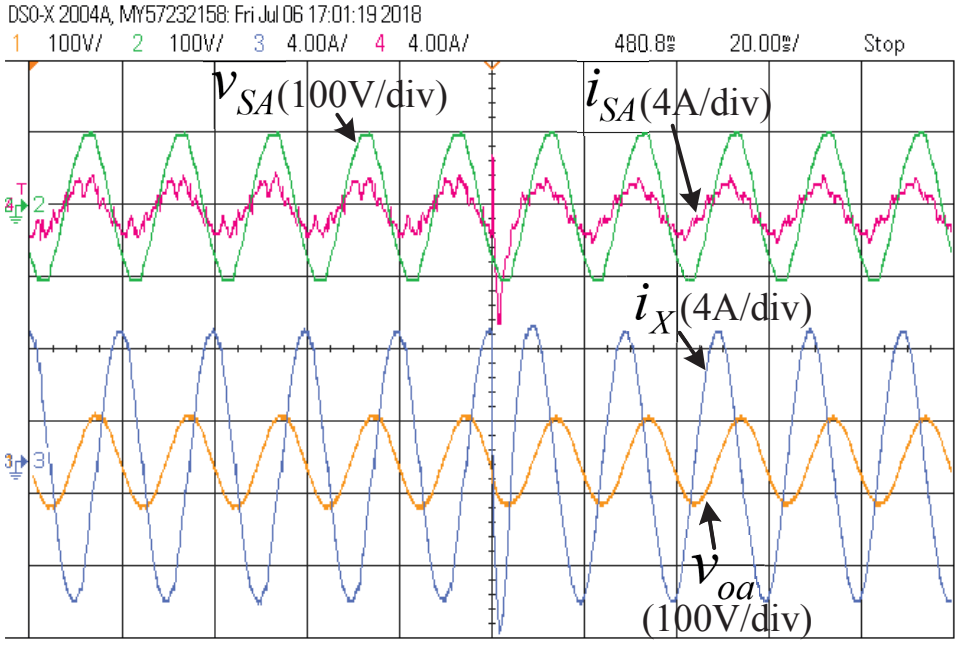


(b)

Figure 6.47: Experimental results for bidirectional power-flow control, input and output currents and voltages, using the digital filter method, with $\tau = 0.5ms$ a) Active power control b) Reactive power control



(a)



(b)

Figure 6.48: Experimental results for bidirectional power-flow control, input and output currents and voltages, using the damping resistor method, with $R_d = 3\Omega$ a) Active power control b) Reactive power control

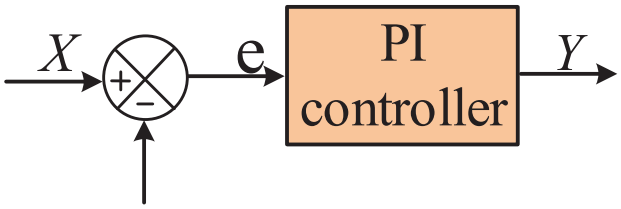


Figure 6.49: Analogue PI controller

6.5 PI Controller

The PI controller as shown in Fig.6.49 is used to make the actual signal match the predefined reference signal. In the proposed VOC method, the PI controller is used to generate the output reference voltage. The controller transfer function can be described by:

$$\frac{Y(s)}{E(s)} = k_p + \frac{k_i}{s} \tag{6.32}$$

The equation can be rearranged as:

$$Y(s) = k_p E(s) + k_i E(s)\frac{1}{s} = Y_p(s) + Y_I(s) \tag{6.33}$$

where k_p is the proportional gain and k_i is the integral gain. The proportional part gives a rapid control response and causes a possible steady state error. Increasing k_p reduces the rise time and steady-state error, although, it may generate overshoot after a certain limit. On the other hand, the integral control can eliminate the steady state error and by increasing k_i, the rise time can be reduced a little, but this increases the overshoot after a certain limit. If there is the derivative part, increasing k_d decreases the settling time and reduces the overshoot. The PI controller can eliminate the steady-state error, but it has a negative impact on the overall stability of the system. It cannot eliminate the oscillations, and generates undesirable overshoots with increasing integral gains.

To become applicable to the digital equipment, the analogue PI control algorithm

has to be discretised using different methods because the control strategies as digital algorithms are implemented in programmable devices such as DSPs, PLCs and microprocessor-based equipment. In order to discretise the continuous time PI controller in Figure 6.49, the integral operator $(\frac{1}{s})$ can be represented in discrete form by three different methods: (Trapezoidal) Tustin's method, forward and backward Euler. To do the transformation, the frequency element s in the continuous time domain should be substitute with its equivalent in the discrete time domain, presented as Z. The function $T(Z)$ for the three transformation methods is presented as follows:

$$\text{Tustin's method:} \qquad T(Z) = \frac{T_s}{2}\frac{Z+1}{Z-1} \tag{6.34}$$

$$\text{Forward Euler:} \qquad T(Z) = \frac{T_s}{Z-1} \tag{6.35}$$

$$\text{Backward Euler:} \qquad T(Z) = \frac{T_s Z}{Z-1} \tag{6.36}$$

where the T_s is the sampling period. By applying backwards Euler method and Z-transform properties in (6.37) and (6.38), the continuous-time transfer function of the PI controller presented in (6.32) turns to the discrete form in Figure 6.50:

$$X[Z] = Z\{x(k)\} = \sum_{k=0}^{\infty} x(k)Z^{-k} \tag{6.37}$$

$$Z\{x(k-n)\} = Z^{-n}X[Z] \tag{6.38}$$

$$\begin{aligned} \frac{Y_I[Z]}{E[Z]} = k_i T_s \frac{Z}{Z-1} &= k_i T_s \frac{1}{1-Z^{-1}} \\ Y_I[Z](1-Z) &= k_i T_s E[Z] \\ y_I(k) &= y_I(k-1) + k_i T_s e(k) \end{aligned} \tag{6.39}$$

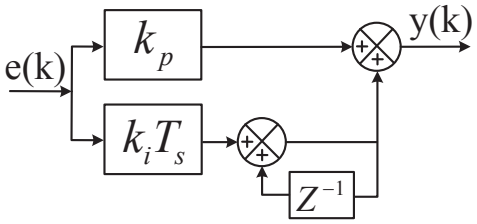


Figure 6.50: Block diagram of the discrete PI controller

Using Tustin's method, the discrete version of the PI algorithm is calculated as:

$$\begin{aligned} \frac{Y_I[Z]}{E[Z]} &= k_i \frac{T_s}{2} \frac{Z+1}{Z-1} = k_i \frac{T_s}{2} \frac{1+Z^{-1}}{1-Z^{-1}} \\ Y_I[Z](1-Z^{-1}) &= k_i \frac{T_s}{2} E[Z](1+Z^{-1}) \\ y_I(k) &= y_I(k-1) + k_i T_s \frac{e(k)+e(k-1)}{2} \end{aligned} \tag{6.40}$$

6.6 Anti-windup PI Controller

Comparing the frequency response of the discretised PI controller, some distortion can be observed. To reduce the generated distortion, sampling frequency f_s has to be much higher than the frequency of interest f.

When a large transient occurs at the input of the PI controller which causes a large error, the integrator accumulates a non-zero error during the transients called integrator windup. If the accumulated error is unwound, an overshoot happens. Also, process saturation can cause a constant error as the output of the process is limited to the maximum or minimum of its scale, and the controller's output cannot affect the controlled variable anymore. To prevent integral windup, the controller output should be limited to the pre-determined bounds and be fed back to the integral part using a closed loop. The integrator continually sums controller error as long as controller error exists. When a large transient occurs at the input of the PI controller which causes a large error, or the error persist for a long time, the integral term grows very large and causes the control element to saturate because the output of the process is limited to the maximum or minimum of its scale. This problem

referred to as integral windup or integral saturation, and the controller loses the ability to regulate the process and has no longer impact on it. Using a limiter to clip the output of the controller to the premium value cannot stop the growth of the integral sum of the error.

6.7 Conclusion

The output impedance of the input filter has an important effect on the system stability. In general, the filter output impedance should be as low as possible when compared to the converter input impedance. Increasing the filter capacitance (C_f) is one of the methods for reducing the filter output impedance as far as it does not decrease the input power factor. Another strategy for achieving low output impedance in the filter for all frequencies is proper filter pole damping. For this purpose, the impacts of some strategies reviewed in brief, using the graphs. Adding a damping resistor and using a digital low-pass filter are the most common methods for stabilisation. Moreover, a combination of these two strategies is proposed, and the stability area, THDs of the input and output currents, and power-up problem were discussed.

Also, the function of the MC analyzed as an interface between the utility and a microgrid using the simulation and experimental tests. For this purpose, the output current was controlled using a VOC method to control the output active and reactive power flow. Two different tests have been done to show the ability of the MC for controlling the bidirectional power flow. The first test is for the unidirectional power flow when the output is connected to the RL load, and the results for unidirectional active and reactive power flow presented. The test has been performed for the suggested stabilisation strategies. As expected from the simulation results, it was possible to increase the damping resistance with adding the digital low-pass filter to decrease the power loss without increasing the THD of the currents.

In the second test, the ability of the MC for the bidirectional active and reac-

tive power flow control was studied. As two power sources were required for this test at the input and output of the converter, two variable transformers and one isolated transformer are used to make two isolated voltage sources. The impacts of the stabilisation methods were analyzed using the simulation tests, and the best method that was a combination of the damping resistor and digital input filter was validated experimentally. The FPGA clock frequency has a significant effect on the experimental results in aspects of the THD of the input and output power, and the stability of the converter. In order to show the effects, the simulation tests have been repeated for a different time-step that represents the FPGA clock. The experimental results confirm the simulation results with the time-step which is consistent with the FPGA clock frequency.

Chapter 7

CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

MCs are a replacement for back to back converter systems that allows heavy, bulky and unreliable DC link components to be avoided. MCs also have regeneration property, and can generate the high quality sinusoidal input and output currents. The possibility of having the unity input power factor by using an adjustable input displacement angle is another advantage of the MCs. Although, due to the lack of the dc-link capacitor they are more sensitive to the disturbances of the input and output voltages, and also have a higher number of power semiconductor devices. Mcs have a wide range of applications including the electric vehicles, military applications, wind turbines and aerospace applications. In this thesis, at first, the structure of the indirect and direct ac-ac converters have been reviewed, and some schemes of the matrix converters as the direct ac-ac converters have been presented.

Two most common modulation methods of the MCs including the Venturini modulation method and SVM have been analyzed in detail, and the simulation and experimental results have been illustrated. The SVM modulation method presents better results in terms of the maximum voltage gain, THDs of the input and output currents and adjustable input power factor compared to the Venturini modulation method, although, SVM is more complicated. The current commutation methods as one of the basics are illustrated due to their importance in MCs operation. The

Output current direction based four-step semi-soft commutation method has been selected to be applied to the prototype MC as one of the safest commutation methods. The study is further completed by the simulation and experimental results.

Details of the design, development and experimental test of a prototype DMC have been presented. This includes the technical points of the input filter design, clamp circuit, over-current and over-voltage protection circuits, and voltage and current measurement circuits.

Due to the application of the MC as an interface between the main grid and the microgrid, bidirectional power flow capability of the MC was an essential part of the research. In this regard, stability of the MC under the change in power flow direction and active and reactive power became an important issue. The input filter elements can significantly affect the stability region of the MC.

As the input current of the MC has a PWM configuration, using a low-pass filter is necessary to smoothen the returned current to the input voltage source. On the other hand, the low-pass LC filter can cause the system to become unstable. To control this effect, some suggestions in the literature have been reviewed, and the impact of each parameter of the system including the input filter parameters, load, input and output frequencies and transmission line impedance are investigated. Some of these parameters have serious impacts on the stability problem, and the others have fewer impacts. In addition, it is not possible to change some parameters like the input and output frequencies or the load or the transmission line impedance. It was seen that the input filter parameters have significant effects on the stability, compared to the other system parameters. Adding the damping resistors or the low-pass digital filter are the two solutions for this problem which have been analyzed comprehensively based on the small-signal model of the system. In the case of the power-up problem and THDs of the currents, adding the damping resistors gives better results, while the digital filter causes less power loss. A combination of these two methods has been suggested and analyzed in this thesis, which can help to increase the damping resistors and decrease the time constant of the digital filter

without any instability problem. This strategy reduces the power loss caused by the damping resistors, while power-up problem improves compare to the case of using only the digital filter.

To assess the performance of the converter for controlling the active and reactive power in both directions, two different tests have been done. The control method is a VOC strategy using the anti-windup PI controllers. In the first test, the MC is used for unidirectional power flow from input source to the output RL load. In this case the active and reactive power flow between the source and the load is controlled effectively by changing the d and q parts of the output current. The second test has been carried out for assessing the MC as a converter between the grid and microgrid, which are exchanging the active and reactive power in both directions. In this case, the utility grid and the microgrid are modeled by using variable transformers at the input and output of the MC. A four quadrant power flow control technique is applied to the MC to change both active and reactive power in both directions. The three strategies for stabilisation of the system have been applied in both tests, and the simulation and experimental results have been presented. It was seen that the combination of using the digital filter and the damping resistor provides better results in terms of the THD of the input and output currents and the power loss.

7.2 Recommendation For Future Work

For future research, extended studies on some of the interesting topics for the matrix converter are recommended as following:

- As indicated in Chapter 5, when SVM with the switching pattern using three zero vectors is applied as the modulation method, it was more difficult to have a stable system for large voltage gains. Therefore, impacts of the modulation methods, switching patterns and switching frequencies are required to be investigated as the items which have influence on the stability of the matrix converter.

- In Chapter 6, some simulation results have been presented for different time-steps to compare them with the experimental tests. It has been shown that when simulation time-step is less than the time period of FPGA clock pulse, the MC stability improved significantly. This means that, the clock frequency of the FPGA is an effective factor in the stability of the MC, and quality of the waveforms which needs to be studied in more details in future.

- Also as FPGA performs the instructions in parallel, research on an all FPGA-based control system instead of the combination of a DSP and a FPGA can clarify the impacts of the speed of the data process on the quality of the input and output currents of the MCs.

- As illustrated in the introduction chapter, MCs have different topologies including the DMC, IMC, sparse MCs and multilevel MCs. The influence of the converter topology on the stability problem can be studied to show if the the structure of the MC has any positive or negative effect on the stability problem.

- Study on the other control methods such as model predictive control and sliding mode control, for bidirectional power flow control in MCs and also their effects on the stability can be an interesting topic as future work.

PUBLICATIONS BASED ON THE THESIS WORK

- Z. Malekjamshidi, M. Jafari, J. Zhang and J. Zhu, "Design and analysis of protection circuits for safe operation of direct matrix converters," 2017 20th International Conference on Electrical Machines and Systems (ICEMS), Sydney, NSW, 2017, pp. 1-4.

- Z. Malekjamshidi, M. Jafari, D. Xiao and J. Zhu, "Operation of indirect matrix converters in different SVM switching patterns," 2015 4th International Conference on Electric Power and Energy Conversion Systems (EPECS), Sharjah, 2015, pp. 1-5.

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- Z. Malekjamshidi, M. Jafari and Jian Guo Zhu, "Design, simulation and implementation of an intelligent power management system for a battery supported

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