Boost Integrated Three-Phase Solar Inverter using Current Unfolding and Active Damping Methods

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***Abstract*—This paper proposes a three-phase grid connected solar inverter with integrated boost function. The circuit operating principle is based on current unfolding and injection method, which is similar to that of a SWISS rectifier. This approach requires only two high frequency switches operating at only half voltage stress, thus leading to a significant reduction in switching losses. Other switches only operate at line frequency, and therefore can be optimized to reduce conduction losses. The proposed inverter therefore can deliver high efficiency. This paper discusses the basic operating principle as well as control method for the inverter. It is revealed that the output currents of the proposed inverter contains intrinsic oscillation due to current unfolding operation. In order to solve this problem, an active damping method is proposed to stabilize the operation. As a result, stable operation of the proposed method is confirmed by simulation. The feasibility of the proposed inverter is also confirmed using a mini laboratory prototype.**

I. Introduction

Photovoltaic (PV) energy is becoming more and more attractive due to continuous drop in PV panel production cost. Large scale installation of PV energy prefers three-phase grid connection in order to reduce transmission loss. Improving the performance for three-phase inverters is therefore an attractive research topic. For examples, additional boost stage is needed to increase effectiveness of a conventional three-phase PV inverter [1]–[3]. Advanced modulation methods were introduced in [4], [5] to reduce switching loss in three-phase inverters. References [5]–[7] discussed current unfolding and harmonic injection methods to improve the performance of grid-connected three-phase inverters. Other researches applied multilevel approach to reduce voltage stress on high frequency switching devices [8]–[11].

This paper proposes a three-phase inverter with integrated boost function as shown in Fig. 1. Despite having 14 switches, only two high frequency switches are required, the rest are operated at low frequency and thus have negligible switching losses. The low-frequency switches are therefore can be selected to optimise the conduction loss. As a result, the benefit of this inverter is loss reduction and its integrated boost function, resulting in a potential high efficiency. Therefore, the proposed inverter is suitable for large-scale grid connected applications such as solar power plant.

The proposed inverter consists of two parts: a boosting stage which behaves like a voltage-source converter and a current unfolding stage which acts like a current-source inverter. This configuration has a similar operating principle compared to a SWISS rectifier [7], but it converts electrical power from dc to three-phase ac.

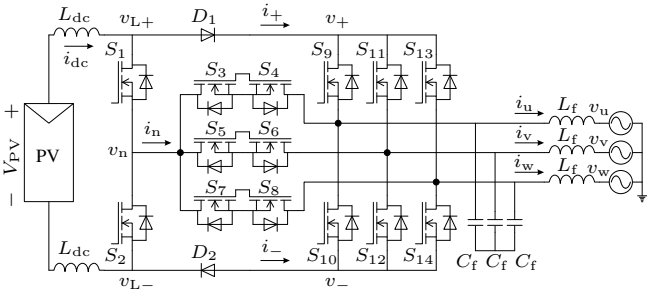

Fig. 1: Circuit configuration of the proposed three-phase solar inverter.

Similar to other current-source inverters, the switching patterns for the proposed inverter must incorporate overlap time to avoid open circuit conditions. This paper demonstrates that the overlap causes unwanted fluctuation at the output. Therefore, this type of inverter has to deal with oscillation problem unlike the SWISS rectifier where this effect is not as severe thanks to uncontrolled rectifier bridge. In order to suppress oscillation, active damping method using current feedback control was proposed for dc to dc converter [12]. This paper proposes that existing voltage sensors at the output can be used to suppress the oscillation via voltage feedback and changing the duty cycle at the boosting stage.

The operation of the proposed method is studied via a scaled down 20-kVA circuit, connecting a PV to a 400-V three-phase transformer before joining a 6.6-kV grid. Simulation results verify stable operation of the inverter as well as the effectiveness of the active damping method. In addition, a mini laboratory prototype is built to confirm the feasibility of the proposed inverter.

II. Circuit Configuration

Fig. 1 shows a circuit diagram of the proposed three-phase solar inverter. A PV panel is connected to the positive and negative terminals of the inverter via two dc inductors $L_{\rm dc}$ to reduce common mode noise. The two dc inductors are then connected to two boost converters which control the input current $i_{\rm dc}$ and achieve maximum

power point tracking (MPPT) for the PV operation at V_{PV}. The inverter requires only two high frequency switches S_1, S_2 and two diodes D_1, D_2 to control three currents: i_+ at the positive terminal, i_- at the negative terminal, and i_{n} at the neutral point. Then, it employs 12 switches $S_3 \sim S_{14}$ to unfold those currents to form three-phase currents i_{u}, i_{v}, i_{w}. Those switches only operate at low frequency and thus have negligible switching loss. Since the circuit operates as a current-source inverter with pulsating output currents, a three-phase filter capacitor C_{f} is needed at the output terminals. Due to the pulsating output currents, there will be small switching ripples remaining at the filter capacitors. Therefore, before connecting to a three-phase grid, a small three-phase filter inductor L_{f} can be applied to minimize ripple effect on sinusoidal grid.

III. Operating Principles

A. *Low-frequency switching operation*

TABLE I: Modulation operation of low-frequency switches in the proposed three-phase inverter.

Switches \ Sectors	I	II	III	IV	V	VI
S_3, S_4	0	1	0	0	1	0
S_5, S_6	1	0	0	1	0	0
S_7, S_8	0	0	1	0	0	1
S_9	1	0	0	0	0	1
S_{10}	0	0	1	1	0	0
S_{11}	0	1	1	0	0	0
S_{12}	0	0	0	0	1	1
S_{13}	0	0	0	1	1	0
S_{14}	1	1	0	0	0	0

Assume that the output three-phase voltages are balanced as:

$$v_{\mathrm{u}} = \sqrt{2}V_{\mathrm{o}}\cos(\omega t), \quad (1)$$
$$v_{\mathrm{v}} = \sqrt{2}V_{\mathrm{o}}\cos(\omega t - 2\pi/3), \quad (2)$$
$$v_{\mathrm{w}} = \sqrt{2}V_{\mathrm{o}}\cos(\omega t + 2\pi/3), \quad (3)$$

where V_{o} is the rms of phase to neutral voltage and ω is the angular frequency.

The first principle of the proposed three-phase inverter is to fold the three-phase voltages v_{u}, v_{v} and v_{w} at the output to match the terminal voltages v_+, v_-, and v_{n} from the positive, negative and neutral terminals respectively. Thus, the switching patterns of $S_3 \sim S_{14}$ are determined by the varying relations of the instantaneous values of the phase voltages v_{u}, v_{v}, v_{w}. First, the switches $S_9 \sim S_{14}$ are operated as a synchronous rectifier to enable reversed current flow from the positive and negative terminals to two phases with the highest and lowest voltages. Then, the switches $S_3 \sim S_8$ connect the neutral terminal to the other phase. For this reason, the proposed inverter requires six operating sectors with an equal interval of $\pi/3$ according to its rotating phase angle ωt. These sectors determine the switching sequences for $S_3 \sim S_{14}$ as shown in Table I, where '1' and '0' indicate 'ON' and 'OFF' conditions of the switching devices respectively. It should be noted that the bidirectional switches $S_3 \sim S_8$ are operated at double the line frequency while $S_9 \sim S_{14}$ only switch at line frequency.

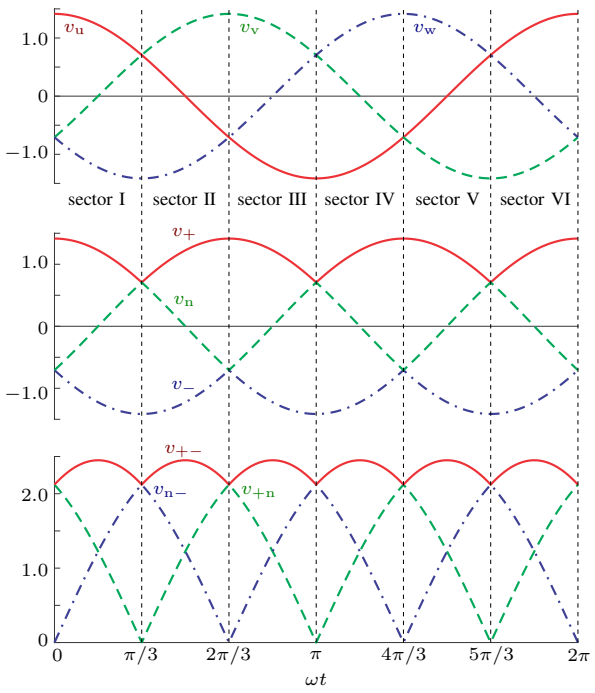

Fig. 2: Voltage folding principle of the proposed three-phase inverter. The voltage scales are displayed as per unit compared to the base value of output rms phase to neutral voltage V_{o}.

For examples, sector I is defined for the case when $v_{\mathrm{u}} > v_{\mathrm{v}} > v_{\mathrm{w}}$. Here, phase u is always positive and thus, is connected to the positive terminal via switch S_9. On the other hand, phase w is always negative and is connected to the negative terminal via switch S_{14}. The remaining phase v can have either positive or negative voltage, so it is connected to the neutral terminal via switches S_5 and S_6 which enable bidirectional output. As a result, the neutral terminal is floating with the middle phase voltage.

Fig. 2 illustrates how the sectors are allocated as well as how the terminal voltages look like. Notice that the voltages are normalized to the base value V_{o}. It is noted that v_+ at the positive terminal takes positive value while v_- at the negative terminal remains negative all the time

$$v_+ > 0, \quad (4)$$
$$v_- < 0. \quad (5)$$

The neutral terminal is floating, but it always takes a value between the positive and negative terminals as

$$v_+ > v_{\mathrm{n}} > v_-, \quad (6)$$

which is an important condition to implement the two boost converters because the output voltages of those

must be positive. Also, in a balanced three-phase system, the sum of those terminal voltages is zero as

$$v_+ + v_\mathrm{n} + v_- = 0. \tag{7}$$

The differences in terminal voltages

$$\begin{aligned} v_{+-} &= v_+ - v_- \\ v_{+n} &= v_+ - v_\mathrm{n} \\ v_{n-} &= v_\mathrm{n} - v_- \end{aligned}$$

determine the stress level on switching devices and indicate a selection guide for the switches. For examples, the maximum value of v_{+-} applies on $S_9 \sim S_{14}$, while the maximum value of v_{+n} and v_{n-} influences the stress voltages on S_1, D_1 and S_2, D_2 as well as $S_3 \sim S_8$ accordingly. Also, the minimum value of v_{+-} indicates the output of the boosting stages, which must be higher than the maximum input voltage from the PV panel. Therefore, the operating condition of input voltage is given by

$$V_\mathrm{PV} < \frac{3\sqrt{2}}{2} V_\mathrm{o} \approx 2.12 V_\mathrm{o}. \tag{8}$$

B. High-frequency switching operation

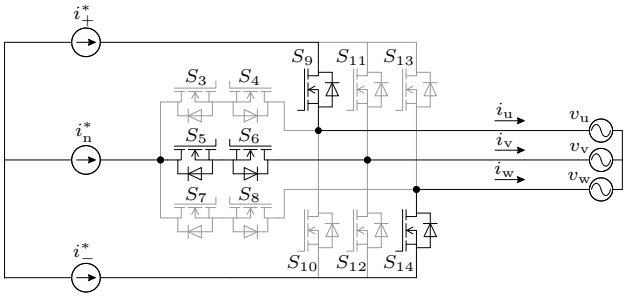

Fig. 3: Equivalent circuit of the proposed three-phase solar inverter for operation in sector I.

The three-phase inverter operates as a current source inverter with an unfolding operation determined by the aforementioned six operating sectors in Table I. Fig. 3 explains how the current unfolding operation is realized with the low frequency switches in section I. Considering the dc side as current sources which actually generate pulse currents. Their average values are determined by the references i_+^*, i_-^*, i_n^*. It can be seen that the phase currents in this sector is connected to the corresponding current sources so that

$$i_\mathrm{u} = i_+^* \tag{9}$$
$$i_\mathrm{v} = i_\mathrm{n}^* \tag{10}$$
$$i_\mathrm{w} = i_-^*. \tag{11}$$

The relationship from (9) $\sim$ (11) mean that the desired output currents can be used to extract the reference values for the input current sources. Similarly, applying the unfolding scheme for the other sectors, the full references for terminal currents at the dc side can be achieved.

Fig. 4 shows how a balanced three-phase currents with unity power factor determines the corresponding references for the terminal current sources via the switching

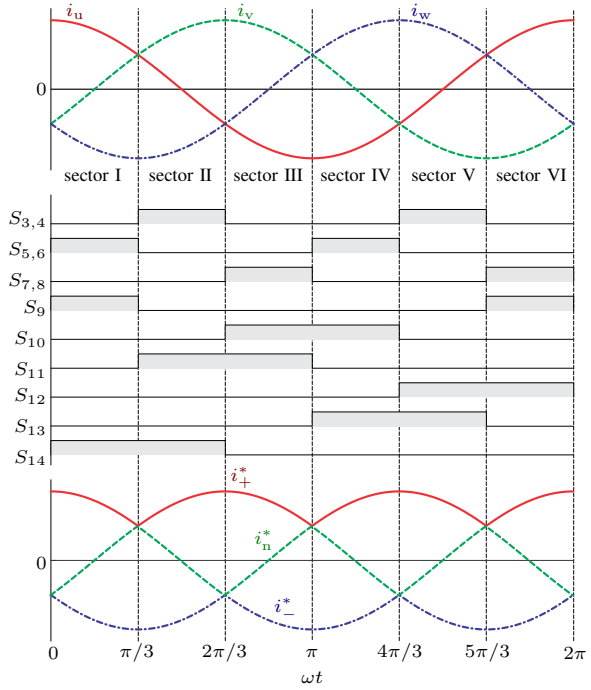

Fig. 4: Unfolding operation of i_+^*, i_n^*, i_-^* to form sinusoidal output three-phase currents i_u, i_v, i_w under unity power factor.

sequences shown in Table I. Notice that i_+^* is always positive and i_-^* always takes negative value so that the boost converters can provide appropriate duty cycles. The remaining neutral current can take either positive or negative value depending on the phase condition. Its value is automatically determined by Kirchhoff's current law as

$$i_\mathrm{n} = -i_+ - i_-, \tag{12}$$

and thus, we only need to control i_+ and i_- by adjusting the duty cycles in the two boost converters to achieve the final output three-phase currents.

C. Commutation transition in low-frequency switching operation

Since the low-frequency part of the proposed topology operates as a current source inverter, the output requires filter capacitor and the modulation needs overlap transition instead of blanking time in voltage source inverters. Fig. 5 shows the transition when changing from sector I to sector II. It can be seen that the positive terminal and neutral terminal are shorted because of two paths created by switches S_3, S_4, S_9 and S_5, S_6, S_{11}.

Ideally, this occurs exactly at $\omega t = \pi/3$ when $v_\mathrm{u} = v_\mathrm{w}$, thus $v_{+\mathrm{n}} = 0$ or there should not be any short-circuit problem. However, the overlap time is not zero in practice due to limitation in switching speed as well as to difficulty in synchronization of the ON/OFF timing. In addition, the voltage at the filter capacitor terminals are not the same as the phase voltages due to existing phase currents, e.g.

$$v_\mathrm{u} = v_\mathrm{Cu} + L_\mathrm{f} \frac{di_\mathrm{u}}{dt}. \tag{13}$$

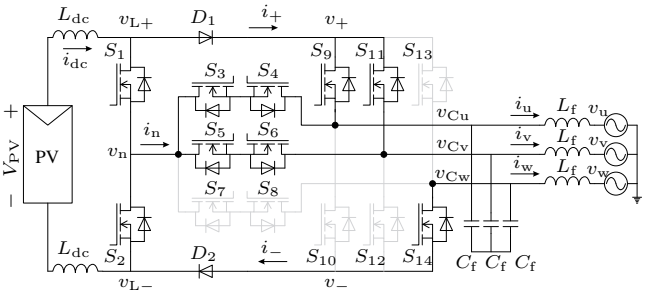

Fig. 5: Commutation transition in switching operation from sector I to sector II.

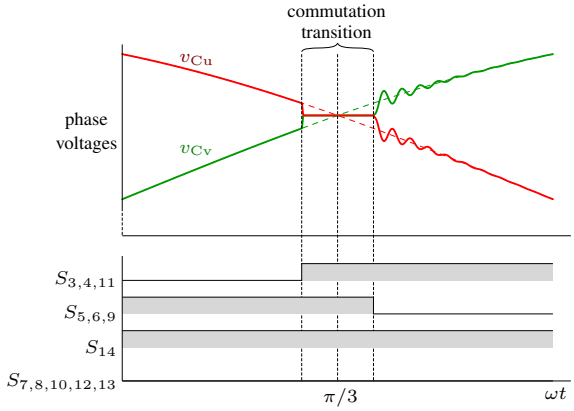

Fig. 6: Voltage waveforms during the commutation transition from sector I to sector II.

Therefore, the transition happens slightly before and ends after $\omega t = \pi/3$ as shown in Fig. 6. When the short circuit occurs, the phase voltage difference is quickly reduced to zero. As a result, the current at the positive terminal i_+ experience a temporary overshoot due to the short circuit. After the transition, the difference will appear again and will cause oscillation in both output voltage and current waveforms because of resonance between output filter capacitors and equivalent circuit inductors. This effect will be demonstrated later by simulation.

D. Active damping method

The aforementioned oscillation at the output due to current unfolding transition will cause distortion as well as increased THD. Thus, this paper proposes an active damping method using voltage feedback at the boost converters to reduce the unwanted effect.

Considering the boost converter at the input, a normal switching operation yields

$$\overline{i_{\text{out}}} = Di_{\text{in}}, \tag{14}$$

where D represents the 'ON' duty cycle of active switch in a boost converter circuit. If the output is connected to a capacitor, resonant oscillation will occur at certain operating conditions.

Fig. 7 illustrates a boost converter equipped with a parallel resistor R at the output. The output current

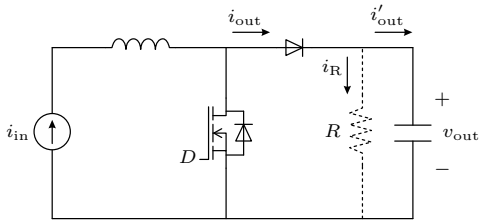

Fig. 7: A boost converter equipped with active damping resistor.

becomes

$$i'_{\text{out}} = i_{\text{out}} - i_{\text{R}}, \tag{15}$$

and thus,

$$\overline{i'_{\text{out}}} = Di_{\text{in}} - \frac{v_{\text{out}}}{R}. \tag{16}$$

This resistor R acts as a damping factor to suppress oscillation in the boost converter. However, real resistor will consumes power and thus increases power loss. Therefore, the duty cycle can be redefined as

$$D' = \frac{\overline{i'_{\text{out}}}}{i_{\text{in}}} = D - \frac{v_{\text{out}}}{i_{\text{in}}R}, \tag{17}$$

to provide active damping without real resistor. Unfortunately, this form will cause unwanted output current reduction which leads to distortion from sinusoidal reference. Thus, we only consider deviation from target value to suppress the unwanted oscillation. Equation (17) is therefore adjusted to be

$$D' = D - \frac{v_{\text{out}} - v^*_{\text{out}}}{i_{\text{in}}R}. \tag{18}$$

This duty cycle provides active damping at the output voltage without affecting the control for large signal.

E. Control method

Applying Kirchoff's voltage law at the dc side of Fig. 1 yields

$$V_{\text{PV}} - 2v_{\text{L}} = v_{\text{L+}} - v_{\text{L-}}, \tag{19}$$

where v_{L} is the voltage across each dc inductor and $v_{\text{L+}}$ and $v_{\text{L-}}$ are the voltages at the output of the upper and lower dc inductors, respectively. The voltage of each input inductor is determined by

$$v_{\text{L}} = L_{\text{dc}}\frac{di_{\text{dc}}}{dt}. \tag{20}$$

Therefore, the total input inductor voltage can be determined using feedback control of i_{dc} as follows

$$2v^*_{\text{L}} = K_{\text{dc}}(i^*_{\text{dc}} - i_{\text{dc}}). \tag{21}$$

At sector I, boosting operation at the positive terminal yields

$$v_{\text{L+}} - v_{\text{n}} = D_+ v_{+\text{n}} \tag{22}$$

$$i_{\text{u}} = i_+ = D_+ i_{\text{dc}}. \tag{23}$$

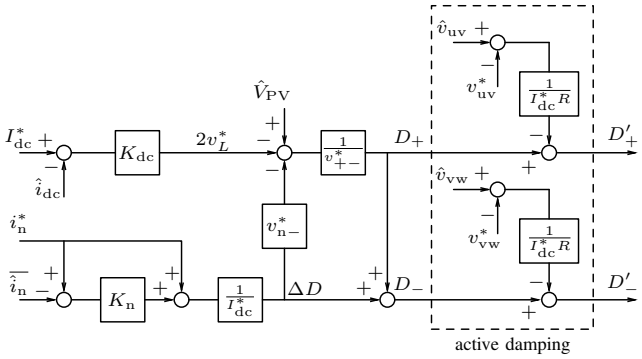

Fig. 8: Control block diagram of the three-phase solar inverter for operation in sector I.

Similarly at the negative terminal, we have

$$v_{\mathrm{L}-} - v_{\mathrm{n}} = -D_- v_{\mathrm{n}-} \quad (24)$$

$$i_{\mathrm{w}} = i_- = -D_- i_{\mathrm{dc}}. \quad (25)$$

The negative sign in the current equation (25) comes from the fact that i_- always takes negative value while i_{dc} is defined to be positive. Considering (12), the sum of (23) and (25) yields

$$i_{\mathrm{n}} = (D_- - D_+)\, i_{\mathrm{dc}} = \Delta D i_{\mathrm{dc}}, \quad (26)$$

where

$$\Delta D = D_- - D_+, \quad (27)$$

is the difference in duty cycles of the two boost converters. Thus, the neutral current i_{n} can be used to determined ΔD as follows

$$\Delta D = \frac{i_{\mathrm{n}}^*}{i_{\mathrm{dc}}^*} + K_{\mathrm{n}} \frac{i_{\mathrm{n}}^* - i_{\mathrm{n}}}{i_{\mathrm{dc}}^*}, \quad (28)$$

where the secondary part is neutral current feedback used for improving the shape of output currents.

Subtracting (22) to (24) yields

$$\begin{aligned} v_{L+} - v_{L-} &= D_+ v_{+\mathrm{n}} + D_- v_{\mathrm{n}-} \\ &= D_+ v_{+\mathrm{n}} + (D_+ + \Delta D) v_{\mathrm{n}-} \\ &= D_+ (v_{+\mathrm{n}} + v_{\mathrm{n}-}) + \Delta D v_{\mathrm{n}-} \\ &= D_+ v_{+-} + \Delta D v_{\mathrm{n}-}. \end{aligned} \quad (29)$$

Taking (19) into consideration, the duty cycle of the upper boost converter can be extracted from (29) as

$$D_+ = \frac{V_{\mathrm{PV}} - 2v_L - \Delta D v_{\mathrm{n}-}}{v_{+-}}. \quad (30)$$

The proposed inverter can be operated following the relations expressed by (19), (21), (27), (28), and (30). The control method for sector I is summarized in Fig. 8 where active damping expressed by (18) is also included.

TABLE II: Circuit parameters used in simulation

Symbol	Meaning	Value
V_{PV}	MPPT voltage of PV	300 V
V_{o}	output phase rms voltage	220 V
I_{o}	output phase rms current	28.2 A
f	line frequency	50 Hz
f_{sw}	switching frequency	20 kHz
L_{dc}	dc inductor	0.5 mH
L_{f}	ac filter inductor	0.2 mH
C_{f}	ac filter capacitor	20 μF

IV. Simulation Results

Circuit simulation was carried out to test the performance of the proposed inverter. The simulated circuit parameters are shown in Table II. The system is designed to operate at 20 kVA where the MPPT voltage of PV reaches around 300 V. The line frequency is set at 50 Hz, while the switching frequency of S_1, S_2 is set at 20 kHz to avoid acoustic noise. The dc inductors are chosen as 0.5 mH to limit the ripple at the PV input to less than 10% at rated power. The output filters were chosen to limit the current THD to less than 5% at rated condition. The overlap time for commutation in low-frequency switching operation is set to be 100 μs in the simulation.

Fig. 9 shows the operation of the proposed inverter without active damping control. The dc input current I_{dc} is controlled to have a stable value at 62 A. Given that the MPPT voltage is $V_{\mathrm{PV}} = 300$ V, the operating power reaches 18.6 kW. It can be seen that the average currents in i_+, i_{n}, i_- are not ideal due to overlap time implementation in switches $S_3 \sim S_{14}$. Due to the intrinsic glitches, the output currents i_{u}, i_{v}, i_{w} contains oscillating component that comes from resonance between the output filter capacitors and equivalent circuit inductors. Due to this oscillation, it is difficult to achieve a low THD at the output.

Fig. 10 shows the operation of the proposed inverter when active damping control was implemented. The average currents in i_+, i_{n}, i_- remains problematic, but the duty cycles D_+ and D_- are adjusted to be D'_+ and D'_- to damp the output oscillation. According to this active damping control, the output currents i_{u}, i_{v}, i_{w} contains minimal distortion caused by the overlap time. This proves the effectiveness of the proposed active damping control.

V. Experimental Results

A mini laboratory prototype was set up to demonstrate the proposed inverter. The PV panel was replaced with a dc voltage source. Its input voltage was set to 170 V so that it can provides enough power to run the three-phase load at 2.13 A. For the sake of simplicity in the feasibility test, the grid was replaced by a three-phase Y connected resistive load consisting of 40-Ω resistors as shown in Fig. 11. The circuit parameters used in the experiment is shown in Table III. Notice that the filter capacitors are

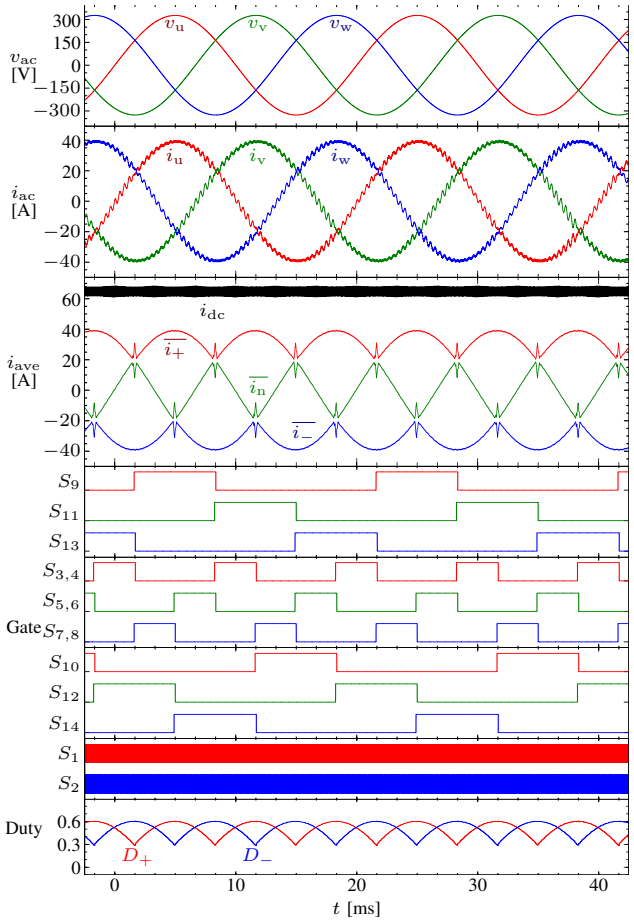

Fig. 9: Simulated waveforms of the proposed inverter without active damping control.

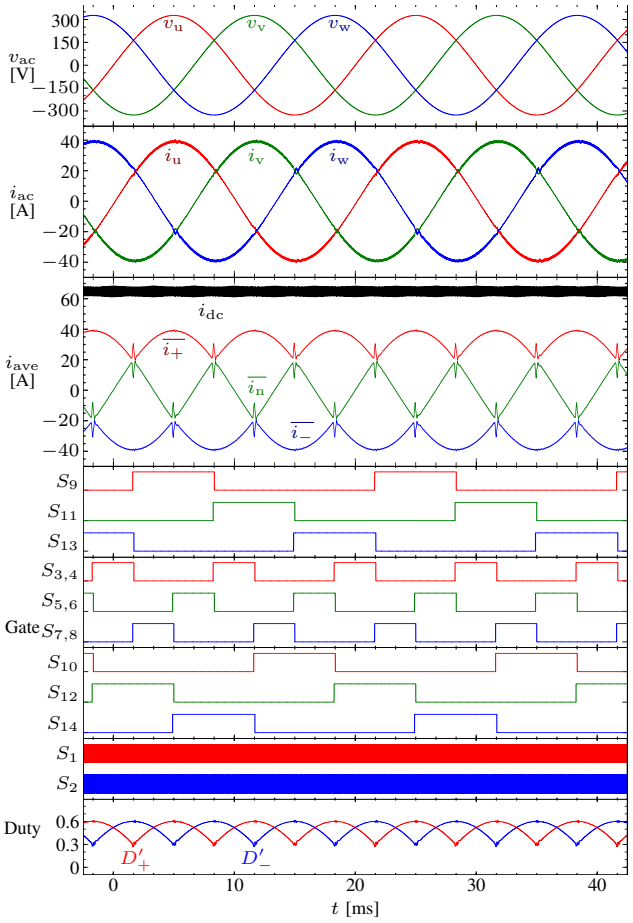

Fig. 10: Simulated waveforms of the proposed inverter when applying active damping control.

TABLE III: Circuit parameters used in experiment

Symbol	Meaning	Value
V_{in}	input voltage	170 V
V_o	output phase rms voltage	85 V
I_o	output phase rms current	2.13 A
f	line frequency	50 Hz
f_{sw}	switching frequency	20 kHz
L_{dc}	dc inductor	0.5 mH
C_f	ac filter capacitor	10 μF
R_l	load resistor	40 Ω

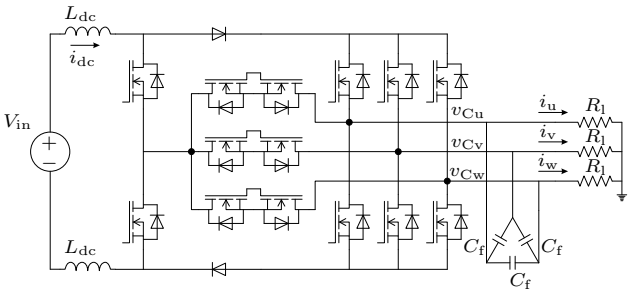

Fig. 11: Experimental setup for feasibility test of the proposed three-phase inverter.

delta connected and the experiment did not employ any filter inductor. The overlap time for commutation in low-frequency switching operation was set to be 25 μs in the experiment.

Fig. 12 shows the measured waveforms on a single phase when operating at 50 Hz. The measured filter capacitor voltage was almost sinusoidal but contained switching ripples due to pulsating output currents in the boost stage. The corresponding output ac current had less switching ripple compared to that of the capacitor voltage due to the presence of parasitic inductance in the resistive load and its connection. Since the parasitic inductance was negligible, the output voltage was proportional with the output current as $v_{Cu} = R_l i_u$ and thus in phase with the output current, resulting in unity power factor. The input current was controlled to have a constant average value at 3.1 A which is just a little above the maximum required output current of 3 A as a requirement for operating the boost converters.

VI. Conclusion

This paper proposed a boost integrated three-phase solar inverter using current unfolding method. The benefits of the proposed topology is that it needs only two high-frequency switches while does not require large output

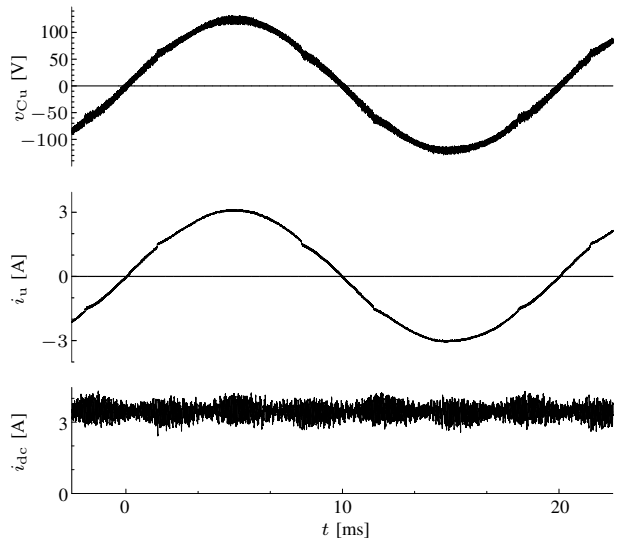

Fig. 12: Experimental verification of the proposed inverter when supporting a balanced three-phase resistive load.

ac inductors. The inverter employs 12 low-frequency switches for unfolding operation, but the conduction loss can be optimized thanks to their negligible switching losses. As a result, high efficiency and/or size reduction in passive components can be achieved.

This paper revealed that the overlap time in switching transition of the unfolding operation causes unwanted oscillation at the output currents. However, it is possible to suppressed the oscillation using active damping method. Simulation study presented stable operation of the proposed inverter and proved the effectiveness of the proposed active damping method. Finally, an experimental verification with resistive load was successfully carried out to confirm the feasibility of the proposed inverter.

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