Switched-Capacitor Integrated Single-Phase (2N+1)-Levels Boost Inverter for Grid-Tied Photovoltaic (PV) Applications

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***Abstract*— This paper presents a switched-capacitor integrated (2N+1)-level (N≥2) boost inverter for single-phase photovoltaic (PV) applications. It consists of N modular switching cells, where each cell consists of two switched capacitors and three active switching elements. A boost converter at the front side of the switching cells helps to maintain the capacitor voltage balance during different operation modes. With this arrangement, the inverter is capable to generate 2N+1 output voltage levels, and able to accommodate a wide range of input voltage. Detailed analysis followed by simulation and experimental results of a 5-level inverter as an example is presented to verify the proposed concept. Further, comparison with other multilevel inverter topologies is presented to show the merit of the proposed concept.**

Keywords- Photovoltaic (PV), multilevel inverter, switched-capacitor, grid-connected converter.

I. INTRODUCTION

Multilevel converter has attracted interest recently due to its high power-quality waveforms, low electromagnetic compatibility (EMC), low switching losses, and high-power capability. Due to this, it has drawn tremendous interests in a wide range of power conversion applications from low power (fraction of kW) to high power (MW level). Examples of such application are for grid-connected renewables, motor drives, electric vehicles, and telecommunication and data centers. Although multilevel has numerous advantages, the cost and size are still the main issue due to the high number of semiconductor devices with the increasing levels of output voltage. The most common type of multilevel inverters is cascade H bridge (CHB), capacitor clamed and diode clamped [1-3]. All these topologies use a large number of power devices, which reduces efficiency and power density. However, this challenge of improving efficiency has been rising swiftly recently. Therefore, many topologies have been proposed to focus on this challenge and overcome this pressing issue [4, 5]. Topologies with common-ground terminal significantly reduce the number of power devices, whilst nullifying the leakage current to the grid [5]-[7]. Similarly, multilevel converters, which clamp the common mode voltage (CMV) during the freewheeling period, have received more attention in the recent time for medium power PV applications as they adopt the concept of common ground for effective elimination of leakage current. However, the requirement of high dc-link voltage (800 V) in some of the conventional multilevel converters (neutral-point-clamped (NPC), active NPC (ANPC) and T type [8]-[10] demand higher voltage boost converter at the front side. Inverter with integrated voltage boost capability has been alternatively seen as a potential candidate for PV applications due to its wide input voltage range.

This paper presents a (2N+1)-level inverter which has boosting feature and uses a less number of semiconductor devices. The paper is organized as follows. Section II shows the circuit configuration, operation principle, and multilevel stages. Section III compares the proposed topology with existing five-level inverter topologies. Section IV shows simulation waveforms in MATLAB-Simulink with loss analysis and efficiency analysis using the PLECS toolboxes and the experimental results. The paper is summarized and concluded in Section V.

II. PROPOSED TOPOLOGY ANALYSIS

A. Circuit Configuration

The general configuration of the proposed novel multilevel converter with (2N+1) levels is shown in Fig. 1. The schematic consists of three parts: (1) at the front end is a DC-DC boost converter to boost the input voltage; (2) to increase the voltage level, the switches and switched-capacitors are used in the second stage, where each cell generates two extra voltage levels, and (3) at the end, the H-bridge inverter is used to convert the DC to AC. Fig. 2 displays the circuit schematic of an example 5-level inverter with the switching pulses which are generated by comparing the modulation and carrier signals. Successive cells for high levels (7-level, 9-level) share one of the capacitor from the antecedent cells, thereby reducing the number of required capacitors at higher levels. For example,

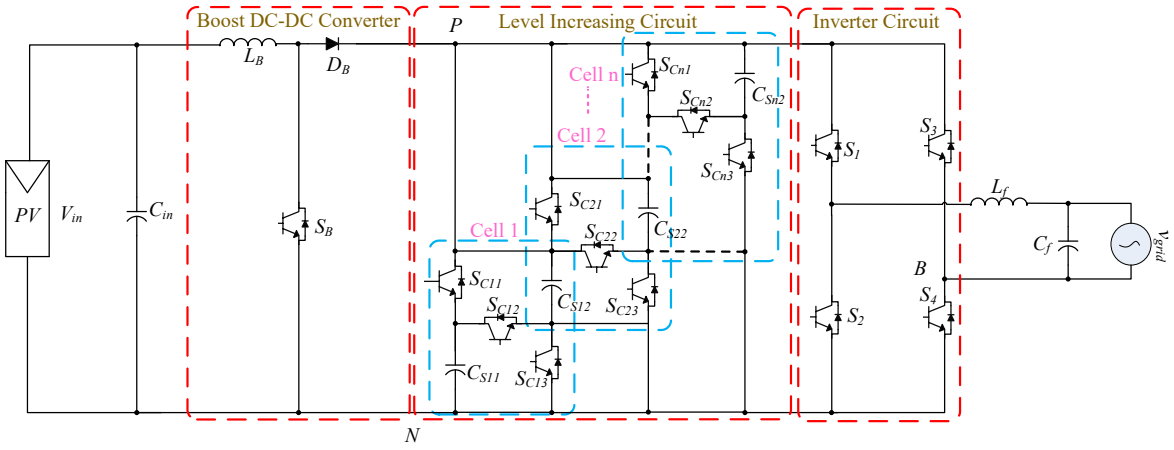

Fig. 1. Circuit schematic of the proposed (2N+1)-level inverter.

switching cells in 5-level consists of three switches and two capacitors, and 7-level consists of 6 switches and 3 capacitors. The input voltage is boosted with an integrated pre-boost stage and then followed by the switched-capacitor voltage boost stage. This integrated boost stage can also be used to track the MPPT of the PV module. As shown in Fig. 2(a), the 5-level inverter consists of voltage doubler circuit with three switches (S_{C1}, S_{C2} and S_{C3}) and two capacitors (C_{S1} and C_{S2}). The boost switch S_B is independent of the switching of the following voltage doubler and unfolding circuit. By appropriately switching the voltage doubler MOSFETs, a precise 2-level voltage ($\hat{V}_{PN}$ and $2\hat{V}_{PN}$) can be achieved before the unfolding circuit (S_1, S_2, S_3 and S_4).

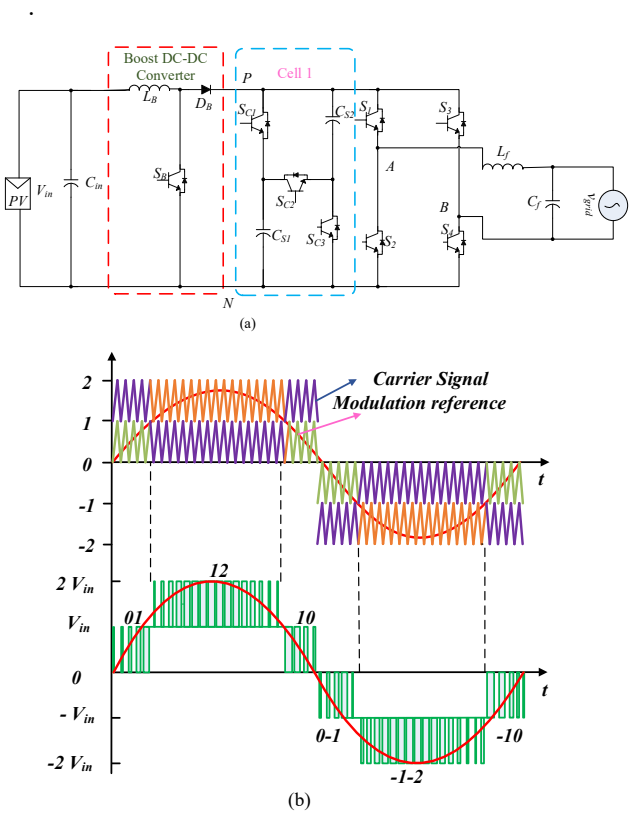

Fig. 2. (a) Circuit schematic of the proposed 5-level inverter, and (b) its modulation technique.

The required level of voltage in C_{S1} and C_{S2} can be precisely controlled by the duty cycle of the switch S_B. At the output side, a small LC filter is used to achieve the sine wave for load/grid connection. For the modulation, four level-shifted carrier signals with different amplitudes as shown in Fig. 2(b) (0 to 1, 1 to 2, -1 to 0, and -2 to -1) are used. Appropriate modulation signals are generated by comparing the signals with the reference signal. Using the voltage doubler circuit, a precise 2-level voltage (±1 and ±2) can be achieved before the unfolding circuit

B. *Multilevel Stages*

Fig. 3 explains the operating principle of multilevel stages. In the proposed topology, the level generating part is shown in Fig. 1. Each cell (see Fig. 1) generates two output voltage levels. The structural view of the cell is shown in Fig. 3(a), which consists of three switches and two capacitors. When the switches S_{C1} and S_{C3} are ON, the capacitors are charging for positive and negative cycle (see Fig. 3(b)). During the capacitor discharging time, the middle switch S_{C2} will be OFF. Therefore, the voltage is achieved from the output side, which is equal to half of the DC-link voltage. On the other hand, during the capacitor discharging time, the switches S_{C1} and S_{C3} are OFF, and the current flows through the switch S_{C2}. Additionally, PV panel is disconnected from the grid side. The achieved output voltage is equal to the DC-link voltage (see Fig. 3(c)). As a result, the level 2 and level -2 are generated by using the switch S_{C2} as shown in Fig. 2.

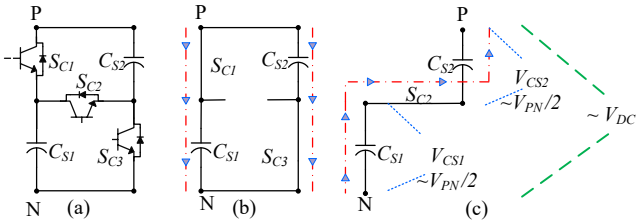

Fig. 3. (a) Illustration of the switching cell: (b) charging capacitor in parallel and simultaneously discharging them to create ±1 voltage levels, and (c) discharging capacitor in series to create ±2 voltage levels.

C. Operation Principle

The proposed circuit has six modes of operation. The switching state of the boost switch is independent of the switching states of the switching cell and the H-bridge. This flexibility helps to switch the boost switch at the high switching frequency and the following power stage at lower switching frequency. This helps to improve efficiency and power density of the converter. Fig. 4(a) and Fig. 4(d) show the disconnection between the input panel and the output grid. Therefore, the input current flows through the boost inductor L_B. The grid current flows through the switches S_1 and S_3 for the positive zero state (see Fig. 4(a)) and the switches S_2 and S_4 for the negative zero state (see Fig. 4(d)). Hence, the zero voltage is developed. After turning off the boost switch S_B, the boost

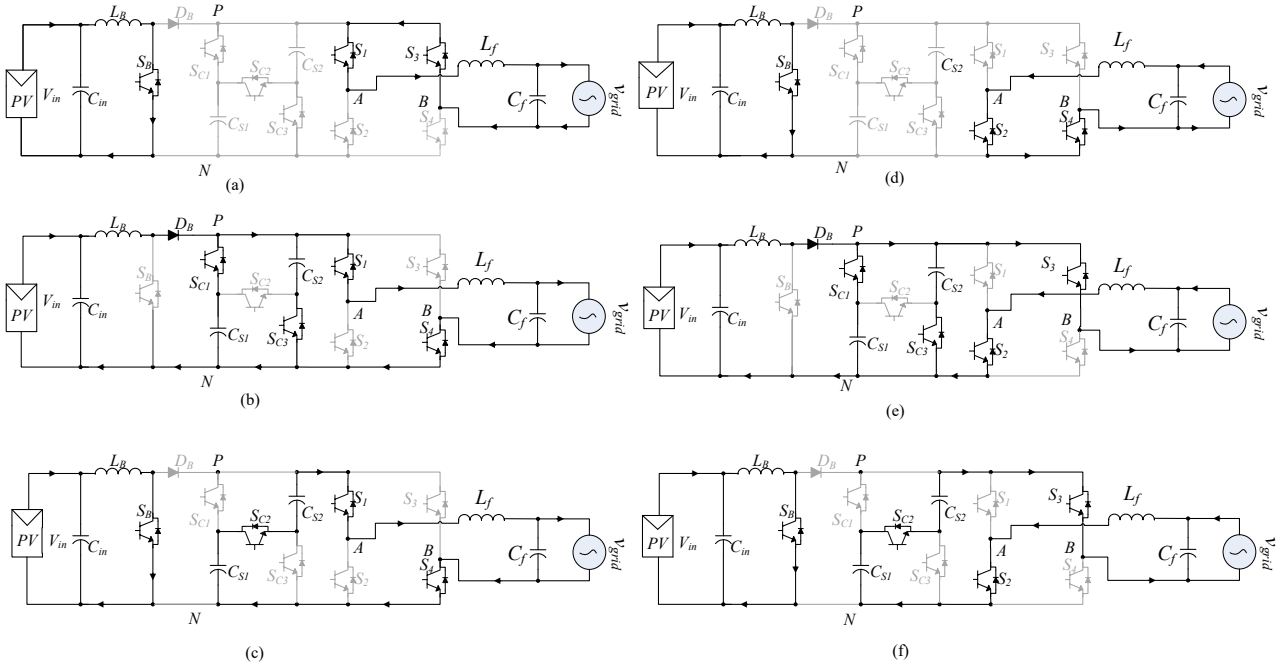

Fig. 4. Operational modes (a) level +0, (b) level +1, (c) level +2, (d) level -0, (e) level -1, (f) level -2.

TABLE I
COMPARISON BETWEEN VARIOUS SINGLE-PHASE FIVE LEVEL INVERTER TOPOLOGIES.

Name	Input voltage, Vin (V_{dc})	Output, V_{grid} (V_{ac})	Voltage level	Semiconductor devices		Additional devices		Extended ability	Need isolated DC sources	Boosting feature	Reactive power capability
				Diode	Switch	Inductor	Capacitor				
NPC	800	230/50 Hz	5	4	8	0	0	Yes	No	N/A	N/A
ANPC	800	230/50 Hz	5	0	8	0	1	Yes	No	N/A	N/A
T type	800	230/50 Hz	5	0	8	0	4	Yes	No	N/A	N/A
Diode clamped	400	230/50 Hz	5	12	8	0	4	Yes	No	No	Yes
Capacitor clamped	400	230/50 Hz	5	0	8	0	10	Yes	No	No	Yes
Cascaded H-bridge	400	230/50 Hz	5	0	8	0	0	Yes	Yes	No	Yes
Topology in [11]	400	230/50 Hz	5	0	10	0	3	No	No	No	Yes
Topology in [12]	400	230/50 Hz	5	0	10	0	3	No	Yes	Yes	N/A
Topology in [13]	400	230/50 Hz	5	0	13	0	4	No	No	No	N/A
Topology in [14]	150	110/60 Hz	7	2	7	0	3	No	Yes	No	N/A
Topology in [15]	400	230/50 Hz	9	4	8	0	4	No	No	No	N/A
Topology in [16]	400	230/50 Hz	5	2	6	0	2	No	Yes	No	Yes
Topology in [4]	200	230/50 Hz	5	0	10	0	3	No	No	Yes	Yes
Topology in [5]	200	240/60 Hz	5	1	8	0	3	No	No	Yes	Yes
Proposed Inverter	100	230/50 Hz	5	1	8	1	2	Yes	No	Yes	Yes

diode D_B works in forwarding bias, and the current flows through the switch S_{C1} and S_{C3}. Therefore, the switched capacitors are charging and the grid current flows through the switches S_1 and S_4 for the positive cycle (see Fig. 4(b)) and switches S_2 and S_3 for the negative cycle (see Fig. 4(e)). The dc-link voltage is variable (in steps), where the peak of dc-link voltage $\hat{V}_{PN}$ can be calculated using (1) as

$$\hat{V}_{PN} = \begin{cases} \frac{V_{in}}{1-D_b}, \text{when } S_{C1} = S_{C3} = 1 \text{ and } S_{C2} = 0 \\ \frac{2\,V_{in}}{1-D_b}, \text{when } S_{C1} = S_{C3} = 0 \text{ and } S_{C2} = 1 \end{cases} \quad (1)$$

The switched-capacitors discharge through the switch S_{C2} where the output voltage is made double the voltage of each capacitor ($\frac{V_{in}}{1-D_b}$) in both the positive (see Fig. 4(c)) and the negative (see Fig. 4(f)) half cycle. In the ideal circumstance, the proposed inverter has five output voltage levels: $\pm\frac{V_{in}}{1-D_b}$, $\pm\frac{2\,V_{in}}{1-D_b}$, and 0. The output voltage of the inverter can be written as:

$$v_{ac} = \hat{V}_{ac}\,\mathrm{Sin}(\omega t + \varphi) \quad (2)$$

$$\hat{V}_{ac} = 2\frac{V_{in}}{1-D_b} \quad (3)$$

From (3), the overall voltage gain G can be written as:

$$G = \frac{\hat{V}_{ac}}{V_{in}} = \frac{2}{1-D_b} \quad (4)$$

In general, the voltage gain of the (2N+1)-level novel multilevel converter can be written as:

$$G = \frac{\hat{V}_{ac}}{V_{in}} = \frac{N}{1-D_b} \quad (5)$$

where, N = 2 for 5-level, N = 3 for 7-level and N = 4 for 9-level inverter. Fig. 5 shows the theoretical voltage gain curve of the inverter for the corresponding 5-level, 7-level and 9-level inverters.

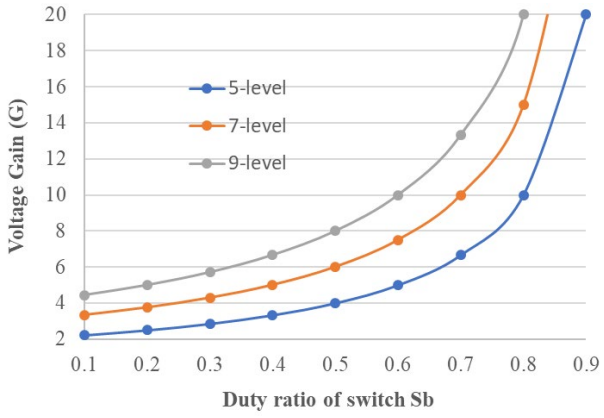

Fig. 5. Theoretical voltage gain curve of 5-level, 7-level and 9-level inverters.

III. Comparison with Existing Multilevel Inverters

Multilevel inverter is widely applicable in both academic and industrial applications, and the research in this area is spreading up rapidly. However, the foremost challenging and focusing area is to reduce the number of semiconductor devices in the inverter topology to improve efficiency and power density. Recently, some topologies have been invented with less semiconductor devices, but those topologies are not capable to increase the number of voltage at the output. On the other hand, a few topologies have been presented in different papers which require only half of the input voltage compared to the conventional topologies to achieve 230 V_{ac} [4] [5]. Table I illustrates the comparison of different single-phase multilevel inverter topologies in terms of the input voltage, power semiconductor devices, level extended ability, boosting feature, and reactive power capability. The NPC inverter is constructed by eight power switches and four diodes to achieve five levels, while ANPC and T-type five-level inverter have no requirements of diodes. Instead, they require additional capacitors. Moreover, they require 2 V_{PN} input supply voltage to produce the 230 V_{ac} signal. The diode clamped, capacitor clamped, and CHB use eight power switches; however, the diode clamped requires extra four capacitors and 12 diodes to achieve five levels in the output voltage. Moreover, CHB needs isolated DC sources. On the other hand, few topologies are compared in this table which have boosting feature and less semiconductor devices. In summary, it is to be noted that the proposed topology needs only 100 V_{dc} input voltage with the reasonable boost duty cycle of 50% which also helps to track MPP. In addition, the required components for a 5-level inverter are one diode, one inductor, two capacitors and eight power switches.

IV. Result and Discussion

This section is divided into two sub-sections. One sub-section presents the software based simulation result and experimental verification. Another sub-section is the loss calculation and efficiency evaluation.

For precisely verifying the simulation result, the same parameters (see Table II) are taken for both the simulation and experiment. The same parameter has been chosen for loss calculation as well.

Table II
Parameters and Components Used for Simulation and Prototype Design.

Description	Values/parameter used
Input Voltage V_{in}	100 V_{dc}
DC link Voltage V_{DC}	358 V_{dc}
Output Voltage V_{grid}	220 V_{ac}
Rated Power P_o	500 VA
Switching Frequency(f_{sw})	20 kHz
Line frequency	50 Hz
Boost Inductor (L_B)	0.9 mH
Boost Diode (D_B)	C5D50065D
Switched Capacitors (C_{S1} and C_{S2})	680 µF (LLS2E681MELA)
Switches (S_B, S_{C1}, S_{C2}, S_{C3}, S_1, S_2, S_3 and S_4)	SCT3022ALGC11
Filter inductor (L_f)	0.68 mH
Filter Capacitor (C_f)	4.7 µF
Load	105.4 Ω
Controller	sb-RIO GPIC

A. Simulation and Experiment Results

To validate the above theoretical findings, computer simulations are carried out in MATLAB-Simulink using the PLECS toolboxes as shown in Fig. 6. The inverter output is filtered out by a small filter to get a pure sinusoidal voltage and current at the load side, and the front stage boost DC-DC converter helps to reduce the input applying voltage. Fig. 6(a) shows the input applying voltage, 5-level inverter output voltage, output voltage and current after applying the small filter, and the voltages across the switched-capacitors. Fig. 6(b)

shows the voltage across each switch and the voltage stress on semiconductor devices are $\left(V_{SB} = V_{S1} = V_{S2} = V_{S3} = V_{S4} = \hat{V}_{PN},\ V_{Sc1} = V_{Sc2} = V_{Sc3} = \frac{\hat{V}_{PN}}{2},\ \text{and}\ V_{DB} = \hat{V}_{PN}\right)$.

To verify the concept of the proposed circuit, the experimental setup (see Fig. 7(a)), and the experimental waveform of input voltage, output voltage, and current is demonstrated in Fig. 7(b) where all eight power switches are implemented using 650 V SiC MOSFETs, and individual heatsinks are used to cool the devices.

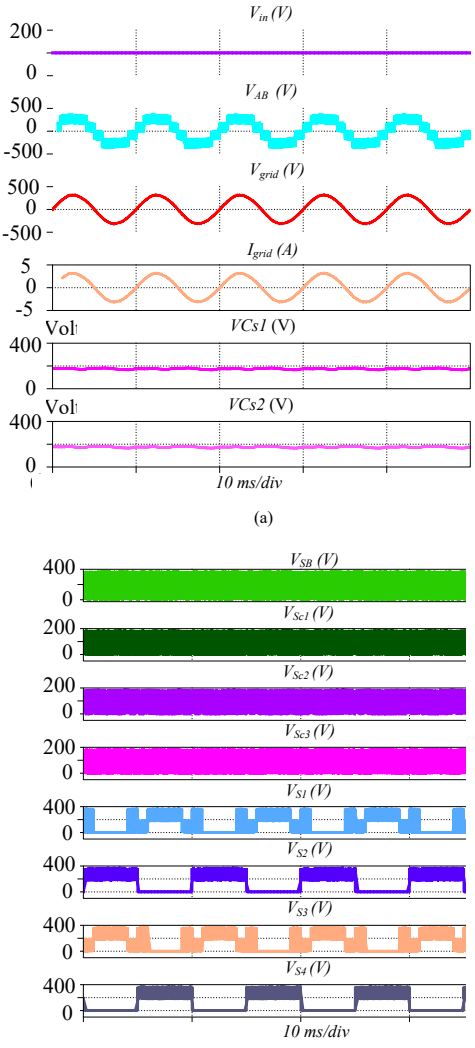

Fig. 6. Simulated waveforms of the proposed five-level inverter.

Electrolytic capacitors are used for the implementation of switched-capacitors. Moreover, the gate drive circuits are setup at the bottom of the PCB board and the control signals are generated by the sb-RIO GPIC controller from National Instrument. This controller is interfaced with LabVIEW software and operates the switching pulses through the LabVIEW software. The resistive load is 105.4 Ω. The achieved output grid voltage is RMS 212 V and the grid current is RMS 1.7 A.

B. Loss Calculation and Efficiency Evaluation

Calculation of losses is a very crucial part of the inverter design. In the multilevel inverter, current can flow in three modes such as blocking mode, conduction mode and switching mode. No current flows through the blocking modes, and therefore no losses are resulted in this mode. As a result, the maximum losses occur in the other two modes. Here the total power loss (P_{total}) (see (6)) is the summation of the conduction losses (P_{CL}) and switching losses (P_{SL}).

$$P_{total} = P_{CL} + P_{SL} \tag{6}$$

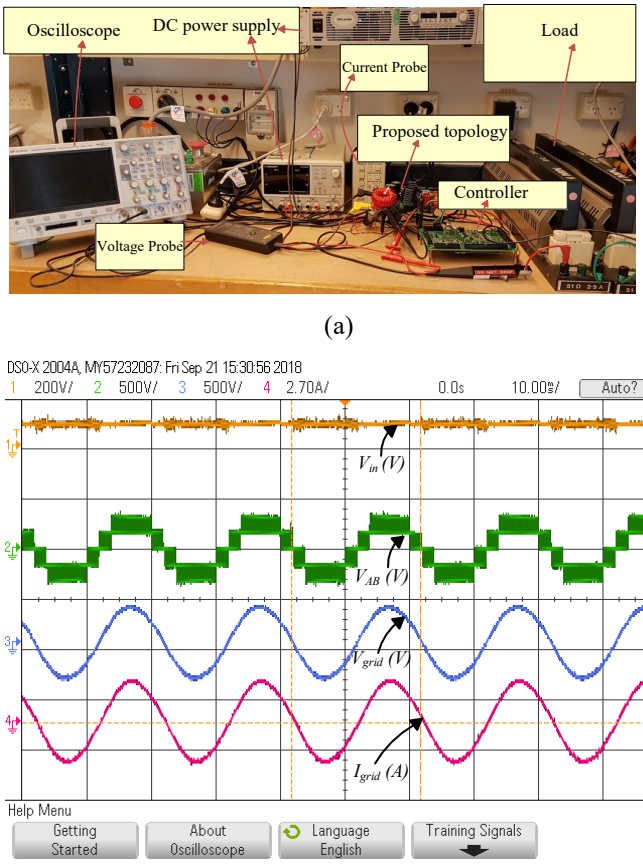

Fig. 7. Proposed 5-level inverter topology: (a) photo of the test bench, and (b) experimental waveforms showing input and output voltage and current.

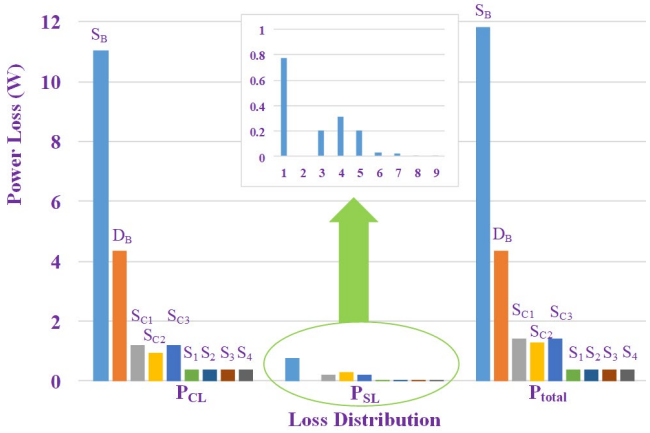

Fig. 8. Simulated result of loss in individual semiconductor devices.

Fig. 8 illustrates the semiconductor device losses in both conduction and switching modes. The maximum losses occur through the boost switch (S_B) and diode (D_B). In the level-increasing part, switch S_{C2} has the maximum loss for both modes (conduction and switching) compared to the other two level-increasing switches (S_{C1} and S_{C3}).

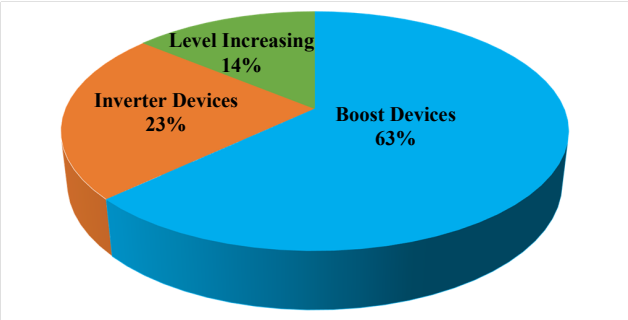

Fig. 9. Loss analysis of different components of the inverter.

The maximum losses occur in the boost part especially through the boost switches. More than 60% losses are resulted over the semiconductor devices (S_B and D_B) of the boost converter, and the rest 37% losses happens in H- bridge inverter devices ($S_1 - S_4$) and level increasing devices (S_{C1}, S_{C2}, and S_{C3}) (see Fig. 9).

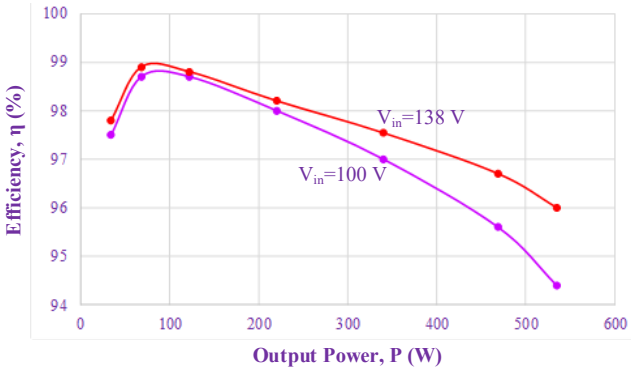

Fig. 10. Efficiency evaluation of the inverter at different input voltage levels.

The maximum efficiency is around 99%, which occurs at 8% of the load. At the rated power level of 500 W, the efficiency is above 94.5 % for 50% boost duty cycle while it reaches 96% for 30% boost duty cycle as shown in Fig. 10.

V. Conclusion

A novel (2N+1)-level single-phase switched-capacitor integrated boost inverter topology is presented where N switching cells are required. Each switching cell of this topology leads to two output voltage levels. For instance, a five-level inverter uses eight power switches, two capacitors, one inductor, one diode, and a small LC filter at the output. In this paper, the proposed topology is briefly analysed with the schematic diagram and the operation principle. Furthermore, the proposed topology is compared with other existing multilevel inverters. The key simulation waveforms and the experimental results are presented. Further, switching and conduction losses are calculated properly for each semiconductor devices and finally the efficiency is evaluated for 30% and 50% boost duty cycle.

The losses are same for switch S_{C1} and S_{C3} as these two switches are operated with same switching pulses. The losses for the H-bridge switches are quite same for individual four switches.

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