Novel High Efficiency H-Bridge Transformerless Inverter for Grid-Connected Single-Phase Photovoltaic Systems

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***Abstract*— This paper proposes a new H-bridge type transformerless inverter for grid-connected photovoltaic (PV) application. The proposed H-bridge zero voltage switch controlled rectifier (HB-ZVSCR) inverter uses additional switches and diodes at the AC side with voltage clamping feature to the DC midpoint. Main characteristics of the proposed inverter are the high conversion efficiency and low leakage current, which make it a suitable candidate for grid-connected PV applications. The analysis and operating principles of the proposed inverter are discussed in details. This theoretical findings has been simulated using PLECS software to verify the common mode voltage (CMV) and leakage current behaviors and the results are compared with similar existing midpoint voltage clamping inverter topologies (i.e. HB-ZVR and HB-ZVR-D). Furthermore, power loss and efficiency of the proposed inverter have been evaluated and compared with existing topologies.**

Keywords*— *PV panel, H-bridge, transformerless inverter, CMV, HB-ZVR, HB-ZVR-D, power loss, efficiency.

I. INTRODUCTION

Photovoltaic (PV) systems can be utilized in both stand-alone and grid-connected modes of operation. In stand-alone systems the PV panel should supply the power directly to load or electrical appliance and in grid-connected systems the PV panel provide the power into the utility grid in different distribution and consumption levels [1]. In grid tied application, the most common way to interface the DC electric energy of PV panel and the AC load side of the utility grid is through utilization of full bridge voltage source inverter (VSI). This topology can be operated in two-level switching scheme (i.e. bipolar modulation) where the efficiency is relatively low due to the increased power losses (core and switches), and in three-level switching scheme (i.e. unipolar and hybrid modulation) where the efficiency is more than the two-level one [2]. The main advantage of using non-isolating inverter topologies is its high conversion efficiency, low implementation cost and small size [3]. Nevertheless, the challenging part is common mode (CM) issues, i.e. leakage current flow through parasitic capacitor in between PV panel to ground and varying common mode voltage (CMV). There are many safety standards that introduce the grid requirements for grid-connected transformerless inverters. For example, standards DIN VDE V 0-126-1-1 and IEC62109-2 define the amount of allowed residual current below 300 mA when the PV panel is connected to the grid and the PV inverter should be disconnected if it exceeds the current limit [4]. Moreover, the residual current is the reason of the increased total harmonic distortion (THD) of the grid current, system losses and electromagnetic interference (EMI) [1]. To eliminate the CM leakage current during the freewheeling period, semiconductor devices (switches and diodes) can be added into a full bridge inverter either at the AC or DC side, and hence the topologies are classified as AC decoupling and DC decoupling based inverters such as HERIC, H5, H6, and hybrid coupling [5-8]. However, these decoupling techniques cannot completely eliminate the CM current, which is due to the junction capacitors of the power switches that introduce some amount of CM current. As a result, some active midpoint clamping based inverter topologies have been proposed for reducing leakage current effectively, i.e. HB-ZVR, HB-ZVR-D, oH5, PN-NPC, H5-D [9-13]. These topologies require two DC-link capacitors with extra switches for clamping purposes.

In this paper, a new H-bridge inverter is introduced with two extra switches and four rectifier diodes. The proposed topology named H-bridge zero voltage switch controlled rectifier (HB-ZVSCR) is based on the voltage clamping method where two DC-link capacitors are utilized at the DC side to eliminate the CM leakage current during the freewheeling period. The main idea of this topology is based on the well-known HB-ZVR topology with some changes in the semiconductor switches through the addition of two extra unidirectional switches to make the freewheeling current path smooth. The proposed topology can achieve a constant CMV and hence a low CM leakage current, in addition to low power losses and high conversion efficiency.

In the following section of this paper, the safety content of single-phase grid-tied transformerless PV inverters is analyzed. In Section III, the proposed

transformerless inverter is introduced and its operating modes are discussed in Section IV. The simulation results of the proposed inverter have been presented in Section V with a qualitative comparison with the related existing topologies. In Ssection VI, power loss and efficiency analysis are investigated for some similar midpoint CMV clamping based topologies. Finally, the paper is concluded in Section VII.

II. Common Mode Issue Analysis

Grid-connected PV systems need special attention to satisfy grid codes and standards. Hence, international agencies have regulated some broadly accepted standards for PV systems, which have to be accepted to avoid safety issues. On the other hand, the parasitic capacitor (C_{PV}) in grid-connected transformerless inverter has a critical impact on its performance. Fig. 1 illustrates the role of C_{PV} in a grid-connected PV cells. PV panels are comprised of the combination of glass, Ethylene-Vinyl Acetate (EVA), back sheet (Tedlar), and aluminium frame, in which a stray capacitance will be created from the PV cell to the frame, to the rack and to the ground.

Moreover, in the transformerless PV inverter, a CM resonant circuit can be created between the parasitic capacitor of PV module and output filter inductors at the grid side, which can cause severe problems such as high ground current and its subsequent problems [9], [14]. Furthermore, the role of output filter in the resonant circuit and its proper selection have to be investigated to clearly understand the CM behavior of the system. Therefore, the mentioned problems will be discussed in the following of this section.

In transformerless inverters, there is galvanic connection between the PV panel and the grid, and hence a resonant circuit can be created between the parasitic capacitor and the output filters of the inverter. Fig. 2(a) illustrates the general structure of single-phase transformerless inverters where the source of resonant circuit is indicated. This circuit comprise of the filter inductors (L_1, L_2), C_{PV} and the CM leakage current (I_{CM}). The power circuit in Fig. 2(a) can be replaced with phase voltages the inverter V_{an} and V_{bn}, which are equal to the potential of "a" and "b" points relative to the neural point "n", respectively (see Fig. 2(b)) [7, 15-17]. The CMV and differential-mode voltage (DMV) can be written based on phase voltages as follows

$$V_{CM} = \frac{V_{an} + V_{bn}}{2} \tag{1}$$

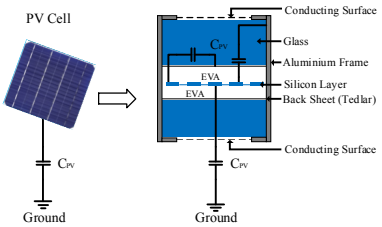

Fig. 2. Parasitic capacitance in PV panels [14].

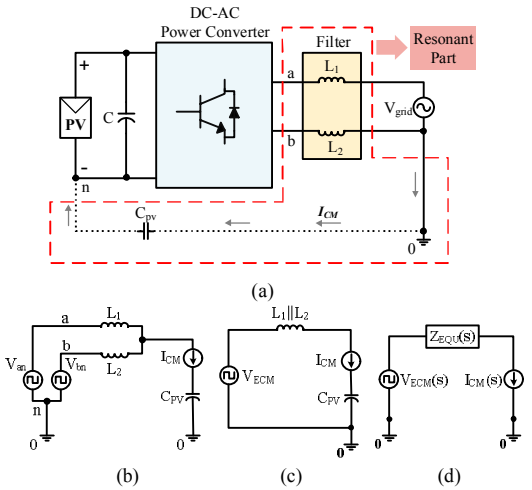

Fig. 1. CM equivalent circuit of a generalized transformerless inverter (a) transformerless inverter, (b) the resonant circuit, (c) considering series connection of components, (d) the s-domain equivalent circuit.

$$V_{DM} = V_{an} - V_{bn} \tag{2}$$

Moreover, the phase voltages can be expressed based on VCM and VDM as mentioned in (3) and (4).

$$V_{an} = V_{CM} + \frac{V_{DM}}{2} \tag{3}$$

$$V_{bn} = V_{CM} - \frac{V_{DM}}{2} \tag{4}$$

To better understand the CM behavior, the equivalent circuit can be simplified in a single loop circuit as shown in Fig. 2(c). The equivalent CMV (V_{ECM}) shown in this figure can be obtained as

$$V_{ECM} = V_{CM} + \frac{V_{DM}}{2}\frac{L_2 - L_1}{L_1 + L_2} \tag{5}$$

The magnitude of the I_{CM} mainly depends on the amount of parasitic capacitance and the amplitude and frequency of the CMV, whose fluctuation can produce large I_{CM}. In order to avoid the I_{CM}, the second part of (5) should be equal to zero, which is dependent on the circuit topology. Moreover, the equivalent CMV has to remain constant in each switching period to reduce the I_{CM}. The effect of DMV can be eliminated in symmetrical topologies like H-bridge inverter by using two identical inductor filter at the output (i.e. $L_1 = L_2$) [7], [15]-[17]. The simplified equivalent CM circuit including the equivalent impedance (Z_{EQU}) is shown in Fig. 2(d).

III. The Proposed Transformerless Inverter

The proposed transformerless inverter (HB-ZVSCR) is shown in Fig. 3(a). The main advantages of the proposed topology is the effective reduction of CM issues with considerably increase in the conversion efficiency. This topology is a modified topology of both HB-ZVR and HB-ZVR-D inverters. HB-ZVR-D is a modified version of HV-ZVR by adding an extra fast-recovery diode and a voltage divider at the DC side that is made up

by two DC-link capacitors. The proposed topology replaces these two diodes with two extra switches and removes the bidirectional switches of HB-ZVR. Hence, the power losses are reduced and an effective freewheeling path is created by rectifier diodes and the extra switches.

The modulation pulses of the proposed inverter are shown in Fig. 3(b). The presented topology has six switches and four diodes. The switches Q_1 to Q_4 working as an H-bridge inverter and the switches Q_5 and Q_6 with rectifier didoes (H-bridge diodes) are used at zero voltage states. Hence, IGBTs (Q_5 and Q_6) are used with one diode bridge rectifier to complete the freewheeling path in both positive and negative cycles.

IV. Analysis and Operating Modes

The proposed inverter has four operational modes that are shown in Fig. 4(a) to Fig. 4(d). The mode 1 is an active state of the positive half cycle (see Fig. 4(a)). In this cycle, Q_1 and Q_4 are conducting, and other switches and diodes are OFF,d the current flows through the filter and load. As a result, the voltage in between point "a" to the neutral (n) is equal to the input voltage (V_{PV}). On the other hand, in mode 2, Q_2 and Q_3 are active in the negative half cycle (see Fig. 4(b)). Hence, the voltage between point "b" to the neutral (n) is equal to V_{PV}. The freewheeling path for the positive cycle is demonstrated in Fig. 4(c). Moreover, the diodes D_2, and D_3 are forward biased and hence both are ON, and the output current flows through these two diodes and the switches Q_5 and Q_6. In the negative half cycle, the freewheeling path is demonstrated in Fig. 4(d). The other two diodes are in forward mode, and the current goes through D_1, D_4 and the switches Q5 and Q6. At the positive and negative half cycles, the voltage at point "b" to "n" and "a" to "n" are zero. Therefore, the CMV is equal to the half of the input voltage (see (6) to (8)).

$$V_{CM}(\text{positive half cycle}) = \frac{V_{pv} + 0}{2} = \frac{V_{pv}}{2} \quad (6)$$

$$V_{CM}(\text{negative half cycle}) = \frac{0 + V_{pv}}{2} = \frac{V_{pv}}{2} \quad (7)$$

$$V_{CM}(\text{zero Vector states}) = \frac{\frac{V_{PV}}{2} + \frac{V_{PV}}{2}}{2} = \frac{V_{pv}}{2} \quad (8)$$

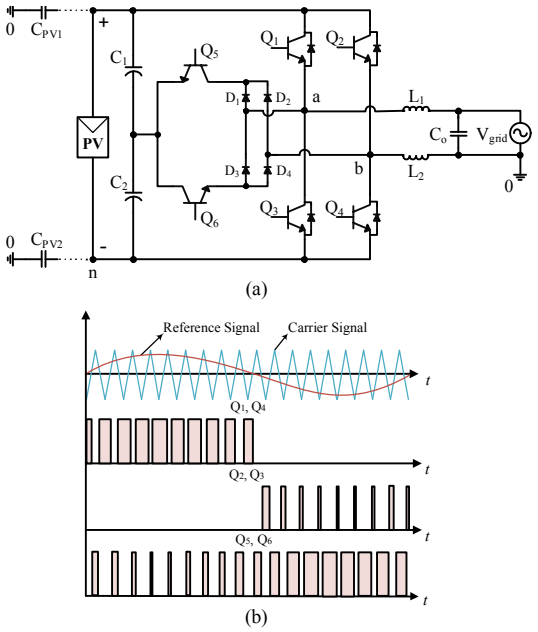

Fig. 4. The proposed H-bridge transformerless inverter, (a) circuit configuration of HB-ZVSCR, and (b) its switching pattern.

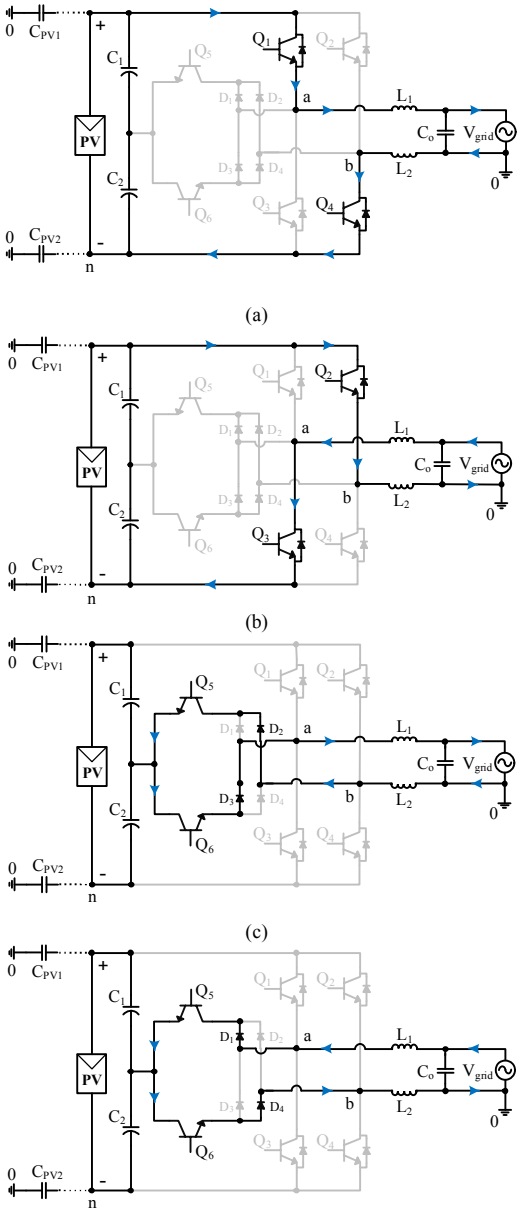

Fig. 3. Operating modes of HB-ZVSCR inverter, (a) mode 1, (b) mode 2, (c) mode 3, and (d) mode 4.

TABLE I
SWITCHING SEQUENCES OF THE MODULATION STRATEGY FOR HB-ZVSCR

Voltage Vector	Q1	Q2	Q3	Q4	Q5	Q6	D1	D2	D3	D4
(+VO)	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
(-VO)	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Zero	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	ON	OFF
Zero	OFF	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	ON

Table I shows the modulation strategy of HB-ZVSCR. In the positive half cycle, the switches Q_1 and Q_4 are ON and the other switches are OFF. Therefore, the positive output voltage ($+V_O$) is achieved, In the freewheeling period D_2 and D_3 rectifier diodes are ON with the switches Q_5 and Q_6 that is zero voltage vector (Zero) states In the negative cycle, another zero voltage vector state occurs with the negative output voltage ($-V_O$).

V. Simulation Results

Simulations was carried out in PLECS software with the parameters displayed in Table II. The simulation are performed for different similar topologies to analyze the operation and overall performance of the similar inverters. The PV array is simulated with DC voltage source (V_{pv}) of 400 V. The stray capacitor (C_{pv1}, C_{pv2}) is modeled with two capacitors of 75 nF value, each connected between the PV terminal and the ground. The ground resistance (RG) is 5 Ω. The filter is made up of two equal inductors (L_1, L_2); each having a value of 3 mH. The grid line to neutral voltage (V_{grid}) is 230 V (rms) with frequency (f_g) of 50 Hz. The switching frequency (f_{sw}) is 20 kHz. The simulation results including the output waveforms and CM behaviors (CM voltage and current) of CMV clamping based topologies (i.e. HB-ZVR, HB-ZVR-D, and proposed HB-ZVSCR) are shown in Fig. 5(a) to Fig. 5(c). It is clear that the CM voltage of HB-ZVR-D and HB-ZVSCR are constant, and hence their CM leakage current are much lower than HB-ZVR. Moreover, the CM current in HB-ZVSCR is smoother than HB-ZVR-D.

TABLE II
PARAMETERS USED FOR SIMULATIONS

Parameter	Value
Input Voltage (V_{pv})	400 V dc
Output Load	50 Ω
Output Voltage (V_{grid})	230 Vac
Line Frequency (f_g)	50 Hz
Output Current (Io)	4.68 A
Modulation Index (M)	0.82
Rated Power	1 kVA
Switching Frequency (f_{sw})	20 kHz
DC bus Capacitor (C_1, C_2)	1600 µF
Filter Capacitor (C_o)	2.2 µF
Filter Inductor (L_1, L_2)	3 mH
Parasitic Capacitor (C_{pv1}, C_{pv2})	75 nF
Switches Q_1 to Q_4 (IKW30N60DTP)	V_{CE}=600 V, I_C=30 A
Switches Q_5 and Q_6 (IRGP4640PBF)	V_{CE}=600 V, I_C=40 A
Diodes D_1 to D_4 (APT15D60B)	V_F=600 V, I_F=32 A

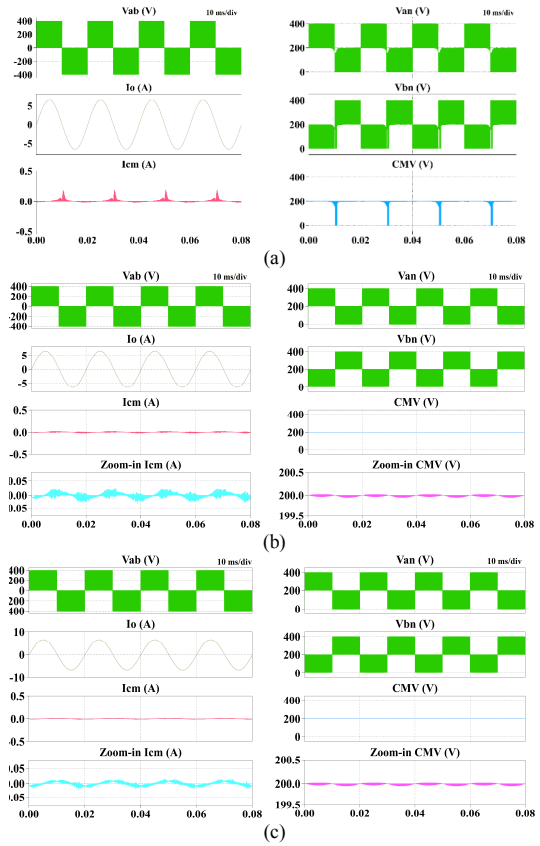

Fig. 5. Simulation results of (a) HB-ZVR inverter, (b) HB-ZVR-D inverter, and (c) the proposed HB-ZVSCR inverter.

VI. Loss Analysis and Efficiency Evaluation

The power losses are found for two existing CMV clamping based topologies where only semiconductor device losses are considered. These losses are compared with the proposed HB-ZVSCR inverter topology. Fig. 6 illustrates the specific semiconductor losses for the three mentioned topologies, where the maximum losses occur through bidirectional switches that are utilized in both HB-ZVR and HB-ZVR-D topologies. Fig. 7 shows the efficiency curves of the mentioned three topologies through a range of output power up to 1 kVA. To find out

TABLE III
SUMMARY OF VOLTAGE CLAMPING BASED TRANSFORMERLESS INVERTER TOPOLOGIES

Topologies Name	Semiconductor Devices				I_{CM} (mA)	CMV	Filter		Reactive power capability	Efficiency (η)	
	IGBTs		Diodes				No. of Inductor	No. of Capacitor		η_{EU}	η_{CEC}
	No.	Voltage (V)	No.	Voltage (V)							
HB-ZVR	5	600	5	600	184	Varying	2	1	Yes	95.2%	96.4 %
HB-ZVR-D	5	600	6	600	22.67	Constant	2	1	Yes	95%	96.35 %
Proposed	6	600	4	600	18.7	Constant	2	1	Yes	96.3 %	97.1 %

the efficiency, the filter losses are also considered in the calculation. The maximum efficiency achieved for the proposed topology is equal to 97.10% when the California Energy Commission (CEC) efficiency formula is considered and 96.30% when the European (EU) weighted formula is considered. The formula to calculate the overall efficiency can be found in (9), and (10) for EU and CEC weighted efficiencies, respectively. Table III illustrates a summary of main features of relevant CMV clamping based transformerless inverter topologies.

$$\eta_{EU} = 0.03\times\eta_{5\%} + 0.06\times\eta_{10\%} + 0.13\times\eta_{20\%} + 0.10\times\eta_{30\%} + 0.48\times\eta_{50\%} + 0.20\times\eta_{100\%} \quad (9)$$

$$\eta_{CEC} = 0.04\times\eta_{10\%} + 0.05\times\eta_{20\%} + 0.12\times\eta_{30\%} + 0.21\times\eta_{50\%} + 0.53\times\eta_{75\%} + 0.05\times\eta_{100\%} \quad (10)$$

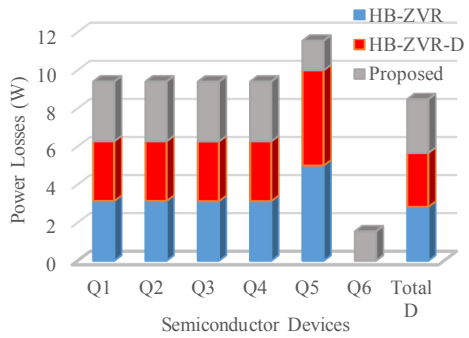

Fig. 6. Power losses for three mentioned inverter topologies.

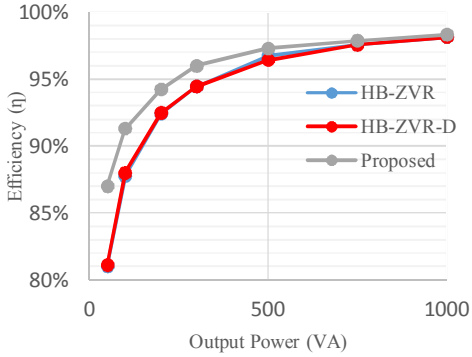

Fig. 7. Efficiency curves for three mentioned inverter topologies.

VII. Conclusion

This paper presents a new CMV clamping based transformerless inverter topology (HB-ZVSCR). The main features of the proposed topology are the constant CMV and the mitigated smooth CM leakage current with increased conversion efficiency. The idea of this topology is taken from HB-ZVR topology with bidirectional switches removed and two freewheeling path switches added. This paper shows that the HB-ZVSCR has the best performance regarding the CM behaviour, power losses and conversion efficiency compared to other similar CMV clamping based topologies.

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