A Classification of Single-Phase Transformerless Inverter Topologies for Photovoltaic Applications

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***Abstract*— In Photovoltaic (PV) applications, a transformer is often used to provide galvanic isolation and voltage ratio transformations. However, a transformer based inverter is bulky and has high conduction losses, therefore lead to a reduction in the inverter efficiency. To overcome this issue, the transformerless inverter topologies are addressed widely, but the main challenge of a transformerless inverter is common mode issue. Numerous topological modifications with their control and modulation techniques makes them difficult to follow, generalize and highlight the advantages and disadvantages. To address the issue, this paper gives an overview on transformerless inverter and classify them into subsection to discuss the merit and demerit of some of the major topologies. Five subsections based on common mode behavior, voltage clamping and decoupling techniques have been demonstrated (i.e., common ground, mid-point clamping, AC-decoupling, DC-decoupling and AC+DC decoupling). To verify the finding and for general consensus, major transformerless topologies are simulated using PLECS. A general summary is presented at the end to stimulate readers**

to acknowledge the problems and identify solutions..

Keywords*— *Single-phase photovoltaic (PV) systems, transformerless inverter, common mode voltage (CMV), leakage current.

I. INTRODUCTION

Nowadays, the use of renewable energy is escalated dramatically and PV solar panel is one of the favourite choices among clean energy sources for electricity production. One of the main factors that lead to this deep interest is due to the reduced cost of PV module production in the last decade. PV inverters that employ an isolation transformer are bulky and difficult to handle for maintenance purposes. Although, the system size can be reduced by employing a DC/DC converter with a high-frequency transformer, the overall efficiency is declined due to the leakage of high-frequency transformer. To overcome the limitations of using the transformer based inverter, non-isolated inverters have been introduced. In contrast, the most challenging facts related to these inverters are common mode voltage (CMV) and leakage current issues as well as the conversion efficiency [1]. Fig. 1 illustrates a general layout of the transformerless inverter PV system which shows the CM issue and leakage current flow path.

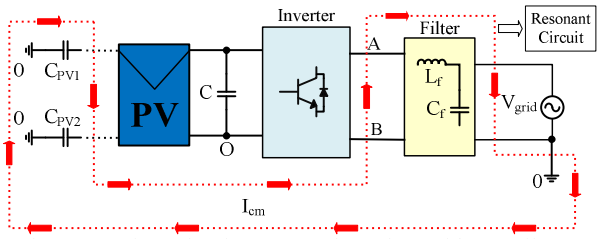


Fig. 1. Transformerless inverter topology along with CM effect.

Amplitude and frequency spectrum of the leakage current depend mainly on the converter circuit topology, modulation strategy and the resonant circuit formed between the ground capacitance, AC filter and grid. The power circuit can be replaced with phase voltages of the inverter V_{AO} and V_{BO}, which are equal to the potential of A and B points relative to the neutral point O, respectively [1-4]. The CMV and differential-mode voltage (DMV) can be written based on phase voltages as follows

$$V_{cm} = \frac{V_{AO} + V_{BO}}{2} \quad (1)$$

$$V_{DM} = V_{AO} - V_{BO} \quad (2)$$

Moreover, the phase voltages can be expressed based on V_{cm} and V_{DM} as mentioned in (3) and (4).

$$V_{AO} = V_{cm} + \frac{V_{DM}}{2} \quad (1)$$

$$V_{BO} = V_{cm} - \frac{V_{DM}}{2} \quad (2)$$

Without galvanic isolation, the potential between the PV array and the ground fluctuates, which charge and discharge the parasitic capacitor (C_{PV1} and C_{PV2}). This fluctuating CMV activates the resonant circuit as discussed above and may lead to a very high ground leakage current. However, the resonant frequency is not fixed, as it depends on the parasitic capacitance together with the DC lines that connect PV array to the inverter. It also depends on the size of the PV array and

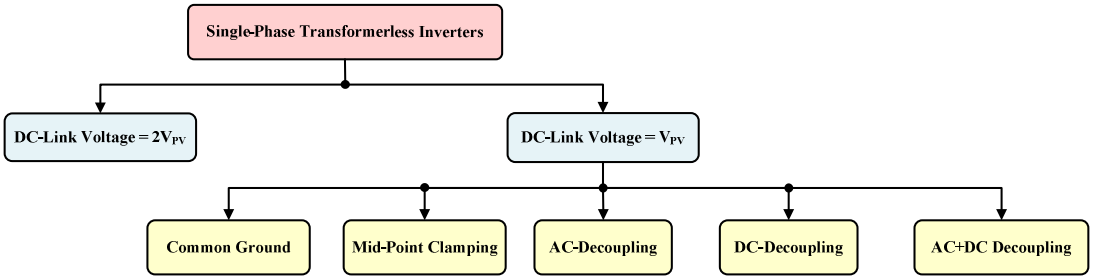


Fig. 2. Classification of single-phase transformerless inverter topologies used in PV systems.

environmental conditions. All these conditions make the elimination of leakage current more difficult [5].

This paper discusses the mentioned issues in various transformerless inverter topologies and provides a broad classification based on the implemented techniques for CM issue elimination. The paper is organized as follows: A broad classification of different single-phase transformerless inverter topologies is presented in Section II with a summary table of all reviewed topologies. The paper is summarized and concluded in Section III.

II. Classification of Single-Phase Tranformerless Inverter Topologies

Voltage source inverters (VSIs) are favorable for PV application due to low cost, high efficiency, and small size over current source inverters (CSIs). Numerous single-phase transformerless topologies for VSIs have been proposed and developed for grid-connected PV systems to improve the performance and compatibility to grid codes. Fig. 2 illustrates a broad classification of some important topologies in two major sub-groups based on the requirement for the DC-link voltage to achieve 230 V_{ac} with 50 Hz grid frequency, i.e. double DC-link voltage ($2\times V_{PV}$) and single DC-link voltage (V_{PV}) Moreover, the single input group can be categorized into five subgroups, based on I_{cm} suppression, decoupling and voltage clamping methods, i.e. common ground, mid-point clamping, AC-decoupling, DC-decoupling, and some AC+DC decoupling topologies.

To shed light on each topology considering the leakage current and CMV, in the following of this section some analysis and simulation results are provided for major topologies to illustrate their key waveforms and CMV behaviors. Table I shows the parameters and values used for the computer simulations performed throughput this section. Moreover, the simulations are carried out in PLECS software.

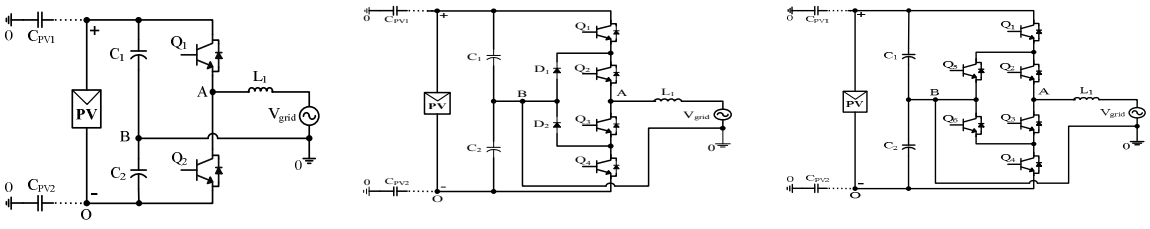
TABLE I
PARAMETERS USED FOR SIMULATIONS

Parameter	Value
Input Voltage (V_{PV})	400 V_{DC}
Output Load	50 Ω
Output Voltage (V_{grid})	230 V_{ac}
Line Frequency (f_g)	50 Hz
Output Current (Io)	4.61 A
Modulation Index (M)	0.82
Rated Power	1000 W
Switching Frequency (f_{sw})	18 kHz
DC Bus Capacitor ($C = 2\times C_1$) & ($C_1 = C_2$)	1.3 mF
Flying Capacitor (C_F)	470 µF
Flying Inductor (L_m)	0.3 mH
Filter Capacitor (C_o)	2.2 µF
Filter Inductor (L_1, L_2)	3 mH
Parasitic Capacitor (C_{pv1}, C_{pv2})	75 nF
Switches (IKW30N60DTP)	V_{CE} = 600 V, I_C = 30 A
Diodes (APT15D60B)	V_F = 600 V, I_F = 32A

A. Double Input ($2V_{PV}$) Single-Phase Transformerless Inverter Topologies

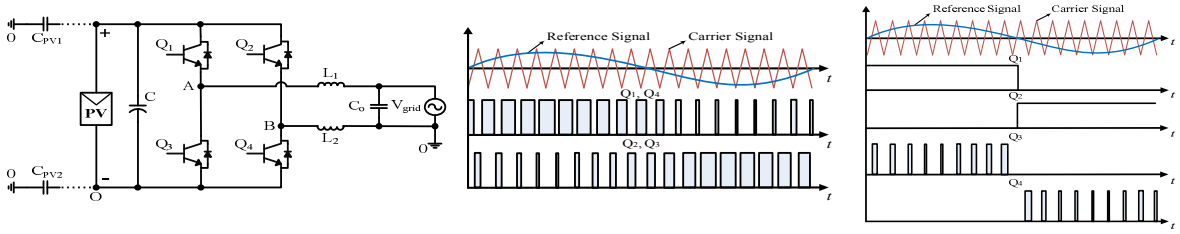
In this section, three single-inductor based transformerless inverters are introduced, where either L_1 = 0 or L_2 = 0 and the parasitic capacitance is 75 nF. The operational modes of each topology are discussed in details. A summary of those topologies is given in Table II.

Two-switch based half-bridge (H-B) inverter works with complementary switching pulses and the input voltage performs charging and discharging on the DC-link capacitors (C_1 and C_2) (see Fig. 3 (a)) [6]. In this circuit it is difficult to achieve the maximum power point of PV panel, and the output current ripple is high. To simplify the control system and improve the efficiency and current ripple, compared to two-switch based H-B, a new topology was introduced by A. Nabae, et al in 1981



(a) (b) (c)

Fig. 3. Circuit Diagram of (a) two-switch H-B inverter, (b) NP Clamped inverter, and (c) ANP clamped inverter.



(a) (b) (c)

Fig.4. Illustration of (a) F-B inverter, (b) its bipolar switching pulses, and (c) its unipolar switching pulses.

[7] called neutral point clamped (NPC), which is well known for minimizing the cost and size of the filter. This topology operates in three levels. The zero voltage stage can be achieved by the clamping technique through the clamp didoes of the midpoint that is shown by the schematic diagram (see Fig. 3 (b)). However, the main negative part of this topology is unbalanced conduction losses and restricted DC-link balance [8], which affects the performance of the whole inverter system. The active NPC (ANPC) is illustrated in Fig. 3 (c) which is an updated version of the conventional NPC topology [9], which mitigates the limitations of NPC topology.

B. Single-Input (V_{PV}) Single-Phase Transformerless Inverter Topologies

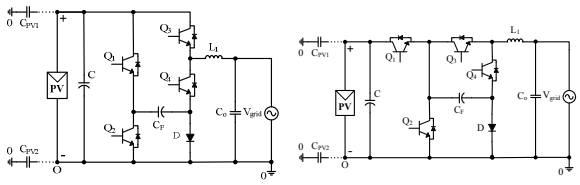
Full-bridge (F-B) single-phase transformerless inverter topologies with both bipolar and unipolar switching pattern [10] are explained in this section. Conventional F-B inverter with bipolar configuration has been used for achieving a constant CMV and a low I_{cm}. However, the loss increases much with the reduced system efficiency; such kind of topology has also been used in a commercially available device SoleraMax 4000 [11]. Hence, unipolar has been introduced for overcoming the limitations.

Fig.4 (a) illustrates the circuit configuration of F-B transformerless inverter topology with the parasitic capacitors on both sides of the PV panels. Bipolar switching pattern is used as shown in Fig. 4 (b). Switches Q_1 and Q_4 are turned ON for the positive half cycle, and the output current flows through the antiparallel diode of Q_2 and Q_4 to the load. On the other hand, Fig. 4 (c) shows the switching modulation of unipolar pattern. In this modulation scheme, Q_2 is complimentary to Q_1 and Q_3 complimentary to Q_4. For the positive half cycle, Q_1 and Q_4 are ON, and hence, the output voltage is equal to the input one. Zero voltage state for the positive half cycle, output current flows through Q_1 and antiparallel diode of Q_2 and for the negative half cycle, output currents flow through Q_3 and antiparallel diode of Q_4.

The topology where the negative polarity of the PV panel is directly connected with the grid is called common ground type topology. The significant advantage of such kind of topologies is the eliminated CM issue. Secondly, the F-B inverter can be extended through the semiconductor devices at either AC or DC side for clamping the voltage. Such kind of topologies are known as the midpoint clamping transformerless inverter topology. The main advantages of midpoint clamping techniques is reduced I_{cm} with low ripple than other topologies where the CMV remains constant. Further, of the other topologies are classified based on decoupling where AC-decoupling based transformerless inverter topologies is extended by adding switches and diodes at AC side. These kind of topologies are presented to achieve low total harmonic distortion (THD) on output voltage and current. Moreover, the I_{cm} reduces by balancing the system and making the CMV constant. Moreover, the extra switches and diodes on the DC side are added to introduce new topologies, which are known as DC-decoupling based transformerless inverter topologies. These topologies introduced to mitigate the I_{cm}through the balancing of the system. In the following some single-input based topologies are discussed.

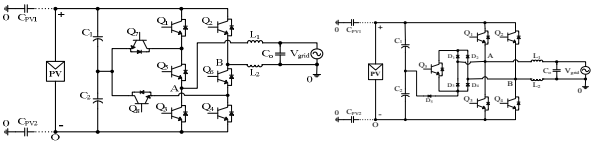
Flying capacitor based common ground transformerless inverters that have been presented in [12, 13] are displayed in Fig. 5 (a) and Fig. 5 (b), respectively. Both topologies operate with the same modulation pulses. In the presented concept, negative polarity of PV panel is directly connected to the grid to get zeroI_{cm}. For instance, the switch Q_1 and diode charge the flying capacitor, and the discharging path is through switches Q_2 and Q_4 which creates the negative polarity.

Positive negative neutral point clamping (PN-NPC) is proposed in [14], which is the combination of the positive neutral point clamping (P-NPC) and negative neutral point clamping (N-NPC) switching cells. The circuit



(a) (b)

Fig. 5. Illustration of (a) inverter in [12], and (b) inverter in [13].



(a) (b)

Fig. 6. Illustration of (a) PN-NPC, and (b) HB-AVR.

diagram of PN-NPC illustrated in Fig. 6 (a). In this topology, four switches are working in grid frequency (f_g) while of the other four are in switching frequency (f_{sw}). This topology is operated in four operational modes for each period of the utility grid. In the freewheeling period, four switches are ON so that inductor current flows through all of those switches that cause high conduction losses.

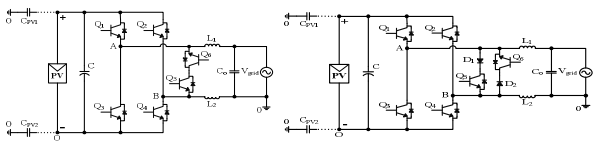
H-bridge zero voltage rectifier (HB-ZVR) (see Fig. 6 (b)) topology is presented in [15]. Four main switches are working like F-B inverter and short-circuited voltage is clamped to the midpoint of DC bus by four rectifier diodes and a bidirectional switch. In the positive half cycle, Q_1 and Q_4 are working to generate the active vector. Similarly, in the negative half cycle, Q_2 and Q_3 are ON and working to generate active vector. When Q_5 is ON, and other switches are OFF. Thus zero voltage states can be achieved.

Highly efficient and reliable inverter concept (HERIC) is well known in string inverters for achieving high efficiency, which is first invented in 2003 [16]. In addition, Sunways NT solar inverter has been manufactured in a German company used broadly in the industry. Moreover, they investigated 5 kW string inverters, with maximum conversion efficiency of 98% [17]. This topology benefits from a low current ripple and a high efficiency by employing Unipolar-SPWM switching. The load current is short-circuited through the switches Q_5 and Q_6 during the freewheeling period. On the other hand, CM issue is presented there as the PV module is decoupled from the grid and voltage is not clamped to the half of the supply voltage [18]. HERIC AC based topology is similar to HERIC topology where used two diodes with the switches Q_5 and Q_6 in series. These two diodes are used to flow the output current at the freewheeling time. The operational modes of these topologies are same as an F-B inverter; only the difference is in the output current flowing path through the extra used diodes and switches in the freewheeling period. The circuit diagrams of both topologies have been given in Fig. 7 (a) and Fig. 7 (b), respectively.

H5 topology is a high efficiency transformerless inverter topology that first has been proposed in [19]. This topology has been patented by one of the best PV inverter producers SMA solar technology. Its operational principles are almost like the F-B inverter. However, one switch is used on the DC side, which is called DC-decoupling switch. This switch is operated in switching frequency (f_{sw}). The upper switches are operated in grid frequency (f_g), and the below switches are operated in switching frequency (f_{sw}). The PV panel is disconnected from the grid side during zero voltage states when the switch Q_5 is OFF; as a result, the current freewheeling period has started that is an effective solution to reduce the I_{cm}. In the positive half cycle, switches Q_5 and Q_4 are turned ON at switching frequency (f_{sw}), and Q_1 at grid frequency (f_g) whereas other two switches are OFF. Contrariwise, Q_5 and Q_2 are turning ON at the switching frequency (f_{sw}) and Q_3 at grid frequency (f_g) whereas of the other two switches are OFF at negative half cycle. At the freewheeling period, the output current flows through Q_1 and the body diode of Q_3 for the positive period and Q_3 and the body diode of Q_1 for the negative period. The main disadvantage of this topology is high conduction losses through the three series associated switches in active phase. The circuit structure and switching modulation of H5 are shown in Fig. 8 (a).

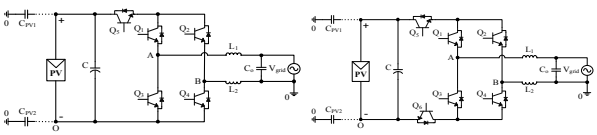
H6 DC side topology is displayed in Fig. 8 (b). This topology is introduced in [2] and is operated in four stages. Moreover, the author explained the presence of junction capacitor in the H6 DC side topology like in H5 topology [4] and the effect of the resonant circuit through the junction capacitor and its consequence leakage current issue. The switches Q_5, Q_1, and Q_6 are conducting in the positive half cycle while Q_3 and Q_2 are OFF. On the freewheeling period of positive and negative half cycle, the body diode of Q_3 is in forwarding bias with conducting switch Q_1, and the body diode of Q_4 is in forwarding bias with conducting switch Q_2 respectively. In this topology, extra low values capacitors were used to remove the CM effect, which is the reason of increased power losses.

H6 with diodes-1 is presented in [20], which is structured by MOSFET switches where four MOSFETs are working as an F-B inverter. Fig. 9 (a) shows the circuit structure of H6 with diodes-1. Simulation results of this topology show that I_{cm} for H6 with diodes-1 is around 200mA. To reduce the I_{cm} correctly, an accurate modulation technique is required. Hence, in [21] a topology that is replaced switch Q_5 and Q_6 by two IGBT is introduced. Moreover, a new modulation controller has



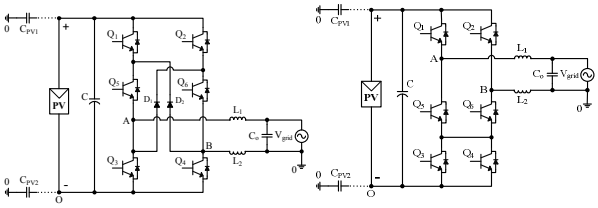
(a) (b)

Fig. 7. Illustration of (a) HERIC (b) HERIC ac based.



(a) (b)

Fig. 8. Illustration of (a) H5, and (b) H6 DC side.



(a) (b)

Fig. 9. Illustration of (a) H6 with diodes-1, and (b) H6-1.

TABLE II
SUMMARY OF FULL BRIDGE TRANSFORMERLESS INVERTERS.

Topology name	Semiconductor Devices				I_{cm} (mA)	CMV	Passive Filter Component		Output Voltage level
	IGBTs		Diodes				No. of Inductor (L)	No. of Capacitor (C)	
	No.	Voltage (V)	No.	Voltage (V)					
Two switches base	2	$1.5\times V_{pv}$	0	---	≤ 2	constant	1	0	2
NP Clamped	4	$1.5\times V_{pv}$	2	$1.5\times V_{pv}$	≤ 3.5	constant	1	0	3
ANP Clamped	6	$1.5\times V_{pv}$	0	---	≤ 2.5	constant	1	0	3
Bipolar F-B	4	$1.5\times V_{pv}$	0	---	≤ 55	199 to 201	2	1	2
Unipolar F-B	4	$1.5\times V_{pv}$	0	---	≤ 1800	200 to 400	2	1	3
S4	4	$1.5\times V_{pv}$	2	$1.5\times V_{pv}$	≈ 0	constant	1	1	3
Siwakoti-H	4	$1.5\times V_{pv}$	1	$1.5\times V_{pv}$	≈ 0	constant	1	1	3
Inverter topology in [12]	4	$1.5\times V_{pv}$	1	$1.5\times V_{pv}$	≈ 0	constant	1	1	3
Inverter topology in [13]	4	$1.5\times V_{pv}$	1	$1.5\times V_{pv}$	≈ 0	constant	1	1	3
Karschny	5	$1.5\times V_{pv}$	0	---	≈ 0	constant	1	1	3
iH5/oH5	6	$1.5\times V_{pv}$	0	---	≤ 20	199.89 to 200	2	1	3
H5-D	5	$1.5\times V_{pv}$	1	$1.5\times V_{pv}$	≤ 200	150 to 249	2	1	3
HERIC Active 1	7	$1.5\times V_{pv}$	2	$1.5\times V_{pv}$	≤ 25	199.93 to 200	2	1	3
HERIC Active 2	6	$1.5\times V_{pv}$	4	$1.5\times V_{pv}$	≤ 25	199.91 to 200	2	1	3
PN-NPC	8	$1.5\times V_{pv}$	0	---	≤ 35	199.3 to 201.1	2	1	3
HB-ZVR	5	$1.5\times V_{pv}$	5	$1.5\times V_{pv}$	≤ 200	163 to 200	2	1	3
HB-ZVR-D	5	$1.5\times V_{pv}$	6	$1.5\times V_{pv}$	≤ 40	199.89 to 200	2	1	3
HERIC	6	$1.5\times V_{pv}$	0	---	≤ 200	165 to 235	2	1	3
HERIC AC based	6	$1.5\times V_{pv}$	2	$1.5\times V_{pv}$	≤ 200	165 to 236	2	1	3
H5	5	$1.5\times V_{pv}$	0	---	≤ 200	159 to 235	2	1	3
H6 DC side	6	$1.5\times V_{pv}$	0	---	≤ 200	151 to 249	2	1	3
H6 DC side improved-1	6	$1.5\times V_{pv}$	0	---	≤ 1000	200 to 400	2	1	3
H6 DC side improved-2	6	$1.5\times V_{pv}$	0	---	≤ 1000	200 to 400	2	1	3
H6 in mid switch	6	$1.5\times V_{pv}$	0	---	≤ 200	159 to 240	2	1	3
H6 with diodes-1	6	$1.5\times V_{pv}$	2	$1.5\times V_{pv}$	≤ 200	150 to 249	2	1	3
H6 -1	6	$1.5\times V_{pv}$	0	---	≤ 200	151 to 258	2	1	3
H6 in mid switch	6	$1.5\times V_{pv}$	0	---	≤ 200	159 to 240	2	1	3
Hybrid bridge	6	$1.5\times V_{pv}$	2	$1.5\times V_{pv}$	≤ 250	158 to 241	2	1	3

been used based on reactive power injection space vector pulse width modulation (SVPWM) technique and proportion-integration-resonance (PIR) current controller. The main demerits of this topology are low reverse recovery issues through the switches, and high conduction losses as in the active mode due to the output current flows through three switches.

H6-1 topology is proposed in [22], and the idea is taken from the topology in [20]. Those papers presented the topologies with six switches and two diodes. However, the presenter removes the extra cross connected diodes and replace the MOSFET switches to IGBT that is demonstrated in Fig. 9 (b). It provides reactive power flow capability that was not available by MOSFET based topologies. In the positive half cycle, $Q_1, Q_6,$ and Q_4 are ON, and current flows through the inductors and complete the cycle. Moreover, zero voltage state switch Q_6 and the antiparallel connected body diode of switch Q_5 are conducted which is not connected with the input and current flows through the load. On the other hand, rest of three switches $Q_2, Q_5,$ and Q_3 are conducted in the negative half cycle. In the negative half cycle zero voltage state occurs, in which current flows in between switch Q_5 and the antiparallel connected body diode of switch Q_6. An overall summary of the reviewed single and double-input based inverter topologies are shown in Table II.

III. CONCLUSION

Single-Phase transformerless PV inverter has gained widespread attention due to the low cost/weight and high efficiency compared to single-phase inverters with galvanic isolation. In this paper, various single-phase transformerless inverter topologies are reviewed systematically and segregated based on common mode behavior, common ground, voltage clamping and decoupling techniques have been demonstrated (i.e., common ground, mid-point clamping, AC-decoupling, DC-decoupling and AC+DC decoupling). Main principles of operation and modulation pattern are presented and compared in table format for each category. To verify the finding and for general consensus, major transformerless topologies are simulated using

TABLE III
QUALITATIVE SUMMARY OF THE MAJOR SINGLE-PHASE TRANSFORMERLESS INVERTER TOPOLOGIES.

Transformerless Inverter Topologies	Advantages	Disadvantages	Reactive Power Capability	Efficiency
Common Ground	▪ No CM effect. ▪ Less semiconductor devices are used. ▪ Small filter required.	▪ Flying capacitor or switched capacitor or flying inductor controlling is difficult.	Yes	Very high
Mid-Point Clampling	▪ Constant CMV and low I_{cm}.	▪ Increased complexity. ▪ More semiconductor devices.	Yes	Medium
AC-Decoupling	▪ Low Conduction losses. ▪ Output current is not flowing through the antiparallel diodes of F-B. ▪ Lower THD.	▪ Additional switches required. ▪ Residual line frequency leakage current.	Yes	High
DC-Decoupling	▪ DC bypass switch helps to disconnect PV from grid during leakage current.	▪ High conduction losses. ▪ Additional devices required. ▪ Unbalanced switching.	Yes	Medium
AC+DC Decoupling	▪ Low output current ripple.	▪ Complex control ▪ More semiconductor devices. ▪ CMV is fluctuated.	Yes (except H6 with diodes-1 and H6 with diodes-2)	Medium

PLECS. As a summary to this review, Table III provides a comparative study of main single-phase transformerless inverter categories concerning their major characteristics.

REFERENCES

[1] A. Kadam and A. Shukla, "A multilevel transformerless inverter employing ground connection between pv negative terminal and grid neutral point," *IEEE Trans. Ind. Electron.,* vol. 64, no. 11, pp. 8897-8907, 2017.

[2] B. Yang, W. Li, Y. Gu, W. Cui, and X. He, "Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system," IEEE Trans. Power Electron., vol. 27, no. 2, pp. 752-762, 2012.

[3] T. K. S. Freddy and N. A. Rahim, "Photovoltaic inverter topologies for grid integration applications," *in Advances in Solar Photovoltaic Power Plants: Springer,* 2016, pp. 13-42.

[4] K. S. Tey and S. Mekhilef, "A reduced leakage current transformerless photovoltaic inverter," *Renew. Energy,* vol. 86, pp. 1103-1112, 2016.

[5] Y. Tang, W. Yao, P. C. Loh, and F. Blaabjerg, "Highly reliable transformerless photovoltaic inverters with leakage current and pulsating power elimination," *IEEE Trans. Ind. Electron.,* vol. 63, no. 2, pp. 1016-1026, 2016.

[6] S. L. Kuo, "Half-bridge transistor inverter for DC power conversion," *IEEE Trans. Ind. Electron. Control Instrum.,* no. 4, pp. 249-253, 1974.

[7] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.,* no. 5, pp. 518-523, 1981.

[8] M. Schweizer, T. Friedli, and J. W. Kolar, "Comparative evaluation of advanced three-phase three-level inverter/converter topologies against two-level systems," *IEEE Trans. Ind. Electron.,* vol. 60, no. 12, pp. 5515-5527, 2013.

[9] X. Yuan, H. Stemmler, and I. Barbi, "Investigation on the clamping voltage self-balancing of the three-level capacitor clamping inverter," *IEEE 30th Annual IEEE Power Electron. Specialists Conf. (PESC),* Charleston, SC, Aug.2002, pp. 1059-1064.

[10] N. Mohon, T. M. Undeland and W. P. Robbins, Power Electronics:Converters, Applications and Design, vol. 2nd ed. New York: *Wiley,* 1995.

[11] B. Burger, "Power electronics for grid connected photovoltaic," *in Proc.Otti Workshop,* pp. 163-216, Jun. 2008.

[12] Y. P. Siwakoti and F. Blaabjerg, "Common-Ground-Type Transformerless Inverters for Single-Phase Solar Photovoltaic Systems," *IEEE Trans. Ind. Electron.,* vol. 65, no. 3, pp. 2100-2111, 2018.

[13] Y. P. Siwakoti and F. Blaabjerg, "A novel flying capacitor transformerless inverter for single-phase grid connected solar photovoltaic system," *7th IEEE Int. Symposium on Power Electronics for Distributed Generation Systems (PEDG),* Vancouver, BC, Aug. 2016 pp. 1-6.

[14] L. Zhang, K. Sun, L. Feng, H. Wu, and Y. Xing, "A family of neutral point clamped full-bridge topologies for transformerless photovoltaic grid-tied inverters," *IEEE Trans. Power Electron.,* vol. 28, no. 2, pp. 730-739, 2013.

[15] T. Kerekes, "Analysis and modeling of transformerless photovoltaic inverter systems," *Doctor of Philosophy*, Institute of Energy Technology, Aalborg University, 2009.

[16] H. Schmidt, S. Christoph, and J. Ketterer, "Current inverter for direct/alternating currents, has direct and alternating connections with an intermediate power store, a bridge circuit, rectifier diodes and a inductive choke," *German Patent DE10,* vol. 221, no. 592, p. A1, 2003.

[17] S. S. Inverters, *http://www.solaraustralia.com.au/sunways_inverter_nt2500_500_series.html,* 2013.

[18] T. Kerekes, R. Teodorescu, P. Rodríguez, G. Vázquez, and E. Aldabas, "A new high-efficiency single-phase transformerless PV inverter topology," *IEEE Trans. Ind. Electron.,* vol. 58, no. 1, pp. 184-191, 2011.

[19] M. Victor, F. Greizer, S. Bremicker, and U. Hübler, "Method of converting a direct current voltage from a source of direct current voltage, more specifically from a photovoltaic source of direct current voltage, into a alternating current voltage," ed: *Google Patents,* 2008.

[20] B. Ji, J. Wang, and J. Zhao, "High-efficiency single-phase transformerless PV H6 inverter with hybrid modulation method," *IEEE Trans. Ind. Electron.,* vol. 60, no. 5, pp. 2104-2115, 2013.

[21] B. Liu, M. Su, J. Yang, D. Song, D. He, and S. Song, "Combined reactive power injection modulation and grid current distortion improvement approach for h6 transformer-less photovoltaic inverter," *IEEE Trans. Energy Conv.,* vol. 32, no. 4, pp. 1456-1467, 2017.

[22] M. Islam and S. Mekhilef, "H6-type transformerless single-phase inverter for grid-tied photovoltaic system," *IET Power Electron.,* vol. 8, no. 4, pp. 636-644, 2015