Electrical challenges of heteroepitaxial 3C-SiC on silicon

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Abstract. We have investigated the electrical conduction in epitaxial cubic silicon carbide films on low-doped and high-resistive silicon substrates. The electrical properties of the film/substrate system such as the carrier concentration, carrier mobility, and sheet resistance were evaluated by performing Hall measurements in a van der Pauw configuration at room temperature. For the SiC on low-doped p-Si, we found that the charge carriers in the substrate always dominate the electrical conduction indicating an electrical shorting of the film to the substrate and the absence of a p/n junction. Meanwhile, for the SiC films grown on high-resistive silicon, we found an evidence of current leakage through a silicon region right below the SiC/Si interface, generated upon SiC growth. Leakage resistances in the kΩ range obtained from TLM structures made of isolated SiC pillars on high-resistive silicon confirmed the presence of a conductive region below the SiC/Si interface. This work also shows that this electrical leakage can be supressed using a high-resistive silicon as the substrate and etching away the conductive region below the interface.

Introduction

Epitaxial cubic silicon carbide films on silicon have attracted extensive interest for semiconductor device applications such as high-voltage, high-frequency diodes, and heterojunction bipolar transistor [1]. This is because they can offer access to the properties of the SiC material such as its wide band gap and high thermal conductivity on the more conventional silicon substrates [2]. Rahimi et al. have shown, however, that the substantial tensile strain generated from the lattice and thermal expansion coefficient mismatch between 3C-SiC and silicon, may reduce the band gap in the SiC epitaxial films [3]. Nevertheless, the impact of this phenomenon on the electrical and electronic performance of the epitaxial SiC films on silicon has not been fully elucidated to date; such information is vital to obtain the optimal performance of devices fabricated from these strained heterojunctions.

We have recently shown that the expected p-n junction between a *p*-type silicon substrate and cubic heteroepitaxial silicon carbide (3C-SiC, naturally grown as unintentionally *n*-type) is either non-existing or very unstable so that severe leakage or shorting of the epitaxial silicon carbide to the underlying silicon substrate is typically found [4, 5]. In this work, we aim to understand and model the electrical conduction in the 3C-SiC(100)/Si(100) system and the substrate influence on the conduction using commercial NOVASiC samples that were grown at temperatures between 1300 and 1400°C [6]. Consequently, we compare the epilayers grown on low-doped *p*-type substrate to those grown on highly resistive substrates, which are typically *n*-type.

Experimental

We focused on unintentionally doped (thus *n*-type) commercial NOVASiC 3C-SiC(100) films with thickness of 500 nm epitaxially grown at 1300-1400°C [6] on 527 µm low-doped *p*-type Si(100) with resistivity ranging from 1 to 10Ωcm as well as on high-resistive Si(100) substrates with resistivity greater than 10kΩcm. For the electrical characterization, we diced the SiC/Si wafers into 1.1x1.1 cm^2 coupons, and sputtered 150 nm thick nickel contacts (no annealing) onto the four corners using a custom made shadow mask, see Fig. 1a and 1b. The electrical properties such as the carrier concentration, carrier mobility, and sheet resistance were estimated at room temperature by

performing van der Pauw Hall measurements on the SiC/Si samples as well as on representative bare Si substrates using Ecopia HMS 5300 Hall Effect Measurement System. SiC/high-resistive Si van der Pauw structures were etched in an inductively coupled plasma (ICP) system using SF_6 gas and oxygen to remove the SiC layer using the Ni contacts as a hard mask (see Fig. 1c) and the Hall measurements were repeated at room temperature. Additionally, SiC on high-resistive Si samples were patterned into transfer length measurement (TLM) structures consisting of 300 nm thick, 500 µm wide aluminium contacts deposited using e-beam evaporation (no annealing) followed by acid etching of aluminium and reactive-ion etching of SiC, see Fig. 2. Current-voltage measurements were performed at room temperature to measure the leakage resistances using a HP4145B semiconductor parameter analyser. Afterwards, the silicon in-between the SiC pillars on the SiC/high-resistive Si van der Pauw and TLM structures were etched using ICP, and all measurements were repeated, see Fig. 4a and 4b.

Results

Table 1. Hall measured transport characteristics at room temperature. Results are the averaged values extracted from three samples for each type.

	Bare *p*-Si	**3C-SiC/*p*-Si**	**Bare high-resistive Si**	**3C-SiC/high-resistive Si**	**Removed 3C-SiC/high-resistive Si**
Carrier type	Holes	Holes	Electrons	Electrons	Electrons
Carrier concentration (cm^{-2})	$1(\pm0.2)x10^{14}$	$1(\pm0.2)x10^{14}$	$1(\pm0.2)x10^{10}$	$3(\pm0.2)x10^{11}$	$4(\pm0.2)x10^{11}$
Mobility (cm^2/Vs)	341(±10)	357(±10)	1220(±10)	1677(±10)	1650(±10)
Sheet resistance (Ω/□)	173±10	166±10	500k±3k	12k±3k	12k±3k

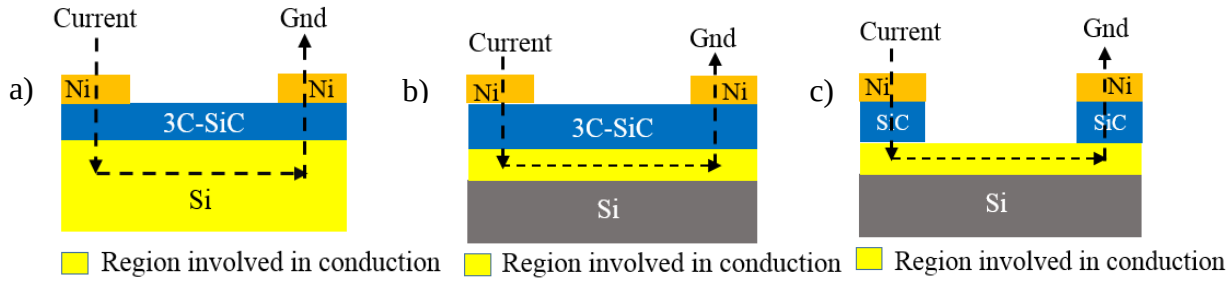

Fig. 1. Schematic of conduction path in the 3C-SiC grown at 1300-1400°C a) on low-doped *p*-Si substrate; b) on high-resistive Si; c) after etching SiC layer between the contacts of SiC/high-resistive Si -the conduction is found to occur within a region of a few micrometres thick below the interface.

From Table 1, the room temperature hall measurement of 3C-SiC grown on a low-doped Si indicates a hole conduction with carrier concentration, mobility and sheet resistance comparable to the bare low-doped *p*-Si substrate. This implies that the SiC films on low-doped Si substrates are typically shorted (either upon growth or during subsequent annealing) and the charge carriers in the thick silicon substrate with relatively high mobility dominate the electrical conduction, as shown in Fig. 1a. The electrical shorting persists even if we etch deep into the substrate, as long as the silicon charge carriers exists [5].

The effects of large tensile strain generated from the lattice mismatch as well as the difference in thermal expansion coefficients between the 3C-SiC film and the thick Si substrate leads to high defect densities [2] as well as changes in the band alignment and band structure at the 3C–SiC/Si heterojunction [3]. The band distortion may make the band gap of SiC more compatible with silicon. We thus hypothesize that the leakage or the shorting phenomenon of the 3C-SiC to the Si substrate is linked to a combination of increased hole current injection from Si to SiC due to a smaller valence band barrier, and the presence of electrically active defects at the SiC/Si interface.

Meanwhile, for the SiC films grown on high-resistive Si, we believe that, in addition to the *n*-type conduction within the SiC film which is relatively limited (only about ~10^{11} cm^{-2} sheet carrier concentration), we also find evidence of conduction through a region just below the SiC/Si interface as shown in Fig. 1b and 1c. To corroborate, the leakage resistances are measured for the SiC/high-resistive Si using TLM structures in Fig. 2, see Table 2.

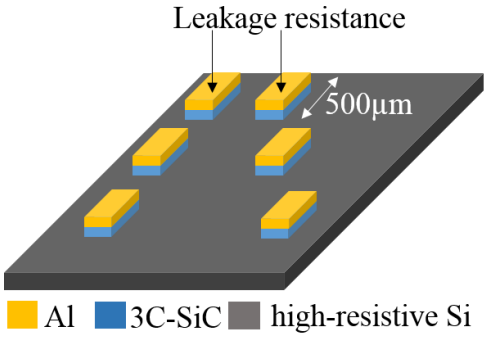

Fig. 2. TLM structures on the 3C-SiC/high-resistive Si for leakage resistance measurement.

Table 2. Leakage resistances across different contact spacing for the SiC TLM structures made on high-resistive Si. Results are the averaged values obtained from two samples.

Contact spacing (µm)	**Leakage resistance (kΩ)**
40	75
60	80
80	85
100	87
160	90
200	95
250	100
300	105

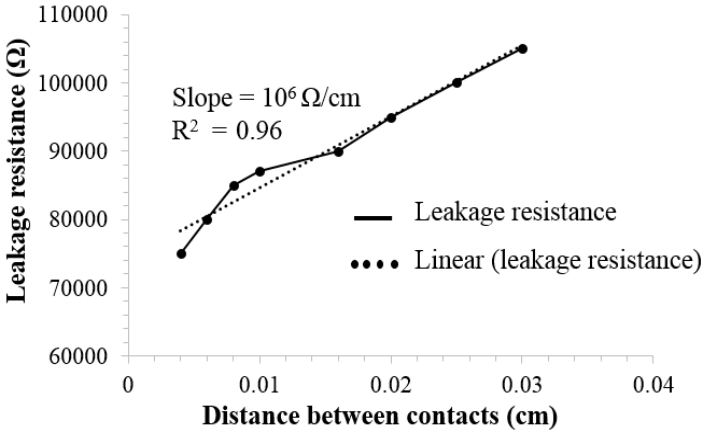

Fig. 3. Fitted TLM leakage resistances versus contact spacing for the SiC on high-resistive Si.

The data in Table 2 indicate that for SiC on high-resistive Si, the leakage resistances are larger than that for SiC on low-doped Si [5]. Fig. 3 shows the fitted leakage resistances obtained using TLM structures on the SiC/high-resistive Si as a function of different contact spacing with a slope of 10^6 Ω/cm. The sheet resistance calculated from slope and width of the contact is ~50kΩ/□ –slightly larger than the sheet resistance of SiC/high-resistive Si obtained using the van der Pauw Hall measurement in Table 1. Note that the actual leakage resistances must be at least one order of magnitude larger than the measured leakage resistance values, for the TLM sheet resistance to agree with the van der Pauw sheet resistance of the bare high-resistive Si substrate (500kΩ/□), to indicate no leakage.

When using a high-resistive *n*-type silicon substrate, we have a large sheet resistance of 500kΩ/□ with limited carriers and thus no p-n junction at the SiC/Si interface. Therefore, any band distortion induced by the interfacial strain in the SiC film may not lead to carrier injection as in the case of low-doped *p*-Si substrates. Indeed, transport measurements of the SiC on high-resistive Si indicate *n*-type majority carriers, which are the carrier type expected in heteroepitaxial 3C-SiC films [4]. However, we also notice in Table 1 that even after total removal of the SiC layer, those carriers persist. We explain this by suggesting that a highly defective region is formed below the interface upon the SiC growth, where the carriers of the SiC film are concentrated.

We can suppress the in-plane electrical leakage of 3C-SiC/high-resistive Si by etching the conductive region for at least 20µm deep as demonstrated in Fig. 4. After etching the silicon in between the SiC

pillars for more than 20µm deep until the conductive region in the substrate is eliminated, we isolate the SiC pillars on the van der Pauw and TLM structures (see Table 3 for Hall measurement and TLM leakage resistance results before and after the silicon etching).

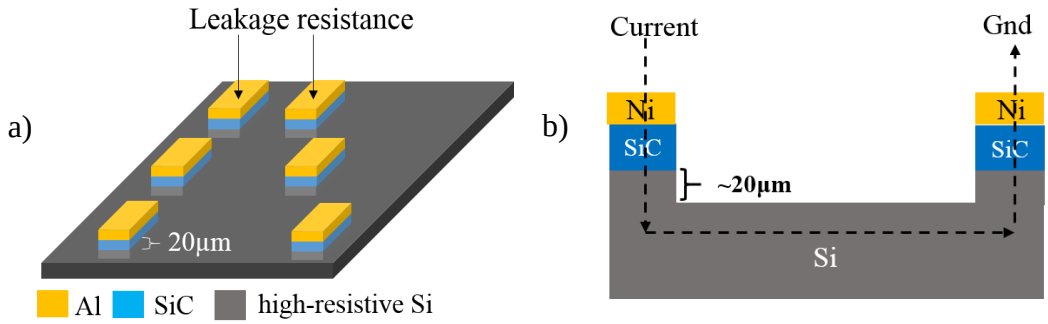

Fig. 4. a) SiC/high-resistive Si TLM structure after ~20 µm deep etching of Si; b) electrical conduction in SiC/high-resistive Si after ~20 µm deep etching of Si

Table 3. Electrical characteristics at room temperature for SiC/high-resistive Si before and after ~20 µm deep etching of silicon between SiC pillars a) van der Pauw Hall measurement results b) TLM leakage resistance results. Results after etching are the averaged values of two samples each.

a)

	3C-SiC/high-resistive Si (before etching)	**3C-SiC/high-resistive Si (after 20µm etch)**
Carrier type	Electrons	Electrons
Sheet carrier concentration (cm^{-2})	$3(\pm0.2)x10^{11}$	$5(\pm0.2)x10^{11}$
Mobility (cm^2/Vs)	1677(±10)	34(±10)
Sheet resistance (Ω/□)	12k±3k	492k±2k

b)

Contact spacing	**TLM leakage resistance**	
(µm)	**before etch (kΩ)**	**after 20µ etch (MΩ)**
40	75	8.5
60	80	8.5
80	85	9.5
100	87	10
160	90	-
200	95	10

Summary

Heteroepitaxial 3C-SiC films grown on low-doped Si are typically electrically shorted to the substrate. This could be due to the presence of a range of electrically active extended defects at the SiC/Si interface, together with an increased hole current injection from the Si to the SiC generated by the intrinsic strain relaxation in the SiC film. Room temperature van der Pauw and TLM measurement results have shown that this electrical leakage/shorting of the SiC to the Si substrate can be overcome by using a high-resistive silicon as the substrate and etching away more than 20 µm deep into the silicon between the SiC pillars.

References

[1] S. Nishino et al., J. Electrochem. Soc. 127(12) (1980) 2674-2680.
[2] X. Song et al., Appl. Phys. Lett. 96(14) (2010) 142104-142104-3.
[3] R. Rahimi et al., J. Phys. D: Appl. Phys. 42(5) (2009) 055108.
[4] A. Pradeepkumar et al., Appl. Phys. Lett. 109 (2016) 011604-011604-5.
[5] A. Pradeepkumar et al., Appl. Phys. Lett. 109 (2016) 196102-196102-2.
[6] M. Zielinski et al., Mater. Sci. Eng. B 165(1) (2009) 9-14.