Multi-tone Excitation Analysis in RF Energy Harvesters - Considerations and Limitations

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Abstract— **The effect of multi-tone excitation on the DC response of a voltage-doubler RF (radio frequency) energy harvester is analysed. Theoretical analysis as well as frequency and time domain simulations were conducted to clarify the findings. Measurements were also carried out to validate the results. The measured, simulations and theoretical results are in good agreement. This paper focuses on evaluating the performance of a voltage doubler rectifier under multi-tone excitation (input power is the same in the single-tone and multi-tone case). Based on time domain and harmonic balance simulations, theoretical and measurement analyses, it is evident that the application of multiple tones simultaneously within the matched frequency band and with the same average available power results in a lower average output DC power when compared with the single-tone case with the same input power. This trend is evident over a broad low input power range of −50 to −10 dBm (0.01-100 µW).**

Index Terms— **Energy harvesting, Multi-tone excitation, Time domain analysis, Voltage doubler rectifier, Wireless power transmission.**

I. INTRODUCTION

The development of wireless power transmission (WPT) technologies [1], [2] that allow sensors [3], [4], mobile devices [5], implantable interfaces [6], [7] and RFID (Radio-frequency identification) [8] systems to operate without batteries, has inspired research interest to develop energy harvesting systems and techniques [1], [9], [10], [11], [12]. Although WPT is a promising solution to provide a viable energy source for Internet of Things (IoT) devices [13], efficient WPT is a challenging issue as it deals with the limited received power (due to the transmission regulation and the path

loss in the far-field WPT). To address this, considerable research has been conducted on the circuit design at the receiver side of wireless power transmission systems to enhance the RF-DC power conversion efficiency (PCE) [1], [14]. However, less work has been dedicated to the signal design at the transmitting terminal to improve the wireless power transfer efficiency (WPTE) [15]-[17].

From a signal design perspective, instead of using the conventional single-tone continuous wave (CW), two-tone CW signals, chaotic waveforms, pulse signals, analogue and digital modulated signals, FSK signals, white noise, and OFDM have been proposed to excite the rectification device (e.g. diode) more efficiently and enhance the WPTE [18]-[40]. In [19]-[21], the rectifier performance with analogue modulated signals (i.e., AM and FM) and digitally modulated signals have been investigated. Pulse signals were also evaluated to improve the PCE and achieve desired performance by introducing the optimum duty cycle and waveforms [22]-[25].

In [26]-[30], the energy transfer efficiency was increased, and the reading range of RFID tags was extended by using high peak-to-average power ratio (PAPR) signals. The effect of using high PAPR signals on the PCE has also been compared to a single carrier constant envelope signal [31]. It was verified that using high PAPR signals such as OFDM, white noise, and chaotic signals lead to rectifier efficiency improvement. It has also been proven that a 20% improvement in the rectifier efficiency can be achieved by using chaotic waveforms instead of using a single tone signal [32]. This was due to the fact that a chaotic waveform [33] (with a high PAPR) could overcome the Schottky Barrier Diode (SBD) threshold voltage at lower average input RF power levels when compared to a single-tone signal excitation. Furthermore, it has been demonstrated theoretically and experimentally that by applying a multi-tone signal with a constant input power level (the same total power level as the single tone) to the single-diode rectifier circuit, an increased output power over the single-tone excitation was obtained [34], [35]. This is again due to the higher PAPR of the multi-tone signal. The effect of multi-tone bandwidth and tone separation on the power conversion efficiency has also been evaluated in [36]. The achieved results indicated that the tag could be activated with less power using multi-tone signals

(with high PAPR) than CW (at the same distance).

On the flip side, using high PAPR signals may cause distortion and clipping in traditional power amplifier architectures. These nonlinear adverse effects will destroy the time-domain shape of the signal as well as the energy efficiency [37]. The proposed method in [37] overcame the problem of amplifying large peak-to-average power ratio (PAPR) signals by using spatial power combining. In this technique, individual tones were amplified and radiated, while spatial power combining achieves the multi-tone signal in free space.

From a circuit design point of view, single-diode rectifier topologies have been widely used to analyse the effect of modulated signals and multi-sine excitation on the power conversion efficiency (PCE) [35], [38], [39], [40].

The pros and cons of applying single tone and multi-tone excitations on a specific single-diode rectifier's performance have been examined [38]. The design of a series diode rectifier when driven by signals with a time-varying envelope (e.g. multi-tone or digitally modulated signals) was also proposed [39], and the dependency of the PCE on the rectifier load was investigated. It was demonstrated that for specific load values a signal with a time-varying envelope can result in a higher efficiency value than a continuous wave (CW) signal. However, an analytical model was only proposed for CW excitation and also an ideal diode model was considered. Furthermore, a theoretical model for the energy-conversion efficiency of single-diode rectifiers under high PAPR waveform excitation is provided in [40]. Analyses have been performed over a high input power range of −20 to 30 dBm to simplify the model. However, in a real wireless power transmission (WPT) scenario, due to the transmission regulation and the path loss, the input power level is usually very low (under −10 dBm). Moreover, simulated results were computed using ideal components (e.g. ideal transmission lines) and package parasitics were not considered.

The voltage-doubler rectifier topology has also been used to analyse the effect of modulated signals and multi-sine excitation on the PCE [41], [43]. In [41], the performance of a voltage doubler rectifier using Schottky diode HSMS-2850 was analysed with QPSK and 16QAM input signals over a high power range of 0 to 10 dBm at 1.62 GHz. It was demonstrated that using modulated signals instead of CW signals degrades the PCE of the rectifier. However, it should be noted that the HSMS-285x family of Schottky-barrier detector diodes has been developed specifically for high volume designs in small signal applications at frequencies below 1.5 GHz [42]. Hence, the breakdown voltage effect or moving out of the square-law region might have caused the PCE degradation over the high input power range (0 to 10 dBm). Moreover, the impact of the modulation scheme and input power on a voltage-doubler rectifier performance was analysed over the input power range of −10 to 10 dBm [43], which is again high input power for a sensitive Schottky diode HSMS-2860 [44]. It was shown that by using QPSK and 16QAM modulated input signals, the efficiency revealed different characteristics depending on the input power. However, details of the circuit design and matching network were not provided to clarify the findings.

The majority of published papers as mentioned earlier have focused on the impact of the PAPR on single-diode rectifiers. Moreover, a few studies have examined the effect of modulated signals and multi-sine excitation on the PCE of a voltage-doubler rectifier topology [41], [43]. However, details of the circuit design and more importantly in-depth theoretical analysis have not been provided to validate the findings.

This study, for the first time, elucidates a comprehensive theoretical analysis, time domain (TD) and harmonic balance (HB) simulations, and measurement validations of the voltage doubler performance under single-tone and multi-tone excitations. This paper investigates the effect of multi-tone excitation on the output DC power of a voltage-doubler FM-band RF energy harvester over a broad range of low input power. The achieved results demonstrate that despite previously published papers (e.g. [32], [34], [35], [36], and [38]) multi-tone excitation may not increase the output DC power (even at ultra-low input power levels) and depends highly on the circuit topology. Hence, the concept of increasing the DC output power by using multi-tone excitation is not true for every system, and in contrast, it is shown here that it degrades the output DC power (even with high peak-to-average power ratio). To the authors' knowledge, this concept has not been reported previously.

The FM rectifier circuit is well matched within 89-111 MHz over a broad low input power range of −50 to −10 dBm (0.01-100 µW) [45], [46]. In order to determine the true efficiency of the rectifier for the cases of multi-tone excitation and also to facilitate the comparison between single tone and multiple tones, the input power is the same in the single-tone and multi-tone case (regardless of the number of excitation tones). The effect of applying multi tones over a broad low input power range were investigated by conducting frequency and time domain analyses and measurements. Theoretical analyses are also carried out to investigate the reason for obtaining a lower amount of DC output with the multi-tone excitation. It is worth mentioning that, the present work investigates the effect of multi-tone excitation with the same average input power for the WPT scenario, using a similar rectifier as was used in [45]. However, [45] has focused on multi-tone excitation with different average input power levels for the ambient energy scavenging scenario; for example, one tone of −10 dBm or two tones of −10 dBm (a total input power of −7 dBm delivered to the rectifier circuit) were applied to the rectifier. Hence, the average input power is not the same as [45].

The remainder of this paper is organised as follows. First, a voltage-doubler rectifier design is described followed by a theoretical time domain analysis. Subsequently, the measurement and simulation results for the multi-tone excitation are presented which validate the theoretical investigations. Finally, the Conclusion section summarises the achieved key findings and demonstrates their potential implications.

II. THEORETICAL ANALYSIS OF A VOLTAGE DOUBLER

The voltage doubler topology has been widely adopted to enhance the sensitivity and efficiency of the rectifier circuit [1],

[45], [46] however, unique characteristics of this circuit have not been fully discovered. This study, for the first time, provides comprehensive theoretical and simulation-based analyses of the voltage doubler performance in the time domain (TD) and frequency domain under single-tone and multi-tone excitations.

A. Broadband Voltage Doubler Rectifier Design

Recently we proposed an efficient rectenna (rectifying antenna) for ambient RF energy harvesting [45], [46]. Based on our previous RF field measurement outcomes [47] the highly sensitive RF scavenger operates over a broad low input power range of −50 to −10 dBm (0.01 to 100 µW) in order to determine the usefulness of low-power rectification in the FM frequency band (89-111 MHz).

(a)

(b)

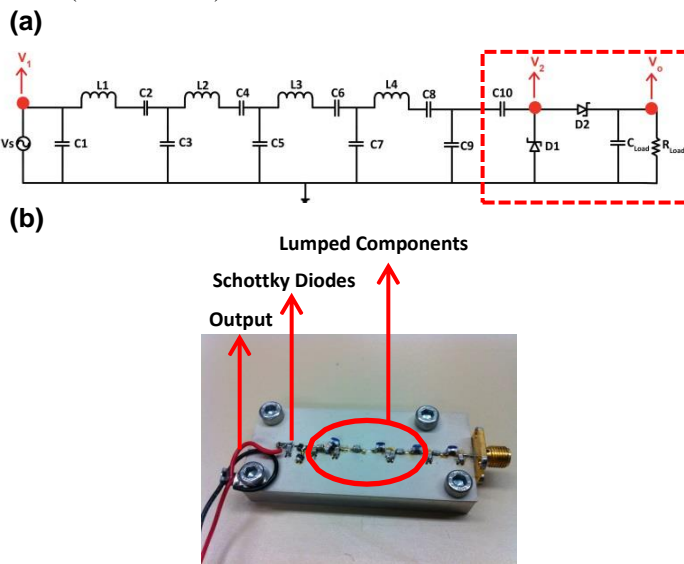Fig. 1. (a) Schematic of the FM rectifier. The optimised values of the standard chip components are: C1=30 pF, L1=150 nH, C2=33 pF, C3=82 pF, L2=150 nH, C4=24 pF, C5=160 pF, L3=82 nH, C6=62 pF, C7=82 pF, L4=560 nH, C8=150 pF, C9=3.6 pF, C10=1 nF, C_{load}=820 pF, R_{load}=18 kΩ [45]. (b) Fabricated rectifier prototype.
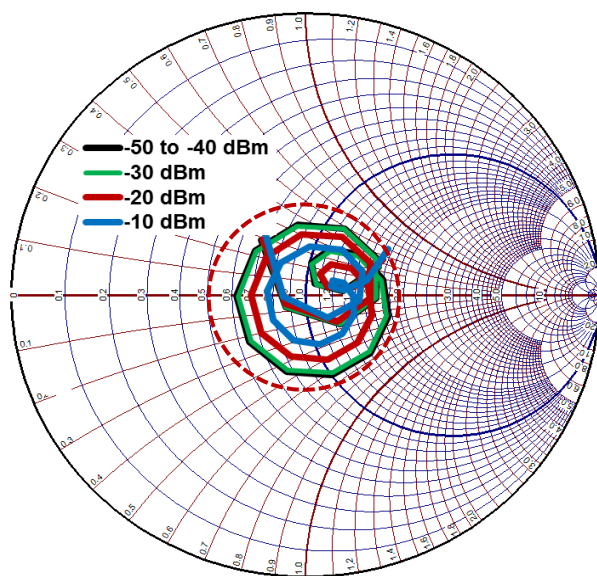

Fig. 2. Measured FM band rectifier impedance matching over 89-111 MHz, with −50 to −10 dBm (0.01 to 100 µW) input RF power. (The 2:1 VSWR boundary is shown with a dashed circle on the Smith Chart).

Fig. 1 depicts the rectifier schematic and prototype, which is used for single-tone and multi-tone analyses in this work. The red circles indicate the points where simulations and measurements are carried out (for both voltage and current).

A voltage doubler topology (the dashed circuit) was used to increase the voltage applied to the series diode in the rectifier [1]. Hence, for a given input power level, the voltage across the series rectifying diode is increased, leading to better conversion efficiency (in comparison with a single-diode envelope detector with the same input power). In this work, a sensitive Schottky detector HSMS2850 (Cj=0.18 pF, Rs=25 Ω, Is=3×10^{-6} A)[42] is chosen due to its low series resistance (Rs), junction capacitance (Cj), and threshold voltage (150 mV) which supports rectification at low input power levels.

In order to evaluate the input matching network performance with various input power levels, a large signal S-parameter (*LSSP*) analysis was conducted. Fig. 2 demonstrates the measurement results using a vector network analyzer (*VNA*) for the input impedance of the circuit presented in Fig. 1. The proposed matching circuit achieves a voltage standing wave ratio (*VSWR*) < 2 at the desired frequency band (89-111 MHz) over input power levels from −50 to −10 dBm (0.01-100 µW). The proposed FM band rectifier circuit with 22% fractional bandwidth is well-matched (|*S11*| < −10 dB) over the broad range of very low input powers [45], [46].

It should be noted that the resistor and capacitor at the output act as a low pass RC filter and remove high frequencies. Using Large Signal S-Parameters analysis in *Keysight ADS* software, the load resistance and the load capacitor were optimised to achieve optimum input matching and power conversion efficiency (PCE).
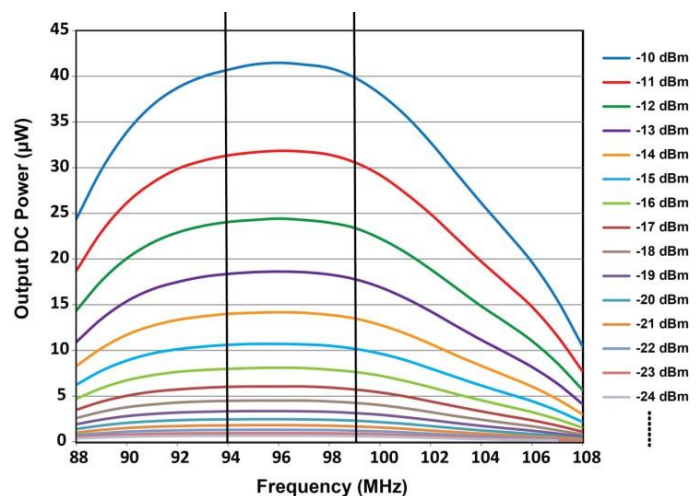

Fig. 3. Simulated output DC power versus frequency for the FM rectifier circuit at different input power levels. Various frequencies from 94 to 99 MHz with similar output will be selected for multi-tone analysis.

Fig. 3 illustrates the frequency response of the rectifier (using harmonic balance (HB) analysis in *ADS)* and indicates that it has a quite similar output DC power (similar efficiency) at the

selected frequencies between 94-99 MHz; hence, a fair comparison between various tones can be performed within this range.

It should be noted that, the true efficiency is defined as the ratio of output DC power (the available power) to the RF input power delivered to the rectifier circuit (1). For the purpose of this study the total average input power (P_{in}) is kept the same in single-tone and multi-tone cases.

$$\eta = \frac{P_{Out,DC}}{P_{in}} = \frac{V_{DC}^2}{R_L \times P_{in}} \qquad (1)$$

B. Multi-tone Signal Model

As mentioned earlier, for the purpose of this study the input power (P_{in}) is the same in single-tone and multi-tone cases.

$$P_{in} = P_1 + P_2 + P_3 \ldots + P_N \qquad (2)$$

where $P_1=P_2=P_3=\ldots=P_N$ and N refers to the number of tones

A time-domain single-tone input signal at frequency ω_1 with amplitude A and phase φ is considered as follows:

$$x(t)_{single-tone} = A\cos(\omega_1 t + \varphi) \qquad (3)$$

An N-tone evenly spaced multi-tone signal at the input is considered with amplitudes $B_1 = B_2 = \ldots B_N$ and frequencies ω_1, $\omega_{2=} \omega_1+\Delta\omega, \ldots, \omega_{N=} \omega_1+(N-1)\Delta\omega$ where $\Delta\omega$ is the frequency spacing between the tones.

In order to generate the highest DC output voltage with a multi-tone signal and to reduce the complexity of this analysis, all the tones are assumed to be aligned in phase [35]. Hence, a multi-tone signal with zero phase difference between the tones can be represented by (4)

$$x(t)_{multi-tone} = B_1\cos(\omega_1 t) + B_2\cos(\omega_2 t) + \cdots B_n\cos(\omega_N t) \qquad (4)$$

where $\omega=2\pi f$ and frequencies are selected between 94-99 MHz. The amplitude B of the multi-tone signal can be computed by considering the power in the single tone.

$$P_{in-single} = \frac{A^2}{2R} \qquad (5)$$

where R is the load resistance and A is the amplitude of the single-tone signal. Hence, if the source is a 50 Ω source, then A will be the open-circuit peak output voltage and R will be 50 Ω. For the multi-tone case, the power in each tone will be $B^2/2R$ and since the average available power in the multi-tone case is assumed to be the same as the single tone, hence, the amplitude B of the multi-tone signal is:

$$B = \frac{A}{\sqrt{N}} \qquad (6)$$

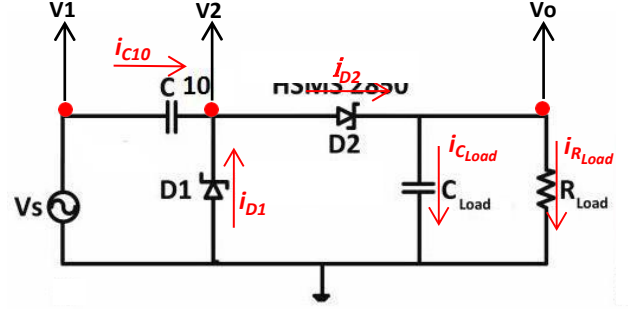### C. Multi-tone Excitation Analysis of the Voltage Doubler

Fig. 4. Schematic of a voltage doubler rectifier (without matching network) consisting of a voltage clamper (C10 and D1), a peak rectifier (D2 and C$_{Load}$) and an output low pass RC filter (C$_{Load}$ and R$_{Load}$).

The voltage doubler rectifier depicted in Fig. 4 consists of a voltage clamper formed by *D1* and *C10* (1 nF) and a peak rectifier formed by *D2* and load capacitor *C$_{load}$* (820 pF). The *R$_{load}$* and *C$_{load}$* form a low pass *RC* filter, which removes high frequencies from the output signal.

In the negative half cycle of the input, *D1* is on while *D2* is cut off. Hence, *C10* charges to $V_s - V_{th1}$, where V_s refers to the amplitude of the input RF signal and V_{th1} denotes the threshold voltage of *D1* (~150 mV). Therefore, the right end of the voltage doubler circuit (comprising *D2*, *C$_{load}$* and *R$_{load}$*) is grounded by the conducting *D1*, while the voltage across the clamping capacitor (*C10*) is charged at the negative peak of the RF input. This explains the operation of the clamper [1], [46]. During the positive half cycle of the input signal, *D2* and *C$_{load}$*, act as a half-wave rectifier. Since *C10* is in series with the voltage source, *D2* receives a total of $2V_s - V_{th1}$ at the peak of the input sine wave; V_s from the source and $V_s - V_{th1}$ from *C10* (*C10* acts as a DC voltage source). Therefore, *C$_{Load}$* charges at $2V_s - V_{th1} - V_{th2} = 2V_s - 2V_{th}$ (V_{th2} is the threshold voltage of *D2* and is equal to the threshold voltage of D1).
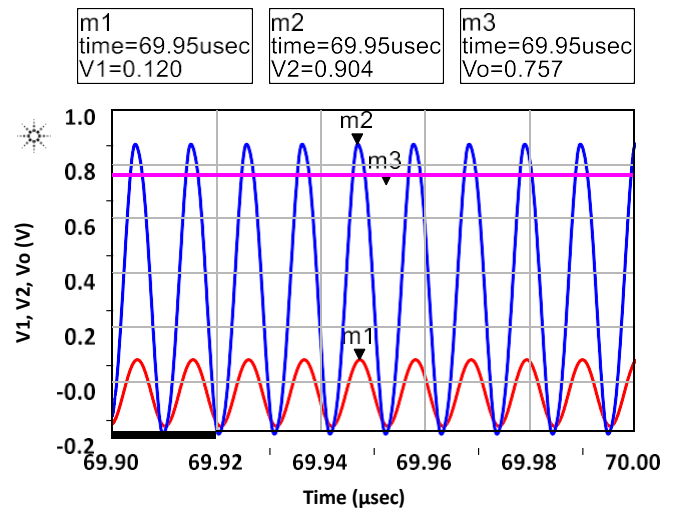

Fig. 5. Time domain waveforms of the voltage doubler rectifier with single tone excitation (at 96 MHz with −10 dBm input power). V1 denotes the input sine wave, V2 refers to the delivered voltage to the input of the rectification device, and Vo is the output DC voltage.

The operation of the voltage doubler rectifier (in the presence of the matching network of Fig. 1) is depicted in Fig. 5. As can be seen, by using this topology the amplitude of the input RF signal (red trace, *V1*) is clamped from 120 mV to 904 mV and is delivered to the rectification device (blue trace, *V2*). Hence, a DC voltage of 757 mV is generated at the output (*Vo*) with −10 dBm input RF power. The small difference between V2 and *Vo* is due to the threshold voltage of the Schottky diodes [44], which is not negligible at low input RF power. Therefore, the performance of the voltage doubler depends on the input signal waveform (*V1*).

As illustrated in Fig. 5, in a voltage doubler rectifier, the voltage at the input to the diodes (*V2*) is much higher than the applied voltage at the input of the matching network (*V1*). The increase between *V1* and *V2* is due to the matching network performance. Since the input to the diodes is highly capacitive (close to open circuit), by realizing conjugate matching a high voltage level at the input of the voltage doubler will be achieved. The matching circuit is working as an impedance transformer that converts the larger (capacitive) impedance seen at the input of the voltage doubler to smaller impedance (typically 50 Ω). Hence, the voltage at the input of the voltage doubler (with larger impedance) is higher than that at the input of the matching network (with smaller impedance); this means *V2* will increase more by the time it is applied to *D2*.

It is worth mentioning that in Fig. 5 all the demonstrated values indicate time domain instantaneous voltages. Furthermore, the time axis runs from 69.9 µsec until 70 µsec as the circuit reached its steady state after 65 µsec.

In order to analyse the voltage doubler behavior mathematically, the non-linear behaviour of the diode is represented by the Shockley equation.

$$i_D = I_s \left(e^{\frac{V_D}{nV_T}} - 1\right) \tag{7}$$

Here, i_D is the diode current, I_S is the saturation current (3 µA) [44], V_D is the voltage across the Schottky barrier, V_T is the thermal voltage *kT/q* (Boltzmann constant times temperature divided by electron charge), and *n* is the ideality factor.
During the negative half cycle of the input, *D1* is conducting and the voltage clamper (formed by *D1* and *C10*) is activated. Hence, applying *Kirchhoff's* law and assuming no reflections due to an impedance mismatch, the voltage across D_1 (*V2*) and the current through C_{10} ($i_{C10} = -i_{D1}$) are expressed as:

$$V_{D1} = V_1 - V_{C10} \tag{8}$$
$$i_{C10} = C_{10} \frac{dV_{C10}}{dt} = -I_s \left(e^{\frac{V_2}{nV_T}} - 1\right) \tag{9}$$

The output DC voltage can be calculated by applying *Kirchhoff's* law and by deriving equations based on the rectifying circuit (consisting of the rectification device (*D2*) and the load capacitor, C_{load} (Fig. 4)).
In the following equations *V2* refers to delivered voltage to the rectification device (*D2*), V_{D2} indicates the voltage drop on *D2*, and *Vo* is the instantaneous output voltage in the time domain.

Furthermore, i_{D2}, $i_{C\,Load}$ and $i_{R\,Load}$ refer to the current through *D2*, the load capacitor and resistor, respectively.

$$V_{D2} = V_2 - V_O \tag{10}$$

$$i_{D2} = i_{C_{Load}} + i_{R_{Load}} \tag{11}$$

Based on (7), the current through *D2* can be expressed as,

$$i_{D2} = I_s \left(e^{\frac{V_{D2}}{nV_T}} - 1\right) \tag{12}$$

$$i_{C_{Load}} = C_{Load} \frac{dV_O}{dt} \tag{13}$$

$$i_{R_{Load}} = \frac{Vo}{R_{Load}} \tag{14}$$

$$\frac{dV_O}{dt} = \frac{i_{D2} - i_{R_{Load}}}{C_{Load}} \tag{15}$$

Hence, *Vo* could be calculated by substituting (7) and (14) in (15):

$$\frac{dV_O}{dt} = \frac{I_s}{C_{Load}} \left(e^{\frac{V_{D2}}{nV_T}} - 1\right) - \frac{Vo}{R_{Load}C_{Load}} \tag{16}$$

By calculating the instantaneous output voltage in the time domain, the DC output voltage can be computed:

$$V_{DC} = \frac{1}{T} \int_{to}^{T+t0} Vo\,(t)\,dt \tag{17}$$

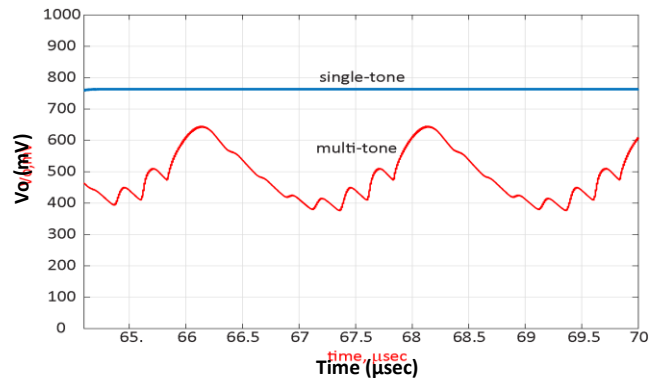Here, *T* indicates the evaluated periods of the instantaneous output voltage signal.

Fig. 6. Time domain analysis of the voltage doubler rectifier using the theoretical model and numerical analysis in Matlab. Blue line shows single tone excitation and red line corresponds to eight-tone excitation. In both cases, the average available power is the same (−10 dBm).

Equation (16) is a non-linear differential equation which is solved in Matlab using numerical analyses. The achieved output voltages of single-tone and multi-tone excitations based on the theoretical model (17) are illustrated in Fig. 6. In both scenarios,

the input RF power is −10 dBm (100 μW). As can be seen, applying eight tones simultaneously results in a lower output DC voltage compared to the single-tone case with the same input power.

The reason is that in the negative half cycle of the input, *D1* is on and *C10* charges to $V_s - V_{th1}$, however, in the multi-tone case, the negative voltage exists for a shorter period of time in comparison to the single-tone case (see also time-domain analysis, Fig. 8, Fig. 9, Fig. 10 and Fig. 11), this means the voltage is not being sufficiently negative. As a result, in the multi-tone case, the clamper capacitor *C10*, does not charge up to the proper level, which degrades the voltage doubler performance and the DC output. Therefore, in multi-tone cases, the operation of the voltage doubler is affected, and it does not act as a true doubler.

The reasons for obtaining a lower amount of DC output in the multi-tone case will be elaborated on later in section III by conducting simulations (in time domain and frequency domain) and also measurements.

III. MULTI-TONE EXCITATION MEASUREMENT AND SIMULATION RESULTS OF THE FM RECTIFIER

The effect of applying multi tones simultaneously with different levels of input power was analysed to validate the theoretical model derived in Section II. To address this, frequency and time domain analyses and measurements are conducted to clarify the findings.

A. Harmonic Balance Analysis and Measurements

In order to demonstrate the effect of multi-tone excitation on the DC response of the rectifier, various concurrent tones (in the matched FM frequency band) were applied to the circuit in the *Keysight ADS* software. The output DC voltage of the rectifier was evaluated using a Harmonic Balance (HB) simulation [1], [46]. The output DC power was then calculated using the output DC voltage across the load resistor.

In the multi-tone measurement, various signals were generated simultaneously with multiple 1 GHz *Rohde* and *Schwarz* signal generators (up to eight generators were used), summed using a power combiner, and passed to the rectifier. The output DC voltage across the load resistance was measured using a Fluke 79III voltage meter and also a digital voltage meter.

For the purpose of this study the input power (P_{in}) is kept the same in single-tone and multi-tone cases. For example, the DC output of the rectifier when one tone of −10 dBm is available at the input can be compared with the output of the rectifier when two tones of −13 dBm or three tones of −14.77 dBm or four tones of −16.02 dBm are available at the input, as in all these cases the total combined input power is the same (−10 dBm). Hence, the total average power (measured at the input of the rectifier circuit) in the multi-tone case, is set to same value as the single-carrier signal. For more clarity, the input power scaling (in multi-tone cases) with the number of tones is

presented as follows:

$$P_{in-multi}(dBm) = 10 * \mathrm{Log}\,(N) + Pin_{each-tone}(dBm) \quad (18)$$

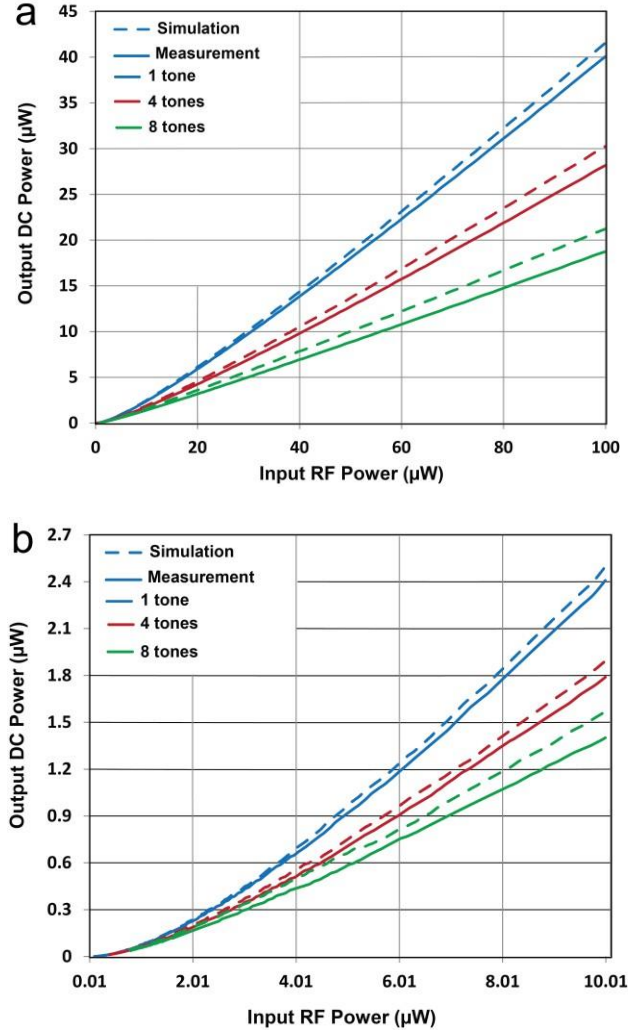where *N* refers to the number of tones and P_{in} indicates the average available input power in dBm.

Fig. 7. (a) Simulated and measured output DC power as a function of input RF power for single and multi-tone excitation with 0.5 MHz frequency spacing (from 94-97.5 MHz) with −50 to − 10 dBm (0.01-100 μW) input RF power. (b) with −50 to − 20 dBm (0.01-10 μW) input RF power.

Fig. 7(a) and Fig. 7(b) compare the simulated and measured output DC power that can be obtained from various simultaneous tones over a broad low input power range of −50 to −10 dBm (0.01-100 μW). Fig. 7 (b) shows the lower power section of Fig. 7 (a) in more detail. The measurement and harmonic balance (HB) simulation results are in good agreement and clearly prove the theoretical analysis. The small difference between the simulations and measurements is due to the ohmic loss, component model accuracy in *ADS*, diode parasitics, and tolerance of the circuit lumped components.
As can be seen from the HB analysis and measurement results, applying multi-tone with the same average available RF power results in a lower output DC power compared to the single-tone
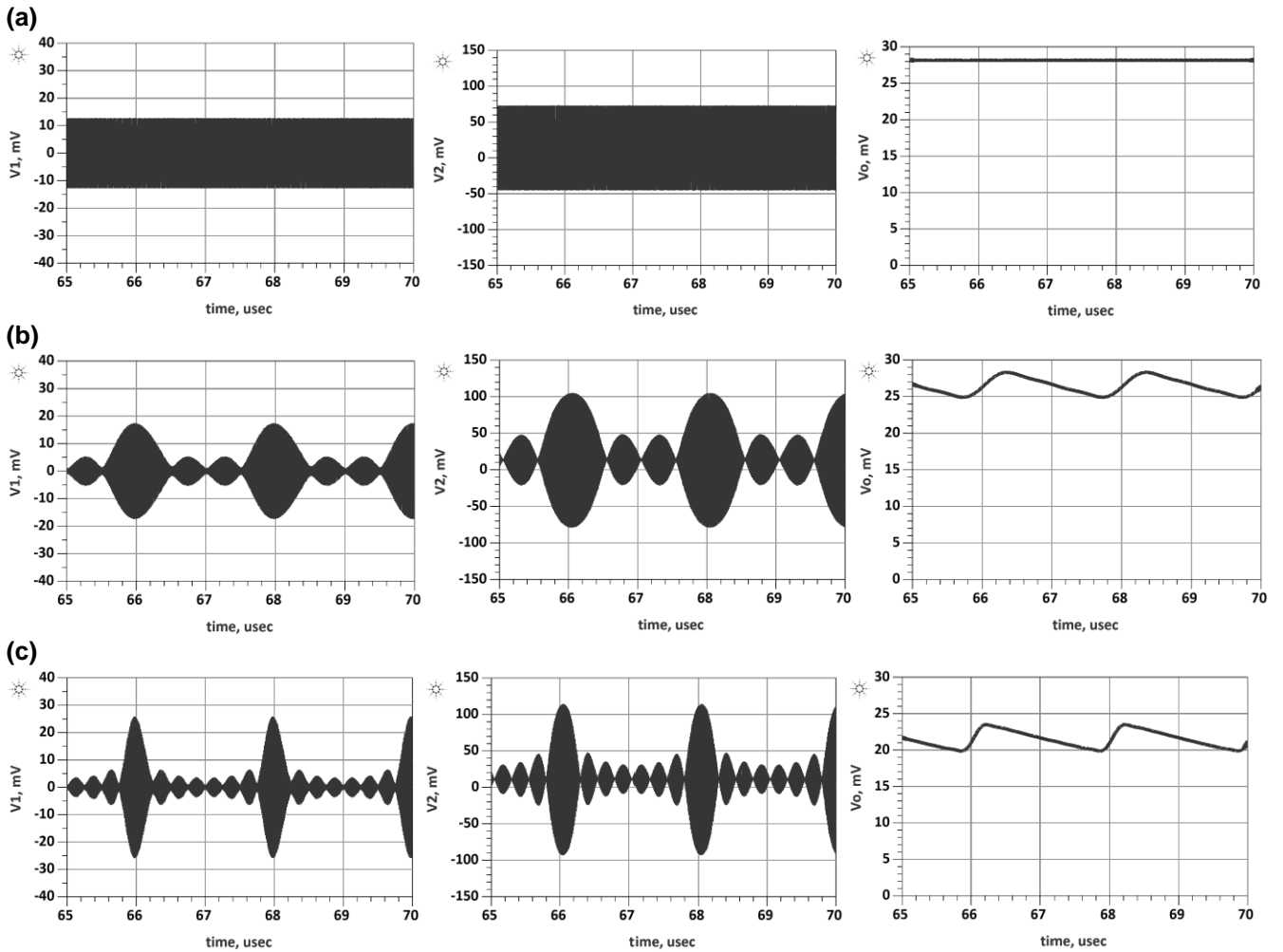
Fig. 8. Time domain analysis for single-tone and multi-tone with an average available power of −30 dBm. (a) One tone of −30 dBm (1 µW). (b) Four tones of −36.02 dBm. (c) Eight tones of −39 dBm.

case with the same input power. For example, as illustrated in Fig. 7 (a), when eight tones with an average available power of 100 µW (−10 dBm) (which means 12.5 µW (−19 dBm) each), with 0.5 MHz spacing are applied to the rectifier, around half of the output DC power (21 µW) can be generated when compared to the single tone of 100 µW (−10 dBm). This trend is evident to low input power levels of 0.01-10 µW (−50 to −20 dBm) as depicted in Fig. 7 (b).

Based on the HB analysis and experimental results of different cases, it is evident that applying multi tones with the same average available RF power results in a lower output DC power when compared to the single-tone case with the same input power. However, further analysis needs to be performed in the time domain to explain this.

B. Multi-tone Excitation Time Domain Analysis

Generating a lower amount of output DC power when the rectifier is driven by several tones is a complex problem. This requires precise analysis of the voltage doubler rectifier performance under multi-tone excitation in the time domain.

In order to investigate the reason for obtaining a lower amount of output DC power in the multi-tone case (as seen in Fig. 7), the delivered voltage to the rectification device ($V2$) and also the output voltage of the rectifier (Vo) are evaluated. Various cases were analysed with −30 dBm, −20 dBm and −10 dBm input RF power (Fig. 8, Fig. 10 and Fig. 11 respectively). Further analyses at −40 dBm and −50 dBm were also performed, and it is evident that the same trend applies to the lower power levels (see Tables A-I and A-II in Appendix).

Fig. 8 (a), (b) and (c), show TD analysis of the rectifier with one-tone, four-tone and eight-tone excitations, respectively, with an average available power of −30 dBm (1µW) and with 0.5 MHz frequency spacing and zero phases. By comparing one-tone (Fig. 8 (a)) and eight-tone excitation (Fig. 8 (c)), in the multi-tone case the total output voltage has dropped from 28 mV (with one tone) to ~21 mV (with eight-tones) with an average available power of −30 dBm in both cases. Table I summarises the rectifier performance for single and multi-tone cases with −30 dBm input RF power. The peak- peak values of the input voltage ($V1p$-p), delivered voltage to the voltage doubler ($V2p$-p), the output voltage of the rectifier (Vo), the current through C_{10} (clamper capacitor), the dynamic resistance of $D1$ (r_d) and also DC value across $D1$ are provided.

The values in Table I are derived from Fig. 8. For example in the single-tone case (Fig. 8 (a));

$V1p\text{-}p$= 13+13= 26 mV and $V2p\text{-}p$=73+45=118 mV.

The DC value across $D1$ (which is referred to as the DC offset voltage) in Fig. 8 can be calculated as follows:

DC value across D1 = V2(peak) − positive voltage amplitude

which becomes 14 mV for the single tone case.

$$\text{DC value across D1(single tone)} = \frac{73+45}{2} - 73 = 14 \text{ mV}$$

TABLE I
TIME DOMAIN ANALYSIS OF THE RECTIFIER AT −30 dBm,
WITH 0.5 MHZ FREQUENCY SPACING, PHASES =0 deg.

N *	V1 P-P (mV)	V2 P-P (mV)	I_{C10} P-P (mA)	DC value across D1 (mV)	r_d of ** D1 (kΩ)	PAPR at V1	PAPR at V2	Vo (mV)
1	26	118	0.0243	14	4.8	2.27	4.26	28
4	36	190	0.0698	~14	2.7	8.38	13.15	~26 ***
8	52	207	0.1	~10	2	16.50	22.51	~21

*N refers to the number of tones

** Dynamic resistance will be elaborated on later in the text.

*** Due to the small ripples, averaged voltage values are used.

Based on Table I, by applying multiple tones with increasing the tone number, the DC value across $D1$ (observed as DC offset in Fig. 8) reduces which consequently prevents $C10$ from charging to its optimum level.

The parameter, which can be used to indicate this change, is the dynamic resistance r_d of $D1$. In order to express the reason for the degradation of the voltage doubler performance in the multi-tone case, the dynamic resistance of $D1$ is analysed [48]. The dynamic resistance is the small signal resistance of the diode at its DC operating point. It is derived from the Schottky's diode equation and it is the inverse of the slope of the current-voltage curve of the diode at the DC operating point. As can be deduced from Table I, by increasing the number of tones the DC value across $D1$ is reduced, and hence, r_d is reduced because the DC value represents a reverse-biasing of $D1$, due to the polarity of $V2$ relative to the orientation of $D1$ (see Fig. 4). This trend is evident to different input power levels of −30 to −10 dBm (Tables I-III).

Therefore, by applying a multi-tone signal, the DC value across $D1$ is reduced and hence, $C10$ will not be able to charge up to its optimum level (this reduction in the DC value can be observed in the dynamic resistance (r_d) change as well).

Peak-to-average power ratio (PAPR) is also calculated at two points ($V1$ and $V2$) and the results are provided in Tables I-III. As can be seen from Table I, PAPR increases by increasing the

number of tones, however, Vo decreases. Therefore, despite previously published papers, PAPR increase is not the main criteria for the DC output enhancement of a rectifier and hence, different factors should be considered for the voltage-doubler topology.

In summary, the reason for the lower DC output voltage in the multi-tone case is due to the input waveform deformation, which is not a conventional sine wave in the multi-tone case. In the multi-tone cases, the negative voltage exists for a shorter period in comparison to the single-tone case and hence, $C10$ does not charge up to its optimal level, which degrades the voltage doubler performance.
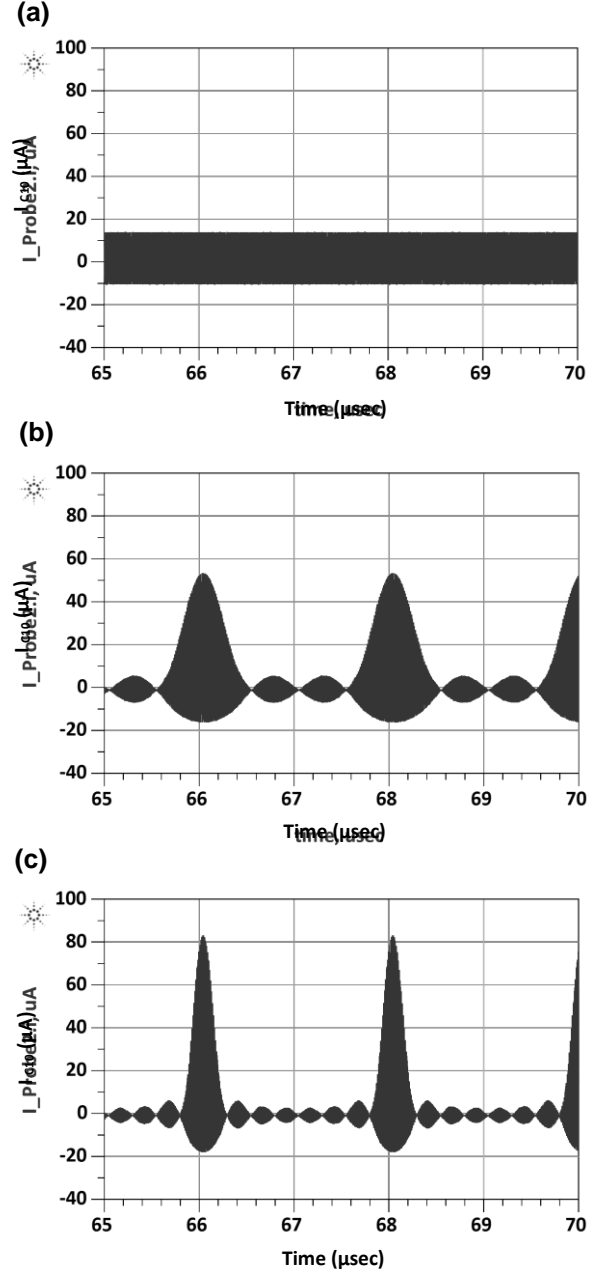

Fig. 9. Time domain analysis of the current through $C10$ (clamper capacitor), for single-tone and multi-tone with an average available power of −30 dBm. (a) One tone of −30 dBm (1µW). (b) Four tones of −36.02 dBm (0.25 µW each). (c) Eight tones of −39 dBm (0.125 µW each).

Therefore, in multi-tone cases, the operation of the voltage doubler is affected, and it does not act as a true doubler.

Changes in the current waveform also degrade the voltage doubler performance in the multi-tone case. As can be seen in Fig. 9, the current (through C_{10}) waveform shape has a sharper peak in the multi-tone case and hence, over the AC cycle, less current is generated compared with the single tone case (due to the lower voltage across the parallel diode). Consequently, when the rectifier is driven by several tones, the total amount of diode current over time is much smaller compared to the single tone excitation case, even though the peak values are increased. This again prevents the clamping capacitor from charging to its optimum level.

Considering the multi-tone cases in Table I, when the peak-peak value of *V2* is increased (e.g. from 118 to 207 mV with the single tone and eight tones, respectively) at the input power level of −30 dBm, the output DC voltage is decreased (from 28 to ~21 mV). This is mainly due to the DC value drop (from 14 to 10 mV) which results in less current and subsequently a lower r_d (from 4.8 to 2 kΩ) since r_d is the inverse of the derivative of current versus voltage. These changes directly influence the voltage doubler performance.

It is worthwhile to highlight that in Fig. 8, the spacing between the two peaks (in μsec) corresponds to the period of the beat frequency, which is the frequency difference between the various tones (in this case the frequency spacing is 0.5 MHz). This is the same in Fig. 9, Fig. 10 and Fig. 11.

It should also be noted that by selecting a higher value output capacitor, the ripple at the output will be reduced by removing the beat frequency. However, the load impedance and load capacitor were optimised to achieve optimum input matching and power conversion efficiency (PCE), hence, by changing these values, the rectifier circuit efficiency will be degraded.

Fig. 10 (a), (b) and (c), depicts time domain (TD) analysis of the rectifier with one-tone, four-tone and eight-tone excitations respectively with an average available power of −20 dBm (10 μW). The frequency spacing is the same as in the previous case (0.5 MHz), and phases are zero degree.

Comparing one tone (Fig. 10 (a)) and eight-tone excitation (Fig. 10 (c)), in the multi-tone case the total output voltage has dropped from 176 mV (with one tone) to ~130 mV (with eight-tones), with average available power of −20 dBm at the input in both cases.

(a)
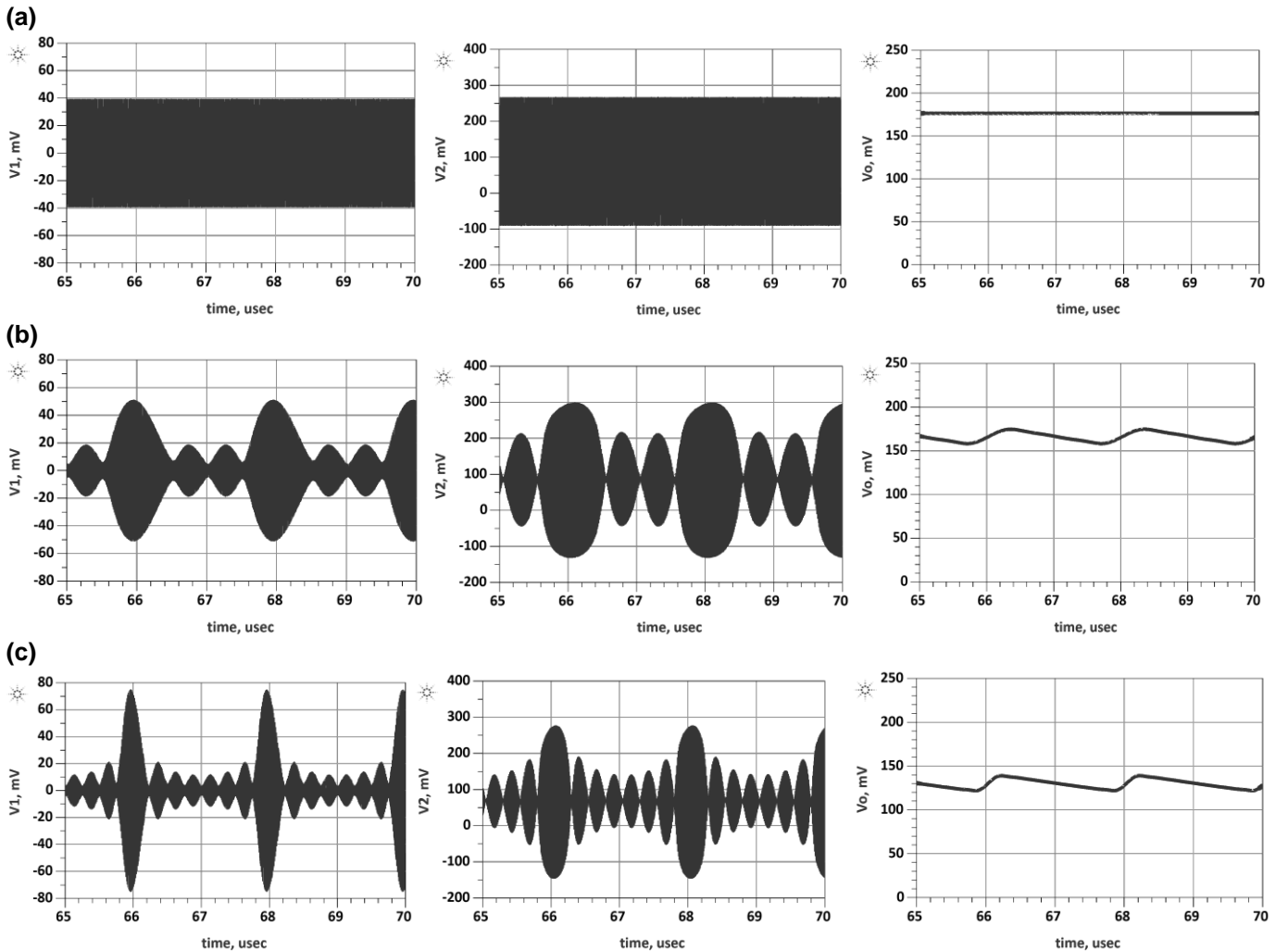
(b)

(c)

Fig. 10. Time domain analysis for single-tone and multi-tone with an average available power of −20 dBm. (a) One tone of −20 dBm (10 μW). (b) Four tones of −26.02 dBm (c) Eight tones of −29 dBm.
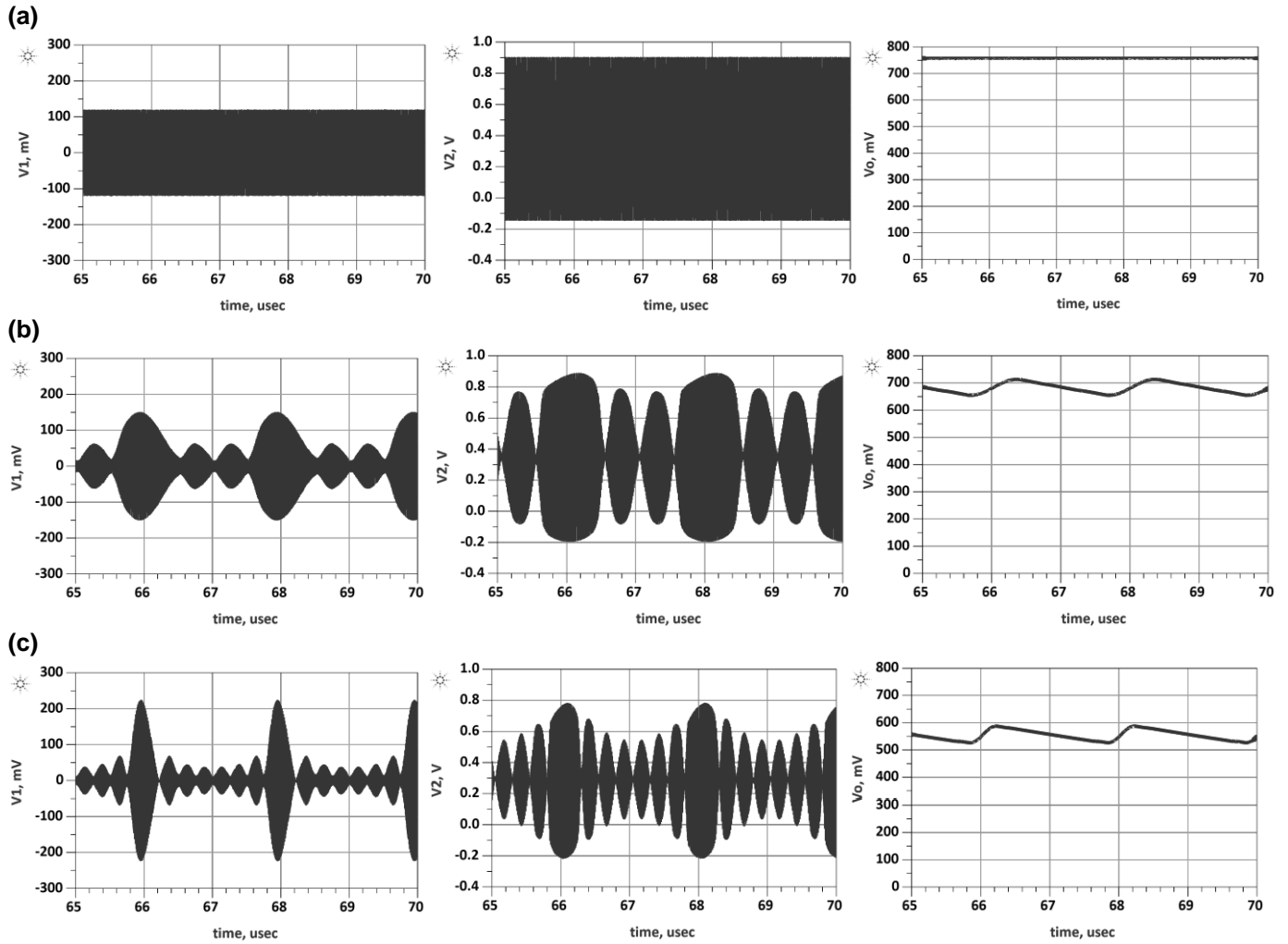
Fig. 11. Time domain analysis for single-tone and multi-tone with an average available power of −10 dBm. (a) One tone of −10 dBm (100 µW). (b) Four tones of −16.02 dBm . (c) Eight tones of −19 dBm.

Table II summarises the rectifier performance for single and multi-tone cases with −20 dBm input RF power.

TABLE II
TIME DOMAIN ANALYSIS OF THE RECTIFIER AT −20 dBm,
WITH 0.5 MHZ FREQUENCY SPACING, PHASES=0 deg.

N	V1 P-P (mV)	V2 P-P (mV)	I_{C10} P-P (mA)	DC value across D1 (mV)	r_d of D1 (kΩ)	PAPR at V1	PAPR at V2	Vo (mV)
1	78	358	0.09	88	3.6	2.21	5.29	176
4	102	400	0.32	~84	1.25	8.21	18.6	162
8	150	424	0.44	67	~0.9	16.54	30.2	~130

Fig. 11, illustrates TD analysis of the rectifier with one-tone, four-tone and eight-tone excitations with an average available power of −10 dBm (100 µW).

In this case, again, the phase is assumed to be zero, and the frequency spacing is 0.5 MHz. Comparing one-tone (Fig. 11 (a)) and eight-tone excitation (Fig. 11 (c)), in the multi-tone case the total output voltage has dropped from 757 mV (with one tone) to ~555 mV (with eight tones) with average available

power of −10 dBm at the input in both cases.

As provided in Table III (at the input power level of −10 dBm) the voltage delivered to the voltage doubler is decreased (from 1051 to 996 mV with the single tone and eight tones, respectively). This is mainly due to the breakdown voltage effect caused by the increasing peak values of the input signal (from 240 to 449 mV with the single tone and eight tones respectively). Moreover, the DC value reduces across D1 from 378 to 292 mV with the single-tone and eight-tone respectively (this is the DC offset in Fig. 11) and degrades the rectification device performance by reducing the dynamic resistance (r_d) of D1 (from 2.3 to 0.5 kΩ) significantly. Hence, the output DC voltage is decreased from 757 to 555 mV (with the single-tone and eight-tone excitations, respectively) with the average available power of −10 dBm due to the breakdown voltage effect as well as the deformation in the input waveform, though the peak-to-average power ratio (PAPR) is increased.

In order to draw a conclusion, different cases were analysed (see Tables A-I and A-II in Appendix) and similar outcomes were achieved. These results demonstrate that multi-tone excitation may decrease the output DC power and depends highly on the circuit characteristics.

TABLE III
TIME DOMAIN ANALYSIS OF THE RECTIFIER AT −10 dBm,
WITH 0.5 MHZ FREQUENCY SPACING, PHASES=0 deg.

N	V1 P-P (mV)	V2 P-P (mV)	I_{C10} P-P (mA)	DC value across D1 (mV)	r_d of D1 (KΩ)	PAPR at V1	PAPR at V2	Vo (mV)
1	240	1051	0.45	378	2.3	2.17	8.59	757
4	302	1031	1	343	1	8.19	26.39	~680
8	449	996	2	292	~0.5	16.72	40.71	~555

IV. CONCLUSION

This paper demonstrates the effect of multi-tone excitation on the output DC response of a rectifier circuit designed for RF energy harvesting in the FM broadcast band. Theoretical analysis as well as frequency and time domain simulations were conducted to clarify the findings. Measurements were also performed to validate the results.

It was demonstrated that applying multi tones simultaneously (within the matched frequency band) results in a lower total average output DC voltage/power, when compared with the single-tone case with the same average available power. This trend was evident over a broad low input power range of −50 to −10 dBm. The reason for obtaining a lower amount of output DC power with the multi-tone excitation was the deformation in the input signal waveform leading to a reduction in the DC voltage across the voltage clamper capacitor and consequently a reduction in the output DC power. These effects, combined with the increased "peakiness" in the input signal waveform prevent the clamping capacitor from charging to its optimal DC voltage, thereby degrading the performance of the voltage doubler rectifier circuit.

The achieved results demonstrated that multi-tone excitation (with the same total power level as the single tone) might decrease the output DC power of a voltage-doubler rectifier and highly depends on the topology which the rectifier is configured. In fact, the concept of increasing the DC output power by using multi-tone excitation is not true for every system, and in contrast, it is shown here that it degrades the output DC power of a voltage-doubler rectifier (even with high peak-to-average power ratio).

V. APPENDIX

Further analyses at −50 (0.01 µW) and −40 dBm (0.1 µW) are performed to clarify the findings and the results are provided in Table A-I and Table A-II.

TABLE A-I
TIME DOMAIN ANALYSIS OF THE RECTIFIER AT −50 dBm,
WITH 0.5 MHZ FREQUENCY SPACING, PHASE=0 deg.

No. tones	V1 P-P (mV)	V2 P-P (mV)	I_{C10} (mA) P-P	DC offset across D1(mV)	r_d of D1 (KΩ)	Vo (mV)
1	2	12	0.0022	0	5.4	~0.32
4	4	24	0.0045	0	~5.3	~0.3
8	6	30	0.0058	0	~5.1	~0.25

TABLE A-II
TIME DOMAIN ANALYSIS OF THE RECTIFIER AT −40 dBm,
WITH 0.5 MHZ FREQUENCY SPACING, PHASE=0 deg.

No. tones	V1 P-P (mV)	V2 P-P (mV)	I_{C10} (mA) P-P	DC value across D1(mV)	r_d of D1 (KΩ)	Vo (mV)
1	8	37	0.0071	1.5	~5.22	3.1
4	12	69	0.0144	~1.4	~4.8	~2.9
8	18	88	0.02	1	~4.4	~2.5

Based on the time domain (TD) simulation, it is evident that a similar trend is applied to the very low power levels as it was discussed in the paper (Tables I-III). However, due to a very small variation of DC offset and hence, dynamic resistance (r_d), in multi-tone cases the output DC voltage does not change significantly (at −50 and −40 dBm).

It is worthwhile to highlight that, by reducing the input RF power levels (from −10 to −50 dBm) the amount of DC offset across *D1* decreases (in all cases) and reaches to 0 at −50 dBm. Therefore, in multi-tone cases with very low power levels, less reduction of the output is expected. The achieved outcomes are in complete agreement with harmonic balance (HB) and measurement results (Fig. 7).

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