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An Asymmetrical Step-Up Multilevel Inverter Based on Switched-Capacitor Network

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Received: 3 June 2019; Accepted: 17 June 2019; Published: 23 June 2019

Abstract: This paper presents a transformerless step-up multilevel inverter based on a switched-capacitor structure. One of the main contributions of the proposed topology is replacing the separated DC voltage source with capacitors which are charged at predetermined time intervals. Therefore, a high-level staircase voltage waveform can be achieved by discharging some of these capacitors on the load. The other contribution of the proposed structure is to eliminate the magnetic elements which traditionally boost the input DC voltage. In addition, asymmetrical or unequal amounts of capacitor voltages create more voltage levels, which enable voltage level increments without increasing the number of semiconductor devices. This paper introduces a self-balanced boost Switched-Capacitors Multilevel Inverter (SCMLI) which is able to create a nearly sinusoidal voltage waveform with a maximum voltage of up to 45 times that of the input voltage DC source. Higher level output voltage levels are also achievable by extending the circuit topology. After determination of the switching angles and selecting the proper switching states for each level, an offline NLC method is used for modulation, which eases the control implementation. Analysis, simulation and experiments are carried out for a 91-level inverter (45 levels for positive and negative voltages and one for zero voltage) are presented.

Keywords: multilevel inverters; self-balanced; single source; transformerless

1. Introduction

Multilevel inverters (MLIs) are widely used in high voltage high power applications such as renewable energy resources, HVDC systems, power industry, high power motor drives, and energy transmission systems [1]. The term "multi-level" was started with the three-level converter in 1981 by Nabae [2], and gradually expanded to higher levels. These converters include arrays of power semiconductors, capacitors and DC sources which generate a staircase voltage waveform through a proper pulse pattern. Neutral point clamped (NPC) and flying capacitor (FC) [3] are among the famous topologies of MLIs, which utilize different capacitors and switches to generate a staircase voltage waveform. Cascaded H-Bridge (CHB) topology is introduced for systems with multiple separate DC sources such as solar cell farms [4] and a single DC source [5].

Increasing the voltage levels improves output voltage quality but leads to an increment of switching devices and other components. This consequently causes complexity in the control and maintenance of such systems. Multilevel converters with asymmetrical or unequal DC sources are introduced to achieve higher voltage levels without increasing the number of circuit components [6,7]. In order to achieve higher voltage levels at the output, [8–10] new structures with fewer components and DC sources have been proposed. Different topologies for symmetric and asymmetric multilevel inverters are shown in [11], which summarizes recent improved topologies. For both symmetrical and asymmetrical topologies, multiple DC sources are required, which may not be available in all conditions [12]. Capacitors can be used in these structures but they also need additional circuits for voltage balancing. Therefore, a converter with the lowest possible number of DC sources and self-balanced capacitors is essential in order to achieve higher voltage levels with a reduced number of components [13]. On the other hand, low voltage DC input sources are used in many applications such as photovoltaic farms [14], electric vehicles [15] and battery applications [16]. Step-up DC-AC Power converters are required to generate voltage for AC loads or grid connection purposes. Traditionally, multi-stage power conversion is required to achieve the required voltage. A transformerless converter is required to convert low voltage DC to high output AC voltage at a single stage.

The authors of [17] presented a single source self-balanced SCMLI topology which uses two switches, two diodes and a capacitor to generate each voltage level. A bipolar MLI based on CHB structure is presented at [18] which consist of full bridge modules. These two topologies suffer from a large number of switching components and high voltage stress on switches. To overcome this limitation, [19] presented a modular SCMLI structure which consists of modules with three powers switches. The number of semiconductors decreased in [20,21] by improving this topology by replacing a diode instead of a switch, which causes a reduction of the number of required drivers as well. The structure proposed in [22] reduces the number of switches to one in each module, which leads to reducing drivers and ease of control in comparison with other topologies. However, the voltage stress on each of the switches increases by voltage level increment as well as increasing the number of series diodes. The authors of [23] presented another SCMLI to reduce voltage stress on the switches based on cascading different modules together. The main problem of this structure is the requirement of additional circuits for balancing purposes.

In this paper, the proposed topology solves the main issues of the mentioned topologies which are (i) the number of switching devices, and (ii) voltage stress on different components during level increment. Moreover, the proposed structure has the ability to boost the input voltage without using any magnetic elements, and can convert a low DC voltage to a high voltage AC output by using single DC source. The challenge of the number of components necessitates the presentation of a step up DC-AC MLI converter based on SC network with reduced number of circuit elements such as capacitors and power semiconductors. Charging the capacitors (up to multiples of input voltage) and smart discharging of several capacitors at predetermined periods enables the proposed topology to increase the number of voltage level steps and boost ratio of the converter. As the input voltage of the converter is low, the rating of components is kept within an acceptable range.

The next section of the paper explains the circuit topology and its modules. Topology operation such as switching states, mathematical analysis, modulation strategy, charging and discharging of capacitors are analyzed at Section 3. A circuit extension and a comparative study is carried out in Section 4. The analyses are validated by a simulation and experimental results in Section 5. A conclusion is presented in Section 6.

2. Proposed Topology

Figure 1a shows circuit topology of the multi-stage converter presented by F. Z. Peng et al. [24] where the capacitors of previous stages charge the capacitors of the next stages and then, the capacitors of the last stage generate multilevel AC voltage through a specific pulse pattern. Half-bridge building block modules (see Figure 1b) are used to connect the capacitors together. This module includes two

two-quadrant switches (S_1 and S_2) which enable bidirectional current flow but can only block positive off-stage voltage. As the capacitors of the last stage are involved in output voltage generation and all capacitors are charged to *Vin*, the number of circuit components increases in order to achieve higher output voltages. This is because of the limitation of the building blocks to control the currents from different ports of the module. Charging capacitors to multiples of input voltage leads to decrement of circuit components. For this purpose, building blocks are required to control the current flow from three ports of the module. Two other switches (S'_1 and S'_2) are added to the module in order to control the current flow from different sides of the module. Figure 2a shows the configuration of the proposed converter where modified modules are used. Owing to the modified module (see Figure 2b), a number of capacitors are combined with power semiconductors to form a multi-stage switched-capacitor network. Special charging and discharging algorithms have to be considered to achieve multilevel output voltage through special arrangement of switches and capacitors. The main difference between the proposed topology and that shown in Figure 1 is the contribution of all the capacitors in multilevel voltage generation as well as charging the capacitors to multiples of *Vin*. As shown in Figure 2, S'_1 and S'_2 can be selected as unidirectional (two-quadrant switches that are shown in circle or square inclusion depending on the requirement for controlling current flow from one side) or bidirectional (four-quadrant switches that are shown in rectangular inclusion) switches.

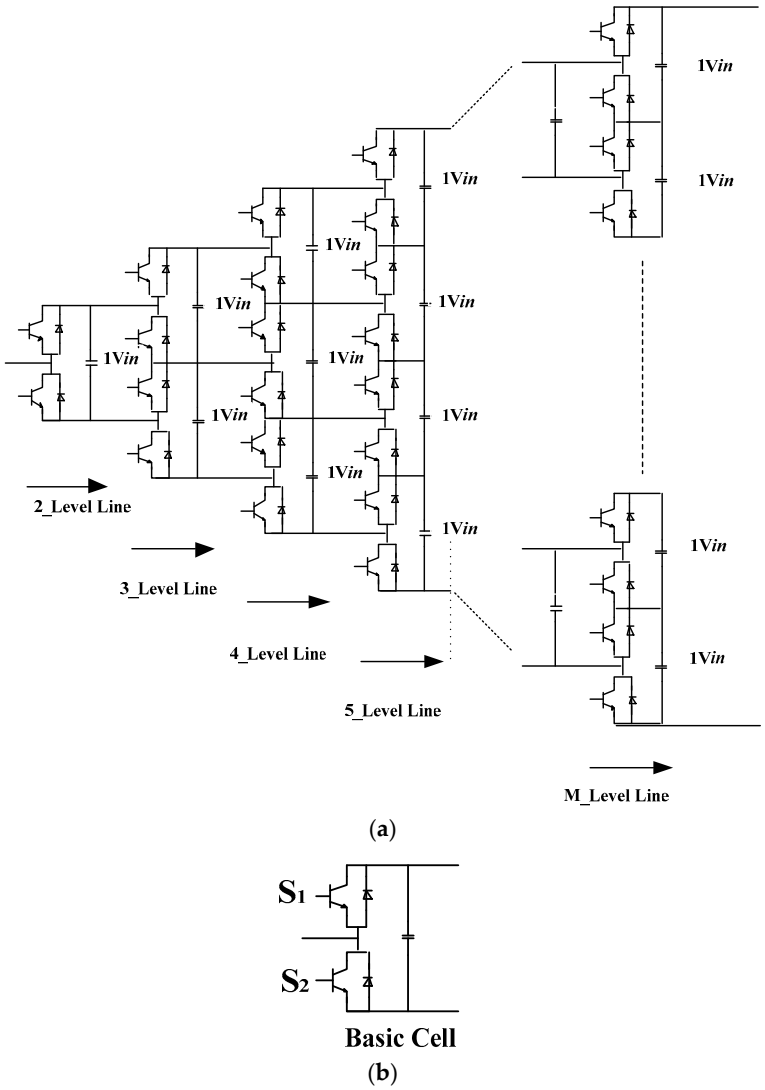


Figure 1. (**a**) Presented topology of [20] (**b**) its basic cell.

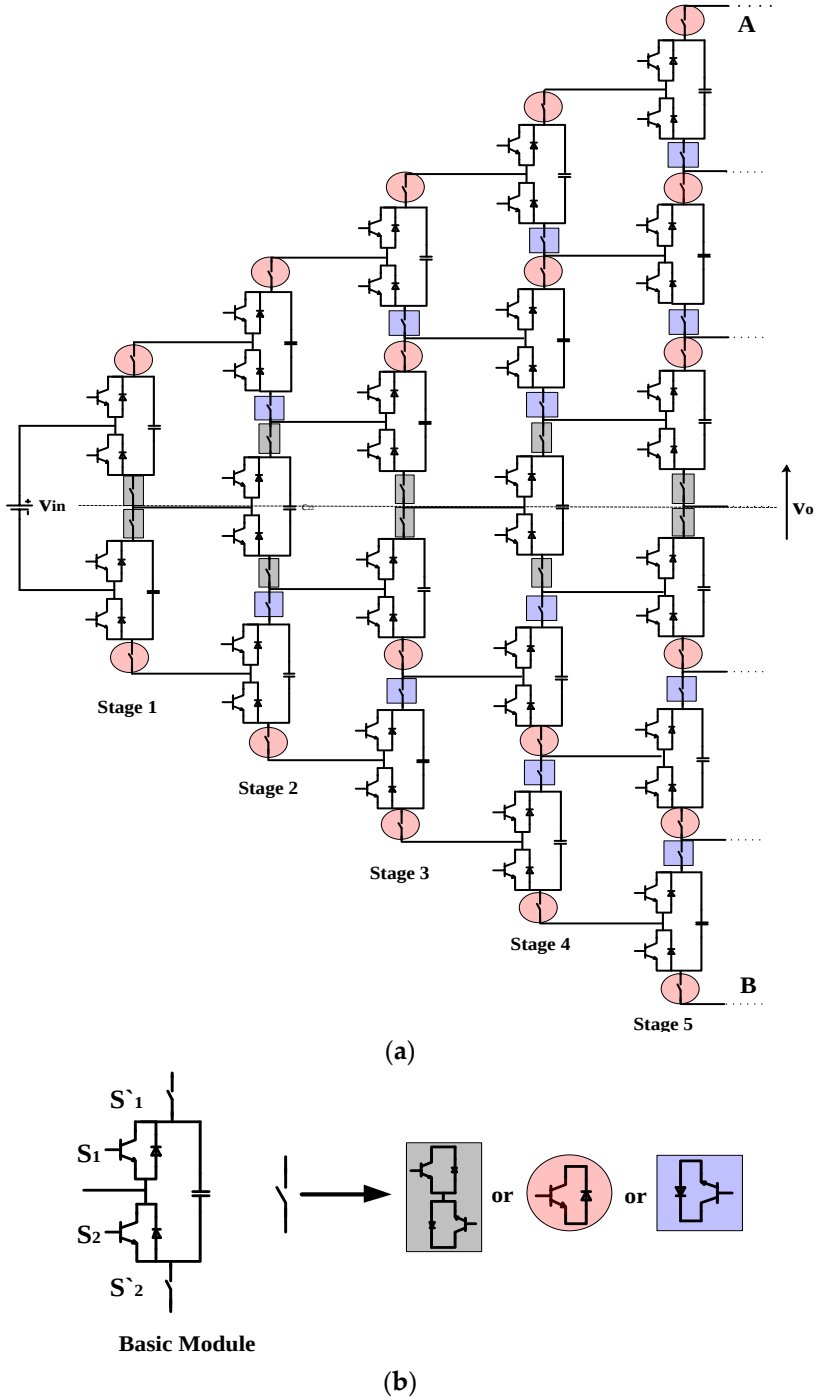


Figure 2. Proposed topology (**a**) Switched-capacitor structure, (**b**) Its building block modules.

3. Operating Principle of the Proposed Topology

Figure 3 shows a three-stage proposed converter where 9 modules and 42 switches (38 for SCMLI and 4 for H-bridge) are used. Note that the modules of the last stage can be simplified, and some of the switches can be eliminated. S_{mn} is nth switch of m^{th} module and C_{Mi} is the capacitor of i^{th} module. A Switching state of (S_{M1}, S_{M2}, ... , S_{M9}) can be defined for this converter where S_{Mi} (i = 1, 2, ... , 9) is the switching state for each module.

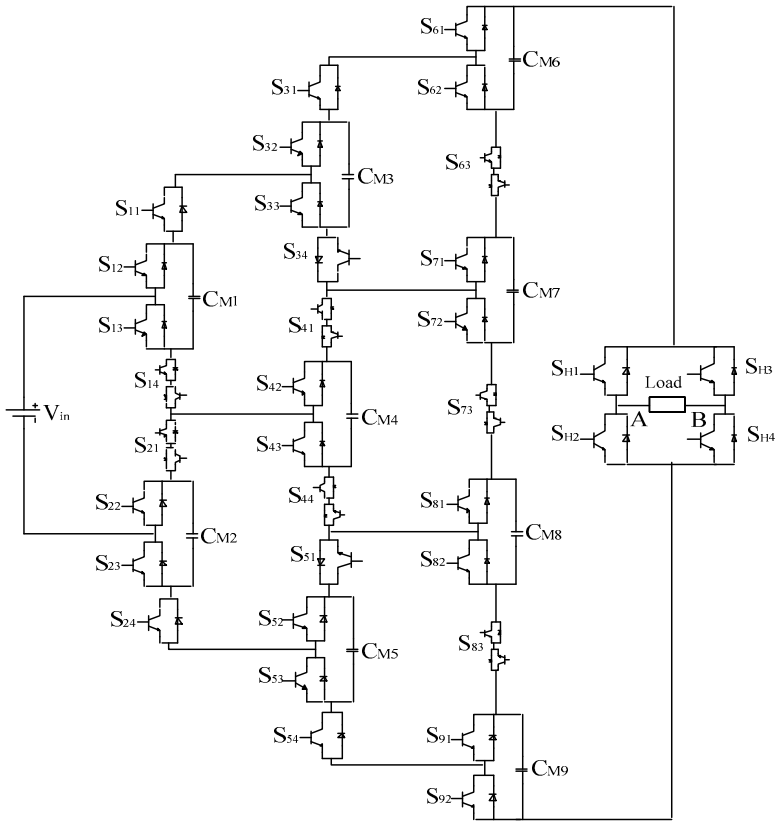


Figure 3. Diagram of a three-stage proposed inverter.

4. Asymmetrical Charging of the Capacitors

As mentioned, the main concept of this inverter is to charge the capacitors to multiples of the input voltage through switches. Figure 4 shows charging some states of different capacitors. As shown in Figure 4a, V_{CM1} reaches to V_{in} through the switches of modules 1 and 2. Voltage of C_{M3} reaches to $3V_{in}$ via C_{M1}, C_{M2} and input DC source (see Figure 4b). C_{M6} and C_{M9} charges to $3V_{in}$ in parallel with C_{M3} and C_{M5} respectively (see Figure 4c). C_{M8} is charged to $14V_{in}$ via specified paths, which are shown in Figure 4d.

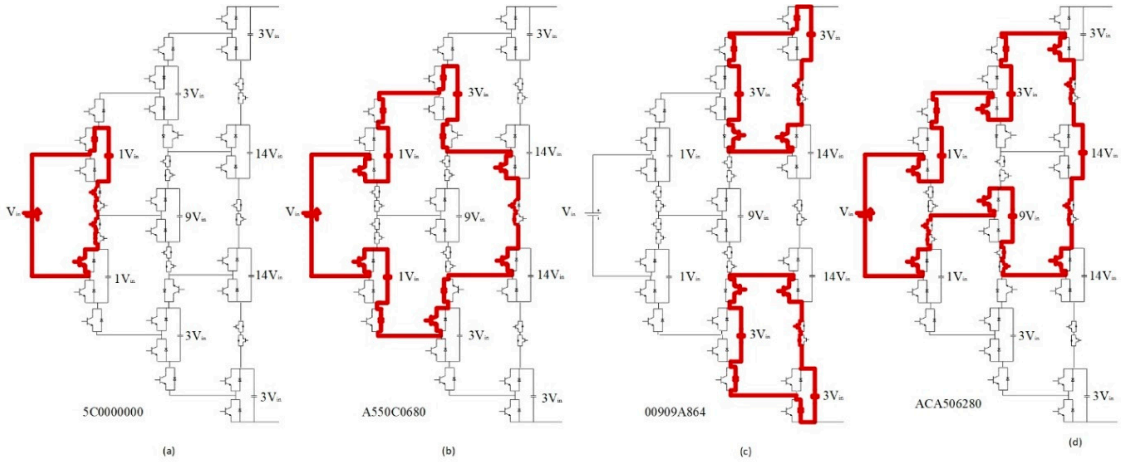


Figure 4. Charging states of different capacitors.

Some selected capacitor charging paths are indicated in Figure 4. According to this figure, by modeling each path, the equation of each capacitor voltage during charging can be achieved. The same

scenario can be carried out for discharging paths to find equations of capacitors voltages during discharging intervals.

Figure 5 shows the model of charging circuit for C_{M1}. In this model, the following non-idealities are considered for diodes, switches and capacitors:

V_{Dij}: Diode on-state voltage of ith module and jth diode
R_{Dij}: Diode on-state resistant of ith module and jth diode
r_{cn}: ESR of nth capacitor
V_{Sij}: Switch on-state voltage of ith module and jth switch
R_{Sij}: R_{Dij}: Switch on-state resistant of ith module and jth switch

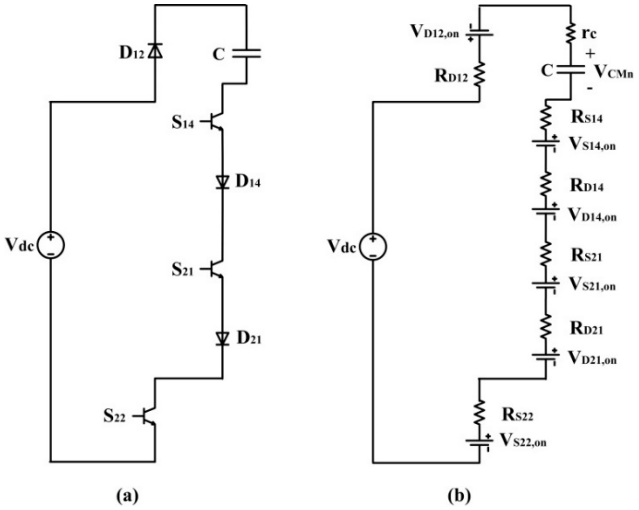


Figure 5. Charging path of C_{M1} (**a**) Real circuit, (**b**) its non-idealises model.

In the case of calculating capacitor voltage, there is a basic equation which compromised both power switches and diode voltage, which for the nth module during charge can be calculated as:

$$V_{C_{Mn}}^{ch}(t) = (V_{in_{Mn}} - (kV_{SW,on} + mV_{D,on}))(1 - e^{-\frac{t}{\tau_{C_{Mn}}}}) \quad (1)$$

There are different switches and diodes in each charging and discharging states and in the above equation, k and m are the number of switches and diodes in the charging paths respectively. C_{Mn}, $V_{dc_{Mn}}$ and $\tau_{C_{Mn}}$ are capacitance value, input voltage and time constant of nth module. Time constant of C_{Mn} during charging can be calculated: (note that, on-resistance of the switches and diodes are considered as the same.)

$$\tau_{C_{Mn}} = (kR_{sw} + mR_D + r_{cn}) \cdot C_{Mn} \quad (2)$$

According to different modules in the proposed asymmetric multilevel inverter (see Figure 4) the input voltage of module 1 is $V_{dc} - (3V_{sw,on} + 3V_{D,on})$ and its time constant is $(3R_{sw} + 3R_D + r_c) \cdot C_{M1}$. Therefore, $V_{C_{M1}}$ can be shown as:

$$V_{C_{M1}}(t) = (V_{dc} - (3V_{SW,on} + 3V_{D,on}))(1 - e^{-\frac{t}{(3R_{sw} + 3R_D + r_c) \cdot C_{M1}}}) \quad (3)$$

The same procedure has to be carried out to calculate all of the capacitor voltages during charging. Table 1 shows different parameters for the calculation of all other capacitor voltages based on Equation (1), which also illustrates the number of switches and diodes in each path.

Table 1. Different parameters for different capacitors.

n	$V_{in_{Mn}}$	k	m
2	V_{dc}	3	3
3	$V_{dc} + V_{C_{M1}}(t) + V_{C_{M2}}(t)$	6	6
4	$V_{dc} + V_{C_{M1}}(t) + V_{C_{M2}}(t) + V_{C_{M3}}(t) + V_{C_{M5}}(t)$	12	8
5	$V_{dc} + V_{C_{M1}}(t) + V_{C_{M2}}(t)$	6	6
6	$V_{C_{M3}}(t)$	3	3
7	$V_{dc} + V_{C_{M1}}(t) + V_{C_{M3}}(t) + V_{C_{M4}}(t)$	10	6
8	$V_{dc} + V_{C_{M2}}(t) + V_{C_{M4}}(t) + V_{C_{M5}}(t)$	10	6
9	$V_{C_{M5}}(t)$	3	3

5. Multilevel Output Voltage Generation

Output voltage generation is carried out according to Table 2, i.e., the information provided about specific voltage generation for each module related to their possible switching states. To achieve a self-balanced system, charging and discharging states for the capacitors of each module should be available by switching pattern. To generate different levels, the ability of modules to keep the voltage within an acceptable range has to be analyzed. Therefore, Table 2 shows possible switching states for each module to generate mentioned output voltages. For each module, capacitor voltage is shown for the available switching states along with its charging or discharging mode. Note that "×" implies that mentioned switching state is not used at that specific module. Charging, discharging and no change mode of the module are shown with "▲", "▼" and "–" respectively.

Having redundant states is an important issue in the generation of output voltage levels for multilevel inverters. According to Table 2, various alternatives are available for each module, which can be selected in order to balance the capacitors voltages. For instance, Module 1 is charged by switching state 5 and will be discharged by A, B and 9. States 0, 3 and C bypass C_{M1}. State D also will charge this capacitor via input DC source. As shown in this table, whether the application of some switching states may lead to charging or discharging the capacitor depends on the switching state of the previous module.

With the same procedure as that used in the previous part, the voltage of each capacitor during discharging intervals can be calculated as:

$$V_{C_{Mn}}^{Disch}(t) = (V_{C_{Mn}}^{p}(t) - (kV_{SW,on} + mV_{D,on}))(e^{-\frac{t}{\tau_{C_{Mn}}}}) \quad (4)$$

where, $V_{C_{Mn}}^{Disch}(t)$ is the discharge voltage of C_{Mn} and $V_{C_{Mn}}^{p}(t)$ is the initial voltage of the capacitor before discharging. Other parameters (m and k) are the same as Table 1.

Choosing a proper switching pattern is the main challenge of this converter. Discharging the combination of capacitors across the load (to form different levels of output AC voltage) may lead to decrements in capacitor voltages. Therefore, to avoid capacitors voltage imbalance, switching states have to be used which are able to charge one or more capacitors during discharging time of other capacitors. This means that the charging time of all the capacitors should be distributed in the discharging intervals.

Table 3 shows the different switching states of the proposed converter to generate different levels. Note that proposed converter has hundreds of switching states, but only the switching states are mentioned in this table, which is crucial for capacitor voltage balancing. As shown in this table, at least one capacitor has the chance to be charged during the discharging of other capacitors (except $39V_{in}$, $41V_{in}$, $42V_{in}$ and $45V_{in}$). Figure 6 shows the paths of charging and discharging for the four selected switching states.

Table 2. possible switching states for each module and voltage state of each capacitor (Charge: ▲, Discharge: ▼, No Change: -).

	V_{CM1}	V_{CM2}	V_{CM3}	V_{CM4}	V_{CM5}	V_{CM6}	V_{CM7}	V_{CM8}	V_{CM9}
0(0000)	0 (-)	0 (-)	0 (-)	0 (-)	0 (-)	0 (-)	0 (-)	0 (-)	$3V_{in}$ (▼)
2(0010)	×	×	×	×	×	$3V_{in}$ (▼)	$14V_{in}$(▼,▲)	$14V_{in}$ (▼,▲)	×
3 (0011)	0 (-)	0 (-)	0 (-)	0 (-)	0 (-)	×	×	×	×
4(0100)	×	×	×	×	×	$3V_{in}$ (▼)	$14V_{in}$ (▼)	$14V_{in}$ (▼)	0 (-, ▲)
5(0101)	$-1V_{in}$ (▲)	$1V_{in}$ (▼)	$-3V_{in}$ (▲)	$9V_{in}$ (▼) $-9V_{in}$ (▼)	$3V_{in}$ (▼)	×	×	×	×
6(0110)	×	×	×	×	×	0 (-)	0 (-)	0 (-)	_
8(1000)	×	×	×	×	×	0 (-)	0 (-)	0 (-)	$3V_{in}$(▼)
9(1001)	$1V_{in}$(▼)	$1V_{in}$(▼)	$3V_{in}$(▼)	$9V_{in}$ (▲▼) $-9V_{in}$(▼)	$3V_{in}$(▼)	×	×	×	×
A(1010)	$1V_{in}$(▼)	$-1V_{in}$(▲)	$3V_{in}$(▼)	$9V_{in}$ (▼) $-9V_{in}$ (▼)	$-3V_{in}$ (▲)	$3V_{in}$ (▲)	$14V_{in}$ (▼)	$14V_{in}$ (▼)	×
B(1011)	$1V_{in}$ (▼)	$1V_{in}$ (▲)	$3V_{in}$ (▼)	×	$3V_{in}$ (▲)	×	×	×	×
C(1100)	0 (-)	0 (-)	0 (-)	×	0 (-)	×	×	×	×
D(1101)	$1V_{in}$ (▲)	$1V_{in}$ (▼)	$3V_{in}$ (▲)	×	$3V_{in}$ (▼)	×	×	×	

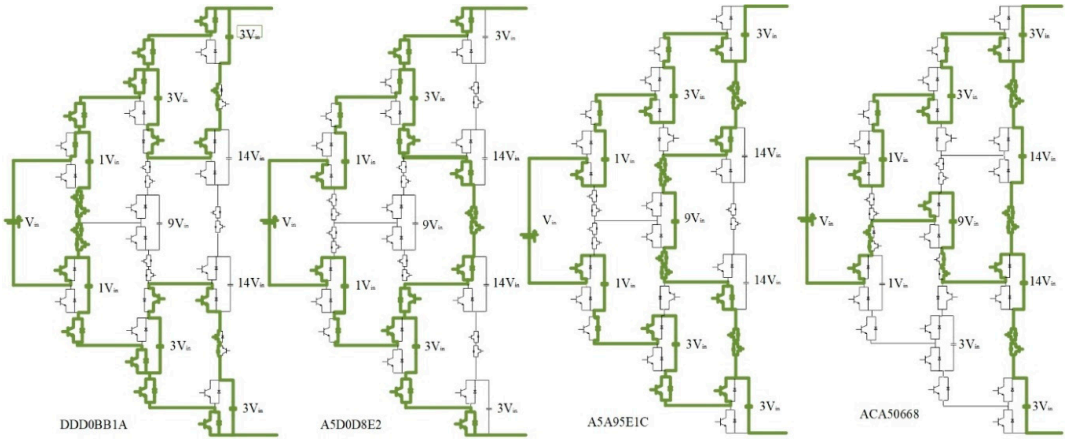


Figure 6. charging and discharging paths for selected switching states.

Table 3. Different switching states of proposed converter.

Level	Switching States (C_{M1}, C_{M2}, C_{M3}, C_{M4}, C_{M5}, C_{M6}, C_{M7}, C_{M8}, C_{M9})
$0V_{IN}$	5C0000000(↑− − − − − − − −) 3A0000000(−↑− − − − − − −) A550C0680(↓↓↑− − − − − −) A530A0680(↓↓− −↑− − − −) A5A956868 (↓↓↓↑↓− − − −) 00909A864(− −↓−↓↑− −↑) ACA506280(↓−↓↓− −↑− −) 350A50628(−↓−↓↓− −↑ −)
$1V_{IN}$	C3D0BA864(− −↓−↓↑− −↑)
$2V_{IN}$	BBD0BA864(↓↑↓−↓↑− −↑) DDD0BA864(↑↓↓−↓↑− −↑)
$3V_{IN}$	A5D0BA864(↓↓↓−↓↑− −↑)
$4V_{IN}$	5D9CBA864(↑↓↓−↓↑− −↑) 3B9CBA864(↓↑↓−↓↑− −↑) BAD39A864(↓↑↓−↓↑− −↑) DCD39A864(↑↓↓−↓↑− −↑)
$5V_{IN}$	BBB0BA864(↓↑↓−↓↑− −↑) DDB0BA864(↑↓↓−↓↑− −↑) BBD0DA864(↓↑↓−↓↑− −↑ DDD0DA864(↑↓↓−↓↑− −↑)
$6V_{IN}$	A5D0D8684(↓↓↑−↓− − − −) A5B0B8684(↓↓↓−↑− − − −) 5C9098684(↑−↓−↓− − − −) 3A9098684(−↑↓−↓− − − −) A5B0BA864(↓↓↓−↓↑− −↑) A5D0DA864(↓↓↓−↓↑− −↑)

Table 3. *Cont.*

Level	Switching States (C_{M1}, C_{M2}, C_{M3}, C_{M4}, C_{M5}, C_{M6}, C_{M7}, C_{M8}, C_{M9})
$7V_{IN}$	BAD39A804(↓↑↓−↓↑− −↑) DCD39A804(↑↓↓−↓↑− −↑) 5D9CDA864(↑↓↓−↓↑− −↑) 3B9CDA864(↓↑↓−↓↑− −↑)
$8V_{IN}$	DDB0DA864(↑↓↓−↓↑− −↑) BBB0DA864(↓↑↓−↓↑− −↑)
$9V_{IN}$	A5B0DA864(↓↓↓−↓↑− −↑) A5B0B8688(↓↓↓−↑− − −↓) A5D0D8688(↓↓↑−↓− − −↓) 5C9094684(↑−↓−↓↓− − −)3A9094684(−↑↓−↓↓− − −)
$10V_{IN}$	BAB39A808(↓↑↓−↓↑− −) DCB39A808(↑↓↓−↓↑− −↓) 5D9CD4064(↑↓↓−↓↓− −↑) 3B9CD4064(↓↑↓−↓↓− −↑)
$11V_{IN}$	DDA0D4064(↑↓↓−↓↓− −↑) BBA0D4064(↓↑↓−↓↓− −↑) DDB05A808(↑↓↓−↓↑− −↓) BBB05A808(↓↑↓−↓↑− −↓)
$12V_{IN}$	5C9094688(↑−↓−↓↓− −↓) 3A9094688(−↑↓−↓↓− −↓) A5D0D4688(↓↓↑−↓↓− −↓) A5B0B4688(↓↓↓−↑↓− −↓) A5B05A808(↓↓↓−↓↑− −↓) A5A0D4064(↓↓↓−↓↓− −↑)
$13V_{IN}$	5D9ABA864(↑↓↓↓↑− −↑) 3B9ABAA864(↓↑↓↓↑− −↑) BAD59A864(↓↑↓↓↑− −↑) DCD59A864(↑↓↓↓↑− −↑)
$14V_{IN}$	359ABA864(−↓↓↓↑− −↑) ACD59A864(↓−↓↓↑− −↑)
$15V_{IN}$	A5A956868(↓↓↓↑↓↓− −↓) 5C999A864(↑−↓↓↑− −↑) 3A999A864(−↑↓↓↑− −↑)
$16V_{IN}$	5D9ADA864(↑↓↓↓↑− −↑) BAB59A864(↓↑↓↓↑− −↑)
$17V_{IN}$	359ADA864(−↓↓↓↑− −↑)
$18V_{IN}$	5C999A808(↑−↓↓↑− −↓) 5C9994064(↑−↓↓↓− −↑) 3A999A808(−↑↓↓↑− −↓) 3A9994064(−↑↓↓↓− −↑)
$19V_{IN}$	DD30B2464(↑↓− −↓↓−↑) DDD0CA8A0(↑↓↓− −↑−↓↓) BB30B2464(↓↑− −↓↓−↑) BBD0CA8A0(↓↑↓− −↑−↓↓)
$20V_{IN}$	ACA596284(↓−↓↓↓↑− −) A550D2684(↓↓↑−↓↓↓− −) 359A58628(−↓↓↓− −↑↓) A530B2684(↓↓− −↑↓↓− −) 5C9008620(↑−↓− − − −↓↓) 3A9008620(−↑↓− − − −↓↓)
$21V_{IN}$	5C9994008(↑−↓↓↓− −↓) 3A9994008(−↑↓↓↓− −↓)
$22V_{IN}$	DD30D2464(↑↓− −↓↓−↑) BB30D2464(↓↑− −↓↓−↑) DDD0CA8A0(↑↓↓− −↑−↓↓) BBD0CA8A0(↓↑↓− −↑−↓↓)
$23V_{IN}$	ACA596288(↓−↓↓↓↑−↓) 359A54628(−↓↓↓↓−↑↓) A5D0C46A0(↓↓↑− −↓−↓↓) A550D2688(↓↓↑−↓↓↓−↓) A5B0A46A0(↓↓↓−↑↓−↓↓) A530B2688(↓↓− −↑↓↓−↓)
$24V_{IN}$	5D0C52408(↑↓− −↓↓↓−↓) 3B0C52408(↓↑− −↓↓↓−↓) BAA3040A0(↓↑↓− −↓−↓↓) DCA3040A0(↑↓↓− −↓−↓↓)
$25V_{IN}$	DD3052408(↑↓− −↓↓↓−↓) BB3052408(↓↑− −↓↓↓−↓) DDA0C40A0(↑↓↓− −↓−↓↓) BBA0C40A0(↓↑↓− −↓−↓↓)
$26V_{IN}$	5C9094A88(↑−↓−↓↓↓−↓) 3A9094A88(−↑↓−↓↓↓−↓) 5C9094648(↑−↓−↓↓−↓↓) 3A9094648(−↑↓−↓↓−↓↓)
$27V_{IN}$	5D0AB2464(↑↓−↓↓↓↓−↑) BAD50A8A0(↓↑↓↓−↑−↓↓)
$28V_{IN}$	ACD50A8A0(↓−↓↓−↑−↓↓) 350AB2464(−↓−↓↓↓↓−↑)
$29V_{IN}$	5C0992404(↑− −↓↓↓↓− −) 3A0992404(−↑−↓↓↓↓− −) 5C99080A0(↑−↓↓− − −↓↓) 3A99080A0(−↑↓↓− − −↓↓)
$30V_{IN}$	5D0AD2464(↑↓−↓↓↓↓−↑) 3B0AD2464(−↑−↓↓↓↓−↑)
$31V_{IN}$	350AD2464(−↓−↓↓↓↓−↑) ACD50A8A0(↓−↓↓−↑−↓↓)
$32V_{IN}$	5C0992408(↑−−↓↓↓↓−↓) 3A0992408(−↑−↓↓↓↓−↓) 5C99040A0(↑−↓↓−↓−↓↓) 3A99040A0(−↑↓↓−↓−↓↓)
$33V_{IN}$	35933AA44(−↓↓− −↑↓↓−) ACCC98A64(↓− − −↓−↓↓↑) 5D0A52408(↑↓−↓↓↓↓−↓) BAA5040A0(↓↑↓↓−↓−↓↓)
$34V_{IN}$	ACA5062A0(↓−↓↓−↓↑↓↓) 350A52628(−↓−↓↓↓↓↑↓) A550C26A0(↓↓↑− −↓↓↓↓) A530A26A0(↓↓− −↑↓↓↓↓) 5C0002220(↑− − − −↓↓↓↓) 3A0002220(−↑ − − −↓↓↓↓)

Table 3. *Cont.*

Level	Switching States (C_{M1}, C_{M2}, C_{M3}, C_{M4}, C_{M5}, C_{M6}, C_{M7}, C_{M8}, C_{M9})
$35V_{IN}$	5D933AA48(↑↓↓− −↑↓↓↓) BACC94A64(↓↑− −↓↓↓↓↑)
$36V_{IN}$	35933AA48(−↓↓− −↑↓↓↓) ACCC94A64(↓− − −↓↓↓↓↑) DD30C24A0(↑↓− − −↓↓↓↓) BB30C24A0(↓↑− − −↓↓↓↓)
$37V_{IN}$	5C9094A64(↑−↓−↓↓↓↓↑) 3A9094A64(−↑↓−↓↓↓↓↑)
$38V_{IN}$	BBCC94A48(↓↑− −↓↓↓↓↓) 5D9334A48(↑↓↓− −↓↓↓↓)
$39V_{IN}$	ACCC94A48(↓− − −↓↓↓↓↓)
$40V_{IN}$	5C9094A48(↑−↓−↓↓↓↓↓) 3A9094A48(−↑↓−↓↓↓↓↓)
$41V_{IN}$	099352248(−↓↓−↓↓↓↓↓)
$42V_{IN}$	359352248(−↓↓−↓↓↓↓↓)
$43V_{IN}$	5C09024A0(↑− −↓−↓↓↓↓) 3A09024A0(−↑−↓−↓↓↓↓)
$44V_{IN}$	5D0AC24A0(↑↓−↓−↓↓↓↓) BA35024A0(↓↑−↓−↓↓↓↓)
$45V_{IN}$	AC35024A0(↓− −↓−↓↓↓↓)

6. Capacitor Calculation for Self-Balancing Purpose

Generally, the maximum discharge amount of each capacitor C_{Mn} during the longest discharging period $[t_1, t_2]$ can be calculated as [25]:

$$Q_{C_{Mn}} = \int_{t_1}^{t_2} I_{out} \sin(2\pi f_s t - \phi) dt \tag{5}$$

where f_s is fundamental frequency, I_{out} is the amplitude of output current and ϕ is the phase difference between output current and voltage [19]. Considering Q_{M1} and Q_{M2} less than 10% maximum charge of C_{M1} and C_{M2} respectively, these capacitors can be achieved as:

$$C_{M1} > \frac{Q_{c_{M1}}}{0.1\, V_{in}} \tag{6}$$

$$C_{M2} > \frac{Q_{c_{M2}}}{0.1\, V_{in}} \tag{7}$$

As C_{M3} and C_{M5} are charged via DC source and series combination of C_{M1} and C_{M2}, $V_{C_{M3}}$ and $V_{C_{M5}}$ are as follows:

$$V_{C_{M3}} = V_{in} + \frac{\frac{C_{M1} \cdot C_{M2}}{C_{M1} + C_{M2}}}{\frac{C_{M1} \cdot C_{M2}}{C_{M1} + C_{M2}} + C_{M3}} \times \left(V_{C_{M1}} + V_{C_{M2}}\right) \tag{8}$$

$$V_{C_{M5}} = V_{in} + \frac{\frac{C_{M1} \cdot C_{M2}}{C_{M1} + C_{M2}}}{\frac{C_{M1} \cdot C_{M2}}{C_{M1} + C_{M2}} + C_{M5}} \times \left(V_{C_{M1}} + V_{C_{M2}}\right) \tag{9}$$

Therefore, C_{M3} and C_{M5} are obtained as:

$$C_{M3} = \frac{\left[\left(\frac{C_{M1} \cdot C_{M2}}{C_{M1} + C_{M2}}\right) \times \left(V_{C_{M1}} + V_{C_{M2}}\right)\right] + V_{in}}{V_{C_{M3}}} - \left(\frac{C_{M1} \cdot C_{M2}}{C_{M1} + C_{M2}}\right) \tag{10}$$

$$C_{M5} = \frac{\left[\left(\frac{C_{M1} \cdot C_{M2}}{C_{M1} + C_{M2}}\right) \times \left(V_{C_{M1}} + V_{C_{M2}}\right)\right] + V_{in}}{V_{C_{M5}}} - \left(\frac{C_{M1} \cdot C_{M2}}{C_{M1} + C_{M2}}\right) \tag{11}$$

With the same procedure, other capacitors and their voltages can be calculated as:

$$V_{C_{M4}} = V_{in} + \left(\frac{\left(\frac{1}{C_{M1}} + \frac{1}{C_{M2}} + \frac{1}{C_{M3}} + \frac{1}{C_{M5}}\right)}{\left(\frac{1}{C_{M1}} + \frac{1}{C_{M2}} + \frac{1}{C_{M3}} + \frac{1}{C_{M5}}\right) + C_{M4}} \right) \times \left(V_{C_{M1}} + V_{C_{M2}} + V_{C_{M3}} + V_{C_{M5}}\right) \quad (12)$$

$$V_{C_{M6}} = \frac{C_{M3}}{C_{M3} + C_{M6}} \times \left(V_{C_{M3}}\right) \quad (13)$$

$$C_{M6} = \frac{\left(C_{M3} \times V_{C_{M3}}\right) + V_{in}}{V_{C_{M6}}} - C_{M3} \quad (14)$$

$$V_{C_{M9}} = \frac{C_{M5}}{C_{M5} + C_{M9}} \times \left(V_{C_{M5}}\right) \quad (15)$$

$$C_{M9} = \frac{\left(C_{M5} \times V_{C_{M5}}\right) + V_{in}}{V_{C_{M9}}} - C_{M5} \quad (16)$$

$$V_{C_{M7}} = V_{in} + \left(\frac{\left(\frac{1}{C_{M1}} + \frac{1}{C_{M3}} + \frac{1}{C_{M4}}\right)}{\left(\frac{1}{C_{M1}} + \frac{1}{C_{M3}} + \frac{1}{C_{M4}}\right) + C_{M7}} \right) \times \left(V_{C_{M1}} + V_{C_{M3}} + V_{C_{M4}}\right) \quad (17)$$

7. Modulation Strategy and Switching States Selection

This is an important factor in capacitor voltage balancing due to the definition of charging and discharging intervals which are required for voltage calculations for capacitors. In this study, a predetermined offline PWM strategy was considered to define the switching angles (the angles in which the levels change). Figure 7a shows a sampled staircase multilevel voltage waveform and a reference voltage in a Nearest Level Control (NLC) modulation technique. Figure 7b shows the schematic block diagram of this strategy. The nearest output voltage level V_n can be determined with [26]:

$$V_n = \frac{1}{V_c} round(V_{ref}) \quad (18)$$

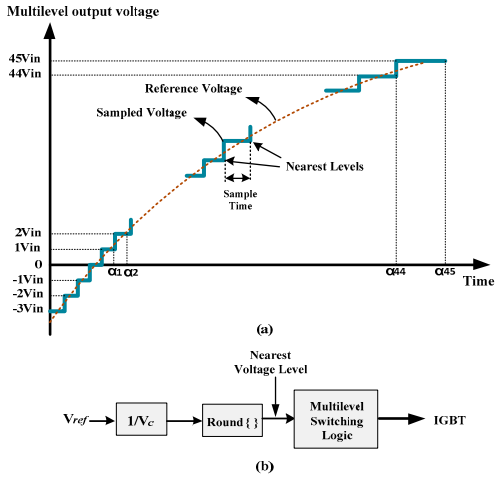


Figure 7. Nearest Level Control (**a**) Waveform synthesis, (**b**) Block diagram.

After determination of each voltage level and its time duration, a precise switching selection has to be carried out according to Table 3. The selection of one state for each level defines the charging or discharging states of each capacitor, which is an important task to keep the voltages within an acceptable range.

8. Comparison with Other Topologies

A comparative study is carried with other famous topologies which are presented at [13,15–19]. Table 4 shows the number of switching devices (Active switches, series diode), drivers for the switches and capacitors versus number of levels (N_L) and number of stages for the proposed inverter (n_{stage}). Note that, as shown in Figure 8, the relation between the number of stages and the number of levels in the proposed converter is:

$$n_{stage} = \begin{cases} 1 & 0 \le N_L \le 19 \\ 2 & 19 \le N_L \le 91 \\ 3 & 91 \le N_L \le 253 \end{cases} \quad (19)$$

Figure 8 presents the number of capacitors and semiconductors (active switches + series diodes) for 0 to 100 levels output. This comparison shows that the proposed converter provides better performance in terms of the number of components. As the converter is for low voltage input voltage sources, multiples of this low voltage amount are still within the acceptable standard range of components.

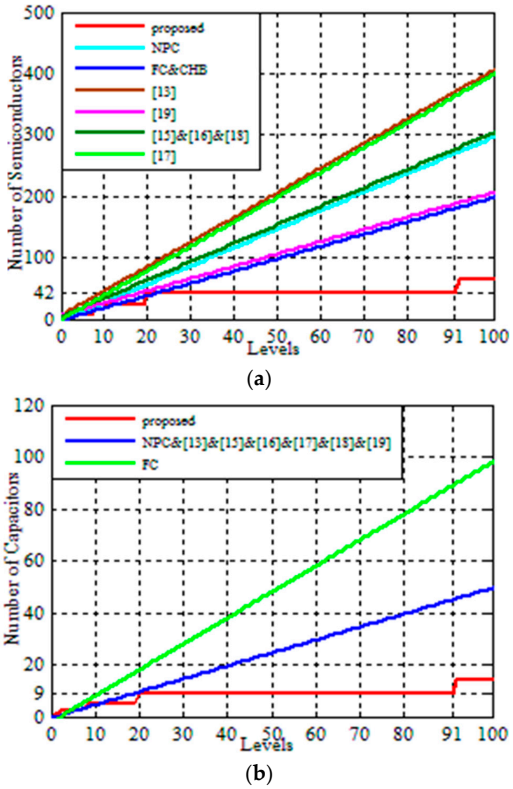


Figure 8. Comparison between proposed topology and others (**a**) number of semiconductors (active switches+ series diodes), (**b**) number of capacitors.

Table 4. Comparison of the proposed topology with conventional and advanced structures.

Topology	Number of Active Switches	Number of Series Diodes	Number of Drivers	Number of Capacitors	Balance Circuit
Proposed	$(2n_{stage}\cdot(n_{stage}+4))$	0	$(2n_{stage}\cdot(n_{stage}+3))+2$	$\frac{(n_{stage}+2)\cdot(n_{stage}+1)}{2}-1$	No Need
NPC	$2(N_L-1)$	N_L-1	$2(N_L-1)$	$(N_L-1)/2$	Need
FC	$2(N_L-1)$	0	$2(N_L-1)$	(N_L-2)	Need
CHB	$2(N_L-1)$	0	$2(N_L-1)$	$(N_L-1)/2$	Need
[13]	$2(N_L+1)+4$	$2N_L$	$2N_L+6$	$(N_L-1)/2$	No Need
[15]	$3N_L+4$	0	$3N_L+4$	$(N_L-1)/2$	No Need
[16]	$2N_L+4$	N_L	$2N_L+4$	$(N_L-1)/2$	No Need
[17]	$3N_L-1$	N_L	$3N_L-1$	$(N_L-1)/2$	No Need
[18]	N_L+5	$2N_L$	N_L+5	$(N_L-1)/2$	No Need
[19]	$2(N_L+1)+4$	0	$2(N_L+1)+4$	$(N_L/2)$	Need

9. The Simulation Results

A MATLAB simulation is conducted to achieve a 91-level output voltage with a maximum of 45 times of input DC voltage. The parameters given in Table 5 are used for the analysis.

Table 5. Simulation parameters.

Parameter	Value
Input Voltage	50 Volts
Number of Output Voltage levels	91
Output Frequency	50 Hz
C_{M1}, C_{M2}	20,000 μF
C_{M3}, C_{M5}	1000 μF
C_{M4}, C_{M6}, C_{M7}, C_{M8}, C_{M9}	100 μF
Resistive Load (R)	100 Ω
Inductive-Resistive Load (R-L)	100 Ω, 318.4 mH

Figure 9a,b show the output voltage and current at 50 Hz for two types of resistive and resistive-inductive loads. As shown in these figures, a high level staircase output voltage is achieved. Discharging currents of the last stage capacitors are shown in Figure 9c,d. The converter and its control strategy are able to balance capacitor voltages within acceptable ranges with considered tolerances (see Figure 10a–c). FFT analysis of the output voltage is shown in Figure 11, which indicates good performance of the proposed topology because of its low harmonic distortion.

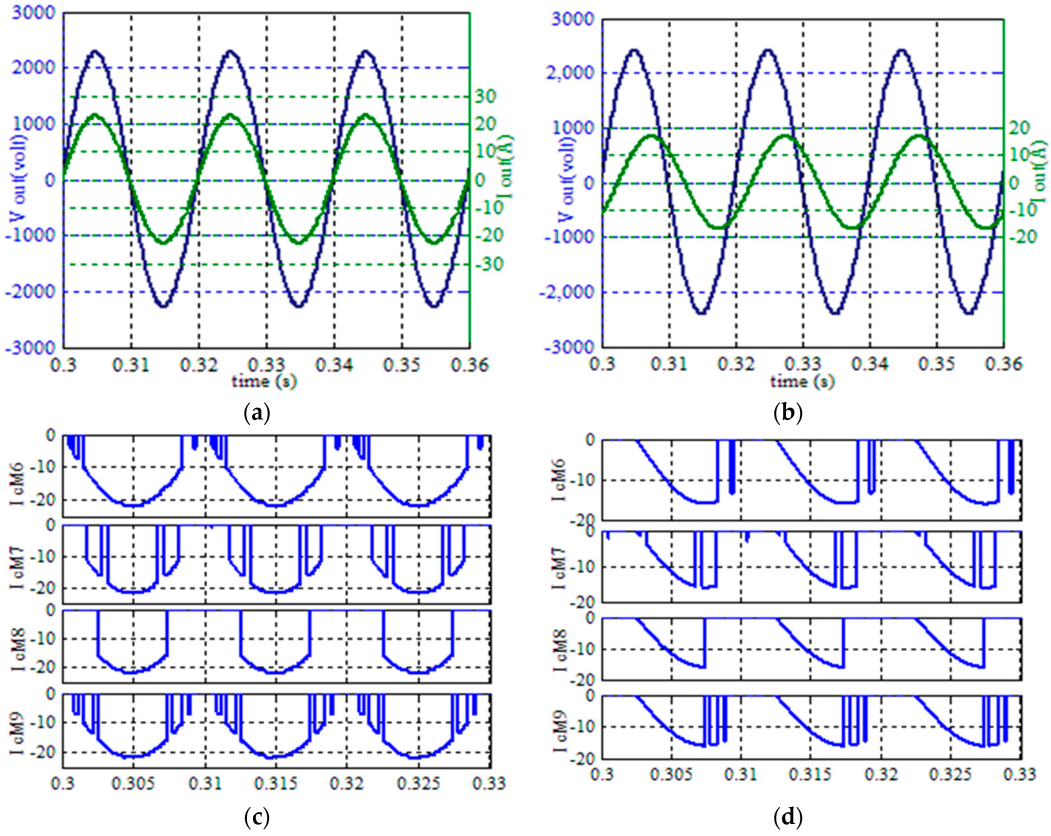


Figure 9. Simulation results (**a**) Output voltage and currents R load, (**b**) Output voltage and currents R-L load, (**c**) Discharging current of the last stage capacitors with R-load, (**d**) Discharging current of the last stage capacitors with R-L load.

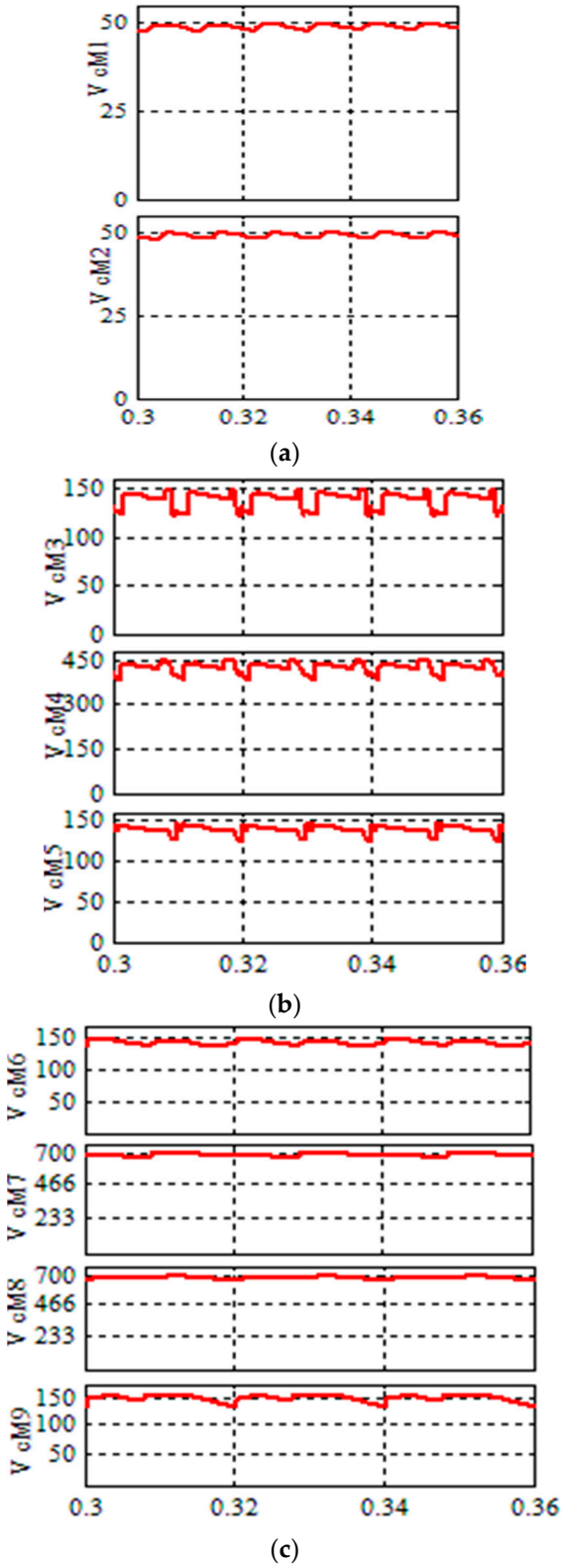


Figure 10. Capacitor's voltage in (**a**) first stage, (**b**) second stage, (**c**) third stage.

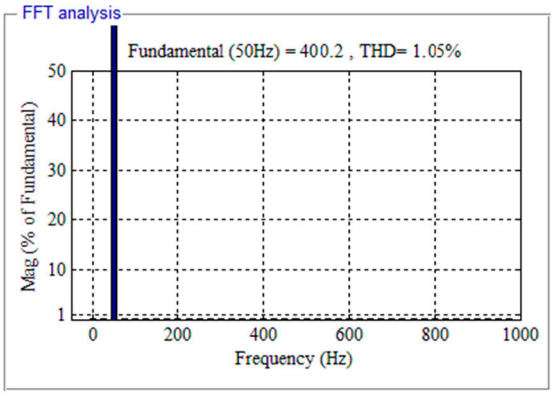


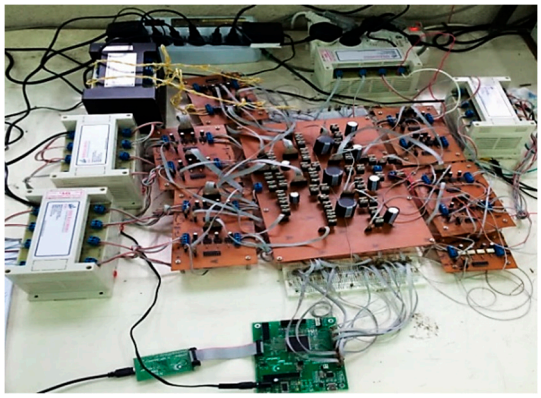
Figure 11. FFT analysis of output voltage.

10. Experimental Results

To validate our simulation and analysis, an experimental test setup was built with an input voltage of 10 volts, as shown in Figure 12a; other components are shown at Table 6. Figure 12b shows the output voltage and current for a pure inductive load, which confirms the application of the proposed structure and its mentioned control strategy under different operating conditions.

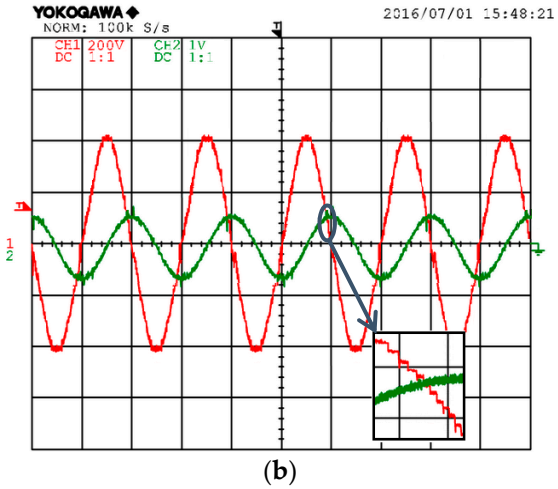
Table 6. Experimental Parameters.

Input Voltage	10 v
Number of Output Voltage levels	91
Output Frequency	50 HZ
C_{M1}, C_{M2}	20,000 µF
C_{M3}, C_{M5}	1000 µF
C_{M4}, C_{M6}, C_{M7}, C_{M8}, C_{M9}	100 µF
Load	570 Ω
Diode	MUR860
IGBT	12n60a4
Driver	HCPL 3120
Processor	DSP TMS320F28335



(**a**)

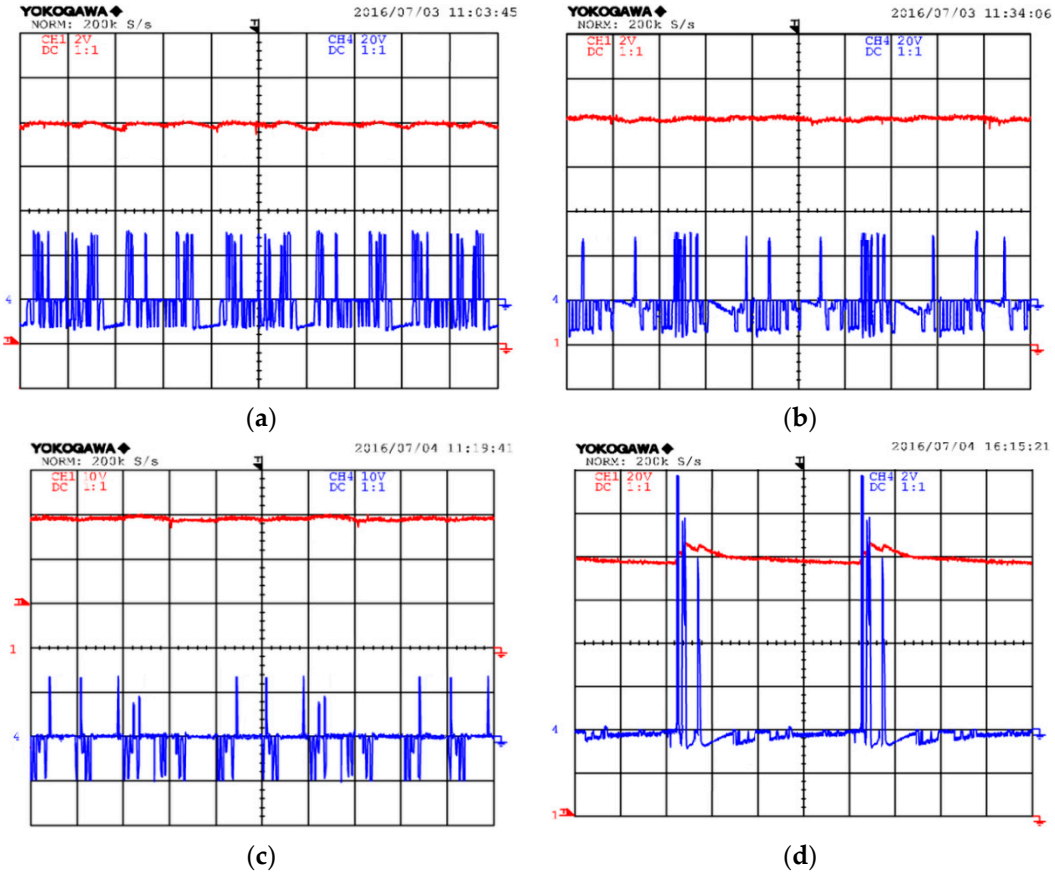
Figure 12. *Cont.*



(**b**)

Figure 12. Experimental results (**a**) Test set up (volt/div = 200 volts), (**b**) Output voltage and current in pure inductive load (Ampere/div = 1 amps) (time/div = 2500 µs).

Figure 13a–d shows the voltages and currents of selected capacitors (C_{M1}, C_{M2}, C_{M3}, C_{M7}) over a 2.5 ms period. It is clear that the number of charges and discharges for the capacitors in the first stage is much higher than that in last stages.



(**a**) (**b**)

(**c**) (**d**)

Figure 13. Voltage and current of capacitors (all channels time/div = 2500 µs) (**a**) C_{M1} (volt/div = 2 volts, Ampere/div = 20 amps), (**b**) C_{M2} (volt/div = 2 volts, Ampere/div = 20 amps), (**c**) C_{M3} (volt/div = 10 volts, Ampere/div = 10 amps), (**d**) C_{M7} (volt/div = 20 volts, Ampere/div = 2 amps).

11. Conclusions

An asymmetrical step-up multilevel inverter is presented in this paper with a single DC source. Bidirectional modules are designed in order to create different paths for the capacitors to be charged or discharged, based on a predetermined pattern. A comprehensive mathematical analysis is conducted to achieve capacitance values and the voltage of each capacitor during the different states. Investigation of a three-stage proposed converter showed that 45 levels can be achieved using different switching states. The application of a full bridge single phase inverter at the end of the proposed converter gives 91 voltage levels (45 positive, 45 negative and one zero level). According to a detailed comparison with other classical and state-of-the-art topologies, the number of different components was reduced to a great extent. A comprehensive simulation study and experimental results are presented to verify the analysis.

Author Contributions: All authors contributed equally to this work and all authors have read and approved the final manuscript.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

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