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High Efficiency Doherty Power Amplifier with Wide OPBO Range for Base Station Systems

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Abstract: A high-efficiency, S-band Doherty power amplifier with wide output power back-off (OPBO) range is presented. A novel parasitic capacitance compensation approach is applied at the output of Cree's GaN high electron mobility transistor (HEMT) to achieve high saturation efficiency in a wide output power back-off range. Specifically, a parallel shorting microstrip line between the transistor output and its match network is adopted to realize parasitic capacitance compensation. The measurement results indicate good Doherty behavior with 10 dB back off efficiency of 40.6-44.2% and saturation efficiency of 70.2-73.3% over 2.9-3.3 GHz. When stimulated by a 20-MHz LTE signal with 7.5 dB PAPR, the proposed Doherty amplifier power, combined with digital pre-distortion, achieved adjacent channel leakage ratios (ACLRs) below -47.2 dBc. The DPA demonstrate superior performance in OPBO range and efficiency, which makes it an ideal component for base station communication systems.

1. Introduction

The Doherty power amplifiers (DPAs) are widely regarded as an effective structure to achieve high efficiency in the output power back-off (OPBO) condition [1], and therefore have been widely used in base station communication systems. However, with the rapid development of communication technology, there is an increasing demand for high efficiency and wide OPBO range. Some high efficiency DPAs have been reported in literatures [1-3], but their OPBO range is relatively small; others featured wide OPBO range but relatively low saturation efficiencies [4-5]. Achieving high efficiency and wide OPBO range simultaneously is a significant challenge for DPA designs.

In recent years, DPAs based on GaN high electron mobility transistors (HEMTs) have attracted great attention. This is largely due to their outstanding material properties, such as its high cutoff frequency and high power density, especially the excellent trade-off between output power and efficiency. However, the presence of parasitic effect, especially the parasitic capacitance at the output of GaN HEMT, has been a major issue limiting the performance of DPAs' drain efficiency and OPBO range. Therefore, it is of great importance to suppress the parasitic effect in DPA circuit designs.

In this paper, a DPA based on CGH40010 GaN HEMTs is presented. A parallel shorted micro-strip line is applied between the transistor output and the output match network to realize parasitic capacitance compensation and consequently a high saturation efficiency in a wide OPBO range at a higher frequency. Details of DPA design, simulation and measurement results are presented in this paper.

2. Device modeling and circuit design

A conventional DPA consists of two power amplifiers (PAs), the carrier PA biased for class-AB operation and the peaking PA biased for class-C operation [1]. The load modulation network dynamically modulates the effective load impedance of the carrier and the peak power amplifier based on the size of the input signal, and this principle allows the DPA to maintain high efficiency while the output power is backed off. DPA efficiency can be theoretically expressed as (1).

$$\text{Efficiency} = RF_{OUT}/RF_{DC} \times 100\% = V_{RF}I_{RF}/2(V_{DC_C}I_{DC_C} + V_{DC_P}I_{DC_P}) \times 100\% \quad (1)$$

In (1), $RF_{OUT}=1/2V_{RF}I_{RF}$ is the output power of DPA, which is also the sum of saturated output power. $V_{DC_C}I_{DC_C}$ and $V_{DC_P}I_{DC_P}$ are the direct-current power consumed by carrier and peaking amplifier, respectively. The OPBO range can be expressed as follows:

$$\text{OPBO} = 10\log[(1+\varphi)\tau]\ (dB) \quad (2)$$
$$\varphi = P_{SAT_P}/P_{SAT_C} \quad (3)$$
$$\tau = P_{SAT_C}/P_{BACK-OFF_C}. \quad (4)$$

P_{SAT_P} and P_{SAT_C} are the saturation output power of peaking and carrier amplifier, and $P_{BACK\text{-}OFF_C}$ is the output power of carrier amplifier at back-off stage. Theoretically, the efficiency at saturated stage is the same as that at OPBO stage, but the P_{SAT_P} is actually lower than P_{SAT_C} at the saturated stage. This is because the imperfect load modulation of DPA and the peaking amplifier cannot achieve a completely open state due to the low power input, which results in the leakage of P_{SAT_P} to ground via the transistor's internal parasitic capacitance, and RF_{OUT} is reduced correspondingly. In most cases, φ and $P_{BACK\text{-}OFF_C}$ are considered to be constant. Therefore, a decrease of P_{SAT_P} will lead to a power reduction of P_{SAT_C}, and thus a deterioration of τ. Consequently, OPBO range of the DPA is compressed.

Additionally, due to the decreasing of output power, the saturated efficiency is reduced. In conclusion, it is critical to suppress P_{SAT_P} and P_{SAT_C} leakage through the

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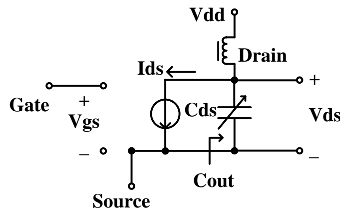

Fig. 1. Simplified transistor equivalent circuit model.

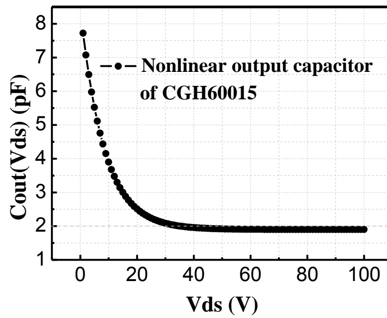

Fig. 2. Nonlinear Output capacitance versus Vds.

parasitic capacitance, so that the DPA's saturated efficiency and OPBO range can be improved.

2.1. Nonlinear output capacitor

Advanced Design system (ADS) is used to build large signal model of non-linear capacitor (CGH60015 in this paper), and the simulation is conducted using a bare-chip model to show the inherent operation of the saturated PA. Fig.1 shows a simplified equivalent circuit model of the GaN HEMT to analyse the parasitic capacitance effect. The transistor non-linear model consists of two elements: drain equivalent current source and nonlinear output capacitor C_{OUT}. In GaN HEMT devices, the C_{OUT} mainly refers to drain-source capacitor (C_{DS}) which is added to the miller effect of the gate-drain capacitance (C_{GD}). The variation of C_{DS} with drain-source voltage (V_{DS}) is slightly nonlinear, but largely affects the waveform of the output power. The relationship between the C_{OUT} of GaN HEMT and V_{DS} can be used to express by

$$C_{OUT}(V_{DS}) = C_{OUT0} + \alpha[1 + tanh(\beta V_{DS} + \gamma)]\ (pF). \quad (5)$$

In (5), C_{OUT0}, α, β, and γ are constant. These parameters are extracted from the Cree GaN HEMT model (CGH60015) in the way of model simulation. C_{OUT0}, α, β and γ are summarized as 1.9 pF, 1192.4, -0.0594714 and -2.94696, respectively [8]. And the relationship between C_{OUT} and V_{DS} is shown in Fig.2, in which the value of C_{OUT} decreases rapidly with the increasing of V_{DS}. The model of the packaged device CGH40010 containing a CGH60015 bare chip used to design the proposed DPA in the next section.

The transistor is equivalent to a voltage controlled current source, in which the voltage and current across C_{OUT} can be described as below:

$$V_{DS}(t_x) = V_{DD} + \int_{-\infty}^{t_x} i(t)dt / C_{OUT}(V_{DS}(t_x)) = V_{DD} + Q(t_x)/C_{OUT}(V_{DS}(t_x)). \quad (6)$$

Where $Q(t_x)$ is the charge of the capacitor C_{OUT} after time t_x. When a negative current i(t) flows through the transistor, $V_{DS}(t_x)$ drops along with the decrease of $Q(t_x)$,which leads to the rapid increase of C_{OUT}. When the bias voltage V_{DD} approaches the minimum value, the transistor is in the low power input range. $V_{DS}(t_x)$ is relatively stable due to a limited drive current and the increasing C_{OUT} as a compensation. The value of $Q(t_x)/C_{OUT}(V_{DS}(t_x))$ is calculated to be approximately a constant in the low power input range, which indicates that V_{DS} is relatively stable, as well as C_{OUT} consequently.

Since C_{OUT} is in a relatively stable range, it's possible to build an external compensation circuit to suppress P_{SAT_P} and P_{SAT_C} power leakage. In this way, the efficiency and OPBO range of DPA can be improved based on (1)-(4).

2.2. Circuit design

An LC parallel resonant circuit is utilized to compensate the transistor's parasitic capacitance. Distribution element circuit, namely microstrip line, is applied to replace lumped elements to avoid additional parasitic effects at this frequency. When the transmission line is shorter than λ/4, it is inductive, and its impedance can be written as

$$Z(-x) = jI_0 Z_0 sin\beta x / I_0 cos\beta x = jZ_0 tan\beta x. \quad (7)$$

Where, I_0 is terminal current and Z_0 is characteristic impedance. $\beta = 2\pi/\lambda$ is the wave number. Therefore, a short-circuited microstrip line is applied as an inductor, with its length x shorter than λ/4. The microstrip lines are in parallel between the output of the two transistors and their output matching circuits. They resonate with the two transistors' C_{OUT} to compensate the parasitic capacitance effect. The impedance between the two transistors' output port and the matching circuits can be expressed by

$$Z = \frac{(R + j\omega L)/j\,\omega C_{OUT}}{R + j(\omega L - 1/\omega C_{OUT})} = \frac{L}{C_{OUT}R} \cdot \frac{1 - jR/\omega L}{1 + j(\omega L/R - 1/\omega C_{OUT}R)}. \quad (8)$$

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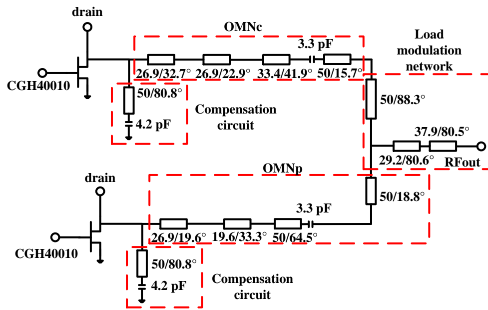


Fig. 3. Output matching circuits of proposed DPA

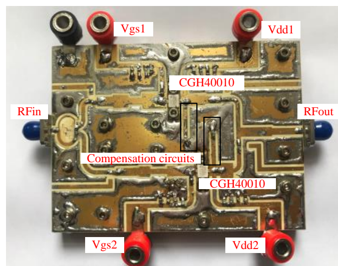


Fig. 4. Photo of te designed DPA

In (8), angular frequency $\omega = 2\pi f$, where f is the centre frequency and L is the inductance value of shorted microstrip line. R is the resistance of shorted microstrip line which equals to Z(-x). When

$$-R/\omega L = \omega L/R - 1/(\omega C_{OUT} R) \quad (9)$$

$$\omega = \sqrt{1/(LC_{OUT}) - R^2/L^2} \quad (10)$$

a resonance occurs in the circuit composed of C_{OUT} and short-circuit microstrip line. The value of L can be expressed by

$$L = \left(1 + \sqrt{1 + 4\omega^2 {C_{OUT}}^2 (Z_0 tan\beta x)^2}\right) / 2\omega^2 C_{OUT}. \quad (11)$$

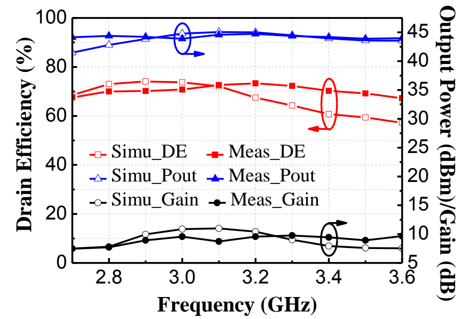
We can use the following formulas to calculate the length, x, and width, y, of the microstrip line that compensates for parasitic capacitance, which can be expressed by

$$x = \omega L / \beta Z_0 \quad (12)$$

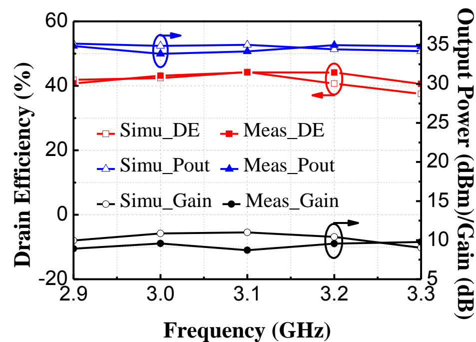
and the width of microstrip line is related to the characteristic impedance Z_0, which can be expressed by

$$Z_0 = \frac{\eta_0}{2\pi\sqrt{\varepsilon_{eff}}} ln\left[\frac{F}{\mu} + \sqrt{1 + \left(\frac{2}{\mu}\right)^2}\right] \quad (13)$$

$$F = 6 + (2\pi + 6)e^{\left[-\left(\frac{30.666}{\mu}\right)^{0.7528}\right]} \quad (14)$$



(a)



(b)

***Fig. 5.** Simulation and measurement results.*

(a) HB Simulation and measure comparison of saturated drain efficiency, output power and gain,

(b) Simulated and measured drain efficiency, output power and gain of the proposed DPA at 10dB back off .

Where $\eta_0 = 120\pi$ is the free-space wave impedance, and $\mu = y/h$ is the coefficient. The h is the thickness of the medium, and ε_{eff} is the relative dielectric constant. From the above formulas, the inductance for compensating the parasitic capacitance can be equivalent to the form of a microstrip line.

Parallel resonance compensates for the parasitic effects, which eliminates the power leakage through C_{OUT} to the ground. Therefore, it prevents the P_{SAT_P} and P_{SAT_C} from attenuation. The OPBO range is extended and the saturation efficiency of DPA is consequently improved due to the increased RF_{OUT}.

Once the capacitance compensation network is determine the DPA is designed based on Cree's CGH40010 GaN HEMT. Rogers4350B is chosen as the power amplifier plate (substrate thickness 30mil, dielectric constant 3.66). The carrier amplifier operates in class AB with a DC bias of 28V and -2.7V. The peak power amplifier operates in class C with a DC bias of 30V and -5.5V. The compensation circuits and output matching circuits of proposed DPA is shown in Fig. 3.

3. Simulation and measurement results

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Table 1 Comparisons with reported high efficiency and high back-off DPAs

Reference	Freq.(GHz)	Pout(dBm)	DE@sat (%)	OPBO(dB)	DE@OPBO(%)
[4]	1.7-2.8	44-44.5	57-71	9	37-41
[5]	0.73-0.98	44	45-68	9	49-64
[6]	1.9-2.2	43.8	-	9	47
[7]	1.6-2.4	40.5-41.5	55-60	6	42-54
[9]	1.5-2.4	42	65	6	>49
[10]	2-2.7	41	58-70	9	45-66
[11]	2	33.2	67	9.1	57.4
[12]	1.5-2.5	42-44.5	55-75	6	42-53
TW.	2.9-3.3	43.9-44.7	70.8-73.3	10	40.6-44.2

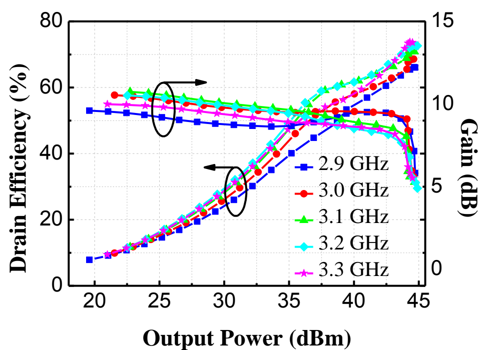

Fig. 6. *Gain and drain efficiency profiles versus output power.*

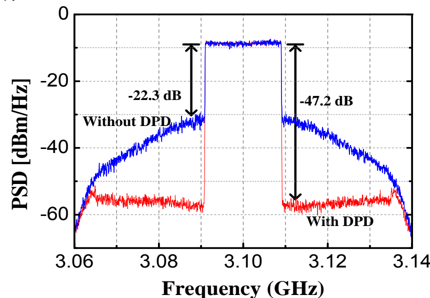

Fig. 7. *Measured power spectral density of a 20MHz LTE signal at 3.1 GHz with and without digital preditortion.*

Fig. 4 shows the photo of the developed DPA circuit, with the compensation network labelled along with RF and DC ports. Characterization of the fabricated DPA driven by a continuous wave (CW) signal is shown in Fig. 5(a) and Fig. 5(b). In Fig. 5(a), the measured drain efficiency (DE) is 67.2-73.3% at saturation and 40.4-52.2% at 6 dB OPBO, over the frequency range from 2.7 to 3.6 GHz, which agrees well with the simulation results. High efficiency of the DPA is observed with saturation output power ranging from 43.9 to 44.7 dBm within the 900MHz bandwidth.

Fig. 5(b) shows the simulated and measured drain efficiency, output power and gain of the proposed DPA at 10 dB back–off power. The back-off drain efficiency around 40.6%~44.2% is achieved over the entire OPBO region of 10 dB, as well as a peak Pout around 44.7 dBm. To further demonstrate the DPA's performance in communication systems, a long-term evolution (LTE) signal at 3.1 GHz (7.5 dB PAPR) is applied to the RF input, with a bandwidth of 20MHz. Digital pre-distortion (DPD) technology is used to increase the DPA's linearity range, which is typical in modern communication systems.

The measured drain efficiency and gain of the Doherty amplifier as a function of the output power are shown in Fig. 6 for 2.9, 3.0, 3.1, 3.2, and 3.3 GHz CW excitation. The typical Doherty high-efficiency region can be observed: it spans from a maximum output power exceeding 44.7 dBm to 10-dB back-off at all of the measurement frequencies. Fig. 7 shows the measured output spectrum of the DPA, with and without DPD applied. An adjacent channel leakage ratio (ACLR) of -47.2 dBc is obtained, which is lower than the requirement for a base station power amplifier, normally -45 dBc. A comparison has been made regarding the performance of the proposed DPA in this work and reported ones in Table 1. The proposed DPA demonstrates significant improvements in both OPBO range and saturation efficiency in the S-band.

4. Conclusion

In this paper, a high-performance S-band DPA is presented based on Cree's CGH40010 GaN HEMT, featuring high efficiency and wide OPBO range. A novel parasitic capacitance compensation network is developed for

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the DPA design, which effectively suppress the power leakage of the transistor. The overall saturation power of the DPA is increased, thus resulting in a significant improvement in the DPA's efficiency and OPBO range. Measured results indicate that the proposed DPA design has an excellent saturation efficiency over 70% and a 10dB OPBO range. Hence, high saturation efficiency in wide output power back off range has been achieved by the DPA, which makes it an attractive device for the transceiver system of cellular base stations.

5. Acknowledgments

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