

MINIATURIZED ON-CHIP PASSIVE DEVICES FOR MILLIMETRE-  
WAVE APPLICATIONS IN BI-CMOS TECHNOLOGY

by  
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## ABSTRACT

Recent advances in silicon-based integrated circuits (ICs) have successfully demonstrated promising system-on-chip (SoC) solutions to support micro- and millimeter-wave (mm-wave) applications. As the end of Moore's Law is approaching, the full potential of active devices is eventually going to be reached. The technical advancement of these emerging technologies can further push through the introduction of alternative equivalent scaling techniques such as the implementation of new design geometries. As the interest in the mm-wave band grows, circuit miniaturization is faced with a unique set of challenges and constraints. In this work, we looked at the growing potential of monolithic integration to design high-performance transceiver system building blocks.

This thesis presents a passive inspired implementation of resonator and bandpass filters designed, and fabricated using IHP 0.13  $\mu\text{m}$  SiGe Bi-CMOS process. Two unique miniaturization design methodologies are presented in this work. In order to fully demonstrate the insight of this approach, a simplified equivalent LC-circuit model is used for theoretical analysis. Using the analyzed results as a guideline along with a full-wave electromagnetic (EM) simulator, two compact bandpass filters (BPFs) are implemented and designed for mm-wave applications.

The first design methodology is a folded-strip-line-based design. The proposed method is based on a planar structure in which neither broadside coupling nor crossover between metals is required. Only a single metal layer is used to implement a compact resonator. To demonstrate its flexibility a



BPF is designed. The 1st BPF has one transmission zero at 58 GHz with a peak attenuation of 23 dB. The center frequency of this filter is 27 GHz with an insertion loss of 2.5 dB, while the  $S_{11}$  is better than 10 dB from 26 to 31 GHz. The 2nd BPF has two transmission zeros, and a minimum insertion loss of 3.5 dB is found at 29 GHz. The  $S_{11}$  is better than 10 dB from 26 GHz to 34 GHz. Also, more than 20 dB stop-band attenuation is achieved from DC to 20.5 GHz and from 48 GHz to 67 GHz. The chip sizes of these two BPFs, excluding the pads, are only 0.023 mm<sup>2</sup> and 0.028 mm<sup>2</sup>, respectively.

The second methodology is designed with ultra-wideband and low insertion loss. The proposed approach uses merely a combination of meander-line structures with metal-insulator-metal (MIM) capacitors. For the 1st BPF, the return loss is better than 10 dB from 13.5 to 32 GHz, which indicates a fractional bandwidth of more than 78%. Also, the minimum insertion loss of 2.3 dB is achieved within the frequency range from 17 GHz to 27 GHz, and the in-band magnitude ripple is less than 0.1 dB. The chip size of this design, excluding the pads, is 0.148 mm<sup>2</sup>. To demonstrate a miniaturized design, a 2nd design example is given. The return loss is better than 10 dB from 17.3 to 35.9 GHz, which indicates a fractional bandwidth of more than 70%. Also, the minimum insertion loss of 2.6 dB is achieved within the frequency range from 21.4 GHz to 27.7 GHz, and the in-band magnitude ripple is less than 0.1 dB. The chip size of the 2nd design, excluding the pads, is only 0.066 mm<sup>2</sup>.

The overall performances of both proposed structures are suitable for miniaturizing design in silicon-based technology. The presented design can be useful to co-design with active devices. As compared to the previously published literature, the presented design in this thesis offer a promising solution in scaling down the physical size of the passive component.



## CERTIFICATE OF ORIGINAL AUTHORSHIP

I certify that the work in this thesis has not previously been submitted for a degree nor has it been submitted as part of requirements for a degree.

I also certify that the thesis has been written by me. Any help that I have received in my research work and the preparation of the thesis itself has been acknowledged. In addition, I certify that all information sources and literature used are indicated in the thesis.

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*Dedicated to My Beloved Parents*

*Francisco and Myrle Bautista*



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# List of Publications

## Journal publications

- **Meriam Gay Bautista**, , He Zhu, Xi Zhu, Yang Yang, Yichuang Sun, and Eryk Dutkiewicz “Compact Millimeter-Wave Bandpass Filter Using Quasi-lumped Elements in  $0.13\mu\text{m}$  (Bi)-CMOS Technology for 5G Wireless Systems,” in *IEEE Transactions on Microwave Theory and Techniques: Special Issue on 5G Hardware and System Technologies* (recently accepted - 4th-Jan.2019) (Corresponding to Chapter 3 and 4)

## Conference publications

- **Meriam Gay Bautista** , Xiao Pu Zhang, Xi Zhu, Eryk Dutkiewicz “Design of On-Chip Edge-Coupled Resonator and Its Application for Bandpass Filter in CMOS Technology,” in *Proc. 2018 18th International Symposium on Communications and Information Technologies (ISCIT)*, Bangkok, Thailand, 2018, pp. 1-4. doi: 10.1109/ISCIT.2018.8587994 (Corresponding to chapter 4)
- **Meriam Gay Bautista**, Jefferson Hora, Eryk Dutkiewicz “Design Methodology of a Miniaturized Millimetre Wave Integrated Passive Resonator Using (Bi)-CMOS Technology,” in *Proc. 2018 18th International Symposium on*

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- **Meriam Gay Bautista**, Yang Yang, Eryk Dutkiewicz, “Compact On-Chip 60 GHz Resonator with Ring Defected Ground Structure for Millimetre-wave Applications,” in *Proc. 2017 IEEE 9th International Conference on Humanoid, Nanotechnology, Information Technology, Communication and Control, Environment and Management (HNICEM)*, Manila, 2017, pp. 1-4.
  - **Meriam Gay Bautista**, Eryk Dutkiewicz, Yang Yang, “Design of a Compact Self-Coupled Resonator and Dual-band Bandpass Filter in 0.13- $\mu\text{m}$  CMOS Technology for Millimetre-wave Application,” in *Proc. 2017 Progress in Electromagnetics Research Symposium - Fall (PIERS - FALL)*, Singapore, 2017, pp. 2653-2658. doi: 10.1109/PIERS-FALL.2017.8293586 (Corresponding to chapter 3 and 4)
  - **Meriam Gay Bautista**, Jin Bao Zhu, Forest Zhu, Yang Yang, Eryk Dutkiewicz “Design of On-Chip Quadrature Hybrid (3dB) Branchline Coupler in 0.13 $\mu\text{m}$  SiGe Technology For Millimeter-wave Applications,” in *Proc. 2017 17th International Symposium on Communications and Information Technologies (ISCIT)*, Cairns, QLD, 2017, pp. 1-5. doi: 10.1109/ISCIT.2017.8261191
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  - **Meriam Gay Bautista**, Eryk Dutkiewicz, Michael Heimlich, “Sub-Threshold Energy Harvesters for Biomedical Implants Application,” *Grace Hopper Conference for Women in Computing Emerging Technology tract presentation*, Oct. 2015

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- Yichuang Sun, Xi Zhu and **Meriam Gay Bautista** “Design of Fifth-order Leap-frog 0.05 deg. Linear Phase Low-pass Filter with Gain Boost Using Nauta OTA,” in *Proc. 2017 17th International Symposium on Communications and Information Technologies (ISCIT)* , Cairns, QLD, 2017, pp. 1-4. doi: 10.1109/ISCIT.2017.8261201
- Y.Sun, **Meriam Gay Bautista**, Forest Zhu and Eryk Dutkiewicz “Design of an Elliptic Filter using Multiple-Loop Feedback Structure in CMOS Technology for Analogue Signal Processing,” in *Proc. 2017 IEEE 85th Vehicular Technology Conference (VTC Spring)*, Sydney, NSW, 2017, pp. 1-5 doi: 10.1109/VTCSpring.2017.8108421