A New Switched-Capacitor Five-Level Inverter Suitable for Transformerless Grid-Connected Applications

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***Abstract*—Transformerless grid-connected inverters have been extensively popular in renewable energy-based applications owing to some interesting features like higher efficiency, reasonable cost and acceptable power density. The major concern of such converters is the leakage current problem and also the step-down feature of the output voltage which causes a costly operation for a single stage energy conversion system. A new five-level transformerless inverter topology is presented in this study, which is able to boost the value of the input voltage and can remove the leakage current problem through a common-grounded architecture. Here, providing the five-level of the output voltage with only six power switches is facilitated through the series-parallel switching of a switched-capacitor module. Regarding this switching conversion, the self- voltage balancing of the integrated capacitors over a full cycle of the grid's frequency can be acquired. Additionally, to inject a tightly controlled current to the local grid, a peak current controller-based technique is employed, which can regulate both the active and reactive power support modes. Theoretical analyses besides some experimental results are also given to corroborate the correct performance of the proposed topology.**

***Index Terms*—Transformerless inverter, Common ground type, Switched Capacitor module and Grid connected applications**

I. INTRODUCTION

TRANSFORMERLESS grid-connected inverters feeding through renewable energy-based resources like photovoltaic (PV) panels are counted as an interesting power circuit architecture owing to their valuable characteristics like the compact size, higher energy conversion efficiency and appropriate manufacturing cost. Since the isolating transformer is to be removed in such structures, some associated problems should be addressed in advance [1-2]. Variable common mode voltage (CMV) and in turn the leakage current problem is the most important item in the circuit feasibility of such converters. Concerning this, the quality of the injected current can be degraded and the strayed power losses of the converter is prone to be increased [3].

Alternatively, having whole the capacity of the input voltage as the peak value of the inverter's output voltage is another crucial challenge. In the presence of the PV with the string inverter, many PV panels are required to be connected in series to make it equal to the required dc-link voltage for a standard grid application. This may need additional step-up power processing stages in buck-type inverters, which can introduce extra power losses [4]. Recently, many power circuit topologies and modulation techniques have been reported in the literature to overcome the aforementioned problems. By adding extra power switches into the conventional full bridge (FB)-based inverters operating with the unipolar pulse width modulation (PWM) mechanism, the CMV of the inverter can be relatively constant and the leakage current value is mitigated. H5 [5], HERIC [6], OH5 [7], and different family of H6 [8-9] inverters are some of the most important topologies of this category. Additional conduction losses, higher value of the leakage current in the reactive power support modes along with the step-down feature in the inverter operation are the main shortcomings of such converters.

Connecting the null of the grid to the neutral point of the conventional half-bridge (HB) inverters is another alternative solution. Here, since the output voltage waveform is bipolar, the quality of the injected current is degraded and the switching losses are high; so the family of neutral point clamp (NPC) inverters with unipolar PWM waveforms are preferred [10-11]. Through the hybrid topological techniques like integrating the flying capacitor (FC) cells into the active-NPC (ANPC) [12] or T-type-based inverters [13], the number of output voltage levels can be enhanced and the quality of the injected current is improved. However, in these cases the inverter output voltage is half of the dc link value, which may require additional front-end boost converters for PV applications.

Use of Common-grounded technique in transformerless inverters is another case study that is suitable for almost totally suppressing the leakage current value in single-phase grid-connected applications [14-27]. Herein the parasitic capacitance of the negative terminal of the PV panels is bypassed through the straight connection of the PV ground and the grid's null. In this case, a virtual dc link capacitor is required to provide the negative cycle of the inverter's output voltage. The charging and discharging principle of such a virtual dc link capacitor is subject in different platforms. Considering this, the five-switch-based three-level common-grounded inverter have been presented in [14] and [15]; however, since the virtual dc bus capacitor is charged in the positive half-cycle only, it requires a relatively large virtual capacitor and bulky inductor as the filter. By integrating an inductor and a charged pumped circuit into the charging path of the virtual dc bus, this operation could be improved in [16-18]; yet more passive elements should be employed in these

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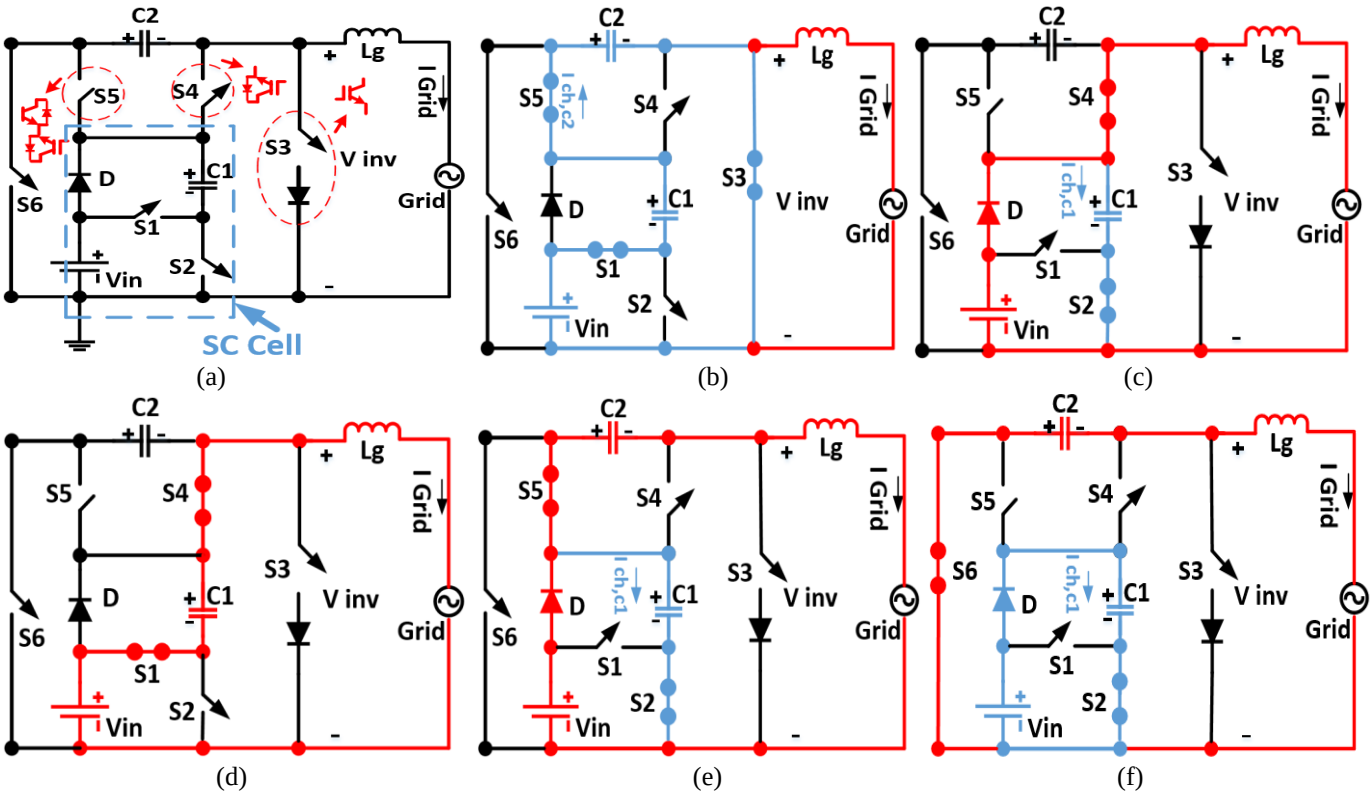

Fig. 1. The proposed five-level SC-based transformerless inverter (a) the main circuit configuration (b) the current flowing path of the zero level (c) the current flowing path of the first positive output voltage level (d) the current flowing path of the top positive output voltage level (e) the current flowing path of the first negative output voltage level (f) the current flowing path of the top negative output voltage level.

structures. In following, three different four-switch-based common-grounded inverters were also proposed in [19] in which the virtual dc bus can be charged and discharged in both half-cycle with unipolar PWM inverter output. Regarding such descriptions, all the mentioned common-grounded structures possess a step-down feature, where the peak of the ac output voltage is less than the dc input. To meet the proper grid amplitude requirement, the double-stage energy conversion system is also employed in [20-22], which increases the number of passive elements and the power losses. To overcome this, a buck-boost type unipolar inverter has been presented in [23] using an inductor-based charge-pumped technology. In this circuit, five power switches are employed to generate three output voltage levels. Using the same concept, a four switches-based inverter was also presented in [24] and [25], while they suffer from the bipolar PWM output voltage.

Considering the virtual dc bus concept in the common-grounded inverters, two different five-level inverter structures were proposed in [26] and [27] that respectively utilized the HB and FC cells. Although the size of the filter is reduced through the enhancement in the number of output voltage levels, the voltage boosting feature is still absent there.

The aim of this paper is to present a new type of common-grounded five-level transformerless inverter, which can improve the performance of the grid-connected systems by its inherent boosting feature and unipolar PWM scheme. Using a switched-capacitor (SC) module and the virtual dc link technique, a voltage boost of two times within a single stage operation can be achieved. In addition, a simple peak current controller (PCC) strategy with appropriate dynamic response is employed to modulate the gate of the involved switches. Through the proposed PCC strategy, a tightly controlled current is also obtained which is able to support both the active and reactive powers of the grid. Rest of this paper is organized as: the working principle of the proposed inverter is explained in section II. The PCC operation of the proposed grid-tied system is described in section III. Losses analysis with design guidelines of the passive elements and the voltage/current stresses analysis of switches are given in section IV. A complete comparative study with other existing topologies is presented in section V and finally a built prototype results are shown in section VI to verify the feasibility and accurate performance of the proposed system.

II. Circuit Description of the Proposed Common-Grounded Five-Level SC-Based Inverter

The overall configuration of the proposed five-level SC-based transformerless grid-connected inverter has been depicted in Fig. 1 (a). Here, six power switches, a single power diode, two capacitors alongside an inductor as the filter are utilized. Using the SC-based module integrated in the circuit, the proposed topology is able to boost the PV voltage as the input dc source within a single stage. In this case, the capacitor C_2 acts as a virtual dc link like what has been using in the conventional approaches. Regarding this circuit architecture, the negative terminal of the input source is directly connected

to the null of the grid, which makes a common-grounded feature for the proposed topology. Here, four of the involved power switches are the unidirectional type with anti-parallel diode, while switch S_3 is unidirectional without antiparallel diode. Also, the switch S_5 is the bi-directional one with the capability of blocking the peak inverse voltage (PIV) in both polarities. In practice, reverse blocking IGBT (RB-IGBT) can be used for this type of power switches [19].

In order to show different current flowing paths of the proposed topology, Fig. 1 (b)-(f) can be considered. Here, the red and blue lines indicate the active grid current and the charging current paths for the capacitors, respectively. Also, $I_{ch,C1}$ and $I_{ch,C2}$ respectively show the direction of the charging current for C_1 and C_2. Considering Fig. 1(b), the zero-level of the output voltage is made through the ON state switch S_3, while by discharging of C_1 through S_1, the diode in the SC cell will be in reverse-biased. By taking a fixed voltage of V_{dc} as the input voltage provided by the PV panels, the capacitor C_2 can be charged to $2V_{dc}$ through S_5 and S_3. In this case, once the voltage across C_2 exceeds the sum of the voltage of the PV panel and C_1, the series diode of S_3 will be in forward-biased and therefore the grid current can pass from the red path line. In turn, once the voltage of C_2 is to be less than $2V_{dc}$, the grid current with any of direction will flow through the blue charging flow path.

Considering the same direction of the grid current and the local grid voltage, the first level of the output voltage ($+V_{dc}$) can be made by the parallel switch of the SC cell (S_2) and also the switch S_4 as shown in Fig. 1 (c). Here, the integrated power diode is in the forward-biased mode and C_2 is disconnected from the grid, whereas irrespective of the grid current's direction, C_1 is charged by the dc supply. Afterwards, in order to make the top-level of the output voltage in the positive half-cycle of the grid voltage, Fig. 1(d) should be taken into account. In this case, S_4 is again turned ON, while through the series switch of the SC cell (S_1), the power diode of the SC cell is in the reverse-biased; therefore the voltage across the charged capacitor C_1 will be added to the dc supply's voltage and in turn the level of $+2V_{dc}$ will be generated. Herein, C_2 is again disconnected from the grid, while depending on the direction of the injected current to the grid (active or reactive power support mode), C_1 can be discharged or charged.

During the negative sequence of the grid voltage, the importance of the pre-charged capacitor C_2 is highlighted. Here, to make the first negative-level of the output voltage ($-V_{dc}$), the switch S_5 should be ON as indicated in Fig. 1 (e), whereas through the parallel switch S_2 in the SC cell, C_1 can be charged. It is clear that in the active power mode, the C_2 will be charged by the dc supply and within the reactive power mode it will be discharged. Taking Fig. 1 (f) into consideration, the top negative level of the output voltage ($-2V_{dc}$) can be generated with a direct contribution of the S_6 and C_2. Here, depending on the grid current's direction, C_2 can be charged and discharged, whereas through the parallel switch S_2 in the SC cell, C_1 can be charged by the supply once again. Regarding the above-mentioned description, the voltage across the C_1 and C_2 remains balanced at V_{dc} and $2V_{dc}$, respectively. Here, in addition to generating the five distinct levels of the output voltage by the aim of only six power switches, the proposed topology offers a valuable voltage boosting feature also. Such advantage is quite important for a PV with string inverter as it reduces the number of PV panels in string.

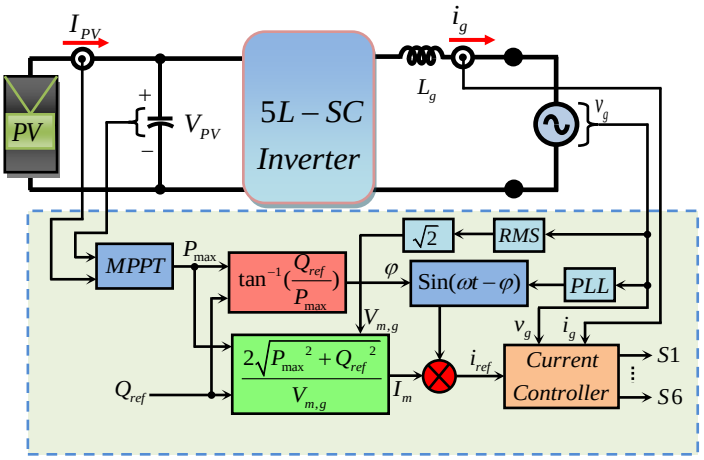

Fig. 2. The overall block diagram of the controlled system.

III. Implementation of the Proposed PCC Technique

A PCC-based technique is used in this study in order to trigger the gate of power switches and also regulate both the active and reactive injected powers of the grid. Generally, the main objective of the transformerless grid-connected inverters is to inject a tightly controlled current into the grid. Among the various schemes of control and modulation strategies, the current controller techniques have been more popular than the voltage-oriented control (VOC) schemes since they possess very fast and robust performance with almost zero steady state errors under various dynamic conditions of the local grid [28-30]. Here, the PCC strategy is a derived version of the conventional hysteresis current controller (HCC) techniques, which can properly track the reference waveform of a controlled system without any extra bands and just by comparing the instantaneous value of the grid's current (i_g) with the reference one (i_{ref}). In this case, the single inductor of the inverter's filter (L_g) plays an important role since it can provide the sufficient phase difference between the inverter's output voltage and the grid's voltage to inject the power into the grid. The overall block diagram of the proposed controlled system is illustrated in Fig. 2. Here, it is supposed to have a PV panel with maximum power point tracker (MPPT) block at the input side of the proposed inverter.

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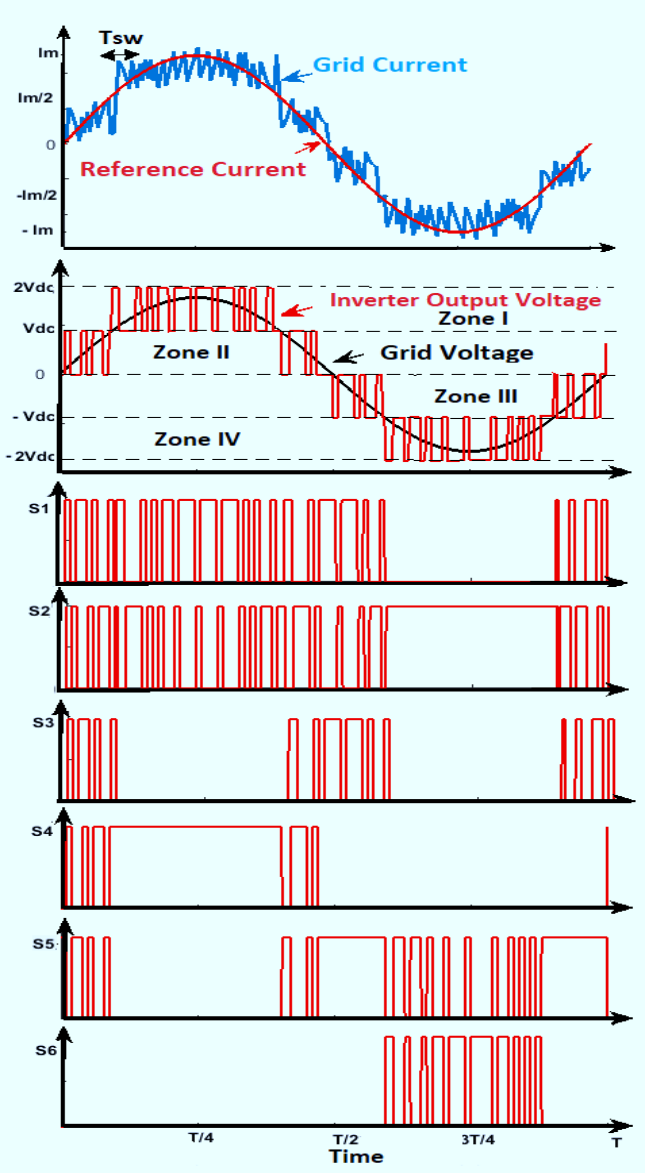

Fig. 3. A typical operation of the proposed PCC technique and the corresponding output voltage with gate switching pulses waveforms at the unity PF.

As it is obvious, the peak value of the reference current (I_m) for the proposed PCC technique can be obtained through the MPPT block. This value depends on the maximum captured power from the PV panel as $P_{\max}$ and the supposed reactive power intending to be injected to the grid (Q_{ref}). Also, a phase-locked loop (PLL) block is needed, which can provide the synchronous phase of the grid voltage for the current reference waveform. To properly address the operating principle of the proposed PCC technique, a measured value of the grid or inductor's current is also required as can be realized by Fig. 2. The proposed PCC technique is on the basis of a sampling time (T_S), which can reflect the variable switching frequency of the switches ($1/T_{Sw}$). The PCC block in the proposed controlled system demands two important input data. The first one is related to the i_g ; so by comparing the desired reference and measured currents within the

Table I. Switching States and PCC Description of the Proposed Five-Level SC-Based Inverter Under the Unity PF Condition

Zone No	PCC Description	ON State Switches	Inverter Output Voltage
I	$i_g \le i_{ref}$	S_4, S_1	$2V_{dc}$
	$i_g > i_{ref}$	S_4, S_2	V_{dc}
II	$i_g \le i_{ref}$	S_4, S_2	V_{dc}
	$i_g > i_{ref}$	S_1, S_5, S_3	0
III	$i_g \le i_{ref}$	S_1, S_5, S_3	0
	$i_g > i_{ref}$	S_2, S_5	$-V_{dc}$
IV	$i_g \le i_{ref}$	S_2, S_5	$-V_{dc}$
	$i_g > i_{ref}$	S_2, S_6	$-2V_{dc}$

sampling frequency, the instant slope and value of the inductor's or grid's current are identified.

To generate all the five the output voltage levels at the inverter's output, a definition of the working zones depending on the instant location of the grid's voltage ($V_g(t)$) with respect to the input voltage (V_{dc}) is needed as the second input data of the proposed PCC. Such working zones are independent from the reference/grid current and are defined as: $V_{dc} \le V_g(t) \le 2V_{dc}$ for zone I, $0 \le V_g(t) \le V_{dc}$ for zone II, $-V_{dc} \le V_g(t) \le 0$ for zone III, and $-2V_{dc} \le V_g(t) \le -V_{dc}$ for zone IV. Regarding the instant slope of the measured grid or inductor's current and considering the defined working zones, the switching pulses of the proposed five-level SC-based inverter are obtained. The operating principles of the proposed PCC technique under the unity power factor (PF) (active power support mode) and the non-unity PF (reactive power support mode) are discussed in the following subsections:

A. Active Power Support Mode (Unity PF)

Considering a low value of the sampling frequency as a role example, the operation of the proposed PCC technique enabling to provide five-output voltage levels within four defined zones at the unity PF for the proposed topology is illustrated in Fig. 3. Herein, the typical waveforms of the inverter's injected current, desired reference current, inverter's output voltage, and the gate pulses of the involved power switches have been depicted. To further clear the modulation process of the switches, Table I can also be taken into account. In this case, during the operation at the unity PF, the direction of the injected grid current is from the inverter side to the grid side. So, from this Table and Fig 3, it is revealed that once the instant value of i_g exceeds the reference current in each of working zones, the slope of the grid's current will have a upward trend. So, the PCC generates the lower output voltage level of each working zone ($V_{inv,low}$) to meet the volt-second balanced principle of the filter's inductor. Also, whenever this value is to be less than the reference current, the slope will be in its negative trend; so the upper output voltage level of each working zone ($V_{inv,up}$) is made.

Similar to other current-controlled based schemes, the switching frequency in each of the defined zones is specific and can be separately derived.

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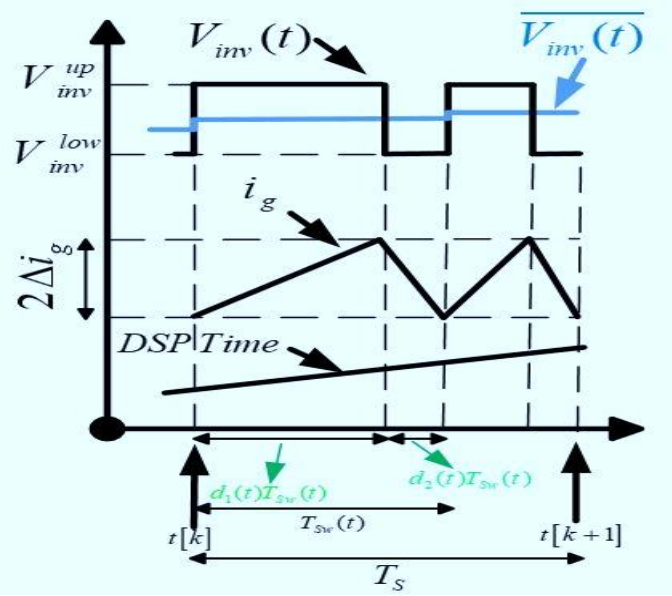

Fig. 4. The proposed PCC description for a defined working zone and during each sampling time between the instant DSP capturing time of k and k+1.

To further explore the performance of the proposed PCC with such a variable switching frequency, Fig. 4 can be considered. In this case, the typical waveforms of the inverter's output voltage, the average voltage of the inverter ($\overline{V_{inv}(t)}$), and the injected grid current during a specific sampling period capturing by the host digital signal processor (DSP) and within a specific operating zone have been depicted. Regarding this and considering the general relationship between the inverter's output voltage and the grid voltage, the following expression can be written:

$$V_{inv}(t) = L_g \frac{di_g}{dt} + V_g(t) \tag{1}$$

Where, $V_{inv}(t)$ can possess two mentioned values ($V_{inv,up}$ and $V_{inv,low}$) in each zone and during each switching period as shown in Fig. 4. Regarding the fact that $\overline{V_{inv}(t)}$ is constant during each switching period [29] and considering a fixed dc link voltage (V_{dc}) as the input voltage of the inverter after the MPPT operation, the variable switching period for each of the working zones can be derived as follows:

$$T_{Sw}(t) = \begin{cases} \dfrac{2\Delta i_g L_g (-V_{dc})}{\left(2V_{dc} - \overline{V_{inv}(t)}\right)\left(V_{dc} - \overline{V_{inv}(t)}\right)} \xrightarrow{for} Zone\ I \\ \dfrac{2\Delta i_g L_g V_{dc}}{\overline{V_{inv}(t)}\left(V_{dc} - \overline{V_{inv}(t)}\right)} \xrightarrow{for} Zone\ II \\ \dfrac{-2\Delta i_g L_g V_{dc}}{\overline{V_{inv}(t)}\left(V_{dc} + \overline{V_{inv}(t)}\right)} \xrightarrow{for} Zone\ III \\ \dfrac{2\Delta i_g L_g V_{dc}}{\left(2V_{dc} + \overline{V_{inv}(t)}\right)\left(V_{dc} + \overline{V_{inv}(t)}\right)} \xrightarrow{for} Zone\ IV \end{cases} \tag{2}$$

Where, Δi_g is the ripple current value across the filter's inductor and $\overline{V_{inv}(t)}$ can possess a positive and negative value in zone I/II and III/IV, respectively.

Table. II. Definition of the Duty Cycle for the Involved Switches

Respective Switch	Zone I	Zone II	Zone III	Zone IV
S_1	$2d(t)-1$	$-2d(t)+1$	$2d(t)+1$	0
S_2	$-2d(t)+2$	$2d(t)$	$-2d(t)$	1
S_3	0	$-2d(t)+1$	$2d(t)+1$	0
S_4	1	$2d(t)$	0	0
S_5	0	$-2d(t)+1$	1	$2d(t)+2$
S_6	0	0	0	$-2d(t)-1$

Having taken Fig. 4 into account and considered such a variable switching period, in order to ease the loss/design analysis, the duty cycle of the involved switches, which is independent from the variable switching period of each zone, can be accordingly derived [30]. Herein, the average value of $V_{inv}(t)$ over each switching period and as for each of the defined zones can be written as follows:

$$\frac{(V_{inv,up})T_{sw}(t)d_1(t) + (V_{inv,low})T_{sw}(t)d_2(t)}{T_{sw}(t)} = \frac{1}{T_{sw}(t)} \int_0^{T_{sw}(t)} V_{inv}(t)d\tau \tag{3}$$

where, $t \gg \tau$ and $d(t)$ is the switching duty cycle in the grid frequency which can be expressed as (4).

$$d(t) = D_m Sin(\omega t) \tag{4}$$

where, ω is the angular term at the grid frequency. Also D_m is the corresponding modulation index related to the maximum amplitude of the grid's voltage ($V_{m,g}$) and the inverter voltage ($2V_{dc}$) and can be found out by (5):

$$D_m = \frac{V_{m,g}}{2V_{dc}} \tag{5}$$

Regarding (3) and considering Fig. 4, $d_1(t)$ and $d_2(t)$ are respectively denoted as the normalized dwell time of the upper and lower inverter's output voltage level over each switching period and they are valid as for each of the working zones; therefore we can write:

$$d_1(t) + d_2(t) = 1 \tag{6}$$

Now, having considered the two-time boost factor of the proposed five-level SC-based inverter output voltage and taken (4) into consideration, the relation of (3) can be further simplified as (7).

$$(V_{inv,up})d_1(t) + (V_{inv,low})d_2(t) = 2d(t)V_{dc} \tag{7}$$

Where, regarding Fig. 4, $2d(t)V_{dc}$ as the function of inverter's output voltage is constant during each switching period [27]. Since, four different working zones have been defined, so considering (6) and (7), the value of $d_1(t)$ and $d_2(t)$ for each of them are different and can be taken from (8) to (11).

$$\begin{cases} d_1(t) = 2d(t) - 1 \\ d_2(t) = 2 - 2d(t) \end{cases} \rightarrow Zone\ I \tag{8}$$

$$\begin{cases} d_1(t) = 2d(t) \\ d_2(t) = 1 - 2d(t) \end{cases} \rightarrow Zone\ II \tag{9}$$

$$\begin{cases} d_1(t) = 1 + 2d(t) \\ d_2(t) = -2d(t) \end{cases} \rightarrow Zone\ III \tag{10}$$

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$$\begin{cases} d_1(t) = 2 + 2d(t) \\ d_2(t) = -2d(t) - 1 \end{cases} \rightarrow Zone\ IV \qquad (11)$$

Therefore, regarding the switching states of the proposed topology given by Table I and considering the above-mentioned relations, the corresponding duty cycle of six involved power switches in each of the working zones are summarized based on Table II.

B. Reactive Power Support Mode (Non-Unity PF)

In the non-unity PF operation, the abovementioned operating principle of the proposed PCC is slightly different. Considering Fig. 2, the required angle (φ) and amplitude (I_m) of the reference current should be identified at the first to make a desired reference waveform. Here, the definition of the four working zones is independent from the reference/measured grid current and is the same as what explained as for the unity PF operation. So, similar to the active power support mode, the specific zone related to the location of the grid voltage in respect to the input voltage must be detected in advance. Since the direction of the injected current in reactive power support mode is from the grid to the inverter (as opposed to the active power support one), then the polarity of the L_g is supposed to change (reverse polarity); so, once the measured value of i_g at each working zone exceeds the i_{ref}, the upper output voltage level of each zone ($V_{inv,up}$) must be created to change the slope of the grid or inductor current transition; and whenever i_g is less than i_{ref}, the lower output voltage of each zone ($V_{inv,low}$) must be generated. Through this switching transition, the volt-second balanced principle of the inductor can be also met like what explained for the unity PF operation. The typical waveforms of the grid current, reference current, grid's voltage, inverter's output voltage and the switching pulses of the involved switches operating at the very low switching frequency and under the non-unity PF condition are also depicted in Fig. 5. Herein, to further clear the states of the switches, Table III can be considered. As it is clear, through the reactive power support mode, the ON/OFF states of the switches is different in contrast to their condition in the active power support mode since the PCC technique is tracking a phase-shifted reference current waveform. Regarding these changes in the state condition of the involved switches, their operating duty cycle is accordingly affected as discussed earlier.

IV. Losses, Design Guidelines and Current/Voltage Stresses Analysis

The aim of this section is to give some descriptions about the conduction losses of the involved power switches as well as the design guidelines of the passive involved components and the current/voltage stress analysis of the employed semiconductor devices. In this case, the switching loss analysis of the switches is similar to other presented works and can be found in the literature [26-27]. Here, all the analysis is done based on the unity PF condition.

A. Conduction Losses

As for the first step, the inverter's output voltage waveform emphasizing on the described dwell times, the current stresses

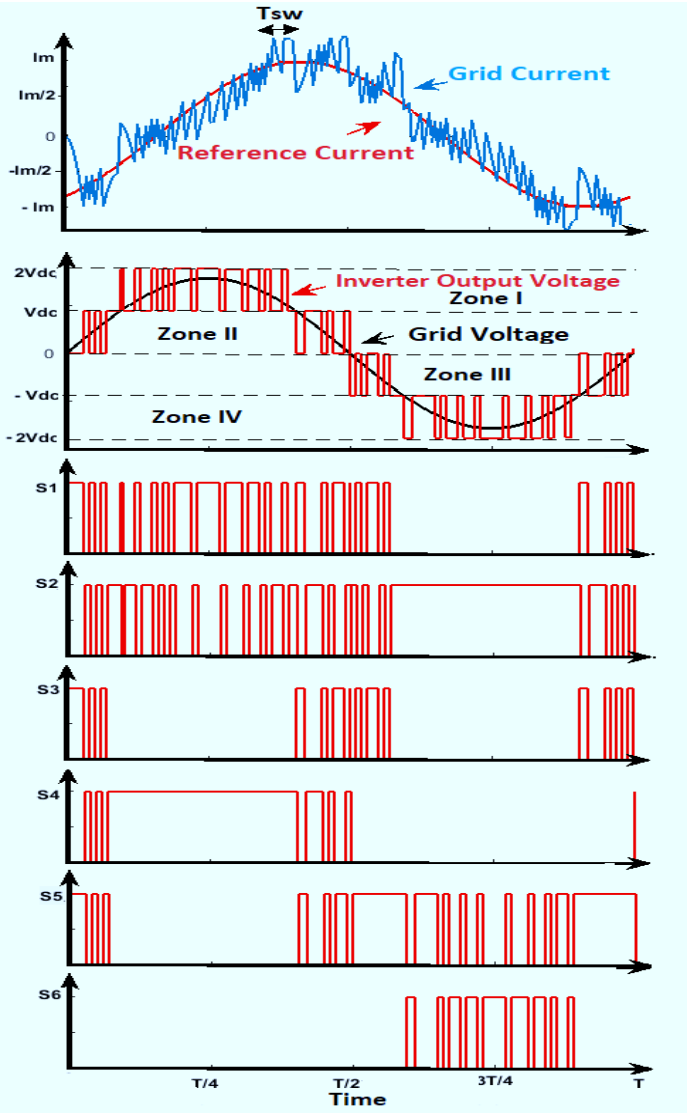

Fig. 5. A typical operation of the proposed PCC technique and the corresponding output voltage with gate switching pulses waveforms at the non-unity PF.

Table III. Switching States and PCC Description of the Proposed Five-Level SC-Based Inverter Under the Non-Unity PF Condition

Zone No	PCC Description	ON State Switches	Inverter Output Voltage
I	$i_g \le i_{ref}$	S_4, S_2	V_{dc}
	$i_g > i_{ref}$	S_4, S_1	$2V_{dc}$
II	$i_g \le i_{ref}$	S_1, S_5, S_3	0
	$i_g > i_{ref}$	S_4, S_2	V_{dc}
III	$i_g \le i_{ref}$	S_2, S_5	$-V_{dc}$
	$i_g > i_{ref}$	S_1, S_5, S_3	0
IV	$i_g \le i_{ref}$	S_2, S_6	$-2V_{dc}$
	$i_g > i_{ref}$	S_2, S_5	$-V_{dc}$

of the involved switches besides the capacitors passing current and a typical waveform of the injected grid's current within two cycles of the grid's frequency ($2T$) are shown in Fig. 6. As it is clear, the time intervals of $[t_1 - 0]$ and $\left[\frac{T}{2} - t_2\right]$ belong

to the second working zone, while $\left[t_3-\frac{T}{2}\right]$ and $\left[T-t_4\right]$ represent the third working zone. Also, the first and fourth working zones' time intervals are respectively indicated as $\left[t_2-t_1\right]$ and $\left[t_4-t_3\right]$. Considering the transition time between the first and second working zone, the instant value of t_1 is equal to (12):

$$D_m \sin(\omega t_1)=0.5 \rightarrow t_1=\frac{1}{\omega}\times \sin^{-1}(\frac{0.5}{D_m}) \quad (12)$$

So, other value of t_2, t_3 and t_4 can be obtained in respect to t_1. Contemporary, the conduction loss of each of the involved power switches over a full cycle of the grid's frequency is obtained as (13):

$$P_{C-Si}=\frac{1}{T}\int_0^T \left|V_{on} d_{Si} i_g(t)\right| dt \quad i=1,2,...,6 \quad (13)$$

Where d_{Si} is the duty cycle of each switch and can be found from Table II. Also, V_{on} is the ON state voltage drop across each power switch and the injected grid current's function can be supposed to be:

$$i_g(t)=I_m \sin(\omega t) \quad (14)$$

Therefore, regarding Fig. 6 and Table II, the conduction loss of a typical power switch such as S_1 at the unity PF can be taken as (15). Using (4) into (15), the obtained value of the conduction loss of S_1 will be about $V_{on}I_m/2\pi$ and the corresponding values of other involved power switches can be also derived in a similar way.

$$P_{C-S1}=\frac{V_{on}I_m}{T}\left(\begin{array}{l} 2\times\int_0^{t_1}\left|(1-2d(t))\sin(\omega t)\right|dt+\int_{t_1}^{t_2}\left|(2d(t)-1)\sin(\omega t)\right|dt \\ +2\times\int_{\frac{T}{2}}^{t_3}\left|(1+2d(t))\sin(\omega t)\right|dt \end{array}\right) \quad (15)$$

Herein, three power switches named as S_1, S_3 and S_5 are put into the charging path of C_2 during the zero output voltage level generation as can be realized by Fig.1 (b).

Also, the power switch S_2 is affected by the charging current of C_1 during the negative output voltage levels and the first positive output voltage level generations. So, these charging currents cause some extra power losses in these mentioned power switches. Therefore, to calculate the average value of the extra power losses (P_{C-Ext}) caused by C_2, we can write:

$$P_{C-Ext}=\frac{V_{on}}{T}\int_0^T \left|i_{Ch,C2}(t)\right| dt=\frac{V_{on}Q_{ext}}{T} \quad (16)$$

Where, Q_{ext} is the charge taken away from C_2 over a full cycle of the grid's frequency. Regarding the passing current waveform of C_2 in the third and fourth working zone shown in Fig. 6, Q_{ext} can be expressed as:

$$Q_{ext}=\int_{t_3}^{t_4}\left|i_g(t)\right|dt+2\times\int_{\frac{T}{2}}^{t_3}\left|d_2(t)i_g(t)\right|dt \quad (17)$$

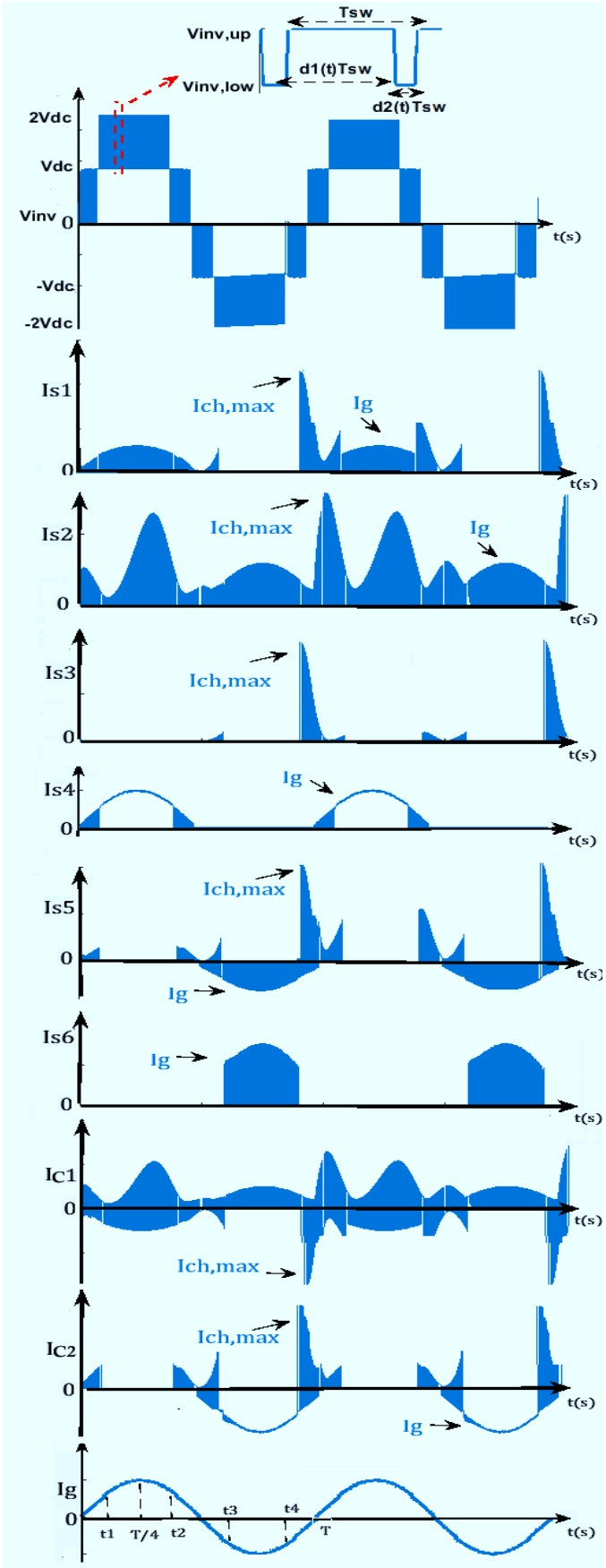

Fig. 6. Typical waveforms of the inverter's output voltage levels, current stress of the switches/capacitors alongside the injected grid current waveform.

Where, $d_2(t)$ is the normalized dwell time of the third working zone calculated by (10). So, (17) can be rewritten as:

$$Q_{ext} = I_m \left(\int_{\frac{T}{2}+t_1}^{T-t_1} \left|\sin(\omega t)\right| dt + 4D_m \int_{\frac{T}{2}}^{\frac{T}{2}+t_1} \left|\sin^2(\omega t)\right| dt \right) \quad (18)$$

Regarding (12), (13) and (16), P_{C-Ext} is obtained as:

$$P_{C-Ext} = \frac{V_{on} I_m}{2\pi} \left(2D_m \sin^{-1}\left(\frac{0.5}{D_m}\right) + \sqrt{1 - \frac{1}{4{D_m}^2}} \right) \quad (19)$$

Therefore, the overall conduction loss of a typical power switch like S_1 can be expressed as (20). The similar way can be also adopted for the extra charge of C_1 and in consequence for the extra conduction loss of S_2.

$$P_{C-T,S1} = \frac{V_{on} I_m}{2\pi} \left(1 + 2D_m \sin^{-1}\left(\frac{0.5}{D_m}\right) + \sqrt{1 - \frac{1}{4{D_m}^2}} \right) \quad (20)$$

B. Design Guidelines of the Passive Elements

B.1. Inductor Determination

In order to find the required value of the inductor interfacing between the proposed inverter and the grid, the inductor's current relation over a switching time period should be derived as follows:

$$i_g(t) = \int_0^{d_1 T_{Sw}} V_L(t) dt + i_g(0) \quad (21)$$

Where, $i_g(0)$ is the initial stored current of the inductor, and $V_L(t)$ is the voltage across of it which has to be obtained during the dwell time generating the upper level of the inverter's output voltage. So, considering the instantaneous current ripple of the inductor ($\Delta i_g(t)$), the following equation can be written:

$$\Delta i_{g,\max}(t) = \frac{(V_{inv,up} - V_g(t)) d_1(t)}{2 f_{sw,\min} L_g} \quad (22)$$

Since switching frequency is variable on the basis of the proposed PCC, so the worst case must be considered to reflect the maximum value of $\Delta i_g(t)$. Here, $f_{sw,\min}$ is defined as the minimum switching frequency of the proposed PCC strategy and can be readily found out by (2). Since the maximum value of the current ripple ($\Delta i_{g,\max}$) is taking place at the peak value of the grid's voltage ($V_{m,g}$), so regarding (22) and the equation of the dwell time of $d_1(t)$ in zone I provided by (8), the minimum required value of L_g for the proposed topology can be expressed as:

$$L_{g,\min} = \frac{8 D_m V_{dc} (2V_{dc} - V_{m,g}) + {V_{m,g}}^2}{16 D_m f_{sw,\min} V_{m,g} \Delta i_{g,\max}} \quad (23)$$

B.2. Capacitance Determination

To determine a correct value for the capacitance of the involved capacitors, the function of the grid's current in respect to the inverter's output power (P_{out}) injecting to the grid at the unity PF can be derived as follows:

Table IV. VA Rating of the Involved Power Switches in The Proposed Five-Level SC-Based Inverter

Power Switches	S_1	S_2	S_3	S_4	S_5	S_6
VA Stress	$4V_{dc}I_m$	$4V_{dc}I_m$	$6V_{dc}I_m$	$2V_{dc}I_m$	$8V_{dc}I_m$	$4V_{dc}I_m$

$$i_g(t) = \frac{P_{out}}{V_{dc} D_m} \sin(\omega t) \quad (24)$$

From the operating principle of the proposed five-level SC-based topology, it is evident that the capacitor C_2 plays an essential role in injecting the inverter's power to the grid since it should be in the injected grid's current flowing path for the negative half cycle of the grid's frequency (zone III and IV). Regarding the current flow path of the SC cell capacitor (C_1) during the positive half-cycle of the grid (Fig. 1 (c) and Fig. 1. (d)), it is revealed that it will be directly put in the injected grid's current flowing path once the inverter is working in Zone I. So, getting considered Zone I and IV as the longest discharged cycle (LDC) of C_1 and C_2, respectively and taking ΔV_{C1} and ΔV_{C2} as their voltage ripple during the time interval of $[t_2 - t_1]$ and $[t_4 - t_3]$ shown in Fig. 6, the following relations can be expressed:

$$\frac{1}{C_1} \int_{t_1}^{t_2} i_{C1}(t) = \Delta V_{C1} \quad (25)$$

$$\frac{1}{C_2} \int_{t_3}^{t_4} i_{C2}(t) = \Delta V_{C2} \quad (26)$$

Where, $i_{C1}(t)$ and $i_{C2}(t)$ are denoted as the passing current through the C_1 and C_2 during the operation in Zone I and IV, respectively. Regarding Table II and (8), such functions can be referred to the grid's current as (27) and (28):

$$i_{C1}(t) = d_1(t) i_g(t) = (2d(t) - 1) i_g(t) \rightarrow Zone\ I \quad (27)$$

$$i_{C2}(t) = i_g(t) \rightarrow Zone\ IV \quad (28)$$

Therefore, considering (25)-(28), the required capacitance of the capacitors can be obtained as follows:

$$C_1 = \frac{P_{out}}{V_{dc} \Delta V_{C1}} \left(\lambda + \frac{0.5T}{D_m \pi} \sqrt{1 - \frac{1}{4{D_m}^2}} \right) \quad (29)$$

$$C_2 = \frac{P_{out}}{V_{dc} \Delta V_{C2}} \left(\lambda + \frac{T}{D_m \pi} \sqrt{1 - \frac{1}{4{D_m}^2}} \right) \quad (30)$$

Where, λ is equal to $\frac{2T}{3}$ in respect to (12). From (29) and (30), it is revealed that owing to the series-parallel switching conversion of the SC cell's capacitor (C_1) and a chopped value of the grid current passing through C_1 described by (27), it can possess a much smaller capacitance than C_2.

C. Current and Voltage Stresses of Switches

In order to calculate the maximum current stress of the involved switches, the maximum value of the charging current of the capacitors should be identified. Considering all the involved resistance of the charging flow path including the Equivalent Series Resistor (ESR) of the C_1 and C_2 ($R_{\Sigma,C1}$ and

$R_{\Sigma,C2}$), the maximum value of the charging current of the capacitors can be expressed as (31):

$$i_{Ch,\max,Ci} = \frac{\Delta V_{Ci,\max}}{R_{\Sigma,Ci}} \quad i = 1,2 \tag{31}$$

Herein, the maximum charging current of C_1 directly affects the current stress of S_2 since it will be in the charging path of C_1 during the operation in Zone I. Also, as earlier mentioned, the current stress of the switches S_1, S_3 and S_5 are affected by $i_{Ch,\max,C2}$ when they are being involved into the charging path of C_2 during the zero output voltage level generation.

Now, having taken Fig. 6 into account and considered (31), the maximum current stresses of the switches can be taken as follows:

$$I_{S1,\max} = I_{S5,\max} = i_{Ch,\max,C2} + I_m \tag{32}$$

$$I_{S2,\max} = i_{Ch,\max,C1} + I_m \tag{33}$$

$$I_{S3,\max} = i_{Ch,\max,C2} \tag{34}$$

$$I_{S4,\max} = I_{S6,\max} = I_m \tag{35}$$

In following, to calculate the voltage stresses of the switches, their PIV rating will be important. Regarding the discussed operating principle of the proposed topology, the maximum PIV of the switches which can also reflect the maximum voltage stresses can be obtained as (36)-(38).

$$V_{S1,\max} = V_{S2,\max} = V_{dc} \tag{36}$$

$$V_{S3,\max} = V_{S4,\max} = V_{S5,\max} = 2V_{dc} \tag{37}$$

$$V_{S6,\max} = 4V_{dc} \tag{38}$$

In this case, by summing all the PIVs of the switches, the per unit scale of the total standing voltage (TSV) will be six. Hereby, in order to reflect a quantitative metric as for the above-mentioned current/voltage stresses of the switches, the product value of Volt/Ampere (VA) rating for each of the power switches and in turn the total Volt Ampere (TVA) rating of the switches can be calculated. Considering a 1kW ac power injected to a standard grid (50 Hz/311 V) and regarding the two times voltage boosting property of the proposed inverter, the minimum required value of the input voltage (V_{dc}) can be set on 160 V. So, with respect to (5), the maximum value of the modulation index (D_m) will be equal to 0.97. With hindsight to such parameters, the maximum current stresses of the capacitors will be about three times more than the maximum value of the injected current. Therefore, concerning (32)-(38), the VA rating of the involved power switches can be summarized in Table IV, where S_5 and S_4 respectively experience the highest and lowest value of VA. Regarding this, the TVA rating of the switches are also equal to $28V_{dc}I_m$.

V. COMPARATIVE STUDY

In order to compare the circuit architecture of the proposed five-level SC-based inverter over some other recently-introduced transformerless grid-connected inverters, a comparative study from different aspects is presented in this section. As shown in Table V, the comparative items include the number of required passive and active elements, minimum and maximum number of ON-state power switches at each instant, the reported value of the inductor size as the filter and the operating switching frequency, the minimum required value of the input voltage utilization, which can reflect the boosting feature of each structure based on a standard grid, maximum number of inverter's output voltage level, the value of the leakage current, the reactive power support ability and finally the rated efficiency reported in publication. Here, in the overall component count column, the input capacitor and the pre-assumed filter of each structure have also been considered. Also, since the TVA information of the other structures is not adequately available in the relevant literature, so their overall TSV and the maximum current stress rating of the switches for each structure have been considered as one of the comparative items. From Table V, it is clear that all the mentioned structures except the proposed topology and those presented in [23] and [24] possess only a buck-type feature; so more PV strings should be series there to regulate the maximum peak value of the grid's voltage. This issue can also affect the PIV and in turn the TSV of the involved switches.

Also, alongside the proposed topology, only five other structures cited as [11-13],[26], and [27] are able to generate five-level of the output voltage, while owing to use of diode instead of power switch in some switching states, [11] and [13] cannot theoretically handle the reactive power support mode. Herein, although the number of required components in these structures are the same with the proposed one, none of them offers any boosting feature. Five-level output voltage generation is a superiority to use the smaller size of the L-type filter, where other two or three-level-based topologies should employ higher order LC or LCL filter to inject a high quality current to the grid. Considering the 160 V as the minimum value of the required dc voltage for a 311 V standard grid and taking the 17 kHz and 20 kHz as the minimum and maximum switching frequency of the proposed PCC technique in 600 W application, the minimum required value of the inductor for the proposed topology will be around 2.3mH as can be calculated by (23). Here although there might be found some cases with smaller inductor size than the proposed topology, either their filter type is on the basis of LC or LCL filter or their switching frequency is higher than the proposed one. Regarding other mentioned five-level inverter structures, [11-13] use the midpoint clamping technique to reduce the leakage current, while the proposed topology and the presented structures in [26] and [27] have employed a common-grounded circuit that can guarantee almost zero leakage current injection.

Reduced number of ON-state power switches is another merit of the proposed topology over its other five-level structures counterparts. Since the operating principle of the mentioned structures during the generation of each level of the output voltage is different, so the minimum and maximum number of ON-state power switches are not the same. As for the proposed topology and at the worst condition, only three power switches are ON during the zero-level output voltage generation (maximum number of ON state power switches is three), whereas in the remaining states, this number is only two (minimum number of ON-state power switches). This feature can also highlight the low value of the conduction loss and in turn the acceptable rate of overall efficiency for the

Table V. A Comparative Summary Between the Proposed Topology and Different Transformerless Grid-Connected Structures

Type of Converter	No. of Components				Min/Max no. of ON-Switches	Inductor Size /Reported Switching Frequency	Required value of V_{in} /Boosting Feature	TSV /Maximum Current Stress	No. of Levels	Leakage Current	Reactive Power Support	Reported Rated Efficiency
	S	D	C	L								
[11]	6	2	2	2	2/4	1mH/20kHz	V_{dc} /NO	$6V_{dc}/I_m$	5	Low	NO	97.5%@2kW
[12]	6	2	2	1	2/2	1.6mH/15kHz	$2V_{dc}$ /NO	$6V_{dc}/I_m$	5	Low	Yes	NA@1kW
[13]	6	2	2	1	2/2	3mH/16kHz	V_{dc} /NO	$5V_{dc}/I_m$	5	Low	NO	97.8%@400W
[14]	5	-	2	1	2/3	8mH/20kHz	V_{dc} /NO	$5V_{dc}/4I_m$	3	Zero	Yes	95%@500W
[15] (Type I& II&III)	5	0	2	1	2/3	4mH/20kHz	V_{dc} /NO	$5V_{dc}/4I_m$	3	Zero	Yes	98%@600W
[16]	5	2	2	2	2/3	5mH/12kHz	V_{dc} /NO	$5V_{dc}/6I_m$	3	Low	NO	97%@1kW
[17]	4	2	4	2	2/2	4mH/24kHz	V_{dc} /NO	$4V_{dc}/4I_m$	3	Zero	Yes	97.2%@500W
[19] Type I&II	4	1	3	1	2/2	0.35mH/50kHz	V_{dc} /NO	$4V_{dc}/3I_m$	3	Zero	Yes	99.1%@800W
[19] Type III	4	-	3	1	1/2	0.8mH/16kHz	V_{dc} /NO	$6V_{dc}/4I_m$	3	Zero	Yes	96%@800W
[23]	5	-	2	2	2/2	0.3mH/20kHz	$0.5V_{dc}$ /Yes	$5V_{dc}/4I_m$	3	Zero	Yes	92.5%@200W
[24]	4	-	3	3	2/2	0.2mH/50kHz	$0.5V_{dc}$ /Yes	$6V_{dc}/3I_m$	2	Zero	Yes	95.7%@300W
[26]	6	-	3	1	3/3	8mH/15kHz	V_{dc} /NO	$6V_{dc}/I_m$	5	Zero	Yes	97%@1kW
[27]	6	1	3	1	3/3	2mH/12kHz	V_{dc} /NO	$6V_{dc}/4I_m$	5	Zero	Yes	95.8%@1.2kW
Proposed	6	1	3	1	2/3	2.3mH/20kHz	$0.5V_{dc}$ /Yes	$6V_{dc}/4I_m$	5	Zero	Yes	98.1%@600W

TABLE VI. Prototype Parameters

Element	Type	Description
All Switches except S_3/S_3	BUPD314/ BUP314	1200V/52A
Gate Driver	TLP 250	IC
Power Diode	MUR1560	600V/15A
Current Transducer	LA55P	Hall Effect
Microcontroller	Beagle Bone Black	ARM
Local Grid's Frequency	50 Hz	-
Sampling/Max Switching Frequency	40 kHz/20 kHz	-
C1 & C2	SMM Series	$0.47mF$ & $1mF$
Magnetizing Inductor	Ferrite Core	$2.3mH$

proposed topology in contrast to others. It is also worth noting that the suggested five-level inverter topologies in [26] and [27] demand a pre-charged circuit procedure with extra voltage sensors for assurance of the capacitors balancing issue, while such concern is quite alleviated by using the series-parallel switching conversion of the SC cell in the proposed topology.

VI. Experimental Verifications

In this section, some experimental results through a laboratory built prototype shown in Fig. 7 are given to reconfirm the feasibility and correctness of the proposed topology. Herein, a PV simulator with the fixed dc link voltage of 180 V is used as the input dc source. Table VI indicates the prototype parameters of the experimental study. Here, the peak of the local grid is 311 V and the passive elements' values are chosen based on the presented design guidelines of section IV. To avoid any computational burden, a hardware-based PLL technique is used to obtain the synchronous phase value of the reference current in the proposed PCC strategy. Regarding these noted notions, the five-level inverter's output voltage besides the injected grid's current and the local grid's voltage waveforms can be observed in Fig. 8(a) and (b), respectively. Here, the maximum value of the inverter's output voltage and the injected current are 360 V and 3.8 A, respectively, which can reflect the boosting feature of the proposed system with about 590 W output power. To show the correct value of the injected active power, the grid's voltage and current have been shown in Fig. 8 (c). From these results, it is clear that the proposed topology with its PCC-based strategy could properly generate all the supposed output voltage levels with appropriate quality of the injected current. Herein, to verify the balanced voltage waveforms of the involved capacitors, the voltage across the C_1 and C_2 is captured and they can be seen by Fig. 8 (d). As shown from this result, they could be balanced at 180 V and 360 V, respectively.

To attest the reactive power support capability of the proposed topology, a phase-shift (lead and lag) in the phase of the reference current has been applied. Considering the operating principle of the proposed PCC technique at the non-unity PF discussed earlier, the logical algorithm for triggering the switches has to be changed based on Table III.

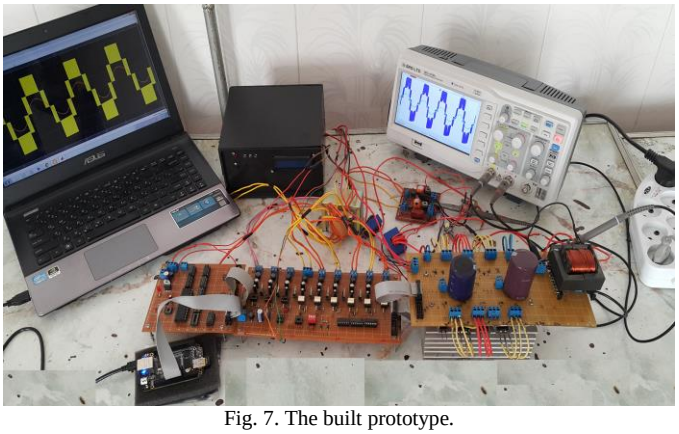

Fig. 7. The built prototype.

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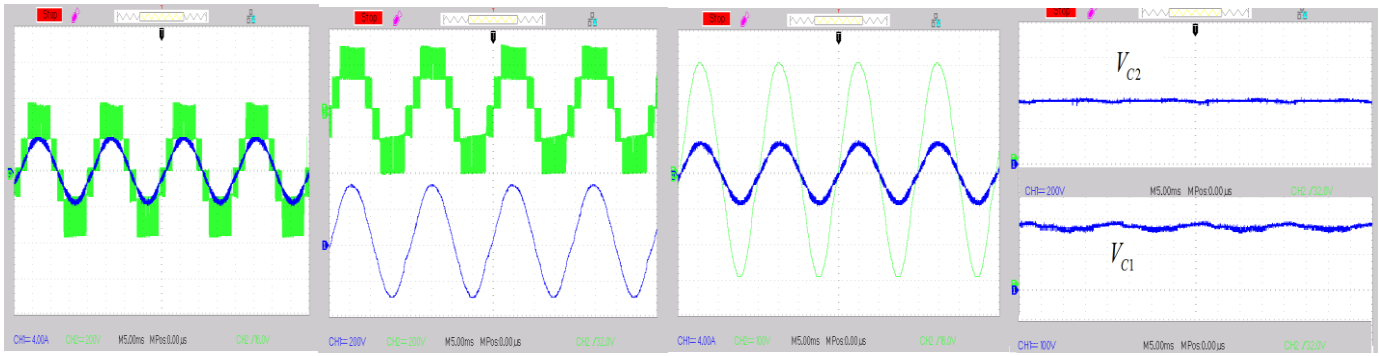
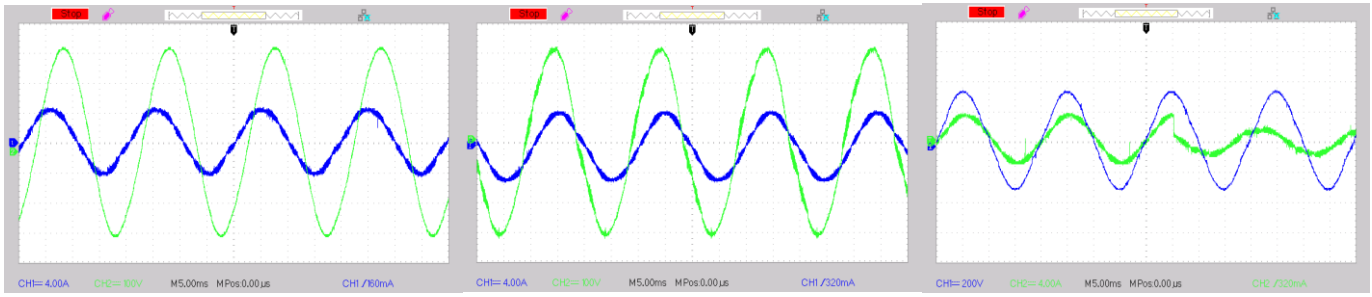


(a) (b) (c) (d)

Fig. 8. (a) Inverter's output voltage (200 V/div) and the injected grid's current (4 A/div) (b) Inverter's output voltage (200V/div) and the local's grid voltage (200V/div) (c) Injected grid's current (4A/div) and local grid's voltage (100 V/div) (d) the voltage across C_2 (200V/div) and the voltage across C_1 (100V/div).

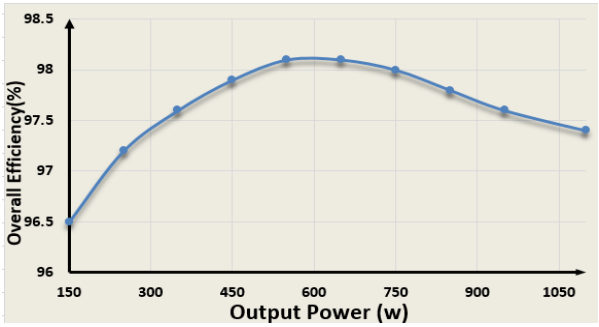


(a) (b) (c)

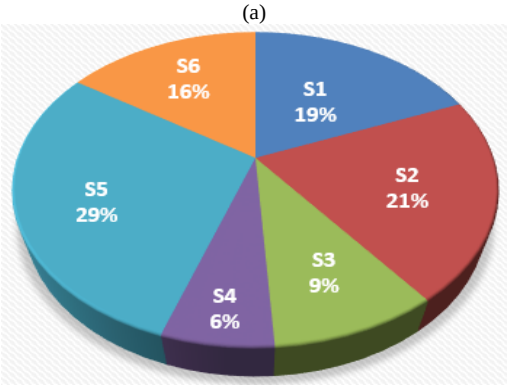
Fig. 9.(a) The leading injected grid's current (4 A/div) with the grid's voltage (100 V/div) (b) The lagging injected grid current (4 A/div) with the grid's voltage (100 V/div) (c) The grid's voltage (blue trace) (200 V/div) and the injected grid current (green trace) (4 A/div) under the step-change of the PF from unity to a non-unity one.

The robust performance of the proposed system in delivering a high quality of the injected grid current can be seen in Fig. 9 (a) and (b). Also, to show the fast and accurate performance of the proposed PCC technique in tracking the desired reference current, the dynamic result of grid's voltage and injected current waveforms from unity PF (active power support mode) to a non-unity one (reactive power support mode) can be readily observed in Fig. 9 (c). Here the overall THD of the injected current is about 1.63% which can properly meet the IEEE standard/power quality grid code. Herein, through measuring the input and output powers of the inverter by the power analyzer, the overall efficiency would be around 98.1%. The variations of the overall efficiency versus a wide range of the output power can be also seen in Fig. 10 (a), while the percentage of losses distribution among different power switches conducted based on the theoretical analysis at the rated power (600 W) can be observed in Fig. 10 (b). Here, S_5 and S_4 that are tolerating the highest and lowest TVA, respectively, impose the maximum and minimum rate of losses among the others as depicted in Fig 10 (b).

In following, to further confirm the theoretical analysis of the voltage and current stresses, the experimental waveform of the capacitors' current is demonstrated in Fig. 11. As is clear, the passing current through the C_2 in the negative half-cycle is quite accorded with the grid's injected current, while its maximum charging current that is about three times more than the I_m can be seen at the beginning of the positive and the negative half-cycle (during the zero output voltage generation in Zone II and III).



(a)



(b)

Fig. 10. (a) Variation of overall efficiency versus the output power (b) losses distribution (%) among different switches at 600 W output power.

In this case, C_1 is charged/discharged in Zone I and II; so such maximum value of the charging current can be also observed in positive half-cycle of the passing current waveform of C_1.

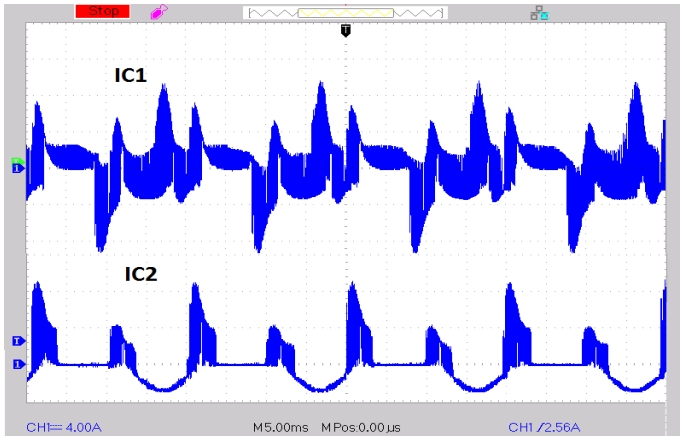


Fig. 11. The measured current waveform through C_1 and C_2 (4 A/div).

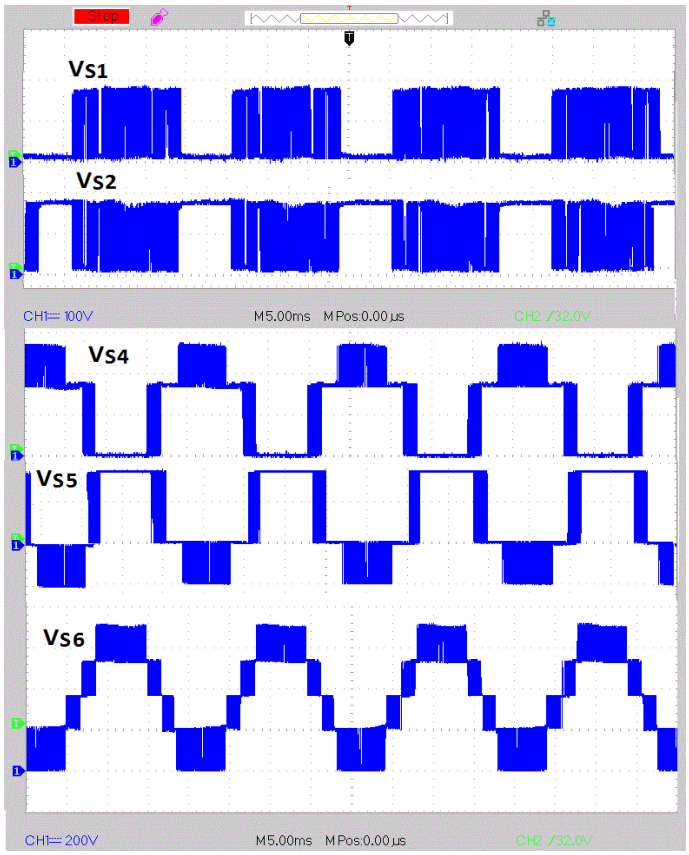


Fig. 12. The measured PIV of power switches; S_1 / S_2 (100 V/div) and $S_4 / S_5 / S_6$ (200 V/div).

On the contrary, to further validate the calculated voltage stresses of the switches, their PIV has been captured by the experiment. Considering Fig. 12, it is clear that the SC cells switches (S_1 / S_2) must tolerate the minimum PIV (180 V), whereas the maximum PIV of S_4 and S_5 is equal to 360 V. As can also be seen the PIV of S_5 shows a bi-directional value, while by adding the voltage across C_2 to the five-level output voltage of the inverter, S_6 indicates the maximum PIV among all the power switches (720 V). Here, the PIV of S_3 has not been depicted since it is quite the same as the inverter's output voltage waveform with the peak of 360 V. The current stresses result of all the power switches can also be observed in Fig. 13 (a)-(c). As can be realized, the results can properly verify the theory provided in Fig. 6. Here S_1 and S_5 that are involved into the charging path of C_2 are carrying almost the same shape of the current stress but with opposite polarity. In this case, S_4 and S_6 (minimum and maximum PIV holder) experience the grid's current waveform shape as their current stresses. So as depicted in Fig. 10 (b), their losses are reasonable. Herein, as for the 3.8 A peak value of the injected current, the maximum current stresses of the switches S_1, S_2 and S_5 is around 15 A which is in agreement with (32) and (33), while S_3 carries only the peak value of the charging current of C_2 (almost 12 A). Finally, in order to confirm the robust and fast dynamic performance of the proposed system with PCC technique, a step change in the peak value of the local grid's voltage is applied (from 1 p.u to 0.8 p.u). So, from Fig. 14 (a) it can be seen that to make a constant injected power to the grid, the amplitude of the reference current of the proposed PCC is jumped from about 3.2 to 4A and in turn the value of the injected current is affected. The balanced voltage waveforms of both the capacitors under this dynamic condition can also be observed by Fig. 14 (b) and (c), where the voltage of C_1 and C_2 are fixed at 180 V and 360 V irrespective of the step change in the peak value of the local grid's voltage.

VII. Conclusion

A new five-level SC-based transformerless grid-connected inverter has been presented in this study. The proposed topology is able to remove the leakage current concern with a common-grounded architecture. Also, with the reasonable number of active and passive involved elements, it offers a two times voltage boosting feature that makes it suitable for PV string applications. A PCC-based strategy has also been employed in following to regulate the value of the injected current. Details of such a controlled system besides some analysis as for the conduction losses, the design guidelines and voltage/current stresses of the switches were also given to further explore the performance of the proposed topology. Finally, a comprehensive comparative study alongside the experimental results of a 590 W built prototype have been presented to confirm the superiority and accurate operation of the proposed system.

References

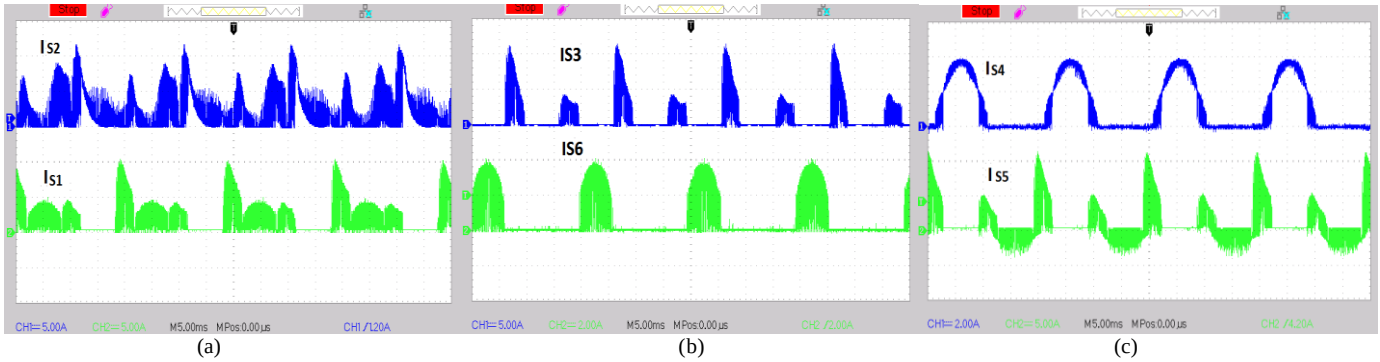
[1] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phasegrid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Applicat.*, vol. 41, no. 5, pp. 1292-1306, Sep./Oct. 2005.

[2] M. Islam, S. Mekhilef, M. Hasan, "Single phase transformerless inverter topologies for grid-tied photovoltaic system: A review," *Renewable and Sustainable Energy Reviews*, vol. 45, pp. 69-86, 2015.

[3] H. Xiao and S. Xie, "Leakage current analytical model and application in single-phase transformerless photovoltaic grid-connected inverter," *IEEE Trans. Electromagn. Compat.*, vol. 52, no. 4, pp. 902–913, Nov. 2010.

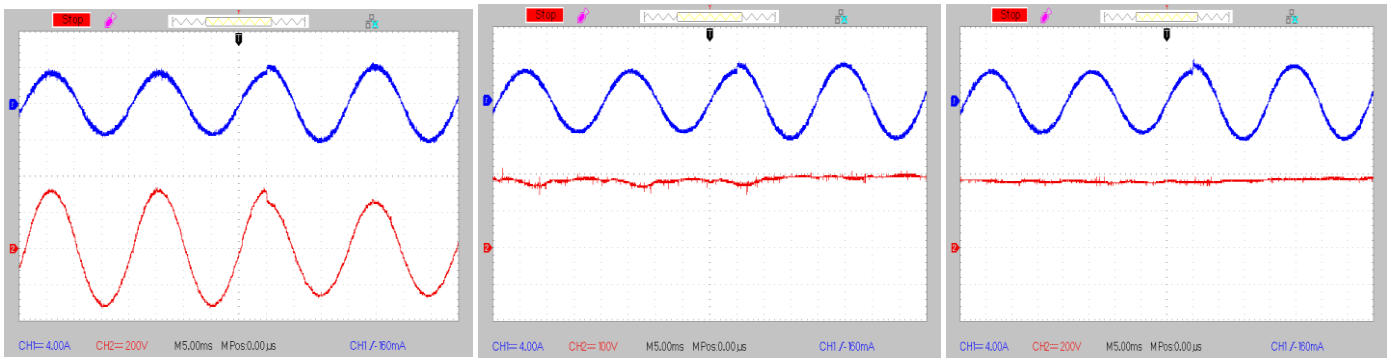
[4] D. Meneses, F. Blaabjerg, Ó Garcia, and Jo ´ se A. Cobos, "Review ´and comparison of step-up transformerless topologies for photovoltaicAC-module application," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2649–2663, Jun. 2013.

[5] S. Saridakis, E. Koutroulis, F. Blaabjerg, "Optimization of SiC-Based H5 and Conergy-NPC Transformerless PV Inverters," *IEEE Emerg. Select. Topics Power Electron.,* vol. 3, no. 2, pp. 555-567, June. 2015.



(a) (b) (c)

Fig. 13. The current stress waveforms of (a) S_1 (5 A/div) and S_2 (5 A/div), (b) S_3 (5 A/div), and S_6 (2 A/div) (c) S_4 (2 A/div) and S_5 (5 A/div).



(a) (b) (c)

Fig. 14. Dynamic performance of the proposed system under a voltage sag in the local grid's voltage (a) The injected current (blue trace) (4 A/div) and the local grid's voltage (red trace) (200 V/div) (b) The injected current (4 A/div) and the voltage across C_1 (100 V/div) (c) The injected current (4 A/div) and the voltage across C_2 (200 V/div).

[6] J. Ketterer, H. Schmidt, C. Siedle, "Inverter for transforming a DC voltageinto an AC current or an AC voltage," Europe Patent 1 369 985 (A2), May 13, 2003.

[7] H. Xiao, S. Xie, Y. Chen, and R. Huang, "An optimized transformerless photovoltaic grid-connected inverter," *IEEE Trans. Power Electron.*, vol. 58, no. 5, pp. 1887–1895, May 2011.

[8] B. Ji, J. Wang, and J. Zhao, "High-efficiency single-phase transformerless PV H6 inverter with hybrid modulation method," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 2104–2115, May 2013.

[9] B. Yang, W. Li, Y. Gu, W. Cui, and X. He, "Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system," *IEEE Trans. Power Electron.*, vol. 27, no.2, pp. 752–762, Feb. 2012.

[10] S. A. Arshadi, B. Poorali. E. Adib, and H. Farzanehfard "High step up dc-ac converter suitable for ac module applications," *IEEE Trans. Industrial. Electron.*, vol. 63, no. 2, pp. 832-839, Feb. 2016.

[11] G. Buticchi, E. Lorenzani, and G. Franceschini, "A Five-level single phase grid-connected converter for renewable distributed systems"*IEEE Trans. Ind Electron.*, vol. 60, no.3, pp. 906–918, Mar. 2013.

[12] H. Wang, L.Kou, Y-F.Liu, and P. C. Sen "A new six-switch Five-level active neutral point clamp inverter for PV applications'' IEEE, Trans. Power Electron, vol 32, no. 9, pp.6700-6715, Sep. 2017.

[13] G. E. Valderrama, G. V. Guzman, E. I. Pool-Mazún, P. R. Martinez-Rodriguez, M. J. Lopez-Sanchez, and J. M. S. Zuñiga, "A single phase asymmetrical T-type five-level transformerless PV inverter," *IEEEJournal of Emerging and Selected Topics in Power Electronics,* vol. 6, no. 1, pp. 140–150, March 2018.

[14] Y. Gu, W. Li, Y. Zhao, B. Yang, C. Li, and X. He, "Transformerless inverter with virtual dc bus concept for cost-effective grid-connected PV power systems," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 793-805, Feb. 2013.

[15] Z. Liao, C. Cao, D. Qiu, and C. Xu, "Single-Phase Common-Ground-Type Transformerless PV Grid-Connected Inverters'' *IEEE Access*, vol. 7, pp. 63277-63287, Apr. 2019

[16] M. Gommeringer, F. Kammerer, A. Schmitt, and M. Braun, "A transformerless single-phase PV inverter circuit for thin-film or back-side contacted solar modules," in *Proc. IEEE IECON 2014*, pp. 1148-1153, Nov. 2014.

[17] J. F. Ardashir, M. Sabahi, S. H. Hosseini, F. Blaabjerg, E. Babaei and G. B. Gharehpetian, "A Single-Phase Transformerless Inverter with Charge Pump Circuit Concept for Grid-Tied PV Applications," *IEEE Trans. Ind. Electron.*, doi. 10.1109/TIE.2016.2645162, Nov. 2016.

[18] S. U. Hasan, B. Shaffer, H. A. Hassan, M. J. Scott, Y. Siwakoti, and G. Town, ''Common-Ground Transformerless Inverter for Solar Photovoltaic Module'' *2018 IEEE Applied Power Electronics Conference and Exposition (APEC),* Apr. 2018.

[19] Y. Siwakoti and F. Blaabjerg "Common-ground-type transformerless inverters for single-phase solar photovoltaic systems'' *IEEE Trans. Ind Electron.*, vol. 65, no.3, pp. 2100-2111, Marc. 2018.

[20] T. T. Tran, M. K.Nguen, Y. C. Lim, and J. H. Choi, '' A Single Phase Quasi H-Bridge Boost Inverter with Common Ground for Grid connected Applications'' *IOP Conference Series: Earth and Environmental Science, Volume 159, conference 1.* 2018.

[21] J. F. Ardashir, M. Sabahi, S. H. Hosseini, E. Babaei and G. B. Gharehpetian, ''A Grid Connected Transformerless Inverter and its Model Predictive Control Strategy with Leakage Current Elimination Capability'' *Iranian Journal of Electrical and Electronic Eng,* vol. 13, no. 2, pp. 161-169. Jun. 2017.

[22] N. Vázquez, M. Rosas, C. Hernández, E. Vázquez, and F. Perez-Pinal, "A New Common-Mode Transformerless Photovoltaic Inverter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 10, pp. 6381-6391, April. 2015.

[23] M. T. Azari, M. Sabahi, E. Babaei and F. A. A. Meinagh. "Modified single-phase single-stage grid-tied flying inductor with MPPT and suppressed leakage current," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 221-231, Jan. 2018.

[24] A. Kumar and P. Sensarma, "A 4-Switch single-stage single-phase buck-boost inverter," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5282- 5292, Jul. 2017.

[25] L. C. Breazeale and R. Ayyanar, "A Photovoltaic Array Transformer-Less Inverter With Film Capacitors and Silicon

Carbide Transistors," *IEEE Transactions On Power Electronics*, Vol. 30, Issue 3, pp. 1297 – 1305, March 2015.

[26] A. Kadam and A. Shukla, "A multilevel transformerless inverter employing ground connection between PV negative terminal and grid neutral point," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 8897–8907, Nov 2017.

[27] F. B. Grigoletto, "Five-level transformerless inverter for single-phase solar photovoltaic applications" *IEEE Emerg. Select. Topics Power Electron.,* 10.1109/JESTPE.2019.2891937.

[28] Y. H. Shin, P.J. Sik , P. K. Bum, B. J. Li and M. G. Woo, "A Digital Predictive Peak Current Control for Power Factor Correction With Low-Input Current Distortion," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 900–912, 2016.

[29] Davoodnezhad, R.; Holmes, D. G.; McGrath, B. P; "A Three-Level Self-Synchronizing Hysteresis Current Regulator with Constant Switching Frequency" *Energy Conversion Conference ECCE Asia Downunder, Aug 2013.*

[30] C.N.M. Ho, V. S. S. Cheung, and H.S.H. Chung; "Constant-frequency hysteresis current control of grid-connected VSI without bandwidth control'' *IEEE Transactions on Power Electronics*, vol. 24, no. 11, pp. 2484–2495, Nov 2009.

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