A Fast and Robust DC-Bus Voltage Control Method for Single-Phase Voltage-Sourced DC/AC Converters

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Abstract: **This paper presents a fast and robust dc-bus voltage control method for improving the performance of single-phase grid-connected dc/ac converters. The proposed technique precisely estimates the double-frequency (2-f) ripple of a dc-bus voltage and removes it from the voltage control loop without adding any additional dynamics or oscillations. Conventionally, the 2-f ripple is managed by using large capacitors which increase the cost and bulkiness of a converter. As a state-of-the-art approach, a notch filter (NF) or a dc-voltage estimator is used to effectively block the 2-f ripple from the voltage control loop that can significantly reduce the capacitor size. However, such an approach introduces new dynamics in the control loop and causes additional oscillations on the bus voltage and increases the settling time of its response. This limits the degrees of freedom of the design to improve the overall system's damping. The proposed method in this paper estimates and removes the 2-f ripple without adding any additional modes (or poles) into the voltage control loop, thus it has no adverse impact on the original bus voltage dynamic response. While the proposed method is used, the dc-bus voltage control can be designed with higher speed and robustness and the whole system can operate with an enhanced transient at both the dc-bus voltage and the output ac current. The performance of the proposed approach is thoroughly analyzed, and its effectiveness is validated through simulations and experimental results.**

***Index Terms*—Double-frequency ripple, dc extraction, single-phase dc/ac converter, notch filter.**

I. Introduction

Grid-interconnection of low-power converter-based devices such as solar photovoltaic (PV) generators, single-phase electric-vehicle (EV) chargers and low-power rectifiers requires employment of single-phase voltage-sourced converters (VSCs) with adequate controls to properly respond to the input/output power exchange and voltage level [1-3]. The VSCs can also participate in grid ancillary services such as reactive power support, harmonics reduction and/or voltage regulation [4-6].

A typical control system of single-phase grid-connected VSC comprises an outer voltage-control loop which is responsible for controlling the dc-bus voltage and an inner current-control loop that is used to control the grid-side current. The design of the control system for a single-phase VSC can become challenging, partly due to the double-frequency (2-f) ripple of the dc-bus voltage which is a natural byproduct of the single-phase ac/dc power conversion [7]. While the 2-f is not removed, it can circulate from the outer

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voltage control loop into the inner current control loop through its input reference signal. As a result, such a disturbance appears on the grid-side current as a third harmonic and also as a shift from desired reactive power [8].

A conventional practice is to increase in the size of passive bus component (dc-bus capacitor) that acts as an energy storage for the grid-side 2-f power. The dc-bus capacitor decouples the pulsation of the grid-side power and limits the amplitude of the 2-f ripple within an acceptable range. Although, this hardware-based solution is effective, it decreases the lifetime, and increases the cost and bulkiness of the converter [9, 10]. As another alternative, an auxiliary circuit is used that draws constant current from the input and creates a high dc voltage to provide the needed pulsation at the output [10-13]. However, this method decreases the efficiency and increases the complexity of both the hardware and the control system.

A state-of-the-art approach is to use a software-based filter in the voltage control loop. The filter prevents the 2-f ripple from penetrating into the control loop and spoiling its variables; without an unnecessary increase in the size of the dc-bus capacitor and complicating the hardware [14, 15]. For instance, a second order low-pass filter (LPF) is used in the voltage control loop of a two-stage EV charger in [5]. The LPF appears to effectively attenuate the 2-f ripple, however, its operation exhibits a low convergence rate [15]. A third-order filter as a dc-observer is introduced in [15] which operates with higher convergence speed. Nevertheless, this method has the drawback of high transient during a quick bus-voltage variation which may be caused by its redundant structure, i.e. using three differential equations for a system which can be designed at order of two. As another approach, a second-order notch filter (NF) is used to block the 2-f ripple from the voltage control of a single-phase VSC [14]. The NF exhibits an optimum response, higher convergence rate and lower transient compared with the other two aforementioned filters. Accordingly, the NF can be considered as the state-of-the-art to tackle the 2-f ripple in a bus-voltage control loop.

Although the steady-state performances of the above-mentioned filters are acceptable, the bus-capacitor size can be reduced substantially using an additional filter means adding more modes (poles) into a voltage control loop. This can produce extra inevitable overshoots, oscillations and settling time and thus limit the flexibility of the design to improve the overall system damping. Consequently, the voltage control loop is forced to be designed with lower bandwidth in order to maintain the system transients within an acceptable range. This issue, which is not addressed in the literature, is the focus of this paper.

This paper proposes a novel idea of removing the 2-f ripple without adding any additional filter to the bus voltage control loop, nor any extra overshoots, oscillations and settling time to the control process. The novel dc-bus voltage control method is based on estimating and removing the 2-f ripple of the bus voltage through exploiting the operating system parameters and variables. Accordingly, the dynamic response of the bus voltage is not affected, and a much higher bandwidth can be achieved. The proposed method is simple in structure and shows a superior robustness and transient response (at both the dc-bus voltage and the output ac

current) compared with the listed conventional bus-voltage control methods. The performance and damping improvement of the proposed approach is investigated and confirmed by analysis, computer simulations and experimental results.

II. Conventional Bus-voltage Control Loop

Figure 1 presents a typical diagram of a single-phase grid-connected device including the VSC, the dc side source or load, the dc bus capacitor, the grid side inductor, and the grid. Figure 2 shows two conventional control structures for the VSC. Each one has an outer bus voltage control loop and an inner current control loop. The two common current-control strategies are proportional-resonant (*PR*) controller in time domain and proportional-integrating (*PI*) controllers in synchronous or direct-quadrature (*DQ*) domain [16, 17].

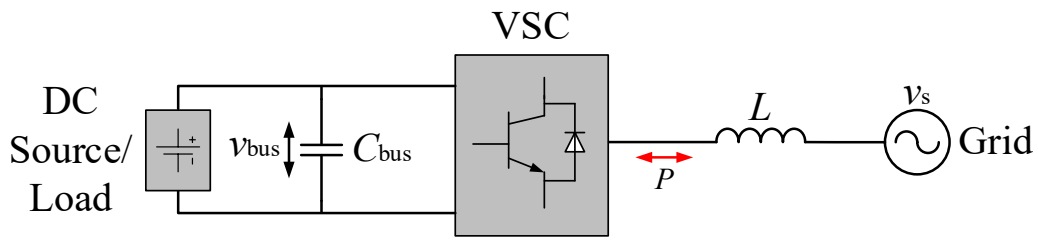


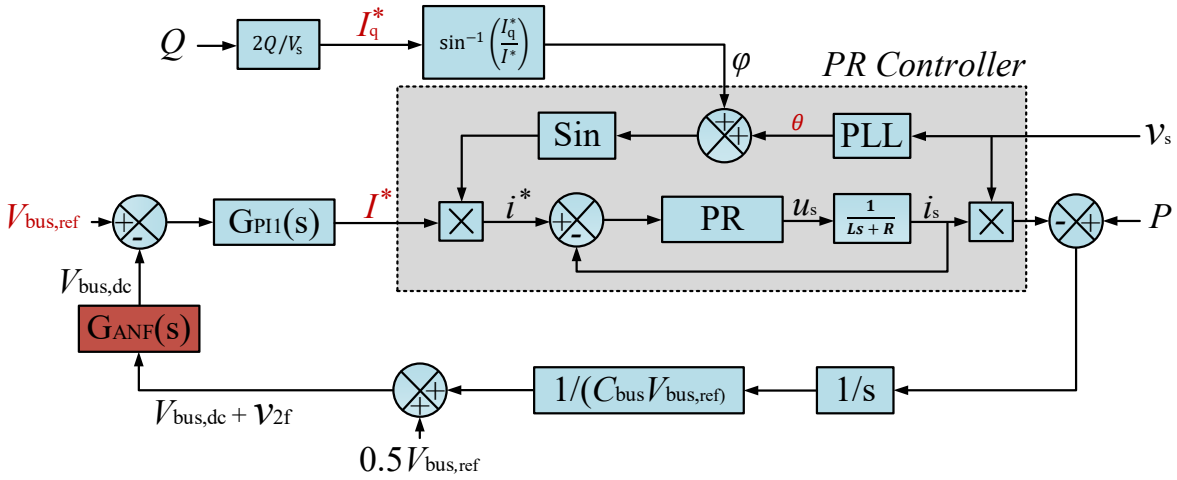
Fig. 1. Typical structure of a single-phase converter-based grid-connected device.

In Fig. 2(a), the outer bus voltage control loop generates the reference signal I^* (which is ideally dc) for the inner current control loop. This reference is multiplied into a sinusoidal signal which is properly synchronized by the PLL (phase-locked loop) output angle θ plus the phase angle φ (the required phase shift for reactive power). This forms the reference i^* for the internal *PR* current controller. As shown, the phase shift φ is calculated from I_q^* which is a user defined parameter and used to command a certain amount of reactive power required for inductive/capacitive operation of the converter. For a unity power factor operation, φ is zero.

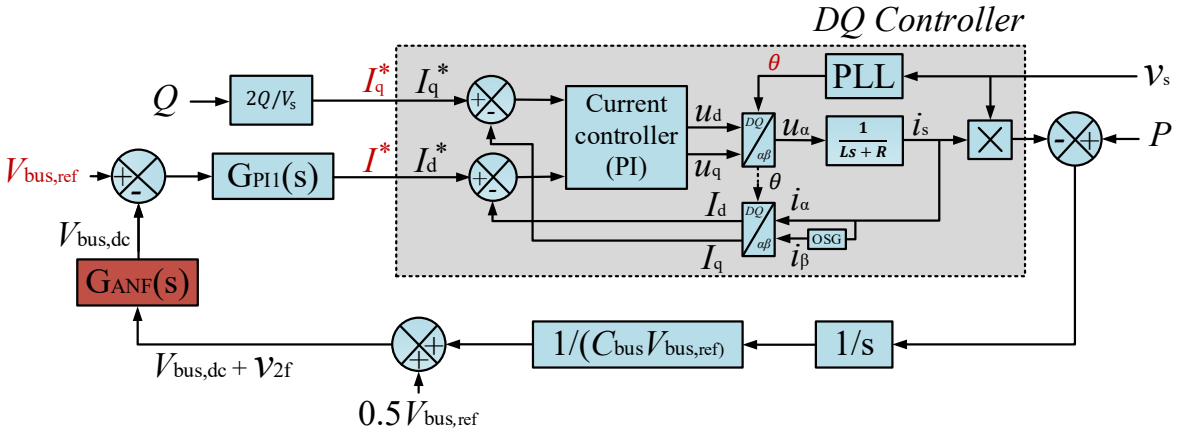
Figure 2(b) presents the block diagram of the VSC control when the internal current control approach is the *PI* or *DQ s*trategy. According to this method, the measured grid-side current i_s is transformed to *DQ* frame, I_d and I_q using the PLL angle. Then I_d and I_q are compared with the two reference signals I_d^* and I_q^*, and the output errors are regulated to zero by the two *PI* controllers. As shown in Fig. 2(b), I_d^* is directly supplied by the outer bus voltage control loop while I_q^* is a user-defined value and commands a certain amount of reactive power required for inductive/capacitive operation of the converter.

The NF on the bus voltage feedback loops in both Figures 2(a) and 2(b) removes the 2-f ripple v_{2f} from the voltage control loop. This allows reduction of C_{bus} without distorting the current reference. However, this tightens the limits of the controllers` (particularly $G_{PI_1}(s)$) design and control bandwidth due to adding additional filter $G_{ANF}(s)$ which adds extra dynamics into the control loop and causes oscillatory responses during sharp transients.

According to the proposed idea in this paper, the 2-f ripple v_{2f} can be eliminated without adding an extra filter to the feedback loop. The references I^* (the output of the bus voltage control loop), $V_{bus,ref}$ (the reference value of the bus voltage), I_q^* (the output of the reactive power controller) and θ (PLL`s output) which are shown by red color and are common in both control systems (Fig. 2(a) and Fig. 2(b)) are used in a proposed algorithm to estimate $v_{2f}(t)$. Then using a simple subtraction, $v_{2f}(t)$ can be removed



(a)



(b)

Fig. 2. Block diagram of a grid-connected VSC control. a) Inner *PR* current controller, b) inner *PI* current controller.

from the feedback loop. As a result, $G_{ANF}(s)$ which is a second-order filter can be eliminated from the feedback loops and the whole control system can be redesigned with a higher bandwidth.

III. Proposed Bus-Voltage Control Loop

A. Derivation of the proposed dc-extraction method

An actual bus voltage can be dominantly modelled as:

$$V_{bus}(t) = V_{bus,dc} + v_{2f}(t) \qquad (1)$$

in which $V_{bus,dc}$ is the dc offset and $v_{2f}(t)$ is the 2-f ripple as expressed by:

$$v_{2f}(t) = V_{2f}\sin(2\theta + \varphi) \qquad (2)$$

where φ is the phase shift between the grid voltage and current and θ is the grid voltage phase angle.

In (2), V_{2f} which is the amplitude of the 2-f ripple can be expressed as:

$$V_{2f} = \frac{S}{2C_{bus}\omega V_{bus,ref}}. \qquad (3)$$

where C_{bus} is the bus capacitance, $V_{bus,ref}$ is the reference value of the bus voltage, and $S = \sqrt{P^2 + Q^2}$ is the transferred ac apparent power, where P and Q are the active and reactive powers.

In the control systems of a VSC which are shown in Figures 2(a) and 2(b), the output signal of the outer bus voltage control loop I^* and I_q^* can be used to estimate the 2-f ripple of the bus voltage $v_{2f}(t)$ (i.e., $\hat{v}_{2f}(t)$) as:

$$\hat{v}_{2f}(t) = \frac{\sqrt{\hat{P}^2 + \hat{Q}^2}}{2C_{bus}\omega V_{bus,dc}}\sin(2\psi + \gamma) \qquad (4)$$

where

$$\hat{P} = \frac{1}{2}V_s I^*,\ \hat{Q} = \frac{1}{2}V_s I_q^*,\ \gamma = \sin^{-1}\left(\frac{I_q^*}{I^*}\right). \qquad (5)$$

The PLL is used to estimate the grid-side voltage phase angle [18, 19]. When the PLL operates in steady-state mode, ψ in (4) will become equal to θ in (2). The PLL also supplies V_s which is the peak value of the gird voltage. Moreover, as the *PR* in Fig. 2(a) and the two *PI* controllers in Fig. 2(b) eliminate the steady-state errors between the measured and reference signals, eventually $\hat{v}_{2f}(t)$ becomes equal to $v_{2f}(t)$. Therefore, the proposed method uses I^*, I_q^*, V_s, $V_{bus,ref}$ and θ to estimate $\hat{v}_{2f}(t)$ and thus (1) is rearranged in the form of (6) to extract $V_{bus,dc}$ from $v_{bus}(t)$ as:

$$V_{bus,dc} = V_{bus}(t) - \hat{v}_{2f}(t). \qquad (6)$$

The block diagram of the proposed method is shown in Fig. 3

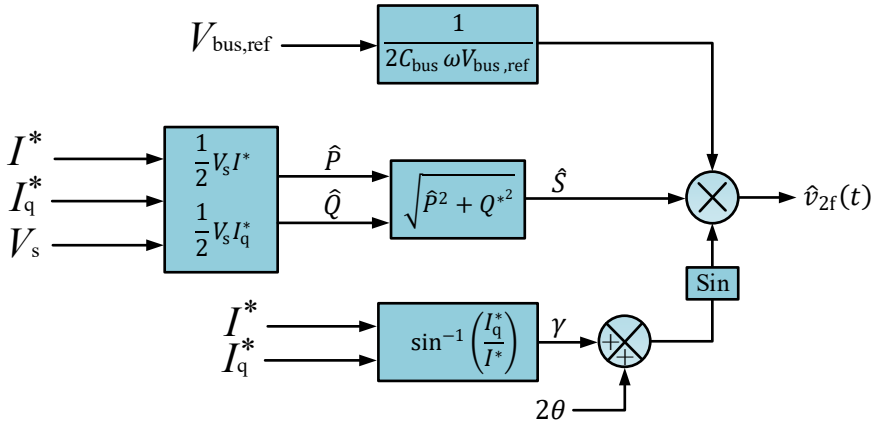


Fig. 3. Block diagram of the proposed dc-extraction method.

According to the proposed dc-extraction algorithm (Fig .3) and the VSC control structures in Figures 2(a) and 2(b), the operation of the proposed method is independent of the type of the internal current controller (*PR* controller or *DQ* controller). However, in this paper, the system in Fig. 2(b) is implemented and the proposed algorithm (Fig. 3) is applied and tested accordingly.

IV. Design Aspects of Proposed and Conventional NF-based Approaches

A. Studied system

Figure 4 shows a simplified linear time invariant (LTI) model of a VSC controller that includes the voltage-control loop, and the current-control loop (*D*-axis) and the plant which represents a single-phase grid-connected VSC with an *L* filter. The inner current control loop is shown by L_1 and the whole control loop is presented by L_2. This model is used in this paper to design to inner current control loop, the outer voltage control loop using conventional NF (Fig. 4(a)), and the outer voltage control loop using proposed dc-extraction method (Fig. 4(b)). G_{ANF} in Fig. 4(a) represents the transfer function of the second order NF as given by:

$$G_{\mathrm{ANF}}(s) = \frac{s^2 + 4\omega^2}{s^2 + 4\zeta\omega s + 4\omega^2} \qquad (7)$$

where ζ is the damping ratio of poles and ω is the angular frequency.

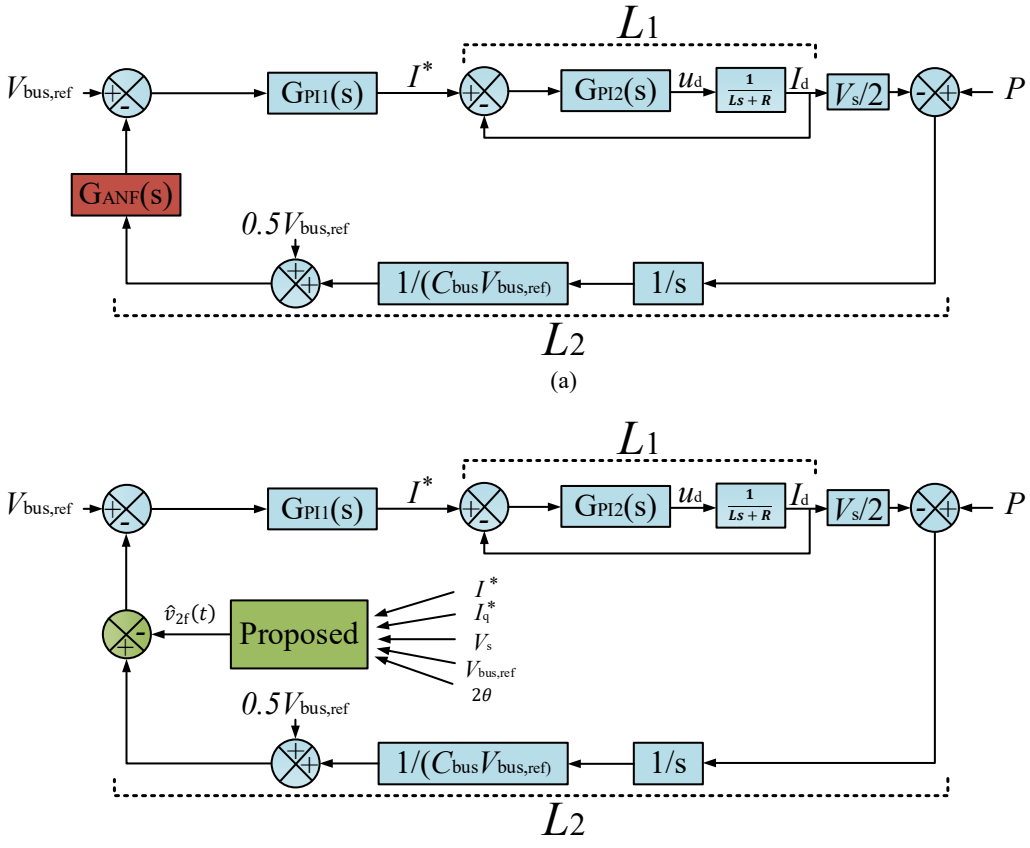


Fig. 4. LTI model of a VSC controller. a) conventional NF-based approach, b) proposed approach.

B. Design of inner current control loop for selecting k_2 and τ_2

In this section, the design process of the inner current control loop (L_1) is presented. The transfer function of loop L_1 is expressed as:

$$H_{L1}(s) = \frac{G_{\mathrm{PI2}}(s)(\frac{1}{Ls+R})}{1 + G_{\mathrm{PI2}}(s)(\frac{1}{Ls+R})}. \qquad (8)$$

The current controller is designed fast enough to avoid interactions with outer loop. The gains of $G_{\mathrm{PI2}}(s)$ are selected using the procedure presented in [20]. According to this method, the gains of $G_{\mathrm{PI2}}(s)$, k_2 and τ_2 are selected using the system`s model in Figures 4(a) or 4(b). For this analysis, the plant is assumed to be $\frac{1}{Ls+R}$ which represents a practical inductor. Following that, the pole of the plant is placed at $-\frac{R}{L}$ and can be cancelled by the zero of $G_{\mathrm{PI2}}(s) = k_2\left(1+\frac{1}{\tau_2 s}\right)$. Then using the system's parameters of Table I, where R=12 mΩ, the gain τ_2 of $G_{\mathrm{PI2}}(s)$ can be determined by $\tau_2 = \frac{L}{R}$ =350 ms. Now while selecting $k_2 = 25$, the pole

of the loop (L_1) will be placed at $\frac{k_2}{L} = 5952$ which is less than half of the selected switching frequency (13 kHz) and is in an appropriate location. The designed $k_2 = 25$ and $\tau_2 = 350\ ms$, which ensure the fast operation of the current control loop, are used throughout this paper for analysis, simulation and experimental tests.

C. Design of conventional NF-based voltage control loop for selecting τ_1

This section presents the integral gain (τ_1) selection for $G_{\mathrm{PI1}}(s)$ in Fig. 4(a) where the conventional NF is applied to the voltage control loop. Characteristic equation of L_2 in Fig. 4(a) is given by:

$$1 - k_1 \frac{V_s}{2C_{bus}V_{bus,ref}}\left(1 + \frac{1}{\tau_1 s}\right)\frac{1}{s}H_{L1}(s)G_{ANF}(s) = 0 \qquad (9)$$

where k_1 and τ_1 are the gains of $G_{\mathrm{PI1}}(s)$.

According to the design procedure of a bus-voltage control loop in [14], τ_1 is supposed to be as small as possible. This achieves higher bandwidth for the bus voltage control loop and thus lower fluctuation of the bus voltage. Figure 5 shows the loci of the poles of the conventional method, given by (9), versus different values of τ_1=12.5 ms, 10 ms, 7.5 ms and 5 ms. As shown, the intersection point of the loci with the real axis shifts toward the left while τ_1 decreases from 12.5 ms to 10 ms which means possible reduction in the fluctuation of the bus voltage. However, as shown, for smaller τ_1 (7.5 ms and 5 ms), the form of the root locus changes and the roots change their trajectory toward the unstable region. This means that using the conventional method, the minimum τ_1 cannot be smaller than 10 ms where the intersection of the roots with real axis is guaranteed. Accordingly, using this analysis, $\tau_1 = 10\ ms$ is selected as the designed gain in this paper to implement the conventional system.

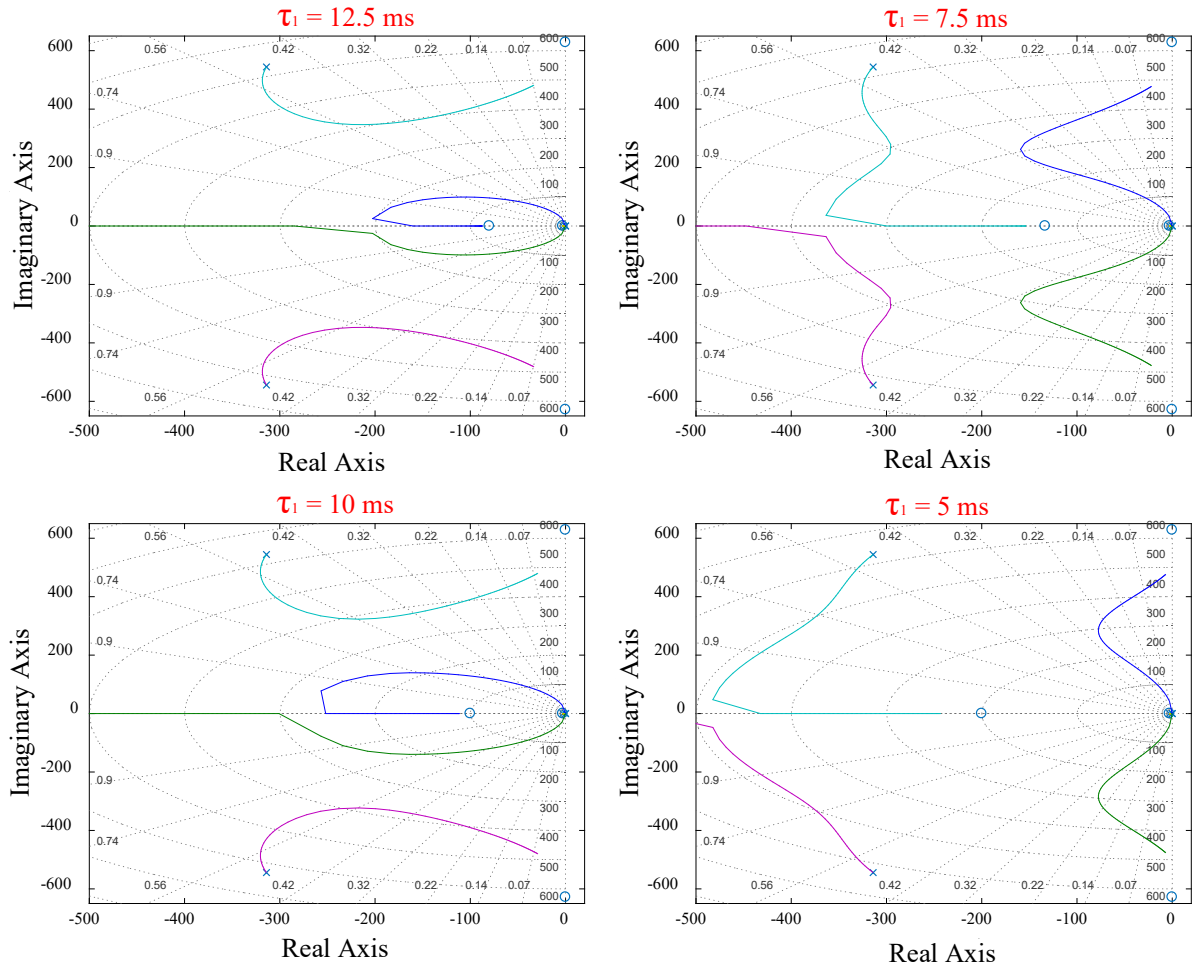


Fig. 5. Loci of the roots of (9) versus different values of τ_1=12.5 ms, 10 ms, 7.5 ms and 5 ms when ζ=0.5.

D. Design of proposed voltage control loop for selecting τ_1

Using the proposed method shown in Fig. 4(b), there is more flexibility in selecting τ_1. Characteristic equation for the proposed method given by L_2 in Fig. 4(b) is expressed as:

$$1 - k_1 \frac{V_s}{2C_{\text{bus}}V_{\text{bus,ref}}}\left(1 + \frac{1}{\tau_1 s}\right)\frac{1}{s}H_{L1}(s) = 0. \qquad (10)$$

Figure 6 shows the loci of the roots of (10) versus different values of τ_1= 12.5 ms, 10 ms, 7.5 ms and 5 ms. As can be seen, unlike the conventional NF method, reducing τ_1 does not change the form of the loci, therefore, smaller τ_1 can be selected and the bus voltage control loop can be designed with lower fluctuation. Using this analysis, $\tau_1 = 5\ ms$ is selected as the designed gain in this paper to implement the proposed system.

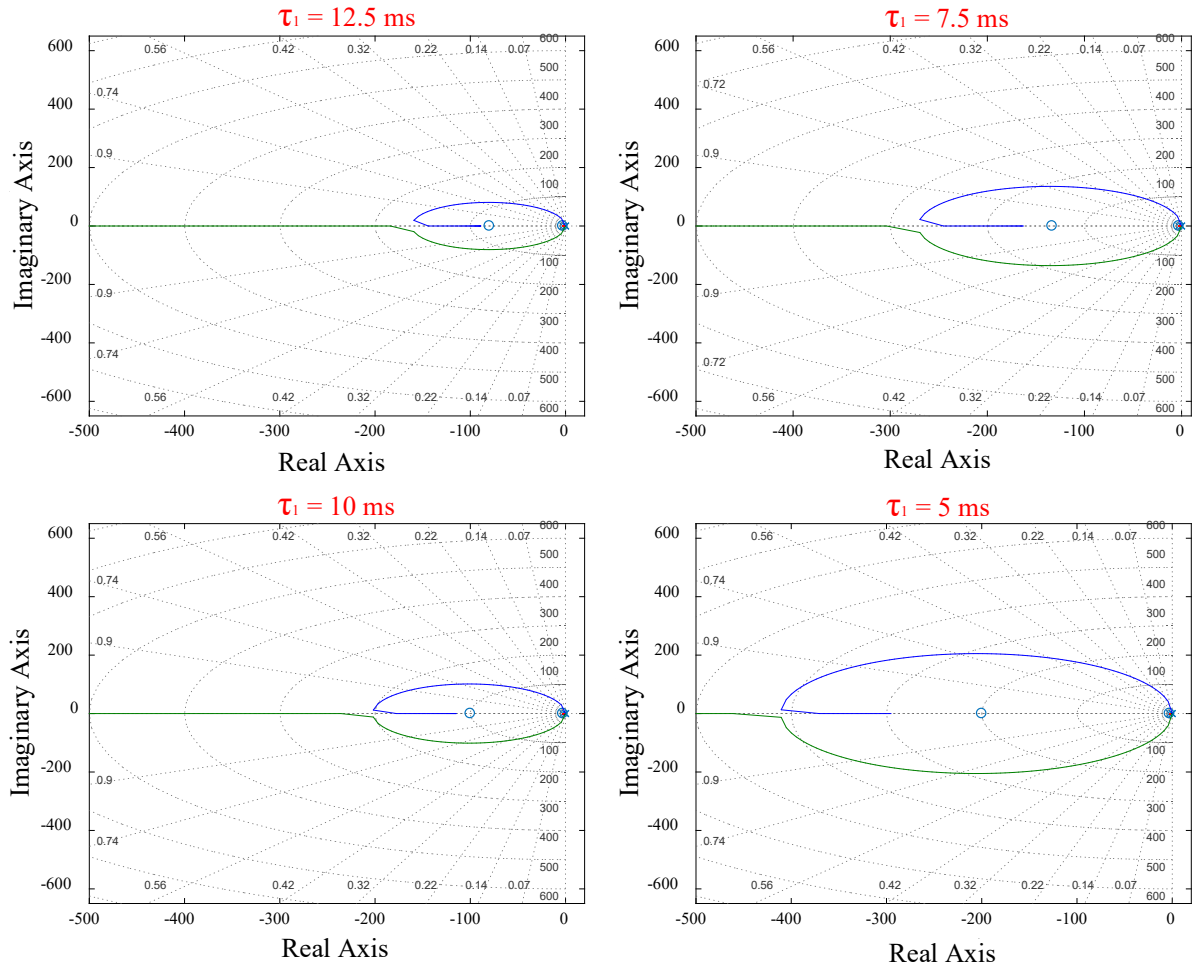


Fig. 6. Loci of the roots of (10) versus different values of τ_1=12.5 ms, 10 ms, 7.5 ms and 5 ms.

E. Proportional gain selection k_1 for the proposed and conventional NF-based voltage control loops

Figure 7(a) shows the loci of the conventional method (9) using the designed $\tau_1 = 10\ ms$. While k_1 increases from zero, the two upper and lower poles move toward the right side. At the same time, their damping reduces remarkably. For instance, at $k_1 = 0.2$, the roots show 0.29 damping corresponding to 38% overshoot. This means that the value of k_1 must be selected as small as possible for the conventional method. Otherwise, the bus voltage will experience large overshoot and oscillations. Such phenomenon is shown in Fig. 8(a).

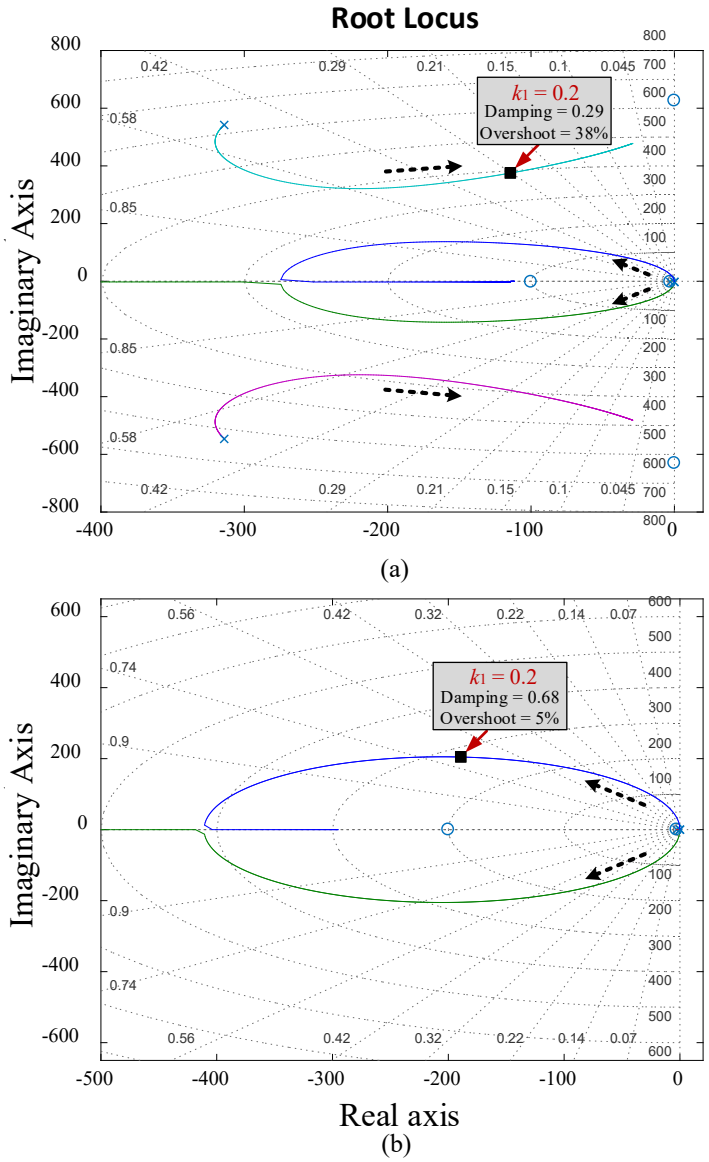


Fig. 7. Loci of the roots of (9) and (10). a) conventional method when $\tau_1 = 10\ ms$, and $\zeta = 0.5$, b) proposed method when $\tau_1 = 5\ ms$.

On the other hand, using the proposed method, larger k_1 contributes to more damping while increases the stability margin of the bus voltage control loop at the same time. This, in the form of loci, is shown in Fig. 7(b). At the same $k_1 = 0.2$, the root exhibits 0.68 damping that corresponds to 5% overshoot. The dynamic of the bus voltage itself is shown in Fig. 8(b). It should be noted that, although higher value of k_1 shows better performance according to the loci in Fig. 7(b), $k_1 > 0.35$ is not recommended. The reason is that a larger k_1 can amplify noises of the system and allow them to pollute the bus voltage control loop.

Using the performed analysis, in order to achieve the best response from both the proposed and conventional NF methods, $k_1 = 0.2$ and $\tau_1 = 5\ ms$ are selected for the proposed method and $k_1 = 0.08$ and $\tau_1 = 10\ ms$ are selected for the conventional method. More designed details of the conventional method is explained in [14]. Thus, the designed gains for the conventional system $k_1 =$

0.08 and $\tau_1 = 10\ ms$ and for the proposed system $k_1 = 0.2$ and $\tau_1 = 5\ ms$ will be used for the rest of analysis, simulation and experimental results in this paper. Table I summarizes the system's parameters.

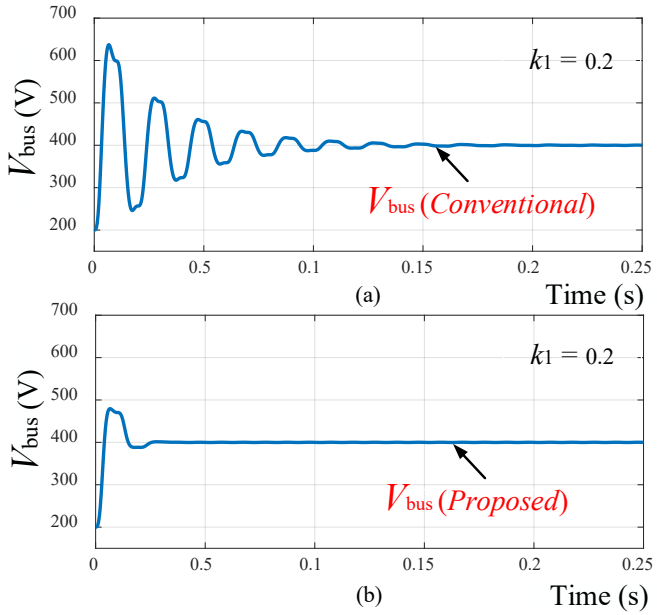


Fig. 8. Comparing the dynamic of bus voltage V_{bus} when the proposed and conventional methods are tuned with the same gain $k_1 = 0.2$. a) bus voltage using the conventional method, b) bus voltage using the proposed method.

TABLE I. SYSTEM PARAMETERS

Circuit Parameter	Item	Value
v_s	AC line voltage	220 V (RMS)
V_{bus}	DC-bus voltage	400 V
f	Line frequency	50 Hz
f_{sw}	Switching frequency	13 kHz
L_f	Filter inductor	4.2 mH
R	Filter resistor	12 mΩ
C_{bus}	DC-bus capacitor	220 µF
Control Parameters (Proposed System)	Item	Value
k_1, τ_1	Gains of $G_{\text{PI1}}(s)$	- 0.2, 5 ms
k_2, τ_2	Gains of $G_{\text{PI2}}(s)$	25, 350 ms
k_3, τ_3	Gains of $G_{\text{PI3}}(s)$	25, 350 ms
Control Parameters (Conventional NF System)	Item	Value
k_1, τ_1	Gains of $G_{\text{PI1}}(s)$	- 0.08, 10 ms
k_2, τ_2	Gains of $G_{\text{PI2}}(s)$	25, 350 ms
k_3, τ_3	Gains of $G_{\text{PI3}}(s)$	25, 350 ms
ζ	NF Damping ratio	0.5

V. Analysis, Comparison and Discussion

A. *Comparison using pole-zero location versus changing ζ*

The transfer function of the whole closed loop (L_2) in Fig. 4(a) for the conventional NF method from P_{in} to V_{bus} is

$$H_c(s) = \frac{V_{\text{bus}}}{P_{\text{in}}} = \frac{(1/s)(1/C_{\text{bus}}V_{\text{bus,ref}})G_{\text{ANF}}(s)}{1 + G_{\text{PI1}}(s)H_{L1}(s)(V_s/2)(1/s)(1/C_{\text{bus}}V_{\text{bus,ref}})G_{\text{ANF}}(s)}. \quad (11)$$

After simplifying, (11) forms a transfer function of order 5.

The whole closed loop transfer function of the proposed method from $V_{\text{bus,ref}}$ to P_{in} is:

$$H_c(s) = \frac{V_{\text{bus}}}{P_{\text{in}}} = \frac{(1/s)(1/C_{\text{bus}}V_{\text{bus,ref}})}{1 + G_{\text{PI1}}(s)H_{L1}(s)(V_s/2)(1/s)(1/C_{\text{bus}}V_{\text{bus,ref}})} \quad (12)$$

which is a transfer function of order 3. Figure 9 compares the pole-zero map of the closed-loop proposed system and the conventional NF versus different values of ($0.1 < \zeta < 0.7$) which is the damping factor of the conventional NF.

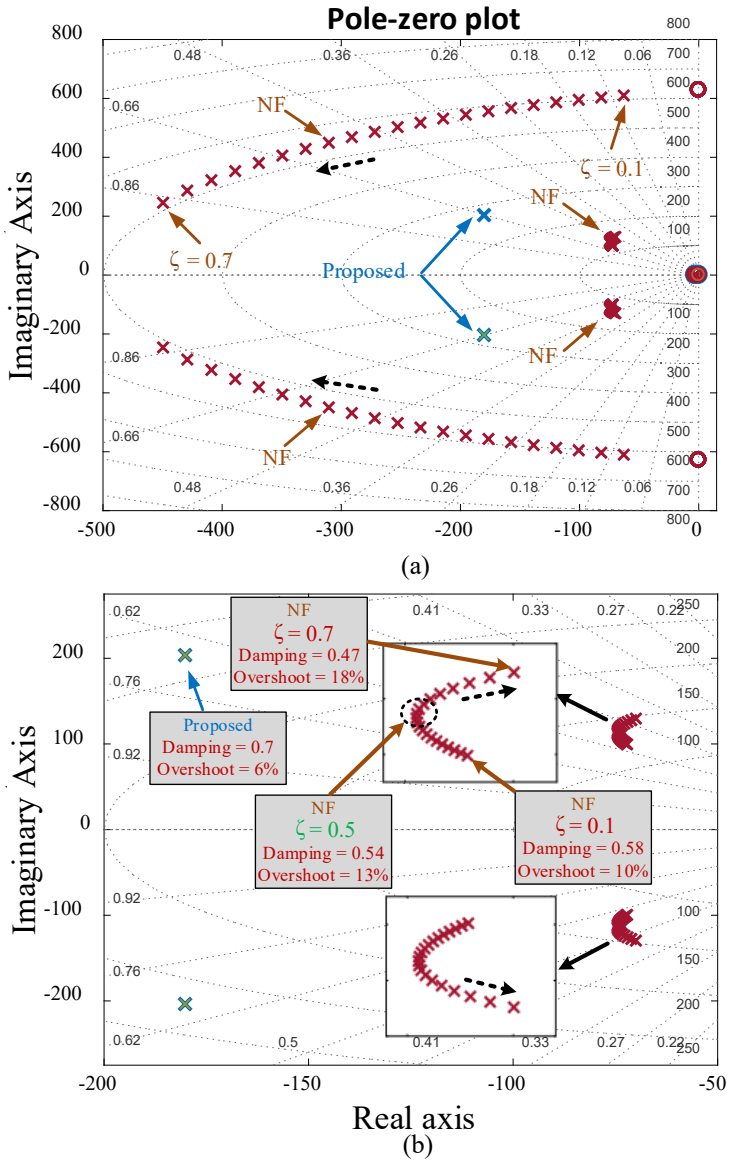


Fig. 9. Pole-zero plot of the closed-loop systems. a) showing the whole plot, b) zoom to show the dominant poles.

The analysis shown in Fig. 9 concludes that the NF`s damping ratio (ζ) should not be small (to avoid poor damping of high-frequency poles) and should not be large (to avoid poor damping of low-frequency poles). Therefore a value of 0.4< ζ <0.6 is recommended and ζ =0.5 is selected for the rest of this study. The approximate settling time can be calculated from

$$t_s \approx \frac{4}{\gamma \omega_n} \qquad (13)$$

where γ is defined as the closed-loop pole's damping ratio and ω_n is their natural frequency. Solving the characteristic equation of (10) results in the equation $s^2 + 2\gamma\omega_n + {\omega_n}^2 = 0$, where γ and ω_n are defined by:

$$2\gamma\omega_n = -k\frac{V_s}{2C_{bus}V_{bus,ref}} \qquad (14)$$

$${\omega_n}^2 = -k\frac{V_s}{2C_{bus}V_{bus,ref}\tau} = \frac{2\gamma\omega_n}{\tau}. \qquad (15)$$

Then substituting the designed $k_1 = 0.2$ and $\tau_1 = 5\ ms$ for the proposed method along with the other system parameters of Table I, ω_n for the proposed method is calculated at 265 rad/s from (15). Accordingly, the settling time t_s is approximated at 21 ms from (13) for the pole`s damping ratio of $\gamma = 0.7$ which is shown in Fig. 9(b). Similarly, using the designed k_1 =0.08 and τ_1 =10 ms for the conventional NF method and the other system parameters of Table I, ω_n = 119 rad/s for the conventional method. Accordingly, t_s is calculated for the two indicated poles with ζ =0.1 and ζ =0.7 in Fig. 9(b). At ζ = 0.1 which corresponds to the pole`s damping ratio of $\gamma = 0.58$, the settling time is estimated from (13) as $t_s \approx 57\ ms$. In addition, at ζ = 0.7 ($\gamma = 0.47$), the settling time is $t_s \approx 71\ ms$. As mentioned before, ζ for the conventional method is designed at 0.5. Therefore, at ζ =0.5 the dominant poles shown in Fig. 9(b) have a damping ratio of $\gamma = 0.54$ and the settling time of $t_s \approx 62\ ms$ is obtained. It can be seen that the proposed method achieves a substantial improved in the settling time ($t_s \approx 21\ ms$) compared with the conventional method ($t_s \approx 62\ ms$).

B. Comparison using pole-zero location versus changing C_{bus}

Figure 10 compares the pole-zero map of the conventional NF and the proposed method when C_{bus} reduces from 1 mF to 75 μF with the step change of 10 μF. As can be seen in Fig. 10(a), the upper and lower dominant poles of the conventional method move toward the imaginary axis (lower damping) while C_{bus} reduces. On the contrary, in Fig. 10(b), the damping of the dominant poles of the proposed method increases while C_{bus} decreases. In this paper, C_{bus} = 220 μF is used for design and implementation of both the proposed and conventional methods. As can be seen, at C_{bus} = 220 μF, the conventional method has two pairs of dominant poles and each one exhibits approximately 0.5 damping. However, the proposed system has one pair of dominant poles, which placed at better damping position of 0.65. This verifies the lower fluctuation of the bus voltage using the proposed system. The settling time of the conventional method is shown as $t_s \approx 62\ ms$ using (13) while the proposed method exhibits $t_s \approx 21\ ms$.

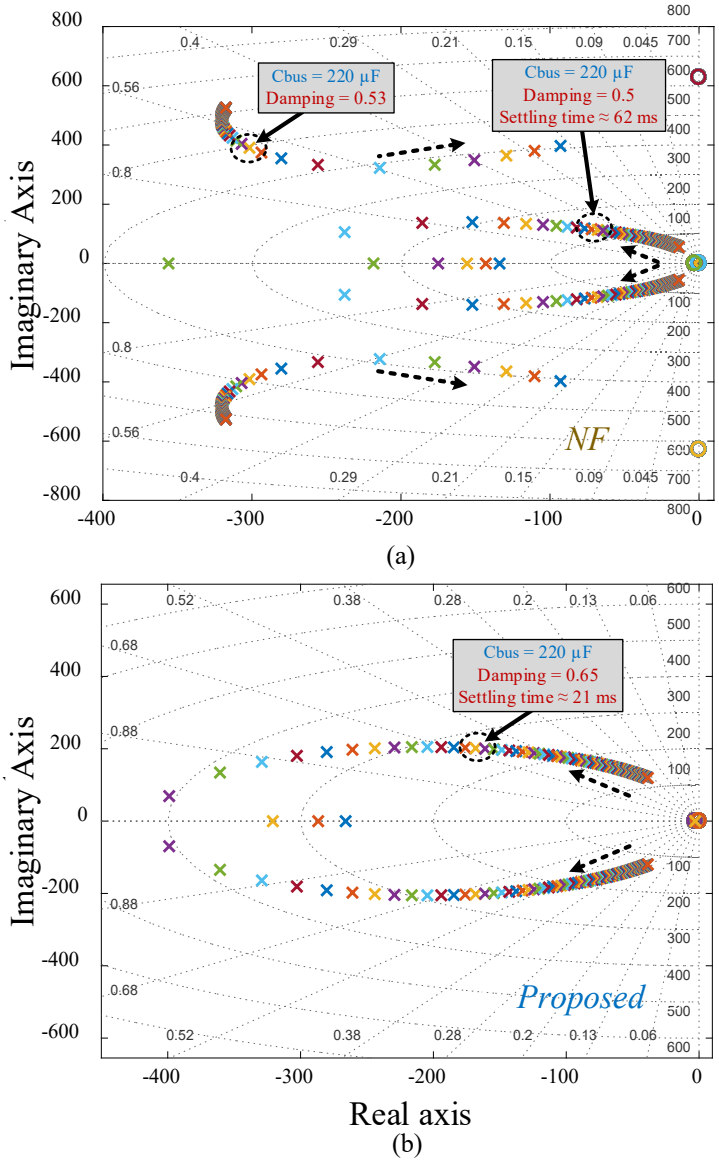


Fig. 10. Trajectory of system poles when C_{bus} reduces from 1 mF to 75 µF with an step of 25 µF. a) conventional NF, b) proposed method.

Table II shows the poles and zeros of both proposed and conventional NF methods (Fig. 4(a) and Fig. 4(b)) when they are designed based on the design procedure explained in Sections IV and V.

Table II. Closed loop poles of the proposed and the conventional NF systems.

No	Closed-loop zeros (Proposed)	Closed-loop poles (Proposed)	Closed-loop poles (Conventional NF)	Closed-loop zeros (Conventional NF)
1	0	-5589.3	-5792.4	0
2	-5952.4	-181.5 + 205.8i	-319.9 +440.2i	-5952.4
3		-181.5 – 205.8i	-319.9 -440.2i	628.3i
4			-74.3 + 117.7i	- 628.3i
5			-74.3 – 117.7i	

VI. Performance Evaluation of Proposed Method

In this section, the dynamic responses and steady-state performance of the proposed control method is evaluated and compared with the conventional NF in [14] using MATLAB Simulink, and experimental results. The proposed method and conventional NF, which are designed in Section IV and V, are implemented and compared in a single-stage grid-connected rectifier as shown in Fig. 11. The parameters in Table I are used for both simulations and experiments.

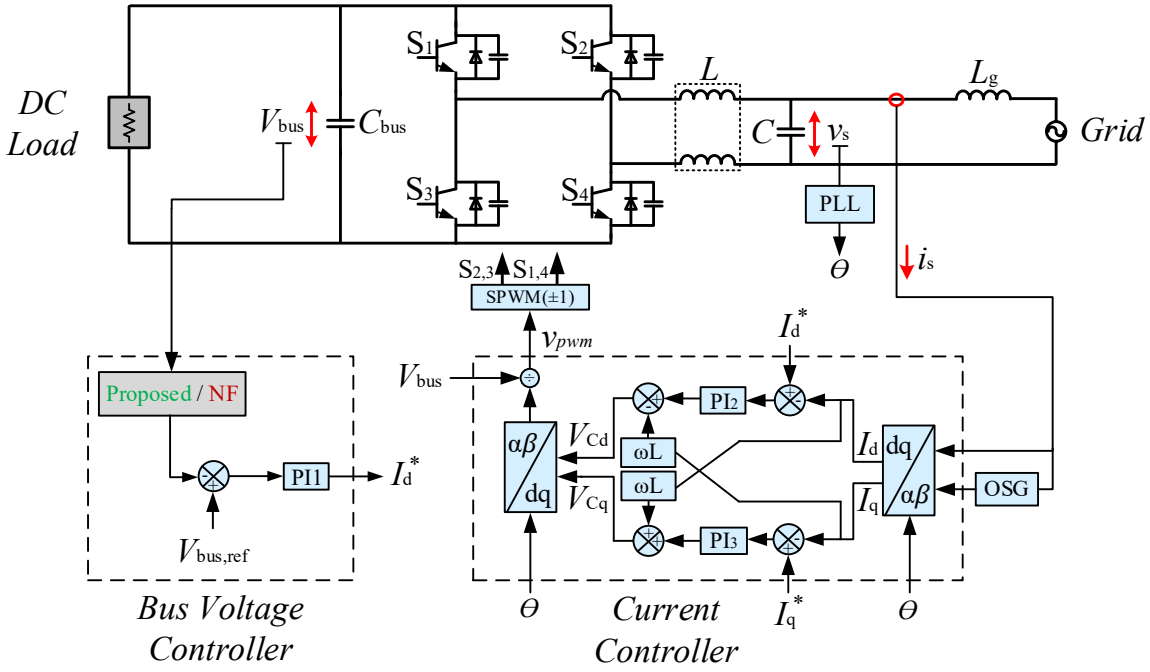


Fig. 11. Overall system topology including the power circuit and the control system.

A. Performance evaluation via simulation results

The tests are performed under the two following conditions: i) during step-change of bus voltage command, and ii) during step-change of input power (load switching). Figure 12(a) shows the bus voltage V_{bus} using the proposed and the conventional NF during a step-change of 400 V →500 V. Figure 12(b) presents V_{bus} during a step-change of 500 V →400 V. As can be seen, when the proposed voltage control method is used, V_{bus} exhibits lower overshoot, oscillations and settling time during the step change. As theoretically calculated in Section V-B, the settling time of the bus voltage is supposed to be 21 ms for the proposed method and 62 ms for the conventional NF which are almost consistent with the simulation results in Figures 12(a) and 12(b). This validates the performed analysis as well as superior performance of the proposed method than the conventional NF.

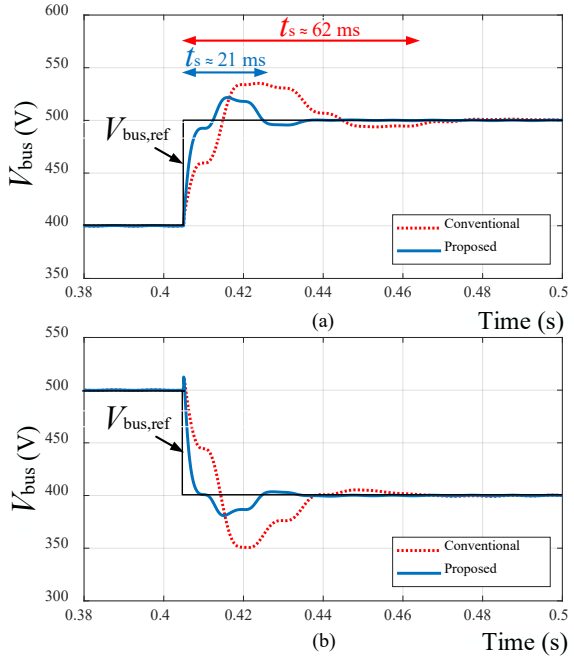


Fig. 12. Dynamic performance comparison during bus voltage variation. a) V_{bus}= 400 V →500 V, b) V_{bus}= 500 V →400 V.

In another test, the dynamic response of V_{bus} is evaluated during load variation while V_{bus} is fixed at 400 V. Figure 13(a) shows the bus voltage V_{bus} and the extracted dc using the proposed method, and Fig. 13(b) shows the grid-side current i_s, when the power P increases from 10 W to 1000 W. Figure 14(a) presents V_{bus} and Fig. 14(b) presents i_s using the conventional NF. As can be seen, both the proposed and the conventional methods can successfully extract the dc component of V_{bus}. However, when the proposed method is applied, V_{bus} and i_s in Fig. 13 exhibit lower transient and settling time than V_{bus} and i_s in Fig. 14 which presents the dynamic response of the conventional method.

Figure 15 shows the transient response of V_{bus} and i_s during a load switching from P = 1000 W to 10 W using the proposed method. Figure 16 presents the results of a similar test when the conventional method is applied. As can be seen, a lower transient is achieved on both V_{bus} and i_s in Fig. 15 validating the better performance of the proposed approach.

The above analyses under different operating conditions validate the robustness of the proposed approach in term of removing the 2-f ripple and its superior performance in improving the overall system damping. Such a salient feature is validated using experimental tests in the following section.

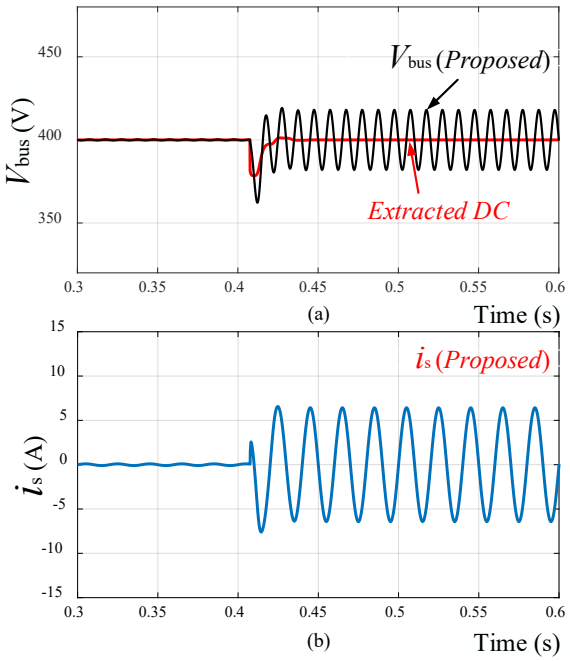


Fig. 13. Dynamic performance of the proposed method during load variation P= 10 W →1000 W.

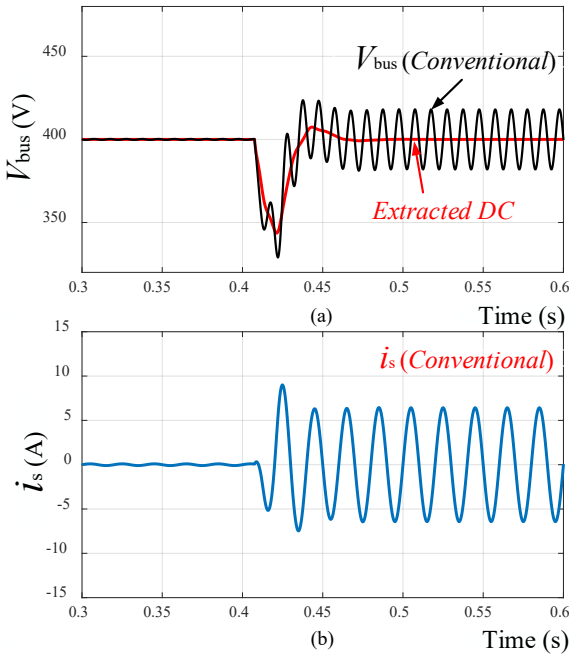


Fig. 14. Dynamic performance of the conventional method during load variation P= 10 W →1000 W.

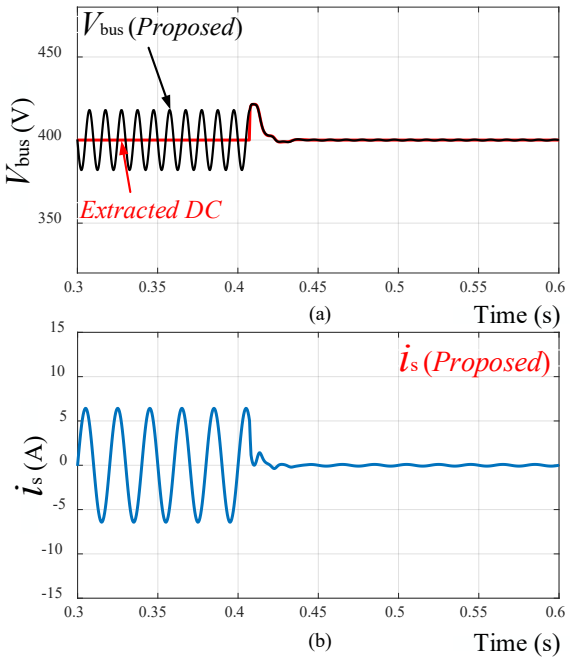


Fig. 15. Dynamic performance of the proposed method during load variation P= 1000 W →10 W.

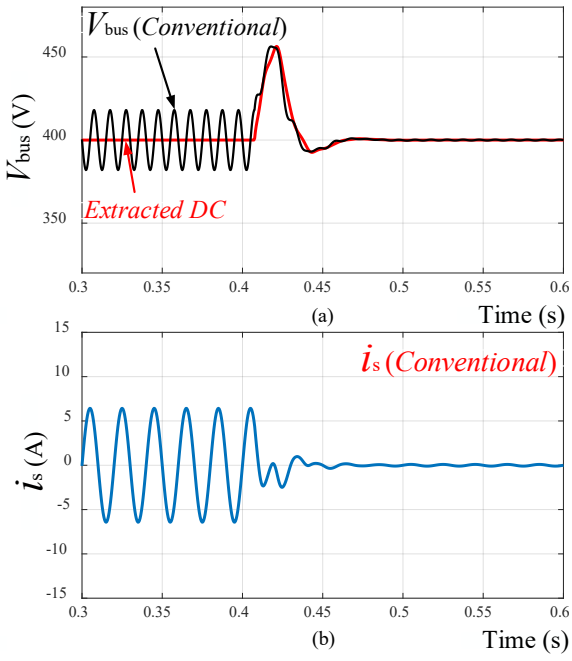


Fig. 16. Dynamic performance of the conventional method during load variation P= 1000 W →10 W.

B. Performance evaluation via experimental results

A laboratory prototype of the single-phase rectifier shown in Fig. 11 is implemented and tested in a grid-connected mode. The system parameters in Table I are used for this purpose. A SEMISTACK – IGBT as the ac/dc grid-connected VSC, a RS Pro 8.14 kVA Variac, a Chroma 63800 electronic load, and an MI 2883EU Class S power quality analyzer are used for experimental testing. The proposed method and the conventional NF in [14], that designed in Section IV and V, are implemented on TMSF28335 controller via programing in C-language and the dynamic performance of V_{bus} and i_{s} are compared using similar test that used in simulation tests.

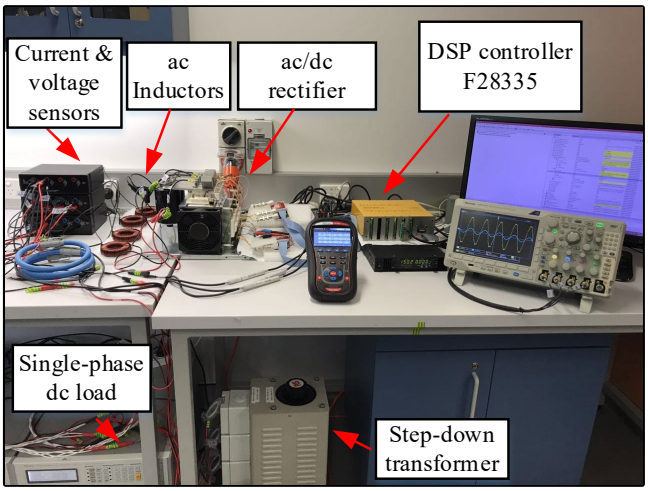
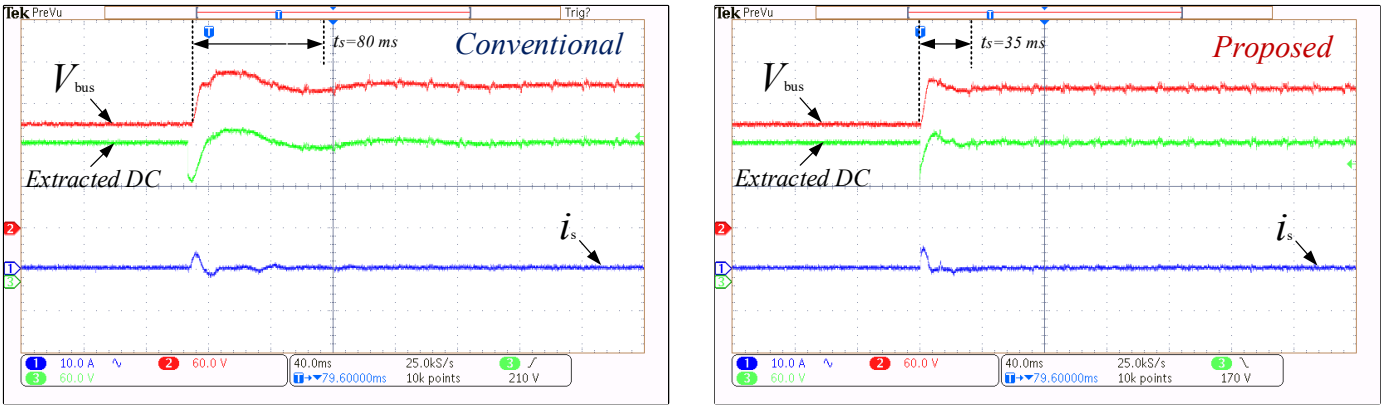


Fig. 17. Experimental setup

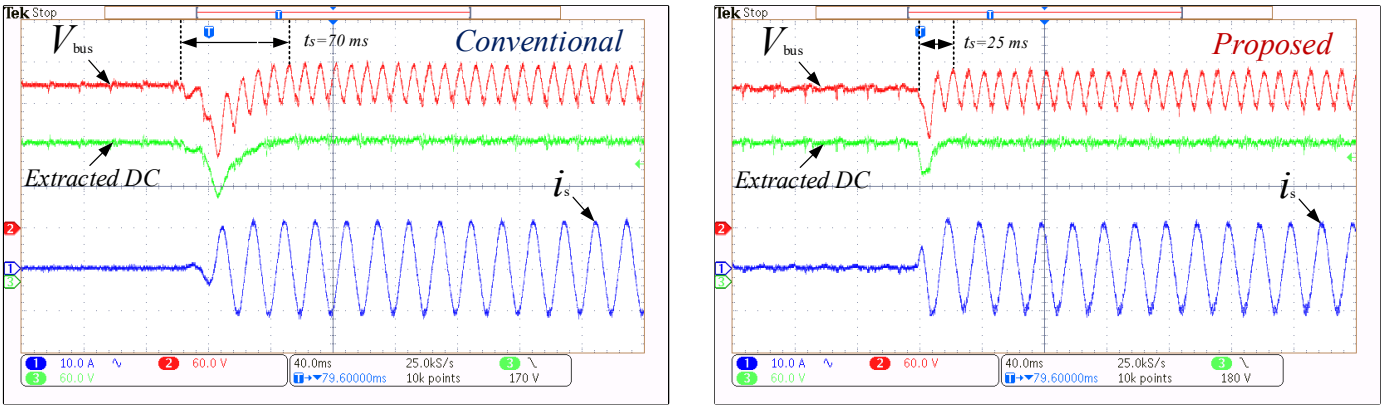
Figure 18 shows a bus voltage V_{bus} startup when $V_{\text{bus,ref}}$ is set to 200 V. Figure 18(a) shows V_{bus} and i_{s} when the conventional NF is used in the bus voltage control loop and Fig. 18(b) shows V_{bus} and i_{s} when the proposed method is applied. Although the two methods show appropriate responses in regulating V_{bus}, the proposed method exhibits lower transients and improved dynamic response compared with the conventional NF. As shown, the settling time of V_{bus} in the conventional method is measured at around $t_{\text{s}} = 80\ ms$ which is close to the theoretical value of $t_{\text{s}} = 62\ ms$ in Section V. On the other hand, using the proposed method t_{s} is reduced to about 35 ms that can also validate the theoretical $t_{\text{s}} = 21\ ms$ shown in Section V. It should be noted that the differences between the measured settling times and the theoretical values are because of the non-linearities and uncertainties of the system which are neglected in the theoretical analysis in Section V.



(a) (b)

Fig. 18. Experimental results of the dynamic response during the bus voltage startup. Grid-side current i_s (Ch.1 10 A/div), bus voltage V_{bus} (Ch.2 60 V/div), and the extracted dc of V_{bus} (Ch.3 60 V/div). a) conventional NF [14], b) proposed method.

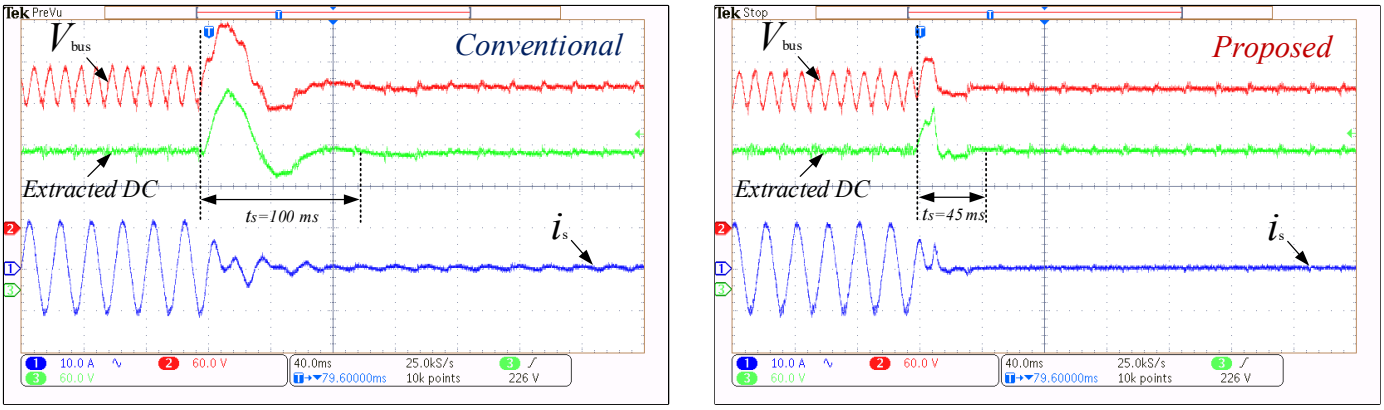
Figure 19 compares the dynamics of both V_{bus} and i_s using both conventional NF and the proposed method during a quick load variation from $P = 0$ to 700 W while $V_{bus,ref}$ is set to 200 V. As shown, the conventional method exhibits a higher transient (undershoot) and settling time ($t_s = 70\ ms$) than the proposed method ($t_s = 25\ ms$). This test also shows the better performance of the VSC in Fig. 11 when proposed method is used. The result of this test revalidates the simulation results in Figures 13 and 14.



(a) (b)

Fig. 19. Experimental results of the dynamic response during a load variation from $P = 0$ W → 700 W. Grid-side current i_s (Ch.1 10 A/div), bus voltage V_{bus} (Ch.2 60 V/div), and the extracted dc of V_{bus} (Ch.3 60 V/div). a) conventional NF [14], b) proposed method.

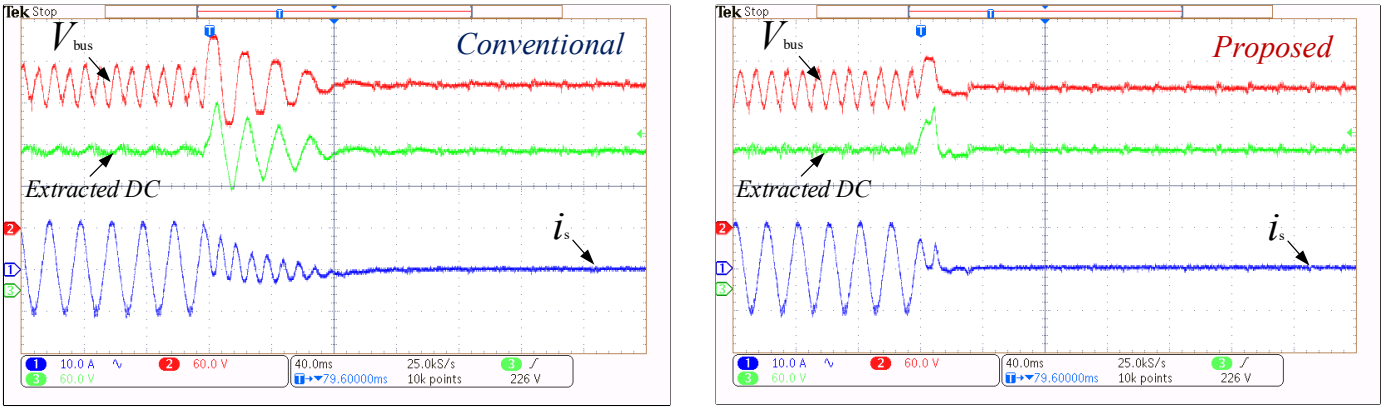
Finally, in the last test, the disturbance of a load switching is applied when $P = 700 \rightarrow 0$ W and the performance of VSC is tested while using both conventional NF and the proposed method. As can be seen in Fig. 20(a), the quick load disconnection generates a substantial transient on V_{bus} which would be harmful for the bus capacitor C_{bus}. However, as Fig. 20(b) presents, when VSC uses the proposed method, such transient will be significantly lower. This test also confirms the robustness and better dynamic response of the proposed approach while revalidating the simulation results in Figures 15 and 16.



(a) (b)

Fig. 20. Experimental results of the dynamic response during a load variation from P = 700 W → 0 W. Grid-side current i_s (Ch.1 10 A/div), bus voltage V_{bus} (Ch.2 60 V/div), and the extracted dc of V_{bus} (Ch.3 60 V/div). a) conventional NF [14], b) proposed method.

It should be noted that all the simulation and experimental tests are performed when the proposed and conventional methods are designed to achieve their best performance. The design process is already explained individually for both conventional and the proposed method in Section IV and V and the outcomes are summarized in Table I via showing the gains of *PI* controllers. Accordingly, it is concluded that the voltage control loop that uses the conventional NF must be designed at a lower bandwidth via tuning $G_{\mathrm{PI1}}(s)$ with the gains ($k_1 = 0.08$ and $\tau_1 = 10\ ms$), whereas when the proposed method is used, a higher bandwidth can be targeted via tuning $G_{\mathrm{PI1}}(s)$ with higher gains ($k_1 = 0.2$ and $\tau_1 = 5\ ms$). In the other word, when the NF is added to the voltage control loop, a fast tuning of $G_{\mathrm{PI1}}(s)$ (high bandwidth) is not possible and would shift the system toward the poor damping area. This is the disadvantage of the conventional method as verified in Fig. 7 and the simulation results presented in Fig. 8. Figure 20 shows this fact while the conventional method is also tuned with the fast tuning of the proposed method ($k_1 = 0.2$ and $\tau_1 = 5\ ms$). As can be seen, this tuning (higher bandwidth) causes larger oscillations on V_{bus} in Fig. 21(a) while the proposed method is remarkably robust and solid.



(a) (b)

Fig. 21. Experimental results of the dynamic response during a load variation from P = 700 W → 0 W when the same design of the proposed voltage control loop is used for the conventional method. Grid-side current i_s (Ch.1 10 A/div), bus voltage V_{bus} (Ch.2 60 V/div), and the extracted dc of V_{bus} (Ch.3 60 V/div). a) conventional NF [14], b) proposed method.

VII. Conclusion

This paper presents a novel dc-bus voltage control method for a single-phase grid-connected VSCs to provide improved power quality. The proposed method estimates the 2-f ripple of a bus voltage and removes it from the control loop directly without adding any filter, nor affecting the dynamic of the bus-voltage control system. While the proposed method is used, the 2-f is precisely eliminated, and the voltage control loop can be designed with higher bandwidth which would be an asset for a VSC to exhibit higher robustness against the common disturbances such as bus voltage variation and/or quick load changing. The proposed method is compared with the conventional NF-based method and its superior performance is validated through mathematical analysis, simulation in MATLAB Simulink and experimental results. The future aim of this research is……..

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