An Enhanced DC-Bus Voltage Control Loop for Single-Phase Grid-connected DC/AC Converters

Seyedfoad Taghizadeh, *Student Member, IEEE*, M. J. Hossain, *Senior Member, IEEE*, Junwei Lu, *Senior Member, IEEE*, Masoud Karimi-Ghartemani, *Senior Member, IEEE*

***Abstract*: This paper presents an efficient method to enhance the dc-bus voltage control loop of a single-phase grid-connected dc/ac converter which improves its responses in terms of oscillation on its dc-bus voltage as well as its output ac current. Conventionally, the double-frequency (2-f) ripple is reduced by using a large electrolyte capacitor which increases the cost and size of the system. A state-of-the-art approach is to use a notch filter (NF) to block the 2-f ripple in the voltage control loop. This can significantly reduce the capacitor size. The existing presentations of this method, however, do not integrate the internal dynamics of the NF into consideration. This paper proposes a new way of implementing the NF which allows integration of its internal variables into the control loop. The resulted system exhibits enhanced transient responses at both the dc-bus voltage and the output ac current. The proposed method is analyzed in detail and its effectiveness is verified through simulations and experimental results.**

***Index Terms*—Double-frequency ripple, dc extraction, single-phase converter, notch filter.**

I. Introduction

Single-phase converters are widely used in low-power distributed generation (DG) applications such as residential roof-top solar photovoltaic (PV) generators [1, 2], low-power rectifier applications [3], and on-board electric-vehicle (EV) chargers [4, 5]. In addition to power exchange, they can also participate in offering ancillary services to the grid. One particular issue with the single-phase converters is the double-frequency (2-f) ripple that is generated on the dc-bus voltage due to the ac power. Conventionally, large capacitors are used to ensure that this ripple does not exceed the limits. This compromises the lifetime, size and cost of the converter [1, 3, 6, 7]. Another solution is to use an auxiliary circuit that draws constant current from the source and creates a high dc voltage to provide the needed pulsation [7-10]. However, this increases the complexity of both the hardware and the control system and decreases its efficiency. A state-of-the-art approach is to use a method of blocking the ripples and preventing them from propagating into the control loop and spoiling its variables [11, 12]. This approach succeeds in substantially reducing the capacitor size but can produce extra oscillatory transient responses. Such oscillations must be maintained within limits

Seyedfoad Taghizadeh and M. J. Hossain are with the School of Engineering, Macquarie University, Australia. E-mail: s.t.taghizadeg@ieee.org, jahangir.hossain@mq.edu.au.

Junwei Lu is with the Department of Science and Engineering, Griffith University, Australia. E-mail: j.lu@griffith.edu.au.

Masoud Karimi-Ghartemani is with the Department of Electrical and Computer Engineering, Mississippi State University, E-mail: ss2821@msstate.edu, karimi@ece.msstate.edu.

in order to facilitate integration of such converters at a high penetration level.

Figure 1 illustrates the typical closed-loop control that is commonly used for a grid-connected single-phase converter, where v_{bus} is the actual bus voltage, $V_{\mathrm{bus,ref}}$ is the reference value of the bus voltage and v_{PLL} is the normalized sinewave signal whose phase angle is generated by a phase-locked loop (PLL) and synchronized with the grid voltage v_{s}. The variable I_{ref} is the output signal of the voltage control loop and is used as an amplitude which is multiplied by v_{PLL} to generate a reference value i_{ref} for the current controller. Accordingly, i_{ref} is synchronized with the grid voltage so that the system can work with unity power factor. To sum up, the outer loop is responsible for controlling the bus voltage while the inner loop controls the current.

The 2-f ripple of the bus voltage circulates into the inner loop through its reference signal (i_{ref}). As a result, such a disturbance inside the current controller demands the sluggish tuning of proportional integral (PI) controllers to prevent the propagation of the ripples into the system. Otherwise, it translates into 3rd harmonics and also phase deviation on the grid-side current [13].

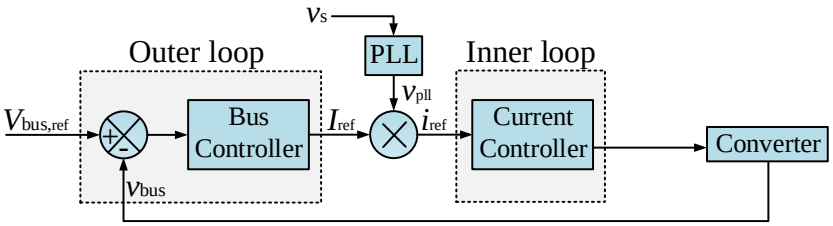


Fig.1. Typical closed-loop control for a single-phase dc/ac converter.

In [5], a low-pass filter (LPF) is used in the voltage control loop of a single-phase EV charger. However, the LPF causes a very low convergence rate as reported in [11]. A dc-observer concept is proposed in [11] for this purpose. This method effectively removes the 2-f ripple, but it shows some high transient oscillations during a step change of the bus voltage which may be related to its redundant structure, i.e. using three differential equations for a system that can be modeled at order of two.

In [12], a second-order notch filter (NF) is used in the voltage control loop to block the 2-f ripples. It succeeds in its main task and results in a significant reduction in the capacitor size while improving the ac-side power quality. This approach appears to be the state of the art. It, however, causes some additional oscillatory peaks and transients due to its fast response and small capacitor.

It is noted that all the existing techniques use some sort of filtering (or estimation) on the bus voltage which is of higher order. This will introduce additional modes (or poles) into the system. This lowers the overall damping of the system, increasing response overshoots, oscillations and settling time. This issue, which is not addressed in the literature, is the focus of this paper. The proposed idea is to deploy the internal variables of the filters (or estimators) in the control loop to allow more degrees of freedom to improve the overall system damping. But this is a challenge because the internal variables of the filter are spoiled by 2-f ripples and their direct deployment will introduce those ripples into the loop. Therefore, a new way of modeling such filters is required to ensure

that the new variables are dc in nature.

We formulate our approach in the context of the method of [12]. An adaptive filter was first introduced in [14] and then modified in [15] to be used for harmonics extraction in a single-phase active-power filter. This is indeed, under certain mild conditions, an alternative time-varying implementation of an NF. Moreover, its internal variables are dc in nature. This is a significant advantage and is built on in this paper to enhance the performance of the dc-bus voltage control in a single-phase converter.

After formulating the approach, the paper develops a design method for additional feedback terms. The proposed method does not engage any new hardware or control dynamic, but it only feeds back some already existing variables in the control loop. Overall, the damping improvement of the control loop is confirmed by analysis, computer simulations and experimental results. The proposed approach also facilitates making the loop adaptive to grid frequency variations without requiring any additional control stages. This is due to the fact that the new implementation of NF allows directly using the phase angle of the PLL in the NF.

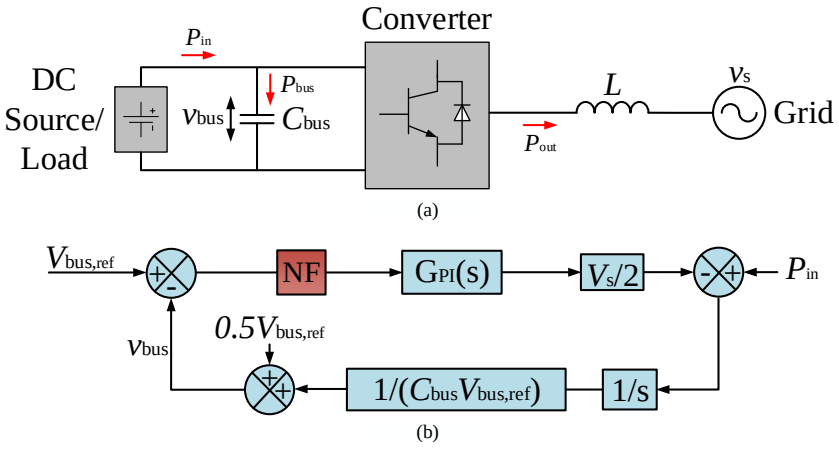


Fig. 2. a) Typical model of a single-phase grid-connected voltage source converter, b) simplified and linearized model of bus-voltage control loop.

II. Modeling of Bus-voltage Control Loop

Figure 2(a) shows a typical model of a single-phase grid-connected voltage source converter and Fig. 2(b) (without NF) presents a simplified and linear time-invariant (LTI) model of the bus-voltage control loop [13]. In this model, the current controller is assumed to be much faster than the voltage loop. The LTI loop shown in Fig. 2(b) is verified in [13] in detail. The PI controller is expressed as $G_{\mathrm{PI}}(s) = k(1 + \frac{1}{\tau s})$, where k and τ are the proportional and integral gains. The characteristic equation of the loop is:

$$1 - k\frac{V_s}{2C_{\mathrm{bus}}V_{\mathrm{bus,ref}}}\left(1 + \frac{1}{\tau s}\right)\frac{1}{s} = 0 \qquad (1)$$

where C_{bus} is the dc-bus capacitor, V_s is the amplitude of the grid voltage and $V_{\mathrm{bus,ref}}$ is the reference value of the dc-bus voltage. The transfer function between the input power P_{in} and the bus voltage V_{bus} is given by:

$$G(s) = \frac{V_{\text{bus}(s)}}{P_{\text{in}(s)}} = \frac{1}{C_{\text{bus}} V_{\text{bus,ref}}} \frac{s}{s^2 + 2\zeta\omega_{\text{n}} + {\omega_{\text{n}}}^2}. \quad (2)$$

The parameters ζ and ω_n in (2) are defined by:

$$2\zeta\omega_{\text{n}} = -k\frac{V}{2C_{\text{bus}} V_{\text{bus,ref}}}, \quad (3)$$

$${\omega_{\text{n}}}^2 = -k\frac{V}{2C_{\text{bus}} V_{\text{bus,ref}}\tau} = \frac{2\zeta\omega_{\text{n}}}{\tau}. \quad (4)$$

The variable P_{in}, which is the input power of the loop, is given by $P_{\text{in}} = P_{\text{bus}} + P_{\text{out}}$, where P_{bus} is the power that flows through the dc bus and $P_{\text{out}} = v_{\text{s}} i_{\text{s}}$ approximates the converter`s injected/absorbed power.

The normalized peak fluctuation of the bus voltage V_{p} caused by the input power disturbances can be obtained from (2), [13], and is given by:

$$V_{\text{p}} = \frac{V_{\text{bus,max}}}{V_{\text{bus,ref}}} = \frac{P_{\text{in}}}{C_{\text{bus}}\left(V_{\text{bus,ref}}\right)^2 \omega_{\text{n}}} e^{-\frac{\zeta cos^{-1}\zeta}{\sqrt{1-\zeta^2}}} \quad (5)$$

Due to the fact that bus-voltage ripple is originated from the oscillating component of the input power $P_{\text{in}} = \frac{V_{\text{s}} I_{\text{s}}}{2}$ which passes through $\frac{1}{C_{\text{bus}} V_{\text{bus,ref}}} \frac{1}{s}$ in Fig. 2(b), the magnitude of the bus-voltage ripple in full power is given by $\tilde{V}_{\text{bus}} = P_{\text{in}} \frac{1}{\left|\frac{1}{j2\omega}\right|} \frac{1}{C_{\text{bus}} V_{\text{bus,ref}}} = \frac{P_{\text{in}}}{2\omega C_{\text{bus}} V_{\text{bus,ref}}}$. Accordingly, the normalized current ripple ratio R_{p} is defined and calculated in [13] as:

$$R_{\text{p}} = \frac{I_2}{I_{\text{s}}} = \frac{{\omega_{\text{n}}}^2}{4\omega^2}\sqrt{\frac{16\zeta^2\omega^2}{{\omega_{\text{n}}}^2}} + 1 \quad (6)$$

where I_2 is the amplitude of the 2-f ripple of the current and is clearly observed from Fig. 2(b) to be

$$I_2 = \frac{V_{\text{s}} I_{\text{s}}}{2}\left|\frac{1}{j2\omega}\right| \frac{1}{C_{\text{bus}} V_{\text{bus,ref}}} \left|k\left(1 + \frac{1}{j2\omega\tau}\right)\right| \quad (7)$$

and finally, again from Fig. 2(b), the magnitude of the bus-voltage ripple is given by

$$V_{\text{ripple}} = \frac{P_{\text{in}}}{2\omega C_{\text{bus}} V_{\text{bus,ref}}}. \quad (8)$$

From (8), it can be seen that V_{ripple} is directly affected by changing the input power P_{in}, C_{bus} and $V_{\text{bus,ref}}$. In [13], a design algorithm is proposed to determine the controller gains k and τ and the capacitance C_{bus}. In [12], the NF is used to block the 2-f ripples of the dc-bus voltage and to prevent those ripples from propagating in the control loop. This will relax the tight limits on C_{bus} and allows reducing its size. This will, however, introduce additional dynamics into the loop that are not fully integrated and cause oscillatory responses during sharp transients.

III. Proposed DC-extraction Method

A. *Alternative Implementation of Notch Filter*

Generally and dominantly, the bus voltage in a single-phase converter has a dc and a 2-f component and can be expressed as:

$$v_{\text{bus}}(t) = V_{\text{bus,dc}} + A_1 \sin(2\omega t) + B_1 \cos(2\omega t) \quad (9)$$

where $V_{\text{bus,dc}}$ is the dc component and $v_{2\text{f}}(t) = A_1 \sin(2\omega t) + B_1 \cos(2\omega t)$ represents the 2-f ripple term. In (9), ωt represents the grid voltage phase angle. The 2-f component of $v_{\text{bus}}(t)$ in (9), which is supposed to be estimated by the proposed algorithm, is expressed as:

$$\hat{v}_{2\text{f}}(t) = K_1 \sin(2\omega t) + K_2 \cos(2\omega t) \quad (10)$$

where K_1 and K_2 are the estimated amplitudes of the sine and cosine terms of $v_{2\text{f}}$. The estimated dc offset is

$$Y_{\text{bus,dc}} = v_{\text{bus}}(t) - \hat{v}_{2\text{f}}(t). \quad (11)$$

The Gradient Descent (GD) method is used to estimate K_1 and K_2 in (10). The cost function J is defined as:

$$J(K_1, K_2) = [v_{\text{bus}}(t) - \hat{v}_{2\text{f}}(t)]^2. \quad (12)$$

According to the GD method:

$$\frac{d}{dt}(K_1, K_2)(t) = -\mu \frac{\partial J(K_1,K_2)}{\partial (K_1,K_2)} \quad (13)$$

where μ is the convergence gain of the algorithm and is a 2x2 positive diagonal matrix. Solving (13) results in

$$\dot{K_1} = \mu_1 \sin(2\omega t)\, Y_{\text{bus,dc}}, \quad (14)$$

$$\dot{K_2} = \mu_2 \cos(2\omega t)\, Y_{\text{bus,dc}}. \quad (15)$$

The integrals of $\dot{K_1}$ and $\dot{K_2}$ are performed and the results are substituted in (10) to generate $\hat{v}_{2\text{f}}(t)$ as:

$$\hat{v}_{2\text{f}}(t) = \left[\mu_1 Y_{\text{bus,dc}} \int \sin(2\omega t)\, dt\right] \sin(2\omega t) + \left[\mu_2 Y_{\text{bus,dc}} \int \cos(2\omega t)\, dt\right] \cos(2\omega t). \quad (16)$$

According to (16), the determined $\hat{v}_{2\text{f}}(t)$ has no dc offset. Now (11) is used to calculate $Y_{\text{bus,dc}}$.

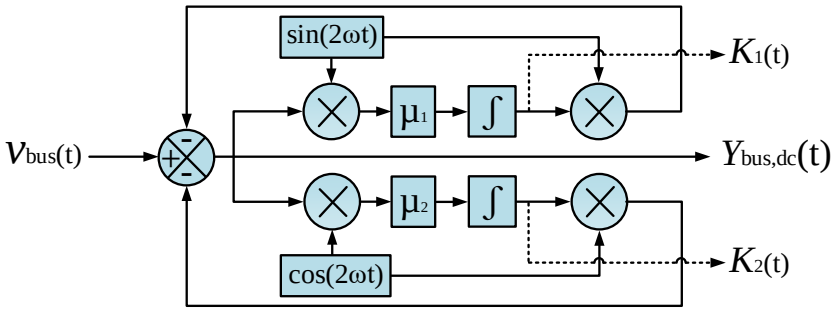


Fig. 3. Block diagram of the proposed dc-extraction method.

Figure 3 shows the block diagram of the proposed dc-extraction method. According to (10) and (11), $Y_{\text{bus,dc}}(t) = v_{\text{bus}}(t) - K_1 \sin(2\omega t) + K_2 \cos(2\omega t)$. Assuming $\mu_1 = \mu_2 = \mu$, two state variables x_1 and x_2 can be defined as follows:

$$x_1 = K_1 \sin(2\omega t) + K_2 \cos(2\omega t), \quad (17)$$

$$x_2 = -K_1 \cos(2\omega t) + K_2 \sin(2\omega t). \quad (18)$$

The derivative of (17) and (18) can be expressed as:

$$\dot{x_1} = \mu Y_{\text{bus,dc}} \sin^2(2\omega t) + 2\omega K_1 \cos(2\omega t) + \mu Y_{\text{bus,dc}} \cos^2(2\omega t) - 2\omega K_2 \sin(2\omega t), \quad (19)$$

$$\dot{x_2} = -\mu Y_{\text{bus,dc}} \sin(2\omega t)\cos(2\omega t) + 2\omega K_1 \sin(2\omega t) + \mu Y_{\text{bus,dc}} \cos(2\omega t)\sin(2\omega t) + 2\omega K_2 \cos(2\omega t). \quad (20)$$

Simplifying (19) and (20) results in $\dot{x_1} = \mu Y_{\text{bus,dc}} - 2\omega x_2$ and $\dot{x_2} = 2\omega x_1$. Accordingly, the open-loop transfer function of the algorithm from $\dot{x_1}$ and $\dot{x_2}$ to $Y_{\text{bus,dc}}$ is given by:

$$\begin{bmatrix} \dot{x_1} \\ \dot{x_2} \end{bmatrix} = \begin{bmatrix} 0 & -2\omega \\ 2\omega & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} \mu \\ 0 \end{bmatrix} Y_{\text{bus,dc}}. \quad (21)$$

Due to the fact that $Y_{\text{bus,dc}} = v_{\text{bus}} - x_1$, where $x_1 = \hat{v}_{2\text{f}}$ according to (11), the feedback coefficient of the algorithm is derived as:

$$B(s) = \frac{x_1(s)}{Y_{\text{bus,dc}}(s)} = \frac{\mu s}{s^2 + 4\omega^2}. \quad (22)$$

and the transfer function of the closed-loop system from $v_{\text{bus}}(s)$ to $x_1(s)$ is determined as:

$$H(s) = \frac{B(s)}{1+B(s)} = \frac{x_1(s)}{v_{\text{bus}}(s)} = \frac{\mu s}{s^2 + \mu s + 4\omega^2} \quad (23)$$

and accordingly the transfer function of the closed-loop system from $v_{\text{bus}}(s)$ to $Y_{\text{bus,dc}}(s)$ is determined as:

$$G_{\text{ANF}}(s) = \frac{Y_{\text{bus,dc}}(s)}{v_{\text{bus}}(s)} = \frac{s^2 + 4\omega^2}{s^2 + \mu s + 4\omega^2} \quad (24)$$

which is a second-order notch filter. Denoting $\mu \triangleq 4\zeta\omega$, where ζ is the damping of poles, the loci of poles of (24) when ζ varies between 0.05 to 0.8 are shown in Fig. 4. The settling time of the filter responses may be approximated by $t_s \approx 5/\mu$ for good values of ζ. For instance, for the gain of the algorithm equal to $\mu = 500$, the settling time is approximately $t_s \approx 10$ ms. For this value, ζ is approximately equal to 0.4. This design appears to be a desired starting point for the filter, in terms of giving it an adequate swiftness of its responses without causing excessive overshoots, and is used to implement and test the proposed dc-extraction method throughout this paper.

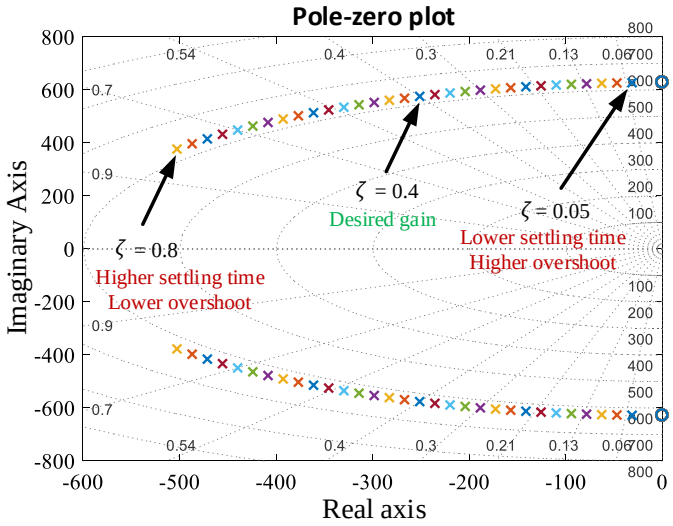


Fig 4. Movement of the notch filter's poles for $0.05 \leq \zeta \leq 0.8$.

This NF implementation has the great advantage that K_1 and K_2 are dc in nature and can be treated as internal state variables and used for further feedback signals to improve the performance of the dc-bus voltage loop as further explained below. The dynamical system of the proposed NF implementation can be expressed as:

$$\begin{bmatrix}\dot{K}_1(t)\\ \dot{K}_2(t)\end{bmatrix}=\begin{bmatrix}-\mu_1\sin^2(2\omega t) & -\mu_1\sin(2\omega t)\cos(2\omega t)\\ -\mu_2\sin(2\omega t)\cos(2\omega t) & -\mu_2\cos^2(2\omega t)\end{bmatrix}\begin{bmatrix}K_1(t)\\ K_2(t)\end{bmatrix}+\begin{bmatrix}\mu_1\sin(2\omega t)\\ \mu_2\cos(2\omega t)\end{bmatrix}v_{\text{bus}}(t). \quad (25)$$

The *Averaging Theorem* can be used to obtain the averaged system [15] by integrating (25) over a full cycle. This entails that

$$K_1(s)=\frac{\mu_1/2}{s+\mu_1/2}A_1, \quad (26)$$

$$K_2(s)=\frac{\mu_2/2}{s+\mu_2/2}B_1. \quad (27)$$

where A_1 and B_1 are defined in (9).

On the other hand, due to the fact that A_1 and B_1 are the amplitudes of the stationary quantities of $v_{\text{bus}}(t)$, and also considering the magnitude of the bus-voltage ripple given by (8), they can be represented by:

$$A_1=\frac{P_{\text{in}}}{2\omega C_{\text{bus}}V_{\text{bus,ref}}}, \quad (28)$$

$$B_1=\frac{Q_{\text{in}}}{2\omega C_{\text{bus}}V_{\text{bus,ref}}} \quad (29)$$

where P_{in} is the input active power and Q_{in} is the reactive power. Since $P_{\text{in}}=V_{\text{d}}I_{\text{d}}/2$ and $Q_{\text{in}}=V_{\text{d}}I_{\text{q}}/2$ in the form of DQ transformation, (28) and (29) can be expressed by:

$$A_1=\frac{V_{\text{d}}}{4\omega C_{\text{bus}}V_{\text{bus,ref}}}I_{\text{d}}, \quad (30)$$

$$B_1=\frac{V_{\text{d}}}{4\omega C_{\text{bus}}V_{\text{bus,ref}}}I_{\text{q}}. \quad (31)$$

This concludes that K_1 and K_2 contain the dynamics of I_{d} and I_{q} through a simple low-pass filter:

$$K_1(s)=\frac{\alpha\mu_1/2}{s+\mu_1/2}I_{\text{d}}, \quad (32)$$

$$K_2(s)=\frac{\alpha\mu_2/2}{s+\mu_2/2}I_{\text{q}}. \quad (33)$$

In (32) and (33), $\alpha=\frac{V_{\text{d}}}{4\omega C_{\text{bus}}V_{\text{bus,ref}}}$. Finally, it must be noted that the proposed method is frequency adaptive since the available phase-locked loop (PLL) supplies the angle ωt to the filter.

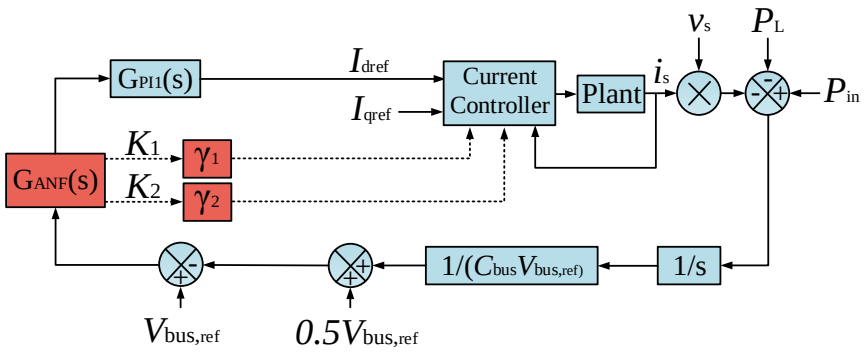


Fig 5. Proposed controller.

IV. Proposed Bus-Voltage Control Loop

This section presents the approach of designing a bus-voltage control loop via including the two state variables of the proposed dc-extraction method ($G_{\mathrm{ANF}}(s)$) to improve the dynamic response of a single-phase dc/ac controller.

A. Structure of the Proposed Bus-voltage Control Loop

The proposed control structure is shown in Fig. 5. The two state variables of $G_{\mathrm{ANF}}(s)$, K_1 and K_2, are used as the two additional proposed feedback variables to improve the system`s dynamic response. Two extra feedback gains [γ_1, γ_2] are used for the two new state variables. Figure 6 shows the LTI model of the current controller and the plant that represents a dc/ac converter with an L filter.

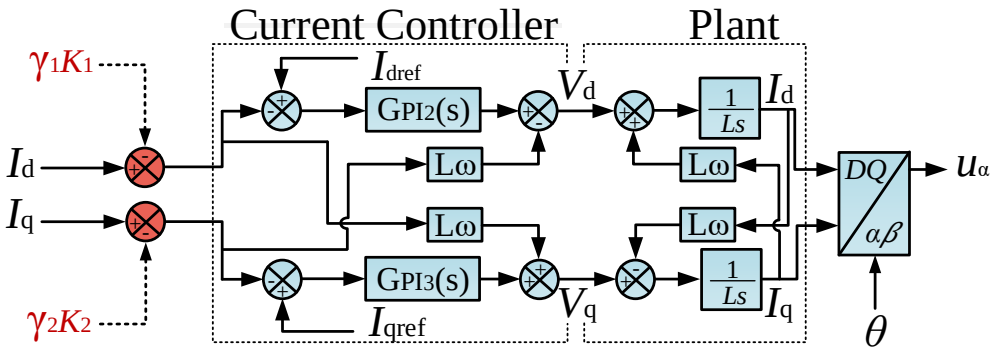


Fig 6. Current controller and plant with L filter.

The current-control loop operates based on the DQ transformation technique so that two PI controllers $G_{\mathrm{PI2}}(s)$ and $G_{\mathrm{PI3}}(s)$ regulate I_{d} and I_{q} to be matched with the two reference signals. The gains of $G_{\mathrm{PI2}}(s)$ and $G_{\mathrm{PI3}}(s)$ are selected based on the system`s model following a procedure presented in [16]. The gains of $G_{\mathrm{PI1}}(s)$ (the PI controller of the voltage control loop) are selected from

the characteristic equation of the LTI model of the bus voltage that is shown in Fig. 2(b). Accordingly, the characteristic equation of the voltage-control loop including $G_{\mathrm{ANF}}(s)$ is derived as:

$$1 - k\frac{V_{\mathrm{s}}}{2C_{\mathrm{bus}}V_{\mathrm{bus,ref}}}\left(1+\frac{1}{\tau s}\right)\frac{1}{s}G_{\mathrm{ANF}}(s) = 0. \qquad (34)$$

According to the Routh–Hurwitz table [17], (34) is in a stable region if $4\omega^2\tau > \mu - k\frac{V_{\mathrm{s}}}{2C_{\mathrm{bus}}V_{\mathrm{bus,ref}}}$, where μ is given in (24). Therefore, k and τ could be selected while the stability of the system is ensured.

Figure 7 shows the trajectory of the closed-loop poles of (34) when μ changes from 50 to 1000. As shown, the zeros and poles of the system are moving toward the negative region of the real axis, verifying the stability of the whole system for various selection of μ in the proposed dc-extraction algorithm.

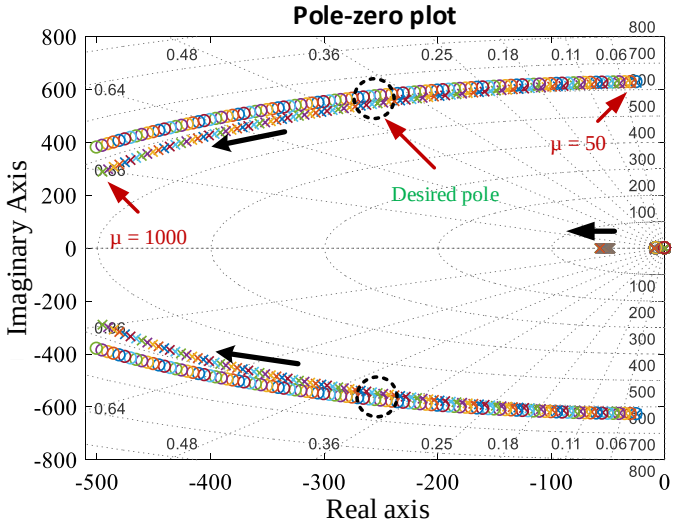


Fig 7. Movement of the closed-loop system`s poles for $50 \le \mu \le 1000$.

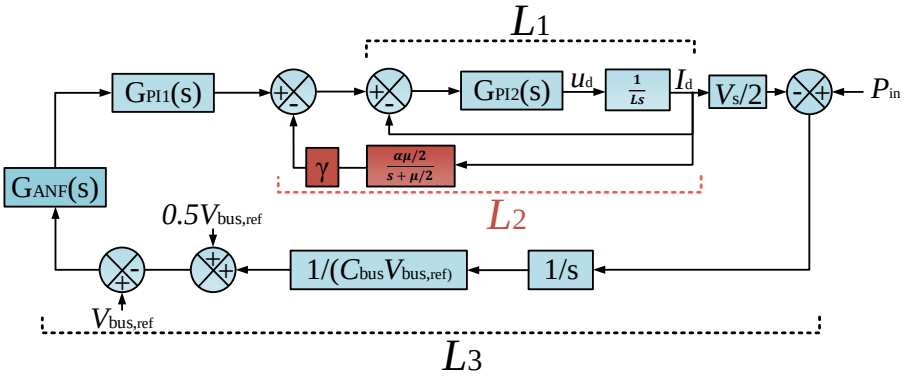


Fig 8. Simplified model for root-locus analysis.

B. Design of Proposed Feedback Gains

In this section, the gain γ selection for the proposed feedback loops, and how they improve the system dynamic, is presented using root-locus analysis. To do so, the LTI model of Fig. 5 is simplified as shown in Fig. 8. The model includes the voltage-control loop, $G_{\mathrm{ANF}}(s)$, current-control loop (D-axis) and the plant. The root-locus of the control block diagram of Fig. 8 is obtained using the characteristic equation of the system, which is expressed as follows:

$$1 + L_1 + L_2 + L_3 = 0 \;\rightarrow\; 1 + \frac{L_2}{1 + L_1 + L_3} = 0 \qquad (35)$$

where L_1, L_2 and L_3 are the three loop transfer functions shown in Fig. 8 and given by:

$$L_1 = \left[k_2\left(1 + \frac{1}{\tau_2 s}\right)\right]\left[\frac{1}{Ls}\right], \qquad (36)$$

$$L_2 = \left[k_2\left(1 + \frac{1}{\tau_2 s}\right)\right]\left[\frac{1}{Ls}\right]\left[\gamma\left(\frac{\alpha\frac{\mu}{2}}{s + \frac{\mu}{2}}\right)\right], \qquad (37)$$

$$L_3 = \left[k_1\left(1 + \frac{1}{\tau_1 s}\right)\right]\left[k_2\left(1 + \frac{1}{\tau_2 s}\right)\right]\left[\frac{1}{Ls}\right]\left[\frac{V_s}{2C_{\mathrm{bus}}V_{\mathrm{bus,ref}}}\frac{1}{s}G_{\mathrm{ANF}}(s)\right]. \qquad (38)$$

Figure 9 shows the loci of the roots of (35) versus the parameter γ increasing from 0 to 0.5 with a step-change of 0.005. The gain μ=500 as designed in Section III and the system parameters in Table I are used for this analysis. As Fig. 9(a) shows, when γ increases from zero, the low-frequency poles (dominant poles) and the higher-frequency poles start moving toward a better damping position. For instance, while γ increases from 0 to 0.3, the damping of the two low-frequency poles increases from 0.56 to 0.78, which corresponds to an overshoot reduction of 12% to 1.9% respectively (Fig. 9(b)). Similarly, the damping of the two higher-frequency poles increases from 0.42 to 0.45. This validates the contribution of the proposed feedback loop L_2 to improve the dynamic response of the voltage control loop.

From the loci of Fig. 9, it is concluded that the new feedback gain can improve the dynamics of the system provided that $0 < \gamma \leq 0.3$. Accordingly, γ=0.15 is selected as an appropriate gain for implementation and testing of the system throughout this paper. It should be noted that the same gain ($\gamma_1 = \gamma_2 = 0.15$) is used for the two proposed feedback loops in Fig. 5. In this section, the root-locus analysis of I_{q} control is ignored due to the fact the transient of the I_{q} control has minimum impact on the dynamics of the bus-voltage control loop.

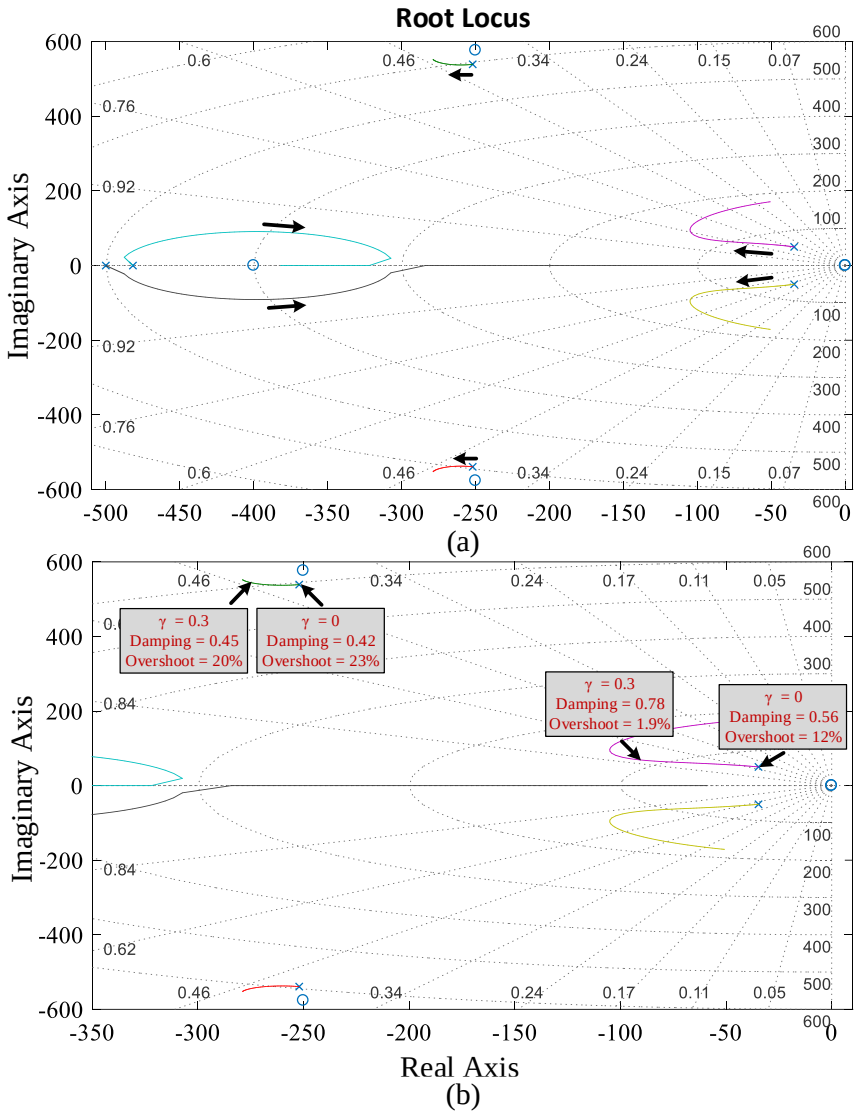


Fig 9. A) Loci of the roots of (35) versus γ increasing from 0 to 0.5 with the step-change of 0.005, b) zoomed version of part (a).

TABLE I. SYSTEM PARAMETERS OF THE DESIGNED SYSTEM

Circuit Parameter	Item	Value
v_s	AC line voltage	130 V
V_{bus}	DC-bus voltage	200 V
f	Line frequency	50 Hz
f_{sw}	Switching frequency	13 kHz
L_{f1}, L_{f2}	Filter inductors	2 x 1.4 mH
L_1, L_2	DC-side inductors	2 x 1.4 mH
C_{bus}	DC-bus capacitor	1.1 mF
Control Parameter	Item	Value
k_{p1}, k_{i1}	Gains of $G_{PI1}(s)$	-0.07, 50
k_{p2}, k_{i2}	Gains of $G_{PI2}(s)$	10, 400
k_{p3}, k_{i3}	Gains of $G_{PI3}(s)$	10, 400

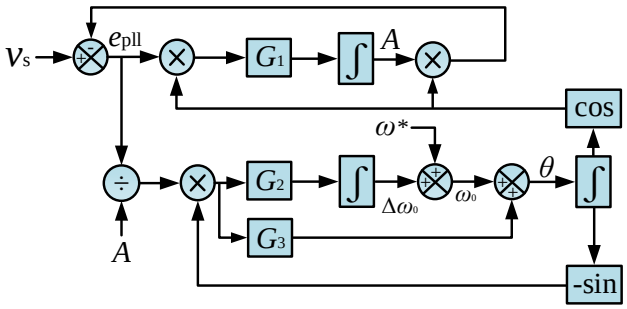


Fig 10. Block diagram of EPLL.

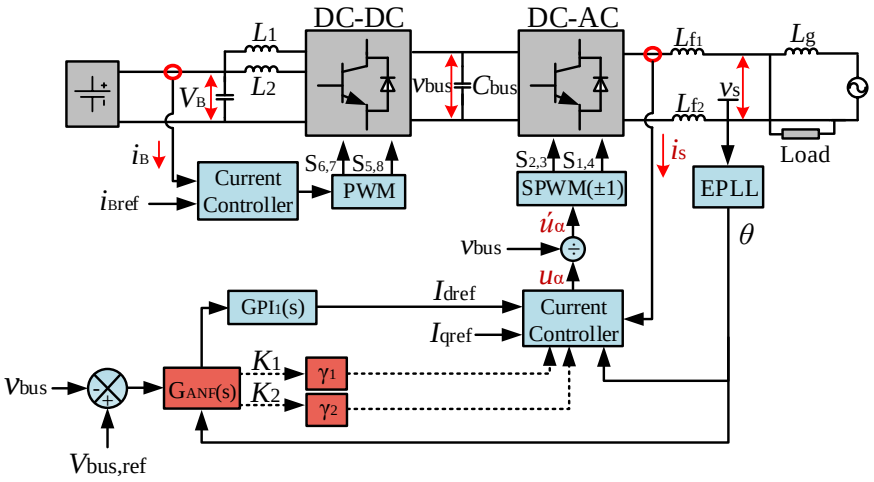


Fig 11. The designed system including the proposed dc-extraction method and the proposed feedback loops.

Figure 10 shows the algorithm of an Enhanced-Phased-Locked loop (EPLL) which is assigned to generate θ for $G_{\mathrm{ANF}}(s)$. The EPLL can accurately track the phase angle of the grid voltage v_{s} and send it to $G_{\mathrm{ANF}}(s)$, thus the proposed algorithm can operate in a frequency-adaptive mode. The design details of the EPLL are presented in [18, 19].

Figure 11 shows the studied system, which includes an H-bridge voltage-source dc/ac converter and an interleaved two-leg buck-boost dc/dc converter. The design of the converter is presented in [20]. Therefore, the design details are omitted in this paper. The proposed dc-extraction method, $G_{\mathrm{ANF}}(s)$, is utilized to remove the 2-f ripple of v_{bus}, thus isolating the control loop from such a disturbance. Otherwise, propagating the 2-f ripple into the current controller could cause 3$^{\mathrm{rd}}$ harmonics as well as phase deviation on the grid-side current, i_{s}. While $G_{\mathrm{ANF}}(s)$ is applied, not only the 2-f ripple is removed, but also the whole control system can be designed with larger bandwidth [13]. The direct application of angle from EPLL to the $G_{\mathrm{ANF}}(s)$ makes it frequency-adaptive.

V. Performance Evaluation of the Proposed DC-extraction Technique via Simulation Results

In this section, the dynamic reponse and steady-state performance of the proposed method is evaluated via several tests performed in MATLAB Simulink. First the dynamic response of the proposed method is tested and compared with the dc-observer in [11]. Then the proposed method and the conventional notch filter of [12] are compared in the single-phase dc/ac converter controller.

A. Dynamic Evaluation

Figure 12(a) shows a transient test of the proposed dc-extraction method and Fig. 12(b) shows the response of the dc-obsrever in [11] during a quick step-change of a bus voltage from 200 V→400V. While the two methods are tuned to achieve an equal settling time, their transient responses are compared. The proposed method exhibits lower oscillations. It should be noted that the high transient of the conventional method is already presented in [11, Page 4540].

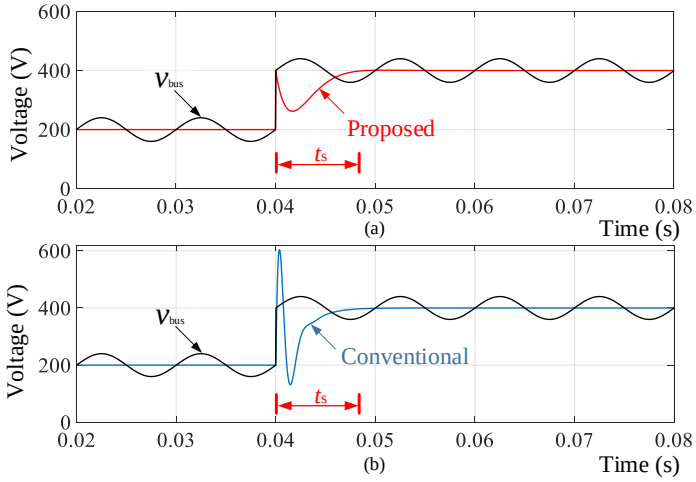


Fig 12. Transient responses during a bus-voltage command variation of 200 V→400V. a) proposed method, b) conventional dc-observer [11].

In another test, the proposed and the conventional NF are compared when they are applied to the voltage control loop of the single-phase dc/ac converter presented in Fig. 11. The voltage control loop that is used for this test is designed using the guidline presented in [13] to limit the maximum bus-voltage ripple by 5% of the nominal voltage value. Table I summarizes the system parameters which are used similarly for the two tested methods (proposed and conventional NF).

Figure 13 shows the result of this comparison during a bus-voltage variation of 400 V→500 V→400 V. Using the same testing platform and similar damping of 0.4 used for both $G_{\mathrm{ANF}}(s)$ in (24) and the conventional notch filter, the voltage control loop including the proposed technique exhibits a better dynamic response due to the three step-changes in bus voltage. This verifies the contribution of using the two proposed feedback loops and validates the root-locus analysis.

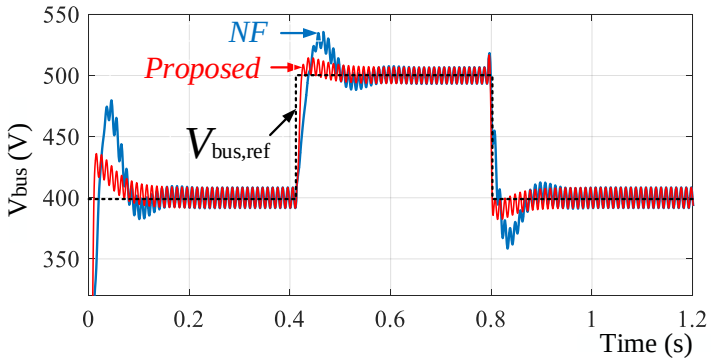


Fig 13. Dynamic responses of the proposed method and the conventional notch filter [12] during a bus-voltage command variation of 400 V→500 V→400 V.

Figure 14(a) shows the dynamic responses of the two systems during a startup bus voltage variation of 0 V→400V and Fig. 14(b) shows the converter`s output currents i_s. As can be seen, the oscillations of the bus voltage using NF translate into oscillations in the ac current while the proposed method exhibits much more stable current responses.

In another test in Fig. 15(a), the proposed method is tested against a higher disturbance of both bus-voltage command variation (400 V→500 V) and a power jump (1 kW→3 kW) at the same time. As shown, although the the proposed method exhibits a higher overshoot than the previous test due to the added disturbance of the power jump, its performance still shows better dynamics than the NF. Figures 15(b) and 15(c) show the converter`s output current using the proposed and the conventional NF respectively.

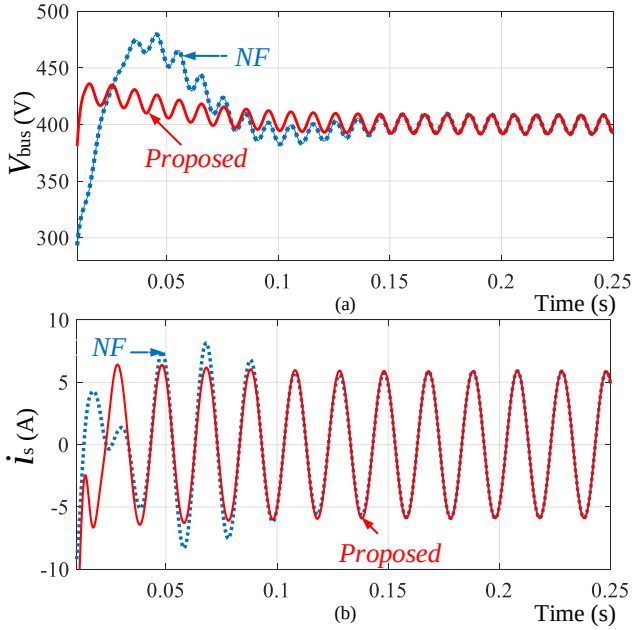


Fig 14. Comparing the dynamic responses of the proposed method and the conventional notch filter in [12] during a startup bus voltage variation. a) bus voltages, b) converter`s output currents.

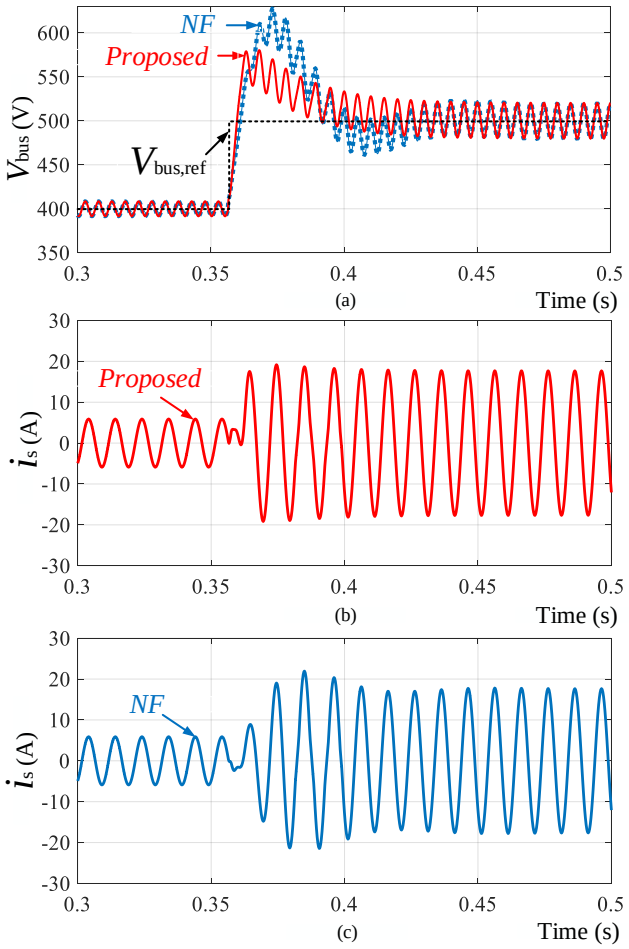


Fig 15. Comparing the dynamic responses of the proposed method and the conventional notch filter in [12] during simultaneous bus-voltage variation of 400 V→500 V and input power of 1 kW→3 kW. a) bus voltages, b) converter`s output current (proposed method), c) converter`s output current (conventional NF).

B. Steady-state Evaluation

Figure 16 shows the steady-state response of the proposed method and its ripple-cancellation feature via comparing i_s before and after applying the proposed method. As Fig. 16(a) shows, after applying the proposed method to the control system of the dc/ac converter, the 3rd harmonic is completely removed from i_s, whereas i_s includes the 3rd harmonic when the system excludes the proposed method (Fig. 16(b)). Such a 3rd harmonic elimination is shown and confirmed in Fig. 16(c) by means of the Fast Fourier Transform (FFT) of i_s before and after applying the proposed method.

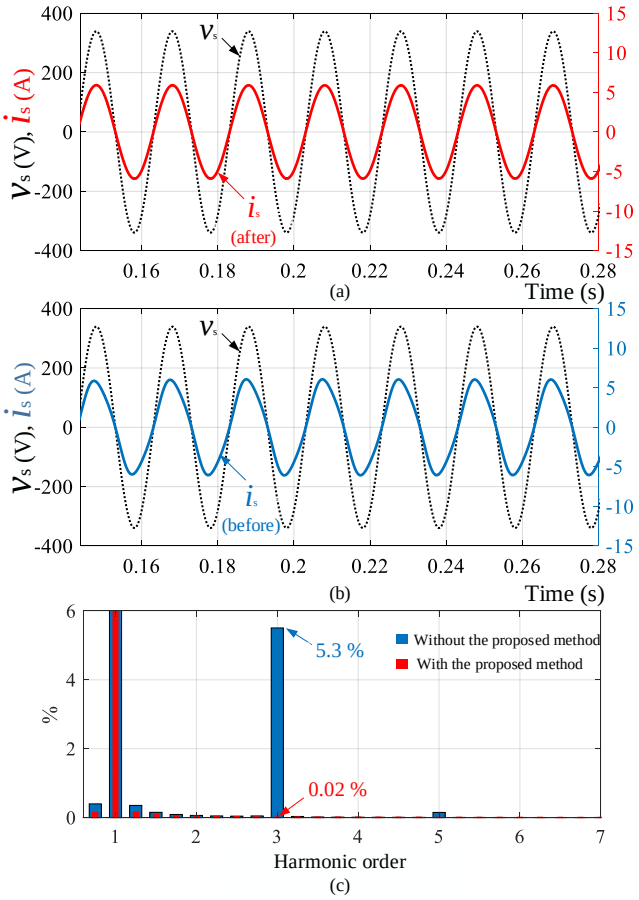


Fig 16. Steady-state response of the proposed method and its ripple cancellation feature. a) grid voltage v_s, and grid-side current i_s after applying the proposed dc-extraction method, b) v_s and i_s before applying the proposed dc-extraction method, c) FFT of i_s before and after applying the proposed method.

Figure 17(a) shows the system`s operation during load switching from 3 kW to 1 kW, that changes V_{ripple} from 25 V to 8.4 V respectively (according to (8)). As shown, when the proposed method is used, the bus voltage exhibits lower fluctuation during such a disturbance. Figure 17(b) compares the dynamic responses of the two systems during load switching from 1 kW to 3 kW. As shown, when the input power increases, the proposed system exhibits improved dynamic response than the conventional system.

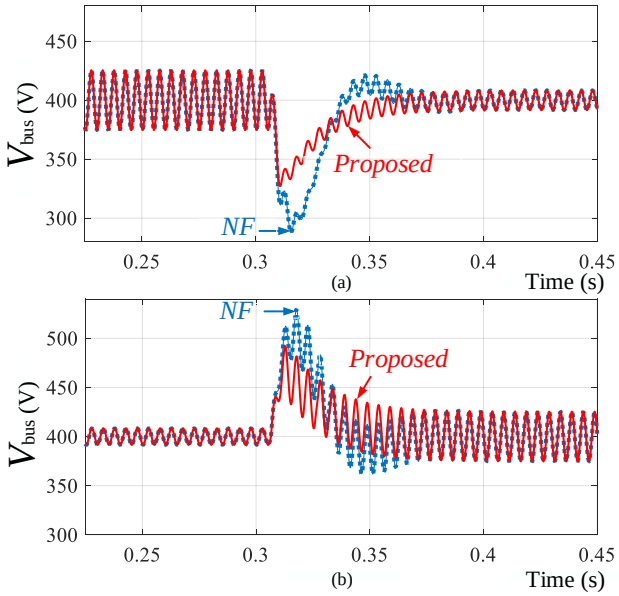


Fig 17. Dynamic responses of the proposed method in comparision with the conventional notch filter [12]. a) during load variation of 3 kW→1 kW, b) during load variation of 1 kW→3 kW.

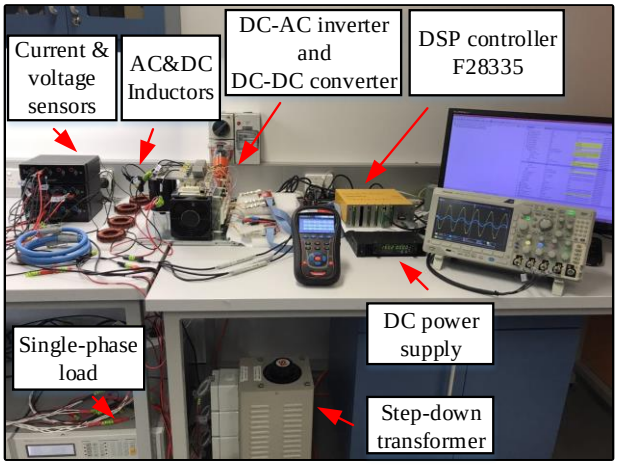


Fig 18. Experimental setup.

VI. Performance Evaluation of the Proposed DC-extraction Method via Experimental Results

The aim of the experimental tests is to validate the simulation results, and to show the robustness of the proposed system in a real system and in the presence of noise. The proposed method is evaluated by both stand-alone and grid-connected testing. The stand-alone tests are performed to show the individual dynamic response of the proposed dc extraction (Fig. 3) as well as its frequency-adaptive performance. The grid-connected tests are carried out to show the influence of the proposed method on the dynamic of the whole voltage control loop and validate the mathematical analysis as well as the simulation results.

For stand-alone testing, emulated system components, the bus voltage v_{bus}, grid voltage v_{s} and grid current i_{s} are internally generated by a TMSF28335 controller via programing in C-language and sent to digital-to-analog converter (DAC) through a serial peripheral interface (SPI). For grid-connected testing, the proposed system in Fig. 11 is implemented and investigated. Figure 18 shows the laboratory prototype of the system, and its parameters are summarized by Table I. A four-leg SEMISTACK – IGBT is used as the dc/ac and dc/dc converters. A Chroma 63800 electronic load, a Sorensen XG 600-1.4 programmable dc power supply and an MI 2883EU Class S power quality analyzer are also used for experimental testing.

A. Stand-alone Testing

Figure 19 shows the response of the proposed algorithm (Fig. 3) during a step change of v_{bus} from 400 V to 450 V. As shown, the proposed dc-extraction method tracks perfectly the bus voltage v_{bus} and generates its dc offset during the rising step change. The grid frequency is fixed at 50 Hz for this test. The result of this test validates the simulation results in Fig. 12(a).

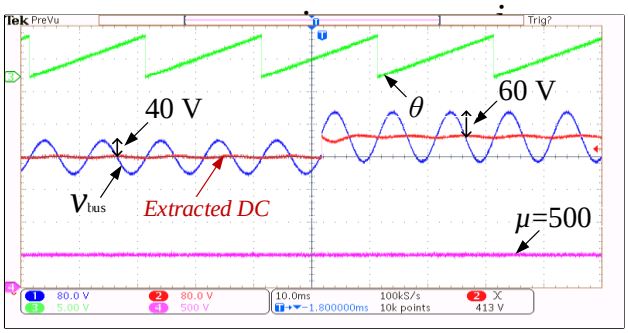
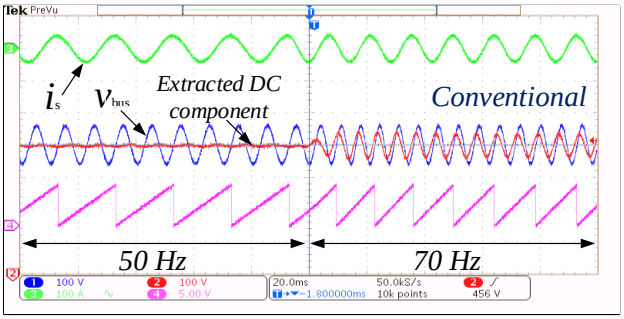
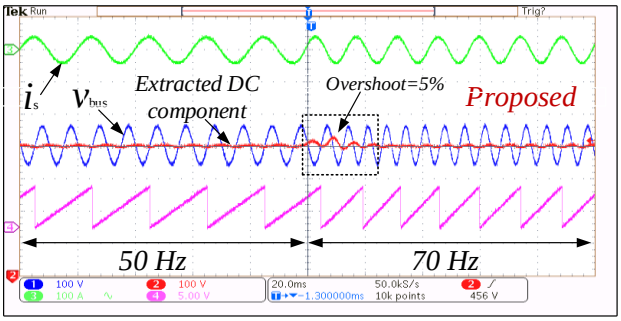


Fig 19. Experimental results of the dynamic response: $V_{\text{bus,ref}}$ increases from 400 V to 450 V. Bus voltage v_{bus} (Ch.1 80 V/div) and its estimated dc (Ch.2 80 V/div), EPLL`s output θ (Ch.3 5 V/div) and μ (Ch.4 200 V/div).

In another test, the grid frequency is rapidly changed from 50 Hz to 70 Hz and the response of the proposed method is compared with the conventional non-adaptive NF in [12]. The conventional NF (Fig. 20(a)) which is tuned at the center frequency (50 Hz) exhibits mal-operation at the different frequency (70 Hz), whereas the proposed method in Fig. 20(b) is able to track the frequency deviation and tune its bandwidth to generate the dc value of v_{bus}. The EPLL in Fig. 10 is used for generating θ so that no extra algorithm needs to be added to the design of the converter. In this paper such an exaggerated frequency deviation (+20 Hz) is used to show the robustness of the system in a visible way.



(a)



(b)

Fig 20. Experimental results of the dynamic response during frequency deviation of +20 Hz. v_{bus} (Ch.1 100 V/div), estimated dc component (Ch.2 100 V/div), i_{s} (Ch.3 100 A/div), EPLL`s output θ (Ch.4 5 V/div). a) conventional non-adaptive NF [12], b) proposed method.

B. Testing the Proposed Method in a Grid-connected Single-phase DC/AC Converter

The designed system in Fig. 11 that includes the proposed control method is implemented and its performance is evaluated in this section. Figure 21 shows the steady-state performance of the system and compares the responses before and after applying the proposed dc-extraction method. As Fig. 21(a) shows, V_{ripple}= ±5.6 V is placed on v_{bus} which is consistent with the theoretical calculation of (8). As shown, such a ripple is translating as 3$^{\text{rd}}$ harmonic on the converter output current, i_{s}. In Fig. 21(b) the 2-f ripple is completely removed from the bus voltage and the 3$^{\text{rd}}$ harmonic is subsequently minimized which verifies the simulation results of Fig. 16(a). The FFT of i_{s} is shown in Fig. 21(c) before and after applying the proposed method. As also shown, the proposed dc-extraction method does not affect the existing system noise, validating its robustness and the independency of its operation in the presence of other disturbances, in terms of removing the 2-f ripple.

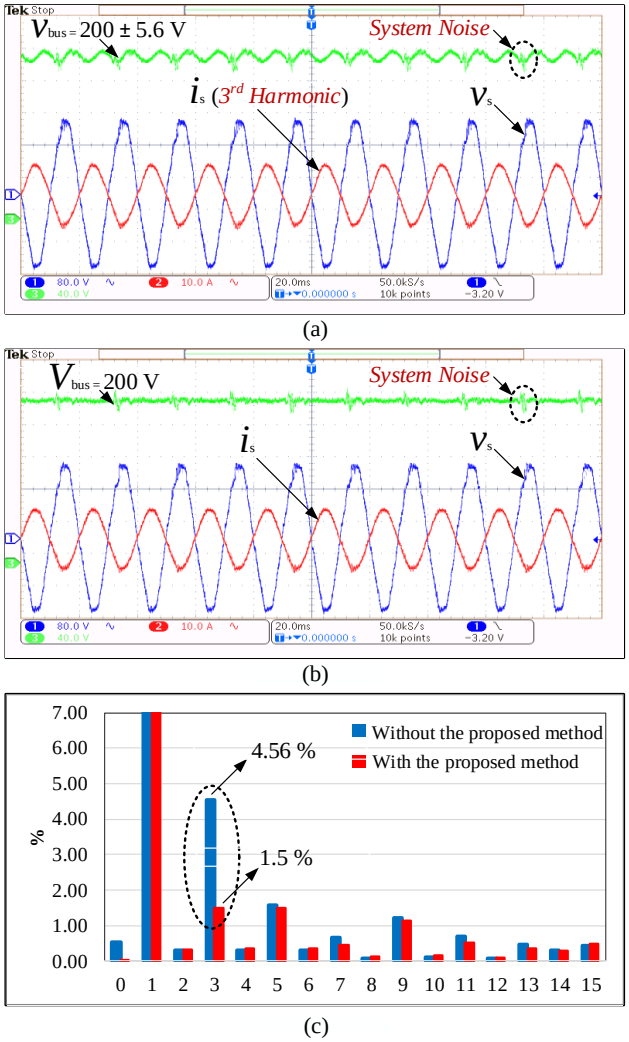
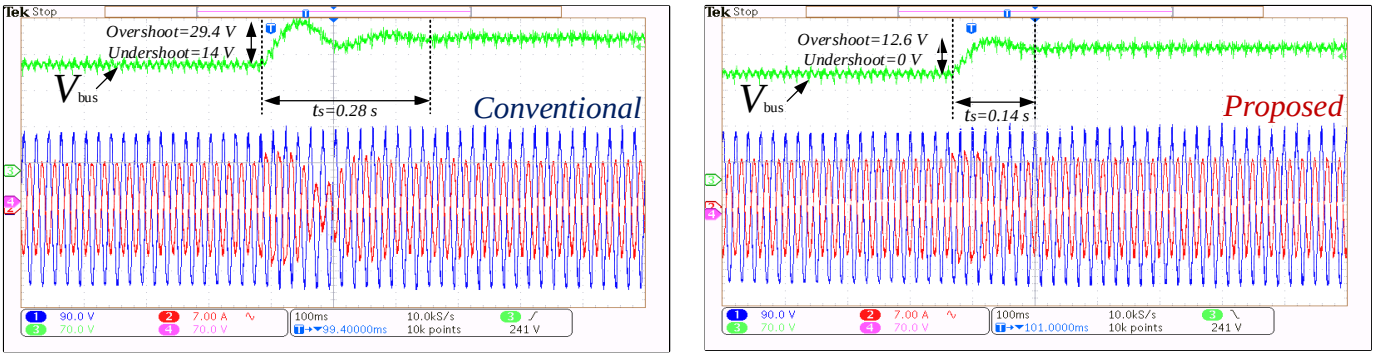


Fig 21. Experimental results of the steady-state response before and after operation of the proposed dc-extraction method. Grid voltage v_s (Ch.1 80 V/div), grid-side current i_s (Ch.2 10 A/div), bus voltage v_{bus} and $V_{bus,dc}$ (Ch.3 40 V/div). v_s=130 Vrms, $V_{bus,ref}$=200 V, P^*=780 W. a) before applying the proposed dc-extraction method, b) after applying the proposed dc-extraction method, c) FFT of i_s before and after applying the proposed method generated by MI 2883EU Class S power quality analyzer.

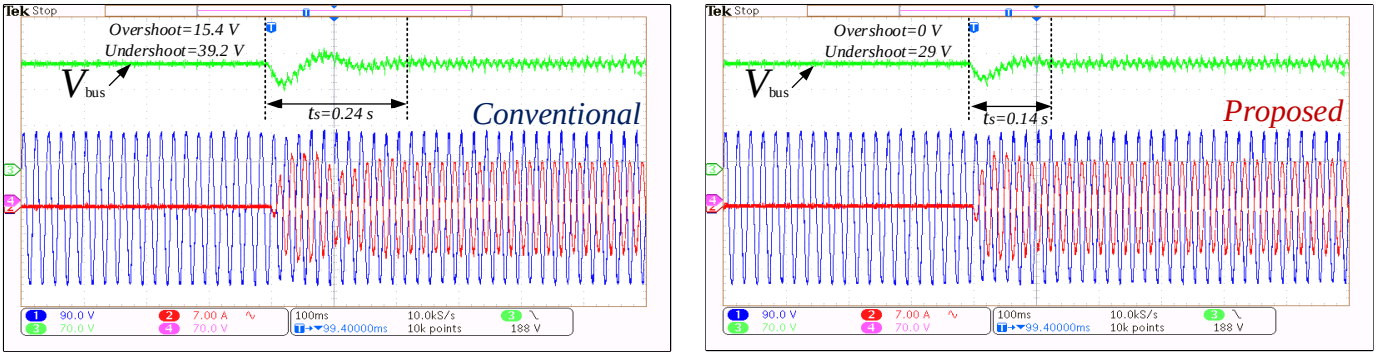
In another test, in Fig. 22, the dynamic response of the system in the grid-connected mode using both the proposed method and the conventional NF in [12] is evaluated during a bus-voltage variation of 200 V→250 V. In this test, the injected power is fixed at 780 W. As shown, using the proposed method in Fig. 22(b), both the bus voltage and the grid-side current i_s show much better dynamic responses compared with v_{bus} and i_s in Fig. 22(a). The result of this test revalidates the simulation result of Fig. 13 and Fig. 14.



(a) (b)

Fig 22. Experimental results of the dynamic response during bus voltage variation v_{bus}=200 V → 250 V while P^*=780 W. Grid voltage v_s (Ch.1 90 V/div), grid-side current i_s (Ch.2 7 A/div), v_{bus} (Ch.3 70 V/div). a) conventional NF [12], b) proposed method.

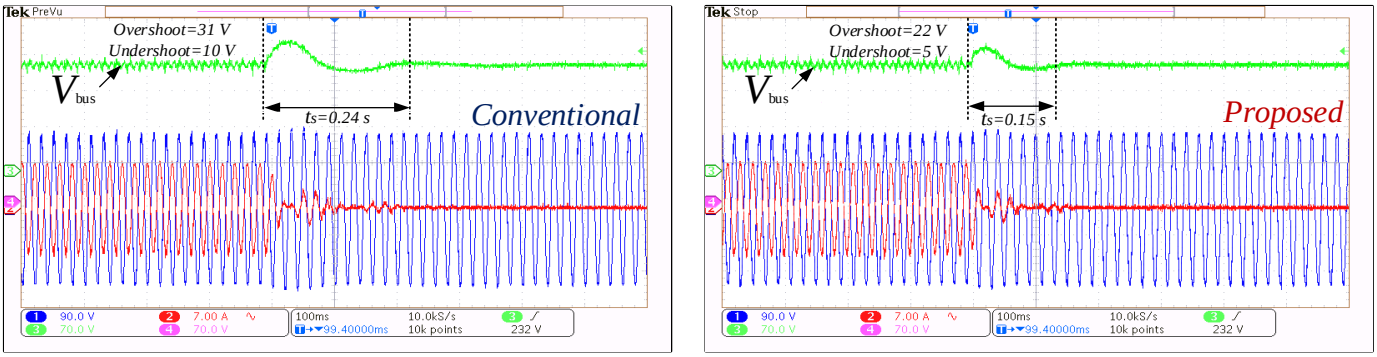
Figure 23 shows the dynamic performance of the system during a power jump of 0 W→780 W while the bus voltage is regulated at 200 V. This test also shows the better dynamic response of the control system when the proposed method is used. The result of this test revalidates the simulation results of Fig. 17(a).



(a) (b)

Fig 23. Experimental results of the dynamic response during power jump P^*= 0 W → 780 W while v_{bus}=200 V. Grid voltage v_s (Ch.1 90 V/div), grid-side current i_s (Ch.2 7 A/div), v_{bus} (Ch.3 70 V/div). a) conventional NF [12], b) proposed method.

Finally, in the last test, the transient of the system is shown when the load is disconnected, reducing the power from 780 W→0 W. Such a quick switching off the load causes an inevitable transient, mainly on v_{bus}. However, when the system uses the porposed technique, this tranient is significantly lower as shown in Fig. 24(b). The results of this test are consistent with the simulation results in Fig. 17(b).



(a) (b)

Fig 24. Experimental results of the dynamic response during power jump P^*= 780 W → 0 W while v_{bus}=200 V. Grid voltage v_s (Ch.1 90 V/div), grid-side current i_s (Ch.2 7 A/div), v_{bus} (Ch.3 70 V/div). a) conventional NF [12], b) proposed method.

VII. Conclusion

This paper identifies a time-varying implementation of the second-order notch filter (NF) and, subsequently, adds two additional internal feedback loops to enhance the transient responses of single-phase grid-connected dc/ac converters (including both rectifiers and inverters). The new feedback loops do not require any additional measurements and they are only based on internal NF variables. A method for designing the proposed feedback gains is also developed. The simulation results verify the superior dynamic and steady-state performance of the proposed controller compared with conventional methods. The proposed technique is also adaptive with frequency via receiving synchronization data directly from the PLL. As a result, no extra frequency-detection algorithm needs to be added to the design of a converter. The experimental results are also presented to confirm the analytical and simulation results.

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