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# Graphene growth on silicon carbide: a review

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Graphene has been widely heralded over the last decade as one of the most promising nanomaterials for integrated, miniaturized applications spanning from nanoelectronics, interconnections, thermal management, sensing, to optoelectronics. Graphene grown on silicon carbide is currently the most likely candidate to fulfill this promise. As a matter of fact, the capability to synthesize high-quality graphene over large areas using processes and substrates compatible as much as possible with the well-established semiconductor manufacturing technologies is one crucial

requirement. We review here the enormous scientific and technological advances achieved in terms of epitaxial growth of graphene from thermal decomposition of bulk silicon carbide and the fine control of the graphene electronic properties through intercalation. Finally, we discuss perspectives on epitaxial graphene growth from silicon carbide on silicon, a particularly challenging area that could result in maximum benefit for the integration of graphene with silicon technologies.

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**1 Introduction** Graphene is a two dimensional single atomic layer of  $sp^2$  bonded carbon atoms arranged in a honeycomb lattice. It is considered as the basic building block for all carbon allotropes such as 0D fullerenes, 1D carbon nanotubes and 3D graphite. Therefore, graphene is often used as a first approach to theoretically describe properties of the other carbon allotropes. The first pioneering theoretical investigation of graphene and its band structure was performed by P. R. Wallace in 1947 [1]. Nearly 57 years later, single-layer graphene was successfully isolated via mechanical exfoliation methods by Geim and Novoselov in 2004 at the University of Manchester [2]. They received the Nobel Prize in Physics in 2010 for groundbreaking experiments on graphene.

Graphene exhibits a number of interesting properties such as high electron mobility at room temperature (250,000  $\text{cm}^2/\text{Vs}$ ), remarkable optical transparency (2.3%), exceptional thermal conductivity (5000  $\text{Wm}^{-1}\text{K}^{-1}$ ) and superior mechanical properties with Young's modulus up to 2.4 TPa [3-7]. Its potential applications include flexible

electronics, optoelectronics, bio-sensing, nanocomposites and energy storage devices such as supercapacitors and lithium ion batteries [8-16]. Furthermore, the peculiar band structure of graphene makes it different from any other material. The conduction and valence bands in graphene meet in 6 single points (Dirac points) at the corners of the Brillouin Zone. For low carrier energies, the bands feature a linear dispersion  $E = \hbar k v_F$ , where  $v_F$  represents Fermi velocity and is about  $1 \times 10^6$  m/s [17]. This linear dispersion relation suggests that the electrons behave as "massless". Since it lacks a bandgap, graphene is described as a semi-metal. Several other unusual phenomena have been observed, such as the anomalous quantum Hall effect, anomalous Berry's phase, suppression of weak localisation, and quantum confinement [18-21]. Such extraordinary phenomena have generated tremendous interest in the scientific community thanks to the extraordinary technological implications, as well as to the possibility of fully understanding the novel science unlocked by two-dimensional materials.

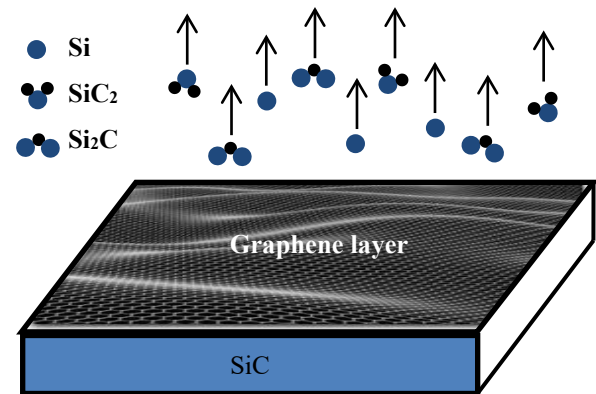
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In this review article, first, we briefly discuss various graphene growth techniques along with their potential applications and drawbacks. Thereafter, we provide a comprehensive scientific progress of graphene growth on silicon carbide (SiC) to date and evaluate its future perspective. After that, we discuss the advantage of growing graphene on heteroepitaxial cubic silicon carbide (3C-SiC) on large area silicon (Si) substrates. Thermal decomposition and metal-mediated graphene growth on 3C-SiC on Si will be further discussed in detail. Finally, the article concludes with a brief discussion on the impact of graphene growth on SiC in connection to future technology.

**2 Graphene growth techniques** Since graphene was isolated first time in 2004 [2] several techniques have been demonstrated to produce high quality graphene for next-generation electronics applications. The most common techniques are micromechanical exfoliation of single crystal graphite [2], chemical vapor deposition (CVD) growth on transition metals and dielectric insulators [22-24], chemical reduction of graphite oxide (GO) [25], carbon nanotubes (CNTs) unzipping [26], and high temperature thermal decomposition of silicon carbide (SiC) [27]. Among these, micromechanical exfoliation of graphite, CVD growth on transition metals and high temperature thermal decomposition of SiC has gained colossal interest in scientific community.

Micromechanical exfoliation of graphite is the commonly used technique to produce the highest quality graphene with the best device characteristics. Carrier mobility in excess of  $\sim 200,000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  has been reported for suspended single layer exfoliated graphene at room temperature [28,29]. However, when transferred onto the  $\text{SiO}_2$  substrates, scattering of electrons by optical phonons of the substrate limits the mobility value to  $\sim 40000 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  [30]. Unfortunately, this method is not appropriate for industrial scale production, suffering from a cumbersome labour intensive process of transfer, and investigation. Further, the thickness, the size, and the distribution of the graphene layers cannot be controlled at a large scale. Therefore, undoubtedly a more scalable technique is required.

CVD growth on transition metals seems promising to produce high quality graphene, potentially on a large scale. In this method, carbon-containing gases such as methane, ethane, or propane, decomposes on the catalytic metal (Ni, Ru, Ir, Cu, Co etc.) surfaces at high-temperature and converts into graphene [31-35]. After growth, the graphene layer needs to be transferred onto an appropriate substrate for characterization. Typical mobility values recorded for the CVD-grown graphene are in the range of 1000 to  $25,000 \text{ cm}^2/\text{Vs}$  [36]. Herein, the dominant scattering mechanisms are dislocations, grain boundaries, and other substrate-related features. Using this CVD process, graphene can be grown on a large metal surface compared to exfoliated graphene. Bae *et al.* has demonstrated a roll-to-roll production of 30 inch graphene film for transparent elec-



**Figure 1** Growth of epitaxial graphene on silicon carbide wafer via sublimation of silicon atoms. (Adapted from Reference 42)

trodes using the CVD method [22]. The single layer graphene produced via this technique showed a sheet resistance value  $\sim 125 \Omega/\square$  with  $\sim 97.4\%$  optical transmittance. Whereas, a stack of doped four layer graphene has demonstrated sheet resistance values as low as  $\sim 30 \Omega/\square$  with  $\sim 90\%$  transparency, which is superior to commercially available transparent electrodes such as indium tin oxides [22]. Although the CVD growth shows aforementioned advantages, the graphene still needs to be transferred onto an insulating substrate. Furthermore, the graphene may be contaminated with metals, which can degrade the performance of graphene-based electronic devices. Therefore, a transfer-free method for fabricating large-area single-crystalline graphene domains is needed to overcome these setbacks.

Thermal decomposition of SiC has been intensively studied lately as a promising route for obtaining highly reproducible and homogenous large-area graphene for electronic applications [37]. The main advantage of thermal decomposition of SiC over other conventional techniques is that the graphene layers can be directly obtained on a commercially available semiconducting or semi-insulating substrate, so no transfer is required before processing electronic devices [37-41]. In this method, a commercially available SiC sample is annealed at high temperature (more than  $1400^\circ\text{C}$ ) in vacuum or under atmospheric pressure conditions. Since the vapour pressure of carbon is negligible compared to the silicon [37], at high temperature silicon atoms evaporate and leave behind carbon atoms on the surface, which subsequently rearranges to form graphitic layers (Fig. 1) [42].

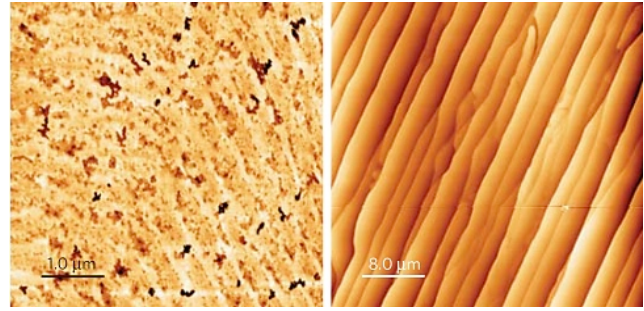
Epitaxial graphene on SiC is considered as a potential material for high-end electronics that might be able to surpass silicon in terms of key parameters such as feature size, speed, and power consumption [43]. Graphene/SiC based electronic devices are believed to have promising potential for future high-frequency applications [44]. In addition, graphene on SiC can be an ideal platform for structured graphene such as transducers and membranes that are directly grown on patterned SiC on Si substrates, discussed in section 4.2 of this article.

**3 Thermal decomposition of bulk SiC** The thermal decomposition of hexagonal SiC (bulk) was first reported by Badami in 1965 [45]. In his experiments, the SiC crystals were annealed to high temperature (in excess of  $\sim 2180$  °C) for an hour in vacuum to obtain a graphite lattice on top. Various stages in the development of this graphite lattice were analyzed using X-ray diffraction methods and a mechanism of decomposition of the SiC proposed. A decade later in 1975, Bommel *et al.* demonstrated the formation of monolayer graphite on both the C-face and the Si-face of hexagonal SiC at a temperature as low as 800 °C in ultra-high vacuum (UHV) [46]. They suggested that collapse of carbon atoms of three successive SiC layers results in the formation of one graphitic layer. Note that graphene was referred as monolayer graphite in these early reports.

Although the epitaxial growth of graphene on SiC had been known for longtime [46], its electronic properties remained unknown until the early 21<sup>st</sup> century. In 2004, De Heer *et al.* at the Georgia Institute of Technology performed first transport measurements on multilayer epitaxial graphene grown via thermal decomposition of SiC in ultra-high vacuum [27,37]. They revealed the Dirac nature of the charge carriers and found the mobility values exceeding to  $\mu = 1,100$  cm<sup>2</sup>/Vs in graphene on SiC. Higher mobility values further obtained by improving the quality of graphene [37,47]. In addition, the discovery of fractional quantum Hall effect, observation of 2D electron gas behavior along with the appealing possibility to incorporate the existing silicon technology to mass produce and pattern epitaxial graphene makes it an appealing material for future electronics.

Even though the thermal decomposition of SiC in high/ultrahigh vacuum appears promising for large scale production of graphene based devices, graphene grown via this technique consists of small grains (30-200 nm) with varying thickness [48,49]. These small-grain structures are formed due to morphological changes of the SiC surface in the course of high-temperature annealing. The quality of graphene produced in high/ultra-high vacuum is poor due to the high sublimation rates at relatively low temperatures. Therefore, a more controllable technique is required to overcome this problem.

Emtsev *et al.* in 2009 demonstrated a novel approach to obtain morphologically superior graphene layers on the SiC surface [38]. This method involves annealing the SiC samples at high temperature ( $>1650$  °C) in an argon environment. The presence of this high pressure of argon reduces the Si evaporation rate [50]. This is because the silicon atoms desorbing from the surface have a finite probability of being reflected back to the surface by collision with argon atoms. The high growth temperature further enhances surface diffusion such that the restructuring of the surface is completed before graphene formation. This finally leads to a significant improvement in the surface mor-



**Figure 2** AFM image of graphene grown on 6H-SiC(0001) by annealing in (a) ultrahigh vacuum at a temperature of about 1280 °C and (b) Ar environment (900 mbar of pressure) at 1650 °C. (Adapted from Reference 38)

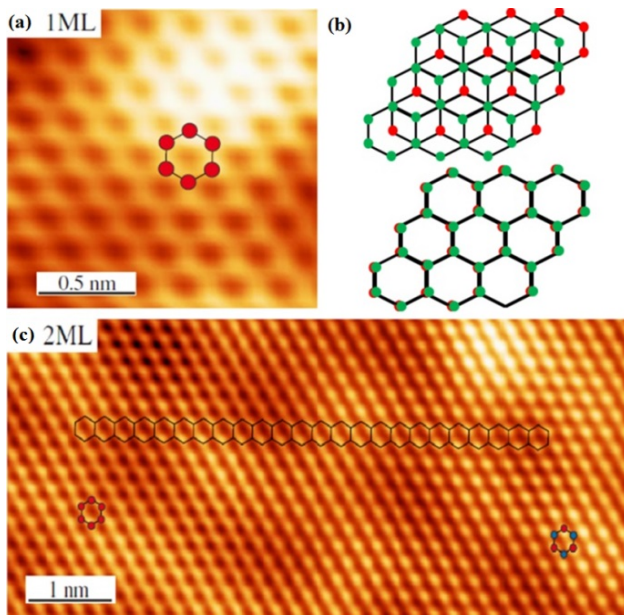
phology of graphene on SiC. Fig. 2 compares the surface morphology (AFM) of the monolayer graphene grown on 6H-SiC(0001) via thermal decomposition in UHV with the graphene grown in an argon environment [38]. It is obvious from the AFM images that the Ar-mediated growth results in a superior morphology compared to the UHV graphitization. Furthermore, the graphene domains obtained in an Ar environment were much larger in size ( $3 \mu\text{m} \times 50 \mu\text{m}$ ). Later, several researchers demonstrated a wide range of domain size, with reports as large as  $50 \mu\text{m} \times 50 \mu\text{m}$  [51,52].

After the discovery of Ar-assisted thermal decomposition of SiC, other techniques such as the confinement controlled sublimation (CCS) method [37] and annealing in presence of an external Si flux [53] have been suggested to further improve the quality of epitaxial graphene. In the case of the CCS method, high-quality graphene layers (single or multiple) are obtained in a near-equilibrium environment [37,43]. Herein, a SiC sample is placed in a graphite enclosure equipped with a small leak. The graphene growth rate is regulated by controlling the evaporation rate of silicon through the leak [37]. While in the Si flux method, quality of the graphene is controlled by controlling the Si vapour pressure using disilane gas [53].

Epitaxial graphene can be grown on either of the two polar faces of a SiC crystal. The growth rate and the electronic properties found to be dependent on the specific polar SiC crystal face. Bommel *et al.* first reported the difference between graphene grown on the C-terminated face ( $000\bar{1}$ ) and the Si-terminated face (0001) [46]. Their low-energy electron diffraction (LEED) results revealed the crystallographic orientation relation between the SiC and the graphene layer. A monocrystalline graphene film is obtained on the SiC(0001), with the unit mesh rotated  $30^\circ$  with respect to the SiC unit cell ( $6 \times \sqrt{3}$  structure). In contrast, a polycrystalline graphene film was found on the SiC( $000\bar{1}$ ) [46,54]. In addition, the rate of graphene growth on the SiC(0001) was found to be much slower compared to the SiC( $000\bar{1}$ ) [37]. A detailed discussion on the understanding of graphene grown on both Si- and C-terminated faces is presented in the following subsections.

**3.1 Graphene growth on Si-face of SiC** A number of groups have succeeded in growing large-area, single crystalline monolayer (ML) graphene on SiC(0001) with good reproducibility [38,55,56]. It was reported that the graphene layer is not directly grown on top of the substrate but rather on a complex  $(6\sqrt{3} \times 6\sqrt{3})R30^\circ$  non-conducting, carbon-rich interfacial layer [43,57-60], which is partially covalently bonded to the underlying SiC substrate. This interfacial layer acts as an electronic ‘‘buffer’’ layer between the graphene films and SiC substrate and provides a template for subsequent graphene growth. Since this buffer layer forms a noninteracting interface with the graphene layers on top of it, monolayer graphene grown on SiC(0001) is electronically identical to a freestanding graphene layer [43]. A detailed discussion on decoupling this buffer layer by intercalation is further presented in section 3.3.

Fig. 3 shows the scanning tunneling microscopy (STM) images of the monolayer (1ML) and bilayer (2ML) epitaxial graphene grown on SiC(0001) [58]. Monolayer graphene revealed a perfect hexagonal structure with six protrusions, highlighted by red dots in Fig. 3a. Such observation is expected for graphene, where the two atoms per unit cell are equivalent and lead to a symmetric appearance in STM. The observed hexagonal pattern seems analogous to the exfoliated graphene on SiO<sub>2</sub>, a characteristic of linear band structure. On the other hand, multilayer graphene grown on the SiC(0001) surface is Bernal stacked and follows either AA' or AB stacking sequence (Fig. 3b) [58].



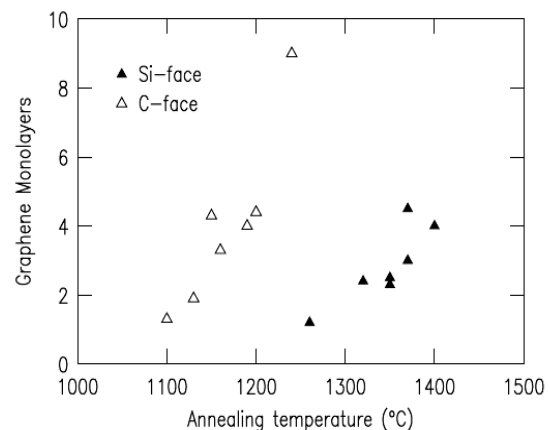
**Figure 3** (a) STM image of monolayer graphene grown on SiC(0001). (b) Schematic of atoms arranged in AB and AA' stacking sequence in a bilayer graphene. (c) STM image of bilayer graphene. Red and red-blue hexagon representing AA' and AB stacking sequences respectively. (Adapted from Reference 58)

Fig. 3c displays the atomically resolved STM image of bilayer graphene (2ML) [58]. The left (red) and right (red-blue) hexagons illustrates the two graphene layers arranged in AA' and AB stacking sequences respectively.

Norimatsu *et al.* and Luxmi *et al.* independently reported that the number of graphene layers on the SiC(0001) can be controlled by controlling the growth parameters such as annealing temperature and time [56,61,62]. Fig. 4 displays the relationship between the numbers of graphene layers and annealing temperatures [56]. It is clear from the plot that the number of layers increases with increasing the annealing temperature. Norimatsu *et al.* also suggested that an extended sintering time at a lower temperature is more effective in producing uniform graphene layer than a simple increase in the temperature. However, at a fixed temperature, graphene grows rapidly in the first ten minutes, slows down gradually, and then the growth nearly stops within one hour after the start of annealing [61]. A full explanation of the phenomenon was provided recently by Zarotti *et al.* [63].

**3.2 Graphene growth on C-face of SiC** In contrast to the Si-terminated (0001) face, graphene grows much faster and thicker on the C-terminated (000 $\bar{1}$ ) face [56,64]. Fig. 4 shows that graphene starts forming at a significantly lower temperature about 1100 °C on SiC(000 $\bar{1}$ ) compared to 1250 °C on SiC(0001) [56]. At a particular temperature, a thicker graphene film is obtained on the SiC(000 $\bar{1}$ ) than on the SiC(0001). For example, at about 1250 °C nine graphene layers grow on the SiC(000 $\bar{1}$ ) while a single graphene layer is formed on the SiC(0001).

As discussed in the previous section, Bommel *et al.* revealed the polycrystalline nature of the graphene film on SiC(000 $\bar{1}$ ). A number of researchers have attempted growing graphene with slightly different growth conditions [52,65-67]. In early reports, the graphene growth regions were described as ‘‘islands’’, since they appeared as pocket



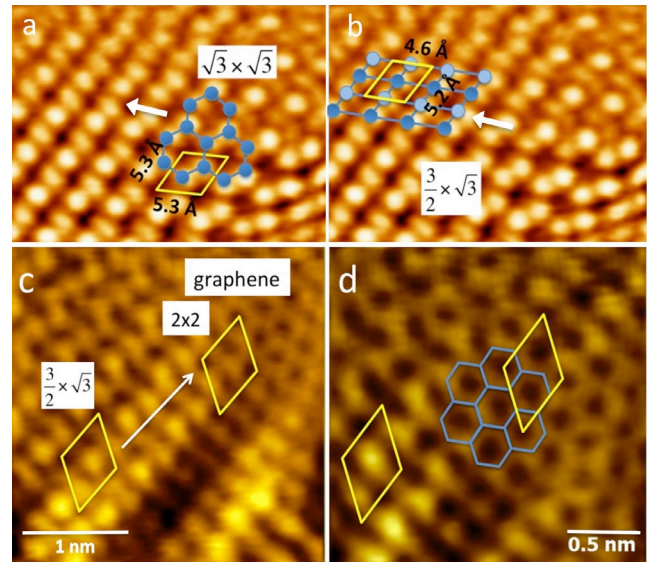
**Figure 4** Graphene thickness as a function of annealing temperature for 6H-SiC (0001) surfaces, showing results for both C-face and Si-face. (Reproduced with permission from Reference 56. ©2010, American physical society)

of graphene on the SiC surface [52,66]. Later, Hite *et al.* discovered that these islands actually exist at a lower level than the surrounding surface and referred to them as graphene-covered basins (GCBs) [65]. They suggested that the crystallographic defects (commonly screw dislocations) in the underlying SiC substrate act as nucleation sites for these GCBs. During expansion, GCBs coalesce with other GCBs having different orientation, sizes and thickness. As a result, the fully developed graphene film on the SiC(000 $\bar{1}$ ) contains misoriented grains with nonuniform thickness. In order to avoid this problem Ouerghi and his group explored the growth on off axis 6H-SiC(0001) wafers in UHV, showing that a perfect uniform graphene monolayer can be obtained on the terraces at 1300 °C, by limiting the Si sublimation rate with N<sub>2</sub> and Si fluxes [68].

By using STM [40], we recently clarified the detailed transformation mechanism of the SiC into graphene on the C-face of 3C-SiC(111): at T>1200 °C SiC start to lose Si atoms, and the top layer rearranges in a SiC( $\sqrt{3}\times\sqrt{3}$ )R30° reconstruction (Fig. 5a). The loss of further Si atoms leads to a new intermediate distorted stage SiC( $\frac{3}{2}\times\sqrt{3}$ )R30° nearly matching the graphene (2×2) structure (Fig. 5b), which evolves into graphene by losing the residual Si atoms (Fig. 5c and d). Note that as the first 4 layers of cubic SiC(111) are arranged in the same order of SiC(0001), their findings are applicable to both structures [40].

Multilayer graphene grown on SiC(000 $\bar{1}$ ) is found to be rotationally disordered and defective [59,69-71]. The graphene layers are ordered in a particular way with alternating 0° and 30° rotations relative to the substrate [43]. Due to this type of non-Bernal stacking, the symmetry between the atoms in the unit cell is not broken in multilayers. As a consequence, each graphene layer possesses the electronic structure of an isolated graphene sheet. Tedesco *et al.* reported a very high carrier mobility of ~150000 cm<sup>2</sup>/Vs for near-intrinsic carrier density at room temperature [72]. This value can reach up to ~250000 cm<sup>2</sup>/Vs for the low temperature measurement in magnetic field below 50 mT for a multilayer graphene [73,74].

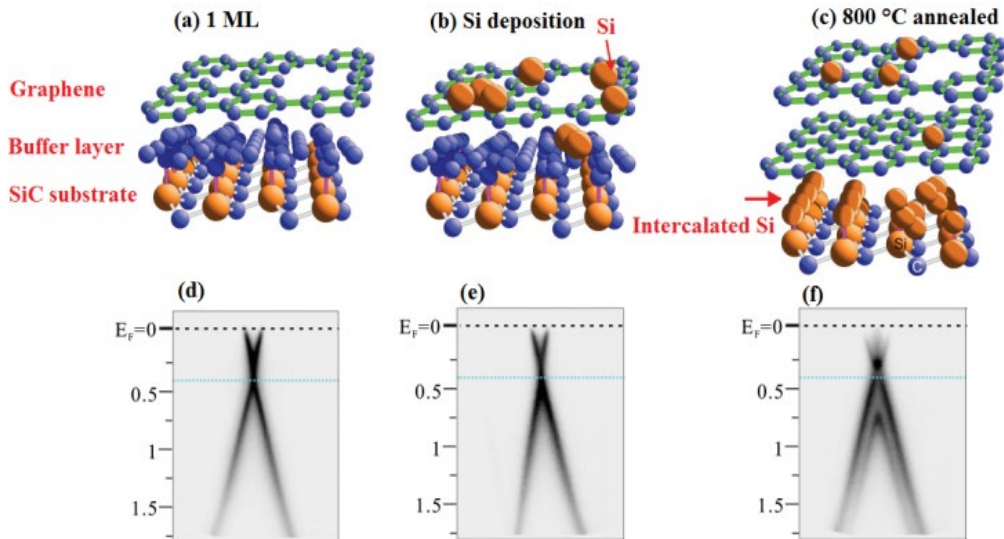
**3.3 Intercalation on graphene in SiC** As discussed in section 3.1, the thermal decomposition of SiC(0001) produces a monocrystalline graphene film along with a ( $6\sqrt{3}\times 6\sqrt{3}$ )R30° reconstructed interfacial carbon layer. This interfacial carbon layer is partially covalently bonded with the underlying substrate surface and does not exhibit the intrinsic electronic structure of graphene and is often called a zero layer or buffer layer [59]. The buffer layer plays a vital role in passivating the dangling bonds of the SiC substrate and induces considerable *n*-doping ( $1\times 10^{13}$  cm<sup>-2</sup>) in the overlying monolayer graphene film [60,75]. This induced doping provides a source of electronic scattering, which is a major problem for SiC-supported graphene structures for future electronic device applications



**Figure 5** STM images of 3C SiC(111)/Si(111) after annealing at 1250 °C. (a-b) ( $3.6\times 2.8$ )nm<sup>2</sup> STM image (V=60 mV I=80 pA) showing the coexistence of two different reconstructed phases. (c) Image acquired in a nearby region, showing the transformation of the  $\frac{3}{2}\times\sqrt{3}$  into graphene. (d) zoom of the area where the reformation is occurring (Adapted from Reference 40)

[57]. Intercalation of a chemical species between the buffer layer and SiC substrate has been demonstrated to be an effective route to overcome this problem. The intercalation process is able to transform the buffer layer into monolayer graphene by decoupling it from the silicon carbide substrate.

Several elements such as Si, H, Li, Au, O, F, Na, Rb and As have been observed to intercalate graphene on SiC substrates [76-84]. Fig. 6 displays the model for Si intercalation as investigated by Xia *et al.* in 2012 [83]. In this case, first, a Si layer was deposited on graphene/buffer/SiC surface (Fig. 6b) and subsequently annealed at 800 °C. During annealing, Si atoms migrate through the existing defects in the graphene sheet and the buffer layer, consequently passivating the Si dangling bonds at the SiC-buffer layer interface (Fig. 6c). Finally, the buffer layer decouples from the substrate forming bilayer graphene on top. This phenomenon was experimentally confirmed by observing angle-resolved photoemission (ARPES) spectra of the corresponding samples. The initial monolayer graphene shows a single  $\pi$ -band crossing the Dirac point at an energy of ~0.4 eV below the Fermi level (Fig. 6d), corresponding to an *n*-type doping concentration of  $\sim 1\times 10^{13}$  cm<sup>-2</sup>. No change in the position of  $\pi$  band was observed after Si deposition (Fig. 6e) and after annealing the sample at 800 °C (Fig. 6f). However, the  $\pi$  band split into two, when the sample was annealed at 800 °C (Fig. 6f), indicating the transformation of the carbon buffer layer and 1 monolayer of graphene into 2 layer graphene upon Si intercalation.



**Figure 6** (a) A schematic structural model for monolayer graphene on the SiC(0001) substrate including a strongly bound ordered  $(6\sqrt{3}\times 6\sqrt{3})R30^\circ$  carbon buffer layer at the interface and defects in the graphene sheet, (b) after Si deposition, (c) after annealing at  $\sim 800^\circ\text{C}$  resulting in a Si intercalated layer and bilayer graphene. The  $\pi$  band around the K point recorded from ARPES spectra for (d) monolayer graphene, (e) after Si deposition, and (f) after successive annealing to  $800^\circ\text{C}$ , respectively. (Adapted from Reference 83)

**4 Graphene on silicon through heteroepitaxial 3C-SiC** Although very high quality graphene has been achieved on bulk SiC through the thermal decomposition technique, the use of SiC wafers leads to limitations in terms of wafer sizes, wafers cost and availability of micro-machining processes.

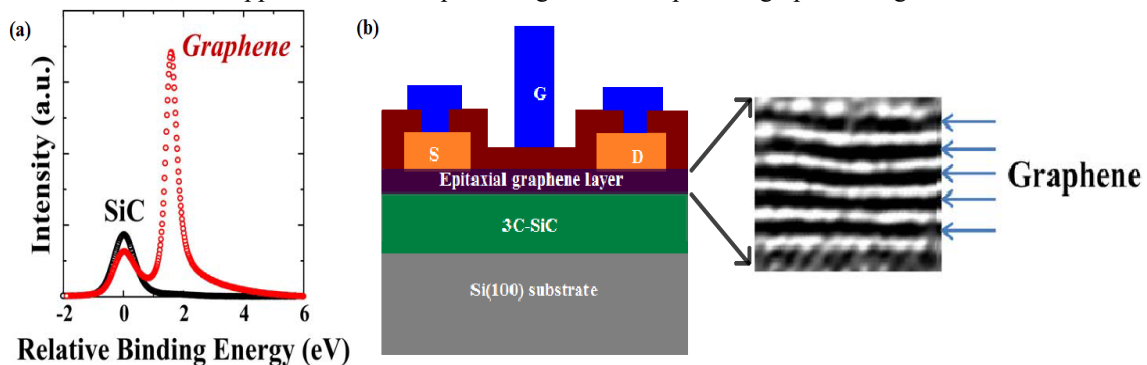
Direct growth of graphene on hetero-epitaxial cubic silicon carbide (3C-SiC) on silicon (Si) substrates would overcome such limitations [85,86]. There are two major advantages associated using Si as a substrate. First, silicon wafers are at the moment still orders of magnitude less expensive than silicon carbide and available in large size up to 12 inches. Second, using a Si as substrate provides easy access to the well-established Si-based integrated circuit technology and infrastructure.

Among the various methods investigated to grow graphene on 3C-SiC on Si, two appear as the most promising:

- 1) Thermal decomposition of 3C-SiC on Si substrate and
- 2) metal-mediated graphene growth. We will discuss these methods in the next subsections.

#### 4.1 Thermal decomposition of 3C-SiC on Si

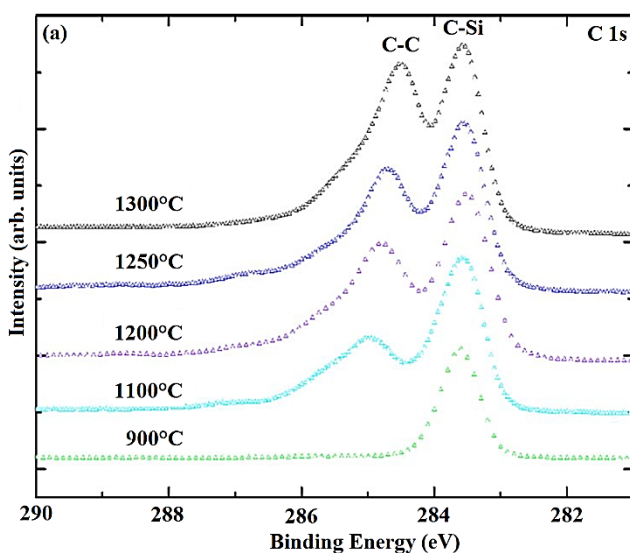
Thermal decomposition is the most widely investigated technique for obtaining epitaxial graphene on 3C-SiC on Si. Several research groups have elegantly presented this technique in their respective reports with slightly different process conditions [39,40,87-91]. The first formal report on the epitaxial growth of graphene on 3C-SiC(111)/Si(110) was published by Miyamoto *et al.* in 2009 [90]. Their graphene growth process consists of two steps; 1) the growth of a 3C-SiC film on a Si substrate via a gas-source molecular beam epitaxy (GSMBE) using monomethylsilane (MMS, 99.999%) as a single source and 2) annealing the samples in ultrahigh vacuum at  $\sim 1300^\circ\text{C}$  for 30 minutes to obtain epitaxial graphene. Fig. 7a shows the C1s core level



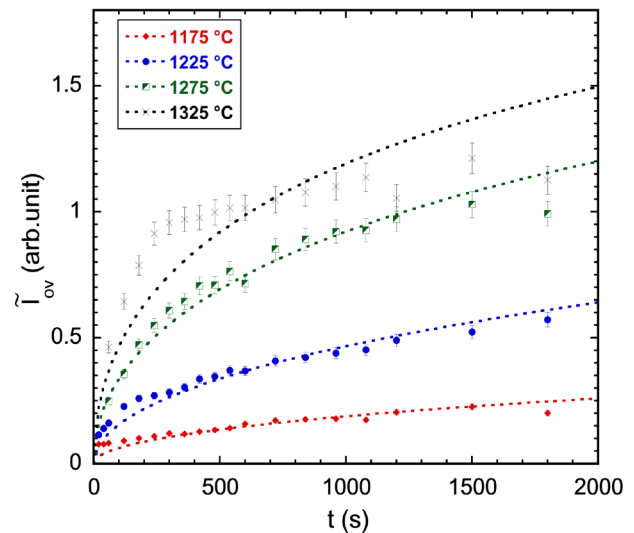
**Figure 7** (a) Comparison of C1s core level spectra of epitaxial 3C-SiC (110) before (black) and after (red) thermal annealing at  $1300^\circ\text{C}$  for 30 min. After graphitization, the  $sp^2$  peak is strongly enhanced. (b) Schematic cross section of GOSFET (left) and TEM image of epitaxial graphene layer (right). (Adapted from Reference 91)

spectrum of the graphene grown on 3C-SiC on Si via this technique, indicating the formation of a well-ordered 2D network of  $sp^2$  bonded carbon atoms [91], also confirmed by Aristov *et al.* [92]. They named this epitaxial growth method as graphene on silicon (GOS). Although their results were very promising, a detailed investigation later clarified that the graphene was actually grew on 3C-SiC(110)/Si(110) instead of 3C-SiC(111)/Si(110) [91]. In successive years, their group produced graphene on 3C-SiC(100)/Si(100) and 3C-SiC(111)/Si(111) substrates as well [88]. Recently, they succeeded in fabricating top-gate and back-gate field effect transistors using GOS as a channel (GOS-FET) [91]. The top-gate GOS-FETs was found to be superior for practical devices mainly in high-frequency applications, because the influence of the substrate to the device performance can be eliminated. A schematic of the top-gate GOS-FET is shown in Fig. 7b [91]. The high-resolution transmission electron micrograph indicates a multilayer graphene grown on the 3C-SiC surface. The transfer characteristics of this top-gate GOS-FET revealed an ambipolar behavior with a minimum conductance at the gate bias voltage of 3.8 V.

Among other research groups, Ouerghi's group from CNRS, France is a major contributor in developing this high vacuum sublimation process and published three consecutive papers in 2010, explaining the graphene growth mechanism [85,87,93]. Their graphene growth method consists of several steps. First, SiC/Si substrates were degassed for several hours at 600°C under UHV conditions followed by annealing under a low (0.1 nm/min) Si flux at 900°C to remove the native oxide. Finally, the samples were annealed at high temperature (900 °C-1300 °C) to obtain epitaxial graphene. The XPS spectra recorded for a number of temperatures to investigate the evaluation of graphene with increasing the temperature. Fig. 8 shows



**Figure 8** C 1s XPS spectra of the fully grown graphene on 3C-SiC(111) for different temperatures. (Adapted from Reference 87)



**Figure 9** Time dependence of normalized XPS C1s intensities from graphene overlayer on SiC/Si(111). (Adapted from Reference 63)

that the core level C1s peak at 284.8 eV associated with the  $sp^2$  bonded carbon atoms clearly appears at 1200 °C [87]. The peak clearly increases with temperature and shift towards lower binding energy.

We recently reported a more comprehensive study on the evolution of graphene layers on SiC/Si substrates as a function of temperature and of annealing time [39,63]. By analyzing the time evolution of the graphene C 1s peak at several temperatures (Fig. 9), we obtain the general growth law as  $h(t)/\lambda = \beta t^\gamma$ , where  $h(t)$  represents the mean overlayer thickness formed on the substrate at the time  $t$ ,  $\lambda$  symbolizes the effective escape depth of electrons in the material and  $\beta$  is a constant. We also found that the time exponent ( $\gamma = 1/2$ ) provides the best fit at all temperatures.

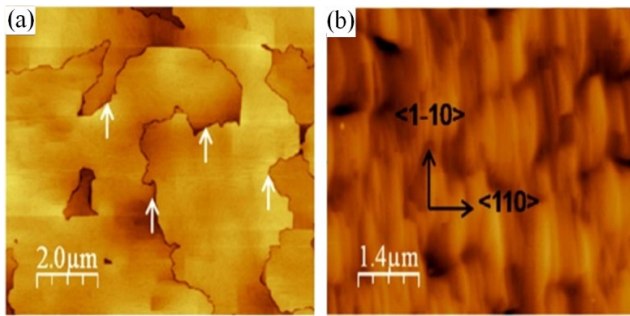
Furthermore, the activation energy of the SiC in the evolution of graphene has been estimated as  $E_a = 2.5 \pm 0.5$  eV, using following formula

$$E_a = \left( U_d^* + \frac{E_{Si}}{2} \right) / 2$$

Where,  $U_d^*$  is the activation energy for Si diffusion in the overlayer and  $E_{Si}$  is the energy (standard enthalpy) for releasing the atomic silicon. This quantitative description allows for a fine-tuning of the desired number of graphene layers.

**Factors affecting graphene growth on heteroepitaxial SiC** Epitaxial graphene obtained via thermal decomposition of 3C-SiC on Si is affected by factors such as crystallographic defects, initial surface roughness and orientation of the 3C-SiC films [89,91,94]. Among all aforementioned factors, orientation of the 3C-SiC film and associated crystallographic defects has the most profound effect on epitaxial graphene. Several researchers have studied the epitaxy of graphene on (100), (111) and (110) oriented 3C-SiC film [87,91,92,94,95]. 3C-SiC heteroepitaxial films





**Figure 10** AFM image of epitaxial graphene grown on (a) 3C-SiC(100)/on-axis Si (the white arrows indicate antiphase domain boundaries), and (b) 3C-SiC(100)/off-axis Si. (Adapted from Reference 95)

grown on (100) Si substrates were characterized by a high density of defects such as antiphase boundaries [96]. These antiphase boundaries can transfer on to the graphene layers (Fig. 10a) with dissimilar thickness, which can deteriorate the intrinsic properties of ideal graphene. 3C-SiC films grown on off-axis (100) Si substrates were used to eliminate these APBs, and single domain epitaxial graphene films obtained on the surface (Fig. 10b) [95]. In contrast, 3C-SiC films grown on (111) Si substrate is believed to be the most desirable surface to grow epitaxial graphene since it is free from APBs and has hexagonal symmetry like 6H-SiC and therefore acts as a good template for graphene growth. Several research groups confirmed this finding by growing graphene on 3C-SiC on (111) Si substrate [94,97]. Remarkable graphene continuity was observed in this case even on the step edges.

Surface roughness of the 3C-SiC film is another important parameter in determining the quality of the epitaxial graphene as discussed above. It strongly influences the electron mobility in the graphene epitaxial layer through strain and misorientation of the graphene crystal structure [89,91]. A surface roughness value less than  $\sim 1$  nm is essential to obtain high quality epitaxial graphene. Various methods such as chemical mechanical polishing, plasma assisted polishing and plasma smoothing have been used to achieve smooth 3C-SiC surface [98-100].

**4.2 Metal mediated graphene growth** The thermal decomposition approach appears to have two major limitations in the case of silicon carbide on silicon. First, the quality of the graphene film produced in high/ultra-high vacuum is limited due to the difficulty in controlling sublimation rates at relatively low (900-1300 °C) temperatures [39,90,94]. A large D to G band Raman intensity ratio ( $I_D/I_G$ ) about  $\sim 1$  was reported, which is considerably high in comparison to the exfoliated graphene [39,90]. Second, the thermal decomposition technique is commonly limited to the use of 3C-SiC(111) surface [39,85,91].

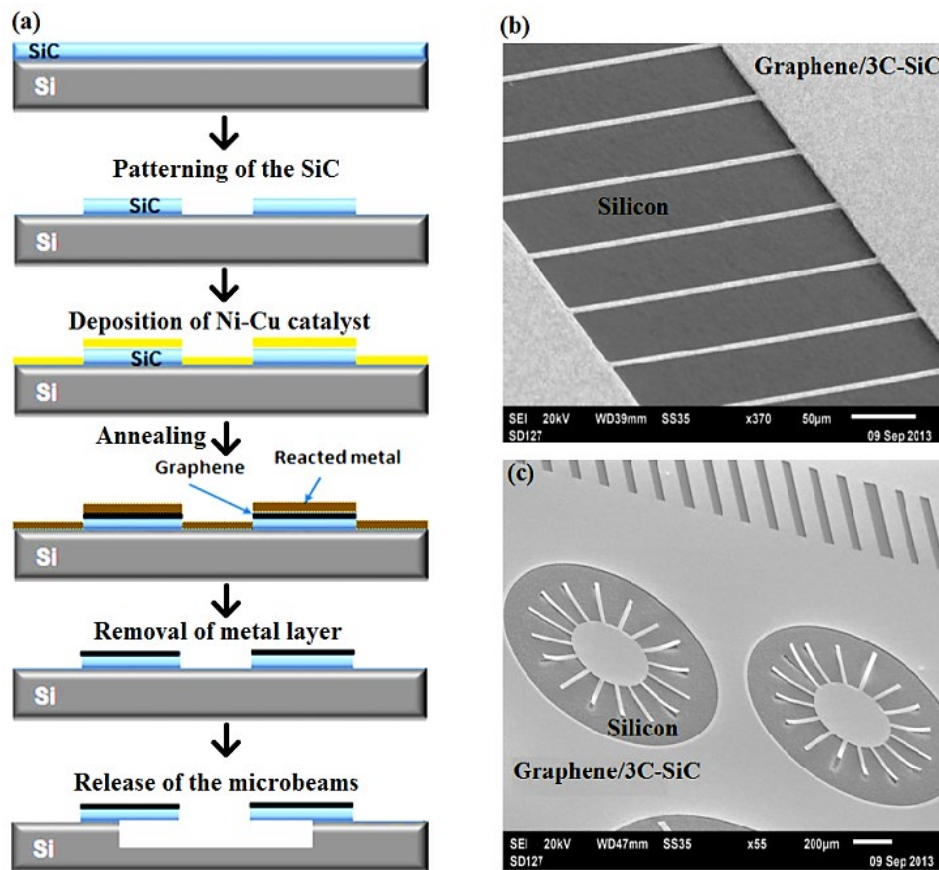
To address these issues, some groups have investigated an alternative catalyst-based approach for obtaining graphene on the 3C-SiC on Si [101-104]. This method involves depositing a metal layer such as nickel or cobalt on

the 3C-SiC surface and subsequently annealing the sample at temperatures ranging from 750 °C to 1200 °C, which is much lower than the thermal decomposition process. During the annealing process SiC reacts with metal, forming a metal silicide and releasing atomic carbon into the system [105]. This released atomic carbon precipitates upon cooling and rearranges into single- to few-layer graphene. In most cases the graphene was found to grow on the metal surface, still needing to be transferred onto a semiconductor or an insulating surface to obtain a functional device, which hinders its utility for large-scale device fabrication [101,103]. Although the earlier attempts at nickel-mediated graphitization from amorphous or crystalline SiC films on silicon had shown some promise, improving the defect density and uniformity of the graphene remained challenging.

In response to these limitations, we have recently demonstrated a novel alloy-mediated catalytic approach to grow high-quality, highly-uniform bilayer graphene on 3C-SiC on both (100) and (111) Si substrates [106,107]. The graphitization process consists of the following steps: 1) deposition of double layer of nickel (Ni) and copper (Cu) onto the 3C-SiC surface; 2) annealing samples at mild temperature (900-1100 °C) for one hour; 3) removal of metal/metal-silicide layer by immersing samples in wet chemical etch solution. The obtained bilayer graphene covers uniformly a 2" silicon wafer with average Raman  $I_D/I_G$  band ratio as low as  $\sim 0.2$  to 0.3, indicative of a lowly defective material [106]. Note that this  $I_D/I_G$  ratio is consistent over large surfaces and considerably small compared to the previously reported graphene on 3C-SiC on Si [39,91,93].

Due to its extraordinary mechanical and electrical properties [2,6], a graphene coating is expected to greatly improve current micro-electro-mechanical systems (MEMS) [108]. However, the low adhesion of transferred graphene is a major drawback for device fabrication and reliability. The alloy-mediated graphene has indicated an adhesion energy to the underlying 3C-SiC film [106] nearly an order of magnitude higher than that of graphene layers transferred onto a SiO<sub>2</sub> layer on Si [109]. Additionally, wafer-scale fabrication of graphitized SiC microstructures (bridges and cantilever) on a silicon substrate through a selective, self-aligned, transfer-free catalytic process was recently demonstrated [107]. Fig. 11a illustrates the complete fabrication process. First, the microstructures are patterned on the 3C-SiC surface via standard photolithography technique. In this, the SiC/Si wafer is coated with photoresist, and the structures are defined. Unprotected SiC areas are selectively removed via plasma etching, and the remaining photoresist is removed using O<sub>2</sub> plasma.

The bimetal (Ni and Cu) catalyst layer is deposited on the entire wafer. After that, the samples are annealed at moderate temperature (1000-1100°C) in a Carbolite HT furnace for one hour to produce graphene and metal/metal-silicide layer on the patterned 3C-SiC surface. The metal/metal-silicide layer is then removed by immersing the



**Figure 11** (a) Sequential steps for the wafer-level fabrication of graphitized silicon carbide microbeams on a silicon substrate. Once the SiC is patterned, the few-layer graphene is grown selectively on the SiC structures via metal-mediated graphitization. The reacted metal layer is subsequently removed, and the structures are released from the substrate to form suspended beams. SEM micrographs of released Graphene/3C-SiC microstructures including (b) bridges and (c) cantilevers. (Adapted from Reference 104)

samples in a wet chemical etch solution. Finally, a  $\text{XeF}_2$  isotropic silicon etching is performed to release the graphitized 3C-SiC structures. Fig. 11b and 11c shows the SEM images of graphitized 3C-SiC microstructures including bridges and cantilevers fabricated via this technique [107].

Finally, we have recently demonstrated that the metal-mediated graphene approach using only nickel can also be optimized to obtain a highly rugged electrode material for on-chip supercapacitors [12]. Therefore, we suggest that although the graphene quality may not match that of graphene grown on silicon carbide wafers, the metal-mediated graphene growth from heteroepitaxial silicon carbide offers large flexibility and opens the door for large-scale fabrication of graphene nanostructures for a large range of electronic, photonic, optomechanical, energy storage and sensing applications on a silicon platform.

**5 Conclusions** The aim of this review article is to provide detailed insight into the graphene growth on SiC surfaces, its properties and technological relevance. The first sections summarize the outstanding properties of graphene and the leading graphene growth techniques such as

micromechanical exfoliation, CVD growth on metals and thermal decomposition of SiC. The thermal decomposition of SiC appears the most promising from the perspective of electronic device fabrication thanks to its direct-growth process on a semiconductor surface, and the extent of control on number of layers, quality, and uniformity obtained. An extraordinary body of knowledge has been gathered over the last decade in the tuning the doping and properties of graphene from silicon carbide through intercalation.

However, bulk SiC substrates present limitations in terms of costs, sizes and difficulty in micromachining. While the quality can be somewhat compromised, direct growth of graphene on hetero-epitaxial 3C-SiC on Si substrates is a promising alternative. Graphene on 3C-SiC/Si offers an alternative that is fully compatible with established silicon fabrication technologies, reducing fabrication costs and allowing seamless integration. A recently developed catalyst alloy-mediated graphene approach on hetero-epitaxial SiC opens the possibility for direct and selective growth of lowly defective graphene on silicon, leading to straightforward patterning and micromachining capabilities.

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