# Carrier Transport and Electrical Conduction in Alloy-Mediated Graphene on Silicon

Aiswarya Pradeepkumar

B. Tech., M. Eng.

A thesis submitted in fulfilment of the requirements for the degree of

# **Doctor of Philosophy**

School of Electrical and Data Engineering

Faculty of Engineering and Information Technology

**University of Technology Sydney** 

January, 2020

### **Abstract**

The possibility of graphene-based micro- and nanoelectronic devices that exploit the extraordinary electronic properties of graphene is the biggest inspiration behind the accelerated development of graphene science and technology. Although the remarkable efforts for establishing graphene as a new electronic material began over 15 years ago, the actual realisation of graphene devices on a large-scale remains elusive, mainly due to feasibility, cost-effectiveness and compatibility issues with the existing semiconductor technology and processes. Significant advancements have been achieved in the synthesis and establishment of transport properties of epitaxial graphene (EG) on 4H- and 6H-SiC, while equivalent progress using silicon (Si) as a platform (via a thin film of 3C-SiC) with reliable electrical transport measurements has not been elucidated to date, due to limitations such as non-uniform coverage of graphene on 3C-SiC/Si and high density of defects within the 3C-SiC.

In this work, we first show that the heteroepitaxial 3C-SiC on Si as the substrate should be carefully approached, as the 3C-SiC/Si heterojunction is electrically unstable and prone to severe leakage or parallel conduction. Subsequently, we find that the interface instability is due to the diffusion of carbon into the silicon matrix during the 3C-SiC growth, creating electrically active interstitial carbon. We overcome these challenges using 3C-SiC on a highly-resistive silicon substrate.

By addressing the parallel conduction issue of the 3C-SiC/Si heteroepitaxial system, in this work, we isolate the charge transport properties of epitaxial graphene (EG) grown directly on 3C-SiC over large areas via an alloy-mediated method and present corresponding physical ab-initio models. Here, we study the properties of EG synthesised on 3C-SiC(100) and 3C-SiC(111). The transport properties of EG on 3C-SiC follow a similar power-law dependence of sheet carrier concentration and mobility and comparable sheet resistance values with the EG on bulk-SiC – although the grain sizes for both are vastly different. Furthermore, we find that the transport properties of graphene within the observed regime are dominated by the substrate interaction, resulting in a large p-type doping, especially for the graphene on 3C-SiC(100). In the case of EG on 3C-SiC(111), the presence of buffer layer reduces the substrate interaction and the charge transfer up to an extent. This work demonstrates a more compelling need to focus

on the engineering of the graphene-substrate interface as opposed to graphene grain sizes in order to tune the charge transport properties of the epitaxial graphene for the integration of 2D materials in functional nanosystems.

# Certificate of original authorship

I, Aiswarya Pradeepkumar declare that this thesis, is submitted in fulfilment of the requirements for the award of Doctor of Philosophy, in the Faculty of Engineering at the University of Technology Sydney.

This thesis is wholly my own work unless otherwise reference or acknowledged. In addition, I certify that all information sources and literature used are indicated in the thesis.

This document has not been submitted for qualifications at any other academic institution.

This research is supported by the Australian Government Research Training Program.

**Production Note:** 

Signature removed prior to publication.

Aiswarya Pradeepkumar

30/01/2020

## **Dedication**

This thesis is dedicated to my parents Pradeepkumar P and Vasanthakumari V

for giving me invaluable educational opportunities

and my husband Nikhil Das

for his support, constant encouragement and care

# Acknowledgements

First of all, I would like to express my sincere gratitude to my supervisor Professor Francesca Iacopi for allowing me to join her team, and her kind support throughout both my Master's dissertation and PhD at first from Griffith University and then from UTS. Her valuable advises, continuous encouragement and constant support were critical throughout the development of my research work. I would also like to thank Dr David Kurt Gaskill, my external supervisor for his feedback at every milestone of my project as well as for hosting me at his lab in the United States in 2017 and helping me to finalise the publications.

I must acknowledge UTS for awarding me the PhD scholarship for three and a half years after my transfer from Griffith University right after my first year. I would like to appreciate the support provided by Dr Ronald Shimmon, and Dr Linda Xiao from chemical technology unit in the Faculty of Science for allowing to access liquid nitrogen for my experiments. My appreciation is extended to all the instrument training and technical support offered by Geoffrey McCredie, Katie McBean, Herbert Yuan from microstructural analysis unit in the Faculty of Science.

Part of the sample fabrication reported in this thesis was performed at Griffith University and Australian National Fabrication Facility (ANFF, Queensland node) at the University of Queensland (UQ). I want to thank the staff members of UQ; Kai-Yu Liu, Elliot Cheng, Doug Mair, Wael Al Abdulla, Elena Taran, and Lien Chau for various instrumental support. I want to thank Shan Don for the software access support from the Australian National Fabrication Facility Design House Virtual Lab.

My sincere appreciation also goes to ANFF staffs at UNSW, for helping me with dicing the wafers used in this study.

My sincere appreciation also goes to Marcin Zielinski from NOVASIC for proving me the 3C-SiC samples throughout my research.

My sincere thanks also go to Dr Neeraj Mishra, Dr Atieh Ranjbar Kermany, Mr Dayle Goding, Dr Mohsin Ahmed, Dr Bei Wang, Dr Zulfiqar Khan, Dr Mojtaba Amjadipour, Mr Patrick Rufangura whose collaboration greatly helped in my work.

Last, but not least, I express my deepest gratitude to my father, mother, husband and all family members for their endearing encouragement, and love.

#### List of Publications

#### Journal Articles:

Aiswarya Pradeepkumar, Mojtaba Amjadipour, Neeraj Mishra, Chang Liu, Michael S Fuhrer, Avi Bendavid, Fabio Isa, Marcin Zielinski, Hansika I. Sirikumara, Thushari Jayasekara, D. K Gaskill, Francesca Iacopi, p-type epitaxial graphene on cubic silicon carbide on silicon ACS Applied Nano Materials (2019)

https://doi.org/10.1021/acsanm.9b02349

Aiswarya Pradeepkumar, Marcin Zielinski, Matteo Bosi, Giovanni Verzellesi, D.
Kurt Gaskill, and Francesca Iacopi Electrical leakage phenomenon in
heteroepitaxial cubic silicon carbide on silicon. Journal of Applied
Physics, 123(21), 215103 (2018)

https://doi.org/10.1063/1.5026124

- Aiswarya Pradeepkumar, Neeraj Mishra, Atieh Ranjbar Kermany, John J. Boeckl, Jack Hellerstedt, Michael S. Fuhrer, and Francesca Iacopi (2016). Catastrophic degradation of the interface of epitaxial silicon carbide on silicon at high temperatures. Applied Physics Letters, 109(1), 011604 (2016)
   http://scitation.aip.org/content/aip/journal/apl/109/1/10.1063/1.4955453
- Aiswarya Pradeepkumar, Neeraj Mishra, Atieh Ranjbar Kermany, John J. Boeckl, Jack Hellerstedt, Michael S. Fuhrer, and Francesca Iacopi (2016). Response to "Comment on 'Catastrophic degradation of the interface of epitaxial silicon carbide on silicon at high temperatures'" [Appl. Phys. Lett. 109, 196101 (2016)]. Applied Physics Letters, 109(19), 196102 (2016)
  http://aip.scitation.org/doi/10.1063/1.4967228

#### **Conference publication:**

 Aiswarya Pradeepkumar, D K. Gaskill, F. Iacopi, "Electrical Challenges of Heteroepitaxial 3C-SiC on Silicon", Materials Science Forum, Vol. 924, pp. 297-301, 2018.

https://www.scientific.net/MSF.924.297

#### **Conference presentations:**

- A. Pradeepkumar, N. Mishra, M. Fuhrer, C. Liu, M. Zielinski, D. K Gaskill, F. Iacopi, "Charge transport properties of epitaxial graphene on cubic silicon carbide on silicon", International Symposium of Epi-graphene, TU Chemnitz, August 2019 (Oral presentation)
- A. Pradeepkumar, N. Mishra, M. Zielinski, D. K Gaskill, F. Iacopi, "Electrical characteristics of epitaxial graphene on silicon", International Conference of 2D Materials, Melbourne, 2018
- A. Pradeepkumar, D K. Gaskill, F. Iacopi, "Electrical Challenges of Heteroepitaxial 3C-SiC on Silicon", International Conference for Silicon Carbide and Related Materials', Washington DC, Sept 2017

#### **Patents:**

Australian Provisional Patent Applications; Nos. 2017903720 and 2017904860 [UTS Ref DISC-2017-019] - submitted for PCT, 2018

## **Table of Contents**

Abstract	i
Certificate of original authorship	iii
Acknowledgements	v
List of Publications	vii
List of Figures	xii
List of Tables	xvii
List of Acronyms	xix
Chapter 1: Introduction	1
1.1 Background and Motivation	1
1.2 Significance and Context	4
1.3 Thesis framework	5
1.4 References	6
Chapter 2: Literature review	9
2.1 Graphene - fundamental characteristics	9
2.2 The electronic band structure of graphene - electronic properties	10
2.3 Graphene growth methods	14
2.3.1 Mechanical exfoliation of single-crystal graphite	14
2.3.2 Chemical vapour deposition on transition metals and dielectric insulator	
2.3.3 Graphene on semiconductors	15
2.3.4 Thermal decomposition of silicon carbide	16
2.3.5 Direct growth of graphene on silicon substrates	17
2.3.6 Graphene on silicon using heteroepitaxial cubic silicon carbide	19
2.4 Transport properties of graphene	21
2.3.1 Mechanically exfoliated graphene	21
2.4.1 CVD graphene grown on copper substrates transferred to SiO <sub>2</sub> /Si	22
2.4.2 CVD graphene grown on copper substrates transferred to Ge(001)	22
2.4.3 Epitaxial graphene on SiC via thermal decomposition	23
2.4.4 H-intercalation of graphene on SiC	25
2.5 Direct growth of graphene on silicon	27
2.5.1 Thermal decomposition of cubic silicon carbide on silicon	27
2.5.2 Carrier scattering mechanism in epitaxial graphene	30
2.6 Summary	31
2.7 References	33

Chapter 3: Methodology	42
3.1 Substrate material – heteroepitaxial 3C-SiC/Si	42
3.2 Graphene synthesis	43
3.3 Electrical characterisation.	44
3.3.1 Hall Effect Measurement	44
3.3.2 van der Pauw sheet resistance measurement	45
3.3.3 Temperature-dependent sheet resistance measurements	46
3.3.4 Transfer Length Method (TLM) structures on 3C-SiC/Si	46
3.4 Instrument specifications	48
3.4.1 Hall effect measurement	48
3.4.2 TLM leakage resistance measurements on 3C-SiC/Si structures	48
Structural characterisation of 3C-SiC/Si	49
3.4.3 Transmission Electron Microscopy	49
3.4.4 Scanning Electron Microscopy (SEM)	49
3.4.5 Stress measurements	49
3.4.6 Sentaurus simulations	49
Surface characterisation of graphene	50
3.4.7 Raman spectroscopy	50
3.4.8 X-ray Photoelectron Spectroscopy	50
3.4.9 Density Functional Theory (DFT)	50
3.5 Summary	51
3.6 References	51
Chapter 4: Electrical degradation of the heterointerface of epitaxial silicon carb	ide on
silicon	
4.1 Abstract	
4.2 Introduction	
4.3 Methodologies	59
4.4 Results and discussion	61
4.5 Conclusions	67
4.6 References	68
4.7 Supporting information	75
4.7.1 References	77
Chapter 5: Electrical characteristics of heteroepitaxial cubic silicon carbide on s	
5.1 Abstract	83
5.2 Introduction	83

5.3 Methodologies	84
5.4 Results and discussion	86
5.4.1 3C-SiC on low-doped silicon.	86
5.4.2 3C-SiC on high-resistivity silicon.	92
5.4.3 Practical solution for the 3C-SiC/Si in-plane leakage	94
5.5 Conclusions	95
5.6 References	96
Chapter 6: Charge transport properties and electrical conduction in epitaxial on cubic silicon	
6.1 Abstract	103
6.2 Introduction	104
6.3 Results and discussion	106
6.3.1 Raman characterization	107
6.3.2 X-ray Photoelectron Spectroscopy	109
6.3.3 Electrical characterization	110
6.4 Conclusions	120
6.5 Materials and Methods	121
6.6 References	124
6.7 Supporting Information (SI)	129
6.7.1 Raman characterisation	130
6.7.2 Graphene layer thickness estimation using XPS data	134
6.7.3 Effect on the number of layers of graphene on the transport proper	ties135
6.7.4 Testing the presence of Ni/Cu metal or metal oxides in the grapher	ne136
6.7.5 Electrical characterization	137
6.7.6 Verifying the coverage of EG on 3C-SiC(100)	138
6.7.7 Density Functional Theory Model	139
6.7.8 References	140
Chapter 7: Conclusions and future works	141
7.1 References	144

# **List of Figures**

Figure 1-1: 42 years of microprocessor trend data. Original data up to 2010 collected and plotted by M. Horowitz et al. <sup>2</sup> New data for 2010 - 2017 collected and plotted by K. Rupp (Source: https://www.karlrupp.net/2018/02/42-years-of-microprocessor-trend-data/)1
Figure 2-1: a) The lattice structure of ideal single-layer graphene made up of two sublattices, A and B. The unit cell comprised of two hexagonal vectors $a_1$ and $a_2$ (length 2.46 Å); (b) Reciprocal lattice of monolayer graphene, defined by the vectors $b_1$ and $b_2$ Blue hexagon denotes the first Brillouin zone of graphene, where are $\Gamma$ , $K_+$ , and $K$ are the points of high symmetry. <sup>2</sup>
Figure 2-2: a) The electronic band structure of monolayer graphene. <sup>2, 5, 10</sup> The plot shows graphene's electronic bands where the electron and hole states meet at the Dirac point. The $K_+$ and $K$ are the two inequivalent points at the corners of the Brillouin zone (black hexagon). The other four corners are equivalent to either $K_+$ and $K$ $K$ $K$ $K$ $K$ $K_+$ and $K$ $K$ $K_+$ $K$ $K_+$ $K$ $K_+$ $K_+$ and $K$ $K_+$ $K$ $K_+$
Figure 2- 3: Dirac dispersions with $2mc^2$ . At $m = 0$ , the bandgap is zero and the dispersion is linear at the Dirac point. 13
Figure 2-4: Schematics of direct graphene synthesis on epitaxial 3C-SiC <sup>100</sup> 20
Figure 2-5: Structure of monolayer graphene on Si-face SiC(0001) with a buffer layer. 24
Figure 2-6: Mobility and sheet carrier density data of the EG synthesized on Si-face of bulk 4H- and 6H-SiC semi-insulating wafers at 300 and 77 K from Tedesco et al. 6 Triangles represent the data of EG on Si-face of SiC; Squares and circles represent the data for n-type and p-type EG on the C-face of SiC, respectively
Figure 2-7: Structure of a) Monolayer graphene on top of buffer layer/3C-SiC b) Quasifree standing bilayer graphene after H-intercalation – buffer layer decoupled from substrate forming additional graphene layer. 138
Figure 3-1: Schematics showing the alloy mediated graphitization of 3C-SiC/Si <sup>1</sup> 43
Figure 3-2: a) Schematics of Hall effect phenomenon <sup>2</sup> b) van der Pauw contacts or Graphene/3C-SiC showing the Hall effect measurement configuration.

Figure 3- 3: Schematics of a) van der Pauw sheet resistance measurement <sup>3</sup> ; b) test structure of graphene on 3C-SiC for the sheet resistance measurement configuration45
Figure 3-4: a) TLM structure, b) I-V measurement on TLM structure46
Figure 3- 5: Total resistance across the different contact spacing <sup>7</sup> 47
Figure 3-6: TLM structures on 3C-SiC/Si. Width of the contacts are 500 $\mu m$ 47
Figure 3- 7: Ecopia HMS-5300 Hall effect Measurement System with AMP55T48
Figure 3- 8: HP 4145B Semiconductor Parameter Analyzer (left) and the probe station (right)
Figure 4- 1: Sheet resistance of the 250nm thick as-grown SiC(100) and the vacuum annealed SiC(100) at 1100°C for 1 hour as a function of temperature in the range between 5K and 300K
Figure 4-2: Resistivity versus temperature for the annealed SiC(100). Activation energy of 44meV is obtained by fitting the data over 30K to 100K (zone II)
Figure 4-3: Absolute stress difference of the epitaxial SiC(100) and SiC(111) films before and after annealing at 1180°C versus film thickness. Each point represents the absolute difference of the average stress for the as-grown and the annealed films. The difference indicates in all cases a transition towards a more compressive stress state with decreasing thickness. Note that the exponential suppression of the stress difference with increasing thickness indicates the interfacial nature of the stress change
Figure 4-4: High-resolution TEM micrographs of the SiC-Si interface of the 250nm-thick SiC(100) and SiC(111) films (a) as-grown SiC(100) film (b) SiC(100) film annealed in vacuum at 1100°C, for 1 hour c) as-grown SiC(111) film d) SiC(111) film annealed in vacuum at 1100°C, for 1 hour. The SiC/Si interface of both the as-grown SiC films appear to be well-defined whereas, the interface of the annealed SiC films appears inhomogeneous.
Figure 4-S1: Photolithographic pattern made on the SiC/Si for the electrical characterisation <sup>3,4</sup> (Courtesy of QMNC, Griffith University)76
Figure 5- 1: a) Layout of the van der Pauw structure on 3C-SiC/Si, b) schematic of electrical conduction path in the SiC grown at 1300-1400 °C on the low-doped p-Si substrate. The whole silicon substrate is involved in the conduction through the injection of holes into the SiC layer
Figure 5-2: Plane view SEM images for IMEM-CNR 3C-SiC a) 500 nm-thin SiC(100) film on on-axis p-Si; where antiphase boundaries (denoted APB) and stacking faults

(denoted SF) are visible; b) 5 µm-thick SiC(100) films on 6° off-axis p-Si substrates; APBs and SFs are not visible
Figure 5-3: Schematic of Si substrate bending into more convex due to the compressive stress exerted by the carbon interstitials within the top portion of silicon
Figure 5-4: TCAD simulation results of the 3C-SiC on low doped p-Si substrate a) electron density and b) hole density, in the SiC/Si system before junction degradation (no defects); c) electron density and d) hole density, in the SiC/Si system after incorporating interstitial carbon degradation within the silicon
Figure 5-5: a) TLM structures on the 3C-SiC/high-resistivity Si, b) Fitted TLM leakage resistances versus contact spacing for SiC on high-resistivity Si93
Figure 5-6: Schematic of conduction path in 3C-SiC/high-resistivity Si grown at 1300 - 1400 °C -the conduction occurs within a region of a few micrometres thick below the interface.
Figure 5-7: SiC/high-resistivity Si after ~20 µm deep etching of Si a) TLM structure, b) electrical conduction
Figure 6-1: Schematic of the process steps for the alloy-mediated synthesis of graphene on the 3C-SiC/Si substrate. <sup>20</sup>
Figure 6-2: Polar plots of Si peak intensity, 3C-SiC TO peak intensity and the ratio of the 2D to G peak intensity as a function of the relative angle ( $\beta$ ) between the polarizations of the analyzer and incident laser, for (a) EG/3C-SiC(100); (b) EG/3C-SiC(111)109
Figure 6-3: XPS C 1s and Si 2p core-level spectrum for; (a) EG/3C-SiC(100) (sample 3 in Table 2) and (b) EG/3C-SiC(111) (sample 1 in Table 6-2)109
Figure 6-4: a) van der Pauw geometry with four-point InSn contacts. b) Schematics of vdP sheet resistance measurements on bare-Si, 3C-SiC/Si and EG/3C-SiC/Si. Temperature-dependent sheet resistance of c) EG/3C-SiC(100), 3C-SiC/Si(100) and bare-Si(100); (d) EG/3C-SiC(111) and 3C-SiC/Si(111) and bare Si(111) in the range between 80 and 300 K; e) mobility as a function of temperature in the range between 80-300K for EG/3C-SiC(100) and EG/3C-SiC(111)
Figure 6-5: Mobility and sheet carrier density data of the EG on 3C-SiC/Si (Table 3) are here superimposed and remarkably in line with those of EG on Si-face of bulk 4H- and 6H-SiC 16 x 16 mm <sup>2</sup> semi-insulating substrates at 300 and 77 K from Tedesco et al. <sup>7</sup> Reprinted from ref 7. Copyright from 2009 AIP publishing
Figure 6-6: Electronic band structure for EG on 3C-SiC with top-substrate demonstrating the effect of substrate interaction on transport properties of epitaxial graphene. (a) Absence of buffer layer (at 100 % oxidation) increase a charge transfer from graphene

into the oxidized substrate with a Fermi level at $0.55~\text{eV}$ below the Dirac point – can be linked to the case of EG/3C-SiC(100); (b) presence of buffer layer (at 60 % oxidation) between EG and substrate reduce the charge transfer from graphene giving Fermi level at $0.43~\text{eV}$ below the Dirac point (E <sub>F</sub> closer to E <sub>D</sub> ) - reflecting the case of EG/3C-SiC(111). Si, C, and O atoms are shown in yellow, black and red spheres. The upper panels show the charge density plot. The blue color mesh represents electron accumulation, and red color mesh indicates electron depletion.
Figure 6-7: (a) and (b) XPS C 1s and Si 2p core-level spectrum for a selected EG/3C-SiC(111) (sample 4) after H-intercalation. (c) and (d) schematic and electronic band structure for H-intercalated EG on top-oxidized substrate 3C-SiC(111) with Fermi level at 0.32 eV, below the Dirac point (E <sub>D</sub> -E <sub>F</sub> ) indicating <i>p</i> -type conduction. The upper panel in (d) shows the charge density plot. Si, C, O and H atoms are shown in yellow, black, red and green spheres. The blue color mesh represents the electron accumulation, and red color mesh indicates electron depletion.
Figure 6-S1: Raman maps of $I_D/I_G$ and $I_{2D}/I_G$ ratios, G and 2D positions, G and 2D FWHM across 30 $\mu m$ x 30 $\mu m$ for a) EG/3C-SiC(100) –sample 1; b) EG/3C-SiC(111) – sample 2. (Selected samples from Table 6-2)
Figure 6-S2: Average Raman spectra (30 $\mu$ m $\times$ 30 $\mu$ m) of EG/3C-SiC(100) and EG/3C-SiC(111) across 30 $\mu$ m x 30 $\mu$ m using 532 nm laser (selected samples from Table 6-2)
Figure 6-S3: $30 \mu\text{m} \times 30 \mu\text{m}$ Raman peak intensity maps of TS1, TS2 and TS3 turbostratic in-plane <sup>1</sup> modes identified between 1700 and 2300 cm <sup>-1</sup> in the Raman spectra of (a) EG/3C-SiC(100) – sample 3; (b) EG/3C-SiC(111) – sample 1 (selected samples from Table 6-2)
Figure 6-S4: Polar plots of Si peak intensity, 3C-SiC TO peak intensity and the ratio of the 2D to G peak intensity as a function of the relative angle for (a) EG/3C-SiC(100); (b) EG/3C-SiC(111) across 2 different spots separated by 1.5 mm
Figure 6-S 5: (a) EDX - no evidence for the presence of nickel or copper metal/metal oxides in the graphene. An Oxford INCAx-sight EDX spectroscopy attached to the FESEM was used to evaluate the elemental composition of the EG at 10 kV; (b) XPS survey spectra of EG/3C-SiC(100) and EG/3C-SiC(111) from Figure 6-3. No XPS peaks for nickel/copper metal or metal oxides between the ranges of 850-960 eV. <sup>6, 7</sup>
Figure 6-S6: Temperature dependent sheet resistances (a) EG/3C-SiC(100), 3C-SiC(100) measurement interrupted at lower temperatures; (b) EG/3C-SiC(111) and 3C-SiC(111) in the range between 4K and 300K.
Figure 6-S7: (a) Sheet resistance (plotted in units of quantum resistance, $h/e^2$ ) as a function of temperature for EG/3C-SiC(100) and EG/3C-SiC(111). (Same samples as

reported in Table 6-2 of the manuscript); (b) Graph showing the combined and de-
identified mobility versus sheet carrier concentration data for EG on Si-face SiC from
literature,8 together with the values for the EG on 3C-SiC from this work. These data as
a whole can be fitted with good confidence with the same power law, indicating that they
share a common conductivity of about $\sim 3 \pm 1$ (e <sup>2</sup> /h)
Figure 6-S8: a) (a) Temperature dependent sheet resistance for EG/3C-SiC(100), 3C-
SiC(100), EG without full coverage on 3C-SiC/Si and EG etched via oxygen plasma (O2
flow rate of 25 sccm at 150W); (b) average Raman spectra (30 μm × 30 μm) of EG without
full coverage on 3C-SiC(100) -SiC LO band intensity is substantially higher than 2D; (c)
Raman peak intensity maps of turbostratic in-plane modes - TS1, TS2 and TS3 of the
poor coverage EG/3C-SiC/Si
Figure 6-S9: Density functional theory calculation results: schematic of the structure
calculated (left, carbon is yellow, Si is blue and 3C-SiC structure was used - see main
text for details) and electronic band structure for EG on 3C-SiC(111) (right) with no
oxidation at the EG/3C-SiC interface and Fermi level at 0.59 eV (dotted line) above the
Dirac point resulting n-type sheet carrier concentration of 2 x 10 <sup>13</sup> cm <sup>-2</sup> 139
Figure 7-1: Cross-sectional view of a top-gate graphene FET

# **List of Tables**

Table 3-1 Summary of all the samples used in this work
Table 4-1 Electrical characteristics measured at room temperature for in-house SiC/Si(100) samples as-grown and after annealing at 1100°C (data acquired with setup 1)
Table 4-2 Residual mean stresses ( $\sigma$ ) for the as-grown and annealed SiC (100) and SiC(111) films and the absolute stress differences between them. The films are of different thicknesses and annealed in N <sub>2</sub> for 2 hours at different temperatures of 1100 $^{0}$ C, 1180 $^{0}$ C and 1250 $^{0}$ C.
Table 4-S1 SiC and silicon resistances (leakage) measured at room temperature for inhouse SiC/Si(100) samples as-grown and after annealing at 1100°C. Results are the averaged values from four measurements
Table 5-1 Summary of the samples used85
Table 5- 2 Hall measured transport characteristics at room temperature. Results are the averaged values extracted from three samples for each type
Table 5- 3 Hall measured transport characteristics at room temperature for IMEM-CNR thin 500 nm and thick 5 μm SiC films grown on the on-axis p-Si and 6° off-axis p-Si substrates. Results are the averaged values extracted from three samples for each type.
Table 5-4 Simulation parameters
Table 5-5 Hall measured transport characteristics at room temperature. Results are the averaged values extracted from three samples for each type
Table 5-6 Electrical characteristics at room temperature for SiC/high-resistivity Si before and after ~20 μm deep etching of silicon between SiC pillars a) van der Pauw Hall measurement results b) TLM leakage resistance results. Results after etching are the averaged values of two samples each
Table 6-1: Summary of attempts to the growth and the transport characterization of epitaxial graphene on Si wafers at room temperature.
Table 6-2 Raman mapping characteristics at 300K, for EG on 3C-SiC/Si of both (100) and (111) orientations showing grain sizes calculated from intensity ratios of D and G bands, peak positions of G and 2D, and FWHM of G and 2D bands. Error bars correspond to the standard deviation of the measured values over an area of 30 x 30 cm <sup>2</sup>

Table 6-3 Hall measured transport properties at 300K. The errors represent the maximum
variation of the values upon the current sweep from 1 to 10 μA112
Table 6-4 Hall characteristics at 300K before and after H-intercalation of EG/3C-SiC(111) (sample 4)
Table 6-S1: Calculated number of layers for the graphene grown on 3C-SiC(100), 3C-
SiC(111) and H-intercalated EG/3C-SiC(111) based on the XPS C1s spectra135

# **List of Acronyms**

CMOS Complementary metal-oxide-semiconductor

2D Two dimensional

CVD Chemical vapour deposition

LPCVD Low-pressure chemical vapour deposition

EG Epitaxial graphene

3C-SiC Cubic silicon carbide

SiC Silicon carbide

SF Stacking faults

APB Anti phase boundaries

UHV Ultra-high vacuum

FET Field-effect transistor

CNP Charge neutrality point

MEMS Micro-electro-mechanical systems

HOPG Highly oriented pyrolytic graphite

QFMLG Quasi free-standing monolayer graphene

SEM Scanning electron microscopy

HRTEM High-resolution transmission electron microscopy

FIB Focused ion beam

TLM Transfer length measurement

ICP Inductively coupled plasma

RIE Reactive ion etching

NEXAFS Near edge X-ray absorption fine-structure spectroscopy

ARPES Angle-resolved photoemission spectroscopy

XPS X-ray photoelectron spectroscopy

FWHM Full width at half maximum

IMFP Inelastic mean free path

LEEM Low-energy electron microscopy

DFT Density functional theory