Carrier Transport and Electrical Conduction in Alloy-Mediated Graphene on Silicon

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Abstract

The possibility of graphene-based micro- and nanoelectronic devices that exploit the extraordinary electronic properties of graphene is the biggest inspiration behind the accelerated development of graphene science and technology. Although the remarkable efforts for establishing graphene as a new electronic material began over 15 years ago, the actual realisation of graphene devices on a large-scale remains elusive, mainly due to feasibility, cost-effectiveness and compatibility issues with the existing semiconductor technology and processes. Significant advancements have been achieved in the synthesis and establishment of transport properties of epitaxial graphene (EG) on 4H- and 6H-SiC, while equivalent progress using silicon (Si) as a platform (via a thin film of 3C-SiC) with reliable electrical transport measurements has not been elucidated to date, due to limitations such as non-uniform coverage of graphene on 3C-SiC/Si and high density of defects within the 3C-SiC.

In this work, we first show that the heteroepitaxial 3C-SiC on Si as the substrate should be carefully approached, as the 3C-SiC/Si heterojunction is electrically unstable and prone to severe leakage or parallel conduction. Subsequently, we find that the interface instability is due to the diffusion of carbon into the silicon matrix during the 3C-SiC growth, creating electrically active interstitial carbon. We overcome these challenges using 3C-SiC on a highly-resistive silicon substrate.

By addressing the parallel conduction issue of the 3C-SiC/Si heteroepitaxial system, in this work, we isolate the charge transport properties of epitaxial graphene (EG) grown directly on 3C-SiC over large areas via an alloy-mediated method and present corresponding physical ab-initio models. Here, we study the properties of EG synthesised on 3C-SiC(100) and 3C-SiC(111). The transport properties of EG on 3C-SiC follow a similar power-law dependence of sheet carrier concentration and mobility and comparable sheet resistance values with the EG on bulk-SiC – although the grain sizes for both are vastly different. Furthermore, we find that the transport properties of graphene within the observed regime are dominated by the substrate interaction, resulting in a large p-type doping, especially for the graphene on 3C-SiC(100). In the case of EG on 3C-SiC(111), the presence of buffer layer reduces the substrate interaction and the charge transfer up to an extent. This work demonstrates a more compelling need to focus

on the engineering of the graphene-substrate interface as opposed to graphene grain sizes in order to tune the charge transport properties of the epitaxial graphene for the integration of 2D materials in functional nanosystems.

Certificate of original authorship

I, Aiswarya Pradeepkumar declare that this thesis, is submitted in fulfilment of the requirements for the award of Doctor of Philosophy, in the Faculty of Engineering at the University of Technology Sydney.

This thesis is wholly my own work unless otherwise reference or acknowledged. In addition, I certify that all information sources and literature used are indicated in the thesis.

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Aiswarya Pradeepkumar

30/01/2020

Dedication

This thesis is dedicated to my parents Pradeepkumar P and Vasanthakumari V

for giving me invaluable educational opportunities

and my husband Nikhil Das

for his support, constant encouragement and care

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List of Acronyms

CMOS	Complementary metal-oxide-semiconductor
2D	Two dimensional
CVD	Chemical vapour deposition
LPCVD	Low-pressure chemical vapour deposition
EG	Epitaxial graphene
3C-SiC	Cubic silicon carbide
SiC	Silicon carbide
SF	Stacking faults
APB	Anti phase boundaries
UHV	Ultra-high vacuum
FET	Field-effect transistor
CNP	Charge neutrality point
MEMS	Micro-electro-mechanical systems
HOPG	Highly oriented pyrolytic graphite
QFMLG	Quasi free-standing monolayer graphene
SEM	Scanning electron microscopy
HRTEM	High-resolution transmission electron microscopy
FIB	Focused ion beam
TLM	Transfer length measurement
ICP	Inductively coupled plasma
RIE	Reactive ion etching
NEXAFS	Near edge X-ray absorption fine-structure spectroscopy
ARPES	Angle-resolved photoemission spectroscopy
XPS	X-ray photoelectron spectroscopy
FWHM	Full width at half maximum
IMFP	Inelastic mean free path
LEEM	Low-energy electron microscopy
DFT	Density functional theory

Chapter 1: Introduction

1.1 Background and Motivation

Silicon-based semiconductor technologies have enabled the improvement of integrated circuit density, and the performance of electronic devices by the continuous miniaturisation as predicted by Gordon Moore in 1965.[1] The continued feature size scaling of complementary metal-oxide-semiconductor (CMOS) transistors have already been experiencing asperities. Figure 1-1 shows the microprocessor trend data over 40 years. Although the transistor counts increases, the power, clock-speed and the performance are at its limits since 2010 due to the physical, material, power-thermal, technological and economic challenges.[1] Alternative technologies (i.e. micro- or nano-devices) using novel materials are required to be the complement to CMOS.

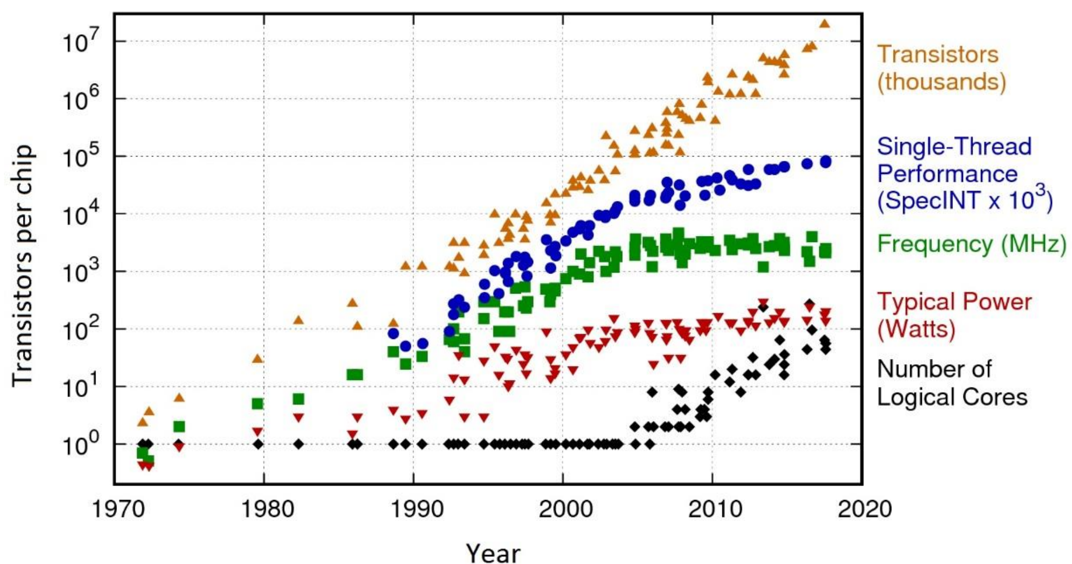

Figure 1- 1: 42 years of microprocessor trend data. Original data up to 2010 collected and plotted by M. Horowitz et al.[2] New data for 2010 - 2017 collected and plotted by K. Rupp (Source: https://www.karlrupp.net/2018/02/42-years-of-microprocessor-trend-data/).

Because of its nanoscale size and extraordinary fundamental properties,[3-7] graphene-based micro- and nanoelectronic devices can help the semiconductor industry to deal with the current CMOS limitations.[4,8]

From the past decade, intensive investigation has been undertaken to unwind the unique and extraordinary electronic properties of graphene[9-12] Due to the outstanding properties, graphene can act as a potential material for various electronic applications such as flexible transparent electrodes,[13-15] interconnects,[16-17] high-frequency transistors,[18] memory

devices,[19] wearable electronic devices and gas sensors.[20,21] Although the fundamental properties of graphene make it ideal for these next-generation electronics; the ability to produce in large areas on an appropriate substrate that is compatible with the current Si-micromachining technologies is a major challenge.

A number of growth methodologies have been reported to synthesize high-quality graphene.[3, 9, 12-13, 22-23] The devices fabricated using mechanically exfoliated graphene flakes have demonstrated the highest performance so far.[24] Besides this, a chemical vapour deposition (CVD) on transition metals is commonly used to produce large-area (up to 30 inches), high-quality graphene in which the grown graphene layers are transferred onto either a semiconducting or insulating substrate.[25] This transfer approach is difficult for commercial, large-scale device fabrication. Therefore, an alternative transfer-free growth technique is essential. Thermal decomposition of silicon carbide (SiC) appears to be a promising self-aligned, transfer-free approach for producing large-scale graphene nanodevices[4] with commended transport properties. [4, 12, 26-27] Yet, the use of the SiC substrate is not compatible with the current semiconductor technologies and processes.

Direct growth of graphene (typically n-type) on silicon substrates has been desirable[28-32] since the silicon wafers are considerably cheap, available in large sizes (up to 12 inches) and enable access to the existing Si-based integrated circuit technology.[32] Direct growth of graphene on silicon is generally described using the thermal decomposition of 3C-SiC/Si. 3C-SiC/Si as a substrate system for graphene possesses several complexities due to the large lattice and thermal mismatches between the 3C-SiC and Si resulting in high density of defects and sharp residual stress at the 3C-SiC/Si.[33-35] A larger Raman D to G intensity ratio (I_D/I_G ~1) was reported for the graphene produced via thermal decomposition of 3C-SiC compared to that of the exfoliated graphene. Furthermore, at relatively low (900 – 1300 °C) growth temperatures, the thermal decomposition process of 3C-SiC/Si reported difficulty in controlling high sublimation rates.[29, 31, 36] The thermal decomposition of 3C-SiC is commonly limited to the use of 3C-SiC/Si(111) substrate.[36]

A few research groups have attempted to report the room temperature transport properties of graphene formed by the thermal decomposition of 3C-SiC/Si,[37-38,28, 32, 37, 39-40] using field-effect transistor (FET) measurements. FET measurements are geometry and

electrostatics dependent and are affected by the substrate.[41] None of the prior studies have considered the influence of the substrate on the transport properties of graphene.

To overcome the challenges of graphene produced by the thermal decomposition process of 3C-SiC, the catalytic approach via a solid source was proposed.[42-44] This method includes depositing a thin layer of metal (nickel or cobalt) on 3C-SiC, followed by annealing. Although these methods have been attempted, uniformity issues and large amounts of defect density remained.[45]

Our research group at the University of Technology Sydney has demonstrated a solid source, alloy-mediated method of graphitisation of 3C-SiC grown on silicon substrate using nickel and copper catalysts and annealing at a temperature of ~1100°C.[46-47] This method is advantageous compared to the conventional thermal decomposition of 3C-SiC in the matter of producing uniform graphene over large scales with much lower Raman I_D/I_G ratios.[45] Major progress has been made on the establishment of transport properties of epitaxial graphene grown on SiC,[4, 12, 27, 31, 48] while an equivalent development of those produced on the silicon substrate is not mature enough to yield plausible electronic devices. Understanding the carrier transport mechanism in graphene synthesised via the alloy-mediated approach on 3C-SiC/Si is vital for the integration of graphene on silicon into the semiconductor industry.

This thesis first describes the interface instability and the parallel conduction issues related to the 3C-SiC/Si heteroepitaxial substrate system. Following that, we provide an in-depth explanation for the historically overlooked leakage phenomenon in 3C-SiC/Si systems by studying the electrical behaviour of 3C-SiC films epitaxially grown under different growth conditions on different silicon substrates. We also demonstrate a solution for the in-plane leakage to obtain isolated SiC mesas or interdigitated structures on silicon.

Addressing the above-mentioned challenges associated with 3C-SiC/Si substrate, this study explains the charge transport properties and presents the corresponding physical models of the transfer-free, wafer-scale, p-type epitaxial graphene grown via the "alloy-mediated" technique on the hetero-epitaxial 3C-SiC synthesised on highly resistive silicon substrates. Using 3C-SiC grown on both (100) and (111) oriented highly resistive silicon substrates, we find that the charge transport properties of the graphene are strongly dominated by the substrate interaction and follows very similar behaviour compared to

graphene on Si- face of 4H- or 6H- SiC.[4, 12, 49] In particular, the presence of oxidation or silicates at the EG/3C-SiC interface results in a charge transfer from graphene into the electron-affinitive oxygen at the interface. This generates large amounts of p-type charges in the graphene, especially in the case of EG/3C-SiC(100). For EG/3C-SiC(111), the presence of a buffer layer in between the graphene and the SiC is found to reduce the charge transfer up to some extent. Within the observed regime, the transport properties of epitaxial graphene on silicon are independent of the graphene grain sizes and the number of layers. Overall, this work suggests a compelling need for tailoring the graphene-substrate interfaces in order to control the transport properties of substrate-supported graphene.

1.2 Significance and Context

The significance of the work is to enable the application of graphene on silicon substrates within the semiconductor industry for the next-generation micro- and nanoelectronic devices. Major advancements have been made in the area of epitaxial graphene on 4H- and 6H-SiC, both in terms of growth as well as the establishment of its transport properties. An equivalent progress on the direct growth technology of graphene on silicon via cubic silicon carbide is also appealing due to its possibility of wide substrate availability, wafer scalability and current semiconductor technology compatibility. However, graphene on silicon approach has not been developed enough yet to yield electronic devices unlike the synthesis on bulk SiC -mainly due to the issue of non-uniform graphene coverage on 3C-SiC as well as the electrical limitations of 3C-SiC/Si.

Heteroepitaxial 3C-SiC/Si system possesses significant limitations due to the high density of defects as well as huge amount of stress at the SiC/Si interface. This will have major consequences on the electrical conduction in 3C-SiC as well as when used as a pseudo-substrate in graphene. To, date few studies have been dedicated to the investigation of the electrical behaviour of 3C-SiC/Si.

This thesis identify a catastrophic interface degradation issue in the 3C-SiC/Si and propose a model for the origin of the interface instability, which is related to the diffusion of carbon atoms into the silicon matrix, forming electrically active interstitial carbon traps. The study address these challenges using 3C-SiC grown on highly resistive Si as the substrate and a solid-source alloy-mediated approach for the graphene growth. Furthermore this thesis isolate and present the temperature-dependent charge transport

properties of the epitaxial graphene on cubic silicon carbide on silicon over large areas and present the corresponding DFT models.

1.3 Thesis framework

The experimental works of this thesis is divided into three sections;

1. Demonstration of SiC/Si heterointerface degradation issue and parallel conduction within the 3C-SiC grown on Si.
2. Explanation of the origin of the interface instability and electrical leakage phenomenon in 3C-SiC/Si and demonstration of a potential solution.
3. Charge transport measurements of epitaxial graphene grown using an alloy-mediated approach on 3C-SiC/highly resistive-Si.

The thesis is structured into seven chapters:

Chapter 1 gives a brief introduction and significance of the work followed by an outline of the thesis.

Chapter 2 gives a detailed state-of-the-art analysis of different graphene growth methods and the respective transport properties.

Chapter 3 provides information on the materials and methodology adopted for this research work.

Chapter 4 - "Catastrophic degradation of the interface of epitaxial silicon carbide on silicon at high temperatures" (journal article). This chapter introduces the 3C-SiC/Si interface instability issue and reports the resulting electrical leakage within the substrate-system

Chapter 5 - "Electrical leakage phenomenon in heteroepitaxial cubic silicon carbide on silicon" (journal article). The chapter models the origin of the SiC/Si interface instability and explains the source of the leakage phenomenon in 3C-SiC/Si which, is directly associated with the epitaxial 3C-SiC growth process.

Chapter 6 – "p-Type Epitaxial Graphene on Cubic Silicon Carbide on Silicon for Integrated Silicon Technologies" (journal article) presents the charge transport properties of epitaxial graphene synthesised on the 3C-SiC/Si system using a catalytic alloy-mediated approach.

Chapter 7 concludes the research work and provides plausible future works that could be performed to advance the work.

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Chapter 2: Literature review

2.1 Graphene - fundamental characteristics

Graphene is a single layer of sp^2-hybridised carbon atoms that are arranged in a hexagonal honeycomb lattice with the C-C bond length of 0.142 nm, see Figure 2-1a.[1] A unit cell of graphene is made up of 2 lattice vectors, a_1 and a_2 (Figure 2-1a), which are defined as:

$$a_1 = \frac{a}{2}(1, \sqrt{3}) \tag{1}$$

$$a_2 = \frac{a}{2}(-1, \sqrt{3}) \tag{2}$$

where, $a = |a_1| = |a_2| = 0.246$ nm, is the lattice constant. The lattice structure of graphene is made up of two interpenetrating hexagonal carbon sublattices, named as A and B that forms the honeycomb pattern. The bonds between the A and B carbon atoms have a strong interatomic coupling of -3.0 eV. The strong value of coupling is the reason for the strength and robustness of the in-plane sp^2-hybridized bonds. The identical A and B carbon atoms make the graphene lattice a sublattice symmetry. The sublattice symmetry greatly influences the electronic structure of the graphene. The structural and electronic properties of graphene are known to arise directly from its lattice structure.[2]

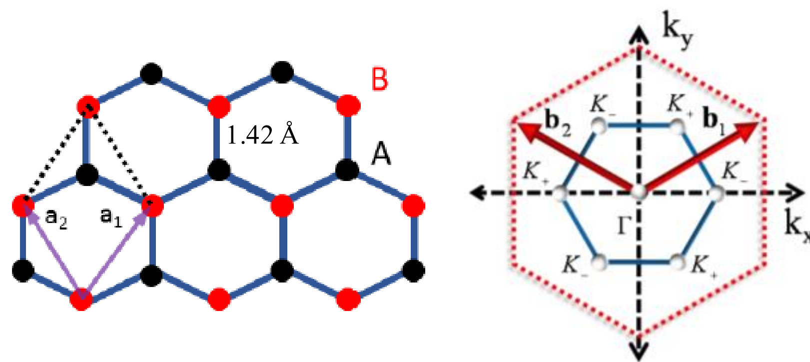

Figure 2-1: a) The lattice structure of ideal single-layer graphene made up of two sublattices, A and B. The unit cell comprised of two hexagonal vectors a_1 and a_2 (length 2.46 Å); (b) Reciprocal lattice of monolayer graphene, defined by the vectors b_1 and b_2. Blue hexagon denotes the first Brillouin zone of graphene, where are Γ, K_+, and K_- are the points of high symmetry.[2]

Figure 2-1b shows the reciprocal lattice of graphene (red dotted hexagon) described by the vectors b_1 and b_2. The Figure also shows the first Brillouin zone of graphene (blue hexagon). Γ (centre of the Brillouin zone) and K_+, K_- (symmetry points around the corners

of Brillouin zone), indicate the high symmetry points. The electronic structure of graphene are localized around these six points in the reciprocal space.[2]

2.2 The electronic band structure of graphene - electronic properties

One of the most astonishing properties of graphene is its zero bandgap, semimetal nature in which the conduction band and the valence band meet at the charge neutrality point, (CNP) -often termed as semi-metallic conductivity.[3-5] The electronic properties of graphene are facilitated by the p_z orbitals arising from the sp^2 bonding of the graphene lattice. P. R. Wallace in 1947 described the band structure of graphene first, using the nearest neighbour tight-binding model (involving only p_z orbitals) and demonstrated the unusual semi-metallic behaviour.[5-7] The tight-binding model was used to approximate the low energy electronic structure of an infinite graphene lattice.[8] Considering that the electrons in graphene can hop to both nearest- and next-nearest neighbor atoms, the tight-binding Hamiltonian for the electrons is[5];

$$\mathrm{H} = -t \sum_{\langle i,j\rangle,\sigma}\left(a_{\sigma,i}^{\dagger} + b_{\sigma,j} + \mathrm{H.c.}\right) - t' \sum_{\langle\langle i,j\rangle\rangle,\sigma}\left(a_{\sigma,i}^{\dagger} a_{\sigma,j} + b_{\sigma,j}^{\dagger} b_{\sigma,j} + \mathrm{H.c.}\right) \quad (3)$$

In which $a_{\sigma,j}$ $(a_{\sigma,i}^{\dagger})$ annihilates (creates) an electron with spin σ = ↑ or ↓. H.c stands for the Hamiltonian conjugation which represents that the Hamiltonian has real eigen values.

The energy vs. wavevector dispersion, E(k), was obtained by solving the Schrödinger equation[8]:

$$\mathrm{H}\Psi = \mathrm{E(k)}\Psi \quad (4)$$

H is the Hamiltonian matrix and Ψ are the wave functions.

Using the tight-binding model and assuming the electron is tightly bound to the lattice sites, the authors from that work obtain the energy dispersion equation[5,8-9];

$$E(k) = \pm\tau\sqrt{1 + 4cos\left(\frac{\sqrt{3}}{2}ak_x\right)\cos\left(\frac{1}{2}ak_y\right) + 4cos^2\left(\frac{1}{2}ak_y\right)} \quad (5)$$

Where a is the lattice constant (0.246 nm). “+” and “–” denotes the bonding (π bands) and the antibonding (π*) states, respectively. The plot of E(k) is the band structure, see Figure 2-2a.

The electronic band structure of graphene consists of hourglass structures around the six corners of the Brillouin zone. This band structure also includes the two inequivalent

points, K_+ and K_-. This conical structure indicates the valence band and the conduction band that meet at the charge neutrality point (usually denoted as the Dirac point) where E(k) = 0 (K point), resulting in a zero bandgap and a linear dispersion at the Dirac point, see Figure 2-2b. The dispersion cones are referred to as Dirac cones. Fermi velocity, V_F is the velocity of quasiparticles at the K point, which is ~10^6 ms^{-1}.[9]

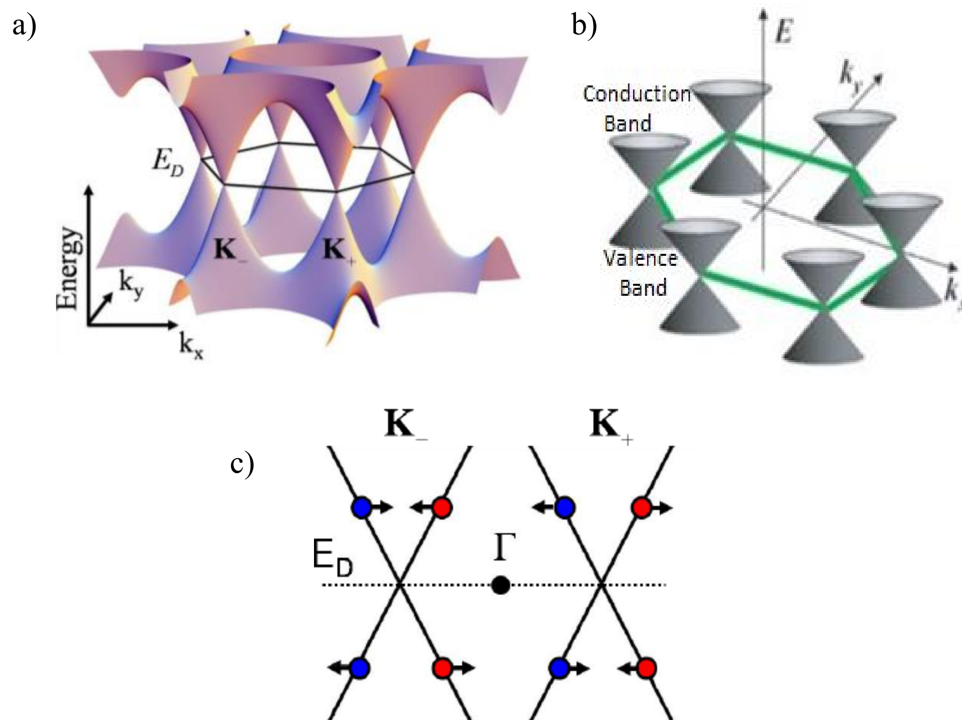

Figure 2-2: a) The electronic band structure of monolayer graphene.[2, 5, 10] The plot shows graphene's electronic bands where the electron and hole states meet at the Dirac point. The K_+ and K_- are the two inequivalent points at the corners of the Brillouin zone (black hexagon). The other four corners are equivalent to either K_+ and K_-, $|K| = 2\pi\frac{a}{3}$, b) Linear dispersion relation showing the vertically mirrored Dirac cones intersecting at the Fermi energy[11]; c) energy dispersion for an infinite graphene sheet along $K_- - \Gamma - K_+$. The pseudospin points parallel or antiparallel towards right moving or left moving particle. Pseudospin depends on whether the particle is located below or above the Dirac point or in the valley.[2]

Electrons within graphene have a chirality referred to as the pseudospin that is related to the momentum vector k. Figure 2-2c shows the pseudospin associated with monolayer graphene (vertical section of two Dirac cones). The pseudospin plays an important role in the charge transport mechanism of graphene.[2, 5, 12]

The carbon atom has six electrons with a [He]$2s^2$ $2p^2$ configuration. In graphene, each carbon atom makes a bond with the other three carbon atoms in the hexagonal crystal two-dimensional plane, by leaving one electron free, which is known as the pi-electron. This pi-electron allows electronic conduction in graphene. A perfect graphene sheet has one free electron per carbon in the pi-level. Therefore, the Fermi level is in between the two symmetrical bands, with no excitation energy needed to excite an electron from just below the Fermi energy to just above the energy position, CNP. The bonding and anti-bonding of the pi orbitals are the reason for the unique and extraordinary electronic properties of graphene.[3, 5] The 2D honeycomb structure is a consequence of electron bonding where the pi bonding and anti-bonding states determine the conduction and valence bands. The linear Energy-Momentum diagram at the Dirac point is one of its results. Because of linear dispersion, the charge carriers in graphene are massless and the bandgap is zero (Figure 2-3)[5] resulting in the semimetal nature.[4] The atomically thin structure of graphene confines the electron transport within the plane, creating two-dimensional electron gas (2DEG) properties.[13-14]

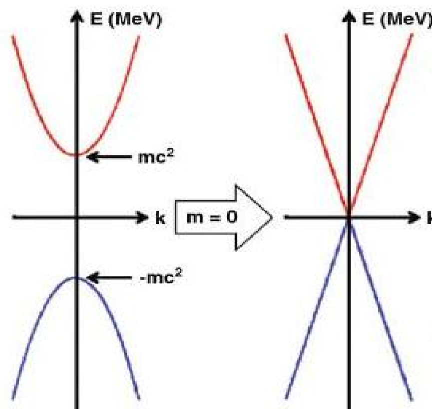

Figure 2- 3: Dirac dispersions with $2mc^2$. At m = 0, the bandgap is zero and the dispersion is linear at the Dirac point.[13]

The lack of bandgap causes significant difficulty in the Field Effect Transistors (FETs) because the FETs need an off state. For the graphene channel to be in an off state there must be an energy gap significantly larger than the thermal excitation energy at the operating temperatures. To overcome this, either a bandgap should be induced by doping[15], or a transport gap should be created by making graphene nanoribbons[16] or strain engineered lattice distortions.[17] Other novel approaches have also been explored by designing special devices that can operate without a bandgap.[4]

Graphene has been extensively investigated in the scientific community over the past fifteen years owing to its outstanding electronic properties such as an exceptionally high carrier mobility (~250,000 $cm^2V^{-1}s^{-1}$)[18-20] and ballistic transport at room temperature.[13-14, 20-22] Graphene also possesses other exciting properties such as significant optical transparency of 2.3%, excellent thermal conductivity of 5,000 $Wm^{-1}K^{-1}$, remarkable Young's modulus at a maximum of 2.4 TPa,[23-27] complete impermeability to any gas,[28] ability to withstand extremely high densities of electric current (a million times higher than copper).[29-30] Another established property of graphene is that it can be readily chemically functionalized.[1, 31-32]

Graphene acts as a potential material for various electronic applications such as flexible transparent electrodes,[33] micro-electro-mechanical systems,[34] high-frequency transistors,[35] and memory devices[36] and gas sensors.[37] This is because of the extraordinary properties of charge carriers in graphene, including high mobility high saturation velocity (~ 5.5×10^7 cms^{-1}), stable crystal structure and ultrathin layer thickness (~ 0.3 nm).[38] Despite these significant properties, graphene electronic devices are currently not widely available and this is due in part to the difficulties associated with its large-scale production processes. The following sections briefly explain different graphene growth techniques.

2.3 Graphene growth methods

In 1962, Boehm et al. reported the synthesis of a suspended monolayer graphite.[39] The name "graphene" was coined by H. P Boehm in 1986.[40] Number of methods have been reported for synthesizing graphene. The most commonly used techniques are mechanical exfoliation of highly oriented pyrolytic graphite (HOPG),[13] chemical vapour deposition (CVD) on transition metals and dielectrics,[33, 41] graphene oxide reduction,[42] unzipping of the carbon nanotubes,[43] and the thermal decomposition of SiC.[14] Among the above methods, mechanical exfoliation, CVD growth and the thermal decomposition of SiC received enormous attention within the scientific community. The following sections give brief explanations of these methods.

2.3.1 Mechanical exfoliation of single-crystal graphite

Andrei Geim and Kostya Novoselov first performed mechanical exfoliation where they separated a single graphene layer from highly ordered pyrolytic graphite (HOPG)[1] using adhesive tape and transferred the layer onto oxidised Si wafers to analyse the electrical properties.[44] This commonly used graphene growth method is reported to yield the highest quality graphene with superior device characteristics to date.[18,3, 13] Graphene produced by this method typically needs to be transferred on to appropriate substrates such as SiO_2 for further application. The transfer process, however, limits the electrical properties due to the scattering with the substrate.[23, 45] Also, the transfer process to suitable substrates can create defects in the graphene that can affect the quality of graphene-based devices. Transferring flakes of graphene in a production environment is not practical as wafer scaling is not possible. Besides these issues, the technique prevents the control of graphene thickness, grain size, and the number of layers over a large scale. Therefore, mechanical exfoliation is not an appropriate technique for large-scale device fabrication, and a more appropriate method is required.

2.3.2 Chemical vapour deposition on transition metals and dielectric insulators

The chemical vapour deposition (CVD) utilises carbon-source gases such as methane, ethane, or propane that decompose at high-temperature on the surface of metals, such as Ni, Ru, Ir, Cu, Co, forming graphene.[46-49] Bae et al. produced large-scale graphene films up to 30 inches using the roll-to-roll CVD method in 2011 for transparent electrodes application.[33] Graphene produced using this method demonstrated a sheet resistance value of 125 Ω/☐, optical transmittance of 97.4% and half-integer quantum Hall effect.[33] The factors such as grain boundaries, lattice defects, dislocations, and other substrate-related features are identified to contribute to the electronic scattering mechanism for CVD graphene.[50] Even though the graphene produced by the CVD shows advantages, the need to etch away original metal substrate, transfer graphene flakes onto a dielectric substrate and the chances of detrimental folds and ripples involved in the transfer process can all increase the cost as well as degrade the performance of nanoelectronic devices based on it.[30] Furthermore, large-scale fabrication of micro- and nanodevices at wafer level will be unrealistic to achieve if the graphene flakes have to be individually transferred and positioned onto the substrates.[51] Hence, new methods have to be explored. In order to avoid the post-growth transfer process, CVD growth is also performed on dielectric (SiO_2, TiO_2, h-BN, Al_2O_3, quartz, Si_3N_4 etc.) substrates.[52-56] The CVD graphene (single layer with grain sizes of ~250 µm – single crystalline) in which the grain boundary scattering and transfer-induced contamination are reduced has demonstrated mobility up to 30,000 $cm^2V^{-1}s^{-1}$ on h-BN substrates.[50] CVD on dielectrics are usually difficult due to the low surface energy of the dielectrics.[57] So a plasma-enhanced CVD at low temperatures are used.

2.3.3 Graphene on semiconductors

Growing graphene directly on semiconductors are essential for graphene-based micro- and nanoelectronic and optoelectronic devices. This will avoid the time-consuming, costly, defect inducing, transfer process involved in the CVD and exfoliation methods. Even though IBM has demonstrated a full wafer-level transfer of a single graphene sheet, the method faces several challenges such as rippling, lower adhesion to the underlying substrate and inconveniency in terms of large scale production.[58] As a solution to these, many researchers have discovered various methodologies of growing graphene directly

on the semiconductors/insulating substrates such as silicon, quartz, aluminium nitride, boron nitride, sapphire, and silicon carbide.[59-63] Graphene growth on these substrates offers improved potential for various applications such as solar cells, interconnects, and heat sink structure interconnects.[30, 51]

Among all potential semiconducting substrates for graphene growth, SiC has gained much attention in the graphene community due to the high-quality graphene it can produce. Graphene on SiC so far has achieved significant advancements both in the area of growth and control of properties.

2.3.4 Thermal decomposition of silicon carbide

Thermal decomposition of SiC is currently a well-established technique for obtaining high quality and reproducible, graphene for electronic applications.[14, 64-68] This method enables the graphene to be grown directly on top of a commercially available insulating or semi-conducting hexagonal (4H- 6H-) SiC substrates. Therefore, the damages involved in the process of transferring graphene to different substrates are completely avoided.[30] The growth procedure involves annealing bulk SiC wafers at high temperatures (above 1400 °C) in vacuum or atmospheric pressure. Due to the higher vapour pressure of silicon compared to carbon, silicon atoms sublimate, leaving behind the carbon atoms that rearrange to form graphene layers. Badami et al. first identified the thermal decomposition process for graphene in 1965.[69] SiC crystals were annealed in high temperature (~ 2180 °C) in vacuum to obtain the graphite. Bommel et al. demonstrated the formation of monolayer graphite on hexagonal SiC at only 800 °C in ultra-high vacuum (UHV) in 1975.[70] These reports refer to graphene as monolayer graphite. Furthermore, G.E. Acheson who synthesised SiC for the first time in 1891, had also reported graphitic layers on SiC.[71]

The first report of patterned epitaxial graphene synthesised on 6H-SiC was published in 2004, by Berger et al. in an article titled "Ultrathin epitaxial graphite and a route to graphene-based electronics".[14] Later, in 2009, Emstev et al. demonstrated a method to produce graphene layers on SiC that are morphologically improved. Here, the bulk SiC wafers were annealed in argon at ~1650 °C.[65] Being a polar material SiC has two inequivalent surface terminations; Si-face that corresponds to (0001) polar surface and C-face that corresponds to $(000\bar{1})$. Graphene has been generally synthesized on different

polarity faces of SiC (Si-face and C-face). Norimatsu et al. and Luxmi et al. demonstrated that the number of epitaxial graphene layers on SiC can be controlled by varying the annealing temperature and the time.[72, 73-74] Furthermore, Ouerghi et al.[75] demonstrated the synthesis of uniform monolayer graphene on terraces of off-axis 6H-SiC by controlling the silicon sublimation rate.

2.3.5 Direct growth of graphene on silicon substrates

Despite being much more challenging, growing graphene directly on silicon substrate is also appealing due to the widespread availability (readily available up to 450 mm in diameter) of silicon and its compatibility with the existing well-established semiconductor technologies and processes.[30] Large-scale graphene should be synthesised on top of silicon substrates to translate the graphene properties into integrated technologies. Due to the low diffusivity and relatively high solubility of carbon on Si surface, graphene growth on silicon has been attempted mainly through a) Germanium and b) a thin film of 3C-SiC, among which the research on 3C-SiC has been receiving much interest.[30] The following section will discuss the problems associated with using 3C-SiC/Si as substrates for epitaxially growing graphene.

2.3.5.1 Heteroepitaxial 3C-SiC on Si

Heteroepitaxial cubic silicon carbide on silicon has attracted enormous interests for the high temperature, high power, high frequency, electronic and micro-electromechanical systems (MEMS) applications even in a harsh environment, due to its wide bandgap and saturated electron drift velocity of SiC ($\sim 2\times10^{7}$ cms^{-1}).[76] Despite the smallest bandgap of 3C-SiC, this is the only polytype of SiC that can be grown heteroepitaxial on large diameters of silicon at lower growth temperatures (below 1500 °C).[77] This makes 3C-SiC a promising material for the fabrication of power electronic devices on a large scale at a low cost. Despite its significant properties, devices based on 3C-SiC are not yet commercially available. This could be attributed in part to the stress-related issues of the 3C-SiC.

2.3.5.2 CVD growth of heteroepitaxial 3C-SiC on Si

The first breakthrough of 3C-SiC growth on Si was by Nishino et al. in 1982.[78] 3C-SiC films are usually grown in a CVD reactor (resistively heated hot wall) using silane (SiH_4),

ethylene (C_2H_4) and propane (C_3H_8) as the suppliers of silicon and carbon (precursor gases) and H_2 as a carrier gas in a three-step process.[78] In the first step, the Si substrate is prepared by etching in a mixture of 4.0 mole % of HCl and H_2, which is heated to 1200°C.[78] A buffer layer growth follows this step. Here, a flow of 0.03 mole % C_3HS in the H_2 is established at room temperature, and the temperature is raised to 1400°C in less than a minute and held for about a minute. After that, the gas flow is shut off and the susceptor allowed to cool down to room temperature. Finally, the crystal is allowed to grow by heating the susceptor and the Si wafer to 1400 °C. Once the temperature has reached the equilibrium, 0.04 mole % silane and 0.02 mole % propane is established in the H_2 flow and the 3C-SiC layer is grown on top of the buffer layer.[78]

The large lattice mismatch (20% at 300 K , (a_{SiC} = 0.436 nm, a_{Si} = 0.543 nm) and thermal expansion coefficient difference (8% at 300 K and 23% at growth temperatures) of 3C-SiC with silicon cause intrinsic strain and huge amounts of defects (stacking faults and anti-phase boundaries, micro twins, and voids in the silicon below the interface). These defects make the epitaxial growth of 3C-SiC on silicon extremely challenging for device-grade applications.[77, 79-80] Note that it has also been reported that growing 3C-SiC films in thick (few hundreds of µm) or on off-axis Si reduces the defects up to some extent.[77] Iacopi et al. demonstrated a significant amount of tensile stress originated in the 3C-SiC films that resulted in excessive concave wafer curvature making further wafer processing extremely difficult.[77, 81] Zielinski et al. observed a less concave curvature for the 3C-SiC films grown at 1300 – 1400 °C due to the creep effects modifying the intrinsic strain in the films.[79] In addition, Camarda et al.[82], Anzalone et al.[83], and Watts et al.,[84] reported that when grown at 1300 – 1400 °C, a strong compressive stress originated at the heterointerface (during the carbonization step) bows the 3C-SiC/Si system downwards. As a consequence of the stress, non-ideal diode characteristics have been reported for the n-SiC/p-Si heterojunction, which limits the reliability of 3C-SiC devices.[85-86] A detailed evaluation of the electrical stability of 3C-SiC films is missing in the literature. All these makes the electrical measurements of graphitized 3C-SiC/Si extremely challenging.

2.3.6 Graphene on silicon using heteroepitaxial cubic silicon carbide

Two of the most promising approaches for graphene on 3C-SiC on silicon are 1) thermal decomposition of 3C-SiC/Si and 2) metal-mediated graphene growth. The following section will discuss the two methods briefly.

2.3.6.1 Thermal decomposition of 3C-SiC on Si

Many researchers have demonstrated the thermal decomposition process of 3C-SiC on Si for graphene growth.[87-93] In 2009, Suemitsu et al. presented the first report of epitaxial graphene growth using 3C-SiC(111)/Si(110) substrate.[90, 94] Graphene growth using this method involves first, growing thin film of 3C-SiC on Si substrate via gas source molecular beam epitaxy (GSMBE) using monomethyl silane gas source and then annealing 3C-SiC in ultra-high vacuum at high temperature (~1300°C) for about 30 min to form epitaxial graphene. This has also been reported by Aristov et al. who named graphene produced via these methods as graphene on silicon (GOS).[93] Ouerghi et al. also explained the graphene growth technique in ultra-high vacuum using silicon sublimation temperature between 1,150°C and 1,300°C.[89] Graphene produced via thermal decomposition of 3C-SiC is affected by defects, surface roughness and the crystallographic orientations of the 3C-SiC films, among which the defects and crystalline orientations of the SiC films affects the most.[91-92] (100) oriented 3C-SiC was characterized by large amounts of anti-phase boundaries.[95] These anti-phase boundaries propagate into the graphene layers and affect the intrinsic properties of the graphene. 3C-SiC films were grown on off-axis Si substrates to overcome this issue.[95] It is believed that the 3C-SiC of (111) orientation is desirable due to the absence of anti-phase boundaries and the similarity of its hexagonal symmetry with that of the 6H-SiC.[30, 96] Thermal decomposition of SiC/Si has major limitations. At lower growth temperatures (900 - 1300°C), the quality of graphene produced at ultra-high vacuum pressure is limited due to the difficulty in controlling the sublimation rates.[30] The Raman D to G intensity ratios are much larger (~1) than that of the exfoliated graphene.[87, 90] This growth technique is mainly limited to the 3C-SiC(111) surfaces.[87]

2.3.6.2 Metal mediated growth on cubic silicon carbide on silicon

To overcome the limitations imposed by the thermal decomposition of 3C-SiC/Si, a few research groups investigated a catalytic method of producing graphene on the 3C-SiC surface.[97-100] The process involves depositing a thin metal layer of nickel or cobalt on the surface of 3C-SiC and subsequent annealing of the metal/3C-SiC/Si samples at temperatures between 750 and 1200°C. The growth temperature in this method is significantly lower than that of the thermal decomposition processes. During the process of annealing, the metals react with the 3C-SiC to form metal silicides and release carbon atoms, that subsequently rearrange to form the graphene. Most cases found graphene present on the metal surface after the growth, which again required to be transferred on to an appropriate substrate. These are limited by the large defect density and non-uniformity of the graphene.[97, 99]

In order to overcome these challenges, our research group guided by Prof Iacopi has described a self-aligned method in which the graphene is grown directly on top of a silicon substrate via a thin film of 3C-SiC using nickel and copper as the catalysts.[100-101] Figure 2-4 shows the graphitisation process.[100]

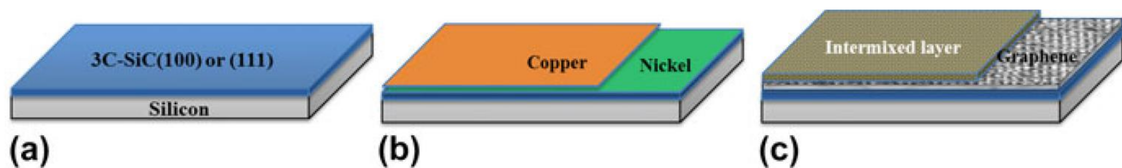

Figure 2-4: Schematics of direct graphene synthesis on epitaxial 3C-SiC[100]

Generally, (100) or (111) orientations of 3C-SiC/Si are selected as the substrate materials for the graphene growth. Thin layers of Ni followed by Cu are sputtered on the 3C-SiC and then annealed at ~1100 °C. The annealing step results in the formation of a highly intermixed layer comprising metals silicides and residues, which is subsequently removed by a wet freckle etch in acids.[100] The graphene layer obtained via this alloy-mediated approach uniformly covers a 2” Si wafer with a very low Raman D to G intensity ratio in the range of 0.2 to 0.3, indicating a low defective graphene,[100] and is more than ~3x fold smaller than that obtained using the thermal decomposition of 3C-SiC/Si.[87, 92, 102]

2.4 Transport properties of graphene

This chapter gives a review of the electronic properties and charge transport of graphene. Graphene has been extensively heralded as one of the most promising materials for the next-generation integrated and miniaturised applications extending from nanoelectronics, interconnects and micro-electro-mechanical systems to optoelectronics. Comprehensive knowledge of the electrical conduction mechanism within the graphene is vital, not only for achieving the device applications but also for continuous performance optimisation.

The pioneering investigation of graphene, its electronic band structure, and linear dispersion began in 1947 by Wallace.[6] Graphene-like structures were already documented since the 1960's however, there were experimental difficulties in isolating monolayers of graphene for performing electrical measurements. In 2004, two physicists Geim and Novoselov at the University of Manchester isolated the single-layer of graphene via the scotch tape mechanical exfoliation method and transferred it onto oxidized silicon substrates for determining the electrical characteristics and to verifying its unique two-dimensional (2D) properties.[13, 44] These scientists were jointly awarded the Nobel Prize for Physics in 2010 for their ground-breaking experiments on graphene. Ever since graphene was isolated, much research was devoted to growth techniques for producing high-quality graphene in large-scale for future electronic devices[14, 103-104] including radio frequency transistors and digital switches.[105-106] The studies mainly focused on two different methods; 1) micromechanical exfoliation of graphite,[40, 44] and 2) graphene grown directly on various substrates known as epitaxial graphene[14, 68-69, 73, 107-110] among which the latter is identified as most amenable for large-scale device processing.[68]

The following section briefly describes the electrical properties of graphene synthesized via different methods.

2.3.1 Mechanically exfoliated graphene

Micromechanical exfoliation of graphite is known to produce the highest quality graphene with the best device characteristics.[18, 20] It has been reported that a suspended single layer of exfoliated graphene demonstrates charge carrier mobility of 200,000 $cm^2V^{-1}s^{-1}$ at $2x10^{11}$ cm^{-2} that allows for a possibility of ballistic transport at cryogenic temperature.[13, 18-20, 111] However, when graphene is transferred onto the SiO_2 substrates, electron scattering by optical phonons of the substrate limits the mobility to a value of

~40,000 $cm^2V^{-1}s^{-1}$.[23, 45] Morozov et al. obtained charge carrier mobilities more than 200,000 $cm^2V^{-1}s^{-1}$ for bilayer graphene at extremely low electron-phonon scattering at room temperature.[111] It was reported that the interaction with the substrate is responsible for the scattering is mechanism in graphene.[18] Charged impurities, interfacial phonons, substrate stabilized ripples, process residues under the graphene, were all considered to contribute to the scattering.[23, 111-112] Improving the substrate quality or removing the substrate were considered as a solution to these.[18]

2.4.1 CVD graphene grown on copper substrates transferred to SiO_2/Si

Owing to the extremely low solubility of C in Cu, many researchers have investigated the CVD (at atmospheric pressure, or below) growth of graphene on metals like Cu.[109-110, 113] Zhang et al. demonstrated a two-step CVD process using toluene as the carbon source to grow the monolayer graphene layer on an electro-polished Cu foil surface at 600°C. They reported for graphene layers transferred to SiO_2/Si substrates hole and electron mobilities of 811 and 190 $cm^2V^{-1}s^{-1}$, respectively. The sheet resistance was ~8 kΩ/□. The domain sizes of graphene grown via these techniques are much larger and are in the order of several mm.[114-115]

2.4.2 CVD graphene grown on copper substrates transferred to Ge(001)

Legally et al. reported that when CVD grown graphene on copper substrate is transferred to germanium, Ge(001), they obtained extremely high conductivity and charge carrier mobility (derived from the relevant transport measurements), higher than that of freestanding, edge-supported graphene (under some circumstances).[116] A mobility of ~5 x 10^5 $cm^2V^{-1}s^{-1}$ at 20 K and ~10^3 $cm^2V^{-1}s^{-1}$ at carrier densities of ~10^{14} cm^{-2} at 300 K were obtained. This work also studied the influence of substrates on the transport properties of graphene by analysing the properties of graphene transferred to different substrates. They reported that carrier scattering from charged impurities trapped in the supporting substrate and at the graphene-substrate interface is thought to be significant factors for graphene mobility limitations.[116]

Epitaxial graphene on semiconductors

2.4.3 Epitaxial graphene on SiC via thermal decomposition

Berger et al. reported the first transport measurements on oriented and patterned epitaxial graphene on SiC that had been formed via thermal decomposition at ~1250 to 1450°C in ultra-high vacuum (10^{-10} Torr).[107] They demonstrated the two-dimensional nature of charge transport in multilayered graphene (three layers, continuous over several mm) grown on 6H-SiC(0001). The transport properties reported n-type graphene with a sheet carrier concentration of 3.6×10^{12} cm^{-2}, mobility of 1100 $cm^2V^{-1}s^{-1}$ and sheet resistance of 1.5 kΩ/□ (at 4 K). Further improvement in the mobility values of graphene was reported using a confined controlled sublimation process.[64, 107] In 2010, de Heer's research group fabricated an array of 10,000 transistors (top-gated) on a single 0.24 cm^2 chip; believed to be the largest density of epitaxial graphene devices so far.[117] Graphene synthesised via thermal decomposition in high-vacuum has smaller grain sizes that fall in the range between 30 - 200 nm with varying thicknesses.[103, 118] Furthermore, it is believed that the quality of graphene produced by ultra-high/high vacuum is reduced due to higher Si sublimation rates at comparatively low growth temperature. To overcome these issues, in 2009, Emstev et al. developed a new method in which the SiC is annealed in an argon atmosphere at high temperature (~1650°C).[65] This resulted in improved grain sizes up to 3 µm x 50 µm. Several researchers then demonstrated much larger grain sizes – more than 75 mm.[119-120]

Electronic properties of epitaxial graphene on SiC depends upon the type of surface termination of SiC (Si-face or C-face). The differences between graphene grown on the C- face ($000\bar{1}$) and the Si-face (0001) were first reported by Bommel et al.[70] Many groups worked on growing large-area single-crystalline monolayers of epitaxial graphene on the Si-face of SiC(0001).[65, 72] It was demonstrated that graphene grown on the Si-face of SiC(0001) possesses a carbon-rich amorphous interfacial layer ($6\sqrt{3}$ $6\sqrt{3}$ R 30) that is partially covalently bonded with the substrate, see Figure 2-5. In addition, the X-ray photoelectron spectroscopy shows the presence of buffer layer components in the C 1s spectra. The interfacial layer acts as an electronic buffer between graphene and the substrate. Since SiC is polar in nature, the transport properties of graphene grown on the buffered substrate are reported to be limited by the polarization effect induced by the buffer layer and the Si dangling bonds on the SiC(0001).[121] Generally, the epitaxial

graphene on SiC has electrons as charge carriers with a carrier concentration of ~10^{12} cm^{-2} and mobility up to ~3000 $cm^2V^{-1}s^{-1}$ at 300 K (measured using hall bars) for the graphene grown on the Si-face.[122-123] The mobility increased significantly when the carrier concentration was decreased with a maximum value of 30,000 $cm^2V^{-1}s^{-1}$ for $5x10^{10}$ cm^{-2} at low temperature.[124-125] The n-type conduction was explained by the donor like states associated with the buffer layer and at the SiC/graphene interface that compensate the polarization effect.[126] Besides, the X-ray photoelectron spectroscopy shows the presence of buffer layer components in the C 1s spectra. Multiple layers of epitaxial graphene formed on Si-face SiC are reported to be ABC stacked.[121]

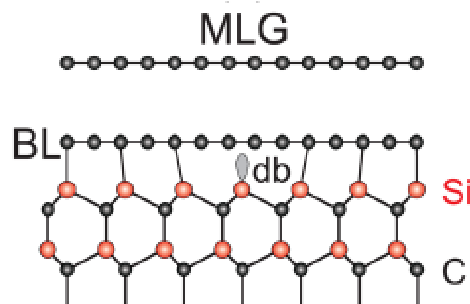

Figure 2-5: Structure of monolayer graphene on Si-face SiC(0001) with a buffer layer.[122]

Graphene on the C- face of SiC does not have a buffer layer. The graphene layers exhibit weaker interactions with the substrate and therefore exhibit superior transport properties.[68, 121] In contrast to the graphene grown on the Si-face of SiC, the graphene grown on the C-face of SiC tends to be thicker[127] and turbostratically stacked.[128] Multilayers of graphene on C-face have an electronic structure similar to that of the monolayer graphene.[128] Norimatsu et al. reported that the graphene layers formed on the C-face are rotationally disordered.[121] De Heer's group reported the rotational faulting decouples the graphene layers and results in properties that are dependent upon single-layer graphene,[129] which also reported by Sprinkle et al.,[10] Wu et al.[130] and Miller et al.[131] Hite et al. discovered that graphene is grown as islands on the C-face.[132] That is, a fully developed graphene contains disoriented grain with non-uniform thickness. To overcome this issue, Ouerghi et al. reported graphene growth on off-axis 6H-SiC(0001) wafers in ultra-high vacuum demonstrating a uniform graphene monolayer by limiting the Si sublimation rate with the help of nitrogen and silicon fluxes.[75] Lin et al. reported Hall measurements on multi-layer epitaxial graphene grown on C-face SiC and indicated the presence of several groups of charge carriers with different mobility ranges.[127] Graphene on C-face shows much larger mobilities compared to those on the Si-face. A mobility of

20,000 $cm^2V^{-1}s^{-1}$ was reported for carrier concentrations in the order of ~10^{12} cm^{-2} at 4 K.[133-134] The mobility increased up to 39,800 $cm^2V^{-1}s^{-1}$ when the carrier concentration was reduced to ~10^{11} cm^{-2}. At room temperature, the top-gate FET mobilities were measured to be 7000-8000 $cm^2V^{-1}s^{-1}$ at carrier concentration of 1.5x10^{12} cm^{-2}.[135] For 5 layers of graphene on C-face SiC, a mobility of 20,000 $cm^2V^{-1}s^{-1}$ or more and a sheet resistance of 200 Ω/□ were measured.[107] Quasi neutral graphene layers possess the highest value of mobility at room temperature, which is 10^6 cm^2 V^{-1} s^{-1} at carrier concentration of 10^{10} cm^{-2}.[136] The difference between the transport properties of graphene on C-face and the Si-face of SiC is shown by Tedesco et. al.[68] This group reported transport properties of graphene grown on both the C-face and Si-face via vacuum sublimation of hexagonal 4H- and 6H- substrates. Mobilities and sheet carrier concentrations of the samples were measured at 300 and 77 K, see Figure 2-6. It demonstrated that the samples show a decrease in mobility with an increase in carrier concentration. This group reported graphene mobilities for near-intrinsic carrier densities at 300 K, which are ~150,000 cm^2 V^{-1} s^{-1} for the EG grown on the C-face and ~5800 cm^2 V^{-1} s^{-1} for that on the Si-face.[68]

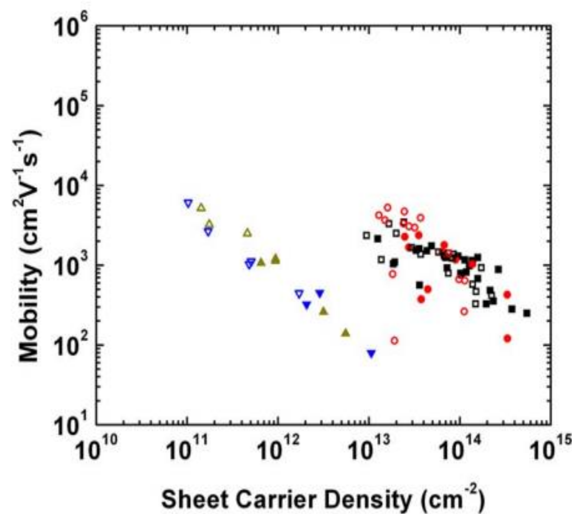

Figure 2-6: Mobility and sheet carrier density data of the EG synthesized on Si-face of bulk 4H- and 6H-SiC semi-insulating wafers at 300 and 77 K from Tedesco et al.[68] Triangles represent the data of EG on Si-face of SiC; Squares and circles represent the data for n-type and p-type EG on the C-face of SiC, respectively.

2.4.4 H-intercalation of graphene on SiC

Graphene layers supported on substrates are known to have transport properties limited by the scattering at the interface.[137] Hence, interface engineering while keeping the structural quality and the epitaxial character intact has been discussed extensively. H-

intercalation is a feasible way of tailoring the interface between graphene and the substrate.

Riedl et al. performed hydrogen intercalation underneath the buffer layer, so the hydrogen saturates the Si-C and dangling bonds.[138] The material after H-intercalation was named quasi-free-standing monolayer graphene (QFMLG), on an H-terminated SiC(0001) surface, see Figure 2-7. The carrier density of QFMLG was reduced and the carrier type was reversed to be p-type.[137-139]

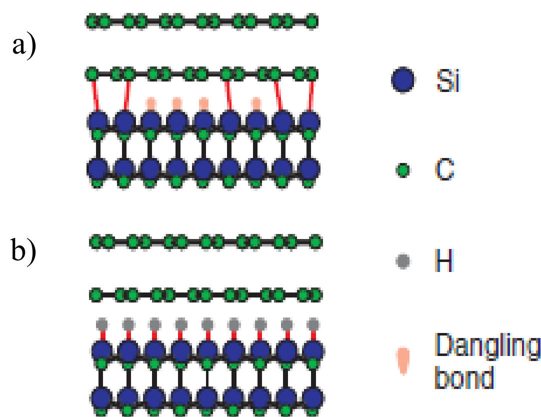

Figure 2-7: Structure of a) Monolayer graphene on top of buffer layer/3C-SiC b) Quasi-free standing bilayer graphene after H-intercalation – buffer layer decoupled from substrate forming additional graphene layer.[138]

Speck et al. examined the properties of QFMLG on 6H-SiC(0001) using infrared absorption spectroscopy, Raman spectroscopy, and the Hall effect.[122] They reported that the QFMLG is hole-doped and mobility of ~3100 cm^2/Vs at 300K. P-type doping was explained by the influence of the spontaneous polarisation of the hexagonal SiC. Furthermore, the group also demonstrated that the doping for QFMLG on 4H-SiC(0001) is 1.5 times larger than that for QFMLG on 6H-SiC(0001) due to larger polarization of the 4H-SiC substrate.[139-141]

Synthesis of graphene on the semi-insulating SiC surface at high-temperature (vacuum or an argon atmosphere) is a promising method that is well established so far. Nevertheless, commercial SiC substrates are expensive and are limited in sizes. A cost comparison of 4H-SiC(0001) and 3C-SiC for Schottky diodes show that a 6 µm thick 4H-SiC would cost about 20$/$cm^2$ when compared to 2$/$cm^2$ for a 3C-SiC of similar thickness produced on an 8" Si substrate.[77] In addition, SiC is not compatible with the existing Si-based technology and processes within the semiconductor industry.

2.5 Direct growth of graphene on silicon

From the perspective of large-scale graphene production for micro- and nano-electronic devices, synthesis of epitaxial graphene directly on Si substrates could possibly permit the post-Si-CMOS roadmap to be a reality. This is primarily due to its micromachining compatibility, low production cost and wafer-scaling capabilities. There have been several attempts towards the area of epitaxial growth of graphene on silicon primarily through either a thin film of germanium or a cubic silicon carbide, among which the latter received enormous interest.

2.5.1 Thermal decomposition of cubic silicon carbide on silicon

Thermal decomposition has been mainly performed on 3C-SiC(111) and 3C-SiC(110) substrates. According to the published reports, the graphitisation of the 3C-SiC(111) is analogous to that of the Si-terminated bulk SiC(0001) surfaces.[88] Photoelectron spectroscopy (PES) data has proven the existence of a buffer layer between the graphene and the SiC(111) substrate, which is similar to the graphene grown on the bulk SiC(0001) surfaces.[49]

Ouerghi et al.[102] reported that in few-layer n-type graphene, the interaction between graphene and the C-face 6H-SiC is much weaker than in the case of graphene on 3C-SiC(100). Bharati et al.[87] also reported on epitaxial graphene on 3C SiC (111) substrates formed via high-temperature annealing. This work reported Bernal stacking of graphene layers and formation of buffer layer in between the graphene and the substrate. The grain sizes reported by this work are between 10 - 15 nm. Later in 2016, the same group reported on APRES measurements of the graphene and found slight n-type doping, less than that of graphene grown on bulk SiC.[142] Electronic structure of few-layer epitaxial graphene on 3C-SiC(100) grown via Si sublimation at high temperature, ultra-high vacuum condition has been studied using near-edge X-ray absorption fine structure spectroscopy (NEXAFS) and angle-resolved photoemission spectroscopy (ARPES) by Aristov et al.[93] However, these studies were not able to evaluate the transport properties of graphene.

Table 2-1 shows a summary of all attempts to measure the graphene transport properties. Kang et al.[143-144] characterized back-gate FETs using a 10 µm wide few-layer graphene (grain size in the range of 8 – 17 nm) channel grown on 3C-SiC(110)/Si(110) via thermal

decomposition in ultra-high vacuum.[144] An n-type behaviour with a sheet carrier concentration of 0.67 to 3.4 x 10^{11} cm^{-2}, estimated mobility of 430 to 6200 $cm^2V^{-1}s^{-1}$ and sheet resistance of 2.84 – 215 kΩ/□ were reported. However, the data showed the presence of massive gate-leakage current that affects the transport properties of the graphene. Later, the same group[143] reported on top-gate few-layer n-type epitaxial graphene FETs fabricated on Si(111) and Si(110) substrates. The sheet resistance (Rsh) is calculated as 90 kΩ/□ on Si(1 1 0) and 17 kΩ/□ on Si(1 1 1).

Moon et al. reported the ambipolar transport properties of top-gated graphene field-effect transistor Si (111) wafers.[145] The field-effect mobility values of 285 $cm^2V^{-1}s^{-1}$ for holes and 175 $cm^2V^{-1}s^{-1}$ for electrons were reported. This group reported a sheet carrier concentration of 6 x 10^{11} cm^{-2} at room temperature, and the electron mobility was ~950 $cm^2V^{-1}s^{-1}$, characterised by a non-contact Hall Lehighton setup. However, no study on the quality of the graphene was demonstrated.

Lee et al.[146] also reported the room temperature transport properties of graphene on Si that is grown via intermediate H-terminated Ge layers. Here the transport measurements were performed on EG only after it was transferred onto a SiO_2/Si substrate – this will be different from the case when EG is on its original substrate.

Aristov et al.[93] and Bharati et al.[142] have reported the n-type sheet carrier concentration of the EG grown on 3C-SiC/Si through the ARPES measurements, however no details on the charge carrier mobility and the sheet resistance are given.

Debrowski et al.[147] has reported the electrical properties in FET configuration for the graphene grown on μm^2 size Ge(100) islands pre-deposited on the Si(100) substrate.

Although attempts were made in the past to report the transport properties of graphene grown directly on silicon, the measurements were not performed on large areas. Note that most of the existing works in the literature although claiming to investigate the electrical properties studied either the ARPES electronic band structure or the room temperature field-effect properties of the graphene. It is widely known that the FET measurements are geometry and electrostatics dependent and are affected by the substrate. This type of measurements do not permit to assess the carrier scattering mechanism involved in the electrical conduction. Hence, the temperature-dependent Hall effect measurements over larger areas are essential to study the carrier transport mechanism in detail. Besides these,

the use of 3C-SiC/Si should be carefully approached as the presence of a large density of defects within the 3C-SiC can result in parallel conductions within the heteroepitaxial system.[80, 86] None of the prior attempts have effectively taken the involvement of parallel conductions into consideration when evaluating the transport measurements. We identify this as a significant gap that is critical for any practical graphene-based electronic or photonic applications.

Table 2-1 Summary of the transport measurements of EG on Si reported so far.

Substrate	**Growth process**	**Charge carrier type, n/p**	**Sheet carrier con., n (cm^{-2})**	**Mobility, μ (cm^2/Vs)**	**Sheet resis., Rsh (Ω/□)**	**Transport property measurement technique**	**Ref**
SiC(111)/n-Si(111)	Thermal decom.	n	$1.8x10^{13}$	-	-	ARPES	148
1. SiC(111)/p-Si(111) 2. SiC(111)/p-Si(110)	Thermal decom.	n	-	-	1. 17 k 2. 90 k	TLM Top-gate FET	143
SiC(111)/Si(111)	Thermal decom.	1. n 2. n/p	$6x10^{11}$	1. 950 2. 175 (n) 2. 285(h)	1. 6 k	1. Hall Lehighton 2. FET	145
SiC(111)/n-Si(111)	Thermal decom.	n	$4x10^{13}$	-	-	Raman G peak blue shift ($16cm^{-1}$)	89
SiC(100)/Si(100) SiC(111)/Si(111)	Thermal decom.		-		3.5k – 50k	Hg probe and c-TLM	149
SiC(111)/p-Si(111)	Thermal decom.	n	No reports on transport properties			ARPES	142
Ge(100)/Si(100)	1.CVD 2.MBE	p	$2.3x10^{12}$ 1. $\sim10^{13}$ 2. $\sim10^{12}$	1. ~600 2. ~1200		E_F = 0.185 eV from ARPES STM on FET configurations	147
H-Ge(110)/Si(110)	CVD 1. Single cryst. 2. Polycr.		$3x10^{11}$	1. 10620 2. 2570	1. 2-5k 2. 6-12k	Back gated GFETS on SiO_2/Si	146

2.5.2 Carrier scattering mechanism in epitaxial graphene

Understanding the charge scattering mechanisms in graphene is crucial to enhance the carrier mobility and hence improve the performance. The ability to tune the carrier density of graphene has led to the exponential growth in graphene research.[11] The major scattering factors of graphene are reviewed in this section.

For a 2D conductor of width W and length L, the mean free path (l_{mfp}) is denoted as the average distance the charge carriers can travel before any scattering. If the $l_{mfp} << W, L$ which is the most usual case, then the charge transport is said to be in the diffusive regime. Within this regime, the carriers scatter randomly many times while moving across the conductor. Carriers in the diffusive region are described by the semi-classical diffusive formulas. If the l_{mfp} matches with W, L or is larger than the dimensions of the sample, then the conduction enters a ballistic transport regime.[150,151]

The Drude conductivity of graphene is;[150]

$$\sigma = ne\mu \qquad (6)$$

Where e is the charge of electron and μ is the carrier mobility. The carrier mobility can be defined for graphene in terms of the mean free path (l_{mfp}) using the formula;[152]

$$\mu = 2(e/h)\left(\frac{\sqrt{\pi}}{n}\right) l_{mfp} \qquad (7)$$

Equations (1) and (2) suggest that at very low carrier densities when the mean free path is finite, the conductivity goes to zero and the mobility to infinity. Due to the massless nature of carriers in graphene, theory shows that the minimum conductivity for both ballistic and diffusive cases is $4e^2/h$.

At high carrier densities, the conductivity is limited by short-range scatterers to a value, ρ_s^{-1}. Therefore, the equation for the conductivity of graphene is given by;

$$\sigma = \left(\frac{1}{ne\mu + \sigma_0} + \rho_s\right)^{-1} \qquad (8)$$

Within the diffusive region, which is the most common regime of graphene transport when the graphene is grown on a supporting substrate like bulk SiC, the charge carriers in graphene are generally scattered due to four main factors: 1) acoustic phonons, 2) surface optic phonons, 3) short-range scattering and 4) Coulomb scattering.[153]

The first two processes are thermally activated, and the effects are negligible at low temperatures. Short-range scattering and Coulomb scattering are caused by the structural defects and charged impurities, respectively[153] and these govern the dependence of n over μ at low temperatures. In monolayer graphene, at a higher order of carrier concentration (>10^{12} cm^{-2}), the mobility is limited by the short-range scattering and it depends on n as n^{-1}. At lower carrier density, the Coulomb scattering dominates and the mobility is independent of n. The decreasing μ with increasing n is explained due to the short-range scattering. In addition, short-range scattering also results in conductivity independent of carrier density.[153]

Hwang et al. [62] established that at the higher carrier density regime, where carrier density is larger than impurity density, 2D graphene transport is dominated by impurity (Coulomb) scattering, and can be theoretically described by a microscopic Drude-Boltzmann model, in which the dominant source of scattering is the charged impurities in the substrate. This work has also reported that the Fermi temperature of graphene is ~1300 K at 10^{12} cm^{-2} and there is no temperature dependence in conductivity between 0 - 300 K due to charged impurity scattering - in agreement with experimental observation.

Chen et al.[23] demonstrated the effects of phonons on a substrate-supported graphene using a SiO_2 substrate. They reported that within the diffusive regime, resistivity of graphene rises linearly with temperature at low temperature, with no carrier density dependence, for acoustic phonon scattering. At temperatures above ~200K, resistivity becomes carrier density-dependent if the scattering is due to polar optical phonons (dominant limiter) of the substrate.

2.6 Summary

This chapter summarizes various graphene growth techniques such as mechanical exfoliation, CVD on metals and dielectrics, thermal decomposition of SiC, thermal decomposition of 3C-SiC and the respective transport properties reported so far. Thermal decomposition of bulk SiC seems to be the most promising growth technique in terms of graphene quality, control of the transport properties, the uniformity of coverage and its ability to grow directly on semiconducting substrates and therefore is highly appealing for future electronic devices including high-frequency transistors and digital switches. An extraordinary work has been performed in the area of tuning and controlling the properties of graphene grown on bulk SiC over the last decade.

Bulk SiC wafers not widely available in large areas, and are not compatible with the existing silicon technologies. Graphene on silicon technology is interesting for a large range of electronic, photonic, energy storage and sensing applications due to its possibility for low cost and large-area production of graphene with current silicon technology compatibility.

Major progress has been made in the area of graphene synthesis on bulk SiC and the establishment of its transport characteristics; however, equivalent progress using silicon as the substrate is still not fully demonstrated.

A few attempts have been made to measure the transport properties of graphene produced by thermal decomposition of 3C-SiC/Si, however, the measurements, in this case, were made mainly using the FET configurations at room temperature. FET measurements are known to be electrostatics and geometry dependent and are largely affected by the substrate. Besides, it does not provide information regarding the carrier scattering mechanisms involved in the electrical conduction. Temperature-dependent carrier transport study is required for a complete understanding of carrier transport mechanism in the graphene. The literature review chapter clearly indicates that no previous low-temperature transport measurements have been performed on graphene grown on 3C-SiC/Si. This is a major literature gap for the establishment of graphene on silicon technology.

3C-SiC/Si as a substrate for graphene also possesses significant electrical limitations due to large amounts of stress and defects generated during the heteroepitaxial growth. No prior attempts reported this issue or addressed the relevant consequences of 3C-SiC/Si on the electrical conduction of graphene.

Therefore, the main research questions derived from the literature review are;

1. What are the electrical limitations of heteroepitaxial 3C-SiC/Si and what are the consequences in 3C-SiC/Si using as a substrate for graphene growth?
2. What causes the origin of the 3C-SiC/Si limitations and how can we overcome that?
3. After addressing questions 1 and 2, what are room temperature and low-temperature transport properties of graphene synthesized on 3C-SiC/Si?

All of these questions are addressed and answered in Chapters 4, 5 and 6.

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Chapter 3: Methodology

3.1 Substrate material – heteroepitaxial 3C-SiC/Si

In this work, we used the unintentionally doped commercial 3C-SiC films (typically n-type), heteroepitaxial grown at different growth conditions on (100) or (111) crystalline oriented 6" or 4" lowly p-doped silicon (resistivity 1-10 Ωcm) as well as on the 2" highly resistive silicon (resistivity >10 kΩcm). For characterisations, the 3C-SiC/Si films were diced into 1.1x1.1cm^2 coupons. Table 3-1 shows a summary of all types of heteroepitaxial 3C-SiC films used in this work.

Table 3-1 Summary of all the samples used in this work

Samples	Supplier	Si resistivity (Ωcm)	Si thickness (µm)	SiC thickness (µm)
SiC/p-Si	NOVASiC	1-10	527 (on-axis)	0.5
SiC/highly-resistive Si	NOVASiC	>10k	235 (on-axis)	0.5
SiC/p-Si	IMEM-CNR	1-5m	279 ± 25 (on-axis)	0.5
SiC/p-Si	IMEM-CNR	1-5m	279 ± 25 (on-axis)	5.0
SiC/p-Si	IMEM-CNR	1-5m	279 ± 25 (6° off-axis (110))	5.0
SiC/p-Si	Griffith U	1-10	680 ± 25 (on-axis)	0.25

3C-SiC samples grown at different conditions on the doped silicon as well as the high-resistivity Si have been used for understanding the electrical properties of 3C-SiC – see chapters 4 and 5.

Investigation of charge transport characteristics of EG in this work has been performed on EG synthesised on heteroepitaxial 3C-SiC that is grown on highly resistive Si substrates from NOVASiC. This is to reduce the substantial amount of parallel conduction associated with the 3C-SiC grown on doped Si substrates.

3.2 Graphene synthesis

Alloy-mediated epitaxial graphene growth

Figure 3-1 shows the novel process of graphitisation adopted in our research group as reported in Iacopi et al.[1] Note that the epitaxial SiC thin films on Si is used as the solid-phase carbon source. The four main steps involved in the graphitisation process are as follows;

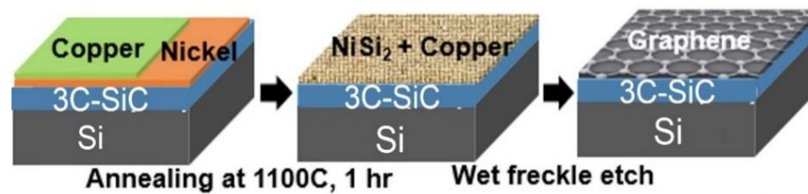

Figure 3-1: Schematics showing the alloy mediated graphitization of 3C-SiC/Si[1]

Sputtering of the metal catalysts

Samples were first cleaned using Acetone and Iso Propyl Alcohol and dried in N_2. After cleaning, the samples were loaded in a DC magnetron-sputtering chamber to sputter Ni and Cu. 10 nm of Ni was deposited on the samples first, followed by copper of 20 nm.[1]

Annealing

The alloy-mediated graphitisation was performed in a Carbolyte high-temperature furnace. The samples were annealed at 1100 °C for ~1 hour at a pressure of $\sim 10^{-5}$ hPa. After annealing, the samples are left to cool to room temperature under vacuum. This method utilises slow ramp rates: a heating rate of ~25 °C/min, and a cooling rate of ~2 °C/min.[1]

Wet freckle etch in acid solution

The annealing step results in the reaction of Ni with the Si in the SiC, which forms the silicides, particularly the Ni_2Si, intermixed with metals, and releases the carbon that precipitates upon cooling. This intermixed metal silicide and metal layer is removed by performing a wet freckle etch using an acid mixture given by 85% Phosphoric acid (H_3PO_4): Glacial acetic acid (CH_3COOH): 70% Nitric acid (HNO_3): 48% Tetraflouroboric Acid (HBF_4): H_2O in the ratio of 70:10:5:5:10. The freckle etch is completed when the samples were finally rinsed with milli-Q water and dried by nitrogen.

Once the samples are synthesized, the four-point van der Pauw contacts are made by soldering InSn.

3.3 Electrical characterisation

3.3.1 Hall Effect Measurement

Hall effect measurement is the method for measuring carrier concentration in small, conductive, uniform materials by examining Hall voltages across them in an applied magnetic field of known magnitude. The phenomenon was named for Edwin Hall, who discovered the effect in 1879.[2]

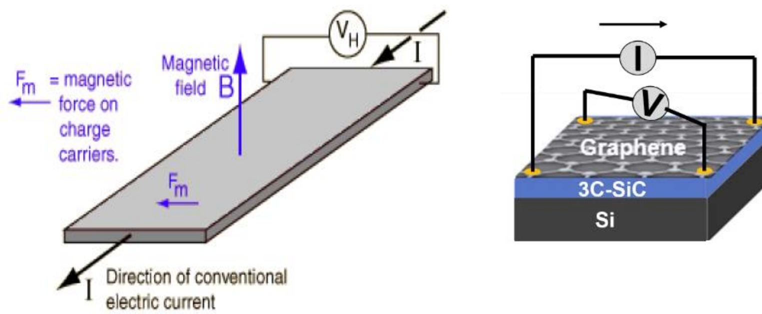

Figure 3-2: a) Schematics of Hall effect phenomenon[2] b) van der Pauw contacts on Graphene/3C-SiC showing the Hall effect measurement configuration.

The measurement involves sweeping a range of current at a perpendicular uniform magnetic field of 0.52 T and measuring the Hall voltage across the metal contacts of the sample. By applying a current of I Amps and perpendicular uniform magnetic field of magnitude B to a sample, as in Figure 3-2 the resulting **Lorentz magnetic force** in the direction, $\mathbf{F_m}$ enacted on particles of velocity $\mathbf{v_p}$, under electric field **E**, in which the q of 1.602×10^{-19} C is given by; [2]

$$\mathbf{F_m} = q\,(\,\mathbf{E} + \mathbf{v_p}\mathbf{B}) \qquad (1)$$

Hall voltage for positive magnetic field V_{HP} will appear transverse to the current, measured with the upper terminal in the direction of $\mathbf{F_m}$, of magnitude as defined by:

$$V_{HP} = I\mathbf{B}/nq \qquad (2)$$

This Hall voltage measurement, however, assumes uniform conductivity in the subject material. To remove the need for this, the magnetic field can be reversed and the Hall voltage measurement re-taken and used to calculate an overall Hall voltage:

$$V_H = (V_{HP} - V_{HN})/2 \quad (3)$$

From the Hall voltage, the carrier concentration can be calculated using the expression:

$$n = \frac{IB}{VHqt} \quad (4)$$

V_H, q (1.602×10^{-19} C), I (current), **B** (magnetic field) are known and hence the carrier concentration, n can be obtained.

If the thickness of the sample is known, it can be included in equation 4 to estimate the bulk carrier concentration in cm^{-3}. Note that for the 2-dimensional materials like graphene that has only conduction in two axes (only in X and Y), the thickness is eliminated, and hence the sheet carrier concentration is given in the units of cm^{-2}. The polarity of the carrier concentration indicates the type of charge carriers within the graphene (n for electrons and p for holes).[2]

3.3.2 van der Pauw sheet resistance measurement

The sheet resistance measurement technique also includes the van der Pauw in which a known range of current is passed along one side of the sample, and the voltage is measured equidistant and parallel to it as shown in Figure 3-3.[3]

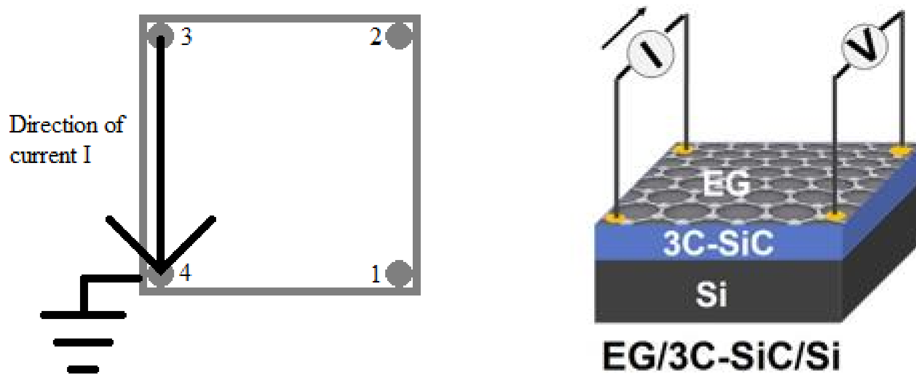

Figure 3- 3: Schematics of a) van der Pauw sheet resistance measurement[3]; b) test structure of graphene on 3C-SiC for the sheet resistance measurement configuration.

The sheet resistance is calculated using the equation:

$$R_{sh} = \frac{\pi}{\ln(2)} \frac{V2 - V1}{I} \quad (5)$$

Since the distance between the contacts is uniform, the units for this measurement are Ω/□. From the values of carrier concentration and the sheet resistance, the mobility of the charge carriers in the sample can be calculated using equation 6:

$$\mu = \frac{1}{qRsn} \qquad (6)$$

3.3.3 Temperature-dependent sheet resistance measurements

Temperature-dependent sheet resistance measurements were performed using 2 setups; one setup at UTS, where is an Ecopia Hall effect measurement system is used to measure the Hall effect properties between the temperature range of 300 K down to 77 K (liquid nitrogen temperature). The second one for the low-temperature Hall effect measurements was Michael Fuhrer's Quantum Design PPMS set up at Monash University.

3.3.4 Transfer Length Method (TLM) structures on 3C-SiC/Si

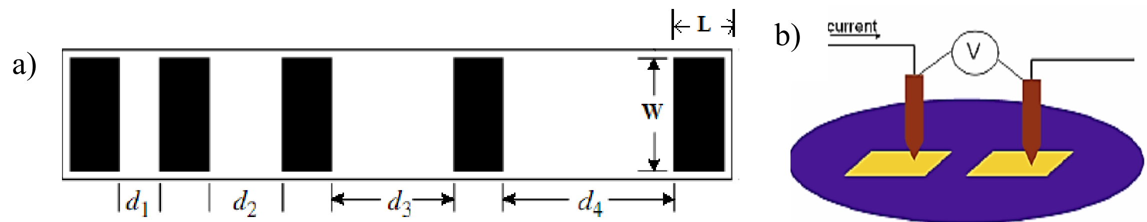

Figure 3-4: a) TLM structure, b) I-V measurement on TLM structure

The Transfer Length Method (TLM) was first introduced by Shockley[4] and independently investigated by Murmann and Widmann[5] and further advanced by Berger et al.[6] The transfer length model uses a variable spacing between the metal pads on the test structure as demonstrated in Figure 3-4a.

In this method, the I-V measurements are performed between the adjacent metal contacts. A linear array of metal pads of width 'W' and length 'L' are fabricated with variable distance' between them.[7] Parameter analyzer and a set of probes are used to sweep current between each set of contacts and measure the corresponding voltage drop between them to give the total resistance (see, Figure 3-4b). The values of total resistances, R = V/I is expected to be linear with the distances between the contacts, d. The total resistance measured as a function of gap spacing d is as given in Figure 3-5. The slope of the graph determines the sheet resistance, R_{sh}.

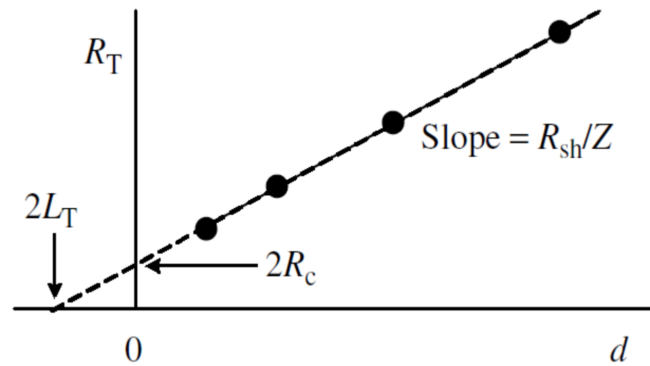

Figure 3- 5: Total resistance across the different contact spacing[7]

Finding a straight fit to the curve obtains the line equation:

$$R_T = \frac{\text{Rsh}}{\text{Z}} d + 2R_c \quad (7)$$

From the values of the slope, the width of the contacts (Z or W) and the y-intercept ($2R_c$) of the graph, we can estimate the value of R_{sh}. R_c is the contact resistance.

3.3.4.1 Test Structure

The schematic of the TLM test structure for measuring the 2-probe resistance between the silicon carbide and silicon (leakage resistance) is shown in Figure 3-6. The test structure was patterned using the lithography.

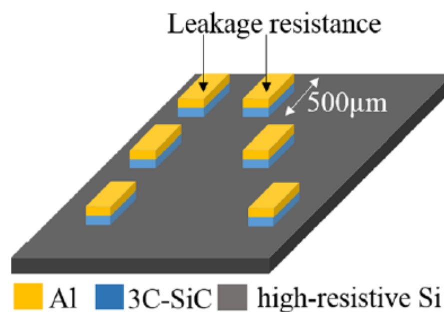

Figure 3-6: TLM structures on 3C-SiC/Si. Width of the contacts are 500 µm

3.3.4.2 Lithography steps

We deposited 300 nm thick and 500 µm wide aluminium contacts using the e-beam evaporation method (not annealed). After the metal deposition, the contacts were patterned on top of silicon carbide using a chromium metal mask via the photolithography. After that, the metal was etched by performing acid etching of aluminium, followed by the reactive ion etching of SiC. Current-voltage at room

temperature using an HP4145B semiconductor parameter analyzer measured the leakage resistances. Subsequently, the silicon in between the SiC pillars for both the van der Pauw and TLM structures of SiC on high-resistivity Si was subsequently etched using ICP and the I-V measurements were repeated.

3.4 Instrument specifications

3.4.1 Hall effect measurement

The four-point probe setup contains four thin collinear brass probes that are used to measure the sample under test. The specifications of the instrument used to perform are detailed below.

- Model & make: Ecopia HMS-5300 Hall effect Measurement System
- Temperature control unit: AMP55T (80-300 K)
- Sweeping current: 1-10 μA
- Data analysis software: HMS5000 (installed in PC)

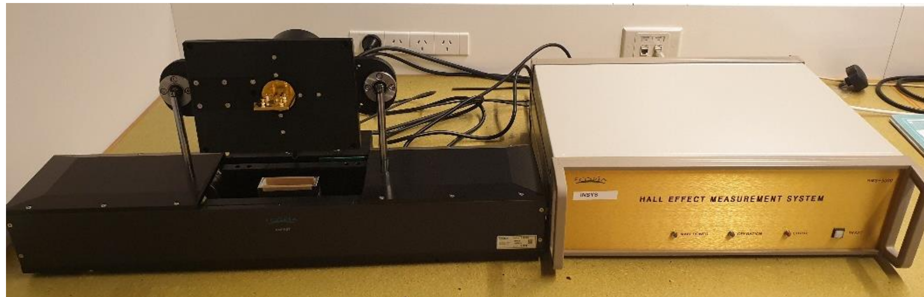

Figure 3-7: Ecopia HMS-5300 Hall effect Measurement System with AMP55T

3.4.2 TLM leakage resistance measurements on 3C-SiC/Si structures

The leakage resistance measurements were performed using an HP4145B semiconductor parameter analyser connected to the probe station.

Figure 3-8: HP 4145B Semiconductor Parameter Analyzer (left) and the probe station (right)

Structural characterisation of 3C-SiC/Si

3.4.3 Transmission Electron Microscopy

High-resolution transmission electron microscopy (HRTEM) was executed to characterize the SiC/Si interface of the as-grown and the annealed SiC(100) and SiC(111) samples using an FEI Tecnai F30 system operating at 200 keV in bright-field mode.[8] Sample foils were prepared using Focused Ion Beam (FIB) lift-out technique using a FEI Strata DB235 FIB/SEM with a Ga^+ ion source. The foils were excavated from the bulk samples and thinned to ~500 nm. Afterwards, Ar^+ ion milling was performed in a Fiscione NanoMillTM to remove Ga^+ ion damages.[8]A 2 μm thick Pt/Au protective layer was deposited on the samples before FIB milling.[8]

3.4.4 Scanning Electron Microscopy (SEM)

We used a Zeiss Supra 55VP high-resolution field-emission scanning electron microscope (FESEM) operating at acceleration voltages between 5-10 kV. Energy Dispersive X-Ray Analysis was performed by tilting the samples and at an acceleration voltage of 5 kV.

3.4.5 Stress measurements

Wafer curvature method is used to measure the biaxial stress. We used a Tencor Flexus 2320 system to measure the wafer curvature of the Si substrate and the substrate-film composite at room temperature.[9] The residual in-plane stress for the SiC film was estimated using the modified Stoney's equation, with appropriate elastic moduli (E). From the residual stress values, the absolute stress difference (MPa) between them was assessed.[8]

3.4.6 Sentaurus simulations

We performed simulations to model the leakage phenomenon and its influence on the electrical conduction using the Synopsys Sentaurus Device^{TM} TCAD simulator for the 3C-SiC on low-doped silicon. The software access was supported by the Australian National Fabrication Facility Design House Virtual Lab.

Surface characterisation of graphene

3.4.7 Raman spectroscopy

Confocal Raman mapping is performed at room temperature in a backscattering geometry using a Renishaw InVia spectrometer operating at 532 nm laser (argon–ion) using 50X objective with a spot size of approximately 1 µm (power: 50%, (34.3/2 = 17.15mW). For calibration, we used a silicon sample as reference (~520 cm^{-1}). In order to improve the statistical accuracy, 30 µm × 30 µm area is mapped using a 0.20 µm step size, and 0.1 s integration time at the centre of each sample. The D, G and 2D bands in the Raman spectrum of the graphene layers are monitored and the intensity ratio of the D- and G-bands (ID/IG) was calculated. D peak is active only when the graphene lattice symmetry is broken and its presence indicate structural defects such as point defects and edges. The G peak is an in-plane vibrational mode involving the sp^2 hybridized carbon atoms comprising the graphene sheet.[10] The intensity ratio of Raman D and G peaks (I_D/I_G) helps to estimate the number of defects in the graphene; where a higher ratio depicts a defective graphene. From the ID/IG ratio and the laser wavelength (λ), the graphene grain size (L_a)[11] can be estimated as:

$$L_a = (2.4 \times 10^{-10})\ \lambda_l^4 \left(\frac{ID}{IG}\right)^{-1} \qquad (8)$$

3.4.8 X-ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS) measurements were performed using a Specs PHOIBOS 100 Analyser operated with a Mg Kα X-ray source (Mg anode operated at 10 keV and 10 mA). The data was calibrated to the adventitious C1s peak present at 284.6 eV to compensate for any surface charging. For quantitative XPS analysis, the areas of the photoelectron peaks are calculated after Shirley background correction. Gauss-type profiles with CasaXPS software enforce peak fitting

3.4.9 Density Functional Theory (DFT)

The DFT calculations were performed using the Quantum Espresso package.[12] At least 8 Å of vacuum space was included to decouple the structure from its periodic image. Hartwigsen-Goedecker-Hutter norm-conserving pseudopotentials were used for the exchange and correlation functional with 45 Ry energy cut-off for the plane-wave basis expansion.[13] A 12 x 12 x 1 Monkhorst Pack grid was used to sample the Brillouin zone.

Generalized Gradient Approximation of Perdew-Burke-Ernzerhof (GGA-PBE) were used for the exchange and correlation functional. van der Waals interactions were included for the GGA exchange and correlation functional using an empirical potential was added to the regular density functional energy as proposed by Grimme et al.[14], implemented in the QE package.

3.5 Summary

We have first studied the 3C-SiC/Si substrate material used in this research we investigated the heterointerface instability of 3C-SiC/Si, an electrical leakage in the substrate system and its effect on the electrical conduction of the 3C-SiC. This is followed by modelling the system and studying the conduction in 3C-SiC/Si prepared under different conditions to explain the occurrence of interface issues and electrical phenomena. We utilised characterisation techniques such as Hall effect measurements, temperature-dependent sheet resistance measurements (5 – 300 K), TLM leakage measurements, stress measurements, TEM and SEM for this purpose.

After clarification of the conduction occurring in the substrate system, we study the transport properties of graphene synthesised on top of an alloy-mediated approach using Ni and Cu catalysts. With the help of Hall effect measurements, temperature-dependent sheet resistance measurements (5 – 300 K), Raman spectroscopy, X-ray photoelectron spectroscopy (XPS) and DFT calculations, we investigated charge transport properties of the graphene and the 3C-SiC/Si substrate by performing van der Pauw measurements on the samples.

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Chapter 4: Electrical degradation of the heterointerface of epitaxial silicon carbide on silicon

Before investigating the charge transport properties of graphene grown on 3C-SiC/Si, it is crucial to have the knowledge of the charge transport behaviour of the 3C-SiC/Si substrate itself on which the graphene is epitaxially grown. Chapter 4 identifies an interface degradation issue of the p-n junction in between the 3C-SiC and the Si at higher temperatures. The p-n junction failure results in a huge amount of electrical leakage in the 3C-SiC/Si system where the charge carriers within the Si dominate the conduction in 3C-SiC. This finding has consequences on the application of 3C-SiC/Si as a substrate for the graphene.

STATEMENT OF CONTRIBUTION TO CO-AUTHORED PUBLISHED PAPER

Chapter 4 is in the form of a published article. The details of the paper including the co-authors are;

Catastrophic degradation of the interface of epitaxial silicon carbide on silicon at high temperatures, *Applied Physics Letters* 109, 011604 (2016)
http://dx.doi.org/10.1063/1.4955453

Aiswarya Pradeepkumar, Neeraj Mishra, Atieh Ranjbar Kermany, John J. Boeckl, Jack Hellerstedt, Michael S. Fuhrer, and Francesca Iacopi

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Contributions of the first author: Design of experiments, sample preparation, room temp. Hall effect measurements, data analyses and interpretation, literature review, manuscript preparation.

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Contribution: TEM measurements

Sign ____________________ Date ____________________

Name: Dr Atieh Ranjbar Kermany

Contribution: Residual stress measurements

Sign ____________________ Date ____________________

Name: Dr John J. Boeckl

Contribution: TEM measurements

Sign ______________________ Date ______________________

Name: Dr Jack Hellerstedt

Contributions: Low-temp. (4K – 300K) sheet resistance measurements, scientific discussions

Sign ______________________ Date ______________________

Name: Prof. Michael S. Fuhrer

Contributions: Low-temp. (4K – 300K) sheet resistance measurements, scientific discussions

Sign ______________________ Date ______________________

Name: Prof. Francesca Iacopi

Contributions: Research supervision, coordination of collaboration, critical manuscript revision

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4.1 Abstract

Epitaxial cubic silicon carbide on silicon is of high potential technological relevance for the integration of a wide range of applications and materials with silicon technologies, such as microelectromechanical systems, wide-bandgap electronics, and graphene. The hetero-epitaxial system engenders mechanical stresses at least up to a GPa, pressures making it extremely challenging to maintain the integrity of the silicon carbide/silicon interface. In this work, we investigate the stability of said interface and we find that high-temperature annealing leads to a loss of integrity. High–resolution transmission electron microscopy analysis shows a morphologically degraded SiC/Si interface, while mechanical stress measurements indicate considerable relaxation of the interfacial stress. From an electrical point of view, the diode behaviour of the initial p-Si/n-SiC junction is catastrophically lost due to considerable inter-diffusion of atoms and charges across the interface upon annealing. Temperature-dependent transport measurements confirm a severe electrical shorting of the epitaxial silicon carbide to the underlying substrate, indicating the vast predominance of the silicon carriers in lateral transport above 25 K. This finding has crucial consequences on the integration of epitaxial silicon carbide on silicon and its potential applications. Epitaxial cubic silicon carbide (SiC) films on silicon attract extensive interest in many semiconductor device applications such as high-voltage, high-frequency diodes, heterojunction bipolar transistors and microelectromechanical systems (MEMS).[1-2] This is because it offers access to the electrical and mechanical properties of the SiC material such as wide bandgap, high thermal conductivity, chemical stability, in addition to a large tuneable tensile stress.[1, 3] However, the large lattice and thermal mismatches between the SiC film and silicon result in a high density of defects[4] and a sharp residual stress gradient at the SiC/Si interface.[5] Consequently, non-ideal diode characteristics have been observed for the common n-SiC/p-Si electronic junction, which poses concerns for the reliability of the 3C-SiC devices.[1, 4, 6-9]

4.2 Introduction

Tanner et al. have characterized the as-grown n-3C-SiC/p-Si hetero-junctions and have demonstrated a strong interface with reverse bias breakdown voltages exceeding 200V, and +/-1V rectification ratio of 200,000 at room temperature.[1] However, the stability of the interface at higher temperatures, which is relevant for the synthesis of graphene on

3C-SiC/Si[10], GaN on SiC/Si[11] and for harsh –environment applications of the SiC/Si[12] has not yet been investigated to-date.

In this work, we evaluate the stability of the SiC/Si hetero-junction at high temperatures by performing stress, electronic transport measurements and high –resolution microscopy of the SiC/Si interface. We show that high temperatures have catastrophic consequences on the SiC/Si junction.

4.3 Methodologies

Unintentionally *n*-type doped epitaxial 3C-SiC films with thickness of 250 nm were grown in-house at 1000°C on low-doped 6" wafers of *p*-type Si(100) and Si(111) with thickness of 680±25 μm in a hot-wall horizontal Low-Pressure Chemical Vapour Deposition (LPCVD) system using an alternate supply of SiH_4 and carbon source gas, described in previous reports.[4, 13] The carbonisation was performed at 950°C using C_2H_2.

For the electrical characterization, SiC/Si wafers were diced into 1x1cm^2 fragments. For measurements with setup 1 (Griffith University), 150 nm nickel contacts were sputtered on the four corners of the aforementioned samples. Electrical properties such as the carrier concentration, carrier mobility and sheet resistance were estimated at room temperature by performing Hall measurements in a van der Pauw configuration on the as-grown SiC(100) films, with electrical probes directly connected with the metal contacts and sweeping the DC input current of 0 to 10mA using a HP4145B semiconductor parameter analyser.[10] Analogous SiC(100) films were annealed at 1100°C using a Carbolite High-Temperature Furnace at 10^{-4} mbar for 1 hour, and the electrical measurements were repeated at room temperature on the annealed SiC films. Complementary measurements were also carried out on the 1x1 cm^2 fragments of the bare silicon substrate. Additionally, equivalent electrical measurements at room temperature were performed on 1x1 cm^2 fragments of commercially available, unintentionally *n*-type doped NOVASiC SiC(100) grown at 1350°C after a carbonisation step at 1100°C [14].

Temperature-dependent transport measurements of the as-grown and the annealed in-house SiC(100) films were performed with a Quantum Design PPMS (subsequently referred to as "setup 2"). 1x1cm^2 fragments of SiC wafers with (5/50nm) Ti/Au contacts on the four corners in the van der Pauw geometry were used. In instances of poor wire bond adhesion, silver epoxy was used to make electrical connections to the samples. Two

probe current-voltage curves were measured to ensure ohmic contact. The measurements were carried out as a function of temperature in the range between 5K and 300K. Hall carrier density values were measured by sweeping the magnetic field +/- 0.1T, symmetrizing the measured R_{xy} response, and fitting the linear slope to extract the carrier density. Temperature-dependent resistivity is used to estimate the ionization energy of dopants in the samples (see below). High-resolution transmission electron microscopy (HRTEM) was performed to characterize the SiC/Si interface of the as-grown and the annealed SiC(100) and SiC(111) films using a FEI Tecnai F30 system operating at 200keV.[4] Sample foils for transmission electron microscopy were prepared via a focused ion beam (FIB) lift-out technique using a FEI Strata DB235 FIB/SEM with a Ga+ ion source. The foils were excavated from the bulk samples and thinned to about 500 nm. Subsequently, Ar+ ion milling was conducted in a Fiscione NanoMill™ to remove Ga+ ion damage. A 2 µm thick Pt/Au protective layer was deposited on the samples prior to FIB milling.

We also conducted a residual in-plane stress analysis on the as-grown and annealed in-house SiC films via full wafer curvature measurement. 3C-SiC(100) and 3C-SiC(111) films grown with different thicknesses on full 6" silicon wafers were used for the study. A Tencor Flexus 2320 system was used for measuring the wafer curvature of the Si substrate and the substrate-film composite at room temperature.[4] The residual in-plane stress for the SiC film was calculated using the modified Stoney's equation with appropriate elastic moduli (E) and Poisson's ratios (ν) values: 130 GPa and 170 GPa, 0.28 and 0.26 for Si(100) and Si(111) respectively.[4-5] After that, the as-grown films were subjected to thermal annealing in N_2 at different temperatures of 1100°C, 1180°C and 1250°C for two hours. This was done in a Hi-Tech Furnace Systems (UK) LPCVD system at sub-atmospheric pressure of 10-1000Pa.[5] From the residual stress values of the as-grown and the annealed film, the absolute stress difference (MPa) between them was assessed.

4.4 Results and discussion

Table 4-1 Electrical characteristics measured at room temperature for in-house SiC/Si(100) samples as-grown and after annealing at 1100°C (data acquired with setup 1).

	As-grown	**Annealed**
Carrier type	Electrons	Holes
Sheet carrier concentration, n_s (cm^{-2})	$3.3(\pm0.2)x10^{14}$	$9.5(\pm0.2)x10^{14}$
Mobility, μ_s (cm^2/Vs)	14(±10)	273(±10)
Sheet resistance, R_s (Ω/□)	1354±1	24±1

Table 4-1 shows the room temperature van der Pauw measurement results of the as-grown and the annealed SiC(100) samples obtained with setup 1. The as-grown SiC(100) indicates *n*-type conduction with sheet carrier concentration (n_s), carrier mobility (μ_s), and sheet resistance (R_s) of $3.3(\pm0.2)x10^{14}$ cm^{-2}, 14(±10) cm^2/Vs and 1354±1 Ω/□ respectively.

Upon annealing, the sample shows an abrupt switch to *p*-type conduction with a n_s ~3 times larger than that of the as-grown sample. In addition, the mobility increases significantly from 14 cm^2/Vs to 273 cm^2/Vs, accompanied by a drastic decrease of the R_s of the sample down to 24 Ω/□. These room-temperature values are in good agreement with those obtained from setup 2, at Monash University.

Complementary room temperature measurements of the bare silicon substrate, indicate p-type conduction with a sheet carrier concentration of ~ $9x10^{13}$ cm^{-2}, from which a bulk carrier concentration of ~ $1.3x10^{15}$ cm^{-3} is estimated, and a mobility of ~341 cm^2/ Vs.

We thus hypothesize that the switch to p-type carriers, increase of mobility and drop of sheet resistance are due to a shorting of the SiC film to the substrate upon annealing with consequent dominance of the carriers in the thick silicon substrate, with relatively high mobility. If we considered the annealed SiC sample in Table 4-1 as an electrically shorted substrate plus film composite, we would estimate a bulk sheet carrier concentration of $1.5x10^{16}$ cm^{-3}. This is an order of magnitude higher than the bulk carrier concentration directly measured on the silicon substrate, which is plausible as a result of the combined carrier contributions from both silicon substrate and the silicon carbide[15].

Further corroborating this hypothesis, the as-grown unintentionally doped (thus *n-type*) commercial NovaSiC SiC films on p-type Si(100) show the unexpected *p-type* conduction

already when measured at room temperature, with n_s, μ_s, and R_s of $1x10^{14}$ cm^{-2}, $272cm^2/Vs$ and 180Ω/□ respectively. When grown on n-type substrates instead, these films always show n-type conduction. This indicates thus that the transport characteristics of the commercial samples may be dominated by the substrate already as-grown. Note that such samples are grown at a much higher temperature of 1350°C.[14]

Low-temperature transport measurements were performed onto the SiC films grown in-house for a more detailed analysis. Figure 4-1 illustrates the low-temperature behaviour of the sheet resistance of the as-grown and the annealed SiC(100) as a function of temperature in the range between 5K and 300K. The sheet resistance of the as-grown SiC film decreases monotonically with temperature. From basic solid-state theory, the resistivity of a semiconductor versus temperature would decrease according to an Arrhenius type behaviour[16-17] such as:

$$\rho \propto T^{3/2} \exp\left(\frac{E_a}{2k_{\mathbf{B}}T}\right) \quad (1)$$

where ρ is the resistivity, k_B is the Boltzmann constant, T is the absolute temperature and E_a is the activation energy of the semiconductor. In particular, for k_BT far below the bandgap of the semiconductor, the activation energy dominating the resistivity behaviour is the donor (for *n*-type) or acceptor (for *p*-type) energy level for the specific dopant.

In hetero-epitaxial SiC on silicon, it is notoriously hard to identify a specific dopant level as the resistivity is affected by a combination of different unintentional defects, including N incorporation.[18] Indeed, by fitting the as-grown SiC resistance behaviour, we confirmed the presence of different donor contributions with energy levels approximately varying from 2meV to 52meV (extracted using equation 1) over the studied temperature range as reported in other literature.[18]

On the other hand, the annealed SiC(100) indicates a more complex behaviour within the same temperature range. For temperatures below ~25K (zone I) its behaviour matches with that of the as-grown SiC, including the presence of a majority of *n*-type carriers. However, just above ~25K, a change in majority carriers to *p*-type is observed, concomitant with a sharp decrease of sheet resistance of several orders of magnitude (zone II). In zone II, this sample shows the typical decreasing resistance behaviour versus temperature expected for a semiconductor with different donor/acceptor characteristics. Above ~150-200K (zone III), the annealed sample shows an increase in resistivity,

associated with a predominance of phonon scattering, while continuing to exhibit prevalent *p*-type conduction.

Figure 4-2 shows the fitted resistivity for the annealed SiC as a function of temperature in the range from 30K to 100K (zone II), with slope = 0.11. The extracted acceptor energy level using equation 1 is about 44meV which is in-line with the boron acceptor energy level in silicon (46meV).[19] Note that this was calculated through an approximated expression of eq. (1) where the power dependence of the temperature was neglected, which is an adequate approximation for low temperatures.

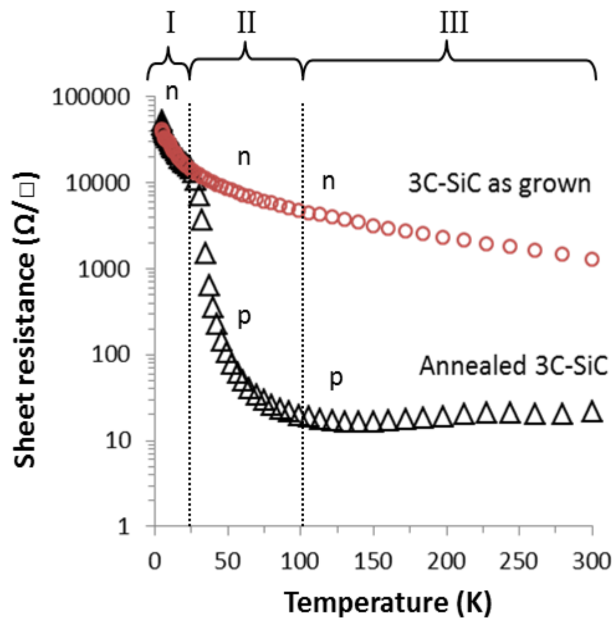

Figure 4-1: Sheet resistance of the 250nm thick as-grown SiC(100) and the vacuum annealed SiC(100) at 1100°C for 1 hour as a function of temperature in the range between 5K and 300K.

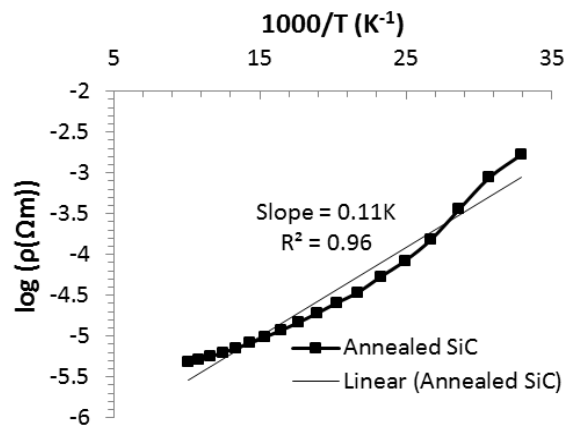

Figure 4-2: Resistivity versus temperature for the annealed SiC(100). Activation energy of 44meV is obtained by fitting the data over 30K to 100K (zone II).

The data in Figure. 4-1 indicate that while the resistivity of the as-grown SiC/Si(100) matches what is expected for an *n*-type 3C-SiC semiconductor film, the behaviour of the annealed SiC/Si(100) matches with that of 3C-SiC only for temperatures below 25K. Above 25K, (zone II) the resistance behaviour closely resembles the one expected from silicon (see the extracted energy level). The fact that above 25K the majority carrier type conduction switches abruptly from *n*- to *p*- type is a further strong indication that the silicon substrate dominates the conduction in the annealed SiC/Si in zone II and III, including room temperature. This all would indeed point to a system in which the conduction of the thin film SiC and that of the silicon substrate are highly intermixed, appearing electrically shorted. The *p*-type conduction within the thick silicon substrate clearly dominates until between 50K and 25K where a substantial freeze- out of the boron dopants in the silicon matrix is reached.[20] Note that the total number of carriers in silicon substrate and in the SiC film are comparable, but the *p*-type carriers in the silicon show much higher mobility, so they dominate the system above the B freeze-out temperature. Therefore, we find that the *n*-type conduction of the SiC film is the prevalent measured signal only below 25K.

If the carbonisation layer, which serves as sealing layer for the out-diffusion of silicon, developed substantial discontinuities, this would allow for extensive charge diffusion at the SiC/Silicon interface with consequent loss of the n-p junction.

If this were the case, the degradation of the interface would likely be accompanied by a relaxation of interfacial stress. Table 4-2 shows residual mean stress (MPa) and absolute stress differences (MPa) of SiC(100) and SiC(111) films of thickness ranging between 50nm and 1 μm, before and after annealing at different temperatures above the SiC growth temperature.

Table 4-2 Residual mean stresses (σ) for the as-grown and annealed SiC (100) and SiC(111) films and the absolute stress differences between them. The films are of different thicknesses and annealed in N_2 for 2 hours at different temperatures of 1100°C, 1180°C and 1250°C.

SiC(100)						
Sample No.	**Thickness (nm±2nm)**	**$\sigma_{as-grown}$ (MPa)**	**σ_{anneal}(MPa)**			**Absolute stress differences (MPa)**
			1100°C	**1180°C**	**1250°C**	
1	49	424		-108		532
2	49	363			-399	762
3	66	302	129			173
4	67	288		-28		315

5	67	322			-208	530
6	92	323		133		190
7	92	291			-15	306
8	270	187		147		39
9	300	305		273		31
10	348	308		297		11
11	994	151		153		-3

SiC(111)						
Sampl e No.	**Thickness (nm±2nm)**	**$\sigma_{as\text{-}grown}$ (MPa)**	**σ_{anneal}(MPa)**			**Absolute stress differences (MPa)**
			1100°C	**1180°C**	**1250°C**	
1	50	423		-462		885
2	53	616			-563	1179
3	69	856	735			121
4	70	1034	891			143
5	69	467		-120		586
6	70	840		439		401
7	71	590			-203	794
8	90	458		100		358
9	95	644			90	554
10	238	524		442		82
11	300	915		852		63
12	945	679		672		7

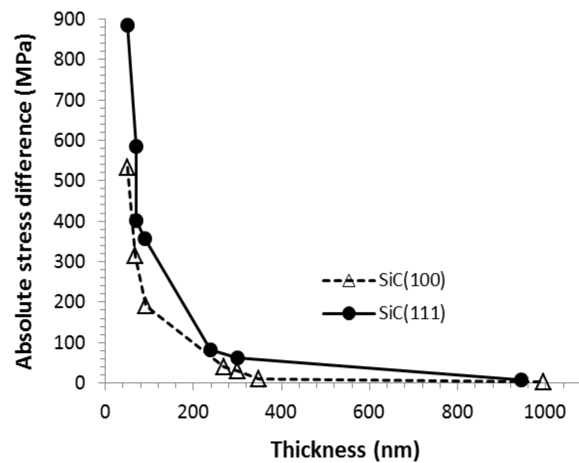

Figure 4-3: Absolute stress difference of the epitaxial SiC(100) and SiC(111) films before and after annealing at 1180°C versus film thickness. Each point represents the absolute difference of the average stress for the as-grown and the annealed films. The difference indicates in all cases a transition towards a more compressive stress state with decreasing

thickness. Note that the exponential suppression of the stress difference with increasing thickness indicates the interfacial nature of the stress change.

We have already reported[5] that the as-grown 3C-SiC films on Si show tensile mean residual stress due to the lattice and thermal mismatches. From TABLE 4-2 we can observe that, when the thin films of SiC are thermally annealed, the stresses tend to become more compressive. The extent of the transition towards a more compressive stress state upon annealing is given by the absolute stress difference (MPa) in Figure 4-3, and it appears to be strongly dependent on the film thickness. In particular, the largest difference is found for the thinnest films, for both SiC(100) and SiC(111). Note that we observed plastic stress relaxation of the substrate after annealing, leading to a change in the bare substrate wafer curvature to more convex. The values of σ_{anneal} in TABLE II were not corrected for this change so that the stress change in Figure 4-3 reflects the interface relaxation as a whole. Note also that the occurrence of plastic deformation of the silicon substrate was reported by Zielinski et al. when growing SiC at high temperatures.[21]

In addition, Table 4-2 shows that, not surprisingly, the extent of stress change also depends on the annealing temperature: higher annealing temperatures lead to a larger change. For example, the 49 nm thick SiC(100) data shown led to an absolute stress difference of 532MPa when annealed at 1180°C while annealing at 1250°C caused a larger stress difference of 762MPa. The absolute stress differences between the as-grown and annealed samples as a function of the film thickness is plotted in Figure 4-3. All the samples shown here are annealed at 1180°C in N_2 for 2 hours. These data indicate that the absolute stress differences after annealing for SiC(100) and SiC(111) are of a similar magnitude. Furthermore, the thickness dependence clearly indicates exponential suppression of the stress difference magnitude with increasing thickness, with samples on the order of 1μm showing virtually no change with annealing. The fact that the transition to more compressive stress on annealing is reduced when moving away from the interface indicates that this is an interfacial stress dominated phenomenon.

Cross-sectional transmission electron microscopy focusing on comparing the SiC/Si interface of as-grown and SiC films annealed at 1100°C should likely indicate morphological changes.

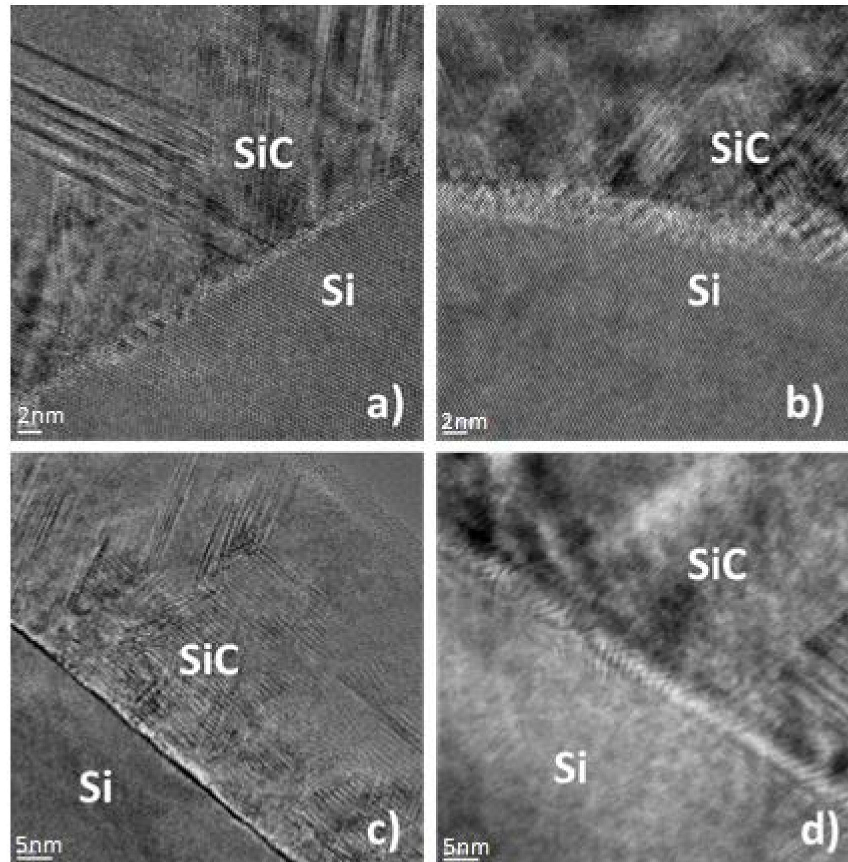

Figure 4-4: High-resolution TEM micrographs of the SiC-Si interface of the 250nm-thick SiC(100) and SiC(111) films (a) as-grown SiC(100) film (b) SiC(100) film annealed in vacuum at 1100°C, for 1 hour c) as-grown SiC(111) film d) SiC(111) film annealed in vacuum at 1100°C, for 1 hour. The SiC/Si interface of both the as-grown SiC films appear to be well-defined whereas, the interface of the annealed SiC films appears inhomogeneous.

Figure 4-4 shows that both the as-grown 3C-SiC(100) and SiC(111) films possess a very thin, well defined ~1nm thick carbonisation layer at the interface. On the other hand, it is evident that, after annealing, the SiC/Si both interfaces have degraded, appearing inhomogeneous in the TEM image.

4.5 Conclusions

This work indicates a substantial degradation of the interface as a failure *mode*, consequence of the combination of high temperatures and high stresses at the SiC/Si interface when hetero-epitaxial 3C-SiC films are grown on a thin carbonisation layer on silicon. A substantial amount of stress is relaxed at the SiC/Si interface by allowing substantial atomic inter-diffusion between the SiC and the silicon substrate. Here we indicate that the carbonization barrier can already break down at temperatures roughly

above 1000-1100°C, although the exact temperature may slightly shift depending on the carbonisation processes. This effect is so prominent that the insulating n-SiC/p-Si junction is destroyed and the layer-substrate system becomes electrically shorted to the substrate.

Such fatal failure can occur both upon film growth at high temperature (NovaSiC) and anneal at high temperature (in-house films). The detailed clarification of the failure mechanisms will be strongly dependent on the specific sample preparation. Here we indicate some possibilities. The interface layer of the in-house SiC films on silicon possesses about a GPa compressive stress.[5] That alone could lead to failure at high temperatures because of enhanced creep effects.[22] For the commercial samples, this is potentially compounded by additional compressive thermal stress[23] of the thin carbonisation layer when brought to 1350°C for the SiC growth and increased interfacial diffusion at high temperatures. The silicon out-diffusion from the silicon substrate to the silicon carbide at high temperatures in the absence of an efficient diffusion barrier is a well –know issue, [23,24] and this creep phenomenon via interface atomic diffusion was indirectly already reported earlier.[22]

This phenomenon has crucial consequences on the applications where the silicon carbide on silicon is exposed to high temperatures. In particular, this regards not only the use of SiC on silicon for harsh environments but also the use of SiC on silicon as pseudo-substrate for the growth of III-N and graphene on silicon, as those materials are currently grown at temperatures above 1000°C. Therefore, we indicate a compelling need to identify a more robust barrier at the SiC/Si interface able to insulate the silicon carbide from the silicon substrate at high temperatures.[23]

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STATEMENT OF CONTRIBUTION TO CO-AUTHORED PUBLISHED PAPER

This section of chapter 4 is in the form of a published article. The details of the paper including the co-authors are;

Response to "Comment on 'Catastrophic degradation of the interface of epitaxial silicon carbide on silicon at high temperatures'"[Appl. Phys. Lett. 109, 196101 (2016)] Appl. Phys. Lett. 109, 196102 (2016)
http://dx.doi.org/10.1063/1.4967228

Aiswarya Pradeepkumar, Neeraj Mishra, Atieh Ranjbar Kermany, John J. Boeckl, Jack Hellerstedt, Michael S. Fuhrer, and Francesca Iacopi

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First author contributions: Designing the experiments, photolithographic patterning of SiC, room temp. leakage resistance measurements, data analyses and interpretation, manuscript preparation.

Name of the first author: Aiswarya Pradeepkumar

Sign ____________________ Date ____________________

Signatures of the co-authors including individual contributions:

Name: Dr Neeraj Mishra

Contributions: Metal sputtering, SiC annealing

Sign ____________________ Date ____________________

Name: Dr Atieh Ranjbar Kermany

Contribution: XeF_2 etching of patterned SiC

Sign ____________________ Date ____________________

Name: Dr John J. Boeckl

Contribution: Scientific discussions

Sign ______________________ Date ______________________

Name: Dr Jack Hellerstedt

Contribution: Scientific discussions, manuscript revision

Sign ______________________ Date ______________________

Name: Prof. Michael S. Fuhrer

Contributions: Scientific discussions, manuscript revision

Sign ______________________ Date ______________________

Name: Prof. Francesca Iacopi

Contributions: Research advice and guidance, coordinating the collaboration, assistance in manuscript preparation, critical revision of the manuscript

Sign ______________________ Date ______________________

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4.7 Supporting information

Dimitrijev of the comment argues that the conclusions of our letter[1] are incorrect, based on two points. We summarize each criticism and respond point by point:

1. Dimitriev questions our conclusion that SiC is electrically shorted to Si-based on the fact that the sheet resistance of the annealed SiC-Si system differs quantitatively from that of the pristine silicon substrate material.[2]

We have studied the temperature-dependent data resistivity of the as-grown and annealed 3C-SiC on Si (Fig. 1 of Ref. 1). As-grown n-SiC/p-Si showed limited n-type conduction as expected for an epitaxial SiC film on silicon, whereas the n-SiC/p-Si sample after annealing showed a resistance two orders of magnitude lower than the SiC layer. The conduction in the annealed sample appears dominated by p-type carriers, with a transition around 25K to n-type conduction similar to the non-annealed n-SiC/p-Si. This results clearly indicate the formation of a new parallel conduction path which is (1) p-type, (2) has higher mobility than SiC, and (3) freezes out around 25 K; these aspects are all in agreement with the Si substrate acting as the new conduction channel. The author proposes no alternative conduction channel which could explain our observations (1)–(3). We do observe a quantitative change in the sheet resistance of the Si substrate (underneath the 3C-SiC), which we ascribe to a change in doping after annealing (Table I of Ref. 1). Notably, the mobility of the p-type conduction channel (273 cm^2/Vs) is very similar to that for the doped Si substrate (341 cm^2/Vs), again suggesting that the additional conduction channel is silicon.

In addition, we performed a simple experiment to verify unambiguously that, after annealing, the SiC is indeed electrically well connected to the silicon substrate.

The as-grown unintentionally n-type doped 3C-SiC(100) with thickness of 300 nm grown in-house on lowly doped 6" p-type Si(100) wafer at 1000°C[1,2] was patterned into structures with 300nm of Aluminium contacts as shown in Figure 4-S1. For the electrical characterization, SiC/Si wafers were diced into 1x1cm^2 fragments.

The current-voltage measurements were performed at room temperature to measure the SiC and silicon resistances (leakage) on the as-grown SiC(100) using a HP4145B semiconductor parameter analyser. Analogous samples were annealed at 1100 °C for 1 h.

After an additional XeF2 etching of silicon up to 14 µm in between the SiC structures, the electrical measurements were done at room temperature.

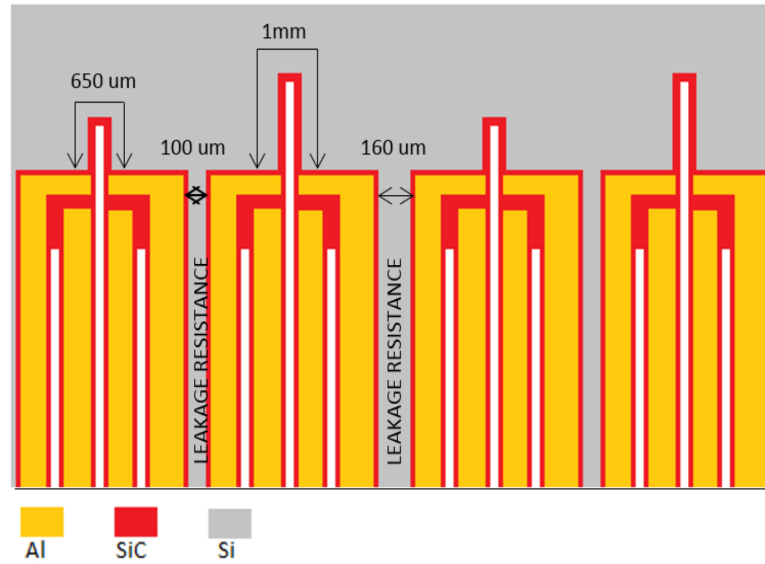

Figure 4-S1: Photolithographic pattern made on the SiC/Si for the electrical characterisation[3,4] (Courtesy of QMNC, Griffith University)

Table 4-S1 SiC and silicon resistances (leakage) measured at room temperature for in-house SiC/Si(100) samples as-grown and after annealing at 1100⁰C. Results are the averaged values from four measurements.

	As-grown	**Annealed**
R_{SiC} of 650µm length (kΩ)	40	3
R_{SiC} of 1mm length (kΩ)	70	4
$R_{leakage}$ across 100µm (kΩ)	2000	1
$R_{leakage}$ across 160µm (kΩ)	2000	1

The as-grown SiC film indicates a factor of 30–50 difference in magnitude of the resistance of the SiC and the leakage through the silicon, as anticipated (Table I). However, after annealing, a major drop in all the SiC and leakage resistances to just a few kΩ is observed (Table 4-S1). This clearly indicates that separate thin-film SiC structures. become electrically shorted through the silicon after annealing, fully supporting our report on the instability of the SiC/ Si interface.[1]

2. The second point of the author's comment rejects the implications of our conclusions

Epitaxial SiC on Si could be used as a pseudo-substrate for the growth of the nanomaterials such as graphene[5] and III-N materials[6], for application as wide as electronic

graphene devices and LED on silicon. Since these materials are generally grown at temperatures greater than 1000°C, we believe it is important to consider the instability we discussed.

As to SiC on silicon for harsh environment operation, we only point out the potential for this failure mechanism to be initiated over time. A conclusive statement on the stability range of the 3C SiC-Si interface in harsh environments can be given exclusively by accurate bias-temperature-stress measurements that we can only encourage the community to investigate.

4.7.1 References

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Chapter 5: Electrical characteristics of heteroepitaxial cubic silicon carbide on silicon

In chapter 4 we have identified that the heterointerface of the 3C-SiC/Si is prone to instability as a consequence of high temperature and large amount of stress relaxed at the SiC/Si interface allowing significant atomic inter-diffusion between the SiC and the Si with the Si dominating the conduction in the 3C-SiC/Si. In the following chapter we have compared the 3C-SiC films grown at different growth conditions on different Si substrates and demonstrated that the interface degradation is general issue associated with any 3C-SiC grown on Si, and find that the Si and C intermix upon or after growth, particularly by the diffusion of carbon into the silicon matrix, creating extensive interstitial carbon traps. The electrical leakage/parallel conduction can only be minimised using a highly resistive silicon (resistivity > 10 kΩcm) instead of a doped silicon as the substrate for growing the 3C-SiC. This evaluation is important and it helps in the successful integration of 3C-SiC/Si as a pseudo-substrate for the epitaxial graphene synthesis.

STATEMENT OF CONTRIBUTION TO CO-AUTHORED PUBLISHED PAPER

Chapter 5 is in the form of a published article. The details of the paper including the co-authors are;

Electrical leakage phenomenon in heteroepitaxial cubic silicon carbide on silicon
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First author contributions: Designing the experiments, sample preparation, Hall effect measurements, SEM study, Synopsys Sentaurus simulations to model the effect of C diffusion on the SiC doping, ICP etching, TLM structure patterning, TLM leakage resistance measurements, data analyses and interpretation, literature review, and manuscript preparation.

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5.1 Abstract

Heteroepitaxial 3C-SiC films on silicon substrates are of technological interest as enablers to integrate the excellent electrical, electronic, mechanical, thermal and epitaxial properties of bulk silicon carbide into well-established silicon technologies. One critical bottleneck of this integration is the establishment of a stable and reliable electronic junction at the heteroepitaxial interface of the n-type SiC with the silicon substrate. We have thus investigated in detail the electrical and transport properties of heteroepitaxial cubic silicon carbide films grown via different methods on low-doped and high-resistivity silicon substrates by using van der Pauw Hall and transfer length measurements as test vehicles. We have found that Si and C intermixing upon or after growth, particularly by the diffusion of carbon into the silicon matrix, creates extensive interstitial carbon traps and hampers the formation of a stable rectifying or insulating junction at the SiC/Si interface. Although a reliable p-n junction maybe not realistic in the SiC/Si system, we can achieve, from a point of view of the electrical isolation of in-plane SiC structures, leakage suppression through the substrate by using a high-resistivity silicon substrate coupled with deep recess etching in between the SiC structures.

5.2 Introduction

Epitaxial cubic silicon carbide films on silicon (3C-SiC/Si and hereafter SiC/Si) have attracted extensive interest for semiconductor device applications such as high-voltage, high-frequency diodes, and heterojunction bipolar transistors.[1] This is because these structures offer access to the properties of SiC, such as its wide bandgap and high thermal conductivity, on more conventional silicon substrates.[2] Despite these significant properties, no 3C-SiC-based devices are currently commercially available[3] and this is due in part to problems associated with SiC/Si junctions.[4-6]

We have recently shown that the expected p-n junction between a p-type silicon substrate to the 3C-SiC, naturally grown as unintentionally n-type, is either non-existing or very unstable so that severe leakage or even plain shorting of the epitaxial silicon carbide to the underlying silicon substrate[1] is typically found.[7-8] The absence of a stable p-n junction at the SiC/Si interface could pose important limitations to the applications of 3C-SiC in power electronics, harsh environment, MEMS, LEDs, graphene-based devices, etc.[2]

To date, a few studies have been conducted on the properties of SiC/Si junctions, however, electrical leakage is linked to stacking fault defects in 3C-SiC.[2] Moreover, studies of strained heterostructures have shown that the substantial tensile strain generated from the lattice and thermal expansion coefficient mismatch between 3C-SiC and silicon may reduce the bandgap of the SiC.[9] Nevertheless, a detailed explanation of the leakage/shorting phenomenon, and the impact of this challenge on the electrical properties of 3C-SiC layers are poorly documented in the literature.

Suemitsu et al. have attempted the growth of SiC onto an intermediate insulating 4H-AlN layer on silicon in order to avoid the diffusion of silicon atoms from the substrate through the SiC layer, which also hampered the graphitization of the SiC surface.[10] This indicates that the instability of the SiC/Si interface affects potential applications in more than one way.

In this work, we develop an in-depth understanding of the historically overlooked leakage problem in 3C-SiC on Si heterojunction system, by studying in detail the electrical behaviour of SiC films epitaxially grown on different silicon substrates under different growth conditions. Based on the findings, we propose a model for the source of electrical and electronic instability of the p-n junction in SiC/Si. Also, based on our understanding of SiC/Si, this work demonstrates a method for solving the problem of in-plane shorting or leakage for isolated SiC mesas or interdigitated structures on silicon.

5.3 Methodologies

In this work we use unintentionally doped (thus n-type), 500 nm thick, NOVASiC 3C-SiC(100) films epitaxially grown on 527 µm low-doped p-type Si(100) having resistivity ranging from 1 to 10 Ωcm as well as high-resistivity (typically n-type, > 10 kΩcm) Si(100) substrates.[11] A second partner, IMEM-CNR, supplied 3C-SiC(100) films grown on 279 ± 25 µm p-type Si(100) with resistivity ranging from 1 to 5 mΩcm.[12] Additionally, we have also tested 5 µm thick SiC films from IMEM-CNR prepared on 0° and 6° off-cut towards (110) Si(100) substrates.[13] Note that the 3C-SiC(100) films from both NOVASiC and IMEM-CNR are grown at 1300-1400 °C. Table I summarizes the samples studied in this work.

For electrical characterization, we diced the SiC/Si wafers into 1.1x1.1 cm^2 coupons and sputtered 150 nm thick nickel contacts (not annealed) onto the four corners using a custom-made shadow mask (Figure 5-1a). We estimated the electrical properties such as

the carrier concentration, carrier mobility, and sheet resistance at room temperature by performing van der Pauw Hall measurements on the SiC/Si samples as well as on representative bare Si substrates using an Ecopia HMS 5300 Hall Effect Measurement System. Scanning Electron Microscopy (SEM) using Zeiss supra 55VP SEM system operating at 10 kV characterized the surface morphology of the epilayers. Moreover, we performed simulations to model the leakage phenomenon and its influence on the electrical conduction using the Synopsys Sentaurus Device™ simulator for the 3C-SiC on low-doped silicon.

Van der Pauw structures of SiC on high-resistivity Si were exposed to Inductively Coupled Plasma (ICP) etching using SF_6 gas and oxygen to remove the SiC layer using the Ni contacts as a hard mask followed by an Energy Dispersive X-Ray Analysis, and the Hall measurements were repeated at room temperature. Furthermore, SiC on high-resistivity Si samples were patterned into transfer length measurement (TLM) structures consisting of 300 nm thick, 500 µm wide aluminium contacts deposited using e-beam evaporation (not annealed) followed by acid etching of aluminium and reactive-ion etching of SiC. Current-voltage at room temperature using HP4145B semiconductor parameter analyser measured the leakage resistances. Afterwards, the silicon in between the SiC pillars for both the van der Pauw and TLM structures of SiC on high-resistivity Si were subsequently etched using ICP, and all measurements were repeated.

Table 5-1 Summary of the samples used.

Samples	**Supplier**	**Si resistivity (Ωcm)**	**Si thickness (µm)**	**SiC thickness (µm)**
SiC/p-Si	NOVASiC	1-10	527 (on-axis)	0.5
SiC/high-resistivity Si	NOVASiC	>10k	235 (on-axis)	0.5
SiC/p-Si	IMEM-CNR	1-5m	279 ± 25 (on-axis)	0.5
SiC/p-Si	IMEM-CNR	1-5m	279 ± 25 (on-axis)	5.0
SiC/p-Si	IMEM-CNR	1-5m	279 ± 25 (6° off-axis (110))	5.0

5.4 Results and discussion

5.4.1 3C-SiC on low-doped silicon

5.4.1.1 Results

Table 5- 2 Hall measured transport characteristics at room temperature. Results are the averaged values extracted from three samples for each type.

	Bare p-Si	**3C-SiC/p-Si**
Carrier type	Holes	Holes
Sheet carrier concentration (cm^{-2})	1(±0.2) x 10^{14}	1(±0.2) x 10^{14}
Mobility ($cm^2V^{-1}s^{-1}$)	341 ± 10	357 ± 10
Sheet resistance (Ω/□)	173 ± 10	166 ± 10

Table 5-2 shows the room temperature Hall measurement results of the low-doped p-Si substrate and 3C-SiC on p-Si. The low-doped p-Si substrate has p-type conduction with sheet carrier concentration, mobility and sheet resistance of 1(±0.2) x 10^{14} cm^{-2}, 341 ± 10 $cm^2V^{-1}s^{-1}$, and 173 ± 10 Ω/□, respectively. 3C-SiC grown on the low-doped p-Si also indicates p-type conduction with a sheet carrier concentration of 1(±0.2) x 10^{14} cm^{-2}, mobility of 357 ± 10 $cm^2V^{-1}s^{-1}$, and sheet resistance of 166 ± 10 Ω/□, comparable to the bare low doped p-Si substrate. This implies that the SiC films grown on low-doped Si substrates are typically shorted and the charge carriers in the thick silicon substrate with relatively high mobility dominate the electrical conduction, as shown in Figure 5-1b. The electrical shorting persists even if we etch deep into the substrate, as long as the silicon charge carriers exist.[8] Note that, we have systematically confirmed that the contacts are not shorting the substrate through the edges.[7-8]

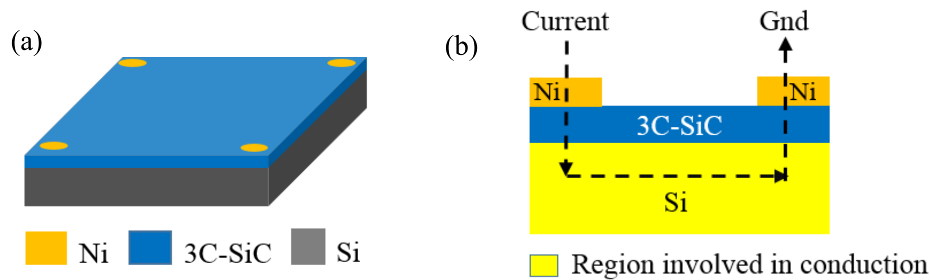

Figure 5- 1: a) Layout of the van der Pauw structure on 3C-SiC/Si, b) schematic of electrical conduction path in the SiC grown at 1300-1400 °C on the low-doped p-Si substrate. The whole silicon substrate is involved in the conduction through the injection of holes into the SiC layer.

The electrical activity of the extended defects such as stacking faults (SF) and antiphase boundaries (APB) in SiC layers has been proposed in the literature to explain the leakage in 3C-SiC devices.[2-3, 14] In order to explore and potentially validate this hypothesis, we tested thicker films where the density of these defects are several orders of magnitude less than the thin films as reported by Song et al.[2].

Table 5-3 shows the room temperature Hall characteristics of IMEM-CNR 500 nm-thin SiC films on p-type Si (0°), 5 µm-thick SiC films on both on-axis (0°) and 6° off-axis p-Si as well as the bare on-axis and off-axis p-Si substrates. We find that the IMEM-CNR 500 nm 3C-SiC films grown on on-axis p-Si are also shorted to the substrate similar to the NOVASiC 3C-SiC films. Moreover, Table 5-3 also clearly shows that the shorting is apparent even for the 5 µm thick SiC films grown on-axis p-Si as the transport characteristics match the underlying substrate. In addition, the transport characteristics of the 5 µm thick 3C-SiC on 6° off-axis p-Si, also exhibits electrical shorting with the substrate. If the extended defects in SiC layers were the main reason for the film-substrate shorting, the leakage would be reduced or absent in the thicker films.[2]

Table 5- 3 Hall measured transport characteristics at room temperature for IMEM-CNR thin 500 nm and thick 5 µm SiC films grown on the on-axis p-Si and 6° off-axis p-Si substrates. Results are the averaged values extracted from three samples for each type.

	SiC on on-axis p-Si			SiC on 6°off-axis p-Si	
	p-Si	500 nm SiC	5 µm SiC	p-Si	5 µm SiC
Carrier type	Holes	Holes	Holes	Holes	Holes
Sheet carrier concentration (cm^{-2})	$6(\pm2)x10^{17}$	$8(\pm2)x10^{17}$	$5(\pm2)x10^{17}$	$6(\pm2)x10^{17}$	$5(\pm2)x10^{17}$
Mobility ($cm^2V^{-1}s^{-1}$)	70 ± 10	50 ± 10	65 ± 10	50 ± 10	50 ± 10
Sheet resistance (Ω/□)	0.17 ± 0.01	0.17 ± 0.01	0.17 ± 0.01	0.18 ± 0.01	0.18 ± 0.01

We performed SEM to determine the extent of extended defects in our samples. Fig. 2 shows an example SEM image of 500 nm thin SiC layers grown on on-axis p-Si and 5 µm thick SiC grow on 6° off-axis p-Si substrates. Figure 5-2a shows that for thin epilayers, the stacking faults and antiphase boundaries are visible whereas, for the thick epilayers these defects are not visible, shown in Figure 5-2b. Thus, although the SEM evidence demonstrates fewer defects at the surface of the thick SiC layers, electrically there is no improvement in the shorting/leakage issue. This indicates that the extended

defects in the SiC layers such as APB or SF probably do not substantially contribute to the leakage phenomenon.

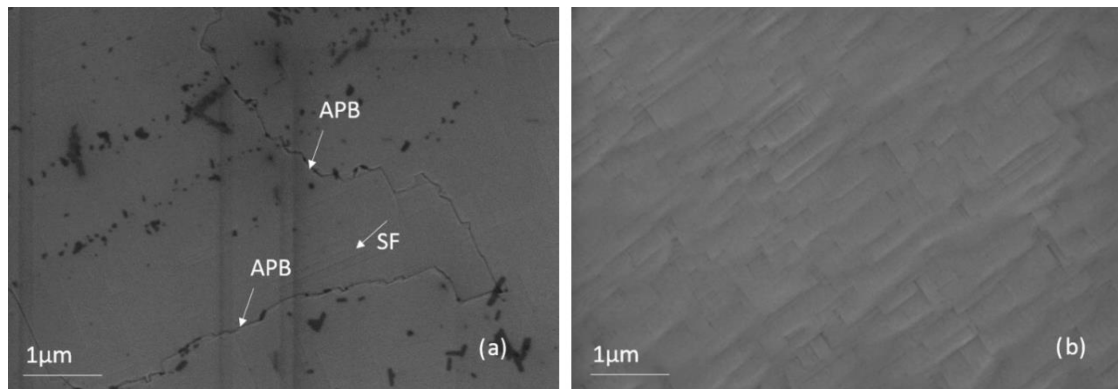

Figure 5-2: Plane view SEM images for IMEM-CNR 3C-SiC a) 500 nm-thin SiC(100) film on on-axis p-Si; where antiphase boundaries (denoted APB) and stacking faults (denoted SF) are visible; b) 5 µm-thick SiC(100) films on 6° off-axis p-Si substrates; APBs and SFs are not visible

5.4.1.2 Discussion and model

In addition to the data presented here, indicating the electrical shorting of SiC/Si films grown at a temperature of 1350°C, we had also previously reported the occurrence of a similar phenomenon in SiC films grown at a lower temperature (~1000°C), after the samples were vacuum annealed at 1100°C.[7-8] We noted that the electrical shorting was invariably accompanied by the relaxation of a considerable amount of compressive stress present at the SiC/Si heterointerface;[7] which was a consequence of the combination of high temperature and high stress at the SiC/Si interface enabling interatomic diffusions between SiC and Si.[15] Due to the stress relaxation at the SiC/Si interface, we observed plastic deformation of the silicon substrate leading to a permanent change in the wafer curvature, becoming more convex (after annealing), as illustrated in Figure 5-3.

Zielinski et al. also observed the occurrence of plastic deformation of the silicon substrate upon film growth when growth temperatures of 1300-1400°C were used.[16-17] In this case, a permanent change of substrate curvature towards a less concave curvature was found, which was used to minimize the total bowing of the substrate upon growth.[16-17] This was an important technological advance, since the significant tensile stress due to the lattice and thermal mismatch of the SiC on silicon system, especially for micron thick SiC films,

would lead to an excessively concave wafer curvature.[15] Such curvature would be particularly challenging for further wafer processing as well as device applications.

In addition, Anzalone et al., Camarda et al. and Watts et al., have reported for SiC grown at 1300°-1400°C intense compressive stress generated within the substrate capable of bowing the whole SiC/Si heterosystem downwards.[18-20] These authors also proposed the stress originated from the early stage of growth (i.e. at the carbonization step), where unspecified "defects" are generated in the silicon substrate.[18-19]

Noting that the SiC/Si samples studied in this work were all grown at high temperatures, similar to that of Zielinski et al., and that all of the samples have shown electrical shorting with the silicon substrate, it seems logical to expect that this phenomenon must be related to a permanent change (plastic deformation) of the substrate (convex) curvature. This permanent curvature change must occur whenever the top portion of the silicon substrate is driven into compression (see schematic in Figure 5-3). We propose that the compression in the top portion of the substrate is due to carbon diffusion into the silicon substrate matrix, as the carbon would expand the Si substrate lattice.

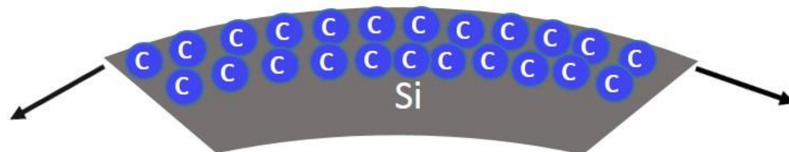

Figure 5-3: Schematic of Si substrate bending into more convex due to the compressive stress exerted by the carbon interstitials within the top portion of silicon.

The guiding reasons for our hypothesis are that due to the high stresses and high temperatures involved in SiC on Si heteroepitaxy, combined with a very high carbon-silicon miscibility (both elements are column IV), a considerable driving force for C and Si inter-diffusion is anticipated in the interfacial region. Indeed, an out-diffusion of silicon forming typical interfacial voids has been reported extensively in the literature.[10, 16] However, the possibility for microscopic atomic carbon diffusion into the silicon matrix has been largely overlooked, as opposed to the macroscopically evident silicon voids. In fact, we note that in all samples used for this work the silicon voids were intentionally suppressed by the vendors through the engineering of the heteroepitaxial process.

Moreover, we expect carbon interstitials to affect SiC/Si electrical junction properties. Note that when the carbon concentration in silicon exceeds the solubility of substitutional

carbon (~10^{17} cm^{-3} at 1300°C),[21] interstitial carbon point defects are formed.[22] A vast extent of atomic diffusion of carbon into the silicon substrate would, therefore, lead to a significant amount of interstitial carbon, which would, in turn, drive the top portion of the substrate into compression while also strongly affecting the SiC/Si electrical junction. Interstitial carbon, complexes between the interstitial and substitutional carbons or carbon precipitates may be electrically active and negatively affect the electrical characteristics of p-n junctions[22-23] resulting in substantial leakage, or even plain electrical shorting, since such defects act as an additional conduction path for charge carriers. The carbon interstitials can behave as deep acceptors in silicon with an activation energy of 0.35 eV from the valence band (hole traps)[23], and assist compensation of unintentional donors in the SiC film as well as hole injection from the Si substrate across the Si/SiC interface further reducing the effectiveness of p-n junction.[4]

Hence, the generation of a considerable amount of interstitial carbon defects in the top portion of silicon upon high-temperature epitaxy would explain both the mechanical and the electrical behaviour observed in the SiC/Si system.

We simulated the effect of interstitial carbon on the junction between SiC and the low-doped p-Si substrate using Technology Computer-Aided Design (TCAD) simulations, performed at 1V bias, using the parameters summarized in Table 5-4.

The initial n-type doping concentration for the SiC films was set to 1 x 10^{19} cm^{-3} according to the value in Pradeepkumar et al., measured prior to the degradation of the p-n junction (see Table IV and Figure 5- 4a).[7] Hole -type doping for the silicon was set at 1.3 x 10^{15} cm^{-3} as per Hall measurements of the bare p-Si in Table 5-2 (see Figure 5-4b). The electronic defects in the silicon were subsequently introduced in the calculation, assuming an ionization energy of 0.35 eV from the valence band (hole traps, deep acceptors) as reported for interstitial carbon in silicon by Simoen et al.[23] The simulations accounting for the interstitial defects show that an acceptor density of about 10^{20} cm^{-3} in the silicon is sufficient in order to invert the conduction of the system from n-type to p-type (Figure 5-4c and 4d).

Table 5- 4 Simulation parameters.

	Thickness (μm)	Doping (cm^{-3})	Hole trap density (cm^{-3})	Ionization energy (eV)
3C-SiC	0.5	1 x 10^{19} (n)	-	-
Si	527	1.3 x 10^{15} (p)	1 x 10^{20}	0.35

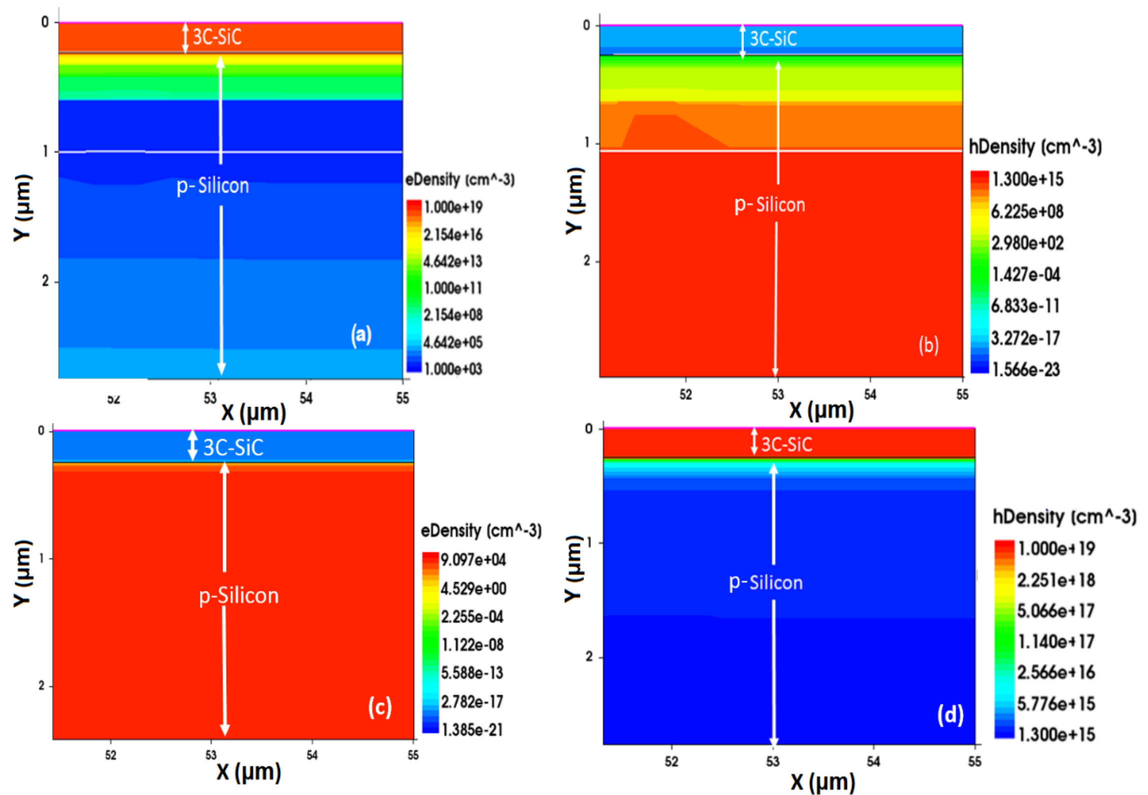

Figure 5-4: TCAD simulation results of the 3C-SiC on low doped p-Si substrate a) electron density and b) hole density, in the SiC/Si system before junction degradation (no defects); c) electron density and d) hole density, in the SiC/Si system after incorporating interstitial carbon degradation within the silicon.

Therefore, the degradation of the p-n junction at the interface of the n-SiC film on p-silicon (upon growth or high-temperature annealing) can be explained by the presence of electrically active interstitial carbon acceptor traps in excess of 10^{20} cm^{-3} within the top portion of the substrate.

For completeness, we note that an additional potential reason for the degradation of the SiC/Si junction could be the reduced bandgap arising from the residual tensile strain in the SiC epilayers.[9] That is, the bandgap reduction results in a smaller valence band barrier

and leads to increased hole current injection from the Si to the SiC.[9] To test the hypothesis of tensile strain-induced SiC bandgap changes on the junction we simulated the SiC/Si system with the strained bandgap and electron affinity values mentioned by Rahimi et al.[9] and found that even a large concentration of those acceptor traps (up to ~10^{20} cm^{-3}) in the film does not appreciably contribute to the degradation of the heterojunction between the SiC film and the substrate.

5.4.2 3C-SiC on high-resistivity silicon

5.4.2.1 Results

In an attempt to electrically insulate the silicon carbide film from the silicon substrate, we have used a high-resistivity silicon as the substrate, as opposed to p-type doped silicon.

Table 5-5 shows the room temperature van der Pauw Hall measurement results of 3C-SiC grown on high-resistivity Si as well as the representative bare Si substrate. High-resistivity silicon shows n-type conduction, with a sheet carrier concentration of 1(±2) x 10^{10} cm^{-2}, mobility of 1220 ± 10 $cm^2V^{-1}s^{-1}$, and sheet resistance of 500 ± 3 kΩ/□.

After the SiC film growth on the high-resistivity Si, the transport characterisation showed a carrier concentration one order of magnitude higher, and the sheet resistance one order of magnitude smaller compared to the bare substrate. However, even after completely removing the SiC layer using ICP etching, the Hall measured characteristics remained largely unaffected and consistent with the values before the removal of the SiC layer. Note that the complete removal of the SiC layer has been confirmed using an Energy Dispersive X-Ray Analysis after etching.

The similar transport characteristics before and after the removal of the SiC layer clearly indicate that the SiC is not responsible for the measured electrical conduction. To clarify this and discern the origin of the conduction in SiC/high-resistivity Si, we measured the leakage resistances between SiC mesas on the high-resistivity Si using the TLM method as shown in Figure 5-5.

Table 5-5 Hall measured transport characteristics at room temperature. Results are the averaged values extracted from three samples for each type.

	High-resistivity Si	SiC/high-resistivity Si	Removed SiC/high-resistivity Si
Carrier type	Electrons	Electrons	Electrons
Carrier concentration (cm^{-2})	$1(\pm2) \times 10^{10}$	$3(\pm2) \times 10^{11}$	$4(\pm2) \times 10^{11}$
Mobility ($cm^2V^{-1}s^{-1}$)	1220 ± 10	1677 ±10	1650 ± 10
Sheet resistance (kΩ/□)	500 ± 3	12 ± 3	12 ± 3

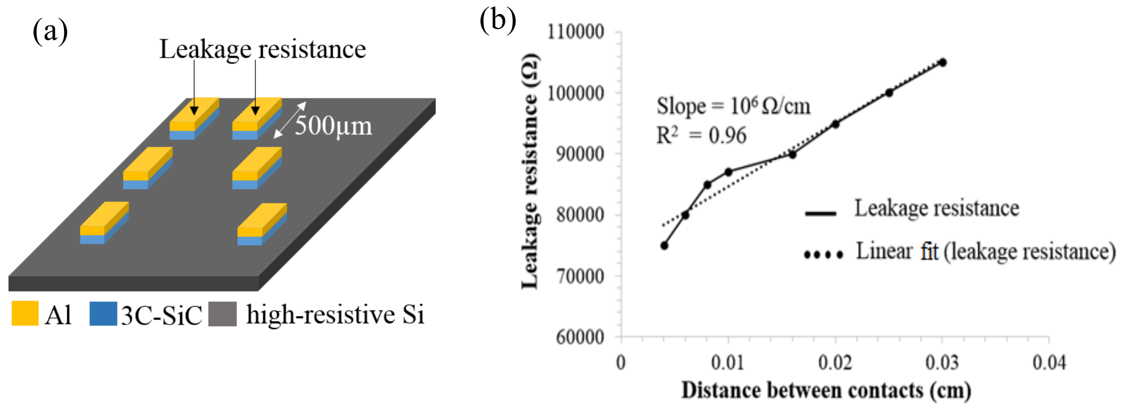

Figure 5-5: a) TLM structures on the 3C-SiC/high-resistivity Si, b) Fitted TLM leakage resistances versus contact spacing for SiC on high-resistivity Si

Figure 5-5b shows the fitted leakage resistances obtained using TLM structures on the SiC/high-resistivity Si as a function of different contact spacing with a slope of 10^6 Ωcm^{-1}. The sheet resistance obtained experimentally from slope and width of the contact is ~50 kΩ/□, about the same order of magnitude of the sheet resistance obtained from the Hall measurements in TABLE 5-2 after growth and/or removal of the SiC. Based on the specification of the high-resistivity substrate, we would expect a 500 kΩ/□ of sheet resistance for the TLM measurement. In conclusion, both van der Pauw and TLM measurements indicate that after the growth of SiC on the high-resistivity silicon, a leakage path is created in a region below the interface, which is not removed by the etching of the SiC.

We suggest that the presence of additional carriers in the order of ~10^{11} cm^{-2} within the high-resistivity silicon forming a leakage path below the interface can be attributed once again to the carbon out-diffusion into silicon forming interstitial carbon. Sze indicates that the interstitial carbon in n-type silicon acts as a donor with a defect level of 0.25 eV from the conduction band, creating effectively an n-type doping.[24] The presence of interstitial carbon point defects within the silicon can thus form a leakage path within the

top portion of the high-resistivity substrate. The schematic representation of the electrical conduction in 3C-SiC on high-resistivity silicon is given in Figure 5-6.

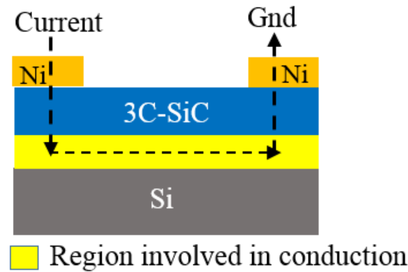

Figure 5-6: Schematic of conduction path in 3C-SiC/high-resistivity Si grown at 1300 - 1400 °C -the conduction occurs within a region of a few micrometres thick below the interface.

5.4.3 Practical solution for the 3C-SiC/Si in-plane leakage

Based upon the conduction path sketched in Figure 5-6, we would expect that removing the conductive portion of the silicon could resolve the leakage problem in the SiC/high-resistivity Si system.

Table 5-6 (a) shows that after etching away the conductive region in the silicon below the SiC/Si interface we obtain a van der Pauw sheet resistance of 492 ± 2 kΩ/□ indicating acceptable electrical isolation between the SiC mesas. The leakage resistances for the SiC/high-resistivity Si using TLM structures after the removal of the conductive region is ~10 MΩ, indicating that leakage is eliminated within the SiC/Si system, see Table 5-6 (b).

Table 5-6 Electrical characteristics at room temperature for SiC/high-resistivity Si before and after ~20 µm deep etching of silicon between SiC pillars a) van der Pauw Hall measurement results b) TLM leakage resistance results. Results after etching are the averaged values of two samples each.

(a)

	SiC/high-resistivity Si (before etching)	SiC/high-resistivity Si (after 20 µm etch)
Carrier type	Electrons	Electrons
Sheet carrier concentration (cm^{-2})	3(±2) x 10^{11}	5(±2) x 10^{11}
Mobility ($cm^2V^{-1}s^{-1}$)	1677 ± 10	34 ± 10
Sheet resistance (kΩ/□)	12 ± 3	492 ± 2

(b)

Contact spacing (μm)	TLM leakage resistance	
	before etch (kΩ)	after 20 μm etch (MΩ)
40	75	8.5
60	80	8.5
80	85	9.5
100	87	10
160	90	-
200	95	10

From both the van der Pauw and TLM results we find that in order to completely isolate the SiC mesas, we need to etch at least 20 μm deep into the high-resistivity silicon between the SiC pillars, see Figures 5-7a and 7b.

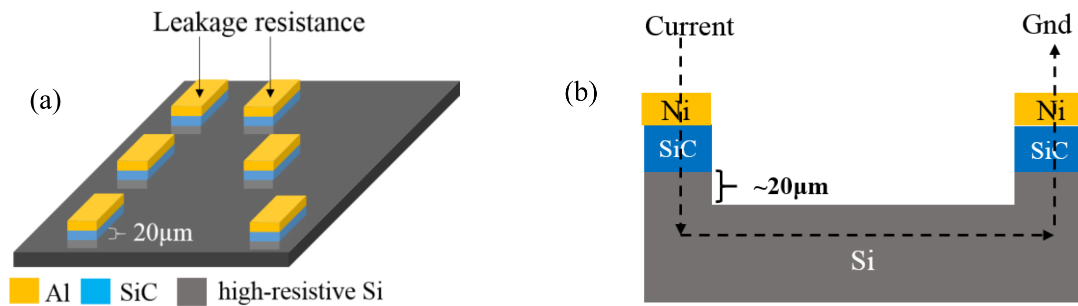

Figure 5-7: SiC/high-resistivity Si after ~20 μm deep etching of Si a) TLM structure, b) electrical conduction

5.5 Conclusions

The scope for application of heteroepitaxial 3C-SiC films grown on Si is typically limited by the electrical instability of the heterointerface. Although this limitation was already known in the scientific community, the reason for this instability had not been addressed. Here we show that, upon epitaxial growth at high temperature, this electrical instability is due to the diffusion[25] of carbon atoms into the underlying silicon matrix-forming electrically active interstitial carbon defects, which also results in strong compression for the top portion of the substrate.

When considering epitaxial SiC on a p-type silicon substrate, we have shown that an interstitial carbon concentration in silicon in excess of 10^{20} cm^{-3} can invert the conduction in the SiC from n-type to p-type due to the generated acceptor traps (interstitial carbon in silicon forming a mid- bandgap level at 0.35 eV), destroying the electrical junction. When

a highly resistive silicon substrate is used instead, we have shown that atomic carbon diffusion within the top portion of silicon generates a leakage path below the SiC/Si heterointerface. We can attribute this phenomenon again to the interstitial diffusion of carbon, generating additional n-type carriers in silicon due to the second type of electronic defect associated with interstitial carbon, which is a donor level 0.2 eV from the conduction band. Nevertheless, we have also demonstrated that we can achieve electrical isolation of SiC mesas on high-resistivity silicon substrates by etching away at least 20 µm into the silicon between the SiC structures.

We also conclude that the electrical instability of the SiC on silicon system is a universal underlying problem associated with direct epitaxial synthesis, no matter the epitaxial approach used, although certain conditions such as temperature are expected to influence the extent of this phenomenon. Therefore, this work clarifies a long-standing issue in the SiC community.

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Chapter 6: Charge transport properties and electrical conduction in epitaxial graphene on cubic silicon

After identifying the interface degradation in the SiC/Si heterosystem and demonstrating the origin of the issue as well as a potential method to overcome it, we investigate the carrier transport properties of epitaxial graphene synthesized on top of the 3C-SiC/Si. Here, we used the 3C-SiC grown on highly resistive silicon substrates (from the findings of the previous chapter) as the substrate for growing graphene via the alloy-mediated graphitization method. This chapter presents the first report of Hall measured temperature-dependent transport characteristics of epitaxial graphene directly grown on silicon substrates and compare it with those well-established graphene on bulk SiC.

STATEMENT OF CONTRIBUTION TO CO-AUTHORED PUBLISHED PAPER

Chapter 6 is in the form of a published article. The details of the paper including the co-authors are;

p-type Epitaxial Graphene on Cubic Silicon Carbide on Silicon, *ACS Applied Nano Materials* (2019), https://doi.org/10.1021/acsanm.9b02349

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First author contribution: Design of experiments, sample preparation, Raman spectroscopy measurements, room temperature and low-temp.(80 K – 300 K) Hall effect experiments, data analyses and interpretation, literature review, manuscript preparation.

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Contributions: SiC growth, scientific discussions

Sign ________________________ Date ________________________

Name: Dr Hansika I. Sirikumara

Contributions: DFT calculations

Sign ________________________ Date ________________________

Name: Dr Thushari Jayasekara

Contributions: DFT calculations, assistance in manuscript preparation

Sign ________________________ Date ________________________

Name: Dr David Kurt Gaskill

Contributions: Research guidance and advice, assistance in structuring the manuscript, critical revision of the article

Sign ________________________ Date ________________________

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Contributions: Research guidance and advice, facilitating and coordinating the collaboration, assistance in structuring the manuscript, critical revision of the manuscript

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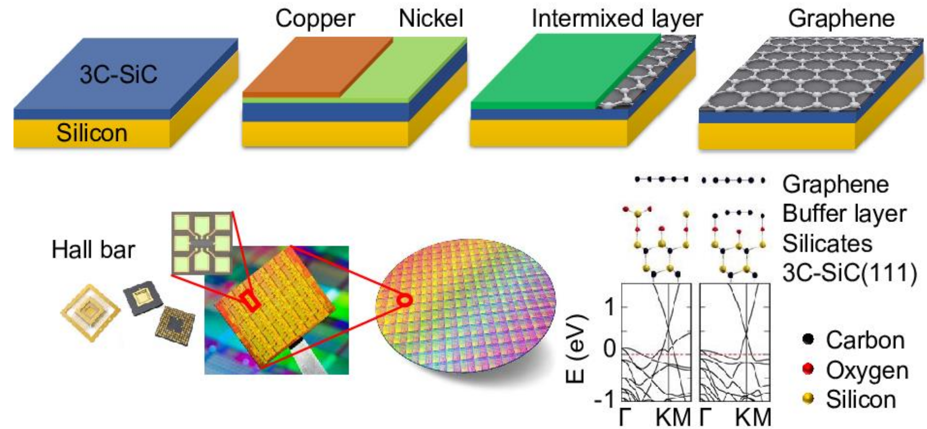
6.1 Abstract



The synthesis of graphene on cubic silicon carbide on silicon pseudosubstrates draws enormous interest due to the potential integration of the 2D material with the well-established silicon technology and processing. However, the control of transport properties over large scales on this platform, essential for integrated electronics and photonics applications, has lagged behind so far, due to limitations such as 3C-SiC/Si interface instability and non-uniform graphene coverage. We address these issues by obtaining an epitaxial graphene (EG) onto 3C-SiC on a highly resistive silicon substrate using an alloy–mediated, solid-source graphene synthesis. We report the transport properties of EG grown over large areas directly on 3C-SiC(100) and 3C-SiC(111) substrates and we present the corresponding physical models. We observe that the carrier transport of EG/3C-SiC is dominated by the graphene-substrate interaction rather than the EG grain size, sharing the same conductivity and same inverse power -law as EG on 4H- or 6H- SiC(0001) substrates – although the grain sizes for the latter are vastly different. In addition, we show that the induced oxidation/silicates at the EG/3C-SiC interface generate a p-type charge in this graphene, particularly high for the EG/3C-SiC(001). When silicates are at the interface, the presence of a buffer layer in the EG/3C-SiC(111) system is found to reduce somewhat the charge transfer. This work also indicates that a renewed focus on the understanding and engineering of the EG interfaces could very well enable the long sought -after graphene -based electronics and photonics integrated on silicon.

Keywords: Epitaxial graphene, Graphene/3C-SiC interface, substrate interaction, mobility, buffer layer, intercalation

6.2 Introduction

Graphene has been extensively investigated over the past decade owing to its anticipated outstanding properties such as exceptional carrier mobility and room temperature ballistic transport.[1-4] The epitaxial growth of graphene on hexagonal (4H- and 6H-) silicon carbide (SiC) wafers has progressed substantially both in quality and process reliability.[3-15] However, when considering cost and wafer scaling challenges of bulk SiC wafers, as well as the relative immaturity of the SiC device technology vis-à-vis the well-established Si-based processing technologies, there is compelling interest to obtain epitaxial graphene (EG) also on silicon wafers for advancing a much wider range of integrated technologies such as integrated electronics and photonics. EG on silicon wafers has been pursued mainly using two different pseudosubstrates; one, a thin film of germanium[16-18] and the other, a thin film of cubic silicon carbide (3C-SiC).[19-27] Table 6-1 shows a summary of attempts made to growth and electrical characterization of EG on Si wafers.

Although the growth of EG on Si wafers has been pursued in the past - either using thin films of 3C-SiC[19, 21-27] or germanium,[16-18] the charge transport behavior of the obtained EG has not been thoroughly assessed over areas large enough to be relevant for semiconductor fabrication. Kang et al.[24] reported room temperature transport properties of few-layer graphene (FLG) grown via thermal decomposition on 3C-SiC(110) substrate using a back-gated field-effect transistor (FET), however, the results are complicated by the presence of large amount of gate-leakage current. Moon et al.[22] and Lee et al.[17] also reported the room temperature transport properties of graphene on Si via intermediate 3C-SiC and H-terminated Ge layers, respectively. However, their measurements were performed, in the first case, using a non-contact Hall micro-wave -based (Lehighton) method, which is an unconventional and not benchmarked method, and in the second case, on EG only after it was transferred onto SiO_2/Si substrates– which, as we will show, is not representative of the electronic properties of the EG on the original substrate. Further to that, Debrowski et al.[16] have reported the electrical properties in FET configuration for the graphene grown on μm^2 size Ge(100) islands pre-deposited on Si(100) substrate. Evaluation of transport properties from FET measurements are geometry and electrostatics dependent and are affected by the substrate.[28] This type of transport measurements approach does not allow a thorough investigation of the scattering mechanisms. Temperature-dependent Hall effect measurements are required in order to provide the full information on the carrier transport in epitaxial graphene.

In this work, we use epitaxial 3C-SiC films grown on silicon wafers as pseudosubstrates for epitaxial graphene growth. As we had previously reported, the major historical limitations in using a 3C-SiC/Si substrate for graphene growth have been not only the difficulty to achieve continuous graphene coverage (mono- or multilayer) on the substrate[29] but also the instability of the 3C-SiC/Si heterojunction, hampering a reliable electrical characterization of the EG.[30-31] Note that, these limiting factors have not been effectively addressed by the prior attempts reported in Table 6-1.

Table 6-1: Summary of attempts to the growth and the transport characterization of epitaxial graphene on Si wafers at room temperature.

epitaxial graphene		transport properties at 300 K					ref
substrate	growth process	n/p[a]	N[b] (cm^{-2})	μ[c] ($cm^2V^{-1}s^{-1}$)	R_{sh}[d] (Ω/□)	measurement technique	
3C-SiC(111)/n-Si(111)	Thermal decom.	n	1.8×10^{13}	-	-	ARPES	21
3. 3C-SiC(111)/p-Si(111) 4. 3C-SiC(111)/p-Si(110)	Thermal decom.	n	-	-	1. 17 k 2. 90 k	Top-gate FET, Transmission line model (TLM)	23
3C-SiC(110)/Si(110)	Thermal decom.	n	$0.6 - 3.4 \times 10^{11}$	430 - 6200	2.8-215 k	FLG back-gated FET	24
3C-SiC(111)/Si(111)	Thermal decom.	1.n 2.n/p	6×10^{11}	1. 950 2. 175 (n) 2. 285 (h)	1. 6 k - -	1. Non-contact hall micro-wave method 2. FET	22
3C-SiC(100)/Si(100) 3C-SiC(111)/Si(111)	CVD	-	-	-	3.5 – 50 k	Hg probe and c-TLM	19
Device size Ge(100) islands/Si(100) –	1. CVD[e] 2. MBE[f]	p	1. 3×10^{13} 2. 10^{12}	1. 600±300 2. 1200±400	-	4-point STM -FET	16
H-Ge(110)/Si(110)	CVD - 1. Single cryst. 2. Poly cryst.	-	3×10^{11}	1. 10620 2. 2570	1. 2-5 k 2. 6-12 k	Back-gated GFET on transferred graphene to SiO2/Si	17
H-intercalated Ge(100)/Si(100)	CVD	-	1. 6.8×10^{12} 2. 9.2×10^{12}	1. 950-1050 2. 470-520	-	1. before H-intercalation 2. after H-intercalation	18

[a]electrons/holes, [b]sheet carrier concentration, [c]mobility, [d]sheet resistance, [e]chemical vapor deposition, [f]molecular beam epitaxy

In this work, we are able to obtain continuous wafer-scale graphene coverage as well as overcome the parallel conduction issue by using a Ni/Cu alloy–mediated EG synthesis onto a highly–resistive 3C-SiC grown on high-resistivity silicon substrates. The alloy–

mediated approach enables a consistent EG coverage over large areas despite the highly defective hetero-epitaxial 3C-SiC surface thanks to liquid–phase epitaxial growth conditions,[20] as opposed to the more conventional EG synthesis by thermal decomposition of the 3C-SiC.[21-27] The highly–resistive silicon substrate, coupled with the high resistivity 3C-SiC are essential to ensure a thorough electrical insulation of the EG from the substrate and enable the transport measurements of EG.[30] Room temperature van der Pauw (vdP) Hall effect measurements indicate p-type graphene on the 3C-SiC/Si pseudosubstrate unlike the typically n-type epitaxial graphene synthesized via thermal decomposition of 3C-SiC.[21,23-25,27,32] Temperature dependent sheet resistance measurement confirms that the EG is electrically isolated from its underlying substrate system. Using Hall effect measurements, X-ray photoelectron spectroscopy (XPS) as well as density functional theory (DFT) calculations we demonstrate that the carrier transport in EG is determined by the strong interaction with its substrate, which contains interface silicates due to the alloy-mediated synthesis. Furthermore, our results imply that the transport properties of the alloy-mediated EG on 3C-SiC is independent of the number of graphene layers as well as the domain sizes in the observed regime.

6.3 Results and discussion

The EG was obtained via a solid–source, Ni/Cu alloy-mediated method at ~1100°C below 5 x 10^{-4} mbar pressure as described by Mishra et al.[20], see Figure 6-1 (refer to Methods section for more details on sample preparation and characterization tools). The EG samples have typically a root mean square roughness ~9 nm, about 2-fold larger than the 3C–SiC/Si which is ~4 nm.[20] Details on the number of graphene layers are provided in the XPS section of this manuscript.

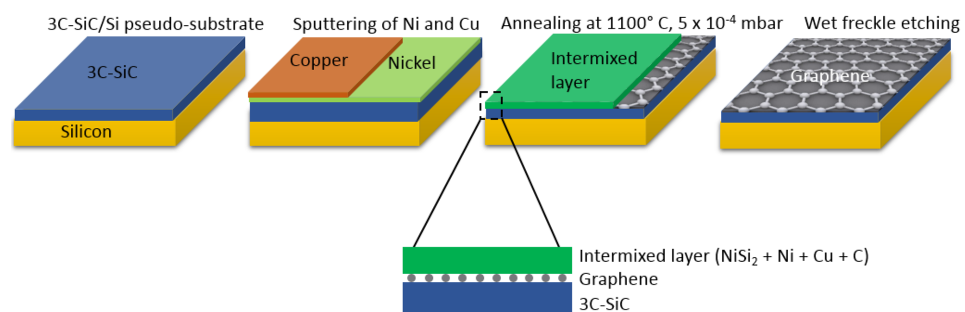


Figure 6-1: Schematic of the process steps for the alloy-mediated synthesis of graphene on the 3C-SiC/Si substrate.[20]

6.3.1 Raman characterization

Table 6-2 Raman mapping characteristics at 300K, for EG on 3C-SiC/Si of both (100) and (111) orientations showing grain sizes calculated from intensity ratios of D and G bands, peak positions of G and 2D, and FWHM of G and 2D bands. Error bars correspond to the standard deviation of the measured values over an area of 30 x 30 cm^2.

EG/3C-SiC(100)						
Sample	I_D/I_G	$L_a{}^a$ (nm)	Peak positions (cm^{-1})		FWHM (cm^{-1})	
			G	2D	G	2D
Sample 1	0.24±0.03	80±10	1582.4±0.1	2698.6±0.1	26.3±0.4	45.2±0.3
Sample 2	0.22±0.03	87±10	1582.5±0.1	2699.2±0.1	25.5±0.5	45.3±0.4
Sample 3	0.22±0.02	87±10	1576.4±0.3	2708.8±0.3	27.9±0.3	51.2±0.2
EG/3C-SiC(111)						
Sample	I_D/I_G	$L_a{}^a$ (nm)	Peak positions (cm^{-1})		FWHM (cm^{-1})	
			G	2D	G	2D
Sample 1	0.22±0.02	87±10	1577.7±0.2	2709.7±0.2	27.0±0.5	56.3±0.5
Sample 2	0.24±0.02	80±10	1581.3±0.1	2698.0±0.1	28.2±0.3	49.2±0.3
Sample 3	0.34±0.01	56±10	1582.0±0.1	2698.0±0.1	27.2±0.4	46.6±0.3
Sample 4	0.35±0.01	55±10	1582.4±0.1	2696.7±0.3	27.1±0.4	55.8±0.6

^{a}*estimated grain size*

Figure 6-S1 shows the example maps of the Raman intensity ratio of D to G peak (I_D/I_G), 2D to G peak (I_{2D}/I_G), G position, 2D position, G full width half maximum (FWHM) and 2D FWHM of the epitaxial graphene grown on 3C-SiC(100) and 3C-SiC(111) substrates. The maps show only a small range of variations across the measured region (quoted in Table 6-2) which indicates the uniformity of the graphene samples. Table 6-2 summarizes the Raman intensity ratios I_D/I_G and I_{2D}/I_G, positions of the G and 2D bands, and FWHM of the G and 2D bands for the selected EG samples. Figure 6-S2 shows the average Raman spectra of the selected EG samples (across 30 μm x 30 μm area) from Table 6-2 indicating the SiC LO, D, G and 2D Raman bands. I_D/I_G mapping ratios of the samples range between 0.22 (±0.03) to 0.35 (±0.01) (Table 6-2). We estimated the average graphene grain sizes for all the EG samples using the I_D/I_G[33] ratios. The grain sizes of the graphene samples range from 55 to 87 (±10) nm. Figure 6-S3 shows the presence of in-plane modes indicative of turbostratic stacking of the graphene layers.[34] In addition, the 2D FWHM values given in Table 6-2 also indicate a turbostratic nature of multilayer graphene

according to Malard et al.[35] (45 – 60 cm^{-1}). Turbostratic stacking has also been observed by Escobedo-Cousin et al. for the few-layer graphene formed by solid phase growth on the Si- or C-face of the bulk SiC.[9]

The complexity of the 3C-SiC and Si interface is known to give rise to a range of defects,[36] yet polarized Raman data imply that the graphene is epitaxial with respect to the pseudosubstrate and hence justifies describing it as epitaxial graphene. Figure 6-2 shows polar plots of the Raman Si peak, 3C-SiC TO peak[37] and the graphene[38] 2D to G peak intensity ratio as a function of the relative angle (β) between the light polarization of the analyzer and incident laser, measured on single spots – see Figure 6-S4 for additional plots taken on 2 other sample spots - for EG/3C-SiC(100) and EG/3C-SiC(111). The results show that the polarized Raman intensities for both the 3C-SiC and the EG have a preferential dependence on each other and with respect to the Si implying an epitaxial relationship amongst the triad. This is easily seen in Figure 6-2a where the preferred polarization angle of 3C-SiC with respect to the Si(100) substrate is about -5 ± 2° and that the EG polarization is about -22 ± 2° with respect to the Si(100). Differently, the Raman peak intensity for Si(111) and 3C-SiC(111) is almost independent of the polarization angle β[39] as shown in Figure 6-2b. Even though it is not possible to use the Si(111) and 3C-SiC(111) for crystallographic references, the maximum of the EG 2D to G Raman intensity ratio is consistent within 3° all over the measured sample spots. We attribute the variation in crystallographic orientation of the EG on Si(100) and Si(111) to the turbostratic nature of the EG and differences in interface structure (see the XPS section below). The plots in Figure 6-2 clearly indicate that the graphene synthesized using the alloy-mediated approach exhibits an epitaxial relation with the highly defective 3C-SiC pseudosubstrate. We note that the angle of rotation of the alloy mediated graphene with the pseudosubstrate is smaller than that of the graphene synthesized on bulk SiC,[27, 40] which is also likely related to the turbostratic nature of the EG.

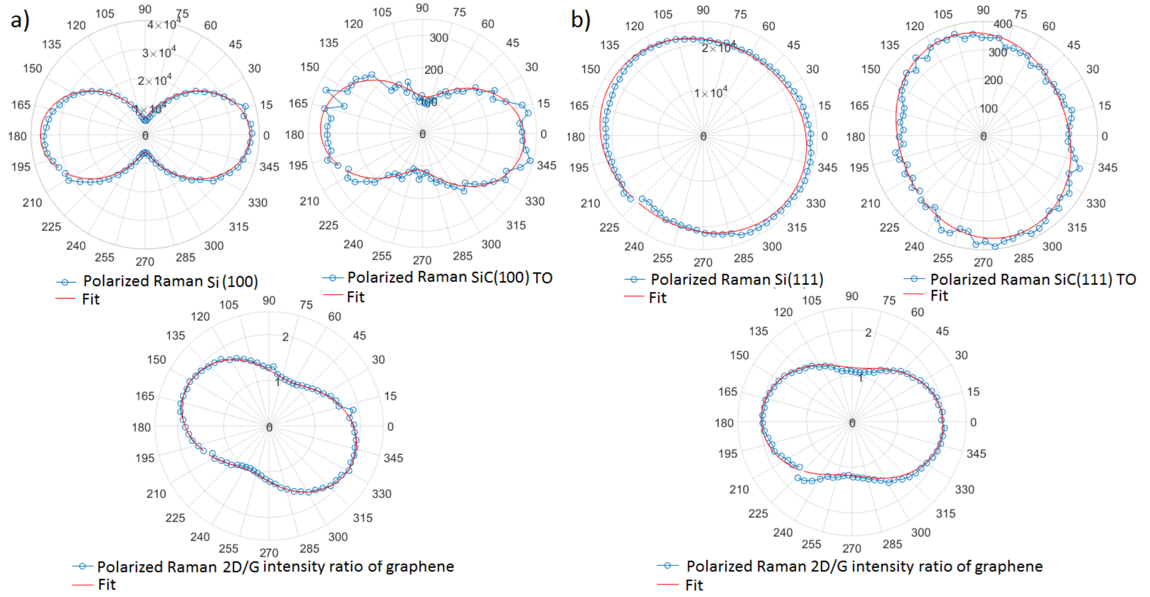
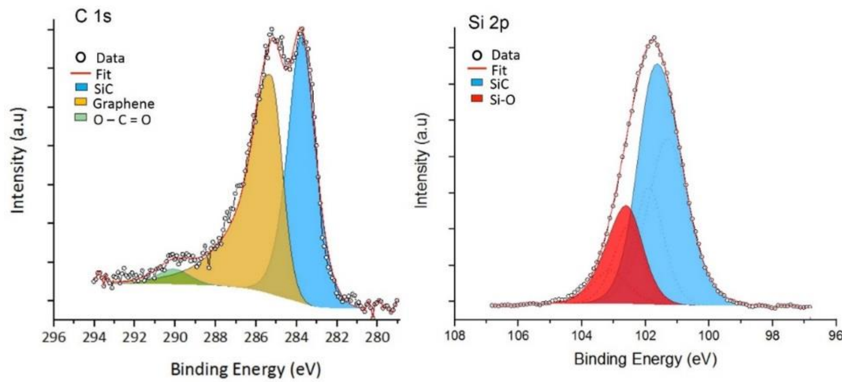


Figure 6-2: Polar plots of Si peak intensity, 3C-SiC TO peak intensity and the ratio of the 2D to G peak intensity as a function of the relative angle (β) between the polarizations of the analyzer and incident laser, for (a) EG/3C-SiC(100); (b) EG/3C-SiC(111).

6.3.2 X-ray Photoelectron Spectroscopy

a) EG/3C-SiC(100)



b) EG/3C-SiC(111)

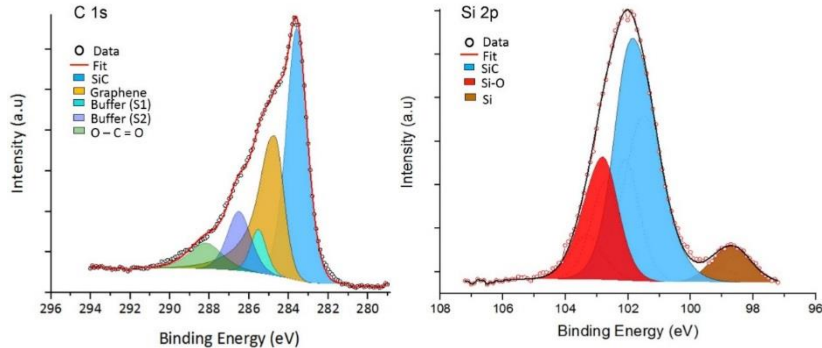


Figure 6-3: XPS C 1s and Si 2p core-level spectrum for; (a) EG/3C-SiC(100) (sample 3 in Table 2) and (b) EG/3C-SiC(111) (sample 1 in Table 6-2)

Figure 6-3 shows the XPS C 1s and Si 2p spectra of EG3C-SiC(100) and EG/3C-SiC(111). A combination of Gaussian and Lorentzian line shapes (Voigt) is used to fit the curves. The background is subtracted using Shirley procedure.[41] For EG/3C-SiC(100), three peaks are used to fit the C 1s spectra, which corresponds to SiC (~283.7 eV), graphene (~285.2 eV), and O-C=O (~290 eV).[9] The EG/3C-SiC(111) C 1s spectrum is different as it shows photoelectron peaks at ~283.6 eV (SiC), ~284.7 eV (graphene), O-C=O (~288.2 eV) and buffer layer components at 285.5 eV (S1), 286.4 eV (S2). The presence of a buffer layer in EG/SiC(111) has also been previously reported in literature.[21, 27, 42] The graphene layer thicknesses are estimated from the C 1s data[43], see supplementary information (SI), section 2 for details. The overall variation of EG thickness across different samples ranges from 3 to 7 layers. Note that since the EG/SiC/Si shows turbostratic stacking, a weak interaction is expected among the layers so that the multilayer graphene is expected to be electrically equivalent to a monolayer.[35]

The Si 2p spectra is fitted with Si $2p_{3/2}$ and Si $2p_{1/2}$ spin-orbit doublets with 0.6 eV splitting: Si-C (~101.3), Si-O (~102.5), Si (~99), the peak positions are reported for Si $2p_{3/2}$. The Si 2p spectra of both EG/3C-SiC(100) and EG/3C-SiC(111) indicate Si-O bonds at ~102.5 eV. This signifies a considerable amount of top-substrate oxidation/silicates at the EG/3C-SiC interface - just underneath the graphene. In the case of 3C-SiC(111), the presence of stacking faults[36] promotes out-diffusion of silicon into the SiC, which is observed at ~100.2 eV in the XPS Si 2p of EG/3C-SiC(111). Note that, neither the XPS survey spectrum (within the range between 850 to 960 eV[44-45]) nor the energy-dispersive X-ray spectroscopy (EDX) indicate the presence of metal (nickel or copper) or metal oxides in the graphene, see Figure 6-S5 for EG on 3C-SiC(100) (sample 3) and 3C-SiC(111) (sample 1).

6.3.3 Electrical characterization

We investigated the room temperature transport properties of the EG samples synthesized on both 3C-SiC(100) and 3C-SiC(111) substrates using the van der Pauw configuration as shown in Figure 6-4a. The room temperature properties are summarized in Table 6-3.

The EG synthesized on 3C-SiC(100) shows p-type carriers with sheet carrier concentration in the range between ~1.5 to 3.3 (±0.2) x 10^{13} cm^{-2}, mobility in the range of 30 to 84 (±2) $cm^2V^{-1}s^{-1}$ and sheet resistance between 6 and 11 (±1) kΩ/□ at 300 K. These values are in good agreement with results obtained using setup 2, an additional

setup with cryogenic capabilities (see Methods for details). As a comparison, the corresponding bare Si(100) substrate shows n-type conduction with sheet carrier concentration, mobility and sheet resistance of 1.0 (±0.2) x 10^{10} cm^{-2}, 1300 (± 10) $cm^2V^{-1}s^{-1}$, and 500 (± 3) kΩ/□, respectively. The 3C-SiC grown on Si(100) also indicates electrons as charge carriers and sheet carrier concentration of 2.0 (±0.2) x 10^{11} cm^{-2}, mobility of ~1700 (± 10) $cm^2V^{-1}s^{-1}$ and sheet resistance of ~20 (± 1) kΩ/□. The electron mobility of 3C-SiC(100) is in accordance with the expected values for 3C-SiC of thickness between 15 and 30 μm.[46]

Hall measurements at 300 K of the EG grown on the 3C-SiC(111) orientation also indicate p-type charges. The charge carriers in this EG show larger mobilities (144 – 330 (±2) $cm^2V^{-1}s^{-1}$), on average about 5 times higher than those of the EG on 3C-SiC(100) substrates, with sheet carrier concentrations of order of 10^{12} cm^{-2}, ~2-5 times smaller than EG on (100) oriented 3C-SiC/Si. The sheet resistances of the samples fall in the range between 2.5 to 10 kΩ/□. Again, as a comparison, the bare Si(111) substrate shows *p*-type conduction with sheet carrier concentration, mobility and sheet resistance of 7 (±0.2) x 10^{10} cm^{-2}, 340 (± 10) cm^2 V^{-1} s^{-1}, and 270 (± 10) kΩ/□, respectively. The 3C-SiC(111) grown on Si(111) exhibits hole type conduction and has sheet carrier concentration of 4.0 (±0.2) x 10^{11} cm^{-2}, mobility of ~250 (± 10) $cm^2V^{-1}s^{-1}$ and, sheet resistance of ~70 (± 3) kΩ/□. 3C-SiC/Si usually unintentionally n-type doped, but in this case, we find a p-type 3C-SiC/Si, which is attributed to the dissuaded carrier inversion effect discussed by Pradeepkumar et al.[30] which is indicative of an unstable p-n heterojunction. Nevertheless, since the 3C-SiC and Si are highly resistive, this does not affect the isolation of graphene on the SiC/Si. Note that the mean free path[47] estimated from the mobility and sheet carrier concentration values from Table 6-3 for EG on both 3C-SiC(100) and 3C-SiC(111) are within a 3 to 10 nm range.

Table 6-3 Hall measured transport properties at 300K. The errors represent the maximum variation of the values upon the current sweep from 1 to 10 μA.

	EG on 3C-SiC(100)			
sample	carrier type	sheet carrier concentration (±0.2) x 10^{13} cm^{-2}	mobility (±2) $cm^2V^{-1}s^{-1}$	sheet resistance (±1) k Ω/□
Sample 1	Holes	1.5	63	6
Sample 2	Holes	1.0	84	11
Sample 3	Holes	3.3	30	6
	EG on 3C-SiC(111)			
sample	carrier type	sheet carrier concentration (±0.2) x 10^{12} cm^{-2}	mobility (±2) $cm^2V^{-1}s^{-1}$	sheet resistance (±1) k Ω/□
Sample 1	Holes	3.3	330	6
Sample 2	Holes	4.6	144	9
Sample 3	Holes	7.0	305	2.5
Sample 4	Holes	3.3	330	6

Further, Figure 6-4b schematically shows the configuration used for sheet resistance measurements; note that all permutations are used to extract the sheet resistance data. Figures 6-4c and 4d show the temperature dependent sheet resistance behavior for EG/3C-SiC/Si, 3C-SiC/Si and the bare-Si substrates between 80 and 300 K for the (100) and (111) surfaces, respectively. The sheet resistance behavior of the EG samples can be clearly distinguished from that of the underlying 3C-SiC/Si and Si substrates by the weak temperature dependence (refer also to Figure 6-S6 for sheet resistance measurements down to 4 K). The sheet resistance data versus temperature also point out that the EG is covering continuously the underlying SiC/Si system. When the coverage is not continuous, this can be easily recognized through the strange temperature dependence of sheet resistance in Figure 6-S8a. Figure 6-4e shows temperature dependent mobility of EG/3C-SiC(100) and EG/3C-SiC(111). The mobility of EG grown on 3C-SiC(100) surface has a weak temperature dependence, gradually increasing after 200 K attaining ~30 $cm^2V^{-1}s^{-1}$ at 300 K. The weak temperature dependence of mobility of EG/3C-SiC(100) may be due to the absence of a buffer layer, consistent with the previous report by Speck et al. for EG on SiC.[10] On the other hand, the mobility of EG/3C-SiC(111), shows a sharp increase after 200K up to a value of ~375 $cm^2V^{-1}s^{-1}$ at 250 K and then decrease until ~330 $cm^2V^{-1}s^{-1}$ at 300 K. The negative temperature dependence of mobility

above 250 K for the EG/3C-SiC(111) may be related to the scattering process originating at the buffer layer – as reported for EG on 6H-SiC.[48]

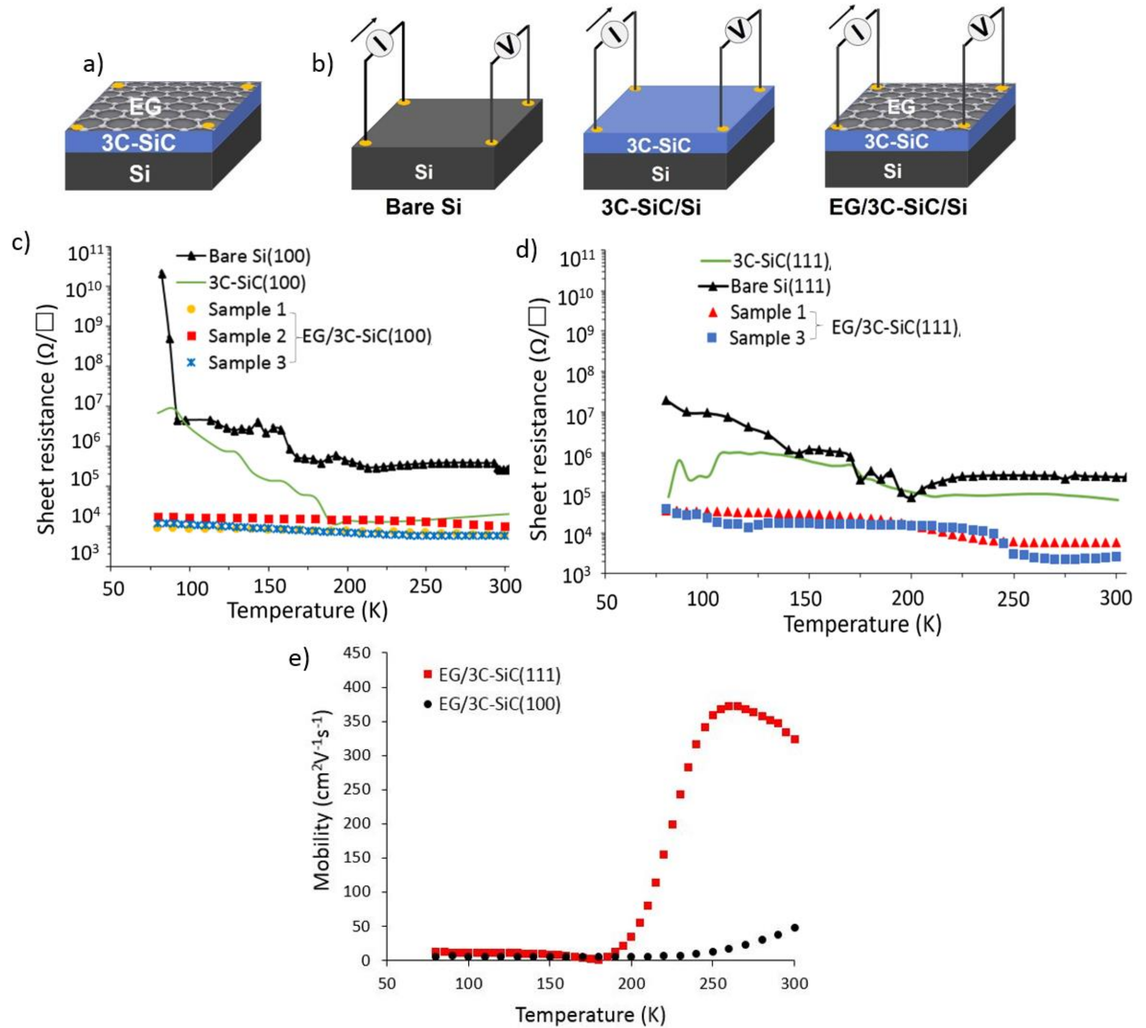


Figure 6-4: a) van der Pauw geometry with four-point InSn contacts. b) Schematics of vdP sheet resistance measurements on bare-Si, 3C-SiC/Si and EG/3C-SiC/Si. Temperature-dependent sheet resistance of c) EG/3C-SiC(100), 3C-SiC/Si(100) and bare-Si(100); (d) EG/3C-SiC(111) and 3C-SiC/Si(111) and bare Si(111) in the range between 80 and 300 K; e) mobility as a function of temperature in the range between 80-300K for EG/3C-SiC(100) and EG/3C-SiC(111).

Next, we compare the sheet carrier concentration and mobility values of the EG given in Table 6-3 with those of the EG grown on 4H- and 6H- SiC from Tedesco et al.[7] Figure 6-5 shows that the mobility and sheet carrier concentration of the EG on 3C-SiC(100) and 3C-SiC(111) follow a very similar power law dependence to those of EG grown on the Si-face of 4H- and 6H- bulk SiC wafers from Tedesco et al.[7] The inverse power law model has been reported as an intrinsic property of epitaxial graphene,[7] and is also in agreement

with additional reports of EG on SiC(0001).[49] We will elaborate further on the relevance of this model for this study.

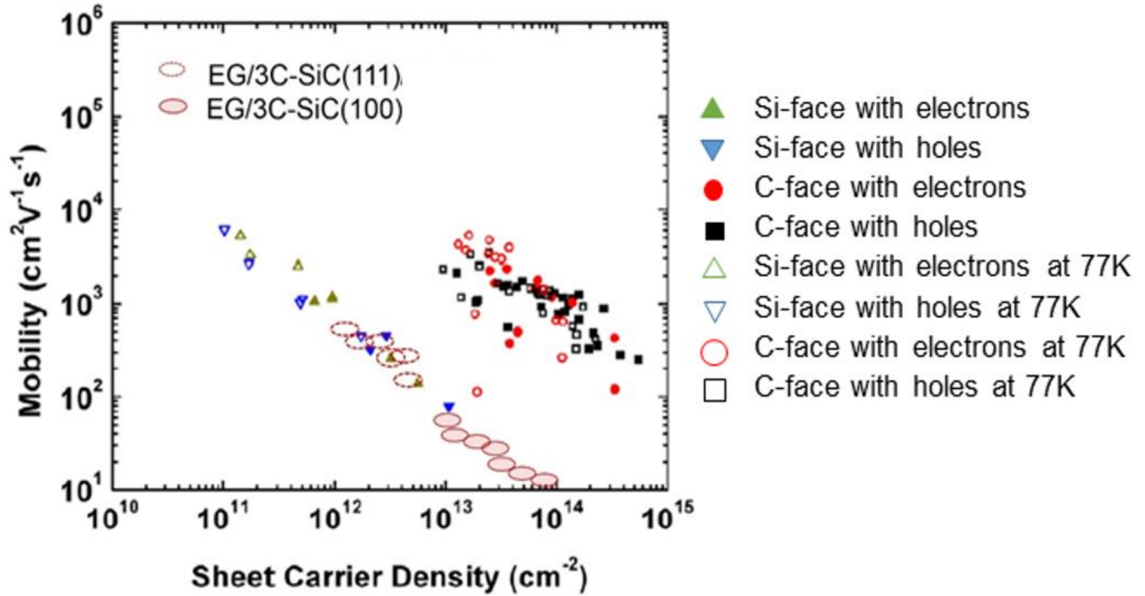


Figure 6-5: Mobility and sheet carrier density data of the EG on 3C-SiC/Si (Table 3) are here superimposed and remarkably in line with those of EG on Si-face of bulk 4H- and 6H-SiC 16 x 16 mm^2 semi-insulating substrates at 300 and 77 K from Tedesco et al.[7] Reprinted from ref 7. Copyright from 2009 AIP publishing.

First of all, the combined and de-identified mobility versus sheet carrier concentration data for EG on Si-face SiC from Tedesco et al.[7], together with the values for the EG on 3C-SiC from this work, can be fitted as a whole with good confidence with the same power law, indicating a common conductivity of about ~3 ± 1 (e^2/h), value close to the expected minimum quantum conductivity of graphene - see Figure 6-S7b. The general nature of the power law in Figure 6-5 also indicates that the tunability of the transport properties of epitaxial graphene is constrained, i.e. when the carrier concentration increases, the mobility has to decrease accordingly.

The power law trend exhibited in Figure 6-5 could be due to short-range weak disorder potentials dominating the carrier scattering process, then one expects a conductivity independent of the carrier density, and then the mobility would be inversely proportional to the sheet carrier concentration.[50] Yet we note that the power law trend could also be explained by long-range scattering behaviour[51-52] where the dopants are considered as the main scattering impurities. For this latter case, conductivity would be a constant[52] and, again, the mobility would be inversely proportional to the sheet carrier concentration. We

note that the latter model would be consistent with interface interaction (i.e. the silicates) dominating the scattering process and, hence, the EG transport properties.[53]

The significant difference in the mobility range between the graphene grown on Si-face and C-face of hexagonal SiC wafers was reported as due to the distinct levels of graphene-substrate interactions on Si-face and C-face surface terminations by Norimatsu et al.[11] For the graphene on Si-terminated SiC(0001) surface, a strong covalent bond interaction of buffer layer with the substrate was reported, whereas the graphene on the C-face of SiC(0001) forms only a weak interaction with the substrate.[11,54] The significantly lower mobility values at higher sheet carrier concentrations of the EG on 3C-SiC(100) may imply that the graphene possesses a much stronger substrate interaction than even the EG on Si-face of hexagonal SiC wafers. We had previously measured the substrate interaction of the EG on 3C-SiC(100), using the double cantilever beam method (DCB).[55] This measurement has yielded an adhesion energy close to 6 J m^{-2}, which is ~3 times larger than the adhesion energy of the graphene to the Cu foils, PMMA and SiO_2 (transferred), as measured with DCB.[55] The adhesion evaluation of EG on bulk SiC with the DCB is extremely challenging and no corresponding value is found in the literature. An attempt to quantify the adhesion of the interface between the EG and the bulk SiC was made by Kim et al.,[56] based on the stress -delamination theory - which hence cannot be compared with the values from the double cantilever method, as the latter is based on a sandwiched configuration and pure opening mode.[57] Another attempt to measure the adhesion energy of EG on Si-face of SiC was made by Wells et al. who reported a value of ~3 J m^{-2} - estimated from the graphene pleat defects.[58] In the case of EG on 3C-SiC(111), even if the interface silicates are present, the mobility and carrier concentration values of EG are close to those on Si-face of SiC. This may indicate that EG on 3C-SiC(111) possesses similar adhesion energy as that of the EG on Si-face SiC.

The epitaxial graphene grown via thermal decomposition on hexagonal SiC or 3C-SiC/Si substrates are generally n-type doped.[12-13, 59] The EG in this work shows a p-type conduction. It is well known that the presence of electron affinitive oxygen at the interface attracts charge carriers from the graphene.[9, 60] The charge transfer from EG into the oxides at the EG/3C-SiC interface is hence likely responsible for the p-type doping in this epitaxial graphene. Even though an equivalent amount of substrate oxidation is detected by the XPS in the case of EG/3C-SiC(111), the presence of buffer layer between graphene and 3C-SiC(111) may screen the substrate interaction of EG.[61-63] *i.e.* charge transfer from

graphene to top-oxidized SiC could be reduced up to some extent by having a buffer layer between epitaxial graphene and the substrate. Consequently, we believe the buffer layer screening is the reason behind the lower sheet carrier concentration and improved mobility of EG/3C-SiC(111) compared to the EG/3C-SiC(100) which does not possess a buffer layer. Although the carrier mobilities of the EG/3C-SiC/Si appear overall lower than those of EG grown on hexagonal SiC wafers,[7] the sheet resistance values are comparable. The sheet resistance of EG/3C-SiC(100) from this work varies from 10 to 30 kΩ/☐ at 4 K (Figure 6-S6a) down to 6 to 11 k Ω/☐ at 300 K (Figure 6-S6a and Table 6-3), and the sheet resistances of EG/3C-SiC(111) varies from ~100 kΩ/☐ at 4 K (**Figure S6b**) down to 2.5 to 10 kΩ/☐ at 300 K (Figure 6-S6b and Table 6-3). Berger et al.[3] reported square resistances of 1.5 k to 225 kΩ/☐ at 4 K for patterned graphene films on SiC. Another work from the same research group[64] have reported for EG on Si-face SiC, sheet resistance in the similar range which is ~ 1.5 to 4.2 kΩ/☐ at 300 K and ~2 to 7 kΩ/☐ at 4 K, respectively. This indicates that the EG grown on 3C-SiC/Si via the alloy-mediated approach has a sheet resistance/conductivity comparable to that of EG on SiC (0001) substrates. In addition, we note that the convergence to the same inverse power law trend observed in Figure 6-5 further confirms that all of the samples of EG/3C-SiC(100), EG/3C-SiC(111), as well as the EG on bulk SiC (Si–face) have roughly the same sheet resistance, which is close to the expected maximum quantum resistance for graphene (see also Figure 6-S7a).

This may appear surprising as the grain sizes for EG on bulk SiC are at least 100 nm and upwards,[14, 65-66] whereas the estimated grain size for the EG/SiC/Si is significantly smaller (Table 6-2). We also observe from Table 6-2 that the grain sizes of both EG/3C-SiC(100) and EG/3C-SiC(111) are comparable, yet their mobilities differ by at least a factor of 5. Finally, we note that the estimated mean free path of the carriers in the EG/SiC/Si (3-10 nm) is much smaller than its grain size as assessed via Raman (Table 6-2). This all suggests that the grain sizes are not the determining factor in the transport properties of the graphene.

Finally, we also note that the variation of number of layers for the EG/SiC/Si samples does not affect the measured transport properties (see also SI, section 3), which is expected for turbostratic stacking of graphene.[35]

To assess the effect of substrate interaction on the transport properties of graphene, we have used an atomistic model for EG on 3C SiC(111), 2x2 graphene cell on top of √3 x √3 R cos 30 SiC supercell. This model has been widely used for studying EG on 6H-SiC(0001).[60] Our first principle calculations for the EG/3C-SiC(111) show that an EG sample on top of a buffer layer with no silicates yields an n-type doped graphene (see Figure 6-S9) - similarly to the EG obtained through the more conventional thermal decomposition method on 6H-SiC(0001)[3, 12-13, 59] and ARPES –reported values of EG on 3C-SiC(111).[21, 25, 27] The alloy–mediated synthesis used in this work induces oxidation on the surface of the SiC layer as demonstrated by the XPS data. In the case no buffer layer was present (at 100 % oxidation – 5 O atoms per unit cell), our calculations show p-type graphene due to charge transfer from the graphene to interfacial oxides – see Figure 6-6a. We propose that a similar charge transfer arises for the case of EG/3C-SiC(100), with no buffer. In the case of the EG/3C-SiC(111), where we observe a buffer layer with XPS, we have modified the calculation to reflect the presence of a buffer taking into account a 60 % surface oxidation level. We find from these calculations that EG/3C-SiC(111) is also p-type, although its Fermi level is closer to the Dirac point as compared to the calculation for EG/3C-SiC(100) – see Figure 6-6b.

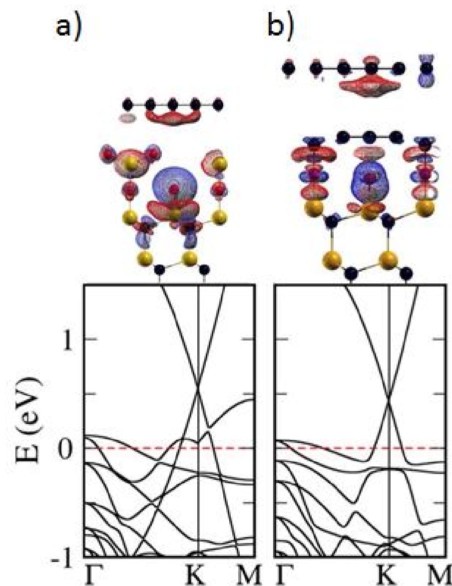


Figure 6- 6: Electronic band structure for EG on 3C-SiC with top-substrate demonstrating the effect of substrate interaction on transport properties of epitaxial graphene. (a) Absence of buffer layer (at 100 % oxidation) increase a charge transfer from graphene into the oxidized substrate with a Fermi level at 0.55 eV below the Dirac point – can be linked to the case of EG/3C-SiC(100); (b) presence of buffer layer (at 60 % oxidation)

between EG and substrate reduce the charge transfer from graphene giving Fermi level at 0.43 eV below the Dirac point (E_F closer to E_D) - reflecting the case of EG/3C-SiC(111). Si, C, and O atoms are shown in yellow, black and red spheres. The upper panels show the charge density plot. The blue color mesh represents electron accumulation, and red color mesh indicates electron depletion.

The electronic band structures in Figures 6-6a and b show Fermi level positions below the Dirac point at ~0.55 eV and ~0.43 eV, respectively. The p-type sheet carrier concentrations estimated from the Fermi levels[21] are ~1.8 x 10^{13} cm^{-2} in the first case - which can be related to that of the EG/SiC(100)/Si and ~1.1 x 10^{13} cm^{-2}, ~1.6 times smaller, in the second case which can be linked to the EG/3C-SiC(111)/Si. This trend is similar to the observed Hall transport properties reported in Table 6-3 and it supports that the difference observed in the transport properties of EG/3C-SiC(100) versus EG/3C-SiC(111) is attributed to the presence/absence of buffer layer resulting in a weaker/stronger EG-substrate interaction.

In an attempt to further reduce the substrate interaction on the transport properties of EG/3C-SiC(111), we performed H-intercalation. The intercalation was performed at conditions similar to Koch et al.[15] (see Methods for more details). Table 6-4 reports the Hall measured transport properties at 300K for EG/3C-SiC(111) (sample 4) before and after the H-intercalation.

Table 6- 4 Hall characteristics at 300K before and after H-intercalation of EG/3C-SiC(111) (sample 4)

	EG on 3C-SiC(111)	
	before H-intercalation	after H-intercalation
Carrier type	Holes	Holes
Sheet carrier concentration (cm^{-2})	3.3(±0.2) x10^{12}	2.8(±0.2) x10^{12}
Mobility ($cm^2V^{-1}s^{-1}$)	330(±2)	350(±2)
Sheet resistance (Ω/□)	6k±1k	6k±1k

Mammadov et al.[12] and Sirikumara et al.[60] reported that H-intercalated EG on 3C-SiC(111) substrates show n-type carriers as passivation of dangling bonds with hydrogen modifies electronic density in graphene when graphene attracts charges from passivated H-atom. However, the observed extent of reduction in sheet carrier concentration after the H-intercalation of EG/3C-SiC(111) in Table 6-4 is only minor.

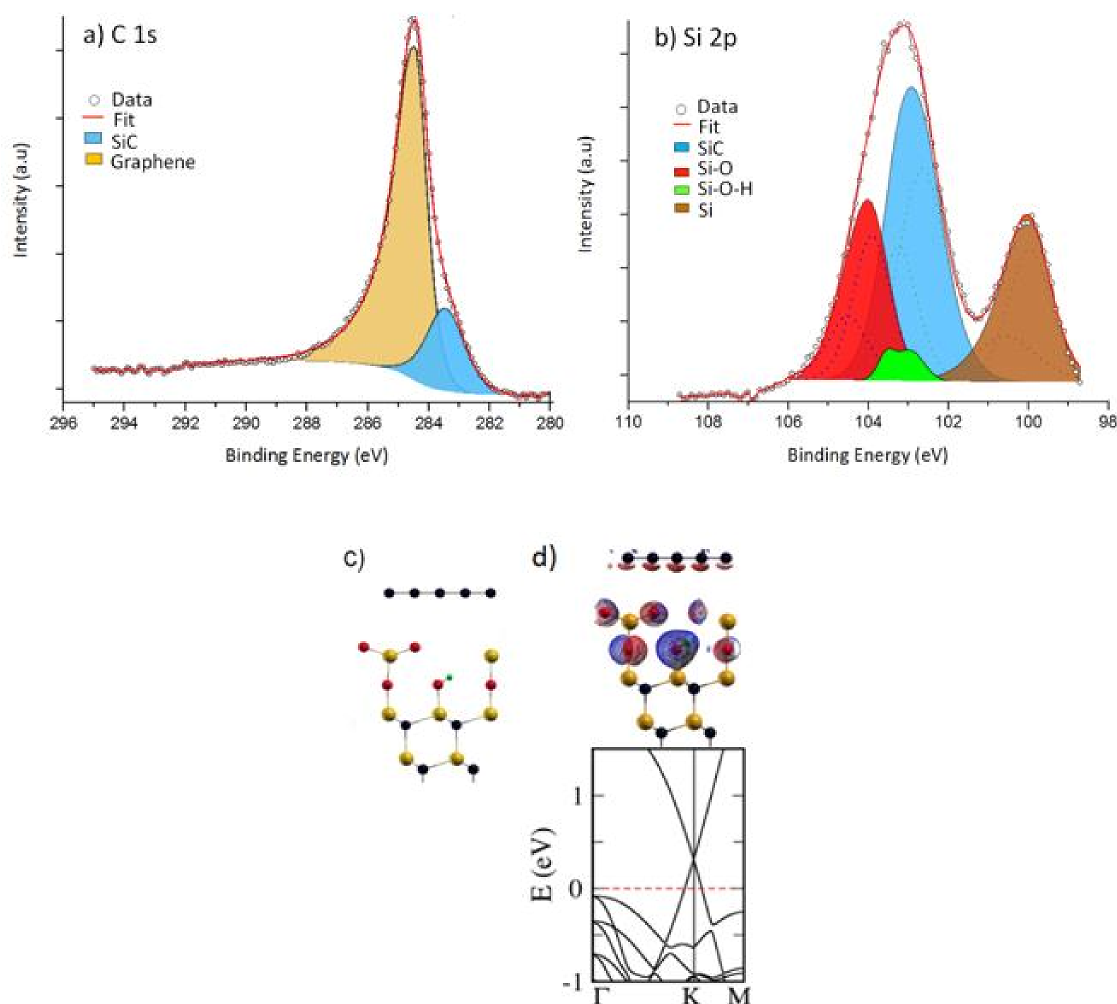


Figure 6-7: (a) and (b) XPS C 1s and Si 2p core-level spectrum for a selected EG/3C-SiC(111) (sample 4) after H-intercalation. (c) and (d) schematic and electronic band structure for H-intercalated EG on top-oxidized substrate 3C-SiC(111) with Fermi level at 0.32 eV, below the Dirac point (E_D-E_F) indicating p-type conduction. The upper panel in (d) shows the charge density plot. Si, C, O and H atoms are shown in yellow, black, red and green spheres. The blue color mesh represents the electron accumulation, and red color mesh indicates electron depletion.

Figures 6-7a and b show the C 1s and Si 2p spectra of the EG/3C-SiC(111) after H-intercalation.

C 1s spectra indicates that the H-intercalation process decouples the buffer layer from the substrate.[41, 61] The Si 2p spectrum shows the presence of Si-O bonds (102.5 eV) and additional Si-O-H bond at 102 eV. We believe that the charge transport properties of the graphene even after decoupling the buffer layer did not show considerable improvement (Table 6-4) because the interface was still occupied by the silicates (Figure 6-7b**)**, which dominates the charge transport in the EG. The effect of the H-intercalation on transport

properties has also been analyzed with the help of DFT calculation (Figures 6-7c and d). The schematic shows that after H-intercalation, the buffer layer in EG/3C-SiC(111) is decoupled, and the Fermi level for the EG is at 0.32 eV below the Dirac point. The estimated sheet carrier concentration is ~6 x 10^{12} cm^{-2}, which points implies a 2-fold expected reduction in the sheet carrier concentration from the non –intercalated EG/3C-SiC(111) (~1.1 x 10^{13} cm^{-2}, Figure 6-6b).

6.4 Conclusions

Epitaxial graphene on 3C-SiC on silicon is of high technological relevance and has been pursued extensively over the last decade to allow for seamless integration with silicon technologies. Graphene on silicon could indeed extend the scope of silicon technologies to enable advanced electronics, including low-loss high-frequency active and passive devices, to on-chip nanophotonics and low-loss plasmonics. All of the aforementioned applications require a very detailed understanding and control of the transport properties of graphene on the silicon pseudosubstrate. However, the lack of large–scale graphene continuity over the 3C-SiC and an unstable 3C-SiC/Si heterointerface had limited adequate characterization and modelling of the electronic transport properties of EG on 3C-SiC on silicon wafers.

In this work, we overcome such issues and describe the transport properties of epitaxial graphene grown over large areas via an alloy-mediated graphitization approach on highly resistive 3C-SiC formed on high resistivity silicon wafers, and also show the corresponding density-functional theory models. Despite a defective substrate (3C-SiC/Si),[36] the polarized Raman measurements demonstrate that the graphene synthesized via the alloy-mediated approach maintains an epitaxial relationship with the substrate; hence using the terminology epitaxial graphene is justified.

We find that the epitaxial graphene is strongly p-type doped as a result of the interaction with the substrate that comprises of silicates generated at the EG/SiC interface by the alloy–mediated epitaxial synthesis, as opposed to the n-type doping found for EG from thermal decomposition of SiC. The estimated charge mean free path for the EG/3C-SiC/Si wafers ranges between 3 - 10 nm, which is a much smaller length than the estimated grain size of the EG. This further evidence indicates that in all cases the transport behavior of the EG on 3C-SiC/Si is dominated by the interaction with its substrate. The charge transport properties of the alloy-mediated EG are surprisingly close to those of EG on

SiC, particularly, showing comparable sheet resistance values and the same inverse power model dependence of the EG sheet carrier concentration and mobility – although the grain sizes are different in both cases. The power law dependence further demonstrates that the carrier transport in EG is determined by the substrate interaction and is affected by the presence of silicates at the interface. The EG on 3C-SiC(111) has a buffer layer, whereas EG on 3C-SiC(100) lacks a buffer layer, consistent with the literature. DFT calculations are consistent with the carrier type and charge transfer from interfacial silicates. The number of layers is in the range between 3 and 7 for EG on both 3C-SiC(100) and 3C-SiC(111), and are turbostratic - in contrast with the EG formed by Si sublimation. The transport properties are independent of the number of layers which is consistent with turbostratic nature of the graphene.

Research group of de Heer reported that the multilayer EG with a silicate layer on top of the SiC enables the tunnelling process through the silicate/Schottky layer/barrier that could be utilized for the development of transistors.[67] In addition, Padilla et al. studied the tunability of graphene/metal-intercalated silicate/SiC and demonstrated the possibility for electronic band engineering based on graphene/SiC interface.[68] The transport measurements of EG/3C-SiC indicates that engineering the interface is key to the control of the transport properties of the EG. We conclude that a renewed attention to more efficient intercalation processes could very well enable epitaxial graphene on silicon substrates for superior integrated functionalities ranging from nanoelectronics to nanophotonics.

ASSOCIATED CONTENT

*S Supporting Information

Additional figures, calculations and analysis

6.5 Materials and Methods

Sample preparation: synthesis of EG on cubic silicon carbide on silicon: We use un-intentionally doped, NOVASiC 3C-SiC films with 500 nm thickness, epitaxially grown on 235 μm thick highly resistive (resistivity >10 kΩcm) Si(100) as well as Si(111) substrates.[30] Prior to graphene growth, the 3C-SiC/Si substrate wafers are diced into 1.1 x 1.1 cm^2 coupons and cleaned in acetone and isopropanol. The alloy-mediated graphene growth was performed via a solid source method using nickel and copper as catalysts and

annealing at 1100°C, 5 x 10^{-4} mbar as reported elsewhere.[20] After annealing, the samples undergo a wet Freckle (~20 hrs) etch to remove the metal residues and silicides. Subsequent characterizations are performed after the wet etch step.

Electrical characterization: Four-point InSn ohmic contacts are soldered onto the EG/3C-SiC/Si samples and representative bare high-resistivity Si substrates and 3C-SiC/Si coupons. We measured the room temperature carrier concentration, carrier mobility, and sheet resistance by performing Hall effect measurements at a magnetic field of 0.55 T and a current range of 1 to 10 μA using an Ecopia Hall effect measurement system, HMS-5300.[30] Transport measurements are performed on at least 10 samples each of EG/3C-SiC(100) and EG/3C-SiC(111) (selected samples are reported in Table 6-3). The errors represent the maximum variation of the values upon the current sweep. The temperature dependent sheet resistance measurements of the graphene samples as well as the 3C-SiC and Si substrates are performed between 80 and 300 K using the Ecopia HMS-5300 system. Equivalent low temperature sheet resistance measurements in the range between 4 and 300 K are also performed on selected samples using a Quantum Design Physical Property Measurement System (PPMS) (referred to as "setup 2") at Monash University. The source current is applied through a Keithley 2400 SourceMeter, which recorded the voltage simultaneously.

Raman spectroscopy: Confocal Raman mapping at room temperature was performed using a Renishaw InVia spectrometer operating at 532 nm laser line using a 50X objective with a spot size of approximately 1 μm and incident power of 17 mW.[20] We used a silicon sample as reference (~520 cm^{-1}) for calibration. A 30 μm × 30 μm area is mapped using a 0.20 μm step size, and 0.1 s integration time at the center of each sample. The Raman D, G and 2D bands of the graphene are examined and the D to G band intensity ratio (ID/IG), G and 2D band peak positions, G and 2D band FWHM were calculated by fitting the maps across the 30 μm × 30 μm area. The error values represent the standard deviation of the ID/IG ratios, measured at five different sites.

Polarized Raman spectroscopy: Polarized Raman measurements were obtained using the 514 nm laser with a motorized rotating λ/2 waveplate (30° steps), and a polarizer on the scattered beam as an analyzer. The Raman Si peak, 3C-SiC TO peak and the graphene[38] 2D to G peak intensity ratio were measured and plotted as a function of the angle (β) between the light polarization of the analyzer and the incident laser. Note that

G peak has no polarization dependence due to the symmetry.[38] The graphene 2D peak is normalized to the G peak in order to minimize laser power fluctuations, as generally reported in the literature.[38]

X-ray Photoelectron Spectroscopy: X-ray photoelectron spectroscopy (XPS) measurements were performed using a Specs PHOIBOS 100 Analyzer operated with a Mg Kα X-ray source (Mg anode operated at 10 keV and 10 mA) at 3 mm spot size. The data was calibrated to the C1s peak present at 284.6 eV to compensate for any surface charging. The photoelectron peak areas were calculated after background correction by Shirley procedure.[41]

Density Functional Theory Calculations: All calculations were performed using the Quantum Espresso package.[69] At least 8 Å of vacuum space was included to decouple the structure from its periodic image. We used a 12 x 12 x 1 Monkhorst Pack grid to sample the Brillouin zone, refer to Sirikumara et al.[60] for more details on the calculations. In order to study the silicate layer of 3C-SiC, we used the model we proposed for oxidized 4H SiC(0001) surface, which was later used to study the epitaxial graphene on oxidized 4H-SiC(0001) surface.[60, 70] The model has an R3 repeating cell of 3C-SiC (111) surface. Si_2O_3 ad-layer is chemically bound to 2 out of 3 surface Si atoms of the R3 cell via Si-O-Si bonds. Therefore, this model is also known as the Si_2O_5 model. In this work, we refer to this structure, Si_2O_5 on 3C-SiC(111), as an oxidized monolayer. Atomic configuration of 3C-SiC(111)/Si_2O_5 is fully optimized using the first principles Density Functional Theory Calculations. A 2 x 2 graphene cell is placed on the fully optimized R3 cell and the geometry is again optimized.

H-intercalation: H-intercalation is performed by annealing the EG/3C-SiC/Si sample in Thermo Scientific Lindberg/Blue M Mini-Mite™ furnace in 1 atm of ultra-pure hydrogen at 860°C for 75 min. Similar conditions are also reported by Koch et al.[15] for quasi-freestanding bilayer epitaxial graphene on SiC(0001). The furnace was left to cool down at room temperature and the sample was removed once the furnace reached room temperature.

ASSOCIATED CONTENT

*S Supporting Information

Additional figures, calculations and analysis

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The manuscript was written through the contributions of all authors.

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6.7 Supporting Information (SI)

p-type Epitaxial Graphene on Cubic Silicon Carbide on Silicon for Integrated Silicon Technologies

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6.7.1 Raman characterisation

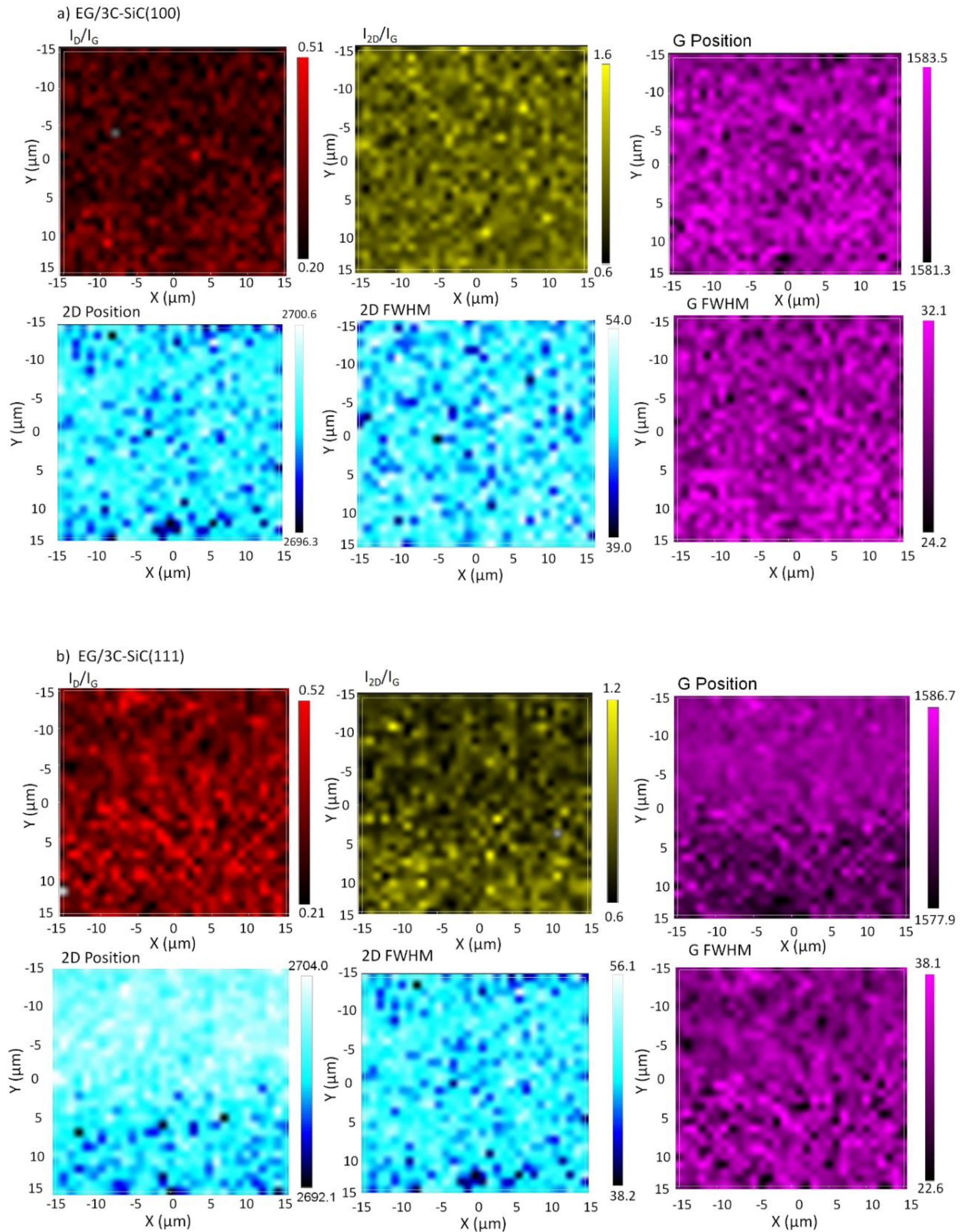


Figure 6-S1: Raman maps of I_D/I_G and I_{2D}/I_G ratios, G and 2D positions, G and 2D FWHM across 30 µm x 30 µm for a) EG/3C-SiC(100) –sample 1; b) EG/3C-SiC(111) – sample 2. (Selected samples from Table 6-2)

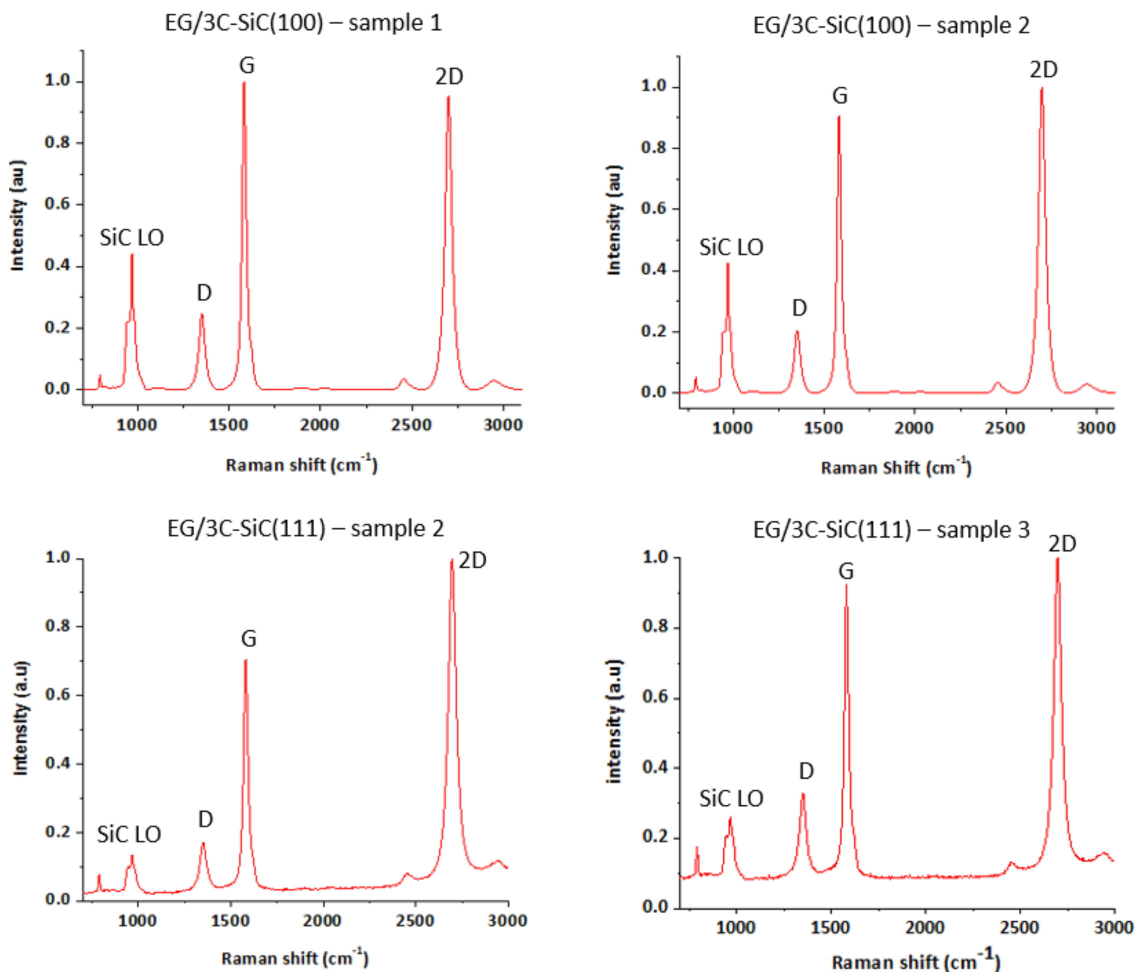
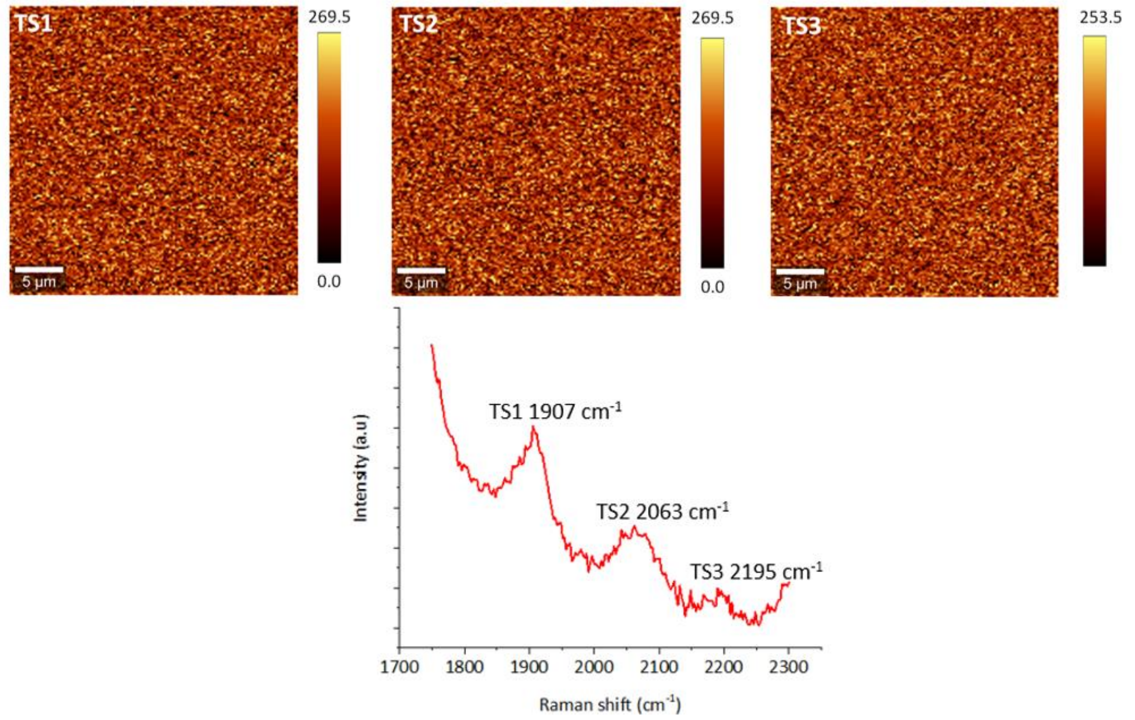


Figure 6-S2**:** Average Raman spectra (30 µm × 30 µm) of EG/3C-SiC(100) and EG/3C-SiC(111) across 30 µm x 30 µm using 532 nm laser (selected samples from Table 6-2)

The Raman maps in Figure 6-S1 are representative results found on EG/3C-SiC(111) and EG/3C(100) samples (specifically, sample 1 and 2 as shown in Table 2) and show that the important quantities (I_D/I_G, I_{2D}/I_G, G and 2D position, G and 2D FWHM) vary in limited range with no obvious pattern. The presence of 2D peaks demonstrate that the samples are graphene. These quantities and associated variations are dependent upon the starting 3C-SiC thickness and the synthesis conditions. A representative average spectrum shown in Figure 6-S2, taken from the examples shown in Figure 6-S1, can be used to make a rough estimate of the intensities of the various components with respect to each other.



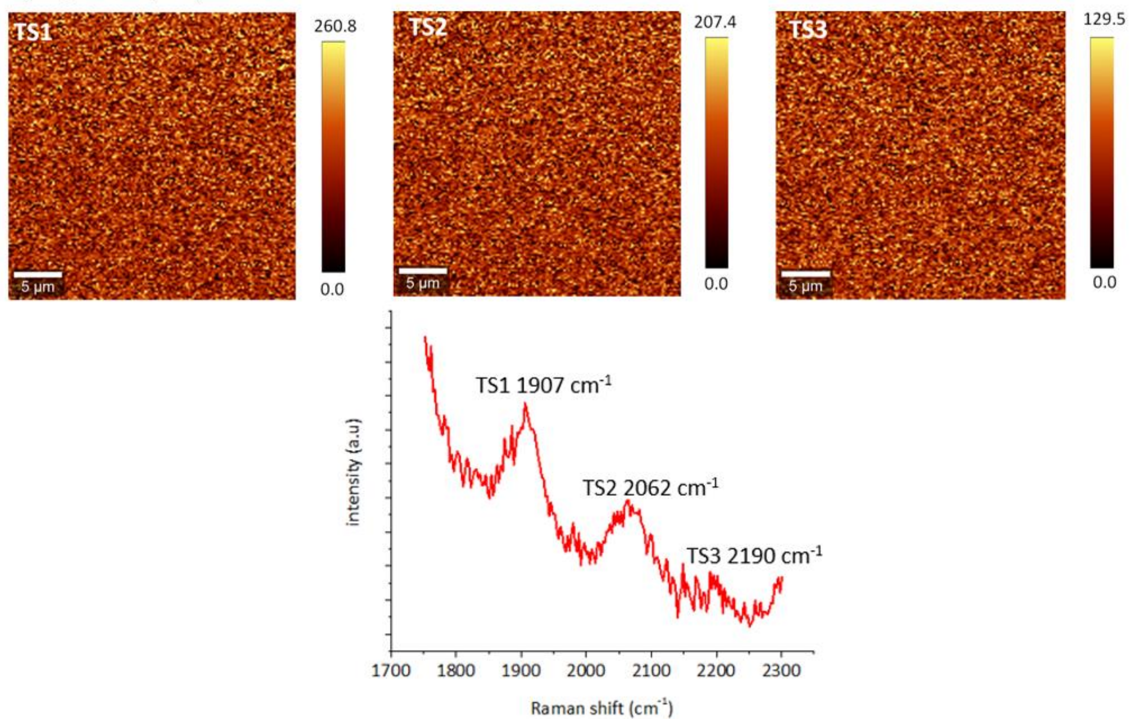
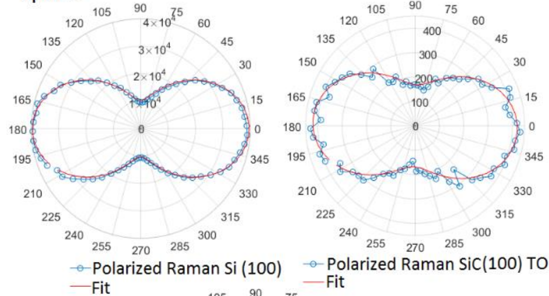


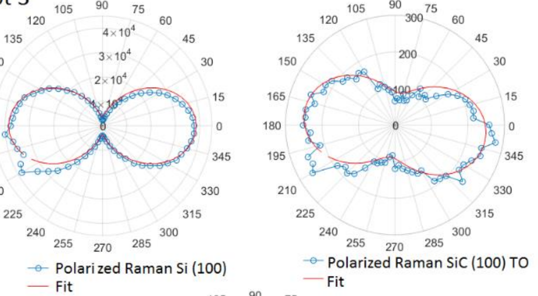
Figure 6-S3: 30 µm x 30 µm Raman peak intensity maps of TS1, TS2 and TS3 turbostratic in-plane[1] modes identified between 1700 and 2300 cm^{-1} in the Raman spectra of (a) EG/3C-SiC(100) – sample 3; (b) EG/3C-SiC(111) – sample 1 (selected samples from Table 6-2)

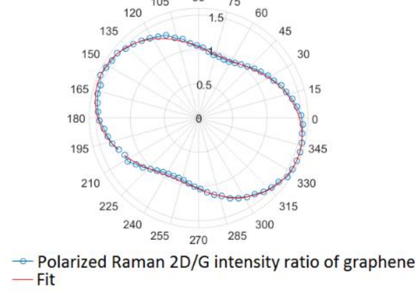
a) EG/3C-SiC(100)

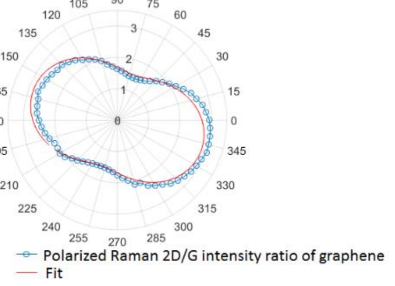
Spot 2



Spot 3

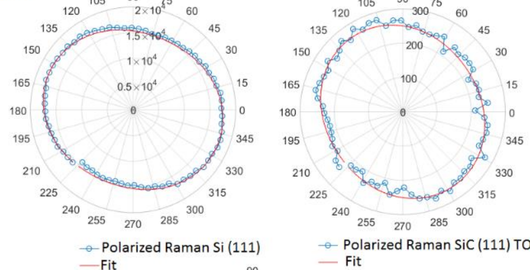




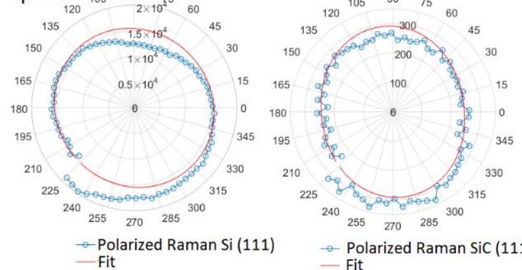


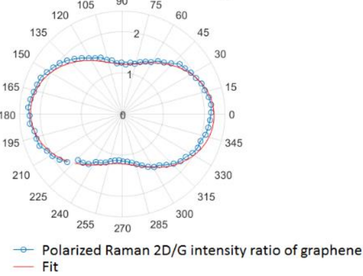
b) EG/3C-SiC(111)

Spot 2



Spot 3





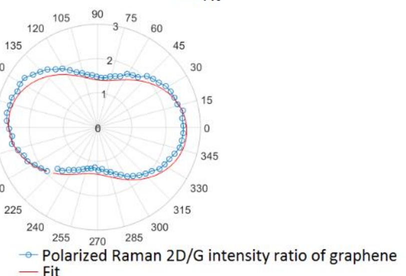


Figure 6-S4: Polar plots of Si peak intensity, 3C-SiC TO peak intensity and the ratio of the 2D to G peak intensity as a function of the relative angle for (a) EG/3C-SiC(100); (b) EG/3C-SiC(111) across 2 different spots separated by 1.5 mm.

6.7.2 Graphene layer thickness estimation using XPS data

The graphene layer thickness can be estimated using C 1s spectra and comparing graphene component to SiC component. The intensity of these components are calculated using the area under their peaks. Using the equation below the graphene layer thickness **t** can be estimated.

$$\frac{N_{Gr}}{N_{SiC}} = \frac{T(E_{Gr})\rho' \, C_{Gr} \, \lambda' \, (E_{Gr})[1 - \exp\left(\frac{-t}{\lambda' \, (E_{Gr})}\right)]}{T(E_{SiC})\rho \, C_{SiC} \, \lambda \, (E_{SiC}) \, \exp\left(\frac{-t}{\lambda \, (E_{SiC})}\right)} . F$$

Where N_{Gr} and N_{SiC} are the intensity of graphene and SiC components in C 1s spectra. ρ is the atomic density, λ is the inelastic mean free path, E represents the kinetic energy of the photoelectrons, F is the photoelectron diffraction correction factor, T is the transmission function of the analyzer and C is the differential cross-section. The superscript ' refers to graphene values. For further information regarding this method, refer to Gupta et al.[2] and Rollings et al.[3]

We calculate the kinetic energies for the photoelectrons by subtracting the binding energy from the incoming photon energy. Here, we are comparing the graphene and SiC components in C1s spectra, therefore, the effect of the transmission function of the and different cross-sections are negligible.[2] The photoelectron diffraction correction factor is considered to be 1.[2] The inelastic mean free path used is based on the TPP-2M formula.[4] Here we used $\rho_{Gr} = 2.26$ g cm^{-3}, $\rho_{SiC} = 3.22$ g cm^{-3}, $\lambda_{Gr} = 2.7$ nm and $\lambda_{SiC} = 2.26$ nm to calculate **t**. The number of graphene layers have been calculated by dividing **t** by the single graphene layer thickness of 0.335 nm.[5]

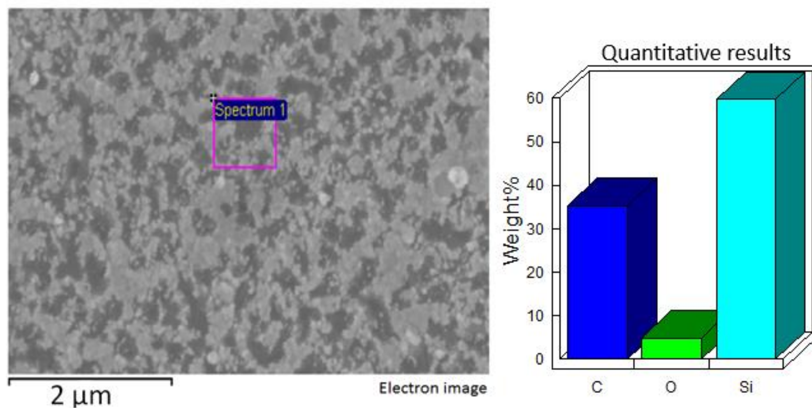
Table 6-S 1: Calculated number of layers for the graphene grown on 3C-SiC(100), 3C-SiC(111) and H-intercalated EG/3C-SiC(111) based on the XPS C1s spectra.

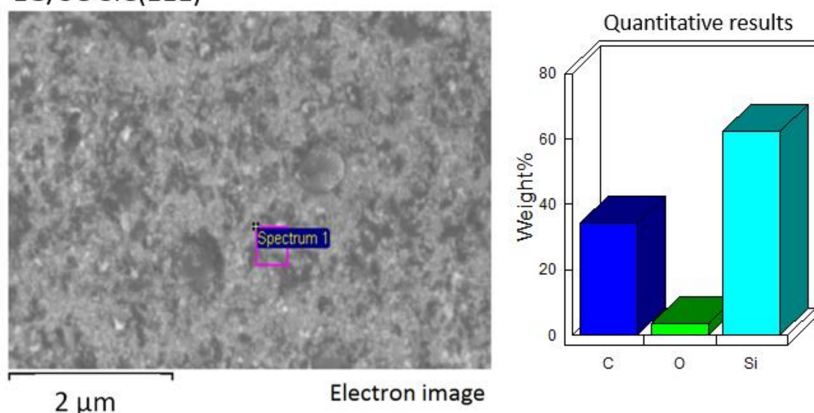
Substrate	Number of graphene layers
3C-SiC(100)/Si(100) (sample 3)	~7
3C-SiC(111)/Si(111) (sample 1)	~3
After H-intercalation on EG/3C-SiC(111) (sample 4)	~7

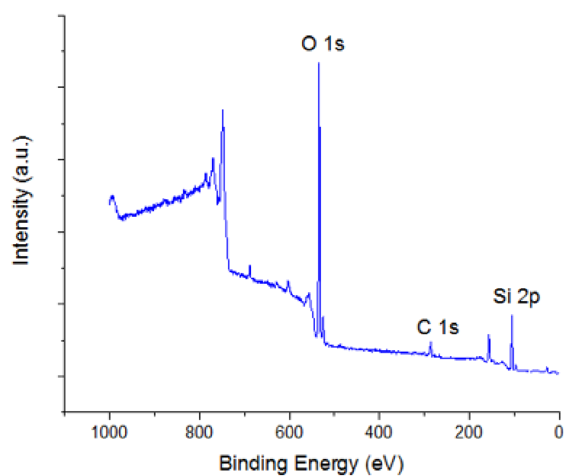
6.7.3 Effect on the number of layers of graphene on the transport properties

The C1s spectra in Figure 6-3a estimates ~7 graphene layers for EG/3C-SiC(100). From the C 1s spectra in Figure 6-3b, the number of graphene layers is estimated to be ~3 for EG/3C-SiC(111) – sample 1 in Table 6-3. C 1s spectra after H-intercalation of EG/3C-SiC(111) (see Figure 6-7) estimates ~7 layers for the EG. Note that the decoupling buffer layer is expected to increase the number of layer by one. Transport properties of EG/3C-SiC(111) before H-intercalation is shown for Sample 4 in Table 6-3. Comparison of transport properties between sample 1 and 4 in Table 6-3 (for EG/3C-SiC(111)) shows that transport properties are independent of the number of layers for turbostratic epitaxial graphene.

6.7.4 Testing the presence of Ni/Cu metal or metal oxides in the graphene







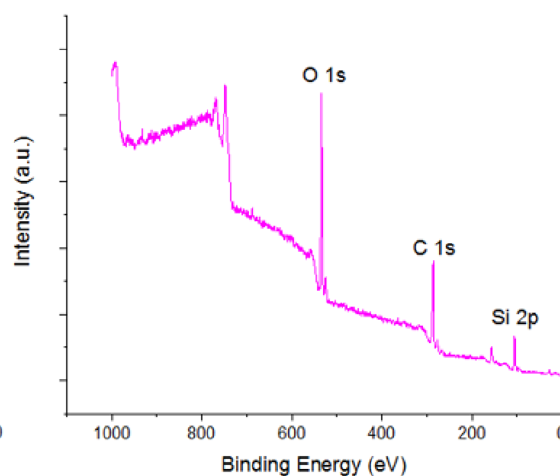


Figure 6-S 5: (a) EDX - no evidence for the presence of nickel or copper metal/metal oxides in the graphene. An Oxford INCAx-sight EDX spectroscopy attached to the FESEM was used to evaluate the elemental composition of the EG at 10 kV; (b) XPS survey spectra of EG/3C-SiC(100) and EG/3C-SiC(111) from Figure 6-3. No XPS peaks for nickel/copper metal or metal oxides between the ranges of 850-960 eV.[6, 7]

6.7.5 Electrical characterization

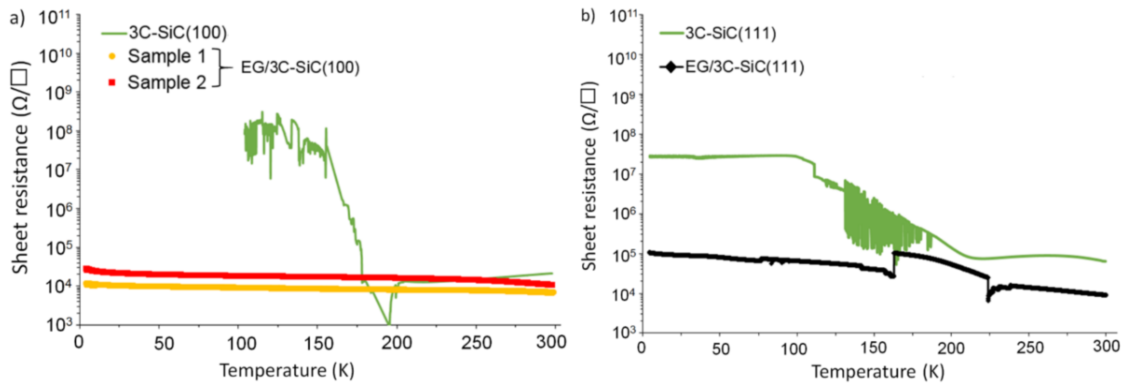


Figure 6-S6: Temperature dependent sheet resistances (a) EG/3C-SiC(100), 3C-SiC(100) measurement interrupted at lower temperatures; (b) EG/3C-SiC(111) and 3C-SiC(111) in the range between 4K and 300K.

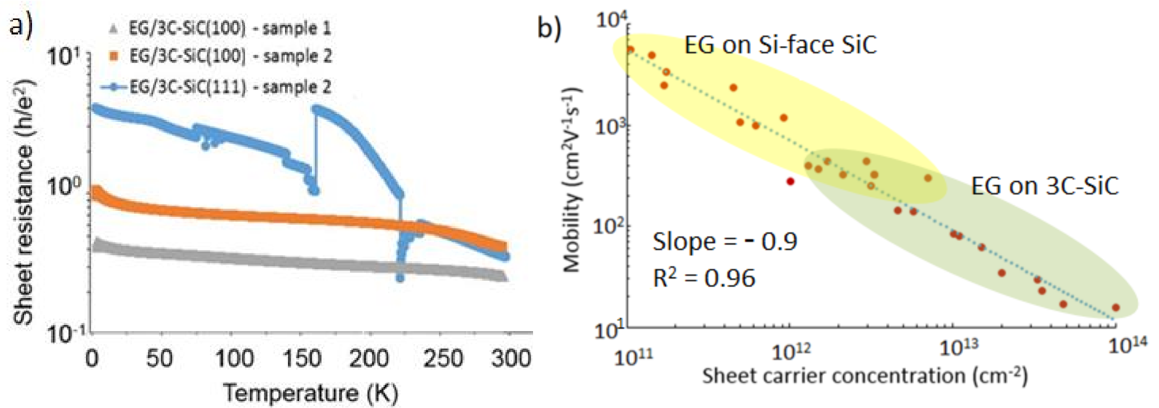


Figure 6-S7: (a) Sheet resistance (plotted in units of quantum resistance, h/e^2) as a function of temperature for EG/3C-SiC(100) and EG/3C-SiC(111). (Same samples as reported in Table 6-2 of the manuscript); (b) Graph showing the combined and de-identified mobility versus sheet carrier concentration data for EG on Si-face SiC from literature,[8] together with the values for the EG on 3C-SiC from this work. These data as a whole can be fitted with good confidence with the same power law, indicating that they share a common conductivity of about ~3 ± 1 (e^2/h).

6.7.6 Verifying the coverage of EG on 3C-SiC(100)

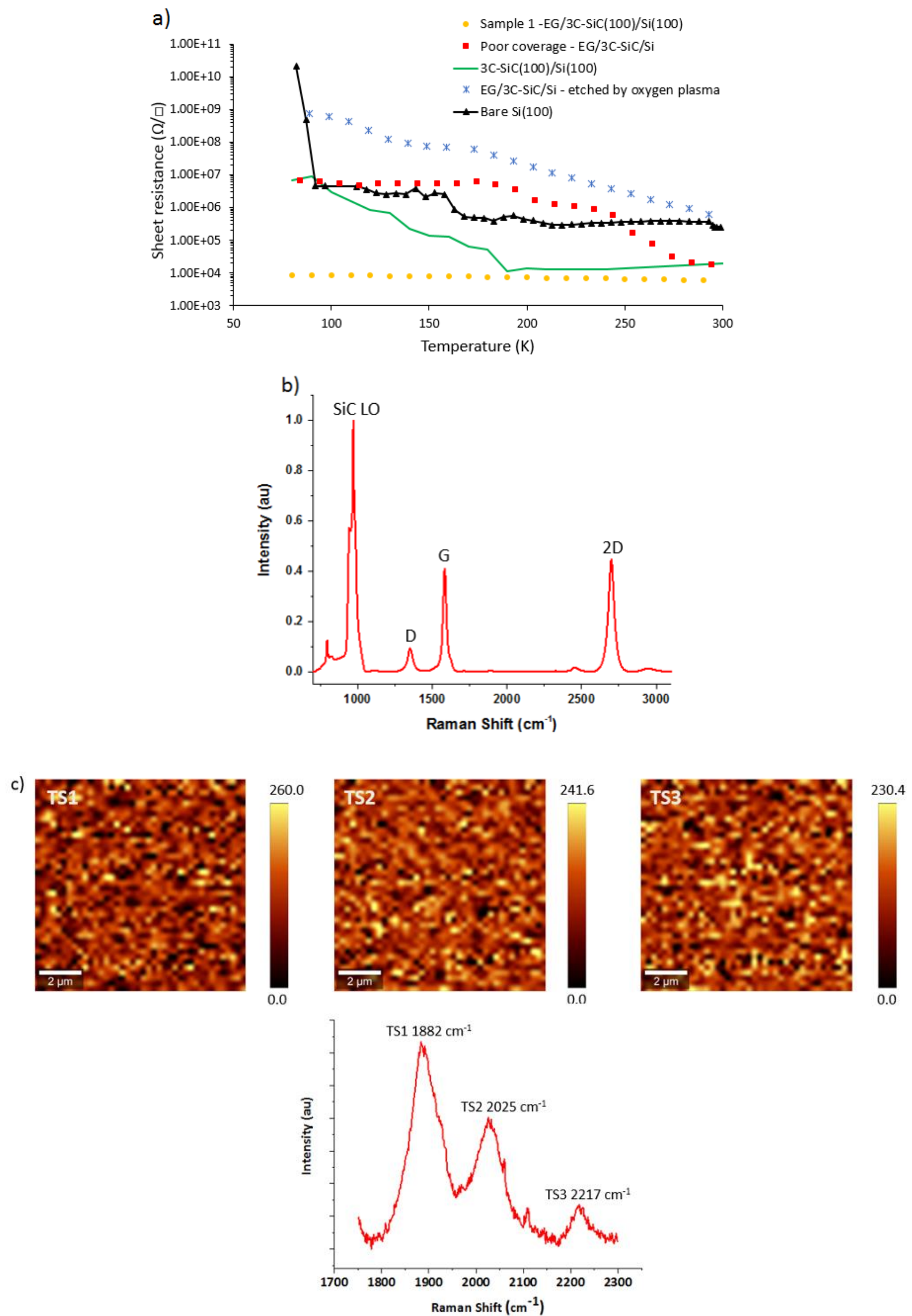


Figure 6-S8: a) (a) Temperature dependent sheet resistance for EG/3C-SiC(100), 3C-SiC(100), EG without full coverage on 3C-SiC/Si and EG etched via oxygen plasma (O_2 flow rate of 25 sccm at 150W); (b) average Raman spectra (30 µm × 30 µm) of EG

without full coverage on 3C-SiC(100) –SiC LO band intensity is substantially higher than 2D; (c) Raman peak intensity maps of turbostratic in-plane modes - TS1, TS2 and TS3 of the poor coverage EG/3C-SiC/Si.

In addition to the measurements in Figures 4c and d, Figure 6-S8a shows the sheet resistance behavior of an EG sample with uneven graphene coverage on 3C-SiC(100) (prepared under same growth conditions – sample non-uniformity may be related to unintentional variations in process parameters). Note that we have reported the presence of a considerable amount of oxidation at the top portion of the substrate after the graphitization process (XPS Si 2p spectra in Figure 6-3a and b). As a result, the sheet resistance of the EG/SiC/Si without full coverage is much larger than that of the as-grown 3C-SiC. These values are close to those for an EG/SiC/Si exposed to oxygen plasma for the complete removal of the graphene. Figure S8b show the average Raman mapping spectra of a non-uniformly distributed EG grown on top of 3C-SiC(100) indicating a prominent SiC LO band compared to the 2D band. Note that samples reported in Tables 6-2 and 3 have the SiC LO peak intensity much smaller than corresponding 2D bands, see Figure 6-S2. Figures 6-S8c shows the peak intensity maps of TS1, TS2 and TS3 turbostratic in-plane modes identified in between 1700 and 2300 cm^{-1} for the poor coverage EG/3C-SiC/Si.

6.7.7 Density Functional Theory Model

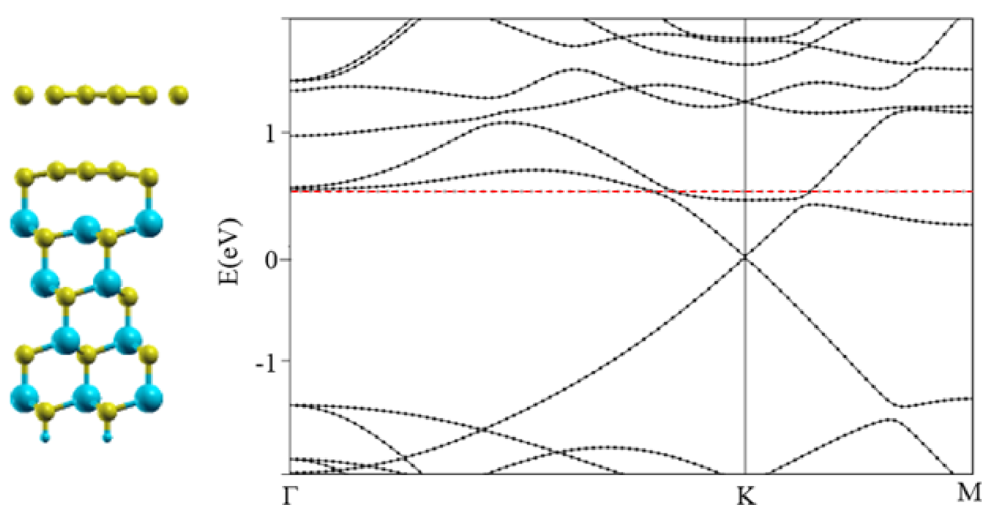


Figure 6-S9: Density functional theory calculation results: schematic of the structure calculated (left, carbon is yellow, Si is blue and 3C-SiC structure was used – see main text for details) and electronic band structure for EG on 3C-SiC(111) (right) with no

oxidation at the EG/3C-SiC interface and Fermi level at 0.59 eV (dotted line) above the Dirac point resulting n-type sheet carrier concentration of 2 x 10^{13} cm^{-2}.

6.7.8 References

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Chapter 7: Conclusions and future works

Direct integration of graphene onto semiconducting substrates have great potential, for example, for high-frequency FETs, solar cells, and heat sink structures for the removal of thermal dissipation.[1-5] Epitaxial graphene on 4H- and 6H- SiC wafers is currently a well-advanced technique in terms of growth as well as the establishment and control of transport properties, with ballistic conduction already demonstrated by the pioneering group of De Heer at Georgia Tech, USA.[3, 6-7] However, SiC wafers are limited in the available size (~3 inches) and are difficult to integrate with the current semiconductor technology and processess.[8] Since silicon is the most widely used material in the semiconductor industry, the establishment of epitaxial graphene process on silicon wafers would be highly beneficial.

The cubic silicon carbide has been identified as a potential pseudo-substrate for growing graphene directly on silicon wafers.[9] However, surprisingly, despite sustained research in this area over the past decade, the EG/3C-SiC/Si is currently not yet mature with plausible transport measurements for device applications. The state-of-the-art analysis shows that the prior attempts to measure the transport properties were using FET configurations[10-11] that are electrostatics and geometry dependent, and are affected by the substrate. No temperature-dependent Hall effect measurements were demonstrated yet over large areas. These were due to the non-uniform coverage of EG formed using the conventional approaches[12] and the problems associated with the SiC/Si junctions,[13] precluding reliable Hall measurements.

The scope of this thesis is to understand in detail what the current limitations of 3C-SiC/Si system are and establish for the first time the electronic transport characteristics of large –scale epitaxial graphene grown on cubic silicon carbide on silicon.

The key contributions of this thesis are;

1. Identification of a typically unstable electronic junction between the 3C-SiC and the silicon substrate, as reported in Chapter 4.

We find that the heterojunction between the 3C-SiC and Si is either non-existing or highly unstable such that severe electrical leakage or even plain shorting of the epitaxial silicon

carbide to the underlying silicon substrate is naturally present. This finding has critical consequences on the transport properties of the EG synthesized on the 3C-SiC/Si.

2. Explanation of the origin of the interface instability issue in the 3C-SiC/Si system, as demonstrated in Chapter 5.

We define and model the source of electrical instability of 3C-SiC-Si heterojunction and explain the electrical conduction mechanism in a typical heteroepitaxial 3C-SiC/Si by analysing the electrical behaviour of 3C-SiC films grown on different silicon substrates under different growth conditions. We explain the origin of the electrical instability through the diffusion of carbon atoms into the silicon matrix creating electrical active interstitial carbon traps during or after the heteroepitaxial growth of 3C-SiC. We also indicate different solutions to eliminate/minimize in-plane leakage, for example, by using a highly resistive Si as the substrate for 3C-SiC growth.

3. Transport properties of EG/3C-SiC/Si over large areas synthesized via an alloy-mediated graphitization method in Chapter 6

Based on the insights from Chapter 4 and 5, this thesis report the charge transport and electrical conduction in EG synthesized onto 3C-SiC on highly resistive Si substrates using an alloy-mediated approach. The alloy-mediated synthesis delivers uniform graphene coverage even if the 3C-SiC/Si surface is highly defective, which has been a significant challenge for the thermal decomposition approach.[12] Moreover, regardless of a defective substrate (3C-SiC/Si), the graphene formed via the alloy-mediated technique maintains an epitaxial relationship with the substrate –as observed from the polarized Raman measurements. This thesis also evaluate the temperature-dependent transport properties of graphene on 3C-SiC(100) and 3C-SiC(111) substrates, compare it with those of the well-established EG on bulk SiC and represent the corresponding density-functional theory models. The key points of the carrier transport analysis in EG/3C-SiC are;

a) Within the observed regime, the transport properties of the EG/3C-SiC are primarily dominated by the substrate interaction, resulting in a strongly p-type doped graphene (unlike the n-type graphene from thermal decomposition of SiC) due to the charge transfer from graphene into the silicates at the EG-SiC interface, –induced by the alloy-mediated synthesis.

b) The estimated mean free path of 3 - 10 nm is much smaller than the estimated grain size for the EG (55 to 87 nm). This further indicates that within the observed regime, the grain sizes are not the limiting factors, and the graphene-substrate interaction dominates the charge transport in EG/3C-SiC.

c) The charge transport in EG/3C-SiC follows a similar trend as the EG on bulk SiC wafers, with comparable sheet resistance values and the power-law relationship between the sheet carrier concentration and mobility –despite having much smaller grain sizes compared to EG on bulk SiC. The power-law relationship further indicates the substrate interaction of graphene.

d) In the case of EG/3C-SiC(111), a buffer layer is present whereas the buffer layer is absent in EG/3C-SiC(100). The buffer layer in EG/3C-SiC(111) reduces the charge transfer (substrate interaction) up to a certain extent, resulting in a lesser amount of p-type doping.

The important conclusion of the thesis is that within the observed regime, engineering of the graphene-substrate interface is more important than grain size in order to control the charge transport properties of epitaxial graphene.

As we can deduce from the observed power-law dependence of the sheet carrier concentration and the mobility of graphene, we confirm that this is a universal trend for the substrate-supported graphene. Thus, the control of the charge transfer/doping in EG is directly linked to the engineering of the surrounding surfaces, hence it is critical for the integration of graphene into future micro- or nanoelectronic devices.

The future directions of this research would include:

<u>Intercalation process</u>

An intercalation method using alternative elements to hydrogen would be a potential pathway to tailor the EG-3C-SiC interfaces and tune the transport properties of graphene. The aim here is to completely decouple the EG from its substrate.

<u>Top-gate graphene field-effect transistor</u>

Top-gated graphene field-effect transistors (GFET) can be fabricated using the alloy-mediated EG to vary the carrier concentration and investigate the ambipolar characteristics of the graphene at different gate voltages. These will enable to differentiate different scattering mechanisms affecting the charge transport in the EG. Figure 7-1 shows the schematic representation of a GFET.

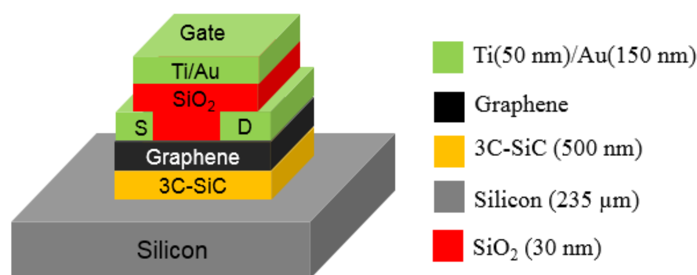

Figure 7-1: Cross-sectional view of a top-gate graphene FET.

7.1 References

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