UNIVERSITY OF TECHNOLOGY SYDNEY
Faculty of Engineering and Information Technology

LOW-COMPLEXITY DIGITAL MODEM DESIGN AND IMPLEMENTATION FOR HIGH-SPEED AERIAL BACKBONES

by

Hao Zhang

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Certificate of Authorship/Originality

I, Hao Zhang, declare that this thesis is submitted in fulfilment of the requirements for the award of PhD, in the School of Electrical and Data Engineering, Faculty of Engineering and Information Technology at the University of Technology Sydney.

This thesis is wholly my own work unless otherwise reference or acknowledged. In addition, I certify that all information sources and literature used are indicated in the thesis.

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ABSTRACT

Wireless communication technology is moving towards the integration of terrestrial networks with space networks. However, a number of grand technological challenges have to be overcome for such integration. This thesis addresses some of these challenges and develops efficient and effective solutions to successfully achieve a high-speed aerial backbone link.

The first challenge is the signal synchronization in presence of large carrier frequency offset (CFO). In this thesis, new methods for preamble-aided coarse timing estimation are investigated. Integrated with simple auto-correlation operation, CFO can be estimated and compensated for better frame synchronization in high-speed aerial backbone links. Moreover, the optimized algorithms can be implemented with low-complexity. Simulation result shows that the proposed method can capture tens of Mega Hertz CFO with rapid convergence.

The In-phase and Quadrature-phase (I/Q) imbalance is another significant factor which impacts on practical wideband wireless backbone systems. An effective algorithm is proposed to estimate I/Q imbalance with specially designed training sequence. After I/Q imbalance estimation, I/Q imbalance compensation is combined with channel equalization as well as sampling rate conversion to form the receiver filters of the system. Simulation result shows that the estimated receiver and transmitter imbalance coefficients are quite close to the true values and the joint algorithm can achieve the desired performance.

Analog-to-digital and digital-to-analog conversion devices for signals with very large bandwidth are not always available due to technical or cost issues. In this thesis, a dual pulse shaping (DPS) transmission scheme is proposed, which can achieve full Nyquist rate transmission with only a half of the sampling rate for each of the two data streams. The condition for cross-symbol interference free transmission is derived and validated for two classes of ideal complementary Nyquist pulses. Structures of the DPS transmitter and receiver are described and low-complexity

equalization techniques tailored to DPS are provided as well. The simulation results with two sets of practical dual spectral shaping pulses verify the effectiveness of the proposed scheme.

Finally, the design and implementation of a high-speed low-complexity digital modem for wireless communications at 0.325 terahertz (THz) are presented. The requirements, architecture and signal processing modules of the system are described. Some key strategies are applied to ensure the proposed low complexity algorithms can be implemented in real-time field-programmable gate array (FPGA) platform. The digital modem implementation and the integrations with IF modules and RF frontend are described and the experimental results of them are provided.

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Patent

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Abbreviation

3GPP - Third generation partnership project

A/D - Analog-to-digital conversion

AWGN - Additive white Gaussian noise

ASIC - Application specific integrated circuit

BER - Bit error rate

BRAM - Block random-access memory

CLB - Configurable logic block

CFO - Carrier frequency offset

CP - Cyclic prefix

CSI - Cross-symbol interference

CRC - Complementary raised-cosine

D/A - Digital-to-analog conversion

DFTs - Discrete Fourier transforms

DPS - Dual pulse shaping

DSP - Digital signal processing

EVM - Error vector magnitude

FDM - Frequency domain multiplexing

FEC - Forward error coded

FF - Flip-flop

FFT - Fast Fourier transform

FPGA - Field-programmable gate arrays

FTN - Faster-than-Nyquist

GbE - Gigabit Ethernet

Gbps - Gigabit per second

GEO - Geostationary Earth orbit

Gsps - Giga samples per second

HDL - Hardware description language

HTS - High-throughput satellite

IDFT - Inverse discrete Fourier transform

I/Q - In-phase and quadrature-phase

IP - Intellectual property

IoT - Internet of thing

ISI - Inter-symbol interference

ISTN - Integrated space and terrestrial network

LDPC - Low density parity check

LEO - Low Earth orbit

LO - Local oscillator

LOS - Line-of-sight

LS - Least square

LNA - Low noise amplifier

LSB - Lower signal band

LTE - Long term evolution

LUT - Look-up table

MAC - Medium access control

MEO - Medium Earth orbit

MHz - Mega Hertz

ML - Maximum likelihood

MMSE - Minimum mean square error

mm-wave - Millimetre wave

NRZ - Non-return-to-zero

OFDM - Orthogonal frequency-division multiplexing

ORCRC - Odd root complementary raised-cosine

PAPR - Peak-to-average power ratio

PCS - Physical coding sub-layer

PHY - Physical layer

PMA - Physical medium attachment

PMD - Physical medium dependent

PN - Pseudo noise

QAM - Quadrature amplitude modulation

RAM - Random-access memory

RC - Raised-cosine

RCRC - Root complementary raised-cosine

RF - Radio frequency

ROM - Read-only memory

Rx - Receiver

RRC - Root raised-cosine

RZ - Return-to-zero

SC - Single carrier

SC-FDE - Single carrier frequency domain equalization

SPS - Single pulse shaping

SRC - Sampling rate conversion

SNR - Signal to noise ratio

THz - Terahertz

Tx - Transmitter

UAS - Unmanned aircraft system

UAVs - Unmanned aerial vehicle

USB - Upper signal band

ZF - Zero forcing

Nomenclature and Notation

Bold capital letters denotes matricess.

$(.)^H$ denotes matrix conjugate and transpose.

$tr\{.\}$ denotes the trace of a matrix.

$\|.\|^2$ stands for the squared Frobenius norm of a matrix.

$E\{.\}$ denotes expectation.