UNIVERSITY OF TECHNOLOGY SYDNEY
Faculty of Engineering and Information Technology

LOW-COMPLEXITY DIGITAL MODEM DESIGN AND IMPLEMENTATION FOR HIGH-SPEED AERIAL BACKBONES

by

Hao Zhang

A Thesis Submitted
in Partial Fulfillment of the
Requirements for the Degree

Doctor of Philosophy

Sydney, Australia

2019

Certificate of Authorship/Originality

I, Hao Zhang, declare that this thesis is submitted in fulfilment of the requirements for the award of PhD, in the School of Electrical and Data Engineering, Faculty of Engineering and Information Technology at the University of Technology Sydney.

This thesis is wholly my own work unless otherwise reference or acknowledged. In addition, I certify that all information sources and literature used are indicated in the thesis.

This document has not been submitted for qualifications at any other academic institution.

This research is supported by the Australian Government Research Training Program.

Signature: Production Note: Signature removed prior to publication.

Date: 10/02/2020

ABSTRACT

Wireless communication technology is moving towards the integration of terrestrial networks with space networks. However, a number of grand technological challenges have to be overcome for such integration. This thesis addresses some of these challenges and develops efficient and effective solutions to successfully achieve a high-speed aerial backbone link.

The first challenge is the signal synchronization in presence of large carrier frequency offset (CFO). In this thesis, new methods for preamble-aided coarse timing estimation are investigated. Integrated with simple auto-correlation operation, CFO can be estimated and compensated for better frame synchronization in high-speed aerial backbone links. Moreover, the optimized algorithms can be implemented with low-complexity. Simulation result shows that the proposed method can capture tens of Mega Hertz CFO with rapid convergence.

The In-phase and Quadrature-phase (I/Q) imbalance is another significant factor which impacts on practical wideband wireless backbone systems. An effective algorithm is proposed to estimate I/Q imbalance with specially designed training sequence. After I/Q imbalance estimation, I/Q imbalance compensation is combined with channel equalization as well as sampling rate conversion to form the receiver filters of the system. Simulation result shows that the estimated receiver and transmitter imbalance coefficients are quite close to the true values and the joint algorithm can achieve the desired performance.

Analog-to-digital and digital-to-analog conversion devices for signals with very large bandwidth are not always available due to technical or cost issues. In this thesis, a dual pulse shaping (DPS) transmission scheme is proposed, which can achieve full Nyquist rate transmission with only a half of the sampling rate for each of the two data streams. The condition for cross-symbol interference free transmission is derived and validated for two classes of ideal complementary Nyquist pulses. Structures of the DPS transmitter and receiver are described and low-complexity

equalization techniques tailored to DPS are provided as well. The simulation results with two sets of practical dual spectral shaping pulses verify the effectiveness of the proposed scheme.

Finally, the design and implementation of a high-speed low-complexity digital modem for wireless communications at 0.325 terahertz (THz) are presented. The requirements, architecture and signal processing modules of the system are described. Some key strategies are applied to ensure the proposed low complexity algorithms can be implemented in real-time field-programmable gate array (FPGA) platform. The digital modem implementation and the integrations with IF modules and RF frontend are described and the experimental results of them are provided.

Acknowledgements

First of all, I would like to express my gratitude to my supervisor Prof. Xiaojing Huang for his continual support and encouragement of my study and PhD research. From employment as a casual staff member in 2015 to undertaking a PhD under him in 2016, I have been grateful for his patient guidance during my journey.

I would also like to thank my co-supervisor Prof. Jay Guo for sharing his valuable experience in support of my research, and I also want to thank A/Prof. Jian Andrew Zhang for his guidance and practical advice in my study period.

Keith Bengston, David Humphrey and Joseph Pathikulangara taught me the finer points of software and firmware design during my time at CSIRO. I am grateful for their advice with difficult technical problems.

Along my path I had many excellent mentors: Dr. Peiyuan Qin, Dr. Can Ding, Dr. Ting Zhang, Dr. Shenghong Li, Dr. Wei Lin, Dr. He Zhu, Dr. Hang Li and Dr. Tom Wang. Collaborating with them has broadened my horizons.

The example of my colleagues Anh Tuyen Le, Yijiang Nan, Shulin Chen, Haihan Sun and Hongyang Zhang provided inspiration that helped me to overcome many difficulties.

Last but not least, I would like to express my gratitude to my family: my father Sumin Zhang, my mother Meiying Guo and my older brother Fei Zhang for their love and wholehearted encouragement. To my loving, encouraging and patient wife Jieqiong Zhang, without whom none of this would have happened: your faithful support during the long process of undertaking a PhD has made all this possible.

Hao Zhang

August, 2019

List of Publications

Journal Papers

J-1. **Hao Zhang**, Xiaojing Huang, Jian Andrew Zhang and Y. Jay Guo, "Dual Pulse Shaping Transmission and Equalization for High-Speed Wideband Wireless Communication Systems", submitted to IEEE Transactions on Circuits and Systems I: Regular Papers.

Patent

P-1. Xiaojing Huang, Y. Jay Guo, Jian (Andrew) Zhang and **Hao Zhang**, "Dual Pulse Shaping Transmission System and Method," AU2018900096, filed on 12 January 2018.

Conference Papers

C-1. **Hao Zhang**, Xiaojing Huang, and Y. Jay Guo, "A 20 Gbps Digital Modem for High-Speed Wireless Backhaul Applications," presented at the 2017 IEEE 85th Vehicular Technology Conference (VTC2017-Spring), Sydney, Australia, 4 - 7 June 2017.

C-2. **Hao Zhang**, Xiaojing Huang, and Y. Jay Guo, "Low-Complexity Digital Modem Implementation for High-Speed Point-to-Point Wireless Communication," presented at the 18th International Symposium on Communications and Information Technologies (ISCIT2018), Bangkok, Thailand, 26 - 29 September 2018.

C-3. **Hao Zhang**, Xiaojing Huang, Jian Andrew Zhang and Y. Jay Guo, et al, "A High-Speed Low-Cost Millimeter Wave System with Dual Pulse Shaping Transmission and Symbol Rate Equalization Techniques," presented at the IEEE International Symposium on Circuits and Systems (ISCAS2019), Sapporo, Japan, 26-29 May 2019.

C-4. **Hao Zhang**, Xiaojing Huang, Ting Zhang, Jian Andrew Zhang and Y. Jay Guo, "A 30 Gbps Low Complexity and Real-Time Digital Modem for Wireless Communications at 0.325 THz," presented at the 19th International Symposium on Communications and Information Technologies (ISCIT2019), Ho Chi Minh City, Vietnam, 25 - 27 September 2019.

C-5. Xiaojing Huang, **Hao Zhang**, Jian Andrew Zhang and Y. Jay Guo, et al, "Dual Pulse Shaping Transmission with complementary Nyquist Pulses," presented at the 2019 IEEE 90th Vehicular Technology Conference (VTC2019-Fall), Honolulu, Hawaii, USA, 22-25 September, 2019.

Contents

Certificate ii

Abstract iii

Acknowledgments v

List of Publications vi

List of Figures xii

Abbreviation xvi

Notation xx

1 Introduction 1

1.1 Background 1

1.2 Challenges for ISTN System 3

1.3 Thesis Organization 6

2 Synchronization in Presence of Large CFO 9

2.1 Introduction and Literature Review 9

2.2 Training Sequence Design 11

2.3 Autocorrelation Implementation 13

2.4 Simulation Results 16

2.5 Conclusions 18

3 Joint I/Q Imbalance Compensation and Channel Equalization in SRC Receiver Filters 20

3.1 Introduction and Literature Review 20
3.2 System and Signal Models 23
3.3 I/Q Imbalance Compensation and Channel Equalization 25
3.4 Simulation Results 31
3.5 Conclusions 34

4 Dual Pulse Shaping Transmission System and Method 36

4.1 Introduction and Literature Review 36
4.2 DPS with Complementary Nyquist Pulses 39
4.2.1 Nyquist Theorem 39
4.2.2 Complementary Nyquist Pulses 39
4.2.3 CSI-Free Conditions for DPS Transmission 41
4.2.4 Ideal DPS Pulses 43
4.3 Equalization with Non-Ideal Pulses 47
4.3.1 System and Signal Models 48
4.3.2 Received and Equalized Signal Models 49
4.3.3 ZF Equalization 52
4.3.4 MMSE Equalization 55
4.4 Simulation Results 56
4.5 Conclusion 59

5 High-Speed Digital Modem Implementation for Wireless Communications at 0.325 THz 61

5.1 Introduction and Literature Review 61
5.2 System Description 63
5.2.1 System Requirements 63

5.2.2 System Architecture 64
5.2.3 Physical Layer Protocol 65
5.3 Signal Processing Modules 67
5.3.1 Transmitter Signal Processing 67
5.3.2 Receiver Signal Processing 67
5.4 Ethernet Interface 68
5.4.1 Functional Overview 68
5.4.2 Interfacing Radio PCS 69
5.4.3 Ethernet Interface Architecture 70
5.5 Implementation of Transmitter and Receiver Filters 71
5.5.1 Transmitter Filter 71
5.5.2 Receiver Filter 73
5.6 Key Strategies for Implementation on FPGA 74
5.6.1 FPGA 74
5.6.2 Key Strategies 78
5.7 Implementation Results 82
5.8 Experimental Results of Digital Modem 84
5.9 Integration with IF Module 85
5.9.1 Test Setup 85
5.9.2 Experimental Results 87
5.9.3 Channel Pre-equalization 89
5.9.4 BER Test with Real-Time Ethernet Traffic 92
5.10 Integration with RF Frontend 98
5.10.1 Architectures of THz RF Frontend 98

5.10.2 Test Setup and Experimental Results 99

5.11 Conclusion 101

6 Conclusions and Future Work **103**

6.1 Summary of Contributions 103

6.2 Future Work 105

6.2.1 Dealing with Nonlinear Channels 105

6.2.2 Achieving Higher-Speed Wireless Communication Systems . . 106

6.2.3 Reducing System Complexity 106

Bibliography **108**

List of Figures

2.1 Training sequence design. 13

2.2 Using autocorrelation for coarse timing. 13

2.3 CFO=30 MHz estimation under 8 dB SNR. 16

2.4 CFO=10 MHz estimation under 8 dB SNR. 17

2.5 BER performance (uncoded) with and without 10 MHz CFO. 17

2.6 Coarse timing detection probability and missed detection probability versus SNRs (CFO = 0). 18

2.7 Coarse timing detection probability and missed detection probability versus SNRs (CFO = 10 MHz). 19

3.1 Baseband block diagram of a point-to-point wireless communication system with the disclosed successive I/Q imbalance estimation and compensation. 23

3.2 Transmitter frame structure. 26

3.3 Flow graph of Rx I/Q imbalance estimation. 27

3.4 Linear filter structure for Rx I/Q imbalance compensation. 28

3.5 Flow graph of Tx I/Q imbalance estimation. 29

3.6 Receiver filter bank (upper) and polyphase filter (lower) structures. . 31

3.7 Estimated channel frequency response and refined channel after I/Q imbalance compensation. 32

3.8 Real (a) and image (b) parts of estimated and true Tx I/Q imbalance coefficients. 33

3.9 Real (a) and image (b) parts of estimated and true coefficients for Rx I/Q imbalance compensation filter. 33

3.10 BER performance (uncoded) with and without Tx or Rx I/Q imbalance compensation. 34

4.1 Waveforms of (a) RCRC pulses, (b) auto-correlation of RCRC pulses, and (c) cross-correlation of RRC and RCRC pulses. 45

4.2 Waveforms of (a) ORCRC pulses, (b) auto-correlation of ORCRC pulses, and (c) cross-correlation of RRC and ORCRC pulses. 47

4.3 Dual pulse shaping transmitter (a) and receiver (b). 48

4.4 Dual pulse shaping scheme 1. 57

4.5 Dual pulse shaping scheme 2. 58

4.6 Dual pulse shaping and RRC spectra. 58

4.7 PAPR comparison. 59

4.8 BER comparison (solid and dashed lines for ZF and MMSE equalization, respectively). 60

5.1 The backhaul system architecture with only half of the proposed 20 Gbps digital modem. 64

5.2 The frame structure of the physical layer protocol. 65

5.3 Transmitter signal processing diagram. 67

5.4 Receiver signal processing diagram. 68

5.5 MAC with two PHY channels. 69

5.6 The 66B bridge architecture. 70

5.7 The Ethernet interface architecture. 71

5.8 Structure of Tx filter for one sample. 72

5.9 Structure of addition tree for the real/imaginary part of one symbol. . 73

5.10 FPGA structure. 75

5.11 A slice of Virtex 7 FPGA. 76

5.12 Flexibility feature of FPGA. 78

5.13 Essential constraints applied to FPGA device. 82

5.14 Route result for the whole system. 84

5.15 Frequency tones used to check I/Q imbalance: tones at input to D/A (a) and tones at output from A/D (b). 85

5.16 16-QAM constellation obtained through external baseband loopback. 86

5.17 Structure of test setup. 86

5.18 A picture of 20 Gbps digital modem and test setup. 87

5.19 A picture of IF link with additive noise. 88

5.20 A picture of spectrum analyzer and switch driver. 88

5.21 Four channels of IF signal. 89

5.22 Frequency response of LSB2 (a), LSB1 (b), USB1 (c) and USB2 (d) channels. 90

5.23 Tx filters without pre-equalization. 91

5.24 Tx filters with pre-equalization of (a) real part and (b) imaginary part. 91

5.25 Real parts of Rx filters (a) without pre-equalization and (b) with pre-equalization. 92

5.26 Constellations (a) without pre-equalization and (b) with pre-equalization. 92

5.27 Spirent TestCenter user interface. 95

5.28 BER test results for individual channels with adjacent channel interference. 96

5.29 BER test results for all four channels. 97

5.30 Block diagram of THz communication system. 98

5.31 Frequency conversion from baseband to RF. 99

5.32 THz system and test setup. 100

5.33 Measured constellations under various loopback tests: Baseband (a), IF (b) and RF (c). 101

Abbreviation

3GPP - Third generation partnership project

A/D - Analog-to-digital conversion

AWGN - Additive white Gaussian noise

ASIC - Application specific integrated circuit

BER - Bit error rate

BRAM - Block random-access memory

CLB - Configurable logic block

CFO - Carrier frequency offset

CP - Cyclic prefix

CSI - Cross-symbol interference

CRC - Complementary raised-cosine

D/A - Digital-to-analog conversion

DFTs - Discrete Fourier transforms

DPS - Dual pulse shaping

DSP - Digital signal processing

EVM - Error vector magnitude

FDM - Frequency domain multiplexing

FEC - Forward error coded

FF - Flip-flop

FFT - Fast Fourier transform

FPGA - Field-programmable gate arrays

FTN - Faster-than-Nyquist

GbE - Gigabit Ethernet

Gbps - Gigabit per second

GEO - Geostationary Earth orbit

Gsps - Giga samples per second

HDL - Hardware description language

HTS - High-throughput satellite

IDFT - Inverse discrete Fourier transform

I/Q - In-phase and quadrature-phase

IP - Intellectual property

IoT - Internet of thing

ISI - Inter-symbol interference

ISTN - Integrated space and terrestrial network

LDPC - Low density parity check

LEO - Low Earth orbit

LO - Local oscillator

LOS - Line-of-sight

LS - Least square

LNA - Low noise amplifier

LSB - Lower signal band

LTE - Long term evolution

LUT - Look-up table

MAC - Medium access control

MEO - Medium Earth orbit

MHz - Mega Hertz

ML - Maximum likelihood

MMSE - Minimum mean square error

mm-wave - Millimetre wave

NRZ - Non-return-to-zero

OFDM - Orthogonal frequency-division multiplexing

ORCRC - Odd root complementary raised-cosine

PAPR - Peak-to-average power ratio

PCS - Physical coding sub-layer

PHY - Physical layer

PMA - Physical medium attachment

PMD - Physical medium dependent

PN - Pseudo noise

QAM - Quadrature amplitude modulation

RAM - Random-access memory

RC - Raised-cosine

RCRC - Root complementary raised-cosine

RF - Radio frequency

ROM - Read-only memory

Rx - Receiver

RRC - Root raised-cosine

RZ - Return-to-zero

SC - Single carrier

SC-FDE - Single carrier frequency domain equalization

SPS - Single pulse shaping

SRC - Sampling rate conversion

SNR - Signal to noise ratio

THz - Terahertz

Tx - Transmitter

UAS - Unmanned aircraft system

UAVs - Unmanned aerial vehicle

USB - Upper signal band

ZF - Zero forcing

Nomenclature and Notation

Bold capital letters denotes matricess.

$(.)^H$ denotes matrix conjugate and transpose.

$tr\{.\}$ denotes the trace of a matrix.

$\|.\|^2$ stands for the squared Frobenius norm of a matrix.

$E\{.\}$ denotes expectation.

Chapter 1

Introduction

1.1 Background

In the past several decades, the field of telecommunications has witnessed explosive growth in terms of technological advancement, which has a deep impact on many aspects of the human society[1–3]. There are three major types of telecommunication infrastructures: the Internet, mobile wireless systems and satellite systems. Since 1969, the Internet has grown into a global network with worldwide coverage and is the main force that revolutionized the information technologies. For mobile wireless systems, from the first-generation analog systems to the current fourth-generation and the future fifth-generation systems, mobile wireless communication networks have been through a series of major development involving upgrading and redesigning of system architectures, network protocols and transmission technologies [4]. Since the launch of the first artificial satellite in 1957, the number of satellites orbiting the Earth has been rapidly increasing. One or several of these satellites form an autonomous system [5] to provide some specific services, such as telecommunications, surveillance, remote sensing, positioning, navigation, and so on. Across different satellite systems, however, real-time resource and information sharing is typically very difficult because many satellite systems cannot provide consistent coverage in large areas due to limited illumination [6, 7].

The unmanned aircraft system (UAS) has attracted much attention recently, and various applications such as infrastructure inspection and environmental investigation are being studied [8–10]. However, a unmanned aircraft does not necessarily

fly within the radio wave coverage of a terrestrial network. Not only do the data acquired by the aircraft need to be collected, but also controlling an unmanned aerial vehicle is important. Therefore, high-speed wireless communication with a UAS is necessary [11].

With the acceleration of Internet of things (IoTs), smart home and virtual reality, the demand for anywhere and anytime broadband access capability is becoming more and more urgent [12]. At the same time, breakthroughs in machine to machine communications and sensor technology are being made [13]. In response to such communication demands, a satellite communication system called the high-throughput satellite (HTS) has been developed to further enable large-capacity communication [14–16]. The satellite-based Internet of things (S-IoT) with next generation HTS will play a vital role to address issues related to human life such as energy management, climate change, transportation, business logistics and building automation, etc [17, 18]. For HTSs currently in practical use, the allocation of communication resources is fixed, and hence cannot be efficiently performed on-demand among various users. Thus, the next generation HTSs need frequency flexibility so that they can flexibly assign communication resources according to the demands of IoT [18].

As one of the most important mobile satellite communication systems, space networks have attracted significant attention recently. Due to the excellent capabilities, such as high bandwidth, global coverage, and continuous services [19, 20], space networks have been widely used in emergency assistance, navigation, positioning and so on [21, 22]. With the explosion of future satellite services, it will be barely possible to deliver a number of applications and services only by satellite communications. Thus, there is an emerging trend to integrate space networks with terrestrial networks.

Mobile satellite communication is becoming an indispensable component of the

future integrated space and terrestrial network (ISTN) which is able to support the flexibility and seamless coverage for providing broadband and broadcast services in the air, at sea and in remote rural areas [23, 24]. The creation of ISTN is of critical importance for industries such as logistics, mining, agriculture, fishery and defense [25]. A high data rate space and terrestrial integrated global information and communications network is the fundamental infrastructure required to support the 21st century industry, economy and society. Currently, there are two parallel major international efforts in the field. The first one is the development of the 5G mobile communications networks that are expected to deliver up to 10 gigabit per second (Gbps) data rates and to be rolled out from 2020 [26]. The second major effort is the development of space communications networks. Based on the early geostationary Earth orbit (GEO) satellites, new space platforms include medium Earth orbit (MEO) and low Earth orbit (LEO) satellites, mini satellites known as CubeSats, and other aerial platforms including stratospheric balloons, airships and aircraft, unmanned aerial vehicles (UAVs), and high-altitude platform stations. In contrast to terrestrial networks, space networks provide communications coverage for people and vehicles. Clearly, the future information network must be one that integrates the space network with the terrestrial network seamlessly [23]. To do so, there are many grand challenges facing industry and the research community. A particularly important challenge is to provide up to hundreds of Gbps data rate wireless links between the space network and the terrestrial network which are referred to as the aerial backbones.

1.2 Challenges for ISTN System

To achieve high-speed aerial backbones for an ISTN, there are some challenges that are needed to be overcome due to the characteristics of satellite communications.

- *Challenge 1: Large Carrier Frequency Offset (CFO)*

  In mobile communications, the CFO is mainly caused by mismatch of the local oscillator at the receiving end. Meanwhile, the relative movement between the transmitter and receiver leads to a Doppler spread. An accurate estimation of large CFO is hard to achieve for the line-of-sight (LOS) satellite channel with low received signal to noise ratio (SNR). Hence, high performance synchronization method that operates under large CFO is required to improve the signal detection. The performance degradation resulting from synchronization errors is much more severe in low SNR scenarios. Moreover, by considering the power limitation of a satellite, a low-complexity synchronization under large CFO condition is needed to reduce the energy consumption and implementation cost.

- *Challenge 2: Power Efficiency*

  A satellite relies on solar power and, consequently, its energy is limited. As such, a transmitter is better to work near the saturation point of the high power amplifier. A transmitted signal with a large peak-to-average power ratio (PAPR) will seriously reduce the energy efficiency. With increasing demands for wireless services with high data rate, low cost transceivers are attractive for the implementation of wireless communication systems. However, it is quite challenge for such implementation due to the impairments caused by imperfections of the radio frequency (RF) front-end. For instance, orthogonal frequency-division multiplexing (OFDM) suffers from the non-linearity of RF power amplifier because of its high PAPR. On the contrary, single carrier (SC) modulation uses a single carrier, instead of many subcarriers typically used in OFDM, so the peak-to-average transmitted power ratio for SC-modulated signals is smaller. This in turn means that the power amplifier of an SC transmit-

ter requires a smaller linear range to support a given average power. As such, this enables the use of a cheaper power amplifier than a comparable OFDM system; and this is the most significant benefit for mobile satellite wireless communication systems. Hence, SC block transmission has been developed as an alternative technique for broadband wireless systems to mitigate the inter-symbol interference (ISI) while achieving higher power efficiency [27] [28]. It is shown that SC transmission with frequency domain equalization has similar performance and signal processing complexity as OFDM, but avoids OFDM's drawback of high PAPR [29]. As a result, SC transmission has been adopted by many wireless standards (e.g., IEEE 802.11ad and IEEE 802.15.3c) to support low power and low complexity wireless transmission. In particular, OFDM for downlink and SC block transmission for uplink of the hybrid approach has been adopted by the Third Generation Partnership Project (3GPP) Long Term Evolution (LTE) standard [30].

- *Challenge 3: Converter Speed*

  With the ever increasing demand for high data rate wireless communications, it is necessary to increase the signal bandwidth and improve the spectral efficiency at the same time. For high-speed wideband wireless applications and aerial backbone networks, millimetre wave (mm-wave) communication systems have been proven to be a viable solution since there is more bandwidth to be used for wireless transmission in mm-wave bands such as the E-band (71-76 and 81-86 GHz) with two 5 GHz contiguous bands and the D band (110-170 GHz) with several tens of GHz bandwidth [31] and [32]. A key limitation is the lack of digital-to-analog conversion (D/A) and analog-to-digital conversion (A/D) that operate a high sampling rate such as 10 Giga samples per second (Gsps) or higher sampling rate. For example, Analog Device, Inc. (ADI) recently published the first commercial A/D which can achieve 10 Gsps

sampling rate with 12 bits [33]. Texas Instruments Incorporated (TI) and Teledyne e2v have the new production of A/Ds with maximum sampling rate at only 6.4 Gsps at the moment [34] [35]. In order to achieve high-speed mm-wave communications with 10 GHz or wider signal bandwidth, higher than 10 Gsps sampling rate D/A and A/D devices must be used. How to adopt lower sampling rate conversion devices to implement more than 10 GHz bandwidth communication system is still a challenge.

- *Challenge 4: System Complexity*

  Due to the application requirements for ISTN and the characteristics of the satellite environment, an ISTN system is expected to effectively reduce energy consumption without degradation in performance or increment in cost, while ensuring availability, reliability and robustness. Considering the sampling rate at more than tens of Gsps for each band and/or multiple simultaneously occupied bands, huge number of data should be dealt with in real-time. Future mobile broadband systems are expected to provide users with the experience of radio access with unlimited performance, i.e., instantaneous delivery of large volumes of multimedia content over a highly stable wireless connection. However, due to the characteristics of satellite communications, the limitation in system volume and power is an important issue. Therefore, low-complexity and effective algorithms are necessary to achieve the required system performance and compensate for the imperfection of wireless channels. Moreover, adopting low-complexity and effective algorithms, how to implement them using as less as possible resource in hardware to reduce the power and volume is still a challenge for researchers.

1.3 Thesis Organization

The remainder of this thesis is organized as follows.

Chapter 2 presents a low-complexity synchronization design with large CFO for high-speed wireless communication. It starts with the requirements of synchronization for achieving desired performance with low system overhead. Then, the design of training sequence with desired frequency domain properties to aid the synchronization, channel estimation and in-phase and quadrature-phase (I/Q) imbalance estimation is provided. The practical implementation of autocorrelation with real-time CFO estimation is described to show the effectiveness for peak capture. Finally, simulation results are shown to demonstration the performance.

Chapter 3 presents a method of estimating and compensating for the receiver and transmitter I/Q imbalances sequentially at the receiver digital baseband for point-to-point wireless communication systems. Firstly, the system and signal models are presented for point-to-point wireless communication systems and the format of transmitter frame is described. Then, how to estimate and compensate for I/Q imbalance, how to estimate and equalize channel and how to complete sampling rate conversion (SRC) function are provided and formulated. Finally, the simulation results are shown to demonstration the performance.

Chapter 4 presents a dual pulse shaping (DPS) transmission scheme where the data symbols to be transmitted are split into two half rate data streams. Firstly, the Nyquist theorem for ISI-free transmission is revisited, and the concept of complementary Nyquist pulse is introduced. Then, the cross-symbol interference (CSI) free condition is proved and two classed of complementary Nyquist pulses satisfying this condition are formulated. Next, the DPS system with practical spectral shaping pulses is described and the zero forcing (ZF) and minimum mean square error (MMSE) equalization techniques for DPS are proposed. Finally, the simulation results are provided to show the performance of the proposed system.

Chapter 5 presents a high-speed low-complexity digital modem for wireless com-

munications at 0.325 terahertz (THz) carrier frequency. The basic system requirements, architectures and signal processing modules for transmitter and receiver sides are described. Implementations of some typical modules included Ethernet interface, transmitter filter and receiver filter are presented. Following the description of field programmable gate arrays (FPGA) structure, some key strategies are elaborated when implementing algorithms in FPGA. The implementation and experimental results for digital modem are shown. Finally, the integrations with IF modules and THz RF front-end are described and the experimental results for integrations are provided.

Chapter 6 summarizes the main contributions of this thesis and discusses some research problems for future work.

Chapter 2

Synchronization in Presence of Large CFO

2.1 Introduction and Literature Review

The initial frequency offset is quite large in radar, mobile-satellite, global positioning system and satellite navigation applications[36]. In order to take into account an initial frequency offset, continuous wave signals are often applied in conjunction with repeated training sequences[37][38]. In a typical arrangement, a receiver can first analyze a continuous wave signal to accurately estimate the frequency error and then compensate for the frequency error before proceeding with the subsequent pseudo noise (PN) correlation process. Conventional coarse timing, which fulfills packet detection and locates data symbol to the accuracy within the length of the training sequence, is based on autocorrelation between the received signal and its delayed version. To avoid the adverse impact of power fluctuation, the autocorrelation is usually normalized to the received signal power, and a timing metric with value between zero and one is obtained. The metric is compared to a threshold to determine the coarse timing offset. This conventional scheme has many advantages, such as low-complexity recursive computation, the use of only two repeated sequences, and the capability of fully collecting the multi-path energy. However, autocorrelation is vulnerable to large CFO and requires much higher implementation complexity to compensate CFO.

In [37], a robust timing metric is designed for timing offset estimation by using the correlation properties of a periodic preamble. This timing metric has a low computational complexity, but is not sharp and has a large variance. In [39] [40],

the authors change the sign of the identical parts of the preamble in [37] to make the timing metric sharper. A timing metric taking advantage of the central symmetry of a preamble is proposed in [38]. In [41], it is shown that applying the periodic parts of more than one preamble can improve the false alarm probability. The application of differential normalization making the values of the timing metric at wrong and correct timing instants more distinct is proposed in [42]. The authors in [43] demonstrate that there are no sufficient statistics for the detection of a preamble that is composed of two identical parts in the time domain, and therefore, the second order statistics used in the previous methods are not sufficient. They also propose fourth order statistics for frame detection. Fourth order differential normalization is used in [44] to improve the synchronization performance. Timing metrics using the cross-correlation of the received signal and pure preamble can be found [45] [46]. In [45], for having a sharper timing metric, the identical parts of the preamble are multiplied by a PN sequence. The authors in [46] improve the timing estimation performance by increasing the correlation length. Although the cross-correlation metrics are sharper than the autocorrelation metrics, they are not as robust as autocorrelation metrics, because they are usually sensitive to CFO, and need to know the exact preamble which may not be easily available or may suffer from considerable implementation complexity when the preamble signal is selected among lots of candidates to identify cell or sector index.

Due to the influence of CFO, it is difficult to achieve a sharp peak from autocorrelation. Therefore, the compensation of CFO is necessary to find the real peak point. However, it is complicated to obtain an accurate value of CFO in time without any delay. Considering these factors, a real-time estimation of CFO which can be used to improve the autocorrelation is necessary.

In a practical wireless communication system, preamble and user data are transmitted separately. Preamble serves as the training signal to facilitate timing and

carrier frequency synchronization, channel estimation, and system parameter acquisition [37] [42]. Although a preamble is multi-functional, it is mostly designed for initial timing and frequency synchronization without a priori knowledge of frequency-selective channel impulse response because accurate channel estimation and system parameter acquisition can be achieved effectively only when timing and frequency are well synchronized. To the contrary, for satisfying the throughput requirement of the system, the preamble should not occupy a significant portion in the frame. So, it is essential to design an short enough and effective preamble for achieving these functions.

In this chapter, a low-complexity design of synchronization with large CFO for high-speed wireless communication is proposed. The estimated CFO can be compensated together with autocorrelation operation. And following CFO compensated autocorrelation operation, the accuracy of estimated CFO can be stabilized at the expected value. More importantly, the complexity of implementation is quite low and only a small percentage hardware resource is occupied in real-time FPGA

The rest of this paper is organized as follows. Firstly, one kind of training sequence with desired frequency domain properties to aid the synchronization, channel estimation and transmitter I/Q imbalance estimation is designed. And then the practical implementation of autocorrelation with real-time CFO estimation is described to show the effectiveness for capturing the segment of transmitted preamble. Finally, the simulation results is shown to demonstration the performance.

2.2 Training Sequence Design

Synchronization includes coarse timing (packet acquisition) and fine timing. Coarse timing is only implemented in system power-up to acquire the data frame as following frames will be received continuously. The preamble contains two training sequences. This allows for fine timing in multi-path propagation environment and

estimation of large CFO value.

Not only the preferred training sequence described below can complete the function of synchronization, but also the training sequence is specifically designed to achieve the best channel and I/Q imbalance estimation performance with low complexity. The essential properties required for such training sequences are that the real and imaginary parts of the time domain signal are orthogonal and their frequency domain representations also demonstrate some desired characteristics. The training sequence in the discrete time domain at the symbol rate is denoted as

$$x\left[n\right] = x_I\left[n\right] + jx_Q\left[n\right] \tag{2.1}$$

where $j = \sqrt{-1}$ is the imaginary unit, $x_I[n]$ and $x_Q[n]$ are the real and imaginary parts of the training sequence $x[n]$ respectively. The length of the training sequence at symbol rate sampling is N_s. Let $X[k]$, $X_e[k]$ and $X_o[k]$ be the discrete Fourier transforms (DFTs) of $x[n]$, $x_I[n]$ and $jx_Q[n]$ respectively where k is also referred to as subcarrier or frequency bin, so that $X[k] = X_e[k] + X_o[k]$. For simplicity, we design the sequences $X_o(k)$ and $X_e(k)$ to take on values of 1 or -1 only at the even and odd indices respectively and satisfy the required symmetric properties, as illustrated in Figure 2.1. The orthogonality of the real and imaginary parts $x_I[n]$ and $x_Q[n]$ may then be denoted as

$$X_e\left[k\right] X_o\left[k\right] = 0 \tag{2.2}$$

with $X_e[k]$ and $X_o[k]$ not being zeros at the same time. In addition, to reduce the computational complexity, $X[k]$ is preferably real with constant magnitude and satisfy the condition

$$X\left[k\right] X\left[-k\right] = \left(-1\right)^k \tag{2.3}$$

where we have assumed that $X[k]$ is a periodic function of k with period N_s.

After the training sequence is constructed, the preamble of the transmission frame can be obtained by adding a cyclic prefix (CP) taken from the last part of

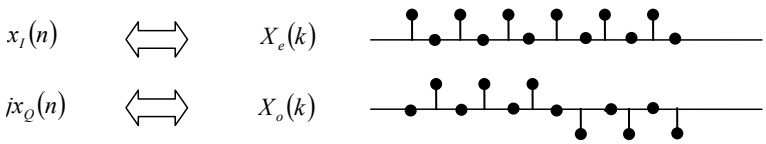


Figure 2.1 : Training sequence design.

the samples of $x[n]$. Preferably, the preamble at symbol rate can be converted to sampling rate after performing pulse shaping and sample rate conversion off-line so that it can be inserted to the transmission frame and directly input to D/A. After the sample rate conversion, the training sequence becomes longer since the sampling rate is normally higher than the symbol rate.

2.3 Autocorrelation Implementation

Coarse timing can be implemented with autocorrelation operation, exploiting the similarity between the two training sequences, as shown in Figure 2.2.

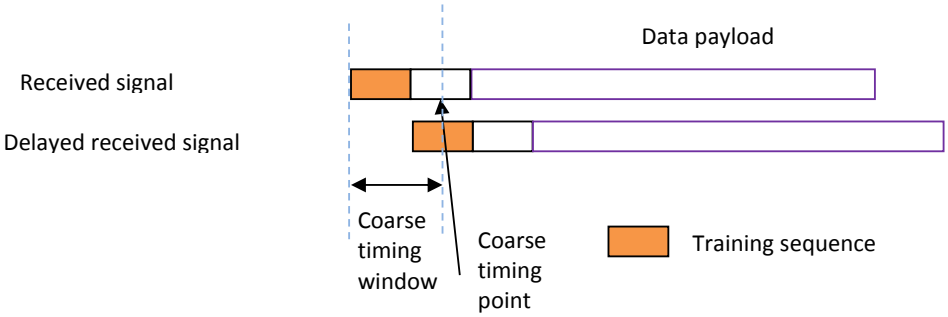


Figure 2.2 : Using autocorrelation for coarse timing.

The autocorrelation is represented as

$$\rho(n) = \sum_{k=n-N+1}^{n} y(k)y^*(k-N) \tag{2.4}$$

where y^* denotes the conjugate of y. Note that $y(k)$ are received signal samples at 2.5 Gsps. At the same time, the noise energy of N signal samples is computed as

$$\sigma(n) = \sum_{k=n-N+1}^{n} [e^{-jarg[\rho(k)]}y(k) - y(k-N)]^2. \tag{2.5}$$

The estimated SNR can be calculated as $SNR(n) = (2|\rho(n)|)/\sigma(n)$ and it is compared with a predefined threshold SNR_{th}. Once $SNR(n_t) \geq SNR_{th}$ at $n = n_t$, it is assumed that the packet is acquired, and the coarse timing point is at n_t.

In practical implementation, the autocorrelation operation is implemented for coarse timing, and the accuracy requirement for this part is not very high. So, when implementing the autocorrelation, we can simplify some parts of the equation. The computation of $\rho(n)$ and $\sigma(n)$ can be efficiently realized by a sliding window, i.e.,

$$\rho(n+1) = \rho(n) + \phi(n+1) \tag{2.6}$$

and

$$\sigma(n+1) = \sigma(n) + |y(n+1)|^2 - |y(n+1-2N)|^2 - 2Re\{\phi(n+1)e^{-jarg[\rho(n+1)]}\} \tag{2.7}$$

where $\phi(n+1) = y(n+1)y^*(n+1-N) - y(n+1-N)y^*(n+1-2N)]$.

Considering eight complex numbers in each system clock (the information of implementation can be found in Section 5.2.3), the eight values of $arg[\rho(n+1)]$ in (2.7) can be approximately equivalent. That means, when calculating the value of $arg[\rho(n+1)]$ for each system clock, we can merge eight samples together and calculate only one angle. Due to the large number of the resource used for the intellectual property (IP) core of cordic from Xilinx [47], it is effective to save lots of resource in this simplified method. Considering the low level of accuracy in the part of coarse timing and the delay from IP core of cordic, we can simply use the look-up table (LUT) [48] with fixed angle information to replace the cordic core.

From the preamble design, the correct coarse timing will be located during the last half of the second training sequence. Due to the periodic repetition of the training sequences, we can easily find that the value of $y(n+1-N)y^*(n+1-2N)$ is the N-point delayed version of $y(n+1)y^*(n+1-N)$. That means, when we calculate the value of $\phi(n)$, we can just calculate the front part of $\phi(n)$, and then store them into a buffer. After the delay of N points, the stored data can be used as the latter part of $\phi(n)$. In this way, half of the number of multipliers for complex numbers are saved in FPGA.

From the above optimized strategies, we can obtain the resource usage of autocorrelation after testing in real system. From Table 2.1, we can see that resource

Table 2.1 : FPGA usage of autocorrelation

Cell Name	Slice LUTs	Slice Registers	Block RAMs	Multipliers
Total Number	433200	866400	1470	3600
Used Number	1774	2726	5	34
Usage Rate	0.4%	0.31%	3.4%	1%

usage of some typical cells including LUTs, slice registers, block random-access memories (BRAMs), multipliers are reasonable for the autocorrelation compared with the total resources in this device. The module of autocorrelation only occupies a very small proportion of the total available resources. The reserved resources can be used for other modules in the whole digital modem.

2.4 Simulation Results

The simulation results are now described as follows. Simulations are carried out by SC signal with 5 GHz and 2.5 GHz bandwidths. The design of training sequence is described in Section 2.2 and the length of training sequence is 64. The autocorrelation is performed during the training period of each frame. That means, the estimated CFO value is updated every frame. Figure 2.3 and Figure 2.4 shows the estimation results with 30 MHz and 10 MHz CFOs under 8 dB SNR in wireless communication systems with 5 GHz and 2.5 GHz bandwidths respectively. After the duration of 300 frames which occupies around 1 ms, the estimated CFOs stabilized at the expected values. Note that the details of frame structure can be found in Section 5.2.3.

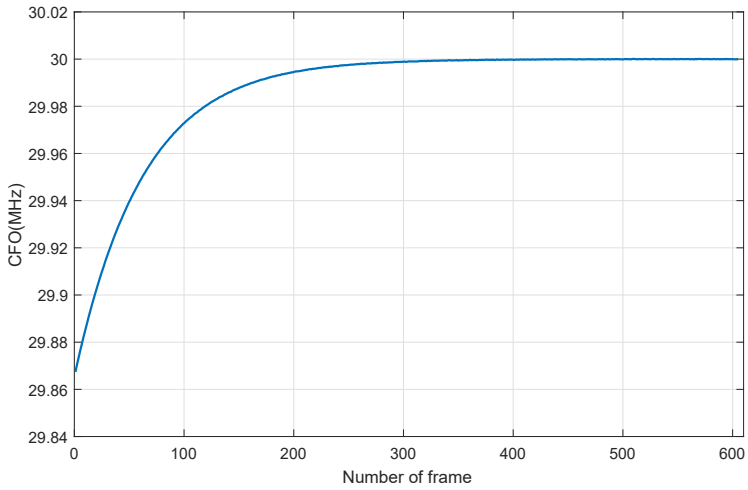


Figure 2.3 : CFO=30 MHz estimation under 8 dB SNR.

The bit error rate (BER) vs SNR performance (uncoded) is evaluated using a 2.5 GHz bandwidth 16-quadrature amplitude modulation (QAM) modulated wireless communication system with and without CFO. There are 5000 frames and each frame contains 27216 bits. The total number of bits for simulations is 136080000 and the lowest BER would be $1/136080000 = 7.35\times10^{-9}$. The results are presented

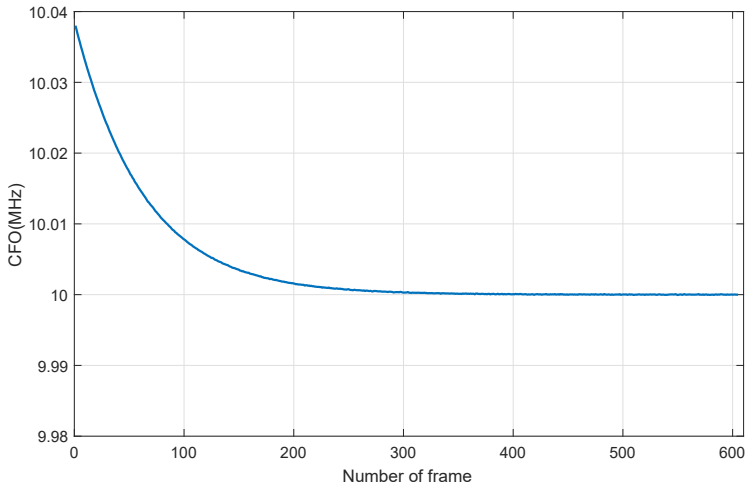


Figure 2.4 : CFO=10 MHz estimation under 8 dB SNR.

in Figure 2.5. It shows that the wideband wireless communication system with CFO estimation and compensation can achieve almost the same performance comparing with the system without CFO. The simulation results indicate that the estimation accuracy is sufficient for supporting 16-QAM without performance loss.

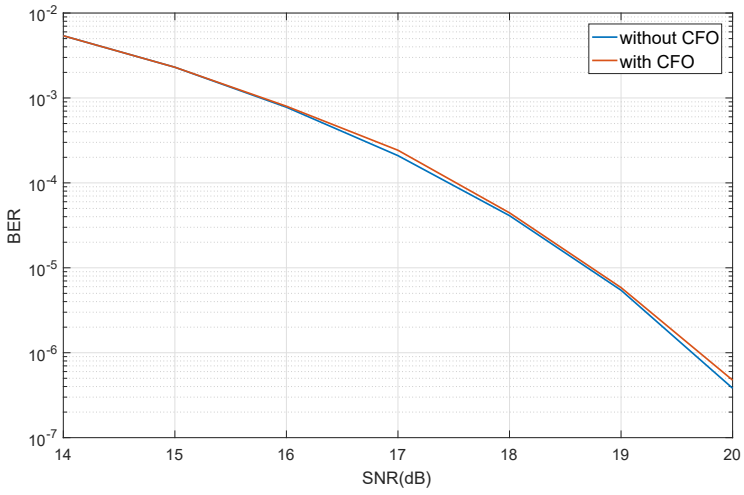


Figure 2.5 : BER performance (uncoded) with and without 10 MHz CFO.

To demonstrate the performance of the above described coarse timing algorithm, simulation results in terms of detection probability and missed detection probability

under various SNRs and carrier frequency offsets are provided in Figure 2.6 and Figure 2.7 respectively. Practical transmitter and receiver I/Q imbalances (with image rejection ratio of about 23 dB) are also added in the simulations.

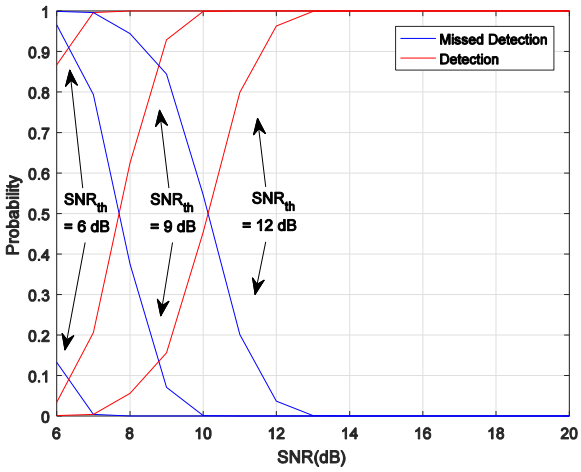


Figure 2.6 : Coarse timing detection probability and missed detection probability versus SNRs (CFO = 0).

2.5 Conclusions

An effective design and implementation of synchronization with large CFO for high-speed wireless communication is proposed and tested. The CFO can be estimated and compensated together with autocorrelation operation. The optimized algorithms are implemented with low-complexity, and the low resource usage is verified in real-time FPGA. From the simulation results, autocorrelation operation can capture tens of MHz CFO and the system has almost no performance loss comparing with the system without CFO.

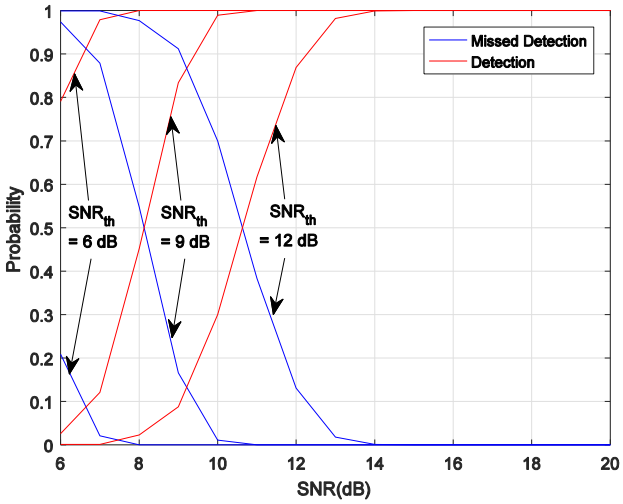


Figure 2.7 : Coarse timing detection probability and missed detection probability versus SNRs (CFO = 10 MHz).

Chapter 3

Joint I/Q Imbalance Compensation and Channel Equalization in SRC Receiver Filters

3.1 Introduction and Literature Review

Many applications require that the I/Q imbalances for both transmitter (Tx) and receiver (Rx) can be estimated and compensated separately. I/Q imbalance is one major issue that needs to be considered in low cost architectures, such as direct conversion transmitter [49]. I/Q imbalance may accrue during up-convertor at the transmitter and down-convertor at the receiver because of the mismatch of the two branches. The distortion introduced by I/Q imbalance can be frequency-independent (caused by the amplitude and phase difference in the non-ideal mixer) or frequency-dependent (caused by inaccuracy of the branch filters). Without proper compensation techniques, the transmission capability of wireless system under I/Q imbalance will be seriously degraded.

In general, it is very hard to compensate I/Q imbalance in analog domain due to its cost and inefficiency [50]. As mentioned in [51], many related works have focused on mitigating the effect of I/Q imbalance in digital baseband. For OFDM systems, the impact of I/Q imbalance is studied [52]. Furthermore, a closed-form BER analysis of OFDM system under I/Q imbalance is derived in [53]. These results show that the effect of I/Q imbalance produces so called mirror carrier interference causing the loss of orthogonality among the subcarriers. Various I/Q imbalance estimation and compensation schemes have been proposed for the compensation of frequency-independent [54] and frequency-dependent I/Q imbalance [50]. Initially,

most solutions use linear compensation methods, such as least square (LS) [55] and MMSE [56]. Later, nonlinear receivers like decision-directed [57], expectation methods maximization [58] and maximum likelihood (ML) [59] methods are introduced for better performance.

There are not many works on I/Q imbalance for single carrier frequency. Under frequency-independent I/Q imbalance, the training sequence design for LS channel estimation of single carrier frequency domain equalization (SC-FDE) is studied in [60]. Then an enhanced channel estimation is proposed using alternative LS (ALS) algorithm [61]. Furthermore, [62] derives the channel model of SC-FDE with independent Tx/Rx frequency I/Q imbalance, PN sequence aided channel estimation and MMSE compensation. Considering the presence of both I/Q imbalance and carrier frequency offset, a three stage compensation scheme for SC-FDE is provided in [63]. For millimeter-wave SC-FDE systems, Cheng et al. [64] propose joint channel and I/Q imbalance estimation using ML criterion and I/Q imbalance compensation using MMSE criterion. However, most existing works focus on the channel estimation under frequency-independent I/Q imbalance and use linear compensation methods to eliminate the effect of I/Q imbalance. Although linear receivers benefit from their low complexity, the BER performance is far from the match filter bound (MFB), especially in highly frequency-selective wireless channel [65]. There exist several nonlinear receivers for SC-FDE system without I/Q imbalance. Among them, one promising design is the iterative block decision feedback equalization [66], which employs feedforward and feedback filters in frequency domain and its performance is close to the MFB. Its iterative architecture has been extended to several special scenarios, such as interference channels [65] and system with imperfect channel state information [67]. Most of the conventional techniques deal with I/Q imbalance at the receiver side only [68, 69], whereas both Tx and Rx side imbalances exist at the same time in practical systems. Estimating and compensating for both Tx and Rx

side imbalances are very challenging as the imbalanced signals are mixed together and the received signals only reflect the overall effect resulted from both Tx and Rx imbalances. When CFO is present in the communication system [70, 71], the overall effect also changes over time. Existing approaches typically require off-line calibration to estimate and compensate for the Tx I/Q imbalance, and then estimate and compensate for the Rx I/Q imbalance using the received signal [72]. Real-time calibration is also possible to deal with time-varying Tx I/Q imbalance [73], however, this calibration will interrupt the data transmission and/or require more system overhead. A feedback channel is also necessary if the imbalance is estimated at the receiver side [74].

To achieve better equalization performance, a wireless SC system commonly uses fractionally spaced linear equalizer, which requires that the sampling rate is higher than the data symbol rate. Therefore, SRC is necessary to convert symbol rate to sampling rate before pulse shaping at the transmitter and sampling rate to symbol rate after equalization at the receiver, which generally increases the digital signal processing complexity. If the SRC can be performed jointly with other functions such as I/Q imbalance compensation and equalization, the complexity will be reduced.

I/Q compensation, channel equalization and SRC play vital roles in high-speed wireless communication systems. Any lack of such signal processing will significantly impact on the performance of the whole system. The bandwidth of our proposed system involves four channels each having 2.5 GHz spectrum. In such wide bandwidth, any imperfection in various filters of IF and/or RF as well as wireless multi-path fading channel introduces ISI at the receiver. In the meantime, existing algorithms for such signal processing are complicated and require lots of hardware resource to implement, especially for high-speed wideband wireless communication.

In this chapter, a low-complexity and an effective method for estimating Rx and

Tx I/Q imbalances and compensating for them in serial at the receiver of a communication system is proposed. The system and signal models for point-to-point wireless communication systems are first presented and the format of the transmitter frame is described. Then, how to estimate and compensate I/Q imbalance, how to estimate and equalize channel and how to complete SRC function are provided and formulated. Finally, the simulation results are shown to demonstrate the performance.

3.2 System and Signal Models

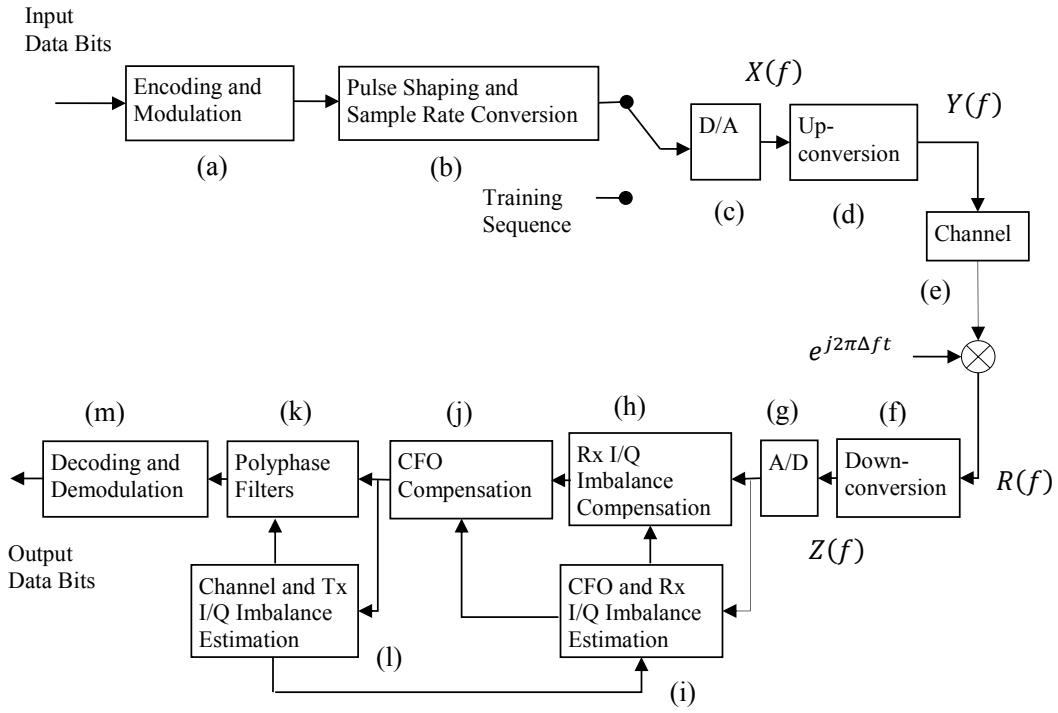


Figure 3.1 : Baseband block diagram of a point-to-point wireless communication system with the disclosed successive I/Q imbalance estimation and compensation.

Figure 3.1 shows a baseband schematic block diagram of point-to-point wireless communication system. The system includes a transmitter which communicates via

a channel with a receiver. CFO will be introduced at the receiver, which can be modelled as the multiplication of the received baseband signal by a phase rotation $e^{j2\pi\Delta ft}$ where Δf is the CFO.

At the transmitter of Figure 3.1, the input data bits are forward error coded (FEC) and modulated by module (a). The resulting data symbols are then input to the pulse shaping and sample rate conversion module (b) to generate output symbols. The output symbols are next provided to a D/A before the signal is up-converted by the up-converter (d) and transmitted over the channel (e). The up-converter will introduce Tx I/Q imbalance. During a training period which starts at the beginning of every transmitter frame, a training sequence is inserted before the data payload. Preferably, the rate of training sequence is equal to data symbol rate and then converted to sampling rate so that it can be directly input to the D/A.

Mathematically, the frequency domain signal model of the transmitted signal can be expressed as

$$Y(f) = U_t(f)\,X(f) + V_t(f)\,X^*(-f) \tag{3.1}$$

where $X(f)$ and $Y(f)$ are the transmitted signals before and after up-conversion respectively, $U_t(f)$ and $V_t(f)$ are the frequency dependent gains of the baseband signal and its image respectively. $U_t(f)$ can be regarded as part of the transmission channel frequency response whereas $V_t(f)$ reflects the interference caused by the Tx I/Q imbalance.

At the receiver of Figure 3.1, the signal received from the channel (e) and distorted by the CFO is first down-converted by the down-converter (f) and passed to an A/D (e). The down-converter will introduce Rx I/Q imbalance. After the CFO and Rx I/Q imbalance are estimated in the module (i), they are compensated in the modules (h) and (j) sequentially. Channel and Tx I/Q imbalance estimations are performed in the module (l) and the estimated channel and I/Q imbalance

parameters are used to calculate the polyphase filter coefficients. The polyphase filters perform combined Tx I/Q imbalance compensation, channel equalization, and sample rate conversion to generate output symbols. The output symbols are then provided to module (m) which applies FEC decoding and demodulation to provide output data bits.

Mathematically, the received signal before down-conversion R(f) can be expressed as

$$R(f) = e^{j\varphi} Y(f - \Delta f) H(f - \Delta f) \tag{3.2}$$

where $\varphi = 2\pi\Delta f t_0$ is a phase rotation caused by the CFO at the beginning of a transmission frame at time instant t_0 and $H(f)$ is the channel frequency response. After down-conversion, the received signal is

$$Z(f) = U_r(f) R(f) + V_r(f) R^*(-f) \tag{3.3}$$

where $U_r(f)$ and $V_r(f)$ are the frequency dependent gains of the received signal and its image respectively. $U_r(f)$ can be regarded as part of the transmission channel frequency response whereas $V_r(f)$ reflects the interference caused by the Rx I/Q imbalance.

3.3 I/Q Imbalance Compensation and Channel Equalization

In order for the receiver to estimate CFO, Rx and TX I/Q imbalances, and channel frequency response, a training sequence needs to be periodically transmitted. Hence, a transmitter frame structure is proposed as shown in Figure 3.2. It consists of a preamble and a data payload. The preamble of each data frame includes the training sequence and its CP. Because all the I/Q imbalance and channel estimation is performed in the frequency domain, the CP is used to convert the linear convolution of transmitted single with the channel to a circular convolution so that fast Fourier transform (FFT) can be applied to convert a signal from time

domain to frequency domain.

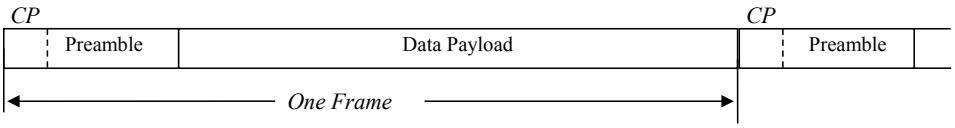


Figure 3.2 : Transmitter frame structure.

Once the training sequence is received at the receiver digital baseband after signal synchronization, Rx I/Q imbalance is estimated as follows.

Firstly, at the beginning of each received frame, the phase rotation is estimated. Then, the received signal $Z(f)$ is weighted by the phase factors $e^{j\varphi}$ and $e^{-j\varphi}$ respectively to have

$$e^{j\varphi}Z\left(f\right)=e^{j2\varphi}U_{r}\left(f\right)Y\left(f-\Delta f\right)H\left(f-\Delta f\right)+V_{r}\left(f\right)Y^{*}\left(-f-\Delta f\right)H^{*}\left(-f-\Delta f\right) \tag{3.4}$$

and

$$e^{-j\varphi}Z\left(f\right)=U_{r}\left(f\right)Y\left(f-\Delta f\right)H\left(f-\Delta f\right)+e^{-j2\varphi}V_{r}\left(f\right)Y^{*}\left(-f-\Delta f\right)H^{*}\left(-f-\Delta f\right). \tag{3.5}$$

Performing the same operations as described by (3.4) and (3.5) for a number of received frames and averaging over the differently weighted received signals, we have

$$E\left\{e^{j\varphi}Z\left(f\right)\right\}=V_{r}\left(f\right)Y^{*}\left(-f-\Delta f\right)H^{*}\left(-f-\Delta f\right) \tag{3.6}$$

and

$$E\left\{e^{-j\varphi}Z\left(f\right)\right\}=U_{r}\left(f\right)Y\left(f-\Delta f\right)H\left(f-\Delta f\right) \tag{3.7}$$

where $E\{.\}$ denotes expectation.

The Rx I/Q imbalance parameter is then estimated as

$$\beta_{r}\left(f\right)=\frac{E\left\{e^{j\varphi}Z\left(f\right)\right\}}{E\left\{e^{-j\varphi}Z^{*}\left(-f\right)\right\}}=\frac{V_{r}\left(f\right)}{U_{r}^{*}\left(-f\right)}. \tag{3.8}$$

A flowchart describing the above Rx I/Q imbalance estimation process is shown in Figure 3.3.

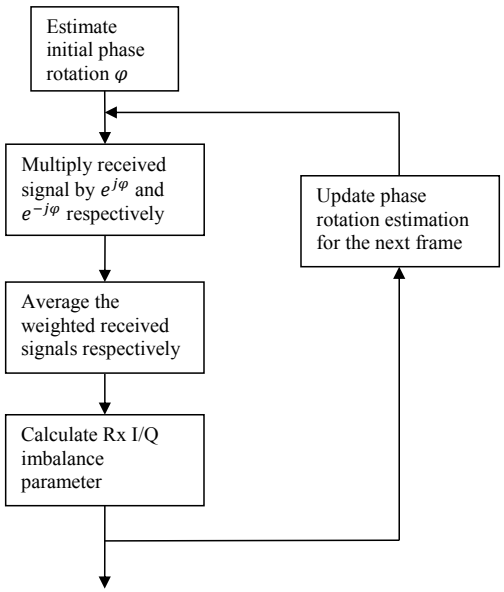


Figure 3.3 : Flow graph of Rx I/Q imbalance estimation.

The estimated Rx I/Q imbalance parameter $\beta_r(f)$ can be used to compensate for the Rx I/Q imbalance by the operation $Z(f) - \beta_r(f)Z^*(-f)$ in the frequency domain. However, in practice, a linear filter in the time domain is preferable. The structure of such a linear filter is shown in Figure 3.4, where the filter coefficients are represented by a vector c which is the inverse discrete Fourier transform (IDFT) of the discrete version of the frequency domain Rx I/Q imbalance parameter $\beta_r(f)$.

After Rx I/Q imbalance and CFO compensation, the Tx I/Q imbalance can be further estimated and compensated from the received signal during the preamble period, which is modeled in the discrete frequency domain as

$$R\left[k\right] = U_t\left[k\right] H_1\left[k\right] X\left[k\right] + V_t\left[k\right] H_1\left[k\right] X^*\left[-k\right] \tag{3.9}$$

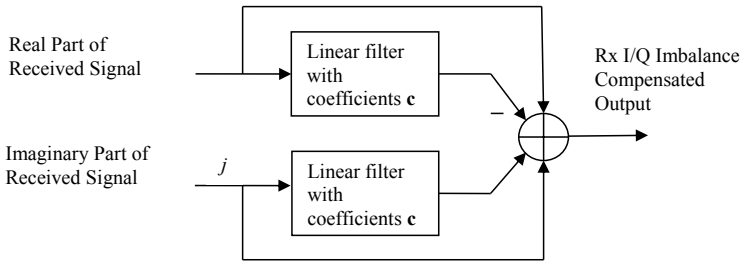


Figure 3.4 : Linear filter structure for Rx I/Q imbalance compensation.

where $X[k]$ is the designed frequency domain training signal as described previously and $H_1[k]$ is the equivalent channel frequency response after Rx I/Q imbalance compensation. Note that the length of $R[k]$ is N.

The Tx I/Q imbalance estimation makes use of the properties of $X[k]$, i.e., $X[k]$ is real, binary, and satisfies the condition shown in (2.3). In fact, multiplying both sides of (3.9) by $X[k]$ for $k = 0, \cdots, N/2$ and by $X[k-N+N_s]$ for $k = N/2+1, \cdots, N-1$, we have

$$\begin{aligned} \tilde{H}[k] &= \begin{cases} R[k]\, X[k], \ k = 0, \cdots, \frac{N}{2} \\ R[k]\, X[k-N+N_s], k = \frac{N}{2}+1, \cdots, N-1 \end{cases} \\ &= U_t[k]\, H_1[k] + (-1)^k V_t[k]\, H_1[k]. \end{aligned} \tag{3.10}$$

$\tilde{H}[k]$ can be interpreted as the estimated channel before Tx I/Q imbalance compensation. From $\tilde{H}[k]$, the Tx I/Q imbalance can be estimated as follows:

Step 1. Compute instantaneous channel estimation $\widetilde{H}(k)$ from the received preamble;

Step 2. For every frequency bin in $\widetilde{H}(k)$, get an interpolated value using two adjacent bins on both sides to obtain $\widetilde{H}'(k)$;

Step 3. Calculate $U(k) = \frac{\widetilde{H}(k)+\widetilde{H}'(k)}{2}$ and $V(k) = (-1)^k \left[\frac{\widetilde{H}(k)-\widetilde{H}'(k)}{2}\right]$;

Step 4. Calculate $H_{V/U^*}(k) = \frac{V[k]}{U^*[-k]}$.

In practice, channel estimation will average over multiple frames to improve the SNR. Therefore, no further averaging on $H_{V/U^*}(k)$ is necessary. This can simplify the algorithm without performance loss. The flowchart describing the above Tx I/Q imbalance estimation process is shown in Figure 3.5.

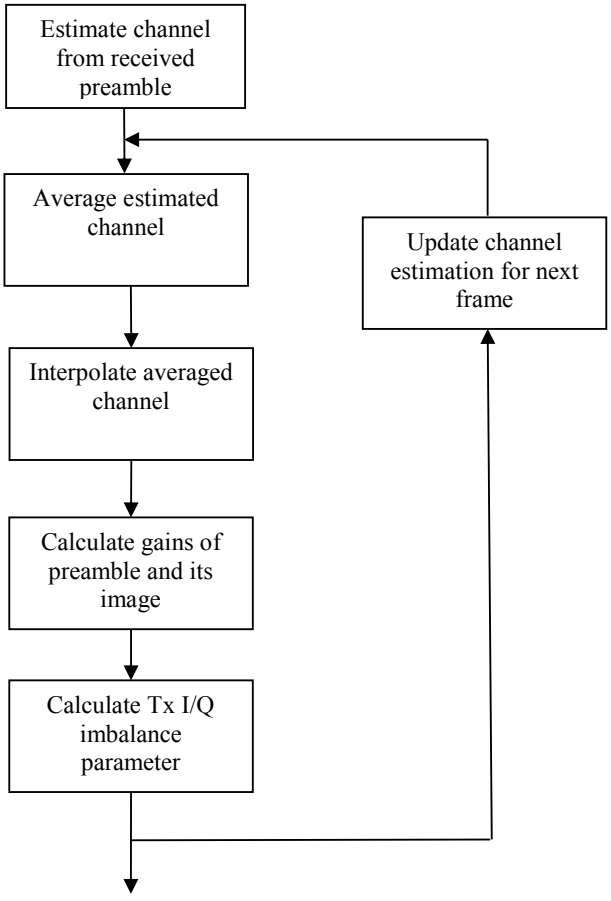


Figure 3.5 : Flow graph of Tx I/Q imbalance estimation.

After estimating the I/Q imbalance, the I/Q imbalance parameter can be com-

bined to the channel estimation. The channel estimation can be defined as

$$H_{U^*}(k) = \widetilde{H}(k) - (-1)^k H_{V/U^*}(k)\widetilde{H}^*((N-k)_N). \tag{3.11}$$

Once the channel is estimated in the frequency domain, the inverse channel estimation can be calculated as

$$C(k) = \begin{cases} \frac{H_{U^*}(k)}{|H_{U^*}(k)|^2+|H_{U^*}(k+N-N_s)|^2} & k = N_s - \frac{N_b}{2}, \cdots, \frac{N_b}{2} \\ \frac{1}{H_{U^*}(k)} & (k = 0, \cdots, N_s - \frac{N_b}{2} - 1) and \\ & (k = N - N_s + \frac{N_b}{2} + 1, \cdots, N-1) \\ \frac{H_{U^*}(k)}{|H_{U^*}(k)|^2+|H_{U^*}(k-N-N_s)|^2} & k = N - \frac{N_b}{2}, \cdots, N - N_s + \frac{N_b}{2}, \end{cases} \tag{3.12}$$

where N_s denotes the training sequence length at symbol rate and N_b denotes the number of frequency points in established bandwidth.

The receiver filters perform all the I/Q imbalance compensation, channel equalization, and SRC functions at the same time. We can combine the coefficients of channel equalization and I/Q imbalance compensation together to simplify the process. For the real and imaginary of symbols, the base filter's frequency responses are calculated respectively as

$$A(k) = [1 - H_{V/U^*}(k)]C(k) \tag{3.13}$$

and

$$B(k) = [1 + H_{V/U^*}(k)]C(k). \tag{3.14}$$

After performing phase shift in frequency domain, we obtain

$$A_p(k) = \begin{cases} A(k)exp(j\frac{2\pi}{N_s}kp) & k = 0, 1, \cdots, \frac{N}{2} - 1 \\ A(k)exp(j\frac{2\pi}{N_s}(k-N)p) & k = \frac{N}{2}, \frac{N}{2} + 1, \cdots, N-1 \end{cases} \tag{3.15}$$

and

$$B_p(k) = \begin{cases} B(k)exp(j\frac{2\pi}{N_s}kp) & k = 0, 1, \cdots, \frac{N}{2} - 1 \\ B(k)exp(j\frac{2\pi}{N_s}(k-N)p) & k = \frac{N}{2}, \frac{N}{2} + 1, \cdots, N - 1. \end{cases} \tag{3.16}$$

After converting $A_p(k)$ and $B_p(k)$ to the time domain by applying N-point IDFT, the coefficients of the receiver filters for filtering the real and imaginary parts of the received signal respectively can be obtained. The block diagram of the receiver filter bank and the structure of each polyphase filter are shown in Figure 3.6.

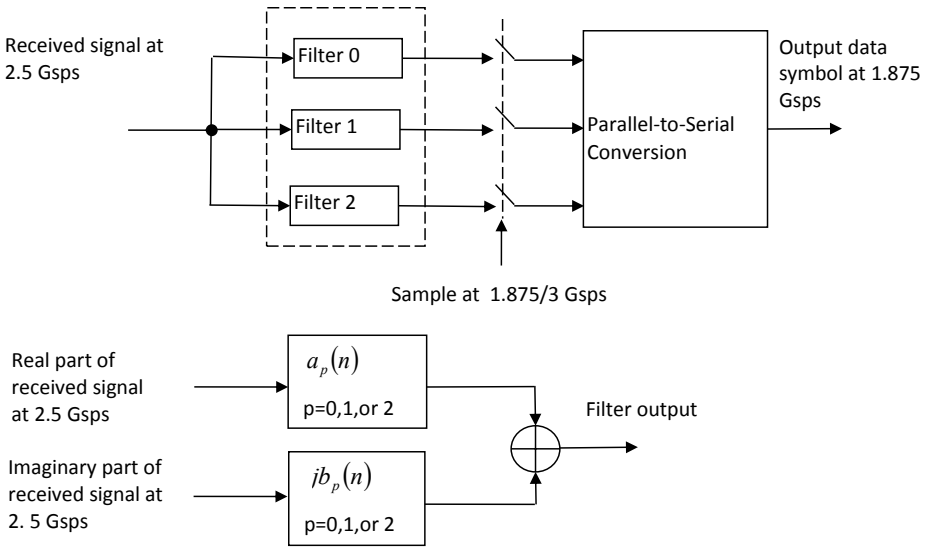


Figure 3.6 : Receiver filter bank (upper) and polyphase filter (lower) structures.

3.4 Simulation Results

To demonstrate the performance of the proposed method for high-speed low-cost communications, the simulation results are presented by SC signal with a 2.5 GHz wideband wireless communication system. The CFO is selected as $\Delta f = 10$ MHz and 16-QAM is used.

I/Q imbalance parameters are selected as follows. For the transmitter, the phase imbalance is -10 degree and the amplitude imbalance is 2 dB. To simulate the fre-

quency dependency, the two-order Butterworth filter with cutoff $2\pi\times0.3735$ radians is applied to the I channel and the three-order Butterworth filter with cutoff $2\pi\times0.3708$ radians is applied to the Q channel. For the receiver, the phase imbalance is 10 degree and the amplitude imbalance is -3 dB. The two-order Butterworth filter with cutoff $2\pi\times0.3871$ radians is applied to the I channel and the three-order Butterworth filter with cutoff $2\pi\times0.3826$ radians is applied to the Q channel.

Figure 3.7 shows a simulated channel frequency response in which the I/Q imbalance is clearly seen (the saw tooth in black curve). After I/Q imbalance compensation, the refined channel frequency response is smoother (the red curve).

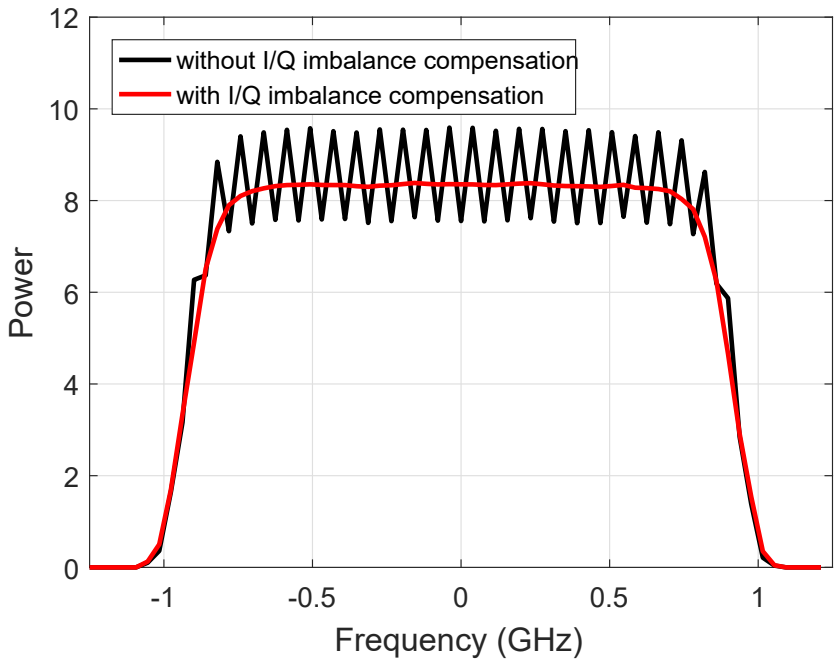
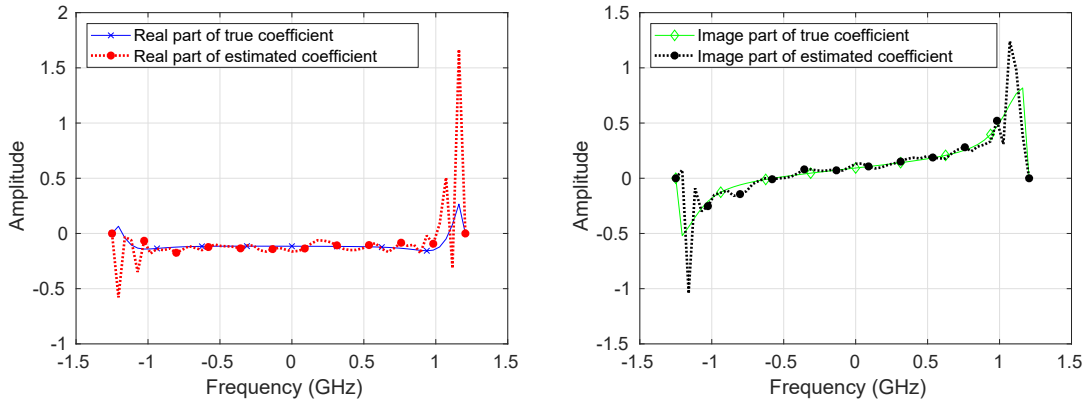


Figure 3.7 : Estimated channel frequency response and refined channel after I/Q imbalance compensation.

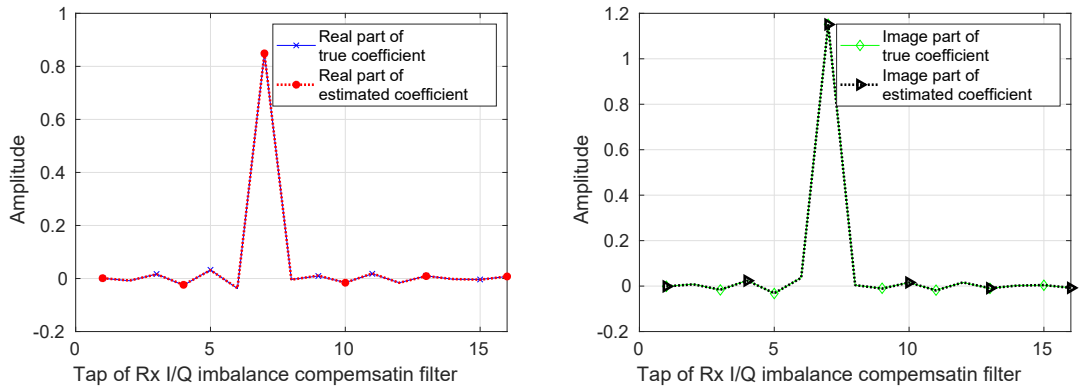
Figure 3.8 shows the real and image parts of estimated and true coefficients for Tx I/Q imbalance compensation. The estimated coefficients in the passband are quite close to the true values except for the coefficients at the edges of the bandwidth.

Figure 3.9 shows the real and image parts of estimated and true coefficients of the Rx I/Q imbalance compensation filter and the estimated coefficients are quite close to the true values.



(a) (b)

Figure 3.8 : Real (a) and image (b) parts of estimated and true Tx I/Q imbalance coefficients.



(a) (b)

Figure 3.9 : Real (a) and image (b) parts of estimated and true coefficients for Rx I/Q imbalance compensation filter.

Finally, the BER performance (uncoded) is evaluated with and without Tx

or/and Rx I/Q imbalance compensation, and the results are presented in Figure 3.10. The BER curve with perfect I/Q imbalance compensation (i.e., assuming perfect knowledge of the I/Q imbalances) is also shown. It is obvious that the performance is poor without any of Tx or Rx imbalance compensation. The BER curve with I/Q imbalance compensation using the estimated I/Q imbalance parameters is very close to the one using true I/Q imbalance compensation, which indicates that the estimation accuracy is sufficient for supporting 16-QAM with negligible performance loss.

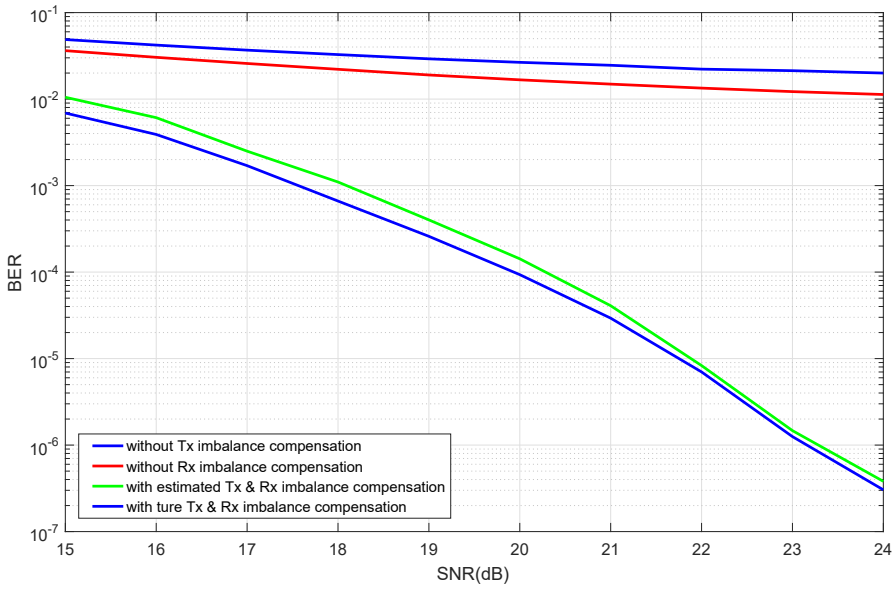


Figure 3.10 : BER performance (uncoded) with and without Tx or Rx I/Q imbalance compensation.

3.5 Conclusions

We have proposed a method of estimating and compensating for the receiver and transmitter I/Q imbalances in sequential at receiver digital baseband for point-to-point wireless communication systems. The Rx I/Q imbalance is estimated by

the received signal's statistical property and is compensated with a time domain linear filter. Using the received training sequence after Rx I/Q imbalance and CFO compensation, the channel and Tx I/Q imbalance are estimated and the compensation for the Tx I/Q imbalance and channel as well as samples rate conversion are jointly performed with a time domain linear filter. From the simulation results, the estimated Rx and Tx imbalance coefficients are quite close to the true values and the joint algorithm can achieve the desired performance.

Chapter 4

Dual Pulse Shaping Transmission System and Method

4.1 Introduction and Literature Review

In conventional digital single carrier communication systems, Nyquist pulse shaping at the transmitter and matched filtering at the receiver are used to achieve ISI free transmission and maximize the received SNR [75]. As one class of Nyquist pulses, raised-cosine (RC) pulses are widely used for such single pulse shaping transmission. Here, a root raised-cosine (RRC) pulse is used as the spectral shaping pulse at the transmitter and the same RRC pulse is used as the matched-filter impulse response. A roll-off factor associated with the RC pulse determines the actual transmitted signal bandwidth, which is often wider than the data symbol rate, resulting in reduced spectral efficiency.

With the ever growing demands for high data-rate wireless communications, it is necessary to increase the signal bandwidth and improve the spectral efficiency at the same time [76]. For high-speed wireless applications and aerial backbone networks, mm-wave technology has been proven to be a viable solution due to the availability of large bandwidth, e.g., 10 GHz in the E-band (71-76 and 81-86 GHz) and several tens of GHz in the D band (110-170 GHz). In order to achieve high-speed mm-wave communications with 10 GHz or wider signal bandwidth, higher than 10 Gsps sampling rate D/A and A/D devices generally need to be used.

When the required high-speed data conversion devices are unattainable or costly, how to achieve high date-rate wireless communications at low cost becomes a signif-

icant challenge. There are existing techniques such as time-interleaved [77] and frequency channelized [78–80] data converters. However, for time-interleaved schemes, the resolution (the number of bits for samples) and speed can not be achieved at the same time. For frequency channelized schemes, the sample/hold circuitry is very difficult to design as it sees the uppermost frequency in the high-frequency subband channels. In addition, the sharp bandpass filters that are needed to achieve high spectrum efficiency are also difficult to realize, especially in integrated chips [81, 82]. Faster-than-Nyquist (FTN) signaling [83, 84] has recently attracted great attention for achieving higher spectral efficiency. However, highly complicated signal processing at receiver is needed to deal with the interference between symbols [79, 80]. Such high complexity can make it unsuitable for many real-time signal processing platforms. Moreover, the PAPR of FTN signals is generally large, which limits the average transmission power.

Systems with reduced sampling rate may also be realized by allowing non-ideal transmission. Non-ideal transmission channels introduce ISI at the receiver and degrade system performance, and the severity of ISI increases with the reduction of sampling rate. ISI can typically be mitigated by ZF equalization [85, 86], MMSE equalization [87, 88] that can solve the noise enhancement problem of ZF, and fractionally spaced equalization (FSE) [89, 90]. However, all these equalization techniques require signal inputs sampled at a minimum of symbol rate. Hence the reduction of sampling rate via non-ideal transmission is very limited.

In this chapter, a DPS transmission scheme is proposed, where the data symbols to be transmitted are split into two half rate data streams, each passing through a respective pulse shaping filter. This allows for half symbol rate D/A and A/D devices to be used in each band to achieve full rate transmission. Different from frequency domain multiplexing (FDM), the two data streams in DPS have overlapped signal spectra, and the requirement for sharp pulse shaping filter is waived. Criterion for

spectral shaping pulse selection to achieve CSI free between the two data streams is derived. The major contributions in this chapter are summarized below.

- The framework of DPS and propose exemplified design for the shaping pulses are introduced. Two classes of ideal complementary Nyquist spectral shaping pulses are first provided, which satisfy the CSI-free condition, i.e., the root complementary RC pulses and their 90 degree phase shifted versions (or Hilbert transforms). Making use of spectral shaping pulses from existing commercial D/A devices, two sets of practical pulses for DPS transmission are also proposed, to demonstrate the feasibility of implementing DPS in real high-speed systems.

- System structure for implementing the DPS scheme is presented, and low-complexity equalization methods tailored to DPS are proposed. Equalization at receiver is performed on each of the two data streams individually to remove both the ISI in each stream and the CSI between them. Low-complexity ZF and MMSE linear equalizers are proposed, and their performance is characterized by providing analytical expressions for SNR.

- An example for detailed implementation of the DPS scheme is provided by referring to a practical millimeter wave system that is being developed in our lab. Simulation results on peak-to-average power ratio and BER are presented, and the proposed DPS scheme is compared with conventional single pulse shaping (SPS) ones.

The overall DPS system has almost same computational complexity, implementation cost and power consumption, with negligible BER performance degradation, compared with conventional SPS systems. Moreover, the proposed DPS transmission system solves the problem currently facing high-speed wideband communica-

tions due to the lack of affordable D/A and A/D at high sampling rate such as 10 Gsps or higher.

4.2 DPS with Complementary Nyquist Pulses

4.2.1 Nyquist Theorem

Nyquist pulse shaping is one of the fundamental techniques widely used in digital communications. Let the signal pulse $h(t)$ be a combination of the transmitter filter, the transmission channel, and the receiver filter (ideally a matched filter). When $h(t)$ is a Nyquist pulse, the following condition of ISI-free response is met

$$h\left(nT_s\right) = \begin{cases} 1, & \text{for } n = 0 \\ 0, & \text{for } n \neq 0 \end{cases} \tag{4.1}$$

where T_s is the symbol duration. In the frequency domain, its Fourier transform $H(f)$ satisfies

$$\frac{1}{T_s} \sum_{k=-\infty}^{\infty} H\left(f - k\frac{1}{T_s}\right) = 1. \tag{4.2}$$

Suppose that the digital communication system has a bandwidth (single sided) B. It can be shown that only if $T_s \geq \frac{1}{2B}$ there exists numerous choices for $H\left(f\right)$ such that the superposition of the overlapping replications of $H\left(f\right)$ separated by $\frac{1}{T_s}$ is a constant as indicated by (4.2).

4.2.2 Complementary Nyquist Pulses

In order to improve the spectral efficiency and achieve Nyquist rate transmission at low cost, the concept of DPS transmission is now introduced that uses what we call as *complementary Nyquist pulses*.

Consider a half Nyquist rate system where the data symbols are transmitted at symbol rate $\frac{1}{2T_s}$. Denote $H_N\left(f\right)$ as the frequency-domain representation of a Nyquist

pulse satisfying the condition $\sum_{k=-\infty}^{\infty} H_N\left(f - k\frac{1}{2T_s}\right) = 1$, where the scaling factor $\frac{1}{2T_s}$ is ignored for convenience. The complementary Nyquist pulse is defined as

$$H_{CN}(f) = 1 - H_N(f), \quad -\frac{1}{2T_s} \leq f \leq \frac{1}{2T_s}. \tag{4.3}$$

With the RC pulse shaping, $H_N(f)$ and its the time domain pulse can have the RC spectrum and RC waveform given by

$$H_{RC}(f) = \begin{cases} 1, & |f| \leq \frac{1-\beta}{4T_s} \\ \frac{1}{2}\left[1 + \cos\left(\frac{2\pi T_s}{\beta}\left(|f| - \frac{1-\beta}{4T_s}\right)\right)\right], & \frac{1-\beta}{4T_s} < |f| \leq \frac{1+\beta}{4T_s} \\ 0, & \text{otherwise} \end{cases} \tag{4.4}$$

and

$$h_{RC}(t) = \begin{cases} \frac{1}{2T_s}, & t = 0 \\ \frac{\sin\frac{\pi}{2\beta}}{4\frac{T_s}{\beta}}, & |t| = \frac{T_s}{\beta} \\ \frac{\sin\frac{\pi t}{2T_s}}{\pi t}\frac{\cos\frac{\pi\beta t}{2T_s}}{1-\left(\frac{\beta t}{T_s}\right)^2}, & \text{otherwise} \end{cases} \tag{4.5}$$

respectively, where $0 \leq \beta \leq 1$ is the roll-off factor. The corresponding complementary raised-cosine (CRC) spectra and CRC waveforms then have the following mathematical expressions

$$H_{CRC}(f) = 1 - H_{RC}(f) = \begin{cases} 0, & \text{otherwise} \\ \frac{1}{2}\left[1 - \cos\left(\frac{2\pi T_s}{\beta}\left(|f| - \frac{1-\beta}{4T_s}\right)\right)\right], & \frac{1-\beta}{4T_s} < |f| \leq \frac{1+\beta}{4T_s} \\ 1, & \frac{1+\beta}{4T_s} < |f| \leq \frac{1}{2T_s} \end{cases} \tag{4.6}$$

and

$$h_{CRC}(t) = \frac{\sin\frac{\pi t}{T_s}}{\pi t} - h_{RC}(t) = \begin{cases} \frac{1}{2T_s}, & t = 0 \\ \frac{\sin\frac{\pi}{\beta}}{\pi\frac{T_s}{\beta}} - \frac{\sin\frac{\pi}{2\beta}}{4\frac{T_s}{\beta}}, & |t| = \frac{T_s}{\beta} \\ \frac{\sin\frac{\pi t}{T_s}}{\pi t} - \frac{\sin\frac{\pi t}{2T_s}}{\pi t}\frac{\cos\frac{\pi\beta t}{2T_s}}{1-\left(\frac{\beta t}{T_s}\right)^2}, & \text{otherwise} \end{cases} \tag{4.7}$$

respectively.

With the definition expressed in (4.3), we see that a Nyquist spectrum and its complementary one have a very interesting property, that is, the sum of the two spectra is always a constant within the signal bandwidth. This implies that if two independent data streams are transmitted using the Nyquist pulse shaping and complementary Nyquist pulse shaping respectively, full Nyquist rate can be achieved even though their respective spectra are overlapped. We call it DPS transmission. Note that DPS transmission is a single carrier technique, but different from conventional FDM by which no spectral overlapping is allowed to avoid adjacent channel interference.

4.2.3 CSI-Free Conditions for DPS Transmission

In general, a DPS transmission system can transmit two independent data streams with any pair of spectral shaping pulses as long as the pair of spectral shaping pulses satisfy certain ISI-free and CSI-free conditions.

Denote the signal spectra of the two parallel symbol streams before matched filtering at the receiver as $H_1(f)$ and $H_2(f)$ respectively. After matched filtering, the signal spectra $|H_1(f)|^2$ and $|H_2(f)|^2$ must satisfy the Nyquist ISI-free condition

$$\sum_{k=-\infty}^{\infty} \left| H_1\left(f - k\frac{1}{2T_s}\right)\right|^2 = 1 \tag{4.8}$$

and

$$\sum_{k=-\infty}^{\infty}\left|H_2\left(f-k\frac{1}{2T_s}\right)\right|^2=1 \tag{4.9}$$

where a scaling factor $\frac{1}{2T_s}$ is ignored for convenience. In addition, to prevent the two data streams from interfering each other, $H_1(f)$ and $H_2(f)$ also need to satisfy a further CSI-free condition. Hence, we have the following theorem.

Theorem 1 (CSI-free condition): The necessary and sufficient condition for a DPS transmission system with pulse shaping spectra $|H_1(f)|^2$ and $|H_2(f)|^2$ to satisfy CSI free is that

$$\sum_{k=-\infty}^{\infty}H_1\left(f-k\frac{1}{2T_s}\right)H_2^*\left(f-k\frac{1}{2T_s}\right)=0. \tag{4.10}$$

Proof. Consider the interference from the first data stream to the second one. Since the matched filter used for receiving the second data stream is $H_2^*(f)$, the interference caused by the signal pulse in the first data stream can be expressed as

$$z\left(t\right)=\int_{-\infty}^{\infty}H_1\left(f\right)H_2^*\left(f\right)e^{j2\pi ft}df. \tag{4.11}$$

At any sampling instant $t=n\times 2T_s$, the interference is

$$z\left(n\times 2T_s\right)=\int_{-\infty}^{\infty}H_1\left(f\right)H_2^*\left(f\right)e^{j4\pi nfT_s}df. \tag{4.12}$$

Segmenting the integral into integrals covering the finite range of $\frac{1}{2T_s}$, we obtain

$$\begin{aligned}
z\left(n\times 2T_s\right)&=\sum_{k=-\infty}^{\infty}\int_{\frac{(2k-1)}{4T_s}}^{\frac{(2k+1)}{4T_s}}H_1\left(f\right)H_2^*\left(f\right)e^{j4\pi nfT_s}df\\
&=\sum_{k=-\infty}^{\infty}\int_{\frac{-1}{4T_s}}^{\frac{1}{4T_s}}H_1\left(f-k\frac{1}{2T_s}\right)H_2^*\left(f-k\frac{1}{2T_s}\right)e^{j4\pi nfT_s}df\\
&=\int_{\frac{-1}{4T_s}}^{\frac{1}{4T_s}}\left[\sum_{k=-\infty}^{\infty}H_1\left(f-k\frac{1}{2T_s}\right)H_2^*\left(f-k\frac{1}{2T_s}\right)\right]e^{j4\pi nfT_s}df.
\end{aligned} \tag{4.13}$$

The necessary and sufficient condition for ensuring $z(n\times 2T_s)=0$ for any n is thus given by (4.10).

Similarly, to ensure interference free from the second data stream to the first one, the condition $\sum_{k=-\infty}^{\infty} H_1^* \left(f - k\frac{1}{2T_s}\right) H_2 \left(f - k\frac{1}{2T_s}\right) =$
$\sum_{k=-\infty}^{\infty} H_1 \left(f - k\frac{1}{2T_s}\right) H_2^* \left(f - k\frac{1}{2T_s}\right) = 0$ should be satisfied.

□

4.2.4 Ideal DPS Pulses

The Nyquist pulse and complementary Nyquist pulse with respective shaped spectra of $H_N(f)$ and $H_{CN}(f)$ are applied to two parallel symbol streams. They can be selected as a root Nyquist pulse and a T_s-delayed root complementary Nyquist pulse, i.e., $H_1(f) = \sqrt{H_N(f)}$ and $H_2(f) = \sqrt{H_{CN}(f)}e^{-j2\pi f T_s}$. It can be verified that these two pulses satisfy the conditions specified by Eqs. (4.8), (4.9), and (4.10).

Alternatively, the two pulses can be selected as $H_1(f) = \sqrt{H_N(f)}$ and $H_2(f) = \begin{cases} -j\sqrt{H_{CN}(f)}, & f \geq 0 \\ j\sqrt{H_{CN}(f)}, & f < 0 \end{cases}$, where $H_2(f)$ is a 90 degree phase shifted version of $\sqrt{H_{CN}(f)}$. It can also be verified that these two pulses satisfy the conditions specified by Eqs. (4.8), (4.9), and (4.10). Note that in this case the time domain pulse of $H_2(f)$ is the Hilbert transform of $\sqrt{H_{CN}(f)}$.

For the RRC spectra and pulses given by

$$H_{RRC}(f) = \sqrt{H_{RC}(f)} = \begin{cases} 1, & |f| \leq \frac{1-\beta}{4T_s} \\ \cos\left(\frac{\pi T_s}{\beta}\left(|f| - \frac{1-\beta}{4T_s}\right)\right), & \frac{1-\beta}{4T_s} < |f| \leq \frac{1+\beta}{4T_s} \\ 0, & \text{otherwise} \end{cases} \tag{4.14}$$

and

$$h_{RRC}(t) = \begin{cases} \frac{1}{2T_s} - \frac{\beta}{2T_s} + \frac{2\beta}{\pi T_s}, & t = 0 \\ \frac{\beta}{2\sqrt{2}T_s}\left[\left(1+\frac{2}{\pi}\right)\sin\frac{\pi}{4\beta} + \left(1-\frac{2}{\pi}\right)\cos\frac{\pi}{4\beta}\right], & |t| = \frac{T_s}{2\beta} \\ \frac{\sin\left(\frac{\pi t}{2T_s}(1-\beta)\right)+2\beta\frac{t}{T_s}\cos\left(\frac{\pi t}{2T_s}(1+\beta)\right)}{\pi t\left[1-\left(\frac{2\beta t}{T_s}\right)^2\right]}, & \text{otherwise} \end{cases} \tag{4.15}$$

respectively, the corresponding root complementary raised-cosine (RCRC) spectra and pulses are given by

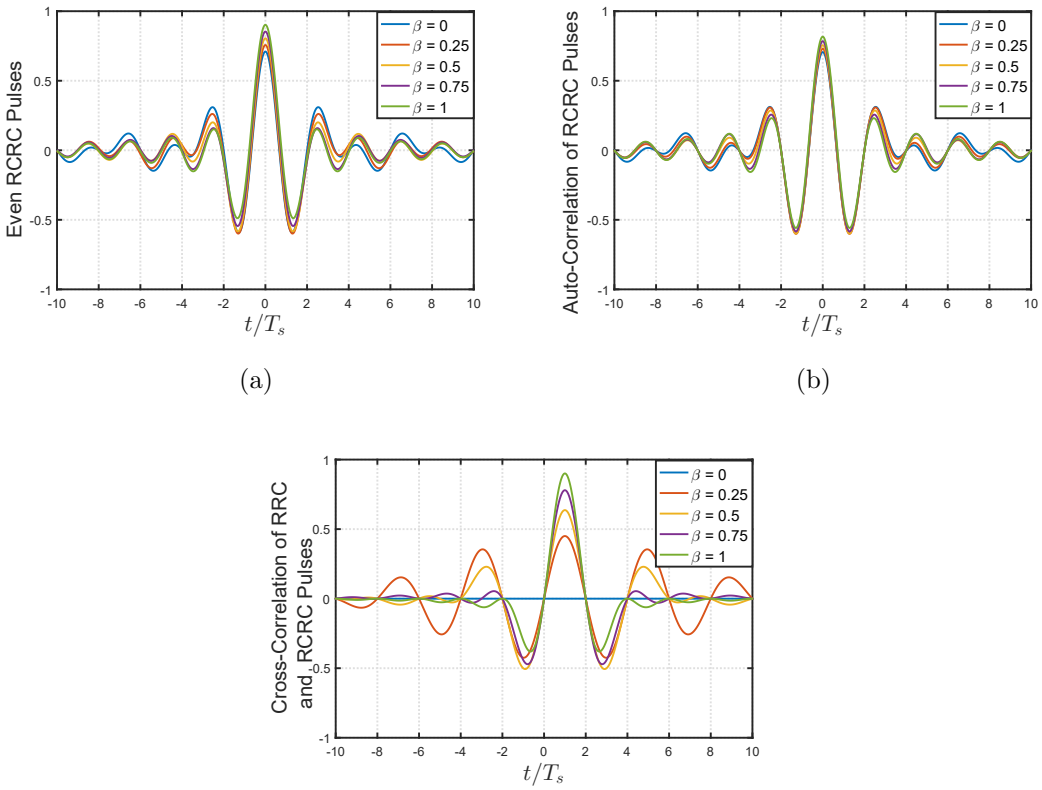
$$H_{RCRC}(f) = \sqrt{H_{CRC}(f)} = \begin{cases} 1, & \frac{1+\beta}{4T_s} < |f| \leq \frac{1}{2T_s} \\ \cos\left(\frac{\pi T_s}{\beta}\left(|f| - \frac{1+\beta}{4T_s}\right)\right), & \frac{1-\beta}{4T_s} < |f| \leq \frac{1+\beta}{4T_s} \\ 0, & \text{otherwise} \end{cases} \tag{4.16}$$

and

$$h_{RCRC}(t) = \begin{cases} \frac{1}{2T_s} - \frac{\beta}{2T_s} + \frac{2\beta}{\pi T_s}, & t = 0 \\ \frac{\sin\frac{\pi}{2\beta}}{\frac{\pi T_s}{2\beta}} - \frac{\beta}{2\sqrt{2}T_s}\left[\left(1+\frac{2}{\pi}\right)\sin\frac{\pi}{4\beta} - \left(1-\frac{2}{\pi}\right)\cos\frac{\pi}{4\beta}\right], & |t| = \frac{T_s}{2\beta} \\ \frac{\sin\frac{\pi t}{T_s}}{\pi t} - \frac{\sin\left(\frac{\pi t}{2T_s}(1+\beta)\right)-2\beta\frac{t}{T_s}\cos\left(\frac{\pi t}{2T_s}(1-\beta)\right)}{\pi t\left[1-\left(\frac{2\beta t}{T_s}\right)^2\right]}, & \text{otherwise} \end{cases} \tag{4.17}$$

respectively. The waveform of $h_{RCRC}(t)$ is shown in Figure (4.1)(a), which is an even function. Figure (4.1)(b) shows the auto-correlation of $h_{RCRC}(t)$. We can find that the value of auto-correlation is zero at $t = \pm 2T_s,\ \pm 4T_s, \cdots$. That means, the RCRC pulse satisfies the ISI-free condition.

The cross-correlation between $h_{RRC}(t)$ and $h_{RCRC}(t - T_s)$ can be computed as $h_{RRC}(t) \otimes h_{RCRC}(t - T_s) = \frac{1}{\pi T_s}\frac{\beta}{1-\left(\beta\frac{t-T_s}{T_s}\right)^2}\sin\frac{\pi t}{2T_s}\cos\left(\pi\beta\frac{t-T_s}{2T_s}\right)$, and is shown in Figure (4.1)(c). The function is zero at $t = 0,\ \pm 2T_s,\ \pm 4T_s, \cdots$, meaning that there is no CSI between the two parallel symbol streams if $h_{RRC}(t)$ and $h_{RCRC}(t - T_s)$ are used as the transmission pulses for the two parallel symbol streams.



(a) (b)

(c)

Figure 4.1 : Waveforms of (a) RCRC pulses, (b) auto-correlation of RCRC pulses, and (c) cross-correlation of RRC and RCRC pulses.

Corresponding to the 90 degree phase shifted version of $h_{RCRC}(t)$ with spectra

$$H_{ORCRC}(f) = \begin{cases} -j\sqrt{H_{CRC}(f)}, & f \geq 0 \\ j\sqrt{H_{CRC}(f)}, & f < 0, \end{cases} \tag{4.18}$$

the odd root complementary raised-cosine (ORCRC) pulse is expressed as

$$h_{ORCRC}(t) = \begin{cases} 0, & t = 0 \\ -\frac{\cos\frac{\pi}{2\beta}}{\pi\frac{T_s}{2\beta}} + \frac{\beta}{2\sqrt{2}T_s}\left[\left(1-\frac{2}{\pi}\right)\sin\frac{\pi}{4\beta} + \left(1+\frac{2}{\pi}\right)\cos\frac{\pi}{4\beta}\right], & t = \frac{T_s}{2\beta} \\ \frac{\cos\frac{\pi}{2\beta}}{\pi\frac{T_s}{2\beta}} - \frac{\beta}{2\sqrt{2}T_s}\left[\left(1-\frac{2}{\pi}\right)\sin\frac{\pi}{4\beta} + \left(1+\frac{2}{\pi}\right)\cos\frac{\pi}{4\beta}\right], & t = -\frac{T_s}{2\beta} \\ -\frac{\cos\frac{\pi t}{T_s}}{\pi t} + \frac{\cos\left(\frac{\pi t}{2T_s}(1+\beta)\right)+2\beta\frac{t}{T_s}\sin\left(\frac{\pi t}{2T_s}(1-\beta)\right)}{\pi t\left[1-\left(\frac{2\beta t}{T_s}\right)^2\right]}, & \text{otherwise.} \end{cases} \tag{4.19}$$

Its waveforms with different values of β are shown in Figure (4.2)(a). We see that $h_{ORCRC}(t)$ is an odd function. Figure (4.2)(b) shows the auto-correlation of $h_{RCRC}(t)$. We can find that the value of auto-correlation is zero at $t = \pm 2T_s,\ \pm 4T_s, \cdots$. That means, ORCRC pulse satisfies the ISI-free condition too.

The cross-correlation between $h_{RRC}(t)$ and $h_{ORCRC}(t)$ can be expressed as $h_{RRC}(t) \otimes h_{ORCRC}(t) = \frac{1}{\pi T_s}\frac{\beta}{1-\left(\beta\frac{t}{T_s}\right)^2}\sin\frac{\pi t}{2T_s}\cos\left(\pi\beta\frac{t}{2T_s}\right)$. It is zero at $t = 0,\ \pm 2T_s,\ \pm 4T_s, \cdots$, meaning that there is no CSI between the two parallel symbol streams if $h_{RRC}(t)$ and $h_{ORCRC}(t)$ are used as the transmission pulses for them. The waveform of the cross-correlation is shown in Figure (4.2)(c).

The above ideal dual RC and complementary RC pulse shaping spectra are band-limited with bandwidth $\frac{1}{T_s}$ and the dual pulse transmission can achieve the full Nyquist rate of $\frac{1}{T_s}$ without ISI and CSI regardless of the roll-off factor. However, the roll-off factor does affect the PAPR of the transmitted signal. Since each parallel data stream only transmits at half Nyquist rate, it is possible to use low sampling rate digital hardware to implement a dual pulse transmission and hence reduce the implementation cost.

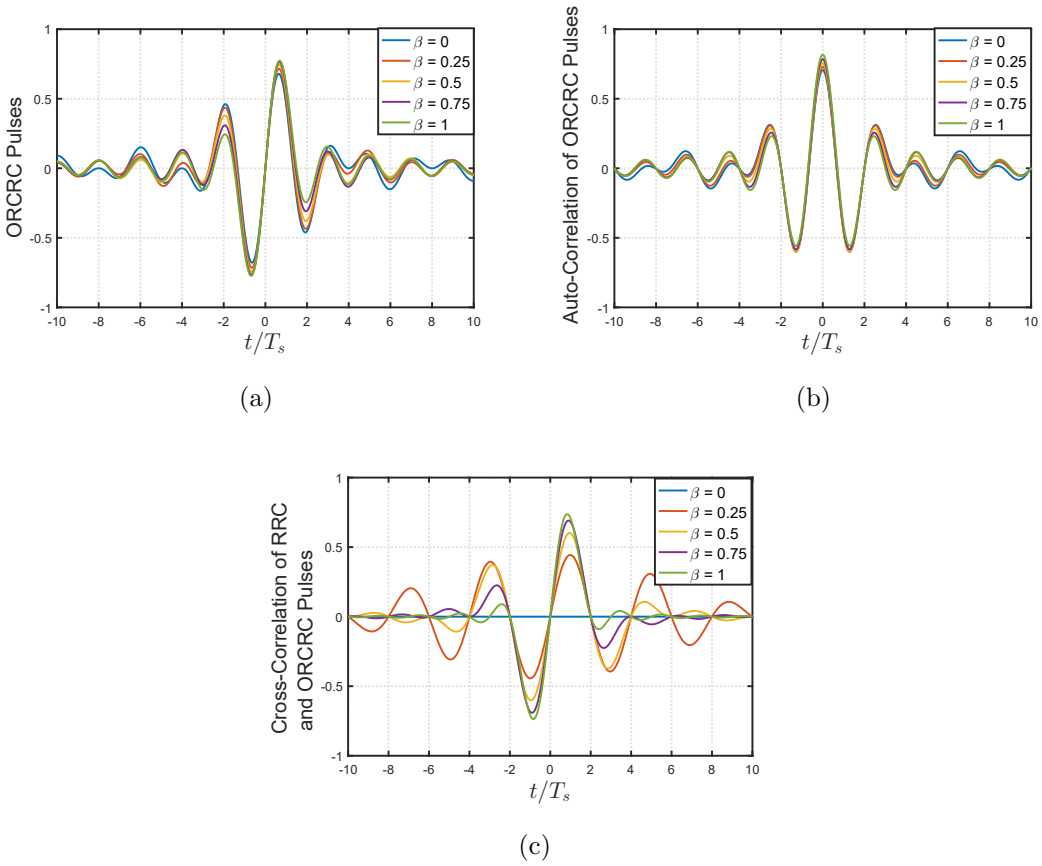


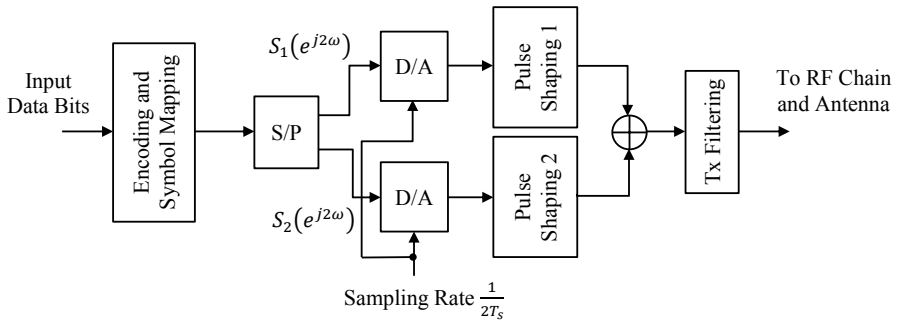
Figure 4.2 : Waveforms of (a) ORCRC pulses, (b) auto-correlation of ORCRC pulses, and (c) cross-correlation of RRC and ORCRC pulses.

4.3 Equalization with Non-Ideal Pulses

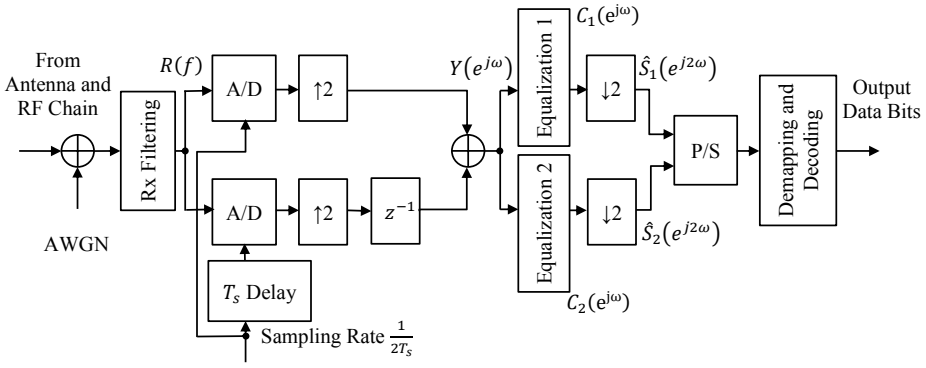
The above proposed complementary Nyquist pulses are non-causal and hence can hardly be used in practical systems. In addition, due to transmission channel distortion, the ISI and CSI free conditions described in Eqs (4.8), (4.9), and (4.10) may not be satisfied. Therefore, equalization is always necessary. Now, we propose a half sampling rate DPS transmission system with two practical equalization techniques, so that high-speed wireless communications can be achieved with practically available low-cost hardware.

4.3.1 System and Signal Models

The block diagram of the DPS transmission system with half symbol rate D/As and A/Ds is shown in Figure (4.3). The RF chains (such as the up and down converters, high power amplifier and low noise amplifier, etc.) and antennas are not shown for simplicity.



(a)



(b)

Figure 4.3 : Dual pulse shaping transmitter (a) and receiver (b).

At the transmitter side, the input data bits are firstly encoded and mapped into data symbols with symbol duration T_s. The serial data symbol stream is split into two half-rate parallel data symbol streams by a serial-to-parallel converter (S/P) which can be easily implemented by digital signal processor, such as FPGA. The two parallel data symbol streams are converted into analog signals by the D/As

with sampling rate equal to half symbol rate. After passing through the two pulse shaping filters respectively, the two parallel data symbol streams form two separate spectrally shaped signals which are then combined and filtered by a transmitter (Tx) filter to form the transmitted baseband signal.

At the receiver side, the received baseband signal is firstly filtered by a receiver (Rx) filter. Then, two digital signal streams are obtained by sampling the received baseband signal using the A/Ds with sampling rate equal to half of the symbol rate, followed by up-sampling by a ratio of two. Note that the clock of the A/Ds for sampling the second data stream have T_s delay. With the second data stream delayed by one sample, the combined digital signal stream is equalized by two equalization filters which operate at symbol rate and down sampled by a ratio of two respectively to recover the two streams of the transmitted data symbols. A parallel-to-serial converter (P/S) merges the two data symbol streams into one serial data symbol stream, followed by de-mapping and decoding to retrieve the transmitted information bits.

From the architecture of transmission system shown in Figure (4.3), we see that each equalizer deals with one data stream with half rate, and two equalizers together achieve full data rate. As each equalizer operates at half rate, the computational complexity of the DPS is almost the same as that of a full speed single pulse shaping system.

4.3.2 Received and Equalized Signal Models

Suppose that the data symbols to be transmitted are represented by a discrete sequence $s(n)$. After S/P, the two parallel data symbol streams can be represented as $s_1(\frac{n}{2}) = \begin{cases} s(n) & \text{for even } n \\ 0 & \text{for odd } n \end{cases}$ and $s_2(\frac{n}{2}) = \begin{cases} s(n+1) & \text{for even } n \\ 0 & \text{for odd } n \end{cases}$ respectively. The Fourier transforms of the two parallel sequences can be expressed as $S_1(e^{j2\omega})$ and $S_2(e^{j2\omega})$ which are periodic functions of ω with period π. Let $H_1(f)$ and $H_2(f)$

denote the frequency responses (the combinations of the respective pulse shaping filter, Tx filter, and Rx filter) for the DPS channels, respectively, and let $W(f)$ denote the noise in the frequency domain. The received signal after the Rx filter in the frequency domain is then expressed as

$$R(f) = H_1(f)S_1(e^{j4\pi fT_s}) + H_2(f)S_2(e^{j4\pi fT_s}) + W(f) \tag{4.20}$$

where the relationship $\omega = 2\pi fT_s$ between the digital frequency ω and the analog frequency f is used. Note that at the input of the A/Ds with T_s clock delay, the signal will appear as a T_s advanced version of $R(f)$ with frequency domain expression $e^{j2\pi fT_s}R(f)$.

After sampling at $\frac{1}{2T_s}$ and then up-sampling by 2, the two received parallel digital signals can be expressed in frequency domain as

$$\begin{aligned} Y_1\left(e^{j\omega}\right) &= \frac{1}{2T_s}\sum_{k=-\infty}^{\infty} R\left(\frac{\omega}{2\pi T_s} - k\frac{1}{2T_s}\right) \\ &= S_1\left(e^{j2\omega}\right)\frac{1}{2T_s}\sum_{k=-\infty}^{\infty} H_1\left(\frac{\omega}{2\pi T_s} - k\frac{1}{2T_s}\right) \\ &+ S_2\left(e^{j2\omega}\right)\frac{1}{2T_s}\sum_{k=-\infty}^{\infty} H_2\left(\frac{\omega}{2\pi T_s} - k\frac{1}{2T_s}\right) \\ &+ \frac{1}{2T_s}\sum_{k=-\infty}^{\infty} W\left(\frac{\omega}{2\pi T_s} - k\frac{1}{2T_s}\right) \end{aligned} \tag{4.21}$$

and

$$\begin{aligned} Y_2\left(e^{j\omega}\right) &= \frac{1}{2T_s}\sum_{k=-\infty}^{\infty} e^{j2\pi\left(\frac{\omega}{2\pi T_s} - k\frac{1}{2T_s}\right)T_s} R\left(\frac{\omega}{2\pi T_s} - k\frac{1}{2T_s}\right) \\ &= e^{j\omega}\frac{1}{2T_s}\sum_{k=-\infty}^{\infty} (-1)^k R\left(\frac{\omega}{2\pi T_s} - k\frac{1}{2T_s}\right) \\ &= e^{j\omega}S_1\left(e^{j2\omega}\right)\frac{1}{2T_s}\sum_{k=-\infty}^{\infty} (-1)^k H_1\left(\frac{\omega}{2\pi T_s} - k\frac{1}{2T_s}\right) \\ &+ e^{j\omega}S_2\left(e^{j2\omega}\right)\frac{1}{2T_s}\sum_{k=-\infty}^{\infty} (-1)^k H_2\left(\frac{\omega}{2\pi T_s} - k\frac{1}{2T_s}\right) \\ &+ e^{j\omega}\frac{1}{2T_s}\sum_{k=-\infty}^{\infty} (-1)^k W\left(\frac{\omega}{2\pi T_s} - k\frac{1}{2T_s}\right) \end{aligned} \tag{4.22}$$

respectively.

After applying one sample delay to $Y_2\left(e^{j\omega}\right)$ and adding it to $Y_1\left(e^{j\omega}\right)$, the received signal has the frequency domain expression

$$\begin{aligned}
&Y\left(e^{j\omega}\right) = Y_1\left(e^{j\omega}\right) + e^{-j\omega}Y_2\left(e^{j\omega}\right) \\
&= S_1\left(e^{j2\omega}\right)\frac{1}{2T_s}\sum_{k=-\infty}^{\infty}\left(1+(-1)^k\right)H_1\left(\frac{\omega}{2\pi T_s}-k\frac{1}{2T_s}\right) \\
&+ S_2\left(e^{j2\omega}\right)\frac{1}{2T_s}\sum_{k=-\infty}^{\infty}\left(1+(-1)^k\right)H_2\left(\frac{\omega}{2\pi T_s}-k\frac{1}{2T_s}\right) \\
&+ \frac{1}{2T_s}\sum_{k=-\infty}^{\infty}\left(1+(-1)^k\right)W\left(\frac{\omega}{2\pi T_s}-k\frac{1}{2T_s}\right) \\
&= S_1\left(e^{j2\omega}\right)\frac{1}{2T_s}\sum_{k=-\infty}^{\infty}H_1\left(\frac{\omega}{2\pi T_s}-k\frac{1}{T_s}\right) \\
&+ S_2\left(e^{j2\omega}\right)\frac{1}{2T_s}\sum_{k=-\infty}^{\infty}H_2\left(\frac{\omega}{2\pi T_s}-k\frac{1}{T_s}\right) \\
&+ \frac{1}{2T_s}\sum_{k=-\infty}^{\infty}W\left(\frac{\omega}{2\pi T_s}-k\frac{1}{T_s}\right) \\
&= \widetilde{H}_1\left(e^{j\omega}\right)S_1\left(e^{j2\omega}\right) + \widetilde{H}_2\left(e^{j\omega}\right)S_2\left(e^{j2\omega}\right) + \widetilde{W}\left(e^{j\omega}\right)
\end{aligned} \tag{4.23}$$

where

$$\widetilde{H}_1\left(e^{j\omega}\right) = \frac{1}{2T_s}\sum_{k=-\infty}^{\infty}H_1\left(\frac{\omega}{2\pi T_s}-k\frac{1}{T_s}\right), \tag{4.24}$$

$$\widetilde{H}_2\left(e^{j\omega}\right) = \frac{1}{2T_s}\sum_{k=-\infty}^{\infty}H_2\left(\frac{\omega}{2\pi T_s}-k\frac{1}{T_s}\right), \tag{4.25}$$

and

$$\widetilde{W}\left(e^{j\omega}\right) = \sum_{k=-\infty}^{\infty}W\left(\frac{\omega}{2\pi T_s}-k\frac{1}{T_s}\right) \tag{4.26}$$

are the digital DPS channel frequency responses and noise frequency domain representation equivalent to the analog DPS channel frequency responses and noise frequency domain representation sampled at $\frac{1}{T_s}$ respectively.

From (4.23), the digital frequency domain received signal model can be expressed

in matrix form as

$$\mathbf{Y}(\omega) = \mathbf{H}(\omega)\mathbf{S}(\omega) + \mathbf{W}(\omega), \text{ for } 0 \leq \omega < \pi \tag{4.27}$$

where $\mathbf{Y}(\omega) = \begin{bmatrix} Y(e^{j\omega}) \\ Y(e^{j(\omega-\pi)}) \end{bmatrix}$, $\mathbf{S}(\omega) = \begin{bmatrix} S_1(e^{j2\omega}) \\ S_2(e^{j2\omega}) \end{bmatrix}$, $\mathbf{H}(\omega) = \begin{bmatrix} \widetilde{H}_1(e^{j\omega}) & \widetilde{H}_2(e^{j\omega}) \\ \widetilde{H}_1(e^{j(\omega-\pi)}) & \widetilde{H}_2(e^{j(\omega-\pi)}) \end{bmatrix}$ and $\mathbf{W}(\omega) = \begin{bmatrix} \widetilde{W}(e^{j\omega}) \\ \widetilde{W}(e^{j(\omega-\pi)}) \end{bmatrix}$.

Denote the frequency responses of the two digital equalizers as $C_1(e^{j\omega})$ and $C_2(e^{j\omega})$ respectively. We apply the equalizers and then down-sample the equalized signal by a factor of 2, leading to spectral overlapping. The outputs are the estimates of the transmitted signals, and can be expressed in the frequency domain as

$$\hat{S}_1(e^{j2\omega}) = C_1(e^{j\omega})Y(e^{j\omega}) + C_1(e^{j(\omega-\pi)})Y(e^{j(\omega-\pi)}) \tag{4.28}$$

and

$$\hat{S}_2(e^{j2\omega}) = C_2(e^{j\omega})Y(e^{j\omega}) + C_2(e^{j(\omega-\pi)})Y(e^{j(\omega-\pi)}), \tag{4.29}$$

or, in the matrix form

$$\hat{\mathbf{S}}(\omega) = \begin{bmatrix} \hat{S}_1(e^{j2\omega}) \\ \hat{S}_2(e^{j2\omega}) \end{bmatrix} = \begin{bmatrix} C_1(e^{j\omega}) & C_1(e^{j(\omega-\pi)}) \\ C_2(e^{j\omega}) & C_2(e^{j(\omega-\pi)}) \end{bmatrix} \mathbf{Y}(\omega) \tag{4.30}$$

for $0 \leq \omega < \pi$. The equalizers $C_1(e^{j\omega})$ and $C_2(e^{j\omega})$ can be determined according to the equalization techniques as will be discussed in the rest of this section. After converting $C_1(e^{j\omega})$ and $C_2(e^{j\omega})$ into time-domain impulse responses, the symbol rate equalizers can be implemented as time-domain linear filters in practical systems.

4.3.3 ZF Equalization

With ZF equalization, the transmitted signal can be recovered from (4.27) as

$$\hat{\mathbf{S}}(\omega) = \begin{bmatrix} \hat{S}_1(e^{j2\omega}) \\ \hat{S}_2(e^{j2\omega}) \end{bmatrix} = \mathbf{H}^{-1}(\omega)\mathbf{Y}(\omega) = \mathbf{S}(\omega) + \mathbf{H}^{-1}(\omega)\mathbf{W}(\omega). \tag{4.31}$$

The inverse channel matrix can be calculated as

$$\mathbf{H}^{-1}(\omega) = \frac{\begin{bmatrix} \widetilde{H}_2(e^{j(\omega-\pi)}) & -\widetilde{H}_2(e^{j\omega}) \\ -\widetilde{H}_1(e^{j(\omega-\pi)}) & \widetilde{H}_1(e^{j\omega}) \end{bmatrix}}{\widetilde{H}_1(e^{j\omega})\widetilde{H}_2(e^{j(\omega-\pi)}) - \widetilde{H}_2(e^{j\omega})\widetilde{H}_1(e^{j(\omega-\pi)})}. \tag{4.32}$$

The frequency responses of the equalizers are then obtained from the inverse channel matrix via the relationship in (4.31) as

$$C_1(e^{j\omega}) = \begin{cases} \frac{\widetilde{H}_2(e^{j(\omega-\pi)})}{\widetilde{H}_1(e^{j\omega})\widetilde{H}_2(e^{j(\omega-\pi)}) - \widetilde{H}_2(e^{j\omega})\widetilde{H}_1(e^{j(\omega-\pi)})}, 0 \le \omega < \pi \\ \frac{-\widetilde{H}_2(e^{j(\omega+\pi)})}{\widetilde{H}_1(e^{j(\omega+\pi)})\widetilde{H}_2(e^{j\omega}) - \widetilde{H}_2(e^{j(\omega+\pi)})\widetilde{H}_1(e^{j\omega})}, -\pi \le \omega < 0 \end{cases} \tag{4.33}$$

and

$$C_2(e^{j\omega}) = \begin{cases} \frac{-\widetilde{H}_1(e^{j(\omega-\pi)})}{\widetilde{H}_1(e^{j\omega})\widetilde{H}_2(e^{j(\omega-\pi)}) - \widetilde{H}_2(e^{j\omega})\widetilde{H}_1(e^{j(\omega-\pi)})}, & 0 \le \omega < \pi \\ \frac{\widetilde{H}_1(e^{j(\omega+\pi)})}{\widetilde{H}_1(e^{j(\omega+\pi)})\widetilde{H}_2(e^{j\omega}) - \widetilde{H}_2(e^{j(\omega+\pi)})\widetilde{H}_1(e^{j\omega})}, & -\pi \le \omega < 0. \end{cases} \tag{4.34}$$

After equalization, the two received pulse shaping spectra in the digital domain become $H_{11}(e^{j\omega}) = \widetilde{H}_1(e^{j\omega})C_1(e^{j\omega})$ and $H_{22}(e^{j\omega}) = \widetilde{H}_2(e^{j\omega})C_2(e^{j\omega})$ respectively. We can verify that the ISI-free conditions, i.e., $\sum_{k=-\infty}^{\infty} H_{11}\left(e^{j2\pi(f-k\frac{1}{2T_s})T_s}\right) = 1$ and $\sum_{k=-\infty}^{\infty} H_{22}(e^{j2\pi(f-k\frac{1}{2T_s})T_s}) = 1$ are both satisfied. The cross-interference spectra in the digital domain become $H_{12}(e^{j\omega}) = \widetilde{H}_1(e^{j\omega})C_2(e^{j\omega})$ and $H_{21}(e^{j\omega}) = \widetilde{H}_2(e^{j\omega})C_1(e^{j\omega})$. And the CSI-free conditions, i.e., $\sum_{k=-\infty}^{\infty} H_{12}(e^{j2\pi(f-k\frac{1}{2T_s})T_s}) = 0$ and $\sum_{k=-\infty}^{\infty} H_{21}(e^{j2\pi(f-k\frac{1}{2T_s})T_s}) = 0$, are also satisfied.

The performance of ZF equalization can be evaluated by computing the SNR for equalized signals as stated by the follow theorem.

Theorem 2 (SNR after ZF equalization): For a DPS transmission system with channel matrix $H(\omega)$, given the SNR at the receiver input γ, the output SNR after ZF equalization is

$$\gamma_{ZF} = \gamma \frac{4\pi^2}{\int_0^{\pi} \|\mathbf{H}(\omega)\|^2 d\omega \int_0^{\pi} \|\mathbf{H}^{-1}(\omega)\|^2 d\omega} \tag{4.35}$$

where $\|.\|^2$ stands for the squared Frobenius Norm of a matrix, i.e., the sum of the absolute squares of its elements.

Proof. Assume that the transmitted signal samples are independent with power spectral density s^2 and the noise is Additive white Gaussian noise (AWGN) with power spectral density σ^2. With the inverse channel matrix $\mathbf{H}^{-1}(\omega)$, the signal power spectral density after ZF equalization is the same as the transmitted signal spectral density. From (4.31), the noise power spectral density after ZF equalization is

$$\begin{aligned} & E\left\{\left\|\mathbf{H}^{-1}(\omega)\,\mathbf{W}(\omega)\right\|^2\right\} \\ &= E\left\{tr\left\{\mathbf{H}^{-1}(\omega)\,\mathbf{W}(\omega)\left(\mathbf{H}^{-1}(\omega)\,\mathbf{W}(\omega)\right)^H\right\}\right\} \\ &= tr\left\{\mathbf{H}^{-1}(\omega)\,E\left\{\mathbf{W}(\omega)\,\mathbf{W}^H(\omega)\right\}\left(\mathbf{H}^{-1}(\omega)\right)^H\right\} \\ &= \sigma^2 tr\left\{\mathbf{H}^{-1}(\omega)\left(\mathbf{H}^{-1}(\omega)\right)^H\right\} \\ &= \sigma^2\left\|\mathbf{H}^{-1}(\omega)\right\|^2 \end{aligned} \tag{4.36}$$

where $(.)^H$ stands for matrix conjugate and transpose, and $tr\{.\}$ stands for the trace of a matrix. Hence, the output SNR is

$$\gamma_{ZF} = \frac{\int_{-\pi}^{\pi} s^2 d\omega}{\int_0^{\pi} \sigma^2 \|\mathbf{H}^{-1}(\omega)\|^2 d\omega} = \rho\frac{2\pi}{\int_0^{\pi}\|\mathbf{H}^{-1}(\omega)\|^2 d\omega} \tag{4.37}$$

where $\rho = \frac{s^2}{\sigma^2}$ is the ratio between signal power at transmitter and noise power at receiver. The signal power spectral density at the input of the receiver is

$$\begin{aligned} & E\left\{\|\mathbf{H}(\omega)\,\mathbf{S}(\omega)\|^2\right\} \\ &= E\left\{tr\left\{\mathbf{H}(\omega)\,\mathbf{S}(\omega)\left(\mathbf{H}(\omega)\,\mathbf{S}(\omega)\right)^H\right\}\right\} \\ &= tr\left\{\mathbf{H}(\omega)\,E\left\{\mathbf{S}(\omega)\,\mathbf{S}^H(\omega)\right\}\mathbf{H}^H(\omega)\right\} \\ &= s^2 tr\left\{\mathbf{H}(\omega)\,\mathbf{H}^H(\omega)\right\} = s^2\|\mathbf{H}(\omega)\|^2. \end{aligned} \tag{4.38}$$

Hence, the SNR at the input of the receiver can be evaluated as

$$\gamma = \frac{\int_0^{\pi} s^2\|\mathbf{H}(\omega)\|^2 d\omega}{\int_{-\pi}^{\pi}\sigma^2 d\omega} = \rho\frac{\int_0^{\pi}\|\mathbf{H}(\omega)\|^2 d\omega}{2\pi}. \tag{4.39}$$

From (4.39) and (4.37), we get (4.36). □

4.3.4 MMSE Equalization

With MMSE equalization, the equalizer frequency responses can be obtained from $\mathbf{G}(\omega)$ for $0 \leq \omega < \pi$, which is given by

$$\mathbf{G}(\omega) = \begin{bmatrix} G_{11}(\omega) & G_{12}(\omega) \\ G_{21}(\omega) & G_{22}(\omega) \end{bmatrix} = \mathbf{H}^H(\omega)(\mathbf{H}(\omega)\mathbf{H}^H(\omega) + \frac{1}{\rho}\mathbf{I})^{-1} \tag{4.40}$$

where $\mathbf{I}$ is a 2×2 identity matrix. The equalizer frequency responses are then obtained as

$$C_1(e^{j\omega}) = \begin{cases} G_{11}(\omega), & 0 \leq \omega < \pi \\ G_{12}(\omega + \pi), & -\pi \leq \omega < 0 \end{cases} \tag{4.41}$$

and

$$C_2(e^{j\omega}) = \begin{cases} G_{21}(\omega), & 0 \leq \omega < \pi \\ G_{22}(\omega + \pi), & -\pi \leq \omega < 0. \end{cases} \tag{4.42}$$

For the performance of MMSE equalization, we have the following theorem.

Theorem 3 (SNR after MMSE equalization): For a DPS transmission system with channel matrix $\mathbf{H}(\omega)$, given the SNR at the receiver input γ, the output SNR after the MMSE equalization is

$$\gamma_{MMSE} = \frac{2\pi}{\int_0^\pi tr\left\{\mathbf{I} - \mathbf{H}^H(\omega)\left(\mathbf{H}(\omega)\mathbf{H}^H(\omega) + \frac{\int_0^\pi \|\mathbf{H}(\omega)\|^2 d\omega}{2\pi\gamma}\mathbf{I}\right)^{-1}\mathbf{H}(\omega)\right\} d\omega} - 1. \tag{4.43}$$

Proof. Based on the MMSE principle, the equalization matrix $G(\omega)$ should be designed such that

$$E\left\{\|\mathbf{G}(\omega)\mathbf{Y}(\omega) - \mathbf{S}(\omega)\|^2\right\} \to min. \tag{4.44}$$

According to the orthogonality principle, to minimize (4.44), we should have

$$\begin{aligned} &E\left\{(\mathbf{G}(\omega)\mathbf{Y}(\omega) - \mathbf{S}(\omega))\mathbf{Y}^H(\omega)\right\} \\ &= \mathbf{G}(\omega)E\left\{\mathbf{Y}(\omega)\mathbf{Y}^H(\omega)\right\} - E\left\{\mathbf{S}(\omega)\mathbf{Y}^H(\omega)\right\} = 0. \end{aligned} \tag{4.45}$$

Assuming that the transmitted signals are statistically independent with power spectral density s^2 and the noise is AWGN with power spectral density σ^2, we have

$$\begin{aligned} & E\left\{\mathbf{Y}(\omega)\mathbf{Y}^H(\omega)\right\} \\ &= E\left\{\left(\mathbf{H}(\omega)\mathbf{S}(\omega)+\mathbf{W}(\omega)\right)\left(\mathbf{H}(\omega)\mathbf{S}(\omega)+\mathbf{W}(\omega)\right)^H\right\} \\ &= s^2\mathbf{H}(\omega)\mathbf{H}^H(\omega)+\sigma^2\mathbf{I} \end{aligned} \tag{4.46}$$

and

$$\begin{aligned} & E\left\{\mathbf{S}(\omega)\mathbf{Y}^H(\omega)\right\} \\ &= E\left\{\mathbf{S}(\omega)\left(\mathbf{H}(\omega)\mathbf{S}(\omega)+\mathbf{W}(\omega)\right)^H\right\} = s^2\mathbf{H}^H(\omega). \end{aligned} \tag{4.47}$$

Substituting (4.46) and (4.47) into (4.45), we obtain $\mathbf{G}(\omega)$ as expressed in (4.40).

The MMSE is

$$\begin{aligned} & E\left\{\left\|\mathbf{G}(\omega)\mathbf{Y}(\omega)-\mathbf{S}(\omega)\right\|^2\right\} \\ &= E\left\{tr\left\{\left(\mathbf{G}(\omega)\mathbf{Y}(\omega)-\mathbf{S}(\omega)\right)\left(\mathbf{G}(\omega)\mathbf{Y}(\omega)-\mathbf{S}(\omega)\right)^H\right\}\right\} \\ &= tr\left\{E\left\{\left(\mathbf{G}(\omega)\mathbf{Y}(\omega)-\mathbf{S}(\omega)\right)\mathbf{Y}^H(\omega)\right\}\right\} \\ &+ tr\left\{E\left\{\left(\mathbf{S}(\omega)-\mathbf{G}(\omega)\mathbf{Y}(\omega)\right)\mathbf{S}^H(\omega)\right\}\right\} \\ &= tr\left\{E\left\{\left(\mathbf{S}(\omega)-\mathbf{G}(\omega)\mathbf{Y}(\omega)\right)\mathbf{S}^H(\omega)\right\}\right\} \\ &= s^2 tr\left\{\mathbf{I}-\mathbf{G}(\omega)\mathbf{H}(\omega)\right\}. \end{aligned} \tag{4.48}$$

The SNR after MMSE equalization is

$$\begin{aligned} \gamma_{MMSE} &= \frac{\int_{-\pi}^{\pi} s^2 d\omega - \int_0^{\pi} s^2 tr\left\{\mathbf{I}-\mathbf{G}(\omega)\mathbf{H}(\omega)\right\} d\omega}{\int_0^{\pi} s^2 tr\left\{\mathbf{I}-\mathbf{G}(\omega)\mathbf{H}(\omega)\right\} d\omega} \\ &= \frac{2\pi}{\int_0^{\pi} tr\left\{\mathbf{I}-\mathbf{G}(\omega)\mathbf{H}(\omega)\right\} d\omega} - 1. \end{aligned} \tag{4.49}$$

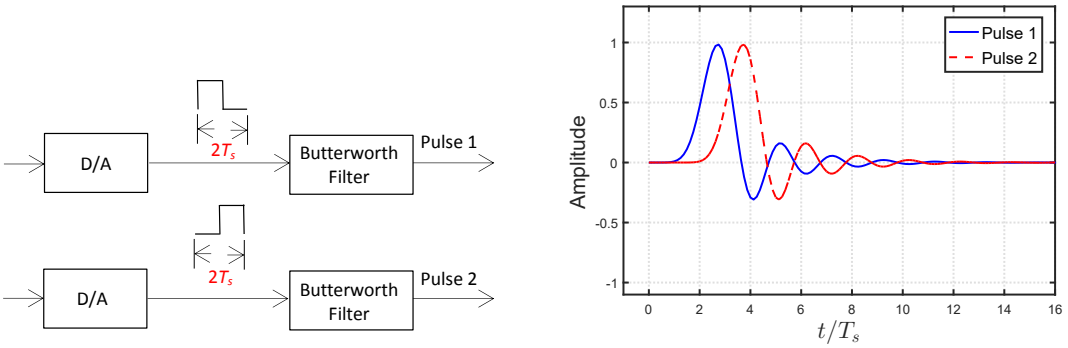
Expressing ρ in terms of γ and substituting it into (4.40), and then substituting the resulting $\mathbf{G}(\omega)$ into (4.49), we obtain (4.43). □

4.4 Simulation Results

To demonstrate the performance of the proposed DPS transmission system for high-speed low-cost mm-wave communications, we now present the simulation re-

sults for a 25 Gbps system with 5 GHz bandwidth operating in the 71-76/81-86 GHz E-band. The sampling rate required for this system is only 2.5 Gsps which is easily achieved with commercial A/D and D/A devices at low cost. The 64-QAM is used to provide 6 bps/Hz spectral efficiency over 5 GHz bandwidth, achieving 30 Gbps raw data rate including some necessary overhead for synchronization, channel estimation, and other system functionalities.

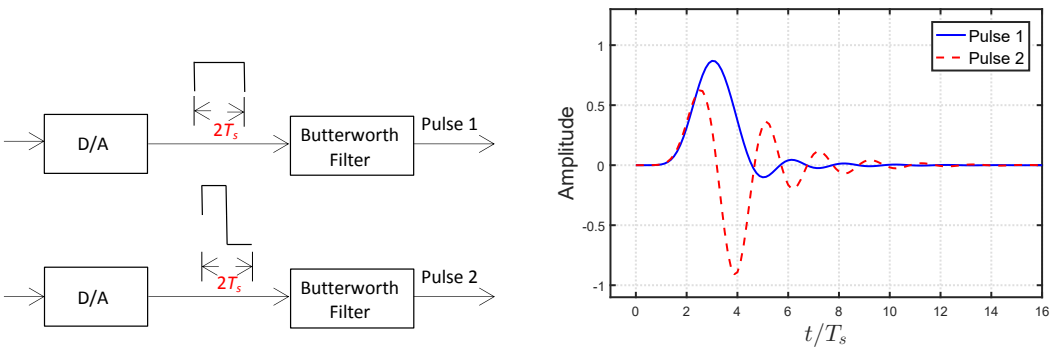
From the data-sheet of the commercial D/As [91], the D/A cores operate in three modes: normal mode (or non-return-to-zero (NRZ) mode), mix mode (or Manchester mode), and return-to-zero (RZ) mode. Two schemes for practical spectral shaping pulse selection are proposed. The first scheme uses a RZ rectangular pulse and its T_s delayed version shown in Figure 4.4(a). After Tx filtering with a 10th order Butterworth low-pass filter, the two spectral shaping pulses are shown in Figure 4.4(b). The second scheme uses a NRZ pulse and a Manchester pulse shown in Figure 4.5(a). The spectral shaping pulses after the same Tx filter are shown in Figure 4.5(b).



(a) (b)

Figure 4.4 : Dual pulse shaping scheme 1.

The frequency responses of the two pulses for each scheme are shown in Figure 4.6. We can find that the two data streams of each DPS scheme have overlapped



(a) (b)

Figure 4.5 : Dual pulse shaping scheme 2.

signal spectra. For comparison purpose, a RRC spectrum with roll-off factor $\beta = 0.15$ used for conventional Nyquist pulse shaping is also shown.

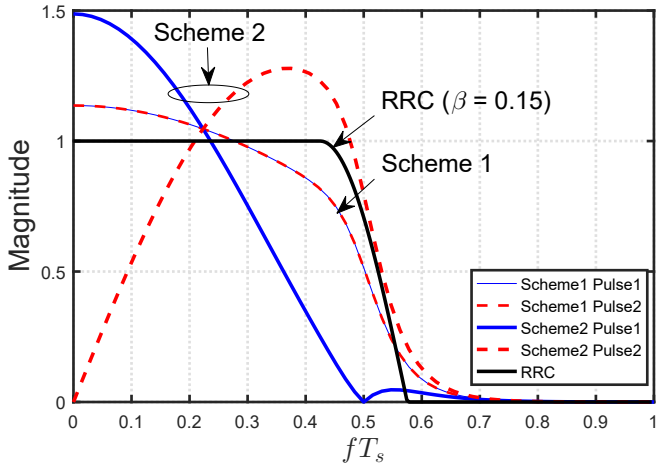


Figure 4.6 : Dual pulse shaping and RRC spectra.

We first compare the PAPR performance between DPS and SPS with Nyquist pulse, and the results are shown in Figure 4.7. We see that DPS has slightly increased PAPR compared to SPS.

We then compare the (uncoded) BER performance between the two pulse shaping

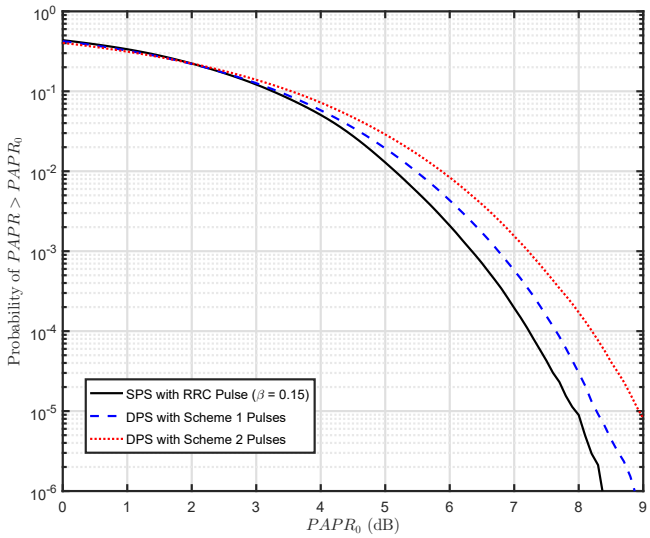


Figure 4.7 : PAPR comparison.

schemes for both ZF and MMSE equalization, and present the results in Figure 4.8 under ideal condition without considering any practical impairment. In AWGN channels, the two pulse shaping schemes achieve almost the same performance for ZF and MMSE equalizations respectively (only ZF performances are displayed). The performance gap between DPS and SPS is very small. The multipath fading channels are generated based on a two-ray model, where the first path is fixed to 1, and the second path is generated following complex Gaussian distribution with mean zero and variance 0.5. The second path is 6 ns behind the first one. With the multipath channels, DPS scheme 2 achieves lower BER than scheme 1, and approaches the SPS performance.

4.5 Conclusion

A DPS scheme where transmitter and receiver can use D/As and A/Ds with sampling rate equal to only half of the data symbol rate is proposed. By introducing the concept of complementary Nyquist pulse, a DPS transmission scheme

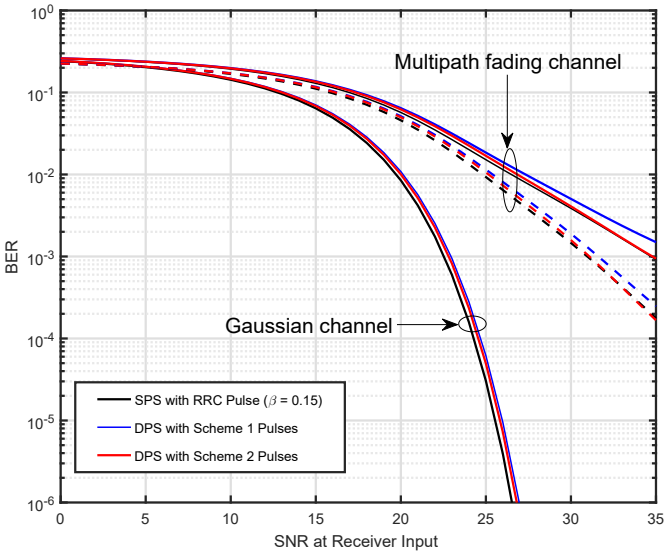


Figure 4.8 : BER comparison (solid and dashed lines for ZF and MMSE equalization, respectively).

is proposed, which can achieve Nyquist rate with half rate sampling satisfying the CSI-free condition. Two classes of ideal ISI and CSI free spectral shaping pulses are formulated referring to the RRC spectra. Low-compleixty ZF and MMSE equalizers are derived and allow for practical dual spectral shaping pulses to be used. Two sets of practical pulses are proposed and simulated to verify the feasibility of the DPS transmission and equalization techniques. Simulation results show that the DPS transmission system can achieve similar BER performance with slightly increased PAPR, compared to conventional single pulse shaping systems. The proposed DPS scheme provides a practical and cost-effective solution for high-speed communications when very high sampling-rate conversion devices are unattainable or too costly.

Chapter 5

High-Speed Digital Modem Implementation for Wireless Communications at 0.325 THz

5.1 Introduction and Literature Review

With ever increasing demand for wireless data transmissions, future wireless communication systems will require very high throughput with hundreds of Gbps or higher data rate. It becomes obvious that bandwidth of future wireless communication systems will increase to tens of GHz, especially for backhaul systems. Broadband wireless communication systems using THz frequencies have recently attracted significant interests because of huge potential applications by opening a super wide untethered bandwidth from 100 GHz to 10 THz for new services.

Due to relatively lower loss for the carrier frequencies in the 100 – 300 GHz bands, several THz communication systems have been reported in recent years. A 2×40 Gbps wireless communication system using 0.14 THz band oritho-mode transducer is shown in [92]. A fully electronic 90 Gbps one meter wireless link at 230 GHz is presented in [93], and the hardware implementation with parallel sequence spread spectrum (PSSS) modulation using 230 GHz RF frontend is also reported in [94]. With 300 GHz carrier frequencies, a 56-Gbps 16-QAM wireless link is demonstrated in [95]. In these researches, the transmitted signals are all generated by the arbitrary waveform generator (AWG) or signal generator and the received data are analyzed by digital analyzers or high performance oscilloscopes. There is no baseband platform connecting IF module or/and THz frontend to transmit or receive data from/to medium access control (MAC) layer to form a complete communication system.

There are some experimental systems which connect the baseband platform in either off-line or real-time mode. In [96], a fixed wireless link at 240 GHz carrier frequency is presented with a sampling rate of 64 Gsps. Due to the high sampling rate, the signal processing has to be performed off-line. A 300 GHz CMOS transceiver for THz wireless communication is described in [97] which can achieve 20 Gbps with a lower sampling rate. A real-time wireless communication system at 0.14 THz is presented in [98], which has throughput of 5 Gbps and a bandwidth of 1.8 GHz respectively.

However, in all the of above mentioned systems, high-speed data rate and real-time signal processing are not achieved at the same time. In a real-time system, an FPGA is the most important part for the baseband platform to implement the digital signal processing (DSP) modules, such as encoder/decoder, modulation/demodulation and channel estimation. There are two typical ways to implement DSP modules with FPGA or application specific integrated circuit (ASIC), i.e., the high-level synthesis (HLS) language and the low-level language such as hardware description language (HDL). The HLS language has attracted interests for the system implementation in recent years. Different applications using HLS are shown in [99] and [100]. In both works, the resource usage of typical cells such as multipliers, BRAMs and LUTs is less than 43% and the clock speed can only achieve 200 MHz. For achieving tens or hundreds of Gbps data rate for wideband wireless communication systems, high-speed system clock such as that of more than 300 MHz is necessary to reduce the resource usage. Otherwise, it is very difficult to implement all DSP modules in one or two affordable FPGA devices for wideband communication systems. With low-level language, there are a large number of implementations available for typical modules of communication systems, such as low density parity check (LDPC) or Turbo decoder, channel estimation and synchronization. However, there are few systems which are implemented with all physical layer DSP modules

for wideband communication links. Moreover, for the ISTN, the power and volume are severely limited on satellites. Therefore, it is necessary to optimize each module for implementing high-speed wireless system in the digital modem.

In this chapter, a high-speed low-complexity digital modem for wireless communications at 0.325 THz is presented. The basic system requirements, architectures and signal processing modules at both transmitter and receiver sides are described. Implementations of some typical modules included Ethernet interface, transmitter filter and receiver filter are presented. Following the description of FPGA structure, some key strategies are elaborated when implementing algorithms in FPGA. The implementation and experimental results for digital modem are shown. Finally, the integrations with IF modules and THz RF front-end are described and the experimental results of the integrated system are provided.

5.2 System Description

5.2.1 System Requirements

The backhaul system under development is required to provide up to 20 Gbps information data rate. The actual data rate at physical layer (PHY) can be adjusted according to the speed of the MAC layer. At the maximum speed of 20 Gbps, the BER is required to be lower than 10^{-7} at 14 dB normalized SNR. When the PHY date rate is reduced, the BER can be further improved. The modulation type is 16-QAM, and the demodulation loss is below 5 dB.

The selection of carrier center frequency depends on the RF band and up/down conversion architecture, which is not the focus of this modem design. However, in order to achieve high-speed transmission between fast moving platforms such as LEO satellites, the modem is required to be able to capture and track significantly large CFO up to tens of Mega Hertz.

5.2.2 System Architecture

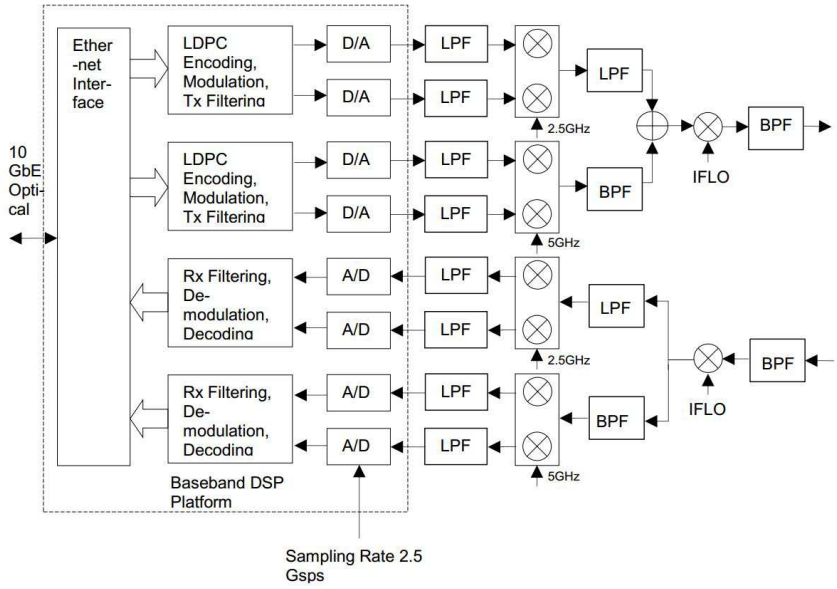


Figure 5.1 : The backhaul system architecture with only half of the proposed 20 Gbps digital modem.

The digital modem is a key component of the high-speed backhaul communication system. Figure 5.1 shows the backhaul system architecture with only half of the proposed 20 Gbps digital modem. The complete digital modem is composed of two baseband digital signal processing platforms, each capable of processing 10 Gbps data rate, and an intermediate frequency (IF) module for transmitter and receiver respectively. When fully operated, the digital modem can transmit and receive Ethernet traffic at 20 Gbps data rate simultaneously.

According to the system design, the 20 Gbps digital modem is equipped with two 10 Gigabit Ethernet (GbE) interfaces. The data bits from one 10 GbE interface are split into two streams, each having 5 Gbps data rate. Each 5 Gbps data stream is transmitted over one 2.5 GHz baseband channel which is shifted to the IF band. There are total four such 2.5 GHz channels for this system. The digital modem consists of two baseband DSP platforms, each having four D/A and A/D devices

respectively. Esach baseband DSP platform is capable of transmission and reception of two 5 Gbps data streams.

At the transmitter, the IF module up-converts the I/Q modulated baseband signals generated by the baseband digital platforms to IF signals. There are total 4 channels of baseband signals, each with 2.5 GHz bandwidth. Two channels are combined to form a 5 GHz bandwidth baseband. These two 5 GHz channels are further up-converted to IF with lower and upper sidebands respectively which are finally combined to form a 10 GHz bandwidth IF signal.

At the receiver, the received IF signal is bandpass filtered to obtain the lower sideband and upper sideband respectively. Each sideband is then down converted to 5 GHz bandwidth baseband signal, and two channels of 2.5 GHz bandwidth baseband signals are finally received by baseband digital platforms. Information data are subsequently demodulated by the digital modem.

5.2.3 Physical Layer Protocol

The PHY layer frame consists of a preamble, pilots and a sequence of symbols carrying data from MAC, as illustrated in Figure 5.2.

Preamble is used for synchronization and channel estimation. The preamble is composed of two blocks, each consisting of 64 samples. The two blocks are sequential and exactly the same.

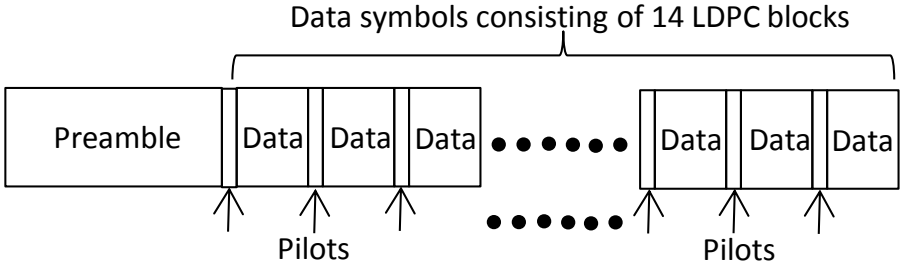


Figure 5.2 : The frame structure of the physical layer protocol.

The pilots in the data symbols are PN-coded symbols corresponding to the constellation points (1+j) or -(1+j). To prevent the generation of spectral lines, each pilot is multiplied by one code of a PN sequence. Each frame starts with the pilot using the first code of the PN sequence, and the PN sequence is not continued between adjacent frames. One Pilot is added in each data block with fixed number of symbols and multiple pilots are spread over the whole frame in order to track the channel variation and compensate for phase noise.

LDPC is known as a coding scheme with performance close to Shannon limit that can achieve very low BERs for low SNR applications [101]. LDPC decoding algorithm has more parallelization, low implementation complexity, low decoding latency, as well as no error-floors at high SNRs and it is considered in the next generation communication standards. The forward error correction uses the 802.11n LDPC code [102] with 1944 bits per block and the coding rate is 3/4. The encoded data bits are then divided into data symbols, using the 16-QAM. There are 252 pilots inserted into 14 LDPC blocks for one PHY frame. There are 1176 clock periods occupied by 14 LDPC blocks and 252 pilots, and 16 clock periods for the preamble. Due to the sampling rate of A/D and D/A are 2.5 Gsps and eight samples are processed in each clock, the system clock frequency is 2.5 Gsps/8 = 312.5 MHz. The total time of one frame is (1176+16)/312.5 MHz $\approx$ 3.82 us. The user data is 1944$\times$3/4$\times$14 = 20412 bits in one frame, therefore, the rate of one band is 20412/3.82 us $\approx$ 5.34 Gbps. For one digital baseband platform, there are two bands implemented separately. As there are two digital baseband platforms in the system, the data rate is 5.34$\times$4=21.36 Gbps, and thus the targeted 20 Gbps data rate can be achieved.

5.3 Signal Processing Modules

5.3.1 Transmitter Signal Processing

The single carrier and I/Q modulation techniques are adopted by each PHY channel. Date symbols with rate 1.875 Gsps are transmitted continuously without guarding interval. At the transmitter, LDPC is used for encoding the data bits from Ethernet interface and then the coded bits are mapped into data symbols using 16-QAM. For each frame, the preamble is added at the start of frame. The data symbols finally go through a RRC pulse shaping filter. Since the signal sampling rate is 2.5 Gsps, SRC is necessary before pulse shaping. The signal processing diagram for the transmitter is shown in Figure 5.3.

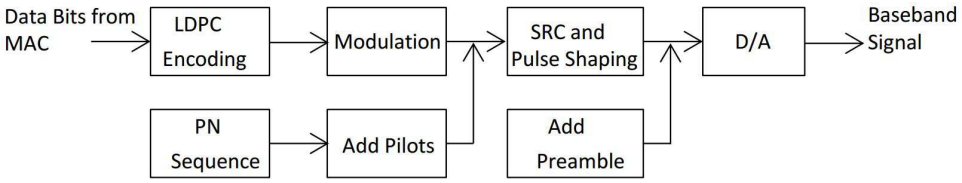


Figure 5.3 : Transmitter signal processing diagram.

5.3.2 Receiver Signal Processing

At the receiver, the first process after receiving data from A/D is frame synchronization for each PHY channel. Once the preamble is captured in this process, it is then used to estimate the channel response, I/Q imbalance, and CFO. The receiver filters, which convert the sample rate to symbol rate and correct all the practical impairments, will be constructed through these estimations. The data demapping and LDPC decoding processes are followed by recovering the data symbols. The signal processing diagram for the receiver is shown in Figure 5.4.

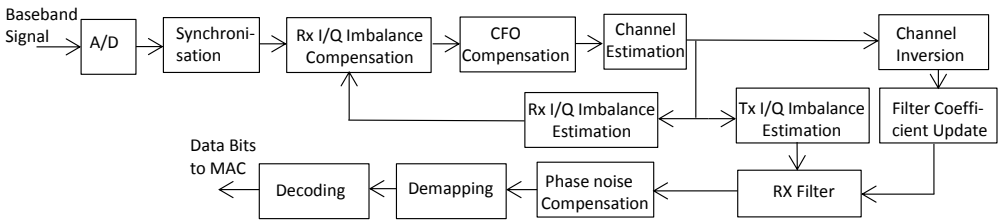


Figure 5.4 : Receiver signal processing diagram.

5.4 Ethernet Interface

5.4.1 Functional Overview

The MAC acts as an interface between the digital modem's PHY layer and the network's physical layer [103]. The MAC can balance network load across two channels when both channels are enabled. One PHY channel may optionally be disabled via the MAC, and PHY channels can also transmit and receive data to/from MAC with fixed length frames. The interface between MAC and PHY is shown in Figure 5.5.

In Figure 5.5 we assume that the radio PHY is split up into sub-layers along the same lines as the IEEE 802.3 Ethernet. The radio physical coding sub-layer (PCS) groups the MAC supplied bit stream into symbols. The FEC block adds an error correcting code. The physical medium attachment (PMA) block performs radio modulation. The physical medium dependent (PMD) block comprises of the digital to analog conversion, IF and RF components.

Considering the reliability and robustness, MAC should preserve Ethernet framing across the radio link. Some additional control characters, which are encoded in-band with the data, are self-synchronized so that MAC functionality can be recovered after any variable bit shift or random data loss.

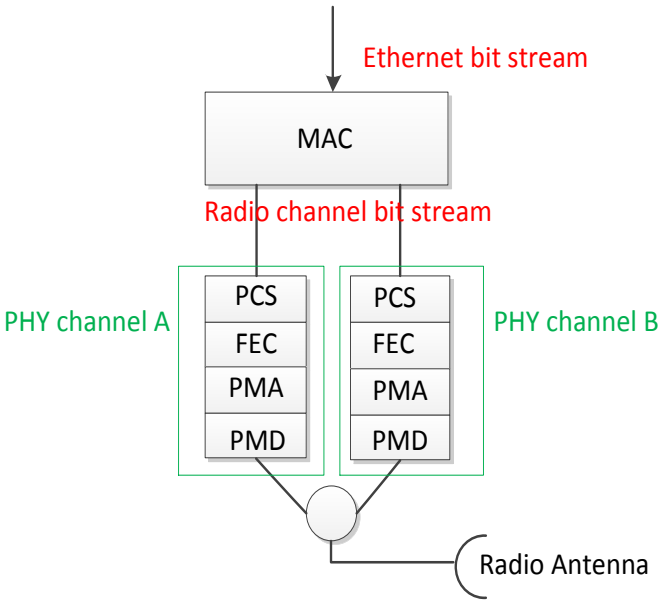


Figure 5.5 : MAC with two PHY channels.

5.4.2 Interfacing Radio PCS

There are several possible architectures for interfacing the radio PCS upper interface to an Ethernet fiber[104], but the most suitable one is the 66B bridge architecture in order to achieve implementation simplicity and low processing delay. Figure 5.6 shows the 66B bridge architecture. The Ethernet PCS block performs the standard Ethernet PCS layer functionality. Native 66 bit blocks are passed directly from the network interface to the MAC. The blocks must be de-scrambled in order to accurately identify the idle control characters that fill in the gaps between Ethernet frames. Idle deletion is important to ensure that buffer memory is utilized efficiently. The Ethernet idle block code can be used for wireless packet padding to keep the transmitter data without guarding interval.

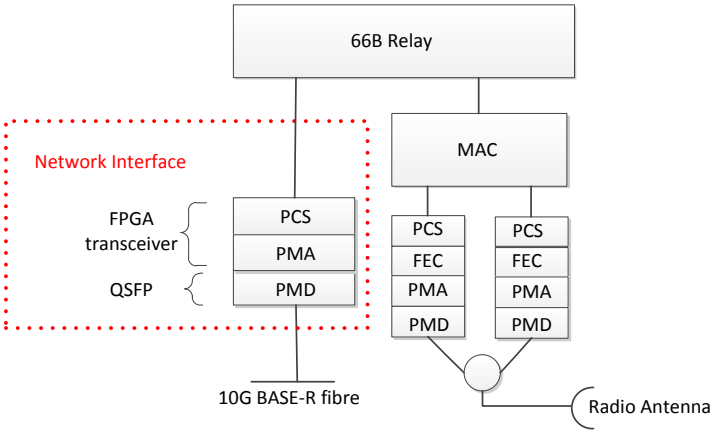


Figure 5.6 : The 66B bridge architecture.

5.4.3 Ethernet Interface Architecture

Figure 5.7 shows the architecture for the MAC interface and 10 GbE packages which are both implemented internally within the FPGA. The lower interface of the MAC package connects to the transmit and receive sides of the two PHY channels. The upper interface of the 10 GbE package is with the GT transceiver.

The idle block insertion and deletion functionalities within the TX FIFO and RX FIFO are necessary for a constant PHY data rate. The PHY's D/A and A/D modules generate the clocks (312.5 MHz) for transmitter and receiver respectively. However, the Ethernet clocks (156 MHz) of the GTX receiver and the GTX transmitter are sourced from the GTX transceiver. The PHY transmitter reads RX FIFO regularly no matter MAC blocks are valid or idle. However, the PHY receiver only sends valid blocks into TX FIFO. Therefore, the MAC should insert and identify the idle blocks for controlling the data rate and sending useful data to the GTX transceiver. The traffic monitor checks the data stream for PHY layer. Ethernet packet framing and checksum errors are calculated in two places at the output of the TX FIFO (Eth_tx) and the output of the RX FIFO (Eth_rx). This is useful for

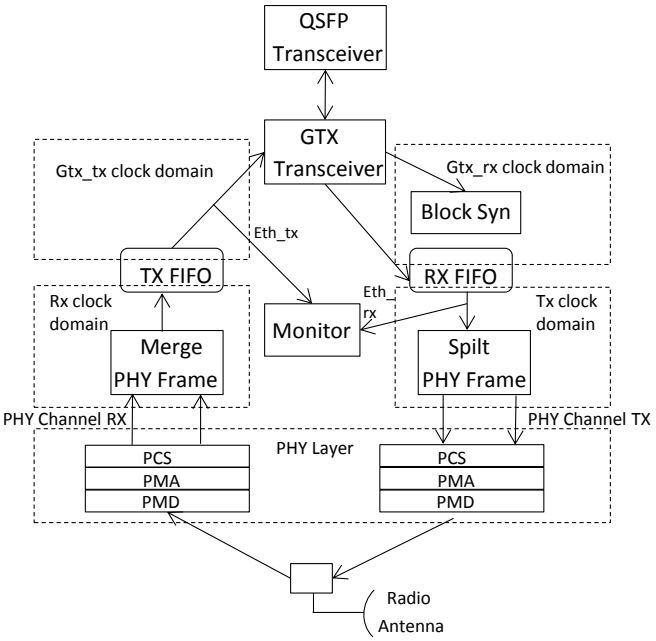


Figure 5.7 : The Ethernet interface architecture.

troubleshooting purposes while the link is operational with user traffic.

5.5 Implementation of Transmitter and Receiver Filters

5.5.1 Transmitter Filter

The design of transmitter filter without or with pre-equalization affects the complexity of channel equalization at the receiver side. In our design, each transmitter filter is an RRC pulse shaping filter with pre-equalization sampled at 2.5 Gsps with different time offset. When pre-equalization is used, coefficients of filters vary with the condition of the IF module. Therefore, filter coefficients can be configured when the FPGA bit-file is generated after channel sounding to determine the channel response of the IF module. In order to be used for wideband system in practice, the length of transmitter filters can not be very small so that the length is chosen as 32 in this design. With different time offsets, each transmitter filter output sample is generated by 24 addition operations with 12 bit width per addition operation, and

eight samples are generated in each FPGA high-speed clock period (312.5 MHz). Considering the filter coefficient configurability and the huge number of addition operations with large word-width, the efficient and effective architecture of transmitter filter is shown in Figure 5.8.

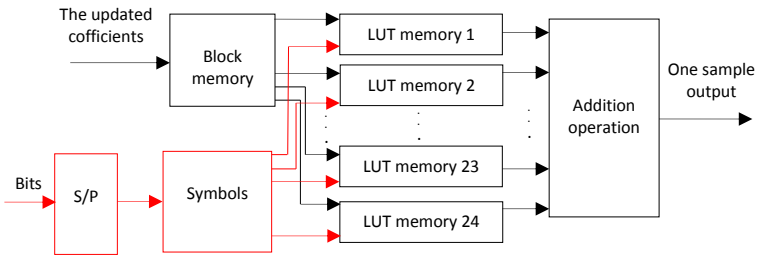


Figure 5.8 : Structure of Tx filter for one sample.

After setting up the digital modem in the IF loopback mode, a special training sequence is sent from the digital baseband platform through the IF module and received by the digital baseband platform. Coefficients for transmitter filters can be calculated by the captured data from the digital receiver. The updated coefficients for different conditions of the IF module can be uploaded into the block memory. The size of coefficients is around 24 Kbits. Due to the sufficient block memories in FPGA[105], it is reasonable to use 1×36 Kbits block memory for storing these coefficients. Following the designed structure of the transmitter filters, one output sample is generated with 24 time offsets in one FPGA clock period. Therefore, coefficients stored in the block memory are divided into 24 small groups, and the size of each group is 1 Kbits. Considering the small size of each small group of coefficients and the minimum of 18 Kbits for each block memory, each small group of coefficients is stored in LUT memory rather than the block memory. At the same time, the structure of LUT memory is optimized for high-speed clock frequency when routing all cells in FPGA. Once coefficients are downloaded into 24 LUT memories,

samples can be generated following the inputs of symbols which are generated from serial-to-parallel converter. The data outputs from 24 LUT memories are added together to generate one output sample.

5.5.2 Receiver Filter

As we know, the length of receiver filters affects the performance and complexity when implementing a practical wireless communication system. Considering these two factors, this design adopts length 54 receiver filters. From Figure 5.9, we can easily find that a large number of multiplications and additions are necessary for the designed receiver filters. Multiplications can be implemented by DSP48 in FPGA[105]. For the addition operations, the length of bits output from DSP48 should be decided for the given precision. In order to achieve good performance, long bit width should be adopted. However, at the same time, the complexity will be increased with the increasing length of bits. Therefore, an appropriate strategy is required to deal with the large number of additions with wide bits. Figure 5.9 shows the effective structure of an addition tree.

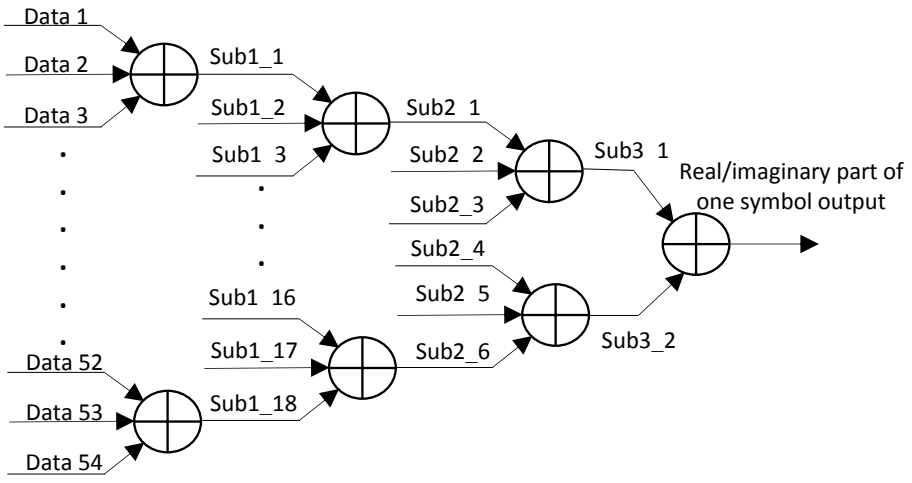


Figure 5.9 : Structure of addition tree for the real/imaginary part of one symbol.

According to the length of receiver filters, there are 54 multiplications for generating 54 data outputs which should be added together. However, we cannot complete all adders in one clock period (312 MHz). Therefore, we divide all adders into four levels. Considering the usage rate and the timing of system clock, we select three data additions in one clock period. In this way, the same resources are needed as that for adding two data in one clock period. At the input of the first level, the length of data bits after multiplications should be long enough to satisfy the given precision requirement. However, after adding each level, the sum of each adder increases. Therefore, one bit can be reduced at the input of next level. With this design, the lengths of input data are 13, 12, 11 and 10 bits for each level respectively. In one clock period, six symbols should be generated and each symbol consits of real and imaginary parts. With this addition tree structure, it is effective to keep the precision while reducing the resource usage.

5.6 Key Strategies for Implementation on FPGA

Before describing the key strategies for implementation on FPGA, let's first describe the structure of FPGA.

5.6.1 FPGA

FPGAs are digital logic devices that can be flexibly programmed to perform a variety of digital functions using a HDL. Their main advantages are their in-field-programmability, as well as their high-speed very-parallel logic processing. Owing to these benefits, FPGAs are desirable for many kinds of applications, including software-defined radio, ASIC prototyping, digital signal processing, cryptography and computer hardware emulation.

There are two main vendors of FPGAs, Xilinx and Altera. Their respective FPGAs exhibit some differences, but also share a number of similarities. Since the

digital modem is implemented on Xilinx's FPGA, let's introduce the FPGA of Xilinx as follows.

The internal structure of an FPGA typically comprises a variable number of four main programmable elements, namely input/output block (IOB), embedded memory, DSP block and configurable logic block (CLB). The FPGA structure shows in Figure 5.10.

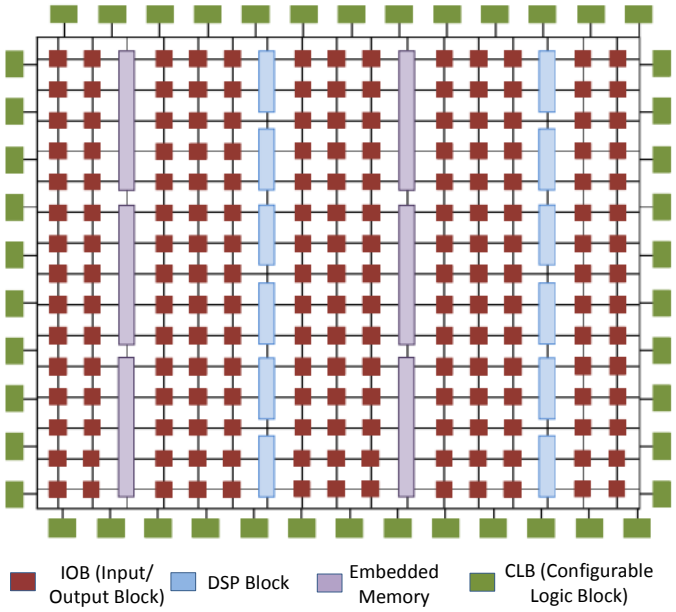


Figure 5.10 : FPGA structure.

An IOB is a collection or grouping of basic elements that implement the input and output functions of an FPGA device.

The embedded memory can be used to generate five types of memories - single-port RAM, simple dual-port RAM, true dual-port RAM, single-port read-only memory (ROM) and dual-port ROM. For dual-port memories, each port operates independently and allows reading and writing to two different locations simultaneously. Operating mode, clock frequency, optional output registers, and optional pins are

selectable per port. For Simple Dual-port RAM, the operating modes are not selectable. The size of these RAM/ROM blocks depends on the particular FPGA being used, as does their access control.

The DSP (or named DSP48) block is an arithmetic logic unit (ALU) embedded into the fabric of the FPGA and is composed of a chain of three different blocks. The computational chain in the DSP48 contains an add/subtract unit connected to a multiplier connected to a final add/subtract/accumulate engine.

A CLB is the basic repeating logic resource on FPGA. When linked together by routing resources, the components in CLBs execute complex logic functions, implement memory functions, and synchronize code on the FPGA. CLBs contain smaller components, including flip-flops (FFs), LUTs, and multiplexers.

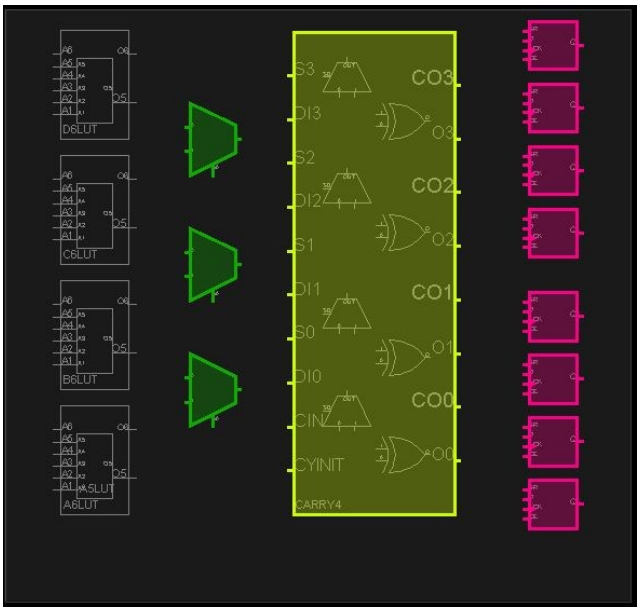


Figure 5.11 : A slice of Virtex 7 FPGA.

Four LUTs and eight FFs as well as multiplexers and arithmetic carry logic form a slice, as shown in Figure 5.11, and two slices form a CLB. The LUTs in Xilinx 7 series FPGAs can be configured as either one 6-input LUT with one output, or

as two 5-input LUTs with separate outputs but common addresses or logic inputs. Each LUT output can optionally be registered in a FF. A LUT is a digital structure that can be programmed to perform any combinatorial function of its inputs, thus completing any possible combination of logic gates. Increasing the number of LUT inputs typically allows the same HDL design to be implemented using fewer LUTs, therefore reducing the amount of FPGA routing required. However, the hardware resources required by a LUT increase exponentially with its number of input bits, hence very large LUTs are impractical. Each FF in a slice is a binary register used to save logic states between clock cycles on an FPGA circuit. The output of each LUT can optionally be connected to a corresponding FF, for facilitating synchronous operation. Alternatively, the LUT output can be connected directly to the other logic blocks. Because one logic block can be programmed to connect any other set of logic blocks, FPGA has the feature of high-speed very-parallel logic processing. However, when achieving high-speed parallel structure, the area of element (resource usage) will be huge. So the balance between the speed of processing and the area of element (resource usage) is hard to achieve when implementing lots of modules in one FPGA device.

Figure 5.12 shows a example when implementing a digital filter. As we known, the digital filter has plenty of addition and multiplication operations. In Figure 5.12 (a), the operation is serial and one time multiplication and addition operation are completed in one clock period. The result of addition operation is used as an input of addition for the following clock period. Due to the number of logic level for each addition is depended on the width of each input data. For simply, considering the 4-input carry chain in popular FPGA currently, the four bits input data is considered for the following description. The logic level is at least two in one clock period, one level for time multiplication and one level for addition. The complexity of routing is low because of less number of operation is needed in the type of serial. If the total

number has four pairs of data which are needed to multiply and add together, there are four clock periods needed to generate the final result. In Figure 5.12 (b), one more multiplication and one more addition are used and the speed of operations is doubled compared with the type of serial. The logic level is at least three in one clock period, one level for time multiplication and two levels for additions. The complexity of routing is medium and it is reasonable for routing the elements on the FPGA. There are two clock periods needed to generate the result for the four pairs of input data. In Figure 5.12 (c), the total number of multiplication and addition are four and three respectively. The logic level is still at least three in one clock period. Although just one clock period is needed to generate the result for the four pairs of input data, the complexity of routing is high and it is a little bit hard to meet the timing constraints for high-speed system clock, especially when high resource usage occurs on one FPGA device.

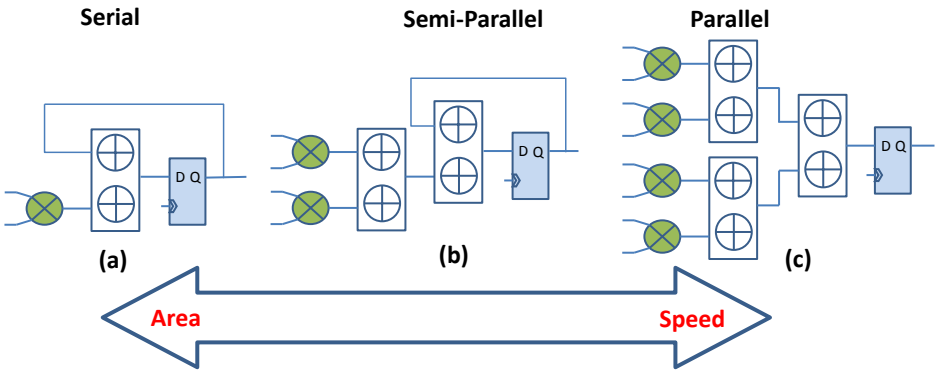


Figure 5.12 : Flexibility feature of FPGA.

5.6.2 Key Strategies

When implementing some DSP modules in FPGA, some key strategies are necessary to be considered for saving more resource and meeting the timing constraints, especially for the high-speed system clocks.

◇ *Strategy 1: Wide Word-Length Addition Operations*

Addition operations are essential when designing the DSP algorithms. The huge number of addition operations with wide word-length occupies lots of LUTs and carry-chains in FPGA. Meanwhile, timing constraints become critical when routing the addition operations, especially with wide word-length. It is not possible to perform lots of operations just in one clock period and hence dividing addition operations into different clock periods is necessary to meet the high-speed system clock timing requirements. Because there are two outputs from one 6-input LUT, three additions in one clock period are adopted in our implementation which occupies the same resources as those of two additions in one clock period. Meanwhile, the logic levels between two registers are kept sufficiently simple for the logic routing to meet high-speed clock timing requirements.

◇ *Strategy 2: BRAM vs Distributed RAM*

When processing all modules, it is necessary to store a certain number of data using the internal memory in FPGA. The BRAM can be used for storing a small number of data. However, timing requirements for the interface of BRAM are difficult to meet, especially when the percentage of occupied BRAM is high and a high-speed system clock is used. Therefore, other kind of memory, the distributed RAM, can be used to replace the BRAM when the size of needed RAM is not very large. Because the distributed RAM is composed of 6-input LUTs, it is quite efficient to use distributed RAM for short address memory, especially the RAM with 64 addresses.

◇ *Strategy 3: Resource Sharing*

There are some modules which are parallelly processed continuously without any idle clock, such as LDPC encoder, Tx filters, Rx filters and LDPC decoder. In this case, the resources which are occupied in each clock period can not be shared.

However, some modules can be processed over a number of clock periods, such as channel estimation. The resources used for channel estimation can be shared in different clock intervals. For example, as we know, the function of FFT requires some resources in FPGA. In our design, each IP core of FFT is shared five times. Moreover, some BRAMs and distributed RAMs are re-used by different functions. Although a certain amount of logics for controlling the interface is necessary, the percentage of these additional resources is quite small compared with that of the saved resources.

◇ *Strategy 4: Optimized Precision*

For the digital modem, a high precision is necessary to achieve better performance. However, to achieve high precision, much more resources are required and it becomes more difficult to meet timing requirements. Therefore, optimized algorithms are needed to reduce the resource usage and maintain the performance at the same time, such as the functions of synchronization and Rx filter. The synchronization consists of coarse timing and fine timing. The coarse timing captures the training sequences in a transmission frame. After this, the fine timing calculates the exact synchronization point from the training sequence segment captured by coarse timing. This implies that the precision of coarse timing can be reduced by using less resources. Although the number of bits for A/Ds is as long as 10, the number of bits used for coarse timing is just 6 in our design. With this reduced precision for coarse timing, the function of synchronization is still achieved and there is no adverse effect on the performance of the whole system. For the Rx filtering, there are lots of taps in the Rx filter for producing one output symbol. For each symbol, there are the same number of addition operations which can be divided into different levels. Since each addition operation contributes a small portion to the final output, the word length of data can be reduced after each addition level and satisfactory performance can still be achieved for the whole system. After algorithm

optimization and implementation, a number of resources are saved and the timing requirements are much easier to be met.

◇ *Strategy 5: Huge Storage Avoidance*

There are four 10 bits A/Ds sampling at 2.5 Gsps, which means that the throughout of raw data is $4 \times 10 \times 2.5 = 100$ Gbps. As we know, the internal memory in FPGA is limited and valuable. The system complexity will be increased if the independent external memory is adopted. It is very less efficient to store a huge number of data in any module when performing DSP in real-time. Therefore, avoiding huge storage is necessary for designing and implementing all DSP modules.

◇ *Strategy 6: Specifying Constraints*

Placing efficient constraints to some processing logics is essential for meeting timing requirements, especially when a high percentage resource usage occurs and/or some high-speed system clocks are used. Even after optimizing the DSP algorithms and the HDL codes, efficient constraints are still necessary to improve the timing when routing the resource in the whole device. In our implementation, some efficient constraints are specified to optimize the routing process and successfully meet timing requirements. Figure 5.13 shows some essential constraints applied to the FPGA device. Due to the large number of multipliers used in the whole device, constraints for more than half of the multipliers are applied. In this way, it is possible to place and route a high percentage of multipliers, the number of which is limited for an FPGA device. The green colored seven columns located on the left side of the device show the multipliers which are restrained. Meanwhile, there are nearly twenty Physical Block (Pblock) constraints which are distributed over in the whole device and each of them is decided after some iterations through the synthesis and implementation stages by Vivado tool.

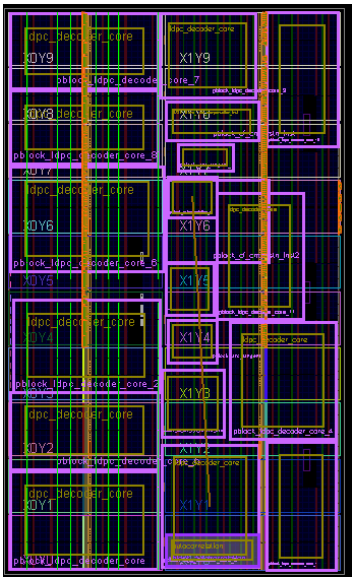


Figure 5.13 : Essential constraints applied to FPGA device.

5.7 Implementation Results

In addition to the transmitter and receiver filters described in Section 5.5, the digital modem also consists of other necessary signal processing modules. At the transmitter side, there are encoding, modulation, transmitter filters and D/A interface modules. At the receiver side, there are synchronization, channel estimation and equalization, receive filters, demodulation, decoding and A/D interface modules. Between the digital modem PHY and the network layer, the 20 Gbps transmitter and receiver fiber interfaces are also implemented. These modules are implemented to deal with high throughput for the wideband system, each being optimized in the FPGA. The signal processing blocks for the main data streams, such as LDPC encoding, 16-QAM mapping, transmit filter, receiver filter, 16-QAM demapping, LDPC decoding, channel estimation, channel equalization and A/D and D/A modules, are shown in Table 5.1. From this table, we can see that resource usage of some typical cells including LUTs, slice registers, BRAMs, multipliers are reasonable for

the whole system compared with the total resources in this device.

Table 5.1 : FPGA Usage of Typical Modules

Module Name	Slice LUTs	Slice Registers	Block RAMs	Multipliers
MAC Fibres	8700	8000	97	0
LDPC Encoder	4240	3900	3	0
TX Filter	11200	15400	8	0
RX Filter	18600	69000	12	1344
LDPC Decoder	120000	144200	182	0
Channel Estimation	19000	32000	10	72
Channel Equalization	7400	20000	20	704
A/D & D/A Interfaces	2000	5000	0	0
Used Number	245800	368600	590	2220
Total Number	433200	866400	1470	3600
Usage Rate	56.7%	42.5%	40%	61.7%

The powerful device, Virtex7-690T produced by Xilinx, is used in our digital baseband platform. Among the total 3600 multipliers in the device, there are 2220 multipliers used. Only the receiver filter module alone has used 1344 multipliers. Considering the limited multipliers in FPGA and high speed system clock, the timing constraints are essential for meeting the timing requirement through effectively alocating the multipliers and, at the same time, adding constraints for specific modules, such as channel estimation and LDPC decoder core. Figure 5.14 shows the route result for the whole system. The yellow cells for the receiver filter are restrained on the left half side of the device due to the large numbers of multipliers used for receiver filter but less other cells used for this module. Therefore, some

other modules, which do not use multiplier, can be placed at the same area of the receiver filter. In this way, it is much easier to meet the timing for the whole system.

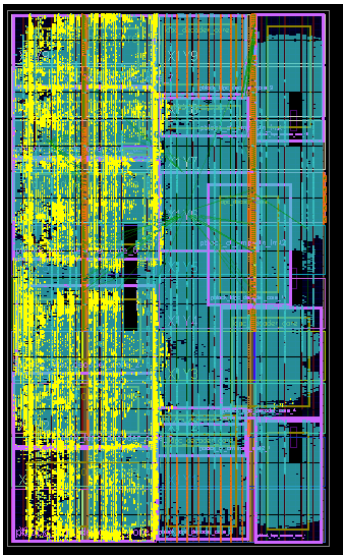
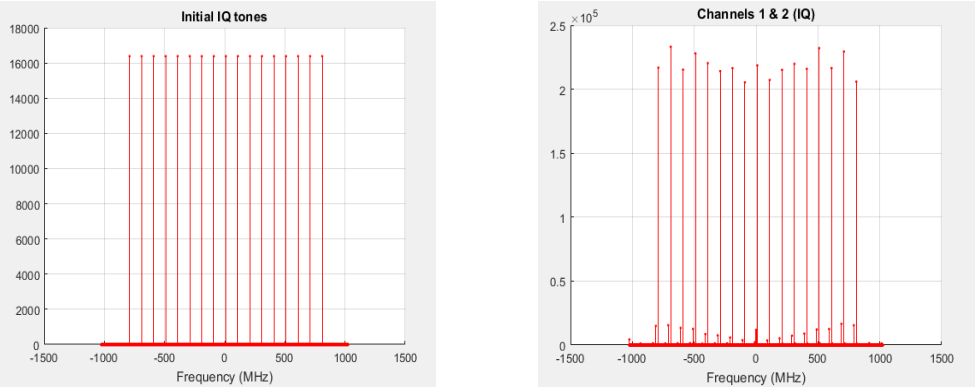


Figure 5.14 : Route result for the whole system.

5.8 Experimental Results of Digital Modem

Before performing real-time system loopback test with IF modules and/or RF frontend, the D/As and A/Ds should be calibrated first. Due to the baseband I/Q modulation architecture, any difference in terms of delay, phase, and amplitude will introduce I/Q imbalance. Figure 5.15 shows the frequency tones used to check I/Q imbalance in the D/A and A/D converter chain, where the left shows the tones (amplitude) to the D/A converters (I and Q channels) and the right shows the tones (amplitude) after A/D converters (I and Q channels). We see that even though every effort has been made to adjust the delays, phases, and the amplitudes of the D/A and A/D converters, there still exists I/Q imbalance indicated by the imaging tones. The residual I/Q imbalance can be compensated by digital signal processing at the receiver.



(a) (b)

Figure 5.15 : Frequency tones used to check I/Q imbalance: tones at input to D/A (a) and tones at output from A/D (b).

After D/A and A/D calibration, the transmitted signal can be looped back via direct D/A and A/D connection. The error vector magnitude (EVM) of the constellation is 4.05% without pre-equalization. Figure 5.16 shows the result of constellation of loop-back via digital modem. From this result, we can make sure that the signal processing produces satisfactory performance for the 16-QAM demodulation without IF module.

5.9 Integration with IF Module

5.9.1 Test Setup

The digital modem is composed of two FPGA platforms, each capable of transmitting and receiving two channels of baseband I/Q signals. Each FPGA platform is connected to a control PC via universal serial bus cable for monitoring and configuring the state of FPGA. The IF transmitter and receiver are connected directly at IF frequency via coaxial cable. A noise generator is used to generate additive Gaussian noise with on/off switch controlled by a spectrum analyzer. A cascade of

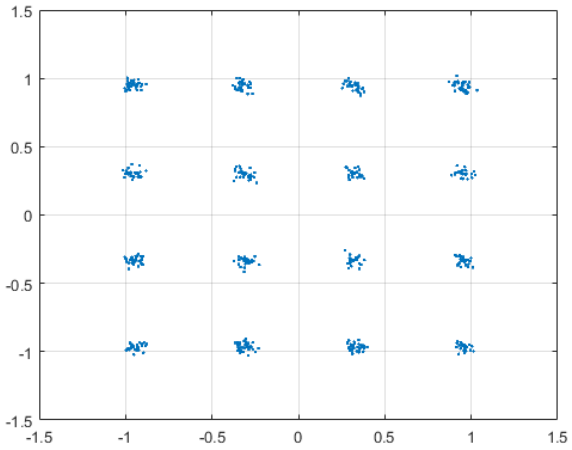


Figure 5.16 : 16-QAM constellation obtained through external baseband loopback.

two wideband amplifiers is used to amplify the noise to sufficient power level. Two attenuators (with 1 dB step and 10 dB step respectively) are used to control the noise level and a switch driver is connected to them to set the attenuation manually. The spectrum analyzer is also used to monitor the transmitted signal power as well as measure both noise and signal powers.

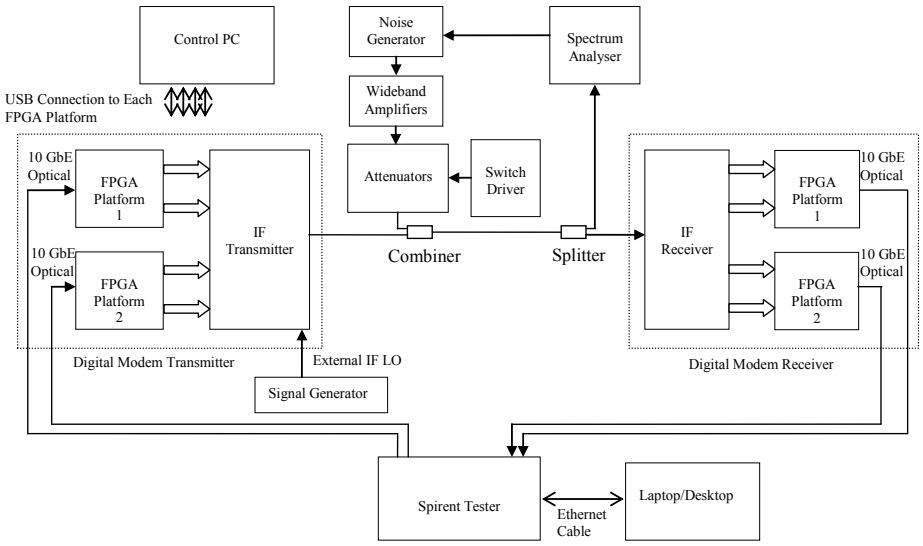


Figure 5.17 : Structure of test setup.

At the transmitter side, two 10 Gbps Ethernet traffic streams generated by the Spirent tester are pseudo-random bit sequences with 128 byte packet size. At the receiver side, the two received 10 Gbps Ethernet traffic streams are fed back to the Spirent tester, and the BER result can be recorded from the user interface window of Spirent tester. Figure 5.17 shows the block diagram of the test setup. A picture of the 20 Gbps digital modem prototype hardware is shown in Figure 5.18. A picture of the IF link connecting the IF transmitter and receiver with additive noise is shown in Figure 5.19. A picture of the spectrum analyzer and the switch driver is shown in Figure 5.20. The signal and noise powers are measured using the marker functions of the spectrum analyzer after properly selecting the marker frequency and the bandwidth. The required noise attenuation can be selected through manually setting the keys on the switch driver.

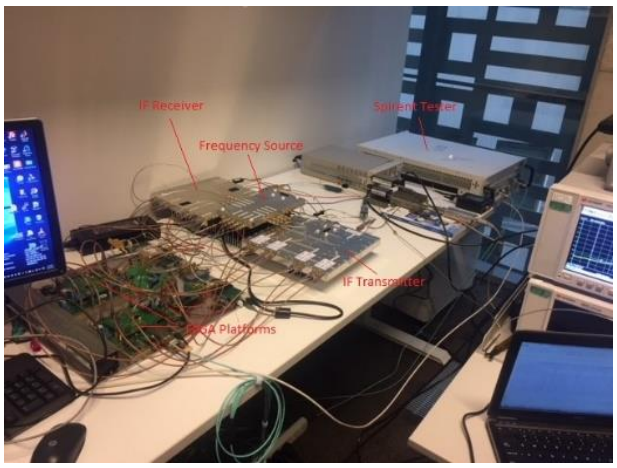


Figure 5.18 : A picture of 20 Gbps digital modem and test setup.

5.9.2 Experimental Results

After verifying the performance of digital modem as described in Section 5.8, the integrated performance of digital modem and IF module can be tested following as the test up in Section 5.9.1. Figure 5.21 shows the four channels of the transmitted IF signals. We can see that there are some local oscillator (LO) leakage in each channel.

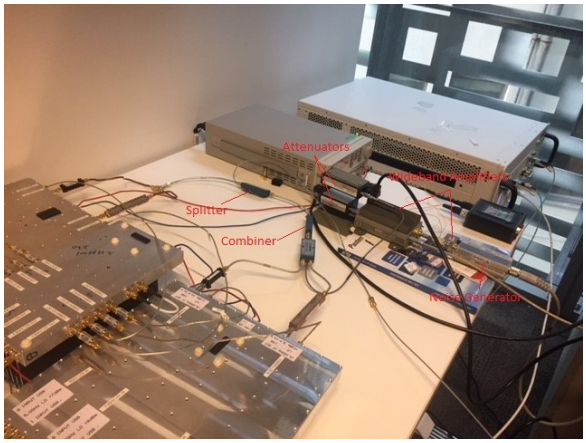


Figure 5.19 : A picture of IF link with additive noise.

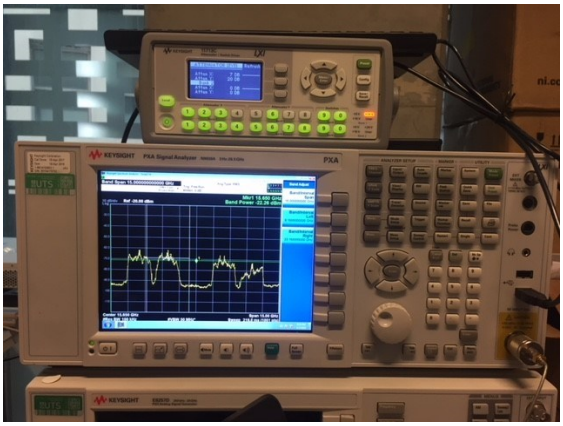


Figure 5.20 : A picture of spectrum analyzer and switch driver.

In addition, the power of the four channels are not balanced when transmitting the same signals from baseband platform. These practical impairments introduce some difficulty to the DSP algorithms.

The test for obtaining the channel frequency response of each channel is performed by transmitting a number of discrete tones throughout the entire bandwidth of each channel. The frequencies of the discrete tones are selected such that their image frequencies appear in-between two original tones, resulting in a shaded area below the frequency response envelope to show the I/Q imbalance. The overall

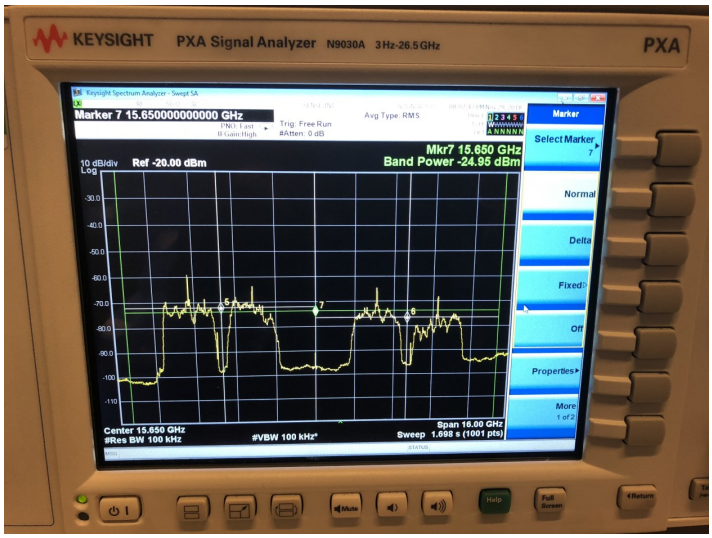


Figure 5.21 : Four channels of IF signal.

channel frequency response including both transmitter and receiver for each channel can be obtained in digital baseband at the receiver side. Figure 5.22 shows the results of four channels calculated using Matlab software after uploading the test data from the digital platform. We see that the channel frequency response fluctuates significantly in the bandwidth of 2.5 GHz. The fluctuated range is around 9 dB. At the same time, the image components of the IF module are also quite severe. This poses significant challenges to the signal processing for recover the transmitted data information. Developing robust algorithms is essential to deal with the impairments from the IF module.

5.9.3 Channel Pre-equalization

Considering the undesirable performance of the IF hardware for the wideband system and in order to reduce the complexity of the whole system as much as possible, an effective way to deal with the significant fluctuation in the channel frequency responses is channel pre-equalization. Figure 5.23 shows transmitter filters without pre-equalization. The filters only have the real part without considering the

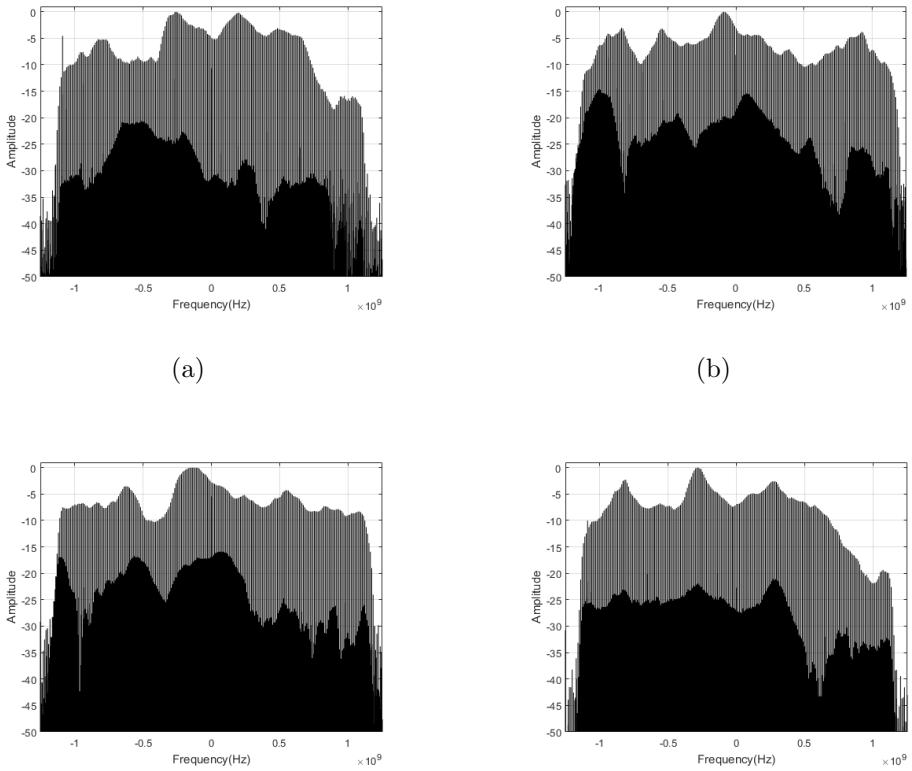


Figure 5.22 : Frequency response of LSB2 (a), LSB1 (b), USB1 (c) and USB2 (d) channels.

influence from IF module. However, after pre-equalization, transmitter filters have changed a lot. Figure 5.24 shows the real part and imaginary part of the transmitter filters with pre-equalization. From this result, we can see that the characters of the signal to be transmitted via the IF module have changed significantly after pre-equalization.

At the receiver side, the characteristics of the channel can be shown from receiver filters. Figure 5.25 shows real part of receiver filters without and with pre-equalization (considering the small value of imaginary part, it is not necessary to show imaginary part). Considering the limited resource in the FPGA, we can

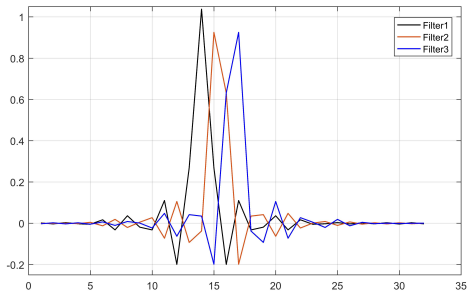
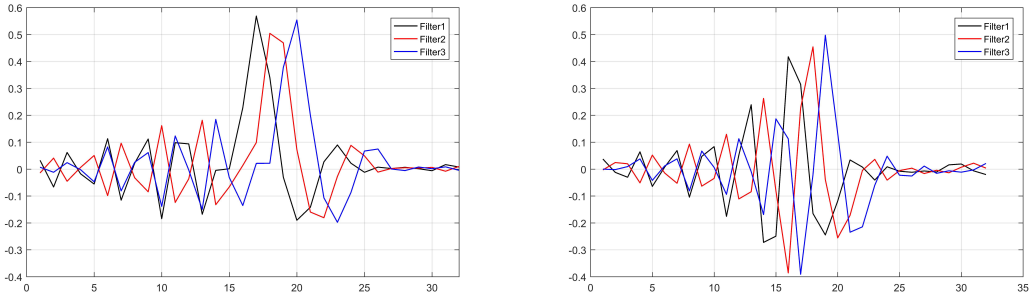


Figure 5.23 : Tx filters without pre-equalization.

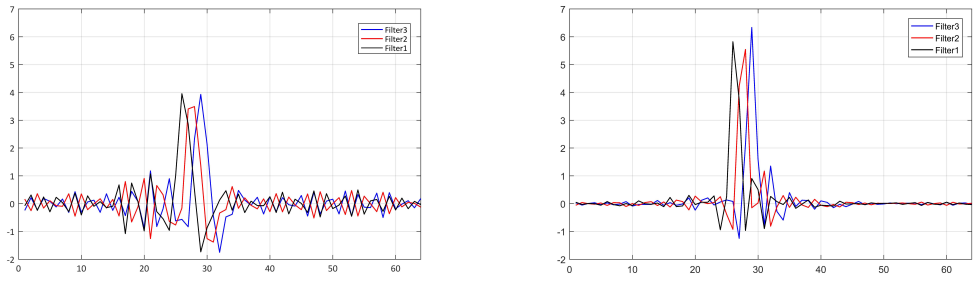


(a) (b)

Figure 5.24 : Tx filters with pre-equalization of (a) real part and (b) imaginary part.

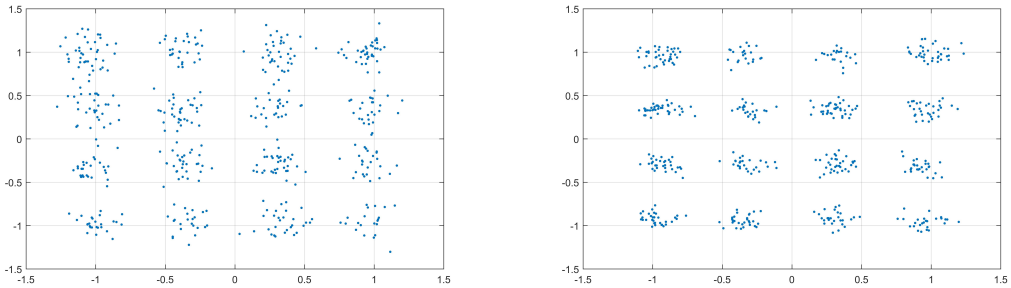
only use the receiver filters with length 54. However, for the filters without pre-equalization, the channel response is very long and hence the 54 length filters can not achieve the required performance. For filters with pre-equalization, we can see that the channel impulse is short and concentrated. Even we use a shorter length filters after pre-equalization, satisfactory performance is still achieved.

Figure 5.26 shows the comparison between the 16-QAM constellations without and with pre-equalization for the selected IF channel. We see that the EVM is significantly improved after pre-equalization. After testing plenty of data, EVMs calculated for the selected channel without pre-equalization and with pre-equalization are 16.3% and 10.3% respectively.



(a) (b)

Figure 5.25 : Real parts of Rx filters (a) without pre-equalization and (b) with pre-equalization.



(a) (b)

Figure 5.26 : Constellations (a) without pre-equalization and (b) with pre-equalization.

From the above results, we see that pre-equalization is an effective way to reduce the influence of the IF module in the wideband system. After adopting the pre-equalization technique and optimized algorithms, the EVM of received signal constellation for the IF module loopback test is 10.3%.

5.9.4 BER Test with Real-Time Ethernet Traffic

In addition to the 20 Gbps data rate, the digital modem should also satisfy the BER requirement which is 10^{-7} at normalised signal-to-noise ratio Eb/N0 = 14

dB. Therefore, there are two important measurements needed to be performed with sufficient accuracy, which are the SNR measurement and BER measurement.

SNR Measurement

The following method is used to measure the SNR:

Step 1. Power on the spectrum analyzer while keeping all the other test equipment off;

Step 2. Measure the spectrum analyzer internal base noise at given center frequency with appropriate bandwidth. For each 2.5 GHz individual channel, the center frequencies are 10.65 GHz, 13.15 GHz, 18.15 GHz and 20.65 GHz respectively with measurement bandwidth 3.75 GHz. For the total four IF channels, the center frequency is 15.65 GHz with measurement bandwidth 15 GHz. The base noise power is denote as P_0 in dB for each center frequency and bandwidth combination;

Step 3. Power on the equipment for noise generation and set the attenuation to 0 dB from the switch driver which is shown in Figure 5.20. Turn on the noise generator by selecting the noise source ON from the spectrum analyzer menu. Measure the noise powers with various center frequencies and bandwidths as above. Denote the noise power as P_n in dB for each center frequency and bandwidth combination;

Step 4. Power on the digital modem (FPGA platforms and IF modules). Load compiled FGPA bit file to each FPGA platform from the Control PC and monitor the modem working status;

Step 5. Set the noise attenuation to the maximum (70 dB) and test the signal powers with various center frequencies and bandwidths as above. Denote

the signal power as P_s in dB for each center frequency and bandwidth combination.

The signal power after removing the spectrum analyzers internal base noise is then calculated as

$$S = 10^{\frac{P_s}{10}} - 10^{\frac{P_0}{10}}, \tag{5.1}$$

and the maximum noise power after removing the spectrum analyzers internal base noise is calculated as

$$N = 10^{\frac{P_n}{10}} - 10^{\frac{P_0}{10}}. \tag{5.2}$$

Since the noise power is measured in a bandwidth which is twice of the signal nominal bandwidth, the minimum SNR (at noise attenuation $Atten = 0$ dB) is thus calculated as

$$\left(\frac{S}{N}\right)_{min} = 2\frac{10^{\frac{P_s}{10}} - 10^{\frac{P_0}{10}}}{10^{\frac{P_n}{10}} - 10^{\frac{P_0}{10}}} = 2\frac{10^{\frac{P_s - P_0}{10}} - 1}{10^{\frac{P_n - P_0}{10}} - 1} = 10log\left(\frac{10^{\frac{P_s - P_0}{10}} - 1}{10^{\frac{P_n - P_0}{10}} - 1}\right) + 3\ dB. \tag{5.3}$$

The SNR at different noise attenuation level is therefore

$$\frac{S}{N} = \left(\frac{S}{N}\right)_{min} + Atten\ (in\ dB). \tag{5.4}$$

Due to the modulation type is 16-QAM, the normalised signal-to-noise ratio Eb/N0 is determined as

$$\frac{E_b}{N_0} = \frac{S}{N} + 10log\left(\frac{1}{4}\right) = \left(\frac{S}{N}\right)_{min} + Atten - 6\ (in\ dB). \tag{5.5}$$

BER Measurement

The Spirent Tester has the capability to perform a variety of different measurement including BER which can be measured as follows:

Step 1. Launch the Spirent TestCenter application from the PC connected to the Spirent Tester chassis;

Step 2. Click Connect to Chassis and Reserve Ports on the user interface to select Ethernet ports;

Step 3. Generate traffic using selected configurations (such as frame length per packet, data rate, data pattern, etc.) and click Apply on the user interface;

Step 4. Start traffic from the Spirent Tester transmitter port and loopback the traffic to the Spirent Tester receiver port. Watch the transmit/receive status from the user interface;

Step 5. From the Traffic Aggregate View on the user interface check the bit error rate and also other measurement results.

Figure 5.27 shows a snapshot of the Spirent TestCenter user interface from which all functionalities can be accessed.

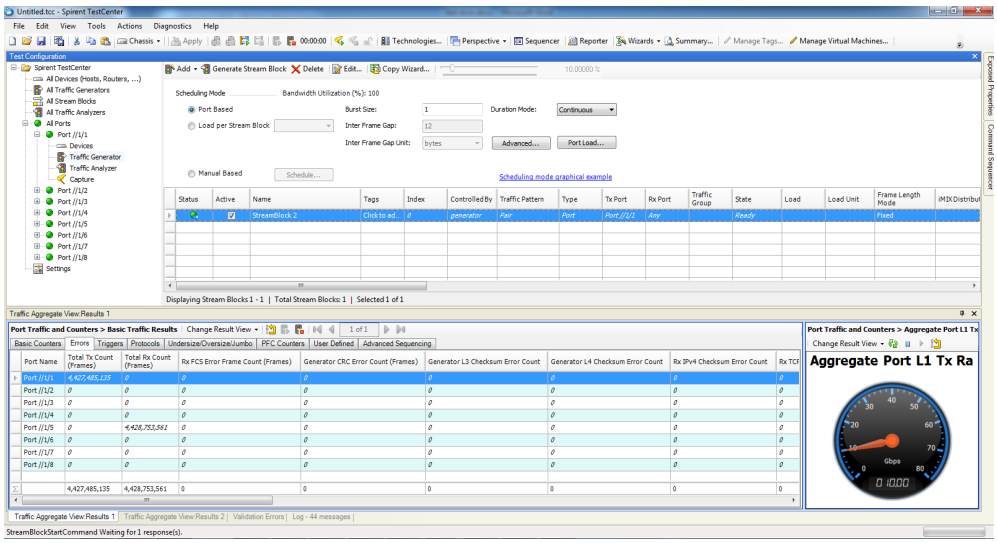


Figure 5.27 : Spirent TestCenter user interface.

BER Results

BER test with real-time Ethernet traffic is finally performed after necessary algorithms update. Firstly, the BER test for each individual channel is conducted. When a channel is under testing, the other channels are tuned off. The data rate for each channel is 5 Gbps with pseudo-random bit sequence and 128 byte packet size. For each channel, we measure the spectrum analyzers internal base noise, the external additive noise under 0 dB attenuation, and the transmitted signal power with 3.75 GHz bandwidth. The SNRs are determined by setting the noise attenuation to a required level according the method described in Section 5.9.4. For each SNR, the BER is read out from the Spirent tester user interface as described in this section.

The measured BERs are shown in Figure 5.28 against Eb/N0. We see that the targeted performance (BER $< 10^{-7}$ at Eb/N0 = 14 dB) is satisfied for all individual channels.

Test conditions: Res BW = 100 kHz, Video BW = 100 kHz, Mech Atten = 0 dB, Integration BW = 7.5 GHz; Ethernet frame size =128, Payload type = PRBS												
Test Parameters	Channels LSB2 and LSB1 (Center frequency = 11.90 GHz)						Channesl USB1 and USB2 (Center frequency = 19.40 GHz)					
SA base noise P0 (dBm)	-51.15						-46.85					
Noise at Atten = 0 dB Pn (dBm)	-20.9						-25.7					
Signal power Ps (dBm)	-22.33			-23.22			-29.87			-33.95		
Noise Atten (dB)	SNR	Eb/N0	BER(LSB2)	SNR	Eb/N0	BER(LSB1)	SNR	Eb/N0	BER(USB1)	SNR	Eb/N0	BER(USB2)
19	20.568	13.2984	3.30E-07	19.677	12.407							
20	21.568	14.2984	9.10E-08	20.677	13.407	1.90E-08	18.7755	11.5055	8.30E-08	14.5548	7.2848	
21	22.568	15.2984	1.70E-08	21.677	14.407	4.10E-09	19.7755	12.5055	6.40E-08	15.5548	8.2848	
22	23.568	16.2984	7.30E-09	22.677	15.407	5.70E-11	20.7755	13.5055	4.70E-08	16.5548	9.2848	
23	24.568	17.2984	5.30E-09	23.677	16.407	4.20E-12	21.7755	14.5055	3.00E-09	17.5548	10.2848	
24	25.568	18.2984	1.60E-08	24.677	17.407		22.7755	15.5055	1.80E-09	18.5548	11.2848	
25	26.568	19.2984	6.60E-09	25.677	18.407		23.7755	16.5055	2.10E-09	19.5548	12.2848	3.50E-08
26	27.568	20.2984	3.60E-09	26.677	19.407		24.7755	17.5055	6.00E-10	20.5548	13.2848	3.20E-08
27	28.568	21.2984	2.00E-09	27.677	20.407		25.7755	18.5055	1.50E-10	21.5548	14.2848	1.40E-08
28	29.568	22.2984	1.50E-09	28.677	21.407		26.7755	19.5055	1.10E-10	22.5548	15.2848	3.30E-09
29	30.568	23.2984		29.677	22.407		27.7755	20.5055		23.5548	16.2848	1.10E-09

Figure 5.28 : BER test results for individual channels with adjacent channel interference.

Finally, all the four channels are combined to transmit 20 Gbps traffic. Each of the 10 Gbps data processing is conducted in separated DSP platforms. The 10 Gbps data traffic is a pseudo-random bit sequence with 128 byte packet size. For each point of Eb/N0, we measure the spectrum analyzers internal base noise, the external additive noise under 0 dB attenuation, and the transmitted signal power with 15 GHz bandwidth. The SNRs are determined by setting the noise attenuation to a required level according the method described in Section 5.9.4. For each SNR, the BER is read out from the Spirent tester user interface as described in Section 5.9.4.

The measured BERs are shown in Figure 5.29 against Eb/N0. We see that the targeted performance (BER $< 10^{-7}$ at Eb/N0 = 14 dB) is satisfied for all four channels for 20 Gbps.

Test conditions: Res BW = 100 kHz, Video BW = 100 kHz, Mech Atten = 0 dB, Integration BW = 15 GHz; Ethernet frame size =128, Payload type = PRBS					
Test Parameters	Channels LSB2, LSB1, USB1, and USB2 (Center frequency = 15.65 GHz)				
SA base noise P0 (dBm)	-45.5				
Noise at Atten = 0 dB Pn (dBm)	-19.55				
Signal power Ps (dBm)	-26.05				
Noise Atten (dB)	SNR	Eb/N0	BER(LSB)	BER(USB)	BER
18	14.46147	7.191487			
19	15.46147	8.191487			
20	16.46147	9.191487			
21	17.46147	10.19149			
22	18.46147	11.19149			
23	19.46147	12.19149			
24	20.46147	13.19149	2.40E-08	9.80E-08	6.10E-08
25	21.46147	14.19149	1.10E-08	2.30E-08	1.70E-08
26	22.46147	15.19149	9.00E-09	1.50E-08	1.20E-08
27	23.46147	16.19149	8.00E-09	2.50E-08	1.65E-08
28	24.46147	17.19149	1.40E-09	2.60E-08	1.37E-08
29	25.46147	18.19149	1.70E-10	8.90E-09	4.54E-09

Figure 5.29 : BER test results for all four channels.

5.10 Integration with RF Frontend

5.10.1 Architectures of THz RF Frontend

The 20 Gbps digital modem is part of the high-speed THz communication system with high temperature superconducting receiver frontend developed at University of Technology Sydney. Figure 5.30 shows the block diagram of a compete THz system. The THz communication system provides point-to-point link at 340 GHz frequency. The digital modem is composed of two baseband digital signal processing platforms, each capable of processing 10 Gbps data rate, an intermediate frequency (IF) transmitter module, and an IF receiver module. A dedicated frequency source is also included. When fully operated, the THz communication system can transmit and receive Ethernet traffic at 20 Gbps data rate.

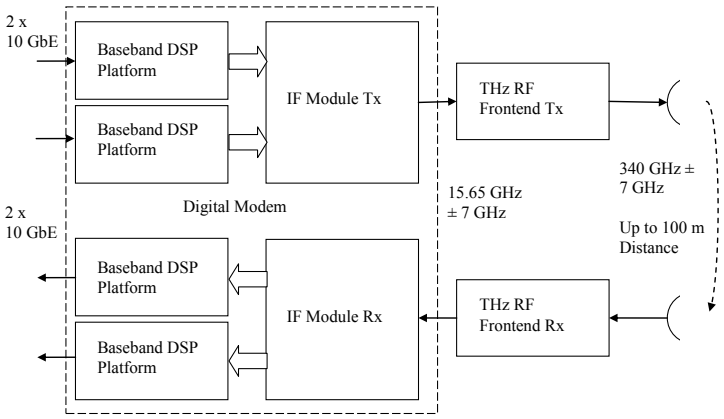


Figure 5.30 : Block diagram of THz communication system.

At the transmitter, the IF module up-converts the I/Q modulated baseband signals generated by the baseband platform to 15.65 GHz IF carrier. There are total 4 channels of baseband signals, each with 2.5 GHz bandwidth. Two of the four bands are first combined to form a 5 GHz bandwidth baseband signal which is further up-converted to the 15.65 GHz IF with only lower sideband. Other two

of the four bands are then combined to form another 5 GHz bandwidth baseband signal which is further up-converted to the 15.65 GHz IF with only upper sideband. The lower sideband and upper sideband are finally combined to form a 12.5 GHz bandwidth IF signal centerd at 15.65 GHz. A 15.65 GHz pilot frequency is also added for carrier frequency tracking at the receiver. The combined IF signal is amplified by a 30 dB amplifier and then up-converted to 325.25 GHz RF signal as shown in Figure 5.31.

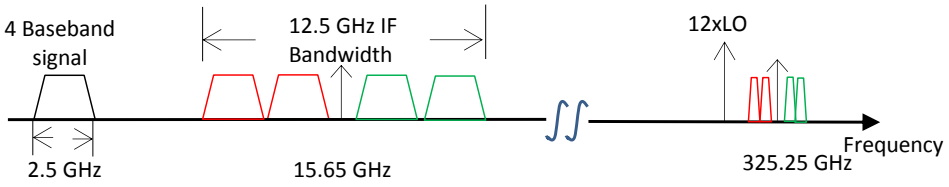


Figure 5.31 : Frequency conversion from baseband to RF.

At the receiver, the RF signal is down-converted to 15.65 GHz IF signal by the 12th harmonics of the LO. Due to the power loss between the transmitter and receiver by the RF frontend, a 30 dB low noise amplifier (LNA) is connected to increase the power of IF signal. The 15.65 GHz IF signal is bandpass filtered to obtain the lower sideband and upper sideband respectively. Each sideband is then down converted to a 5 GHz bandwidth baseband signal, and two channels of the 2.5 GHz bandwidth baseband signals are finally received by the baseband platform. Information data bits are subsequently demodulated by the digital modem.

5.10.2 Test Setup and Experimental Results

The baseband platform is composed of two FPGA devices, each capable of transmitting and receiving two channels of baseband I/Q signals. The IF transmitter and receiver are connected with the baseband platform and RF frontend via coaxial cable. Commercial RF Tx and Rx frontends are connected by the waveguide. A

spectrum analyzer is used to monitor the received signal power. A picture of the THz communication systme testbed is shown in Figure 5.32.

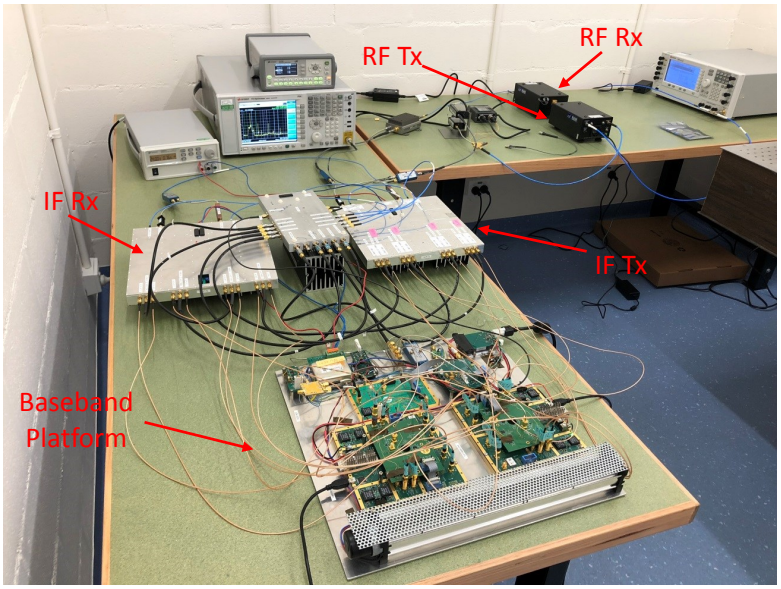
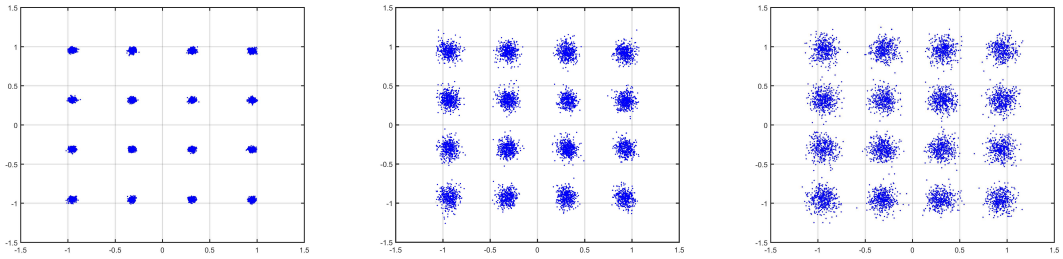


Figure 5.32 : THz system and test setup.

After testing the performance of the IF module, the whole THz system can be connected with RF frontend together. The performance is further deteriorated slightly. The EVM of signal constellation for the whole THz system is 11.6%.

Figure 5.33 shows a comparison of the 16-QAM constellations among the baseband platform loopback via direct D/A and A/D connection, the IF module loopback and the Thz system connection.

Table 5.2 shows a summary of recently published THz communication systems with baseband platforms implemented. The system presented in this thesis can achieve 30 Gbps raw data rate and, more importantly, all the DSP modules are implemented in real-time.



(a) (b) (c)

Figure 5.33 : Measured constellations under various loopback tests: Baseband (a), IF (b) and RF (c).

Table 5.2 : Summary of Recently Published THz Communication Systems

Ref.	[96]	[97]	[98]	This work
Year	2015	2018	2017	2019
EVM	20.4%	12%	–	11.6%
Modulation	8-PSK	16-QAM	16-QAM	16-QAM
Symbol Rate (Gbaud)	21.33	5	1.25	1.875×4
Sample Rate (Gsps)	64	–	5	2.5×4
Raw Date Rate (Gbps)	64	20	5	30
Bandwidth (GHz)	32	18.4	1.8	2.5×4
Efficiency (Bit/s/Hz)	2	1.08	2.78	3
Type	Off-line	Off-line	Real-time	Real-time

5.11 Conclusion

The low-complexity digital modem implementation for high-speed and wideband THz system is presented in this chapter. The requirements, architecture and signal processing of the system are described to show that the system can be implemented

with currently available FPGA technology. Optimized architectures are designed for Ethernet interface, transmitter and receiver filters which can be implemented with low resource usage on the FPGA. Some important strategies in FPGA implementation are described for simultaneously achieving low resource usage and meeting timing constraints at high-speed system clocks. The experimental performance of digital modem and IF modules is verified via the real-time Ethernet traffic. We also show that pre-equalization significantly improves the EVM for the 16-QAM demodulation with the practical wideband IF module. The experimental test results using digital and IF hardware prototype verify the excellent performance of the real-time THz communication system. It is shown that, by adopting the proposed low-complexity design and effective implementation strategies, high-speed wideband wireless communications can be achieved with high performance real-time signal processing.

Chapter 6

Conclusions and Future Work

6.1 Summary of Contributions

This thesis aims to investigate how to improve the synchronization performance in presence of large CFO for an aerial backbone link, how to reduce the digital modem complexity by combining the I/Q imbalance compensation, sample rate conversion, and channel equalization into a single receiver filter, how to adopt the lower sampling-rate conversion devices for achieving higher bandwidth low-complexity wireless communications, and how to implement the digital modem in real-time and demonstrate the performance using FPGA platform. The main contributions are summarized as follows.

1. Low-complexity synchronization with large CFO for high-speed wireless communication

It has been always a big challenge to perform accurate signal synchronization in presence of large CFO in wireless communications. An effective method of synchronization with real-time CFO estimation and compensation is proposed in this thesis, by which CFO can be estimated in conjunction with autocorrelation operation. Meanwhile, the estimated CFO is compensated to improve the accuracy of autocorrelation. Although the estimated CFO is not accurate enough at the beginning, its accuracy is gradually improved as the autocorrelation proceeds. With some shared operations between autocorrelation and CFO estimation, the complexity of this method is quite low and can be implemented with low resource usage. From the overall simulation and experimental results, the peak of autocorrelation can be

captured with large CFO and the resource usage is quite low relative to the whole system.

2. Joint I/Q compensation, channel equalization and SRC for wideband wireless communication

In order to reduce digital signal processing cost and increase the data rate for high-speed wideband wireless communication, a low-complexity and effective method of estimating Rx and Tx I/Q imbalances and compensating for them in serial at the receiver of a communication system is proposed in this thesis. The method comprises of the following steps: (a) transmitting a training sequence periodically at the transmitter with desired frequency domain properties for achieving efficient channel and Tx I/Q imbalance estimation; (b) estimating the Rx I/Q imbalance based on the received signals statistical property in presence of CFO and compensating for the Rx I/Q imbalance with a time domain linear filter; and (c) estimating the channel and Tx I/Q imbalance using the received training sequence after RX I/Q imbalance and CFO compensation and recovering the transmitted data symbols with a time domain linear filter which jointly compensates for the Tx I/Q imbalance and channel as well as performs sample rate conversion. From the simulation and experimental results, the joint algorithm can achieve the desired performance.

3. DPS transmission technique

Considering the limited speed of D/A and A/D converters, a DPS transmission scheme is proposed by which the data symbols to be transmitted are split into two half rate data streams, each passing through a respective pulse shaping filter. This allows for half symbol rate D/A and A/D devices to be used in each band to achieve full rate transmission. A system structure for implementing the DPS scheme is presented and low-complexity equalization method tailored to DPS is proposed.

From the simulation result, the DPS scheme provides a practical and cost-effective solution for high-speed communications when very high sampling-rate conversion devices are unattainable or too costly.

4. Real-time implementation of a high-speed digital modem

Based on the proposed algorithms as mentioned above, a 20 Gbps digital modem is implemented in real-time FPGA. The architectures of the system are designed according to the performance requirements. Signal processing modules are designed and implemented with the low-complexity algorithms, and some key strategies are proposed for implementing the algorithms in FPGA. The optical interface is implemented for connecting the real-time Ethernet traffic. Focusing on the baseband platform, some effective strategies which can reduce the resource usage and improve the timing performance are developed. Adopting these strategies, the implementation of a wideband wireless communication system dealing with some hundreds of Gbps raw data without guarding interval to/from D/As and A/Ds becomes possible. After algorithm optimization, the resource usage is low in FPGA and the timing constraints with high speed system clock can be met. The performance of baseband platform, IF module and RF frontend is evaluated and real-time experimental test results are successfully achieved.

6.2 Future Work

With the rapid development of communication technologies, the following research directions may be the focus for the future work.

6.2.1 Dealing with Nonlinear Channels

Due to the use of high power amplifier, the nonlinearity is unavoidable in the wireless communication systems. Although the digital per-distortion technique can deal with the nonlinear distortion at the transmitter side, it is of significant im-

portance to study the detection algorithm for a nonlinear high spectral efficiency system. In addition to the practical channel impairments, such as the I/Q imbalance and channel frequency response distortion, the nonlinear channel will further increase the complexity and difficulties for the high-speed wireless communication. Existing nonlinear channel model focuses on Volterra model [106] [107]. However, Volterra model has multiple orders and the implementation complexity is quiet high. Therefore, it is necessary to design high-efficiency algorithms to deal with channel non-linearity for the high-speed wideband wireless communications.

6.2.2 Achieving Higher-Speed Wireless Communication Systems

In Chapter 5, a 20 Gbps digital modem for wireless communication system is described. The modulation type is 16-QAM and the bandwidth is 2.5 GHz for each channel. Wider bandwidth and higher modulation level are two significant factors for achieving higher-speed wireless communication systems. Considering the sufficient bandwidth in D band or THz band, a wireless communication system with 50 to 100 Gbps data rate are being developed at University of Technology Sydney. The modulation level will increase to be 64-QAM or more. However, the low-complexity algorithms for wide bandwidth with higher order modulation are very difficult to develop. Future work related higher-speed wireless communication system will be focused on developing digital signal processing algorithms suitable for implementation on the digital hardware.

6.2.3 Reducing System Complexity

In Chapter 5, the 20 Gbps digital modem is implemented in two FPGA devices. For future higher-speed wireless communication systems, higher sampling rate converters will be adopted to support signal processing at digital baseband. Considering the sampling rate at more than 5 Gsps for each band and/or multiple simultaneously occupied bands, huge number of data should be dealt with in real-

time. Low-complexity algorithms and system structure are needed for reducing the power assumption and hardware volume, especially for the ISTN system. How to reduce the resource usage for implementation and simplify the system structure still requires significant efforts for future higher-speed wireless communications.

Bibliography

[1] A. Varghese and D. Tandur, "Wireless requirements and challenges in industry 4.0," in *2014 International Conference on Contemporary Computing and Informatics (IC3I)*, Nov 2014, pp. 634–638.

[2] M. A. M. Albreem, "5G wireless communication systems: Vision and challenges," in *2015 International Conference on Computer, Communications, and Control Technology (I4CT)*, April 2015, pp. 493–497.

[3] J. Thompson, X. Ge, H. Wu, R. Irmer, H. Jiang, G. Fettweis, and S. Alamouti, "5G wireless communication systems: prospects and challenges [guest editorial]," *IEEE Communications Magazine*, vol. 52, no. 2, pp. 62–64, February 2014.

[4] B. Kalra and D. Chauhan, "A comparative study of mobile wireless communication network: 1G to 5G," *International Journal of Computer Science and Information Technology Research*, vol. 2, pp. 430–433, 09 2014.

[5] P. Hajipour, A. Shahzadi, and S. Ghazi-Maghrebi, "Improved performance for a heterogeneous satellite-cooperative network with best relay node selection," *China Communications*, vol. 16, no. 5, pp. 93–105, May 2019.

[6] S. Xu, X. Wang, and M. Huang, "Software-defined next-generation satellite networks: Architecture, challenges, and solutions," *IEEE Access*, vol. 6, pp. 4027–4041, 2018.

[7] X. Chen, G. Dai, G. Reinelt, and M. Wang, "A semi-analytical method for pe-

riodic earth coverage satellites optimization," *IEEE Communications Letters*, vol. 22, no. 3, pp. 534–537, March 2018.

[8] Y. Abe, H. Tsuji, A. Miura, and S. Adachi, "Frequency resource allocation for satellite communications system based on model predictive control and its application to frequency bandwidth allocation for aircraft," in *2018 IEEE Conference on Control Technology and Applications (CCTA)*, Aug 2018, pp. 165–170.

[9] J. Liu, Y. Shi, Z. M. Fadlullah, and N. Kato, "Space-air-ground integrated network: A survey," *IEEE Communications Surveys Tutorials*, vol. 20, no. 4, pp. 2714–2741, Fourthquarter 2018.

[10] L. Wang, C. Jiang, L. Kuang, S. Wu, H. Huang, and Y. Qian, "High-efficient resource allocation in data relay satellite systems with users behavior coordination," *IEEE Transactions on Vehicular Technology*, vol. 67, no. 12, pp. 12 072–12 085, Dec 2018.

[11] J. M. Martnez-Heredia, Z. Garca, J. L. Mora-Jimnez, S. Esteban, and F. Gaviln, "Development of an emergency radio beacon for small unmanned aerial vehicles," *IEEE Access*, vol. 6, pp. 21 570–21 581, 2018.

[12] H. Yao, L. Wang, X. Wang, Z. Lu, and Y. Liu, "The space-terrestrial integrated network: An overview," *IEEE Communications Magazine*, vol. 56, no. 9, pp. 178–185, Sep. 2018.

[13] N. Zhang, S. Zhang, P. Yang, O. Alhussein, W. Zhuang, and X. S. Shen, "Software defined space-air-ground integrated vehicular networks: Challenges and solutions," *IEEE Communications Magazine*, vol. 55, no. 7, pp. 101–109, July 2017.

[14] H. Fenech, S. Amos, A. Tomatis, and V. Soumpholphakdy, "High throughput satellite systems: An analytical approach," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 51, no. 1, pp. 192–202, January 2015.

[15] L. Del Consuelo Hernandez Ruiz Gaytan, Z. Pan, J. Liu, and S. Shimamoto, "Dynamic scheduling for high throughput satellites employing priority code scheme," *IEEE Access*, vol. 3, pp. 2044–2054, 2015.

[16] A. Botta and A. Pescape, "On the performance of new generation satellite broadband internet services," *IEEE Communications Magazine*, vol. 52, no. 6, pp. 202–209, June 2014.

[17] M. Chernyshev, Z. Baig, O. Bello, and S. Zeadally, "Internet of things (iot): Research, simulators, and testbeds," *IEEE Internet of Things Journal*, vol. 5, no. 3, pp. 1637–1647, June 2018.

[18] Y. Wang, Q. Li, J. Jiao, S. Wu, and Q. Zhang, "ARM: Adaptive random-selected multi-beamforming estimation scheme for satellite-based internet of things," *IEEE Access*, vol. 7, pp. 63 264–63 276, 2019.

[19] X. Zhu, C. Jiang, L. Kuang, N. Ge, and J. Lu, "Non-orthogonal multiple access based integrated terrestrial-satellite networks," *IEEE Journal on Selected Areas in Communications*, vol. 35, no. 10, pp. 2253–2267, Oct 2017.

[20] C. Qiu, H. Yao, F. R. Yu, F. Xu, and C. Zhao, "Deep Q-learning aided networking, caching, and computing resources allocation in software-defined satellite-terrestrial networks," *IEEE Transactions on Vehicular Technology*, vol. 68, no. 6, pp. 5871–5883, June 2019.

[21] K. Kaneko, H. Nishiyama, N. Kato, A. Miura, and M. Toyoshima, "Construction of a flexibility analysis model for flexible high-throughput satellite

communication systems with a digital channelizer," *IEEE Transactions on Vehicular Technology*, vol. 67, no. 3, pp. 2097–2107, March 2018.

[22] H. Fenech, S. Amos, A. Tomatis, and V. Soumpholphakdy, "High throughput satellite systems: An analytical approach," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 51, no. 1, pp. 192–202, January 2015.

[23] X. Huang, J. A. Zhang, R. P. Liu, Y. J. Guo, and L. Hanzo, "Airplane-aided integrated networking for 6G wireless: Will it work?" *IEEE Vehicular Technology Magazine*, vol. 14, no. 3, pp. 84–91, Sep. 2019.

[24] H. Yao, L. Wang, X. Wang, Z. Lu, and Y. Liu, "The space-terrestrial integrated network: An overview," *IEEE Communications Magazine*, vol. 56, no. 9, pp. 178–185, Sep. 2018.

[25] T. Huang, W. Yang, J. Wu, J. Ma, X. Zhang, and D. Zhang, "A survey on green 6G network: Architecture and technologies," *IEEE Access*, vol. 7, pp. 175 758–175 768, 2019.

[26] M. Jaber, M. A. Imran, R. Tafazolli, and A. Tukmanov, "5G backhaul challenges and emerging research directions: A survey," *IEEE Access*, vol. 4, pp. 1743–1766, 2016.

[27] D. Falconer, S. L. Ariyavisitakul, A. Benyamin-Seeyar, and B. Eidson, "Frequency domain equalization for single-carrier broadband wireless systems," *IEEE Communications Magazine*, vol. 40, no. 4, pp. 58–66, Apr 2002.

[28] X. Zhang, E. Chen, and X. Mu, "Single-carrier frequency-domain equalization based on frequency-domain oversampling," *IEEE Communications Letters*, vol. 16, no. 1, pp. 24–26, January 2012.

[29] Y. R. Zheng and C. Xiao, "Channel estimation for frequency-domain equalization of single-carrier broadband wireless communications," *IEEE Transactions on Vehicular Technology*, vol. 58, no. 2, pp. 815–823, Feb 2009.

[30] A. H. Mehana and A. Nosratinia, "Single-carrier frequency-domain equalizer with multi-antenna transmit diversity," *IEEE Transactions on Wireless Communications*, vol. 12, no. 1, pp. 388–397, January 2013.

[31] X. Li, Y. Xu, J. Xiao, K. Wang, and J. Yu, "Modulation optimization for D-band wireless transmission link," in *2017 Optical Fiber Communications Conference and Exhibition (OFC)*, March 2017, pp. 1–3.

[32] W. T. Khan, A. C. Ulusoy, G. Dufour, M. Kaynak, B. Tillack, J. D. Cressler, and J. Papapolymerou, "A D-Band micromachined end-fire antenna in 130-nm SiGe BiCMOS technology," *IEEE Transactions on Antennas and Propagation*, vol. 63, no. 6, pp. 2449–2459, June 2015.

[33] Analog Device Inc., "High Speed ADC," March 2019, https://www.analog.com/en/parametricsearch/10826.

[34] Texas Instruments Inc., "Analog-to-digital converters," March 2019, http://www.ti.com/data-converters/adc-circuit/products.html.

[35] Teledyne e2v, "Analog-to-digital Converters," March 2019, https://www.teledyne-e2v.com/products/semiconductors/adc/.

[36] G. Cui, C. Wang, W. Wang, and Y. Zhang, "Frequency offset compensation for satellite communication system with CE-OFDM," *China Communications*, vol. 14, no. 8, pp. 93–104, Aug 2017.

[37] A. J. Coulson, "Maximum likelihood synchronization for OFDM using a pilot symbol: algorithms," *IEEE Journal on Selected Areas in Communications*, vol. 19, no. 12, pp. 2486–2494, Dec 2001.

[38] B. Park, H. Cheon, C. Kang, and D. Hong, "A novel timing estimation method for OFDM systems," *IEEE Communications Letters*, vol. 7, no. 5, pp. 239–241, May 2003.

[39] H. Minn, V. K. Bhargava, and K. B. Letaief, "A robust timing and frequency synchronization for OFDM systems," *IEEE Transactions on Wireless Communications*, vol. 2, no. 4, pp. 822–839, July 2003.

[40] K. Shi and E. Serpedin, "Coarse frame and carrier synchronization of OFDM systems: a new metric and comparison," *IEEE Transactions on Wireless Communications*, vol. 3, no. 4, pp. 1271–1284, July 2004.

[41] M. Ruan, M. C. Reed, and Z. Shi, "Training symbol based coarse timing synchronization in OFDM systems," *IEEE Transactions on Wireless Communications*, vol. 8, no. 5, pp. 2558–2569, May 2009.

[42] J. A. Zhang and X. Huang, "Autocorrelation based coarse timing with differential normalization," *IEEE Transactions on Wireless Communications*, vol. 11, no. 2, pp. 526–530, February 2012.

[43] H. Abdzadeh-Ziabari and M. G. Shayesteh, "Sufficient statistics, classification, and a novel approach for frame detection in OFDM systems," *IEEE Transactions on Vehicular Technology*, vol. 62, no. 6, pp. 2481–2495, July 2013.

[44] A. Mohebbi, H. Abdzadeh-Ziabari, and M. G. Shayesteh, "Novel coarse timing synchronization methods in OFDM systems using fourth-order statistics," *IEEE Transactions on Vehicular Technology*, vol. 64, no. 5, pp. 1904–1917, May 2015.

[45] G. Ren, Y. Chang, H. Zhang, and H. Zhang, "Synchronization method based on a new constant envelop preamble for OFDM systems," *IEEE Transactions on Broadcasting*, vol. 51, no. 1, pp. 139–143, March 2005.

[46] H. Abdzadeh-Ziabari and M. G. Shayesteh, "Robust timing and frequency synchronization for OFDM systems," *IEEE Transactions on Vehicular Technology*, vol. 60, no. 8, pp. 3646–3656, Oct 2011.

[47] Xilinx, "CORDIC," 2019. [Online]. Available: https://www.xilinx.com/products/intellectual-property/cordic.html

[48] X. Virtex7, "7 Series FPGAs Configurable Logic Block," 2016. [Online]. Available: https://www.xilinx.com/support/documentation/data_sheets/ds180_7Series_Overview.pdf

[49] V. Rampa, "I/Q compensation of broadband direct-conversion transmitters," *IEEE Transactions on Wireless Communications*, vol. 13, no. 6, pp. 3329–3342, June 2014.

[50] B. Narasimhan, D. Wang, S. Narayanan, H. Minn, and N. Al-Dhahir, "Digital compensation of frequency-dependent joint Tx/Rx I/Q imbalance in OFDM systems under high mobility," *IEEE Journal of Selected Topics in Signal Processing*, vol. 3, no. 3, pp. 405–417, June 2009.

[51] X. Zhang, H. Li, W. Liu, and J. Qiao, "Iterative iq imbalance compensation receiver for single carrier transmission," *IEEE Transactions on Vehicular Technology*, vol. 66, no. 9, pp. 8238–8248, Sep. 2017.

[52] C.-L. Liu, "Impacts of I/Q imbalance on QPSK-OFDM -QAM detection," *IEEE Transactions on Consumer Electronics*, vol. 44, no. 3, pp. 984–989, Aug 1998.

[53] F. J. Lopez-Martinez, E. Martos-Naya, J. F. Paris, and J. T. Entrambasaguas, "Exact closed-form ber analysis of OFDM systems in the presence of IQ imbalances and ICSI," *IEEE Transactions on Wireless Communications*, vol. 10, no. 6, pp. 1914–1922, June 2011.

[54] M. Valkama, M. Renfors, and V. Koivunen, "Advanced methods for I/Q imbalance compensation in communication receivers," *IEEE Transactions on Signal Processing*, vol. 49, no. 10, pp. 2335–2344, Oct 2001.

[55] A. Tarighat, R. Bagheri, and A. H. Sayed, "Compensation schemes and performance analysis of IQ imbalances in OFDM receivers," *IEEE Transactions on Signal Processing*, vol. 53, no. 8, pp. 3257–3268, Aug 2005.

[56] D. Mattera, L. Paura, and F. Sterle, "Mmse WL equalizer in presence of receiver IQ imbalance," *IEEE Transactions on Signal Processing*, vol. 56, no. 4, pp. 1735–1740, April 2008.

[57] S. Traverso, M. Ariaudo, I. Fijalkow, J. l. Gautier, and C. Lereau, "Decision-directed channel estimation and high I/Q imbalance compensation in OFDM receivers," *IEEE Transactions on Communications*, vol. 57, no. 5, pp. 1246–1249, May 2009.

[58] M. Marey, M. Samir, and O. A. Dobre, "EM-based joint channel estimation and I/Q imbalances for OFDM systems," *IEEE Transactions on Broadcasting*, vol. 58, no. 1, pp. 106–113, March 2012.

[59] M. Marey, M. Samir, and M. H. Ahmed, "Joint estimation of transmitter and receiver IQ imbalance with ml detection for alamouti OFDM systems," *IEEE Transactions on Vehicular Technology*, vol. 62, no. 6, pp. 2847–2853, July 2013.

[60] S. Narayanan, B. Narasimhan, and N. Al-Dhahir, "Training sequence design for joint channel and I/Q imbalance parameter estimation in mobile SC-FDE transceivers," in *2010 IEEE International Conference on Acoustics, Speech and Signal Processing*, March 2010, pp. 3186–3189.

[61] W. Hou and M. Jiang, "Enhanced joint channel and IQ imbalance parameter estimation for mobile communications," *IEEE Communications Letters*, vol. 17, no. 7, pp. 1392–1395, July 2013.

[62] S. Narayanan, B. Narasimhan, and N. Al-Dhahir, "Baseband estimation and compensation of joint TX/RX I/Q imbalance in SC-FDE transceivers," in *2009 43rd Annual Conference on Information Sciences and Systems*, March 2009, pp. 551–556.

[63] C. Zhang, Z. Xiao, B. Gao, L. Su, and D. Jin, "Three-stage treatment of TX/RX IQ imbalance and channel with CFO for SC-FDE systems," *IEEE Communications Letters*, vol. 18, no. 2, pp. 297–300, February 2014.

[64] X. Cheng, Z. Luo, and S. Li, "Joint estimation for I/Q imbalance and multipath channel in millimeter-wave SC-FDE systems," *IEEE Transactions on Vehicular Technology*, vol. 65, no. 9, pp. 6901–6912, Sept 2016.

[65] N. Souto, R. Dinis, A. Correia, and C. Reis, "Interference-aware iterative block decision feedback equalizer for single-carrier transmission," *IEEE Transactions on Vehicular Technology*, vol. 64, no. 7, pp. 3316–3321, July 2015.

[66] N. Benvenuto and S. Tomasin, "Iterative design and detection of a DFE in the frequency domain," *IEEE Transactions on Communications*, vol. 53, no. 11, pp. 1867–1875, Nov 2005.

[67] N. Souto, R. Dinis, and J. C. Silva, "Impact of channel estimation errors on SC-FDE systems," *IEEE Transactions on Communications*, vol. 62, no. 5, pp. 1530–1540, May 2014.

[68] L. Anttila, M. Valkama, and M. Renfors, "Circularity-based I/Q imbalance compensation in wideband direct-conversion receivers," *IEEE Transactions on Vehicular Technology*, vol. 57, no. 4, pp. 2099–2113, July 2008.

[69] B. Narasmihan, C. Chien, Sheng-Hong Yan, P. Liang, and H. Hwang, "Robust low-complexity blind frequency-dependent I/Q estimation and compensation," in *2013 IEEE Global Communications Conference (GLOBECOM)*, Dec 2013, pp. 4331–4336.

[70] X. Cai, Y. Wu, H. Lin, and K. Yamashita, "Estimation and compensation of CFO and I/Q imbalance in OFDM systems under timing ambiguity," *IEEE Transactions on Vehicular Technology*, vol. 60, no. 3, pp. 1200–1205, March 2011.

[71] Y. Pan and S. Phoong, "A time-domain joint estimation algorithm for CFO and I/Q imbalance in wideband direct-conversion receivers," *IEEE Transactions on Wireless Communications*, vol. 11, no. 7, pp. 2353–2361, July 2012.

[72] Y. Li, L. Fan, H. Lin, and M. Zhao, "A new method to simultaneously estimate TX/RX IQ imbalance and channel for OFDM systems," in *2013 IEEE International Conference on Communications (ICC)*, June 2013, pp. 4551–4555.

[73] S. Chen, A. Al Amin, and W. Shieh, "Real-time IQ imbalance compensation for coherent optical OFDM transmission," in *2011 Optical Fiber Communication Conference and Exposition and the National Fiber Optic Engineers Conference*, March 2011, pp. 1–3.

[74] X. Huang, Y. J. Guo, and J. A. Zhang, "Transceiver I/Q imbalance self-calibration with phase-shifted local loopback for multichannel microwave backhaul," *IEEE Transactions on Wireless Communications*, vol. 15, no. 11, pp. 7657–7669, Nov 2016.

[75] J. G. Proakis, *Digital Communications*. McGraw-Hill, third edition, 1995.

[76] J. G. Andrews, S. Buzzi, W. Choi, S. V. Hanly, A. Lozano, A. C. K. Soong, and J. C. Zhang, "What will 5G be?" *IEEE Journal on Selected Areas in*

Communications, vol. 32, no. 6, pp. 1065–1082, June 2014.

[77] A. Buchwald, "High-speed time interleaved ADCs," *IEEE Communications Magazine*, vol. 54, no. 4, pp. 71–77, April 2016.

[78] W. Namgoong, "A channelized digital ultrawideband receiver," *IEEE Transactions on Wireless Communications*, vol. 2, no. 3, pp. 502–510, May 2003.

[79] T. Yu, M. Zhao, J. Zhong, J. Zhang, and P. Xiao, "Low-complexity graph-based turbo equalisation for single-carrier and multi-carrier FTN signalling," *IET Signal Processing*, vol. 11, no. 7, pp. 838–845, 2017.

[80] K. Wang, A. Liu, X. Liang, S. Peng, and Q. Zhang, "A faster-than-nyquist (FTN)-based multicarrier system," *IEEE Transactions on Vehicular Technology*, vol. 68, no. 1, pp. 947–951, Jan 2019.

[81] B. Baeuerle, A. Josten, M. Eppenberger, D. Hillerkuss, and J. Leuthold, "Low-complexity real-time receiver for coherent Nyquist-FDM signals," *Journal of Lightwave Technology*, vol. 36, no. 24, pp. 5728–5737, Dec 2018.

[82] W. Liu, D. Chen, K. Luo, T. Jiang, and D. Qu, "FDM-structured preamble optimization for channel estimation in MIMO-OQAM/FBMC systems," *IEEE Transactions on Wireless Communications*, vol. 17, no. 12, pp. 8433–8443, Dec 2018.

[83] A. Prlja and J. B. Anderson, "Reduced-complexity receivers for strongly narrowband intersymbol interference introduced by faster-than-nyquist signaling," *IEEE Transactions on Communications*, vol. 60, no. 9, pp. 2591–2601, Sep. 2012.

[84] T. Ishihara and S. Sugiura, "Iterative frequency-domain joint channel estimation and data detection of faster-than-nyquist signaling," *IEEE Transactions on Wireless Communications*, vol. 16, no. 9, pp. 6221–6231, Sep. 2017.

[85] H. B. Almelah and K. A. Hamdi, "Spectral efficiency of distributed large-scale MIMO systems with ZF receivers," *IEEE Transactions on Vehicular Technology*, vol. 66, no. 6, pp. 4834–4844, June 2017.

[86] D. Darsena, G. Gelli, F. Melito, and F. Verde, "Performance analysis of amplify-and-forward MIMO-OFDM links with linear ZF equalization," in *2013 IEEE International Conference on Communications Workshops (ICC)*, June 2013, pp. 296–300.

[87] H. Gazzah, "A note on optimum MMSE/ZF multichannel equalization delay," in *2010 17th International Conference on Telecommunications*, April 2010, pp. 919–922.

[88] K. Kuchi, "Limiting behavior of ZF/MMSE linear equalizers in wideband channels with frequency selective fading," *IEEE Communications Letters*, vol. 16, no. 6, pp. 929–932, June 2012.

[89] N. Benvenuto, S. Ciccotosto, and S. Tomasin, "Iterative block fractionally spaced nonlinear equalization for wideband channels," *IEEE Wireless Communications Letters*, vol. 4, no. 5, pp. 489–492, Oct 2015.

[90] G. Kutz, N. Zach, and W. Chen, "Low complexity frequency domain LMMSE equalization for single carrier systems," *IEEE Communications Letters*, vol. 17, no. 12, pp. 2268–2271, December 2013.

[91] Analog Device Inc, "AD9739 (Rev. E)," 2018. [Online]. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/ad9739.pdf

[92] C. Lin, B. Lu, C. Wang, and Q. Wu, "A 240 Gbps wireless communication system using 0.14 THz band oritho-mode transducer," in *2015 40th Inter-*

national Conference on Infrared, Millimeter, and Terahertz waves (IRMMW-THz), Aug 2015, pp. 1–2.

[93] P. Rodrguez-Vzquez, J. Grzyb, N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "Towards 100 Gbps: A fully electronic 90 Gbps one meter wireless link at 230 GHz," in *2018 15th European Radar Conference (EuRAD)*, Sep. 2018, pp. 369–372.

[94] K. KrishneGowda, P. Rodrguez-Vzquez, A. C. Wolf, J. Grzyb, U. R. Pfeiffer, and R. Kraemer, "100 Gbps and beyond: Hardware in the loop experiments with PSSS modulation using 230 GHz RF frontend," in *2018 15th Workshop on Positioning, Navigation and Communications (WPNC)*, Oct 2018, pp. 1–5.

[95] K. Takano, K. Katayama, S. Amakawa, T. Yoshida, and M. Fujishima, "56-Gbit/s 16-QAM wireless link with 300-GHz-band CMOS transmitter," in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, June 2017, pp. 793–796.

[96] I. Kallfass, F. Boes, T. Messinger, J. Antes, A. Inam, U. Lewark, A. Tessmann, and R. Henneberger, "64 Gbit/s transmission over 850 m fixed wireless link at 240 GHz carrier frequency," *Journal of Infrared, Millimeter, and Terahertz Waves*, vol. 36, no. 2, pp. 221–233, Feb 2015. [Online]. Available: https://doi.org/10.1007/s10762-014-0140-6

[97] S. Hara, K. Takano, K. Katayama, R. Dong, S. Lee, I. Watanabe, N. Sekine, A. Kasamatsu, T. Yoshida, S. Amakawa, and M. Fujishima, "300-GHz CMOS transceiver for terahertz wireless communication," in *2018 Asia-Pacific Microwave Conference (APMC)*, Nov 2018, pp. 429–431.

[98] Q. Wu, C. Lin, B. Lu, L. Miao, X. Hao, Z. Wang, Y. Jiang, W. Lei, X. Den, H. Chen, J. Yao, and J. Zhang, "A 21 km 5 Gbps real time wireless com-

munication system at 0.14 THz," in *2017 42nd International Conference on Infrared, Millimeter, and Terahertz Waves (IRMMW-THz)*, Aug 2017, pp. 1–2.

[99] J. Lei, Y. Li, D. Zhao, J. Xie, C.-I. Chang, L. Wu, X. Li, J. Zhang, and W. Li, "A deep pipelined implementation of Hyperspectral target detection algorithm on FPGA using HLS," *Remote Sensing*, vol. 10, no. 4, 2018. [Online]. Available: http://www.mdpi.com/2072-4292/10/4/516

[100] J. Lei, L. Wu, Y. Li, W. Xie, C.-I. Chang, J. Zhang, and B. Huang, "A novel FPGA-based architecture for fast automatic target detection in Hyperspectral images," *Remote Sensing*, vol. 11, no. 2, 2019. [Online]. Available: http://www.mdpi.com/2072-4292/11/2/146

[101] D. J. C. MacKay and R. M. Neal, "Near shannon limit performance of low density parity check codes," *Electronics Letters*, vol. 32, no. 18, pp. 1645–, Aug 1996.

[102] K. Gunnam, G. Choi, W. Wang, and M. Yeary, "Multi-rate layered decoder architecture for block LDPC codes of the IEEE 802.11n wireless standard," in *2007 IEEE International Symposium on Circuits and Systems*. IEEE, 2007, pp. 1645–1648.

[103] IEEE Computer Society LAN/MAN Standards Committee and others, "Wireless LAN medium access control (MAC) and physical layer (PHY) specifications," 1997.

[104] P. A. Bottorff, N. R. Figueira, D. W. Martin, T. J. Armstrong, and B. Raahemi, "10 Gigabit ethernet mappings for a common LAN/WAN PMD interface with a simple universal physical medium dependent interface," Sep. 13 2005, US Patent 6,944,163.

[105] Xilinx, "FPGA Family," 2010. [Online]. Available: https://www.xilinx.com/data

[106] Y. Hu, J. J. Obregon, and J. . Mollier, "Nonlinear analysis of microwave FET oscillators using volterra series," *IEEE Transactions on Microwave Theory and Techniques*, vol. 37, no. 11, pp. 1689–1693, Nov 1989.

[107] G. D. Mitsis, M. G. Markakis, and V. Z. Marmarelis, "Nonlinear modeling of the dynamic effects of infused insulin on glucose: Comparison of compartmental with volterra models," *IEEE Transactions on Biomedical Engineering*, vol. 56, no. 10, pp. 2347–2358, Oct 2009.