University of Technology Sydney

Faculty of Engineering and Information Technology

Advanced Control Strategies for Multilevel Power Converters in Hybrid Microgrid Applications

A thesis submitted for the degree of
Doctor of Philosophy

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(2019)

Title of the thesis:

Advanced Control Strategies for Multilevel Power Converters in Hybrid Microgrid Applications

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I, Shakil Ahamed Khan declare that this thesis, is submitted in fulfilment of the requirements for the award of Doctor of Philosophy, in the School of Electrical and Data Engineering at the University of Technology Sydney.

This thesis is wholly my own work unless otherwise reference or acknowledged. In addition, I certify that all information sources and literature used are indicated in the thesis.

This document has not been submitted for qualifications at any other academic institution.

This research is supported by the Australian Government Research Training Program.

Production Note:
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Date: 11 February 2020

Acknowledgments

I would like to express my sincere gratitude to my principal supervisor Professor Youguang Guo, for his guidance and sincere encouragement throughout my graduate studies. I am also grateful to Professor Jianguo Zhu, my co-supervisor, for his mentorship and support in my research. Their opinions and advice have provided me with great assistance in completing my Ph.D. research work.

I would also like to express thanks to my research group mates, in particular Dr. Yam Siwakoti of the Centre for Electrical Machines and Power Electronics, University of Technology Sydney (UTS), for their precious time, mentorship, sharing of knowledge and technical support.

I would also like to express my gratitude to all my friends for their encouragement. I especially would like to thank Mahmudul Hasan Sohag and Sabbir Ahamed Khan for their constant support and encouragement.

My deepest and most gratitude goes to my family members, my father Md Ismail Khan, my mother Mst Shefali Akther. Finally, I would like to thank my loving Sanzida Tafseer Nishat for her endless love, support and continued patience.

Publications and Conference Contributions

The following publications are part of the thesis.

Peer reviewed international journal publications

[1] **S. A. Khan**, Y. Guo, Y. P. Siwakoti, D. D. Lu and J. Zhu, "A Disturbance Rejection Based Control Strategy for Five-Level T-Type Hybrid Power Converters with Ripple Voltage Estimation Capability," *IEEE Transactions on Industrial Electronics*. doi: 10.1109/TIE.2019.2942550 (Early access version is available in online: https://ieeexplore.ieee.org/document/8848848)

[2] **S.A. Khan**, Y. Guo and J. Zhu, "Model Predictive Observer Based Control for Single-Phase Asymmetrical T-type AC/DC Power Converter," *IEEE Transactions on Industry Applications*, vol. 55, no. 2, pp. 2033-2044, March 2019, Doi: 10.1109/TIA.2018.2877397 (Published)

[3] **S. A. Khan**, M. R. Islam, Y. Guo and J. Zhu, "An Amorphous Alloy Magnetic-Bus-Based SiC NPC Converter With Inherent Voltage Balancing for Grid-Connected Renewable Energy Systems," *IEEE Transactions on Applied Superconductivity*, vol. 29, no. 2, pp. 1-8, March 2019, doi: 10.1109/TASC.2018.2882448 (Published)

[4] **S. A. Khan**, M. R. Islam, Y. Guo and J. Zhu, "A New Isolated Multi-Port Converter With Multi-Directional Power Flow Capabilities for Smart Electric Vehicle Charging Stations," *IEEE Transactions on Applied Superconductivity*, vol. 29, no. 2, pp. 1-4, March 2019, Doi: 10.1109/TASC.2019.2895526 (Published)

[5] **S. A. Khan**, Y. Guo, Yam. S, M. N. Habib Khan and J. Zhu, "Topology, Modeling and Control Scheme for a New 7-Level Inverter with Reduced DC-Link Voltage," *IEEE Transactions on Industrial Electronics*. (Under review)

[6] **S. A. Khan**, Y. Guo, and J. Zhu, "A Robust Method for Fast Estimation of Grid Voltage Parameters under Distorted Grid," *IEEE Transactions on Power Electronics*. (Preparing)

Peer reviewed international scientific conference publications

[7] **S. A. Khan**, Y. Guo, M. N. Habib Khan, Y. P. Siwakoti and J. Zhu, "Model Predictive Control without Weighting Factors for T-type Multilevel Inverters with Magnetic-Link and Series Stacked AC-DC Modules," *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, 2019, pp. 5603-5609. doi: 10.1109/ECCE.2019.8912486 (Published)

[8] **S. A. Khan**, M. N. Habib Khan, Y. Guo, Y. P. Siwakoti and J. Zhu, "A Novel five-Level Switched Capacitor Type Inverter Topology for grid-Tied Photovoltaic Application," *In proc. 2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, 2020, (Accepted).

[9] **S. A. Khan**, Y. Guo and J. Zhu, "Model predictive control applied to a single phase seven-level active rectifier," *2017 20th International Conference on Electrical Machines and Systems (ICEMS)*, Sydney, NSW, 2017, pp. 1-6. doi: 10.1109/ICEMS.2017.8056405 (Published).

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[12] **S. A. Khan**, M. N. Habib Khan, Y. Guo, Y. P. Siwakoti, and J. Zhu, "A novel single source three phase seven-level inverter topology for grid-tied photovoltaic application." *In proc. International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, Nanjing, 2020. (Accepted)

Abstract

In recent years, the traditional electrical power grids are gradually changing into smart grids and emerging as the next-generation power systems. The application of power electronics is playing a vital role in these changes. The recent advancements in power electronics have provided significant momentum for high penetration of renewable energy sources, energy storages, and modern loads into the hybrid microgrid associated with the smart grid. Nevertheless, it also introduces several challenges in terms of reliability and robustness, power quality, and cost. Developing advanced control strategies and converter architecture to mitigate these challenges will be vital. This thesis presents advanced control strategies and circuit architectures for the grid-connected system in hybrid-microgrid applications. The system parameter variations and uncertain disturbances are critical for achieving the control objectives in AC/DC power conversion. In this thesis, disturbance rejection based control strategies have been proposed and implemented to ensure improved steady-state and dynamic performances to follow the references. The control of power converters connected with the electrical grid requires fast and accurate estimation of grid voltage parameters (i.e., amplitude, phase, and frequency), which are carried out using the grid synchronization method. The performance of synchronization methods is affected by the growing power quality issues. This thesis presents novel methods for fast and accurate estimation of the grid voltage parameters. These methods demonstrate enhanced performance to eliminate the disturbances, such as the presence of DC-offset, harmonically distorted grid, grid frequency variations, voltage sag and swell, etc. This thesis also presents a novel single-source three-phase multilevel converter with voltage boosting capability for medium-voltage photovoltaic applications. The new circuit structure significantly reduces the DC-link voltage requirements, the number of components and their voltage stresses in comparison to traditional topologies. It can reduce the dc-link voltage requirements by 75% in comparison to the traditional neutral point clamped (NPC), flying capacitors, active NPC (ANPC), hybrid and hybrid clamped ANPC topologies, and 50% to advanced ANPC topologies. It can also reduce the number of required switches and capacitors as well as their voltage stresses compared to these state-of-the-art topologies reported in the literature so far. The performance

of the proposed control techniques and circuit topologies have been validated by simulation and experimental results.

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Nomenclature

Global abbreviations used in this thesis

AC	=	Alternating Current
ANPC	=	Active Neutral Point Clamped
APF	=	Active Power Filters
AHB	=	Asymmetrical H-Bridge
ANF	=	Adaptive Notch Filter
AFE	=	Active Front End
BW	=	Bandwidth
CMBMC	=	Common Magnetic-Bus Multilevel Converter
CHB		Cascaded-H-bridge
DC	=	Direct Current
DES	=	Distributed Energy Source
DG	=	Distributed Generation
DSP	=	Digital Signal Processor
DPC	=	Direct Power Control
EV	=	Electric Vehicle
ES	=	Energy Storage
ESS	=	Energy Storage Systems
ESO	=	Extended State Observer
EMI	=	Electromagnetic Interference
EMC	=	Electromagnetic Compatibility
FCS	=	Finite Control Set
FIR	=	Finite Impulse Response
FLL	=	Frequency-Locked Loop
FLC	=	Fourier Linear Combiner
FC	=	Flying Capacitor
G2V		Grid-to-Vehicle
IIR	=	Infinite Impulse Response
IPT	=	Inverse Park Transformation
LPF	=	Low Pass Filter
LMS	=	Least Mean Square
MLI	=	Multilevel Inverter
MC	=	Multilevel Converter
MPC	=	Model Predictive Control
MMC	=	Modular Multilevel Converters
MAF	=	Moving Average Filter
MMPD	=	Modified Mixer Phase Detector
MWFLC	=	Modified Weighted-Frequency Fourier Linear Combiner
NPC	=	Neutral Point Clamped
NF	=	Notch Filter
PI	=	Proportional Integral

PR	=	Proportional Resonant
PV	=	photovoltaic
PCC	=	Point of Common Coupling
PLL	=	Phase-Locked Loop
PD	=	Phase Detector
PWM	=	Pulse Width Modulation
QSG	=	Quadrature Signal Generation
RES	=	Renewable Energy Source
RECS		Renewable Energy Conversion System
SMC	=	Sliding Mode Controller
SVR	=	Step Voltage Regulator
STATCOM	=	Static Synchronous Compensator
SOGI	=	Second-Order Generalized Integrator
SRF	=	Synchronous Reference Frame
THD	=	Total Harmonic Distortion
TD	=	Transfer Delay
UPS		Uninterruptible Power Supplies
VSC	=	Voltage Source Converter
V2G	=	Vehicle-to-Grid
VOC	=	Voltage Oriented Control
VCO	=	Voltage-Controlled Oscillator
WES	=	Wind Energy System
WFLC	=	Weighted-Frequency Fourier Linear Combiner

1 Introduction

This chapter presents the background and motivation of this research, followed by the organisation of this thesis to present the flow of the research work. The state-of-the-art technologies, project objectives, and limitations are outlined and discussed.

1.1 Background

In recent years, the traditional power grids are evolving to smart grids and emerging as the next generation of power systems. The smart grids encompass interconnected clusters of microgrids and consist of a combination of single/three-phase loads and generation units. These microgrids comprise AC and DC subgrids, known as hybrid microgrids, where the distributed generation units, energy storages, and loads are connected through power electronics converters [1, 2]. The recent developments of semiconductor devices, high-speed processor, and advanced controller applications in power electronics have provided significant momentum in increasing the penetration of the distributed energy sources (DESs) into the grid. Nevertheless, the high penetration of power electronics-based system imposes new challenges such as (1) smooth integration of the DESs into the grid under grid disturbances, (2) ensuring system reliability, robustness, and stability, (3) maintaining the required power quality, and (4) meeting the requirements in terms of efficiency, price, system size and weight. Therefore, it calls for a significant improvement of converter structures and associated control strategies to mitigate these challenges for smart interfacing of energy sources and loads into the microgrid.

The hybrid microgrids encompass a combination of single-phase/three-phase generation units and loads. Single-phase generation units and loads in residential and commercial buildings form an essential part of distributed grids compared with the dominantly three-phase industrial buildings [2]. Single-phase voltage-source converters (VSCs) are the main component to integrate DC-bus microgrids comprising electric vehicles (EVs), energy storages (ESs), and renewable energy sources (RESs) into the distribution grid. The VSCs can also perform other important tasks, such as active voltage regulation provided by the

DESs power conversion system, injecting high-quality current, and synchronization [3-6]. In such a single-phase power conditioning system, the control of DC-bus voltage is a significant task to ensure the reliable operation of the power conversion system [7-10]. It is thus of great importance to design a robust control system for the VSCs. In single-phase VSCs, the DC-bus voltage control, and active/reactive power control are the challenging task due to the presence of the double-grid frequency ($2\omega_0$) pulsating power component. It flows through the DC side of the converter and causes double-line frequency voltage ripple in the DC-bus voltage. The presence of this voltage ripple in the DC-bus is inherent in both inverter and rectifier mode operations. This ripple component also exists in these-phase unbalanced systems [7, 11-15]. The presence of this ripple in a feedback control system degrades the quality of AC current by adding additional harmonics, and therefore, it must be removed in order to achieve high-quality power conversion.

Generally, a low bandwidth proportional-integral (PI) controller is employed to regulate the DC-bus voltage to eliminate the effect of $2\omega_0$ ripple in a feedback control system. The low bandwidth controller, however, introduces a significant phase delay in the DC-bus voltage control loop. As a result, the control performance to regulate the DC-bus voltage is affected during transients, and the converter must be designed to ensure reliable performance against the overvoltage during the transient. A high bandwidth controller is required to have improved dynamic performance, and thus, a trade-off should be made between the conflicting constraints, such as the grid current quality and dynamic performances [3, 16]. The DC-bus voltage is affected by the active power variations, which can be caused by the connection/disconnection of RESs or the critical load [17]. The variations in the active power can cause fluctuations in the DC-bus voltage and may trigger the protection systems if the bus voltage is not well controlled. DC-bus capacitance variation is another concern which also affects the DC-bus voltage controller. The DC-bus capacitance variation is usually caused by the connection or disconnection of converters into the DC-bus [18]. Any voltage events may cause all the converters to trip and, thus an unwanted transient phenomenon can occur on the bus voltage. Therefore, the DC-bus voltage control in a hybrid microgrid is of major concern and has become a key challenge to address.

A significant aspect of controlling the grid-connected power converters is the grid synchronization. A robust grid synchronization method is required by the control unit for the accurate and fast estimation of grid voltage fundamental parameters (e.g., grid voltage amplitude, phase angle and frequency). Numerous synchronization methods have been reported in the literature. All the methods work accurately in extracting the grid voltage parameters under the ideal grid condition. However, in practice, the real-life electrical power system is affected by the presence of various events. The performance of the synchronization method is affected by various disturbances in the grid, especially under grid faults. Large installation of power electronics systems in the grid such as photovoltaic (PV) system, wind energy systems (WESs), energy storages (ESs), and non-linear loads connected at the point of common coupling (PCC) increases grid harmonics and DC current, which also affect the performance of the synchronization methods. The grid synchronization system is responsible for keeping the smooth connection of the power electronics system to the grid and meeting the grid connection standards such as maintaining the required power quality and limiting the DC current injection into the grid. Poor transient performances of the synchronization methods may cause instability in the systems and may damage the components in the converters. Therefore, a synchronization unit should respond fast and accurately to common disturbances faced by equipment interfacing with the power grid [19-23]. The challenge is to design a robust synchronization method for fast and accurate estimation of the grid parameters under adverse grid conditions.

In hybrid microgrids, the renewable energy sources like PV systems are connected into the grid through single-phase or three-phase DC/AC power converters. Power electronic designs have usually been cost driven. For grid-connected applications, the DC-link voltage should be higher than the peak of the AC grid voltage in order to inject power into the grid. The voltage requirements can be up to twice the grid voltage for some topologies like traditional neutral point clamped (NPC) converter. Therefore, in grid-connected PV systems, a high-boost DC/DC stage is required to provide the required voltage level to feed the DC/AC converter topologies, which can be realized by using multiple DC/DC boost converters, or a large number of series-connected PV panels. The use of multiple converters as the front-end converter reduces overall system efficiency and reliability. Moreover, it increases system cost,

converter size, and control complexity. For PV applications, alternately, a series of PV panels can be employed to eliminate extra boost stage to provide the desired DC-link voltage levels. However, the series connection of PV panels can cause mismatch among the PV panels, which reduces the amount of energy extracted from the PV panels [24]. Therefore, improving system performance through sophisticated circuit structure with reduced control complexity, cost and component count is usually desired, and has become important challenges to address.

1.2 Research Motivation

Research focusing on hybrid microgrid attributes to designing high-performance circuit topology and associated controller to enhance the system performance in terms of reliability, cost, and power quality. The energy generation units and nonlinear loads in the industry and residential area are emerging as the inevitable part of smart grids. The distributed generations (DGs) comprise PV, WE, ES, and EV battery storage. Nowadays, it is desired that the RESs would be a significant part of power generation and should support the grid when required. Besides the RESs, the battery used in EVs, and energy storages may support the grid. The single-phase bidirectional AC/DC converters are the key component used to interface the DC-bus microgrid, which consists of the generation units and nonlinear loads. The control of these converters is of great importance for the smooth integration of the components in DG and supporting the grid by offering reactive power compensation. Compared to the three-phase system, the control of active and reactive power is a challenging task in single-phase power conversion systems due to the presence of double-grid frequency power ripple. In order to filter this ripple, the control scheme requires a low bandwidth controller. However, the low bandwidth controller introduces a high phase delay in the control loop, and thus degrades the transient performance of the closed-loop control system. The active power drawn by the converter varies due to the connection and disconnection of critical loads and renewable energy sources in the DC-bus. It affects the DC-bus voltage controller and can trigger the protection system. The DC-bus capacitance variations are usually caused by the connection or disconnection of converters into the DC-bus [18], which also affect the DC-bus voltage controller. Addressing the shortcomings of the existing controller to reject uncertain disturbances has been the main motivation behind developing more advanced controller.

The grid synchronization plays a significant role in the operation of power converters interfaced into the grid. It is responsible for delivering high-quality power into the grid from RESs and ESs, maintaining the grid current quality during ESs and electric vehicles (EVs) charging, and accurate control of active and reactive power during power transfer with the grid. Smooth integration of the sources and loads connected into the grid also depends on the performance of the synchronization methods. A robust synchronization method should respond fast and accurately to common disturbances faced by electric grid such as line notching, phase jump, frequency variations, voltage unbalance, line dips and harmonics. The synchronization unit is a small part of the controller and thus should be designed with low complexity and computational burden. The most popular and widely used synchronization method is the phase-locked loop (PLL). Among various PLLs, the structure of power based PLL (pPLL) is simple, and its parameter tuning and analysis are straightforward [25]. Nevertheless, the limitations of the pPLLs include the follows. It does not provide the grid voltage amplitude information, it suffers from oscillatory error in the estimated grid frequency and phase in the presence of grid impurity and under off-nominal grid frequencies, and it presents poor dynamic performance under adverse grid conditions. Due to these limitations, the pPLLs are not a widely used method for grid synchronization in real-time applications, although the structure is simple, and its parameter tunning is straightforward.

In recent years, the quadrature signal generation (QSG) based PLLs have attracted much attention, and are widely used in grid-connected applications [25, 26]. Most QSGs can provide an accurate estimation of the fundamental and their quadrature component of the grid voltage as long as the grid voltage is in the ideal condition such as that the grid frequency is always fixed and not polluted by harmonic/subharmonics or DC component. Nevertheless, the above-mentioned situation for the grid voltage may not always exist, particularly in microgrids and weak grid conditions [26]. Some of the QSGs require accurate estimation of the input signal frequency to generate the fundamental and its quadrature component of the input signal. Most QSGs methods do not provide sufficient filtering and thus suffer from oscillatory error in the estimated quantities if the input signal is polluted by harmonics, subharmonics, and DC-offset. There are some PLLs which have been proposed recently to improve the performances. However, these methods are complex in their structure, requiring

long computation time, ineffective under wide frequency variations and suffering from oscillatory error in the presence of DC-offset and subharmonics. Addressing the shortcomings of the existing PLLs has been the main motivation behind developing more advanced PLLs.

In hybrid microgrids, most generations are usually from distributed energy sources like PVs. These sources are interfaced in the grid side through DC/AC converters. These converters are responsible for the power conversion and the power quality concern. High installation and equipment cost of PV power conversion system brings the focus of research towards the design of advanced topology and associated controller. In PV systems, the PV modules are integrated through DC/AC inverters and their associated DC/DC converters. Over the decades, traditional two-level inverters have been commonly employed topology due to their simplicity. It shows that compared to the traditional two-level inverters, multilevel inverters (MLIs) are potentially attractive and extensively used in a wide range of power conversion applications ranging from low to high voltage/power conversion systems. The MLIs enable the use of low-cost switching devices, reduce filter size, and reduce losses in the semiconductor switches while generating high-quality power. Different types of MLIs are available in the literature to synthesize multilevel output voltage and widely employed in different applications. Most of the topologies are cost-driven due to the use of a large number of components, requiring complex control strategy, high voltage rating components, and high DC-link voltage. Some of the topologies require independent DC voltage sources. For grid-connected applications, the DC-link voltage should be higher than the peak of the AC voltage at the point of common coupling (PCC). Most MLI topologies require high DC-link voltage, and it can be up to twice of PCC peak voltage. For example, the popular NPC inverter topology requires twice the PCC voltage in the DC-link. Thus, for PV based generation units, a high-boost DC/DC converter is required for generating the required DC-link voltage, which can be realized by using multiple cascaded DC/DC converters. Thus, it increases system cost, converter size, and control complexity. Alternately, the high DC-link voltage can be generated by using a large number of series-connected PV modules. However, it may cause mismatch among the PV modules, and thus, reduces the extracted energy from PV systems. Considering this aspect, addressing the shortcomings of the existing topologies has been the main motivation behind developing more attractive circuit architecture.

1.3 Research Objectives and Limitations

1.3.1 Research Questions and objectives

The integration of power electronics converter-based distributed generations (DGs) into the power grid causes emerging challenges. It also provides opportunities for power quality control. The emerging challenges will be further increased in the future due to high penetration of power electronics-based DGs and loads, and we need to deal with the following questions:

- *What control strategy can be developed to improve the system performance under various disturbances?*
- *What improvement can be made in the grid synchronization techniques to deal with the growing power quality issues?*
- *Is there any method to further reduce the control complexity?*
- *Is there any new converter topology to further reduce the system complexity, cost, and control complexity?*

With these research questions, the objectives of this Ph.D. project are to improve the control performances of the grid-connected power converters and to develop new multilevel converter topology. The main goal of this research project will be concentrated on developing disturbance rejection capability-based controller design for the power converters and designing advanced grid parameter estimation methods for the control unit. Another important goal of this project is to design a new multilevel converter structure with more features. Both goals of this project are achieved in details by:

Advanced control strategies for the grid-connected power converters-

The most crucial part of the grid-connected power converter system is to design a robust controller to ensure system stability and reliability under different conditions. The system uncertainty issues (i.e., converter load changes, parameter variations, and grid disturbances) adversely affect the performance of the controller. To deal with these challenges, some advanced control strategies will be designed in this project. The DC-bus voltage control of the grid-connected converters plays a significant role to transfer power with the grid. The

main objective of this thesis is to design disturbance rejection based control techniques to regulate the DC-bus voltage while maintaining the desired power quality and power factor.

Robust grid parameters estimation methods for power converters-

A robust grid parameters estimation technique is required to ensure the accurate reference signals for the control unit of the grid-connected converters so that they can work safely and effectively. This task is usually done by the grid synchronization method. The grid-synchronization method is responsible for high-quality power conversion and meeting the grid connection standards. The power quality issues in the grid voltage adversely affect the performance of the synchronization method. Moreover, the poor dynamic performance of the synchronization method can cause instability and may damage the devices in the power converter. In this regard, robust synchronization techniques will be presented in this project with advanced functionalities compared with the state-of-art techniques.

Multilevel power converter for grid-connected PV applications-

Multilevel power converters have many advantages compared to the traditional two-level converter topology. Nevertheless, most of the multilevel converter topologies require a high front-end DC voltage power supply. Therefore, in some applications like grid-connected PV system, a high boost DC/DC stage is required to provide the required voltage level to feed the converters, and thus, increase increases system cost, converter size, and control complexity. The key to solving this problem is designing the new converter structure with voltage boosting capability. In this regard, a new multilevel converter topology with voltage boosting capability will be proposed in this project. A predictive control algorithm will be derived to control the converter for synthesizing multilevel output voltage while realizing the desired active and reactive power. These advantages will support the high penetration of PV systems into the grid. A benchmarking of the existing single-source multilevel converter topologies will be carried out.

1.3.2 Project Limitations

Regarding the control scheme implementation, only single-phase five-level converter structures are considered in this project. The developed controller can later be used for other single-phase and three-phase converter structures available in the literature with minor

modifications and adaptions. The experimental studies conducted in this project are carried out at stepped-down grid voltage, which is obtained by using variac. The load disturbances are generated by manual switching, but this can be done by using programmable loads. The grid voltage disturbances are generated in OPAL-RT based environment to test the performances of the developed controller at the nominal grid voltage. The performances of the controller can later be verified by generating grid faults in real-time grid simulator.

The performance of the grid synchronization methods is tested under various grid disturbances, which are generated by using a digital signal processor (DSP) chip. These disturbances can later be generated by using real-time grid simulator or programmable AC power supply.

There are many control schemes available in the literature to track the reference current. Most of the developed control strategies used the predictive current controller. Some other controllers such as proportional resonant (PR) controller are available in the literature. These controllers can also be used, and performances can be evaluated in terms of power quality.

Regarding the proposed multilevel converter testing, only OPAL-RT based system is used in this project to verify the performances at the distribution grid voltage level. Real-time hardware can also be implemented in medium to high voltage level. The performance of the proposed topologies can also be compared by implementing the other existing topologies.

1.4 Thesis Outline

This thesis deals with the converter topology and control design in hybrid microgrid applications. This thesis can be divided into three main aspects; (a) design of advanced control strategies converter structure for grid-connected power converters, which is covered in Chapters 2, 3 and 4; (b) developing robust grid parameters estimation methods for grid-connected power converters, which is presented in Chapters 5 and 6; and (c) designing high performance multilevel converter structure, which is presented in chapter 7. To conduct the stated research objectives, the rest of this thesis is arranged as follows:

Chapter 2 presents a new residential microgrid structure, which consists of high-frequency magnetic-link and a multilevel converter. A control algorithm is developed to control the converters.

Chapter 3 presents the control aspects of the grid-connected five-level power converter. A new cascaded control scheme based on proportional-integral (PI) combined with an observer to better follow the reference DC-bus voltage is presented in this chapter. A predictive current control strategy is developed as the reference current tracking controller for the five-level converter. The developed algorithm also minimizes the capacitor voltages unbalancing problem in the DC-bus of the converter.

Chapter 4 presents a DC-bus ripple estimation method of the grid-connected single-phase power converters. A filter-less method for eliminating this ripple to estimate the DC value of the bus voltage is presented, which improves the dynamic performance of the DC-bus voltage controller. The active power disturbances and system parameter variations can cause fluctuations in the DC-bus voltage, and thus, the converter reliability is challenged and may trigger the protection system. This chapter presents an advanced control strategy based on sliding mode controller (SMC) incorporated with an extended state observer (ESO) to effectively mitigate the challenges. The detailed stability analysis of the proposed controller is also presented in this chapter.

Chapter 5 presents a new power-based phase-locked loop (pPLL), which is capable of estimating the grid voltage amplitude. A frequency estimation approach is employed so that the pPLL can perform well over a wide range of grid frequency. This method eliminates the oscillatory error in the estimated grid frequency in the presence of grid harmonics. The detailed small-signal modeling and stability studies are presented, together with experimental results, to validate the robustness.

Chapter 6 presents a novel quadrature signal generation (QSG)-based grid synchronization method for grid-connected power converters. The presence of DC offset, subharmonics, and frequency drift affect the performance of the existing synchronization methods. These disturbances cause oscillatory and offset errors in the estimated grid parameters, which is addressed in the new method. The developed technique works well in all kind of grid disturbances.

Chapter 7 presents a detailed benchmarking of mainstream multilevel converters in terms of DC voltage requirements, number of components required, and their voltage stress. A novel multilevel converter is presented in this chapter, which reduces the DC voltage supply

requirement, number of components, and their voltage stresses compared to the existing topologies. A predictive control algorithm is also derived to control the converter that has performed well in realizing the desired active and reactive power.

Chapter 8 summarizes the main contributions of this project. Besides, future research directions are also outlined in this chapter.

2 Multi-Sourced Energy Conversion Systems in Residential Microgrid

2.1 Introduction

Nowadays, efforts are being made to harvest the maximum energy from clean renewable energy resources (RESs) due to environmental and global sustainability concerns. With the large-scale RESs installation, distributed generations (DGs) have been placed as a possible mainstream way of electric power generation over the fossil fuel-based centralized generation systems. In particular, multiple DGs are used in conjunction with central electric power generators to support the utility grid. To overcome the future energy crisis, the residential house should be a component of the DG system and must have the capability to provide power for the residential electricity demand and support the utility grid when required. Despite several advantages, this scheme involves substantial transients compared to the centralized electric power generation system, because of the intermittent nature of RESs [27-29]. Therefore, reliability and robustness are the main challenges associated with this scheme towards the successful implementation of the smart grid. To overcome these challenges, energy storage systems can provide a promising solution to bring RESs into the mainstream power generation [30-32]. With the exponentially growing installation of energy storages (ESs), they can be used as the substantial energy storage for DGs to store excess energy from the RESs [33-36]. When energy demand is higher during peak load, the stored energy should be released to support the utility grid. Besides energy storing service, the ESs can also provide some other ancillary services such as reactive power compensation, load voltage control, and current harmonic filtering services [8, 37, 38]. Hence, the importance of energy storage is very evident to support the grid to overcome the challenges associated with the intermittent nature of RESs. The voltage regulation in the distributed generation system is an important issue. When the grid interfaced RESs generates more power than the local load demand, the excess power from the RESs increases the voltage level in the network. The intermittent nature of RESs, such as photovoltaics (PVs) also creates an oscillation in the distribution system grid voltage. The voltage fluctuation events in the gird voltage can cause the grid-

connected converters to trip and would cause the unwanted transient phenomenon. The reactive power injection into the can help in realizing the regulated grid voltage. The step voltage regulator (SVR), static VAR compensator (SVC), and static synchronous compensator (STATCOM) can be used to regulate the voltage within the desired range [39-41]. However, the high installation cost of these devices encourages us to use an alternative approach to regulate the voltage. Nowadays, it is desired that the RESs and ESs systems installed in the residential and commercial application should participate in voltage regulation by storing excess energy in the storage system and injecting reactive power into the grid to regulate the grid voltage. The desired amount of reactive power can be generated based on the demand by the grid by smartly controlling the converters interfaced into the grid. As the RESs installation is increasing, the voltage regulation in the distribution system is becoming very difficult. Thus, the concept of voltage regulation by controlling the grid-interfaced power electronics converters is becoming inevitable.

The DC/AC converters are the key components used as an interface among the RESs/ESs and the distribution grid. These converters are responsible for dealing with increasingly stringent grid connection standards, power quality, as well as performing other ancillary services like voltage regulation by reactive power injection into the grid. In residential/industrial applications, a common converter architecture usually used for renewable energy integration is the full-bridge two-level converter. Compared with conventional two-level converters, multilevel AC/DC converters present more advantages and have gained popularity in recent years due to their emerging applications. These benefits include reduced current harmonics, higher voltage-handling capability, higher power density, and lower switching losses. These converters have traditionally been used in energy storage systems (ESS), vehicle-to-grid (V2G), grid-to-vehicle (G2V), uninterruptible power supplies (UPS), and DC microgrids to effectively control power flow in the AC grid [19, 34, 37, 42, 43]. Consequently, various topologies and control techniques have been proposed over the years with a pertinent focus on improving the system dynamic performance and robustness. It is very evident to satisfy several requirements to interface REs and ESs with the utility grid. The design of a reliable and robust control system is also crucial for grid-connected the AC/DC converters for realizing the desired active and reactive power.

Usually, the RESs and ESs interface with the power grid is realized by using different power conversion systems, such as one DC/DC converter to boost up the RESs/ESs voltage level and one two-level DC/AC converter to interface the grid.
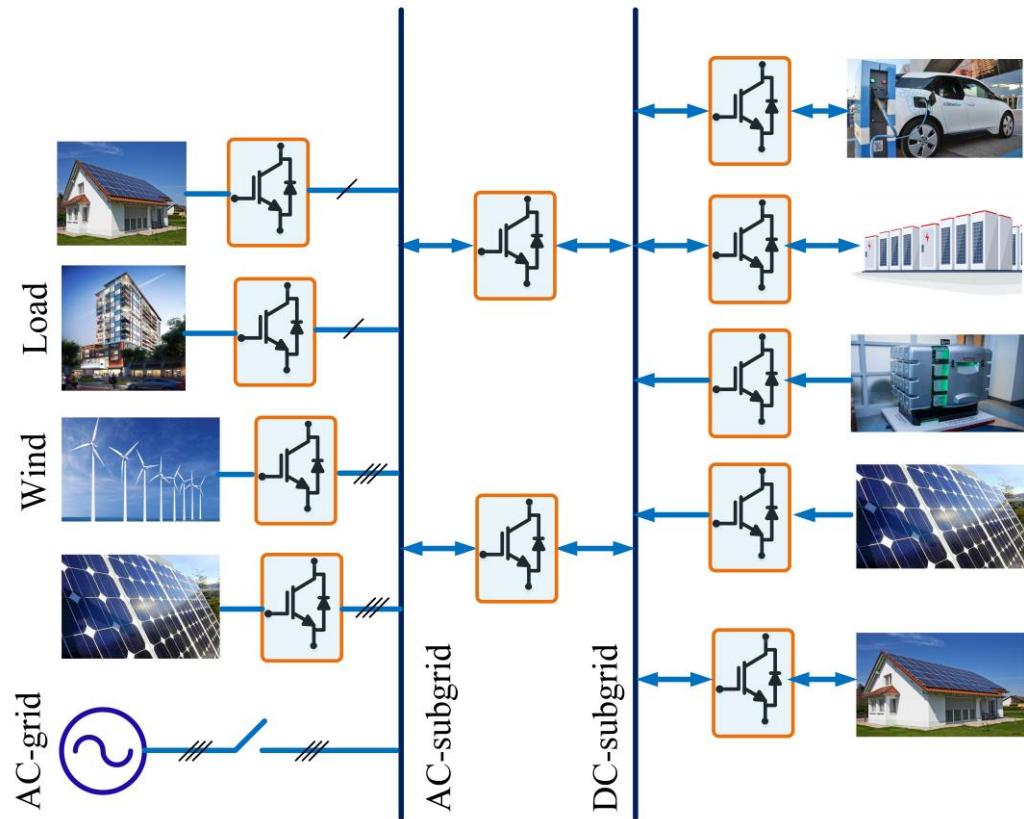
Fig. 2.1 Structure of a typical hybrid microgrid system.

Fig. 2.1 shows the typical structure of a hybrid microgrid system. Based on this structure, the RESs and ESs installed in residential and commercial applications are integrated into the AC sub-grid through different power electronics-based energy conversion systems. Fig. 2.2 illustrates the existing approaches to interface these sources into the AC grid [212]. According to this figure, the use of magnetic-link-based converter system reduces the required number of power converter cells. As a consequence, it reduces the system's size and cost. Since the number of power electronics-based systems integration into the grid is increasing, the harmonics in the grid voltage is also noticeably increasing. The use of multilevel converter in the grid-side can significantly reduce the harmonics injected into the grid. In recent years,

multilevel converters have been widely used in low-voltage applications (below 690 V), like photovoltaic (PV) inverters, uninterruptible power supply (UPS) systems, and wind energy (WE) conversion systems [44]. This work is focused on developing advanced converter structure with reduced power conversion stages and associated control scheme to integrate RESs and ESs into the grid, and producing the required reactive power to regulate the grid voltage, while reducing the harmonics injected into the grid incorporating multilevel converter.
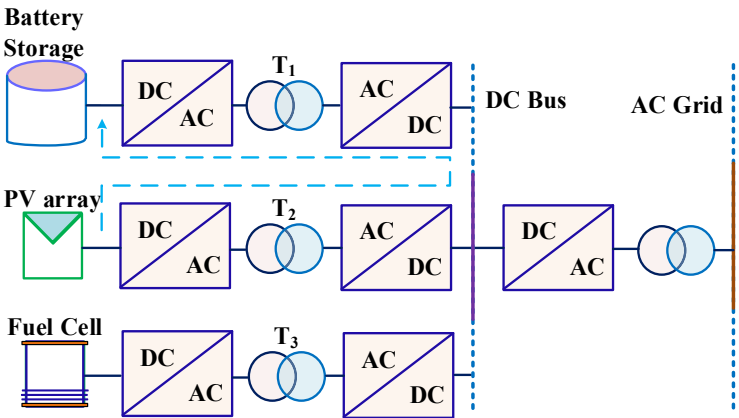
(a) without magnetic-link.
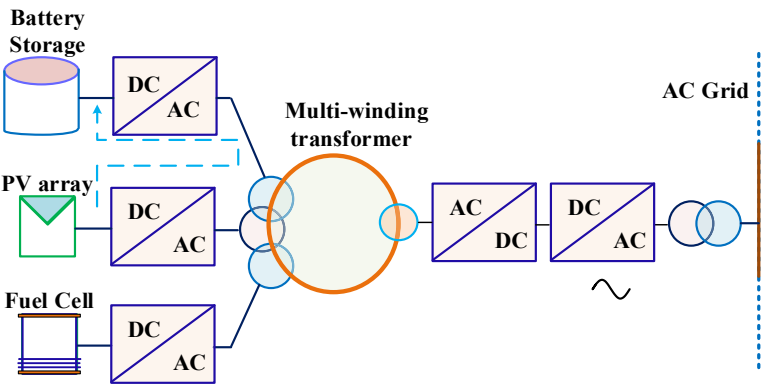
(b) with magnetic-link.

Fig. 2.2 Traditional two typical power converter structures installed in residential/industrial applications, (a) without, and (b) with the magnetic-link.

2.2 Proposed System

The motivation of this work is to develop an improved converter structure with reduced components and the associated control strategy to address the challenges of the existing systems. In this regard, a common magnetic-bus multilevel converter (CMBMC) is presented in this work. This structure comprises a single-input/multi-output port high-frequency magnetic-link. Fig. 2.3 illustrates the proposed CMBMC structure. This converter consists of a common magnetic-bus, where multiple sources are interfaced through DC/DC converters. Compared to the other structures, including the approaches illustrated in Fig. 2.2, this approach reduces the number of power conversion stages to integrate multiple sources. However, the main challenge with this structure is to regulate the bus voltage. If RESs, such as PV panels are connected in the bus, the converters interfaced with the PVs need to operate at different voltage levels due to varying environmental conditions in order to extract the maximum available power from the PVs. The bus voltage fluctuates due to the varying operating voltage of the PV interfaced converter. As a consequence, it also affects the grid-side converter. This work presents an algorithm to address this problem. In the proposed algorithm, the ESs interfaced converter is controlled to regulate the bus voltage for compensating the voltage fluctuation caused by the varying operating voltage of the PV system. A reference charging/discharging current is calculated to drive the bidirectional DC/DC converter connected with the ESs. The operation of the CMBMC is defined according to the energy in the PV panels, required active and reactive power to be injected into the grid, and the rated power of the converter. The PV and ES systems are operated based on a coordinated control system. In this system, if the available energy in the PV panels is higher than the demanded active power, the extra power is stored in the ES. After meeting the active power demand, the converter can provide the required reactive power support to stabilize the grid voltage.

The magnetic-link consists of multiple output ports. The number of turns in the transformer depends on the required voltage transformation ratio, which is designed based on the bus voltage and the DC/AC stage requirements. In the proposed MLI structure, each output port is connected to a full-bridge AC/DC module followed by a filtering capacitor to

generate smooth DC voltages from the high-frequency AC voltage. The purpose of generating multiple constant DC voltages is to provide the required voltage levels for the multilevel inverter structure. The DC ports of the AC/DC modules are connected in series to add up the DC voltages. In this structure, the AC/DC modules are stacked as a parallel-AC series-DC system. The purpose of series DC stacking is to deliver the required voltage levels for the MLI. The employed MLI structure is based on T-type configuration, where bidirectional switches are introduced to connect with the stacked modules and the middle point of a leg of the H-bridge cell.
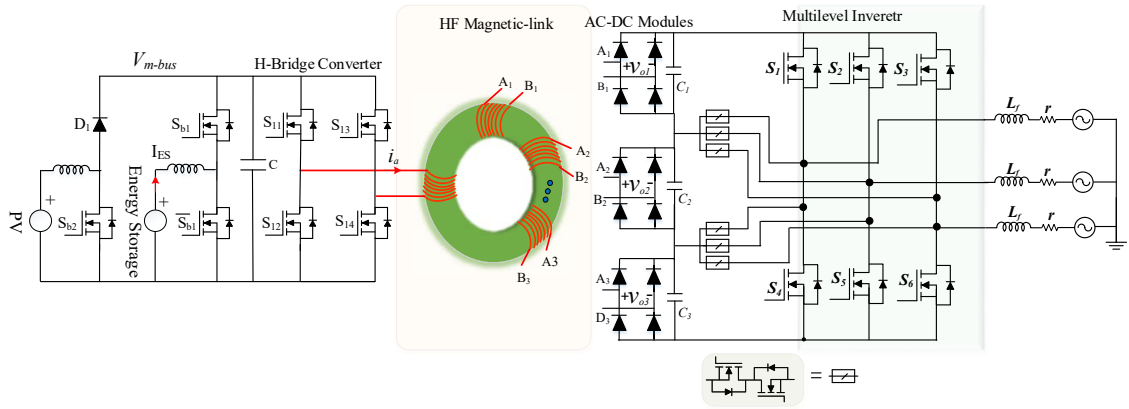
Fig. 2.3 Proposed circuit structure for residential/industrial applications.

Magnetic-link-based architecture provides galvanic isolation, which is mandatory for different applications. The MLI is controlled to operate at leading and lagging power factor while realizing multilevel voltage output to ensure high-quality power from the energy sources.

2.3 Control Algorithm

The block diagram of the proposed scheme is illustrated in Fig. 2.4. In the proposed circuit structure, the unidirectional DC/DC boost converter is employed to interface the PV modules into the common magnetic-bus, whereas a bidirectional DC/DC converter is employed to interface the energy storage unit. The major advantages of this structure are that it can integrate multiple converters in a single bus with reduced circuit components and provides the necessary galvanic isolation from the grid. The operation of the CMBMC is

defined based on the available energy in the PV, demanded active and reactive power from the central controller, and the rated power of the converter.
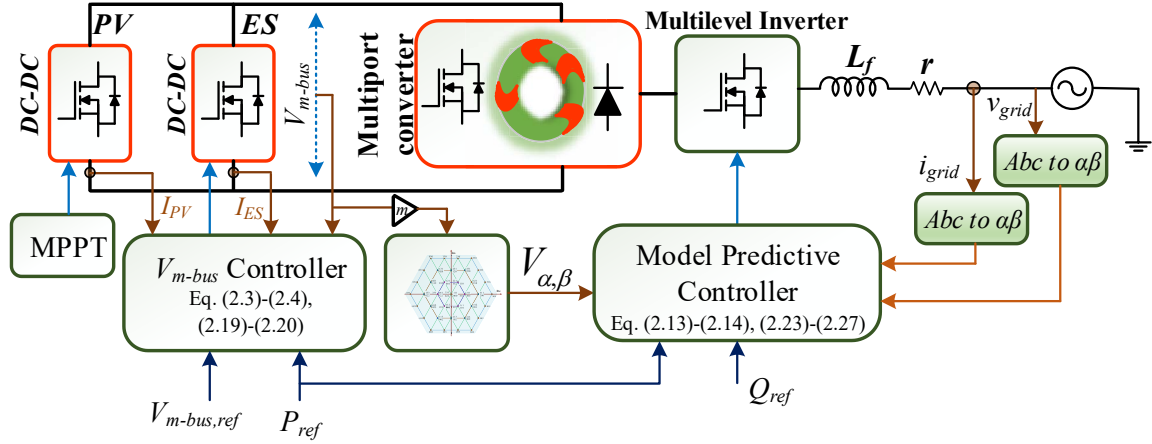
Fig. 2.4 Proposed control scheme block diagram.

To calculate the reference charging/discharging current of the energy storage unit for the operation of CMBMC during different modes, a power theory should can be defined as

$$P_{grid} = p_{pv} + p_{ES} + p_{bus} \tag{2.1}$$

where p_{pv} is the PV modules power, p_{ES} is the ES power (which is positive during the discharging mode and negative during the charging mode), p_{bus} denotes the power necessary to regulate the magnetic-bus voltage, and S_{grid} is the total power delivered into the grid that can be represented as

$$S_{grid} = P_{grid} + jQ_{grid} \tag{2.2}$$

where P_{grid} and Q_{grid} are the injected active and reactive power, respectively.

For a given environmental condition, the operating voltage and current of the PV interfaced converter vary to extract the maximum power from the PV panels. Thus, in order to ensure the maximum power from the PV panel and regulated bus voltage, the reference charging/discharging current of ES (I_{ES}) is defined as

$$I_{ES} = I_{m-bus} - I_{PV} = \frac{n(p_{ref} + p_{bus})}{V_{m-bus}} - I_{PV} \tag{2.3}$$

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where $V_{m\text{-}bus}$ is the reference magnetic-bus voltage, and n is the voltage gain of the bidirectional DC/DC converter.

The difference between the desired common magnetic-bus voltage and the measured voltage at the point of common coupling determines the reference power (p_{bus}) to regulate the bus voltage. In the proposed control algorithm, the reference p_{bus} is calculated by using proportional-integral controller. The expression for p_{bus} is given by

$$p_{bus} = \left(k_P(V^*_{m-bus} - V_{m-bus}) + k_I \int (V^*_{m-bus} - V_{m-bus})dt\right) \times V^*_{m-bus}$$ (2.4)

where V^*_{m-bus} is the reference magnetic-bus voltage shared by the DC/DC converters, and V_{m-bus} is the measured bus voltage.

After meeting the active power demand by the central controller, the converter has the capability to deliver reactive power, which can be calculated as

$$Q_{grid} = \sqrt{S^2_{grid} - P^2_{grid}}$$ (2.5)

where S_{grid} denotes the total power delivered into the grid, and also denotes the rated power of the grid-side converter.

For single-phase circuit, the reference direct axis current (i_d) and quadrature axis current (i_q) can be calculated as

$$i_d = \frac{2P_{grid}}{v_d}$$ (2.6)

$$i_q = -\frac{2Q_{grid}}{v_d}$$ (2.7)

where v_d is the direct axis component of the grid voltage.

The reference grid current for single-phase circuit is given by

$$i_{g-ref.} = \frac{2P_{grid}}{v_d}\sin(\omega t) - \frac{2Q_{grid}}{v_d}\cos(\omega t)$$ (2.8)

where the value of ωt is acquired from a phase-locked loop.

The three-phase structure with eighteen semiconductor switches is fed by the common magnetic-link based multiport converter. The outport port of the magnetic-link consists of diode rectifier to obtain the balanced DC supplies for the grid-side converter, as shown in Fig. 2.3.

The voltage vectors applied to the grid by the inverter can be described in the $\alpha\beta$ frame as

$$v = \frac{2}{3}\left(v_{an} + v_{bn}e^{j(2\pi/3)} + v_{cn}e^{j(4\pi/3)}\right) \tag{2.9}$$

There are 64 voltage vectors available for seven-level operation. Among them, 37 voltage vectors exist in the finite control set due to the redundancy of several voltage vectors that generate equal output voltage vectors. The spatial positions of these 37 voltage vectors are illustrated in Fig. 2.5.
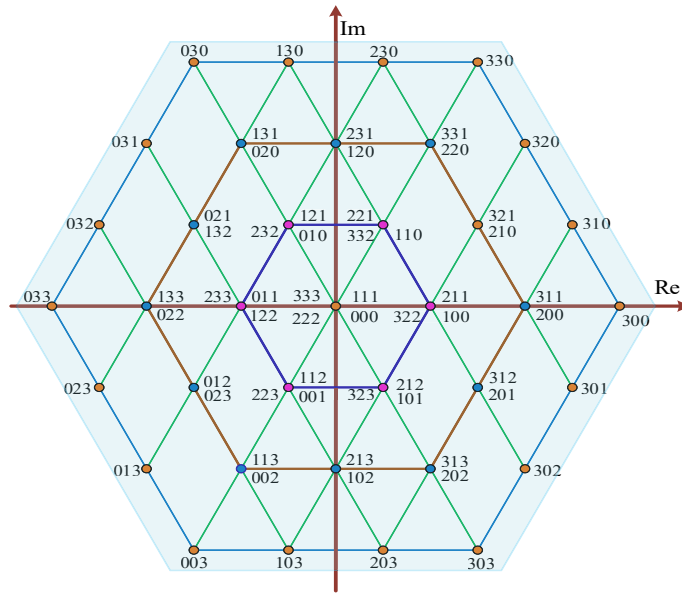
Fig. 2.5 Switching states in *dq0* plane.

The current injected into the grid can also be expressed is the $\alpha\beta$ frame as

$$i = \frac{2}{3}\left(i_a + i_b e^{j(2\pi/3)} + i_c e^{j(4\pi/3)}\right) \tag{2.10}$$

The grid current dynamics can be expressed in the direct axis (i_d) and quadrature axis (i_q) components as

$$\frac{di_d}{dt} = \frac{v_d}{L_f} - \frac{v_{gd}}{L_f} + \omega i_q - \frac{r}{L}i_d \tag{2.11}$$

$$\frac{di_q}{dt} = \frac{v_q}{L_f} - \frac{v_{gq}}{L_f} - \omega i_d - \frac{r}{L}i_q \tag{2.12}$$

where v_{gd}, and v_{gq} are the (d, q) components of the grid voltages, i_d, and i_q are the (d, q) components of the grid currents, L_f is the filter inductance, ω is the grid frequency, and r is the equivalent series resistance of the filter inductor L_f.

Then, the active and reactive powers of this system can be calculated by

$$P = \frac{3}{2}\text{Re}\left(v_g i_g^*\right) = \frac{3}{2}\left(v_{gd}i_d + v_{gq}i_q\right) = \frac{3}{2}\left(v_{g\alpha}i_{g\alpha} + v_{g\beta}i_{g\beta}\right) \tag{2.13}$$

$$Q = \frac{3}{2}\text{Im}\left(v_g i_g^*\right) = \frac{3}{2}\left(v_{gq}i_d - v_{gd}i_q\right) = \frac{3}{2}\left(v_{g\beta}i_{g\alpha} - v_{g\alpha}i_{g\beta}\right) \tag{2.14}$$

Considering a lossless system, the power balance relation between the grid-side inverter and the proposed common magnetic-bus based DC system can be expressed as

$$V_{m-bus}I_{m-bus} = \frac{3}{2}v_{gd}i_d \tag{2.15}$$

2.3.1 Bidirectional DC/DC Converter

In the CMBMC, the bidirectional DC/DC converter is employed to transfer power from the PV panels to the ES and ES to the grid. During the ES charging/discharging, the converter is controlled to charge/discharge at constant current according to the desired reference value calculated from (2.3). The switches in the converter are operated in the opposite manner to avoid a short circuit. When the switching state of the switch Sw_1 is on, the dynamical behavior of the bidirectional DC/DC converter can be expressed as

$$V_{m-bus} = L\frac{di_{ES}}{dt} + V_{ES} \tag{2.16}$$

where V_{ES} is the energy storage voltage, L is the inductance of the circuit, and i_{ES} is the instantaneous value of the ES current.

Similarly, when the switching state of the switch Sw_1 is off, the dynamical behavior of the converter is expressed as

$$L\frac{di_{ES}}{dt} + V_{ES} = 0 \tag{2.17}$$

According to (2.16) and (2.17), the dynamics of the converter can be expressed as

$$S.V_{m-bus} = L\frac{di_{ES}}{dt} + V_{ES} \tag{2.18}$$

where S is the switching state. According to the forward Euler's approximation with a sampling period Ts, (2.18) can be written as

$$i_{ES}^{k+1} = i_{ES}^{k} + \frac{T_S}{L}(S.V_{m-bus} - V_{ES})$$ (2.19)

To realize constant charging/discharging operation of the ES, the cost function can be defined as

$$G = (i_{ES}^{k+1} - i_{ES})^2$$ (2.20)

where i_{ES} is the reference charging/discharging current calculated from (2.3).

2.3.2 Unidirectional DC/DC boost converter

A DC/DC boost converter is employed as an interface between the PV panels and the common magnetic-bus. In this case, the boost converter is controlled to extract the maximum power from the PV panels by using maximum power point tracking (MPPT) algorithm. In the proposed approach, the energy extracted from the PV panels can be stored into the ES or can be transferred into the grid. If the available PV power is higher than the required power to be injected into the grid, the extra power available in the PV panels can be transferred into the ES.

2.3.3 Grid-side inverter

To control the grid side converter, the predictive control algorithm is used. The injected grid current dynamics of the of the inverter can be expressed in the α-β coordinates as

$$\frac{di_{g\alpha}}{dt} = \frac{1}{L_f}v_\alpha - \frac{1}{L_f}v_{g\alpha} - \frac{r}{L_f}i_{g\alpha}$$ (2.21)

$$\frac{di_{g\beta}}{dt} = \frac{1}{L_f}v_\beta - \frac{1}{L_f}v_{g\beta} - \frac{r}{L_f}i_{g\beta}$$ (2.22)

The discrete-time model of the grid current at $(k+1)^{th}$ instant for a sample time Ts can be expressed as

$$i_{g\alpha}^{k+1} = i_{g\alpha}^{k} + \frac{T_s}{L_f}\left(v_{\alpha}^{k} - ri_{g\alpha}^{k} - v_{g\alpha}^{k}\right) \tag{2.23}$$

$$i_{g\beta}^{k+1} = i_{g\beta}^{k} + \frac{T_s}{L_f}\left(v_{\beta}^{k} - ri_{g\beta}^{k} - v_{g\beta}^{k}\right) \tag{2.24}$$

Thus, the expression for the active and reactive power at the $(k+1)^{th}$ instant can be approximated as

$$P_g^{k+1} = \frac{3}{2}\left(v_{g\alpha}^{k}i_{g\alpha}^{k+1} + v_{g\beta}^{k}i_{g\beta}^{k+1}\right) \tag{2.25}$$

$$Q_g^{k+1} = \frac{3}{2}\left(v_{g\beta}^{k}i_{g\alpha}^{k+1} - v_{g\alpha}^{k}i_{g\beta}^{k+1}\right) \tag{2.26}$$

For realizing the desired active and reactive power, the cost function $J_{cost.}$ is defined as

$$J_{Cost.} = \left(P_g^{k+1} - P_{ref}\right)^2 + \left(Q_g^{k+1} - Q_{ref}\right)^2 \tag{2.27}$$

where P_{ref} and Q_{ref} are the active and reactive power references, respectively.

2.4 Simulation Results

Fig. 2.6 presents a typical operation of the CMBMC considering the PV to grid, and ES and PV to grid operation modes, where the injected active and reactive power is varied according to different grid requirements. During the first time interval (1.25 s to 1.3 s), the CMBMC is controlled to operate in PV to grid operation mode. In this mode, 1 kW active power is injected into the grid provided only by the PV system. The reference magnetic-bus voltage is set to 200 V. In this mode, the PV power is equal to the sum of injected power into the grid and the power loss in the circuit. During the second time interval (1.3 s to 1.38 s), the available PV power is varied, and the desired active power is still 1 kW. As it can be seen that the ES discharging current is changed from 0 to the required value to inject 1 kW active power to the grid. The second trace shows the bus voltage during this transient. As shown, the bus voltage is stabilized to 200 V. During the third time interval (1.38 s to 1.46 s), the active power reference value is changed from 1 kW to 1.5 kW, and the available PV power is kept the same. As it can be seen that the discharging current is changed accordingly to inject the new active power reference into the grid. The bus voltage is also stabilized after the transient while generating the distinct seven-level voltage, as shown in the fifth trace of Fig. 2.6. During

the interval from 1.25 s to 1.46 s, the desired reactive power is set to 0 Var. The fourth trace in Fig. 2.6 shows that the grid current and voltage are kept in phase. During the first time interval (1.46 s to 1.52 s), the desired reactive power is changed from 0 Var to -1 kVar. As shown in the fourth trace, the injected grid current phase angle is changed accordingly to generate the desired reactive power. Furthermore, at 1.52 s, the reactive power reference is changed from -1 kVar to 1 kVar. It can be seen that the grid current phase angle is changed to realize the required reactive power. During these transients, the bus voltage is stabilized without noticeable transient.
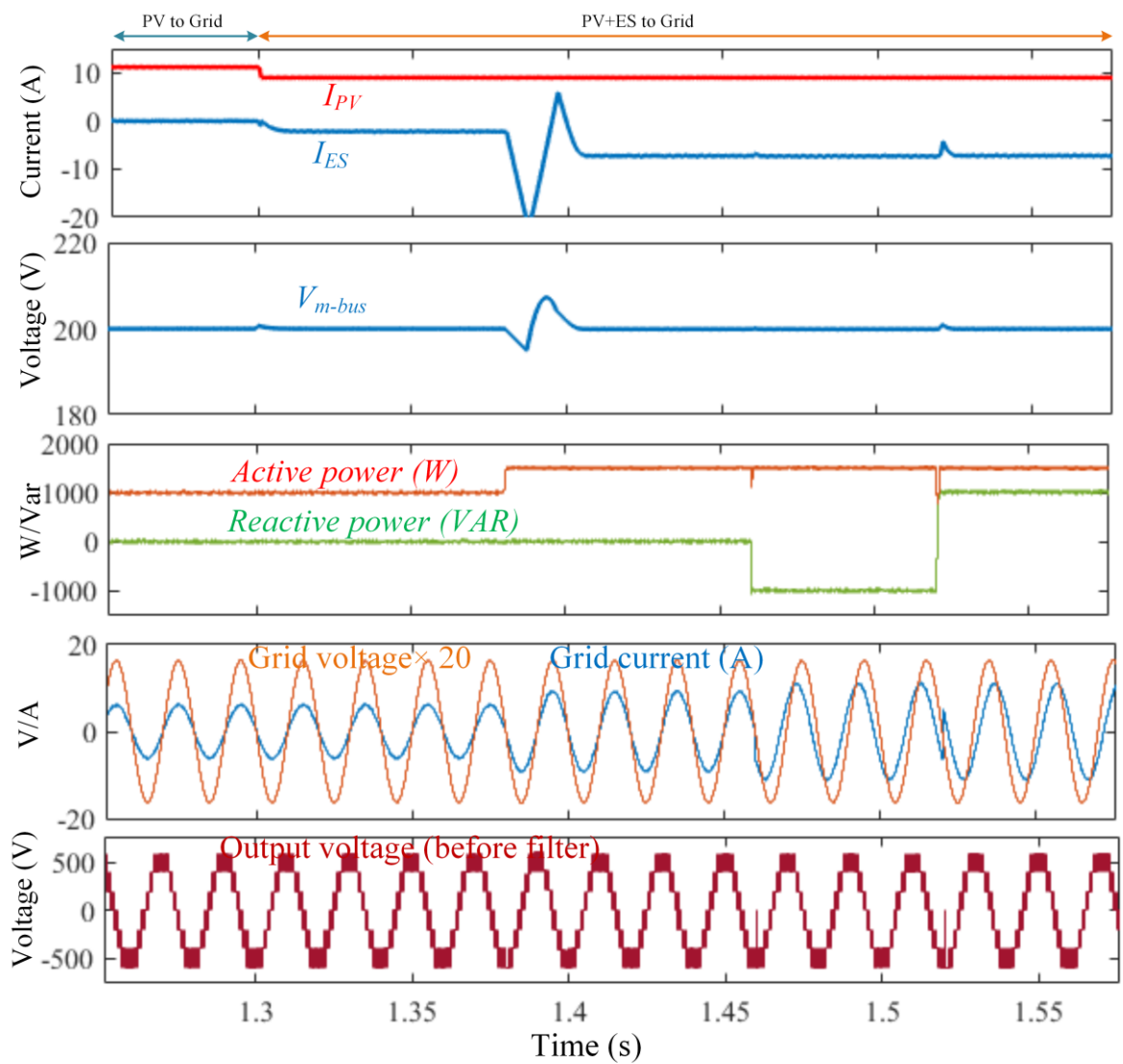
Fig. 2.6 Principle of operation of the proposed CMBMC employed to interface PV and ES into the grid.

An AC-microgrid is also simulated in Matlab/Simulink environment to see the effect of active and reactive power injection on the grid stability. Fig. 2.7 presents a typical operation of the circuit considering the PV to ES, and PV to grid operation modes, where the injected active power is varied 0 to 1 kW. During the first time interval (0.45 s to 0.5 s), the PV available power is set to 1 kW, and the desired active and reactive power to be injected into the grid are set to 0 kW, and 0 kVar, respectively. The grid is operated in normal operation mode and the observed grid frequency is in nominal value, as shown in the second trace of Fig. 2.7.
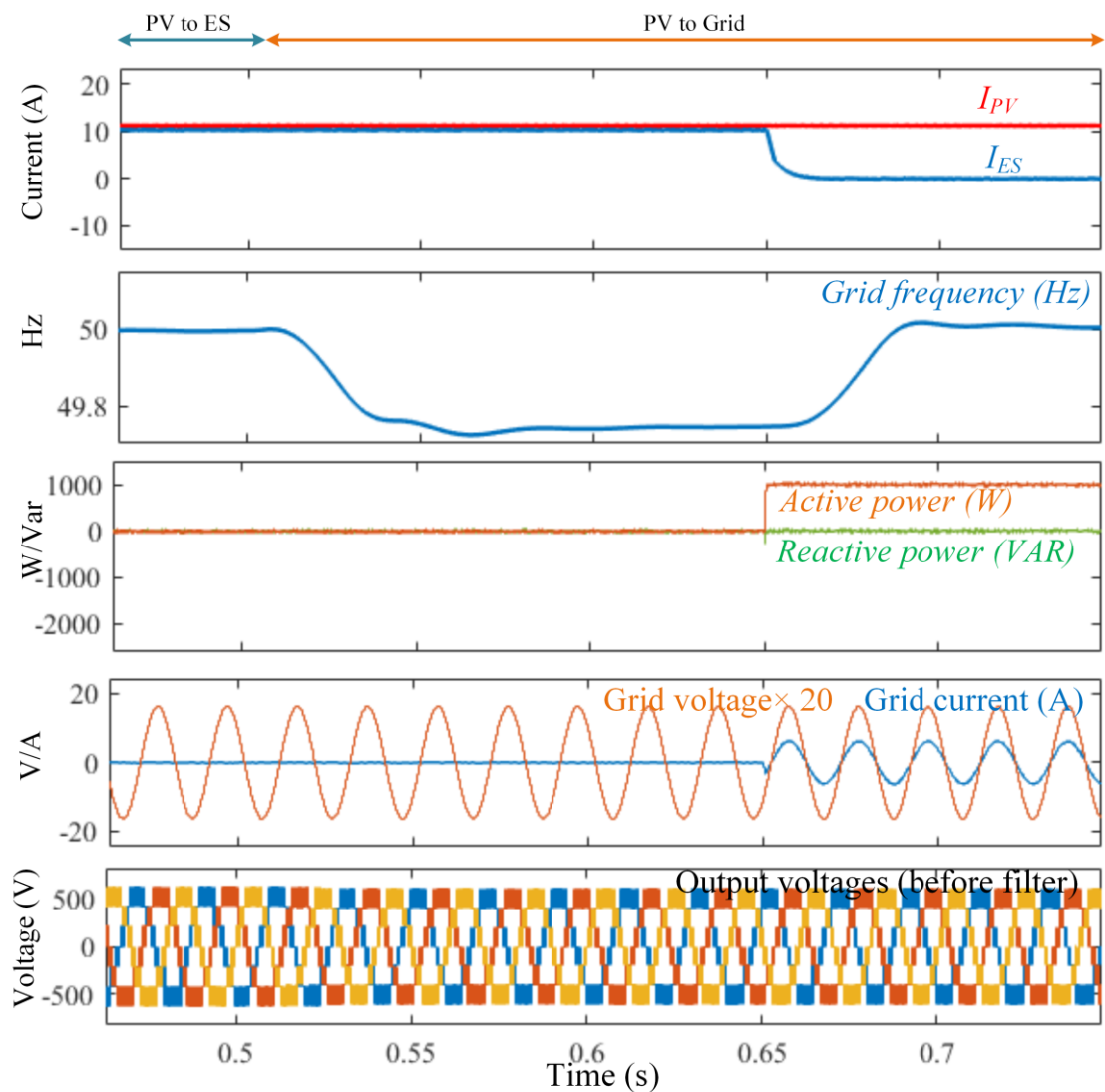
Fig. 2.7 Principle of operation of the proposed CMBMC employed to interface PV and ES into the grid.

In this mode, the proposed algorithm calculates the charging current and charges the ES to store the PV available power. The PV current and the charging current are shown in the first trace of the figure. At 0.5 s, 1 kW active power load is connected in the grid and the active power reference value of the converter is still kept to 0 kW. It can be observed that the grid frequency is dropped to around 49.7 Hz. At 0.65 s, the desired active power reference is set to 1 kW. As shown, the ES charging current is restored to zero to provide the required power into the grid. It can also be observed that the grid frequency is returned to the nominal value.
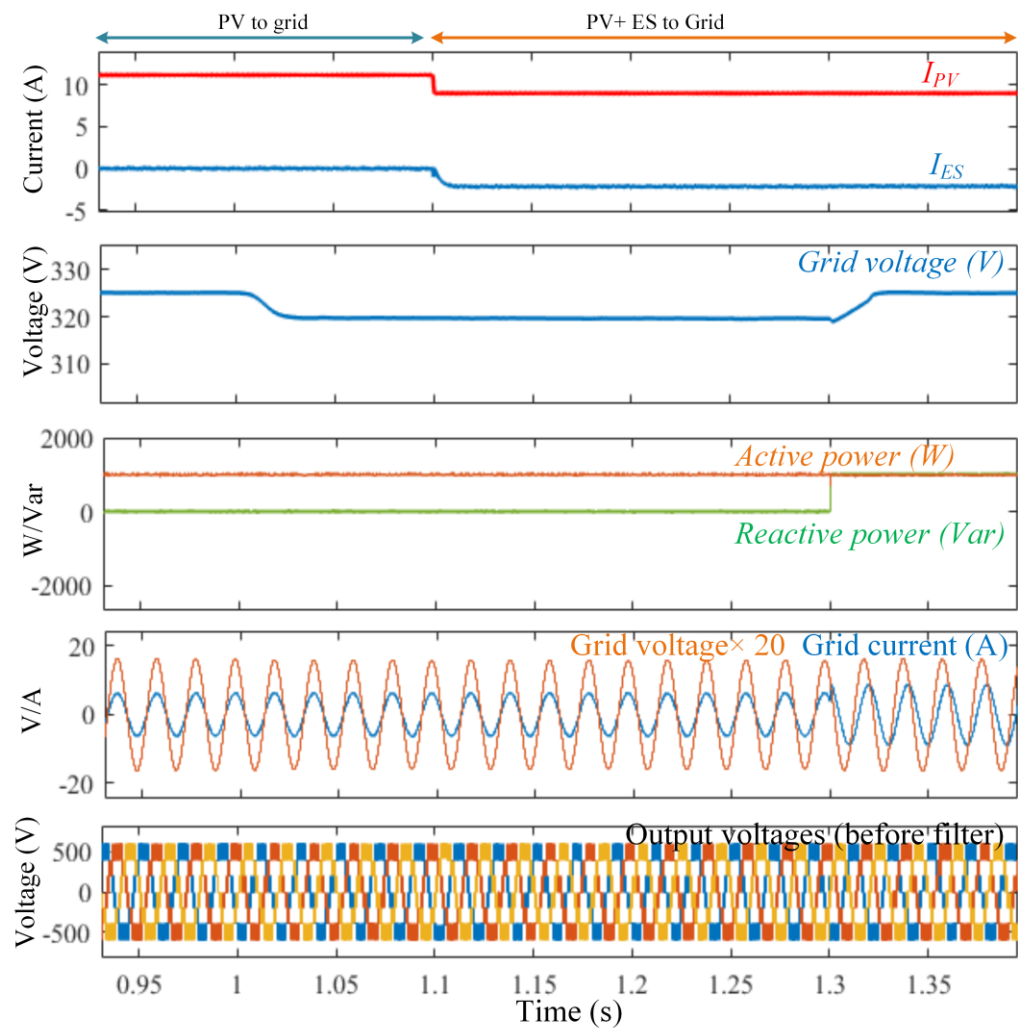
Fig. 2.8 Principle of operation of the proposed CMBMC employed to interface PV and ES into the grid.

Fig. 2.8 presents an operation of the circuit considering the PV to ES, and PV to grid operation modes, where the injected reactive power is varied from 0 to 1 kVar. During the first time interval (0.0.93 s to 1.1 s), the PV available power is set to 1 kW, and the desired active power and reactive power to be injected into the grid are set to 1 kW, and 0 kVar, respectively. The grid is operated in normal operation mode, and the observed grid voltage is of nominal value, as shown in the second trace of Fig. 2.8. At 1.0 s, 1 kVar reactive power load is connected in the grid, and the reactive power reference value of the converter is still kept to 0 kVar. It can be observed that the grid voltage is dropped to around 320 V. At 1.3 s, the desired reactive power reference is set to 1 kVar. As shown, the observed grid voltage is returned to the nominal value. At 1.1 s, the PV available power is decreased. In order to inject the demanded active power, the ES will provide the rest of the power. In this mode, the proposed algorithm calculates the discharging current and discharges the ES to inject the demanded power into the grid. The PV current and the ES discharging current waveforms are shown in the first trace of the figure.

2.5 Experimental Results

A prototype of the proposed converter structure designed for single-phase seven-level operation is built and tested to verify the performance. The derived predictive algorithm is programmed in a DSP chip (TMS320F28379). A multi-winding transformer core made by using nanocrystalline vitroperm alloys is used as the common magnetic bus because of its unique combination of properties. A 60 V DC source is used as the input source. However, multiple DC sources can be integrated with the proposed architecture. In the multi-winding transformer, one primary winding with 20 turns is used as the primary, which is connected to the input DC source through a full-bridge inverter, and three windings are used as the secondary with the same number of turns. The output ports of the three AC/DC modules are connected in series to add up the DC voltages to 180 V to generate the highest voltage level. The experimental result is shown in Fig. 2.9. As it can be seen that, the proposed structure generates distinct seven levels at the output of the converter, and balanced voltages are observed across the DC-link capacitors with the proposed control scheme, as shown in Fig. 2.10. It can be concluded that the proposed structure reduces the control complexity due to the

self-balanced capacitor voltages, and thus eliminates the weighting factors and necessary tuning in the cost function formulation.
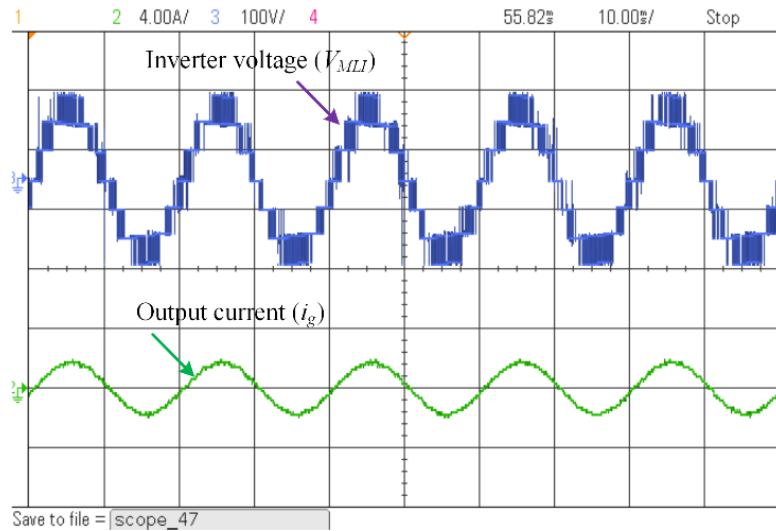
Fig. 2.9 Measured waveform showing output voltage levels and current.
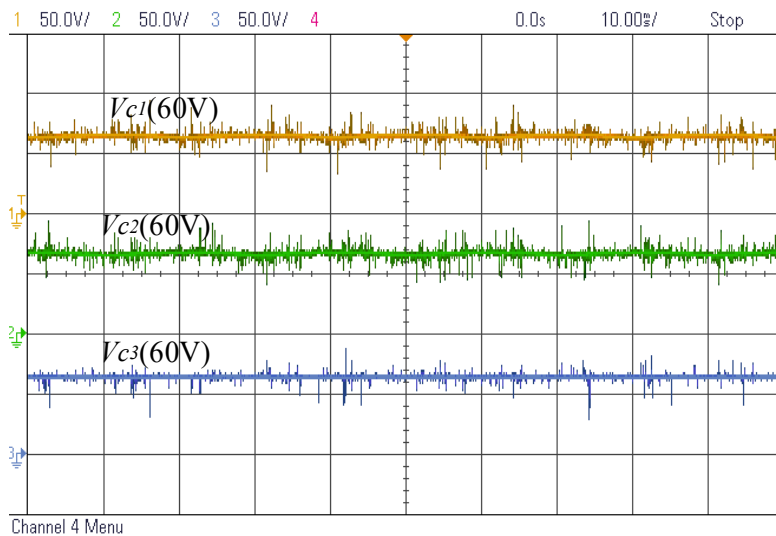
Fig. 2.10 Measured waveform showing output voltage levels and current.

To demonstrate the transient performance of the proposed controller, a step change in the reference current is introduced. The obtained results are shown in Fig. 2.11. As it can be seen that the output current of the converter follows the reference current, and the transient has lasted less than 10 ms. The primary excitation voltage and current waveforms of the MWT (winding 1) are shown in Fig. 2.12(a), and the corresponding induced voltage and

current waveforms in the output ports (windings 2, 3, and 4) of the MWT are shown in Fig. 2.12(b)-(d), respectively.
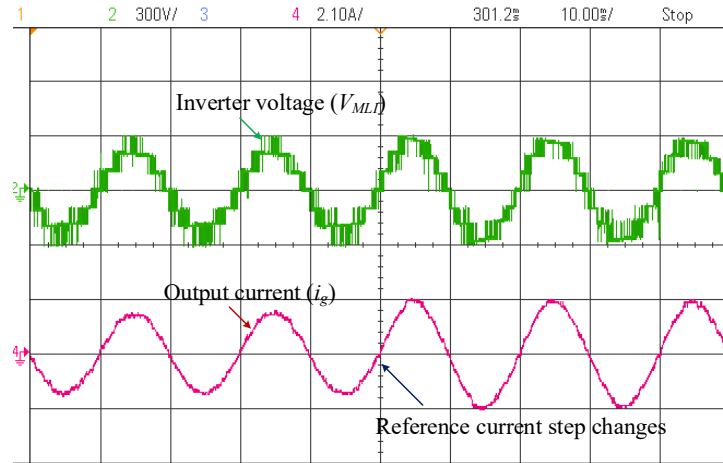
Fig. 2.11. Experimental results during reference grid current transient case.
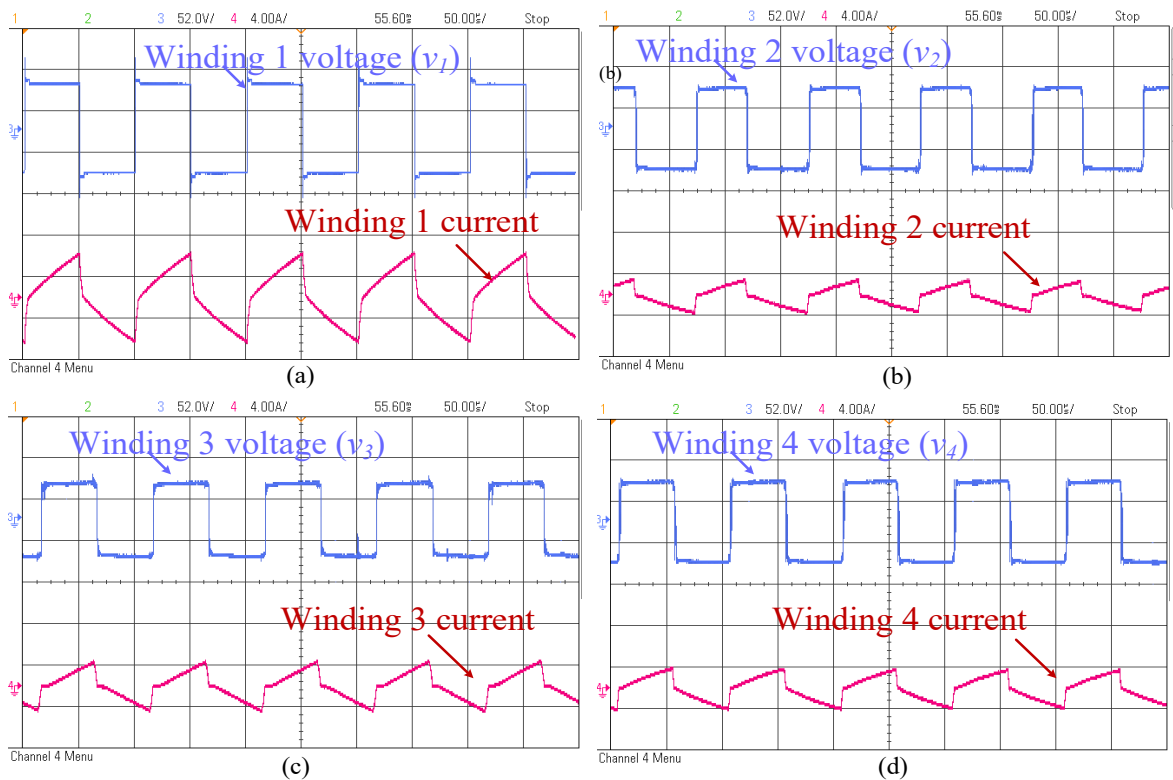
Fig. 2.12 Experimental waveforms of the magnetic link, (a) winding 1 excitation voltage and current waveforms, (b) winding 2 induced voltage and current waveforms, (c) winding 3 induced voltage and current waveforms, and (d) winding 4 induced voltage and current waveforms.

2.6 Conclusion

The major works of this chapter is summarized below.

- A common magnetic-bus based multilevel converter structure and associated control scheme have been presented, which can integrate multiple energy sources and energy storages with reduced power conversion stages.
- A control algorithm has been derived to stabilize the bus voltage for ensuring the maximum power extraction from the PV panels.
- The proposed structure can generate multilevel output voltage with reduced control complexity due to inherent voltage balancing capability in the series-connected capacitors in the DC-side of the inverter.
- It can generate the desired active and reactive power (leading/lagging power factor) reference values.

A common magnetic-bus based multilevel converter architecture was presented in this chapter, which is suitable for residential/industrial applications. This structure can integrate multiple energy sources and storages with reduced power conversion stage. This structure also ensures magnetic isolation, which is required for grid-connected PV application. A control algorithm was developed to stabilize the bus voltage while extracting the maximum energy from the PV source. The magnetic-link based structure generates balanced voltages across the series-connected capacitors in the DC-side of the multilevel converter. As a result, it reduces the control complexity of the multilevel inverter. A predictive control algorithm was also derived to generate the desired active and reactive power. It is capable of generating both lagging and leading power factor. Thus, this converter can be used to support the grid voltage. A single-phase version of this topology was also built and tested.

3 Model Predictive Observer Based Control Scheme for Five-level Converters in Microgrid Applications

3.1 Introduction

Single-phase two-level AC/DC power converters are widely used in residential and low-power industrial applications. Contrary to the conventional two-level power converters, multilevel converters (MCs) present more advantages, including the higher quality of output waveforms, higher voltage-handling capability using medium-voltage switching devices, higher power density, and lower switching losses [45-49]. Single-phase MCs have gained popularity in the recent years due to their emerging applications, such as energy storage systems (ESSs), active power filters (APFs), vehicle-to-grid (V2G), grid-to-vehicle (G2V), uninterruptible power supplies (UPSs), and renewable energy conversion systems (RECSs). Consequently, various topologies and control methods have been proposed over the years with a pertinent focus on maintaining high power quality, improving the system dynamic performance and robustness. Regarding the control of single-phase grid-connected multilevel AC/DC converters, the important control objectives are the reference grid current tracking with the lowest total harmonic distortion (THD), DC-link voltage regulation, and supply of a desired reactive power [8, 50]. The DC-link plays a significant role in the power flow between the utility grid side and the DC-side. Thus, the important control objective is to self-support the DC-link voltage due to the external disturbances and system parameter changes, while preserving the desired reactive power.

The available literature shows that numerous methods have been extensively studied to accomplish these control objectives, including the most conventional voltage oriented control (VOC) methods [6, 51-54]. The dynamic performances of these control methods depend on the tuning of proportional-integral (PI) parameters. The other commonly used techniques are hysteresis controller, *dq*-axis current controller, and proportional resonant (PR) current controller [19, 43, 55-57]. The dynamic performances of these methods are related to the

tuning of PI parameters. Since the AC/DC converters are highly non-linear, the controllers require the system parameters information during the different operating conditions. As the PI coefficients are required to be tuned during the different operation points, these control strategies cannot achieve the required control objectives under external disturbances [58].

Different from the conventional controllers, a widely used strategy is the direct power control (DPC) method [59-62]. This method uses hysteresis comparators and power switching lookup tables. Compared with the traditional control methods, the DPC can realize improved dynamic performances and robustness to achieve DC-link voltage regulation, and has been extensively applied in three-phase systems [63]. However, constructing an accurate power switching lookup table is difficult, and hence, may produce high power ripples. As a result, this method affects the steady state performance of the system [64], which limits its application. Recently, several advanced control methods have been proposed to improve the control performance of the DPC, which include model predictive DPC [65-76], deadbeat DPC [77], and fuzzy logic based DPC [78, 79]. Compared with the direct power and current control methods, predictive control methods provide faster demand tracking speed and generate lower power ripples [68, 69]. MPC based method has been extensively studied in recent years due to its simplicity, free of modulation, flexibility, and options to include nonlinearities and system constraints. However, in a conventional predictive control method, the outer DC-link voltage control is generally governed by a PI controller to generate the active and reactive power reference for the inner MPC-based power control loop. Consequently, the system performance still suffers in the presence of external disturbances due to the use of PI-based DC-link voltage controller. Recently, many nonlinear control approaches have been suggested for controlling three-phase AC/DC power converters, including sliding-mode control (SMC) [56, 80], nonlinear adaptive control [81], and passivity-based control [82]. To the best knowledge of the authors, these methods have been used as the inner current controller, and PI-controller has been used as the DC-link voltage controller. As a consequence, the control performance still suffers because of the uncertainties of external disturbances and system parameter variations. Therefore, it is much desired to design a reliable and robust control strategy to rapidly regulate the DC-link voltage to the required value in the presence of disturbances, which is crucial for grid-connected AC/DC power

converters. The available literature shows that the recent control concepts have been applied to the three-phase AC/DC power converter applications. However, to the best of authors' knowledge, these controllers' implementation has not been validated for single-phase multilevel converter applications.

The focus of this work is the design, implementation, and evaluation of a robust control scheme for the five-level asymmetrical T-type (5L-T-AHB) AC/DC converter. The 5L-T-AHB converter topology has been proposed in [83, 84], where a new modulation strategy has been proposed to operate as a transformerless grid-connected inverter. Furthermore, a finite control set model predictive control (FCS-MPC) technique has been applied to operate this converter as an active rectifier [85]. This architecture suffers in terms of capacitor voltage unbalancing problem in the DC-link. Moreover, its applicability to realize reactive power compensation and DC-link voltage regulation under external disturbances has not been demonstrated. In this chapter, an FCS-MPC with a disturbance observer based control technique is proposed to provide a high degree of disturbance rejection capability and robustness against the external disturbances to this converter. Moreover, the capacitor voltage balancing technique and reactive power compensation capability are also included in the proposed cost function formulation. In this scheme, an FCS-MPC is employed as the inner current tracking controller, and a PI controller combined with an ESO based disturbance observer is employed as the outer voltage control loop. This voltage control loop generates the active power reference for the inner FCS-MPC based current tracking controller.

The major novelty of this approach is the PI-ESO based controller design to reject external disturbances and realize a high performance to regulate the DC-link voltage. In this study, the DC-link load resistance of the converter, which influences the dynamics of the system, is considered as the external disturbance. Theoretical analysis is also provided to present the closed-loop behavior of the proposed control scheme. Moreover, an FCS-MPC algorithm is derived to track the required current reference, while maintaining balanced voltages in the series connected capacitors and achieving a desired reactive power value.

3.2 System Configuration and Mathematical Model

3.2.1 Dynamic model of 5L-T-AHB converter

The circuit configuration of the employed 5L-T-AHB converter is shown in Fig. 3.1. Based on the circuit configuration, this converter should be controlled to generate five distinct voltage levels in the AC-side to reduce the harmonic content of the grid current with less dv/dt stressing in the semiconductor devices. The following assumptions are made: a) neglecting both conduction and switching losses, b) capacitances C_1 and C_2 have equal values ($C_1 = C_2 = 2C$), and $L_1 = L_2, (L = L_1 + L_2)$. Considering a charge balance condition, the continuous-time dynamic model of the converter that defines the dynamical behavior of the converter can be expressed as follows

$$v_g = v_{L_1} + v_{L_2} + v_r + \psi(t)v_{dc} = v_L + v_r + v_c(t) \tag{3.1}$$

$$i_g = i_c + i \tag{3.2}$$

where $v_c(t) = \psi(t)v_{dc}$, v_g is the grid voltage, v_L is the voltage across the filter inductors, v_r is the voltage across the equivalent series resistance of the filter inductors, v_c represents the converter voltage, i_g denotes the grid current, i_c denotes the grid-side capacitor current, and ψ is the control input which takes the values in the finite set from Table 3.1. Substituting (3.2) into (3.1) yields

$$v_g = L\frac{di}{dt} + ri + v_c(t) = L\frac{di_g}{dt} - LC_f\frac{d^2v_g}{dt^2} + v_c(t) + r(i_g - C_f\frac{dv_g}{dt}) \tag{3.3}$$

where L is the grid side filter inductance, and r represents the equivalent series resistance of the filter inductor L. By using the forward Euler approximation method with a sampling period T_S, (3.3) can be rewritten as

$$v_g{}^k = \frac{L}{T_S}\left(i_g{}^{k+1} - i_g{}^k\right) - \frac{LC_f}{T_S^2}\left(v_g{}^{k+1} - 2v_g{}^k + v_g{}^{k-1}\right) + ri_g{}^k - \frac{rC_f}{T_S}\left(v_g{}^{k+1} - v_g{}^k\right) + v_c{}^k \tag{3.4}$$

where k is discretized t.

Rearranging (3.4), in terms of the predicted grid current, $i_g{}^{k+1}$ can be expressed as

$$i_g^{k+1} = \left(1 - \frac{rT_S}{L}\right)i_g^k + \left(\frac{C_f}{T_S} + \frac{rC_f}{L}\right)v_g^{k+1} - \frac{T_S}{L_f}v_c^k + \left(\frac{T_S}{L} - \frac{2C_f}{T_S} - \frac{rC_f}{L}\right)v_g^k + \frac{C_f}{T_S}v_g^{k-1} \quad (3.5)$$

where v_g^{k+1} can be obtained as [86]

$$v_g^{k+1} = 3v_g^k - 3v_g^{k-1} + v_g^{k-2} \quad (3.6)$$

The 5L-T-AHB converter topology consists of a single DC-link in parallel with the series connected capacitors. Therefore, it is required to integrate the voltage balancing technique into the control method to ensure equal capacitor voltages (i.e. $v_{C_1} = v_{C_2} = v_{dc}/2$) to generate five distinct voltage levels in the AC-side. The dynamic equations for the capacitor voltages are expressed as follows:

$$C_1 \frac{dv_{C_1}}{dt} = i_{C_1} = i_{H_1} - i_{dc} = i_{H_1} - \frac{v_{C_1} + v_{C_2}}{R} \quad (3.7)$$

$$C_2 \frac{dv_{C_2}}{dt} = i_{C_2} = i_{H_2} - i_{dc} = i_{H_2} - \frac{v_{C_1} + v_{C_2}}{R} \quad (3.8)$$

where i_{C_1} and i_{C_2} represent the currents through the capacitors C_1 and C_2 respectively, i_{H_1} and i_{H_2} represent the internal currents of the converter, R denotes the equivalent load resistance value, and i_{dc} denotes the DC-side current. According to the MPC requirements, the present values of i_g, v_g, v_{C_1}, and v_{C_2} are required to predict the future behavior of i_g. The capacitor voltages balancing of the employed converter is also a control objective. The predictive values of the capacitor voltages of this converter can be presented in discrete-time form using the classical forward Euler method as follows:

$$v_{C_1}^{k+1} = v_{C_1}^k + \frac{T_S}{C_1}i_{H_1}^k - \frac{T_S}{C_1}i_{dc}^k \quad (3.9)$$

$$v_{C_2}^{k+1} = v_{C_2}^k + \frac{T_S}{C_2}i_{H_2}^k - \frac{T_S}{C_2}i_{dc}^k \quad (3.10)$$

The measured values of i_{H_1} and i_{H_2} can be obtained from the individual switching functions as shown in Table 3.1, and thus unnecessary measurements of i_{H_1} and i_{H_2} can be avoided. Therefore, to predict the future behavior of the grid-current and the capacitor voltage values, (3.5), (3.9), and (3.10) will be used by the proposed controller.
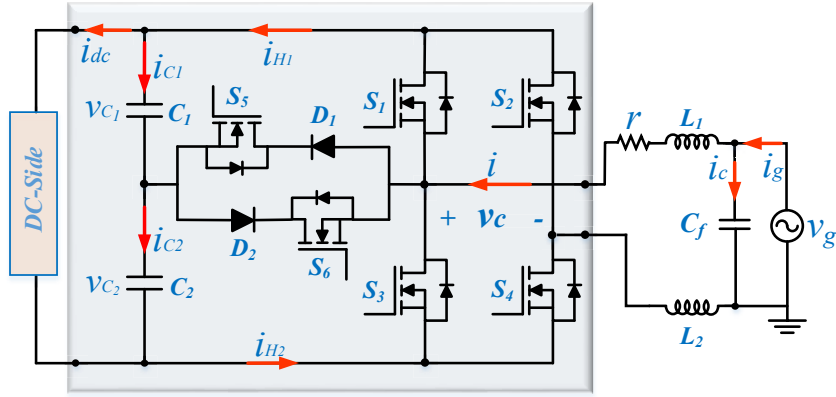
Fig. 3.1 Topology of the 5L-T-AHB converter.

Table 3.1 Possible States of the 5L-T-AHB Converter

	S_1	S_2	S_3	S_4	S_5	S_6	i_{H1}	i_{H2}	ψ	v_c
$v_g>0$	0	0	0	0	0	0	i	i	1	$+v_{DC}$
	0	0	0	0	1	0	0	i	1/2	$+v_{DC}/2$
	0	0	1	0	0	0	0	0	0	0
$v_g<0$	0	0	0	0	0	0	i	i	-1	$-v_{DC}$
	0	0	0	0	0	1	i	0	-1/2	$-v_{DC}/2$
	0	0	0	1	0	0	0	0	0	0

3.2.2 D-Q mathematical model

The grid voltage v_g, the inductor current i, and the converter voltage v_c of the employed converter are defined as follows

$$v_g = v_d \sin(\omega t) + v_q \cos(\omega t) \tag{3.11}$$

$$i = i_d \sin(\omega t) + i_q \cos(\omega t) \tag{3.12}$$

$$v_c = v_{cd} \sin(\omega t) + v_{cq} \cos(\omega t) \tag{3.13}$$

where v_d, i_d and v_{cd} are the *d*-axis components, and v_q, i_q and v_{cq} are the *q*-axis components of the grid voltage, the inductor current, and the converter voltage vectors v_g, i, and v_c respectively in *dq* rotating frame.

The equivalent circuit of the employed converter is shown in Fig. 3.2. The dynamic model of the employed converter in the DC-side is given by

$$C\frac{dv_c}{dt} = i_C = i_s - i_{load} - i_{R_S} = i_s - \frac{v_{dc}}{R_{load}} - \frac{v_{dc}}{R_S} \qquad (3.14)$$

where R_S represents the switching loss of the converter and R_{load} denotes the equivalent load resistance value.

The inductor current i and grid voltage v_g can be decomposed in their d and q parts at the grid frequency. Thus, (3.1) and (3.14) will become

$$L\frac{di_d}{dt} = v_d - i_d r + i_q \omega L - v_{cd} \qquad (3.15)$$

$$L\frac{di_q}{dt} = v_q - i_q r - i_d \omega L - v_{cq} \qquad (3.16)$$

$$C\frac{dv_c}{dt} = i_s - i_{load} - i_{R_S} \qquad (3.17)$$

Considering the system is in the steady state condition, according to the energy conservation law, the input power from the utility grid must be equal to the power consumed by the load, the semiconductor switching losses, and the capacitor charging power. The reference value of the output voltage is v_{dc}. Therefore i_s can be expressed as

$$i_s = \frac{v_d i_d + v_q i_q}{2v_{dc}} \qquad (3.18)$$

From (3.17) and (3.18), we have

$$C\frac{dv_c}{dt} = \frac{v_d i_d + v_q i_q}{2v_{dc}} - \frac{v_{dc}}{R_{load}} - \frac{v_{dc}}{R_S} = \frac{1}{v_{dc}}(p^* - p_{load} - p_{R_S}) \qquad (3.19)$$

where $p_{load} = \frac{v_{dc}^2}{R_{load}}$, $p^* = \frac{1}{2}(v_d i_d + v_q i_q) = v_{dc} i_s$, and $p_{R_S} = \frac{v_{dc}^2}{R_S}$.

By using (3.16), (3.17), and (3.19), the state-space model of the system can be expressed as follows

$$
\begin{bmatrix} \dot{i}_d \\ \dot{i}_q \\ \dot{v}_c \end{bmatrix} = \begin{vmatrix} -\dfrac{r}{L} & \omega & 0 \\ -\omega & -\dfrac{r}{L} & 0 \\ \dfrac{v_d}{2v_{dc}C} & \dfrac{v_q}{2v_{dc}C} & -\left(\dfrac{1}{CR_{load}} + \dfrac{1}{CR_S}\right) \end{vmatrix} \begin{bmatrix} i_d \\ i_q \\ v_c \end{bmatrix} + \begin{bmatrix} \dfrac{1}{L} & 0 \\ 0 & \dfrac{1}{L} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_d - v_{cd} \\ v_q - v_{cq} \end{bmatrix} \qquad (3.20)
$$

3.3 Proposed Control Scheme

This section covers the demonstration of the proposed control scheme. The block diagram of the proposed controller is illustrated in Fig. 3.3. The control objectives concerning the single-phase 5L-T-AHB converter are to regulate the DC-link voltage and provide the desired reactive power. The DC-link voltage of the power converter is determined by the active power. Therefore, in the dq rotating frame, the d-axis component (i_d^*) of the current i is computed dynamically to maintain the desired output voltage. Similarly, the instantaneous reactive power is determined by the q-axis component (i_q^*) of the current i. Hence, the converter currents (d-axis component (i_d) and q-axis component (i_q)) should follow the dynamically calculated references i_d^* and i_q^* respectively to realize the desired control objectives.
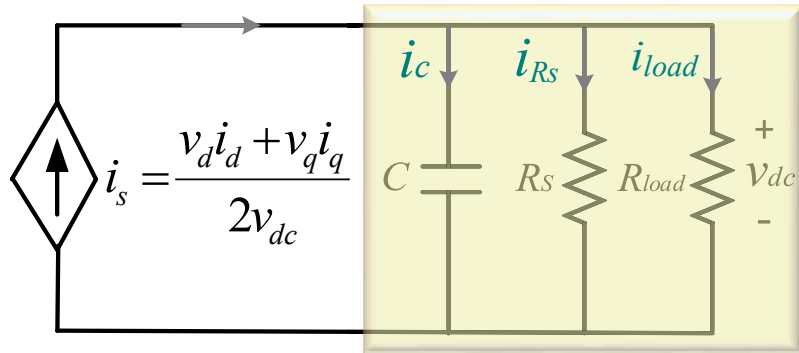
Fig. 3.2 Equivalent circuit of the 5L-T-AHB converter.
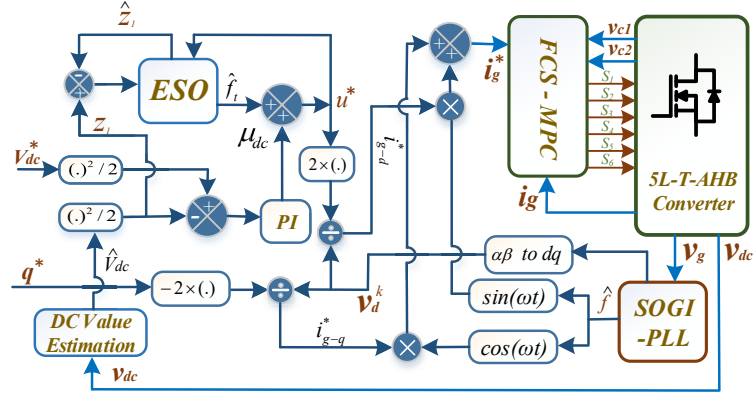
Fig. 3.3 Block diagram of the proposed ESO-based AC/DC converter control system.

Note that the DC-link voltage of the AC/DC converters is affected by the external load disturbances. To achieve the dynamic voltage regulation in the presence of active power disturbances, this work has adopted an ESO-based disturbance observer, which dynamically modifies the active power reference for the MPC-based inner current control loop. For the employed converter, the MPC with finite control set (FCS-MPC) is used to define the state of this converter in each sampling period. The FCS-MPC offers several advantages, including the possibility to realize multiple control objectives, handling system constraints and the option to include nonlinearities.

3.3.1 FCS-MPC for 5L-T-AHB power converter

The FCS-MPC algorithm has been derived for current control in 5L-T-AHB converter drives. The objectives of the controller are to track the current reference (i_g^*), and to balance the series connected capacitor voltages. The current i_g^* is calculated from the active power dynamic reference (u^*) obtained from PI-ESO controller and the desired reactive power (q^*) values. To accomplish this purpose, the FCS-MPC scheme operates in discrete time and uses the discrete model of the converter which is presented in Section II. The measured system states are used for the state predictions of the control variables for the employed converter model. The state predictions are then evaluated for each of the possible switching states to provide the best performance. It is based on an optimization criterion and uses a cost function

which is explained in the following section. Among these switching states, the one which minimizes the cost function is applied to drive the employed converter.

3.3.2 Multi-objective cost function formulation

In the conventional MPC algorithm to control the single-phase two level converters, the predicted values of the grid current reference at the instant $(k+1)$ is calculated at each sampling instant by using (3.5) for each of the possible switching states. Among these switching states, the one which minimizes the cost function defined in (3.21) is selected and then applied to the power converter till the next sampling instant.

$$g_{conv.} = \left| i_g^{*\,k+1} - i_g^{\,k+1} \right| \tag{3.21}$$

Only the grid-current variable is usually taken into account in the cost function defined in (3.21) to generate different voltage levels. Thus, the weighting factor selection and tuning process are not necessary. However, for the employed multilevel converter, the multilevel voltage synthesizing will be affected by this strategy due to voltage unbalancing problem that occurs in the series connected capacitors. Therefore, for this particular multilevel power converter, it is important to maintain balanced voltage across the series connected capacitors to generate five distinct voltage levels in the AC-side. The proposed cost function for the adopted 5L-T-AHB converter is defined as

$$g_{conv.} = \lambda_i \left(i_g^{*\,k+1} - i_g^{\,k+1} \right)^2 + \lambda_v \left(v_{C_1}^{\,k+1} - v_{C_2}^{\,k+1} \right)^2 \tag{3.22}$$

The trade-off between the capacitor voltage balancing and the grid-current waveform quality can be realized by adjusting the weighting factors λ_i and λ_v in (3.22). It can be observed that a large value of λ_v will take sides in the capacitor voltage balancing by paying the penalty of low THD of the line current, i.e., the line current THD will be affected by the capacitor voltage balancing. In this work, the weighting factors are formulated as follows

$$\lambda_v = \frac{p^*}{V_{dc}^2} \tag{3.23}$$

$$\lambda_i = 1 \tag{3.24}$$

where p^* is the active power reference calculated from the PI-ESO controller.

In (3.22), the grid-current reference i_g^{*k+1} computation is important to realize the required control objectives, which is explained in the following section.

3.3.3 Reference grid current calculation

In a single-phase system, a virtual two-phase system is usually generated to calculate the instantaneous active and reactive power. The second-order generalized integrator (SOGI) is a widely employed method to generate the orthogonal signal of the single-phase voltage and current signals. The transfer functions of SOGI in s-domain are expressed as follows

$$x_\alpha(s) = \frac{k\omega s}{s^2 + k\omega s + \omega^2} x(s) \tag{3.25}$$

$$x_\beta(s) = \frac{k\omega^2}{s^2 + k\omega s + \omega^2} x(s) \tag{3.26}$$

where k represents the damping factor.

The performance of SOGI is related to the tunning of parameter k. Applying (3.25) and (3.26) to the grid voltage v_g and the current i_g, the orthogonal component of the voltage v_g and current i_g can be presented as follows

$$v_{g-\alpha} = V_g \sin(\omega t) \tag{3.27}$$

$$v_{g-\beta} = V_g \sin\left(\omega t + \frac{\pi}{2}\right) \tag{3.28}$$

$$i_{g-\alpha} = I_g \sin(\omega t + \phi) \tag{3.29}$$

$$i_{g-\beta} = I_g \sin\left(\omega t + \phi + \frac{\pi}{2}\right) \tag{3.30}$$

According to the instantaneous power theory, the active power p^k and the reactive power q^k of single-phase system are defined as

$$\begin{bmatrix} p^k \\ q^k \end{bmatrix} = \frac{1}{2} \begin{bmatrix} v_{g-\alpha}^k & v_{g-\beta}^k \\ v_{g-\beta}^k & -v_{g-\alpha}^k \end{bmatrix} \begin{bmatrix} i_{g-\alpha}^k \\ i_{g-\beta}^k \end{bmatrix} = \frac{1}{2} \begin{bmatrix} v_{g-d}^k & v_{g-q}^k \\ v_{g-q}^k & -v_{g-d}^k \end{bmatrix} \begin{bmatrix} i_{g-d}^k \\ i_{g-q}^k \end{bmatrix} \tag{3.31}$$

where $v_{g-\alpha}$, $v_{g-\beta}$, $i_{g-\alpha}$, $i_{g-\beta}$, are the α-axis and β-axis components of the grid voltage and the line current in the two-phase $\alpha - \beta$ stationary reference frame, respectively.

v_{g-d}, v_{g-q}, i_{g-d}, and i_{g-q} are the d-axis and q-axis components of the grid voltage and the line current in the dq rotating frame, respectively.

The grid voltage is oriented to d-axis in synchronous reference frame. Thus, the grid-side instantaneous active power p^k and reactive power q^k are given by:

$$p^k = \frac{1}{2} v_{g-d}{}^k i_{g-d}{}^k \tag{3.32}$$

$$q^k = -\frac{1}{2} v_{g-d}{}^k i_{g-q}{}^k \tag{3.33}$$

To calculate the reference grid current, the quantities in rotating reference frame in (3.32) and (3.33) are used. Therefore, the expression for reference grid current is given by [87]

$$i_g{}^k = i_{g-q}{}^k \cos(\theta) + i_{g-d}{}^k \sin(\theta) \tag{3.34}$$

The quantities $sin(\theta)$ and $cos(\theta)$ in (3.34) can be obtained by using phase locked-loop (PLL). In the proposed control scheme, a DC offset rejection capability based PLL [88] has been used. The block diagram of the employed PLL is illustrated in Fig. 3.4. Finally, using (3.32) - (3.34), the grid-current references can be expressed as

$$i_g{}^k = \frac{2p^k}{v_{g-d}{}^k} \sin(\theta) - \frac{2q^k}{v_{g-d}{}^k} \cos(\theta) \tag{3.35}$$

3.3.4 ESO-based disturbance observer design

The proposed control scheme includes an ESO as a disturbance observer in the DC-link voltage control loop. This observer has been used to compensate the total system disturbances f_t to the converter that consists of the external disturbance p_{load} and plant dynamic variation p_{R_S}. Finally, the observed value $\hat{f}_t$ has been used to compensate the control output μ_{dc}. Therefore, the resulted control output $p^* = u$, can be written as

$$u = \mu_{dc} + \hat{f}_t \tag{3.36}$$

where $\hat{f}_t$ is the observed value obtained from the ESO, and μ_{dc} is the PI controller output defined as

$$\mu_{dc}(e_{dc}) = k_p e_{dc} + k_i \int e_{dc} dt \tag{3.37}$$

where the voltage regulation error $e_{dc} = z_1 - z_1^*$ with $z_1 = \frac{(v_{dc})^2}{2}$ and $z_1^* = \frac{(v_{dc}^*)^2}{2}$.

Using (3.19), the dynamic of z_1 can be expressed as

$$C\frac{dz_1}{dt} = (p^* - p_{load} - p_{R_S}) = p^* - f_t \tag{3.38}$$

where $f_{t=}p_{load} + p_{R_S}$.

Using (3.38), we have

$$C\frac{dz_1}{dt} = u - z_2 \tag{3.39}$$

where $p^* = u$ and $f_t(t) = z_2$.

The disturbance z_2 is treated as an extended state, and the time derivative of z_2 is denoted h. Therefore, we have

$$\frac{dz_2}{dt} = h(t) \tag{3.40}$$

Hence, based on the above-mentioned analysis, the state-space model is derived as follows

$$\begin{bmatrix} \dot{z}_1 \\ \dot{z}_2 \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{1}{C} \\ 0 & 0 \end{bmatrix}\begin{bmatrix} z_1 \\ z_2 \end{bmatrix} + \begin{bmatrix} \dfrac{1}{C} \\ 0 \end{bmatrix}u + \begin{bmatrix} 0 \\ 1 \end{bmatrix}h \tag{3.41}$$

Using (3.41), the ESO can be designed as follows

$$\begin{bmatrix} \dot{\hat{z}}_1 \\ \dot{\hat{z}}_2 \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{1}{C} \\ 0 & 0 \end{bmatrix}\begin{bmatrix} \hat{z}_1 \\ \hat{z}_2 \end{bmatrix} + \begin{bmatrix} \dfrac{1}{C} \\ 0 \end{bmatrix}u + \begin{bmatrix} \dfrac{\beta_1}{C} \\ -\beta_2 \end{bmatrix}[z_1 - \hat{z}_1] \tag{3.42}$$

where $\hat{z}_1$ and $\hat{z}_2$ are the estimated values of z_1 and z_2 respectively, β_1 and β_2 are positive gains of ESO.
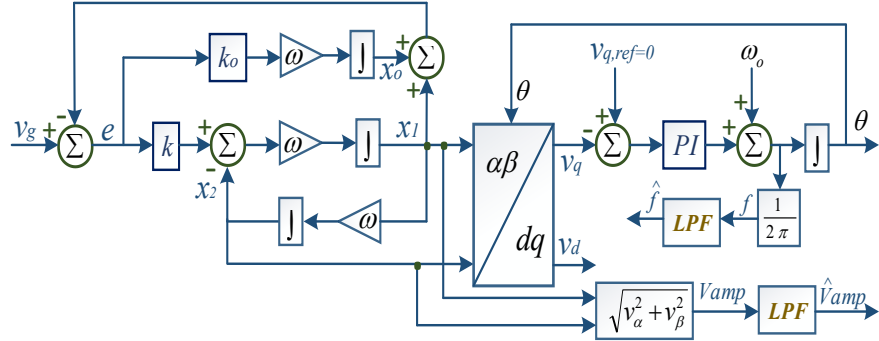
Fig. 3.4 DC- offset rejection based SOGI-PLL.

3.3.5 Parameter tuning and stability analysis

By subtracting (3.42) from (3.41), the error dynamics can be expressed as

$$
\begin{bmatrix} \dot{e}_1 \\ \dot{e}_2 \end{bmatrix} = \underbrace{\begin{bmatrix} -\beta_1/C & -1/C \\ \beta_2 & 0 \end{bmatrix}}_{A} \begin{bmatrix} e_1 \\ e_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} h
\tag{3.43}
$$

where $e_1 = z_1 - \hat{z}_1$ and $e_2 = z_2 - \hat{z}_2$

From (3.43), the gains β_1 and β_2 should be selected such that the roots of the characteristic polynomial of A, i.e., $\lambda(s) = s^2 + \frac{\beta_1}{C}s + \frac{\beta_2}{C}$ are in the left half-plane for Hurwitz stable.

Based on (3.38), we have

$$
C\frac{dz_1}{dt} = p^* - p_{load} - \frac{2z_1}{R_S}
\tag{3.44}
$$

Using Laplace transformation, (3.44) can be expressed as

$$
z_1(s) = \frac{R_S}{R_S Cs + 2} p^*(s) - \frac{R_S}{R_S Cs + 2} p_{load}(s)
\tag{3.45}
$$

After mathematical simplifications, the ESO can be expressed as follows

$$
\begin{bmatrix} \dot{\hat{z}}_1 \\ \dot{\hat{z}}_2 \end{bmatrix} = \begin{bmatrix} -\beta_1/C & -1/C \\ \beta_2 & 0 \end{bmatrix} \begin{bmatrix} \hat{z}_1 \\ \hat{z}_2 \end{bmatrix} + \begin{bmatrix} 1/C & \beta_1/C \\ 0 & -\beta_2 \end{bmatrix} \begin{bmatrix} u \\ z_1 \end{bmatrix}
\tag{3.46}
$$
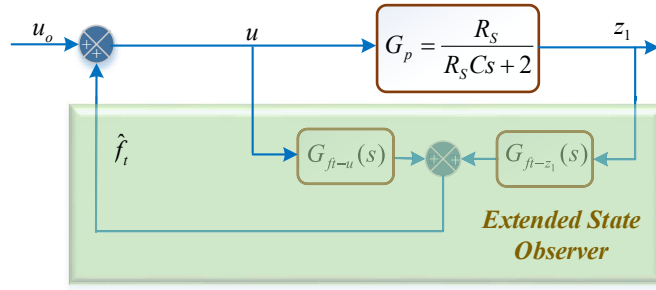
Fig. 3.5 Equivalent transfer function of extended state observer.

Based on Fig. 3.5 and (3.46), the expressions for G_{ft-u} and G_{ft-z_1} are given as follows

$$G_{f_t-u} = \frac{f_t(s)}{u(s)} = \frac{\beta_2}{Cs^2 + \beta_1 s + \beta_2} \tag{3.47}$$

$$G_{f_t-z_1} = \frac{f_t(s)}{z_1(s)} = \frac{-\beta_2 Cs}{Cs^2 + \beta_1 s + \beta_2} \tag{3.48}$$

Using (3.47) and (3.48), the transfer function of the observer can be expressed as follows

$$\hat{f}_t(s) = \frac{\beta_2}{Cs^2 + \beta_1 s + \beta_2} u(s) - \frac{\beta_2 Cs}{Cs^2 + \beta_1 s + \beta_2} z_1(s) \tag{3.49}$$

The revised model from the controller output u_o to the $z_1(s)$ is given as follows:

$$\overline{G}_p(s) = \frac{z_1(s)}{u_o(s)} = \frac{G_p}{1 - G_u - G_{Z_1} G_p} = \frac{R_S}{(CsR_S + 2)} \times \frac{1}{\left(\left(\frac{\beta_2 CsR_S}{(CsR_S + 2)(Cs^2 + \beta_1 s + \beta_2)}\right) - \left(\frac{\beta_2}{(Cs^2 + \beta_1 s + \beta_2)}\right) + 1\right)}$$

$$\tag{3.50}$$

where $G_p = \dfrac{R_S}{R_S Cs + 2}$ and u is the output of the controller.

The adopted controller performance and stability of the system are affected by the DC-side capacitance variations. To evaluate the robustness of the system, the closed loop poles of $\overline{G_P}$ have been studied for the DC-link capacitance variations from 0.002 F to 0.004 F. The root loci of the system model $\overline{G_P}$ for this capacitance variation are illustrated in Fig. 3.6. According to the figure, it is observed that the pole moves in the direction of the imaginary axis as the capacitances vary from 0.002 F to 0.004 F. As a result, the system becomes oscillatory with a reduced damping when the capacitance increases. However, the system

presents robustness against the capacitance variations, because the pole location is still far away from the imaginary axis.
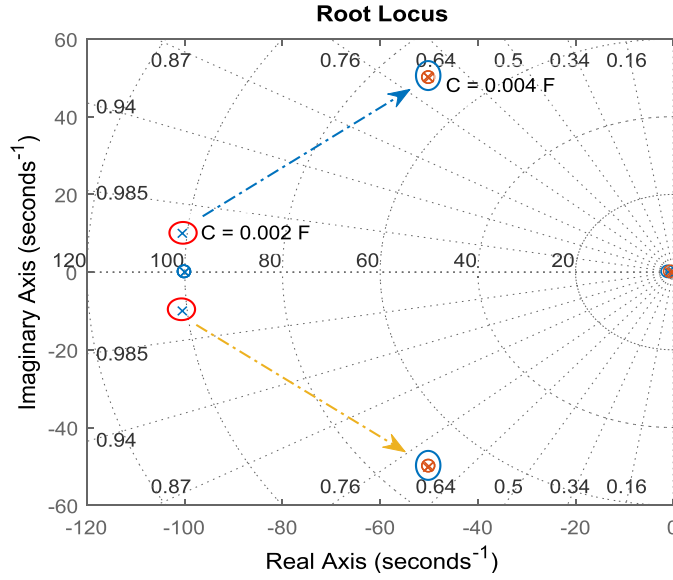
Fig. 3.6 Root loci of the proposed system for the change of capacitance value.

3.3.6 ANF based DC value estimation of the DC-link voltage

In a single-phase system, the instantaneous grid voltage and current are given by:

$$v_g(t) = V_g \sin(\omega t) \tag{3.51}$$

$$i_g(t) = I_g \sin(\omega t + \phi) \tag{3.52}$$

Therefore, the instantaneous power can be expressed as [89]

$$p_{g,inst} = \frac{1}{2}V_g I_g \cos(\phi) - \frac{1}{2}V_g I_g \cos(\phi)\cos(2\omega t) + \frac{1}{2}V_g I_g \sin(\phi)\sin(2\omega t)$$

$$= P - P\cos(2\omega t) + Q\sin(2\omega t) \tag{3.53}$$

where $P = \frac{1}{2}V_g I_g \cos(\phi)$, and $Q = \frac{1}{2}V_g I_g \sin(\phi)$.

The proposed control scheme feeds back the DC-link voltage signal to the controller. As the single-phase AC/DC converter has the double harmonic pulsating power ripple, the output voltage will have an intrinsic double line frequency AC ripple component superimposed on top of the DC-link. Therefore, the DC-bus voltage can be described as

$$v_{bus} = V_{dc} + V_{ripple}\sin(2\omega t) \tag{3.54}$$

In (3.54), the low frequency ripple signal propagates into the closed-loop control system. Therefore, it causes challenge to estimate the active power reference to track the reference DC-link voltage, which degrades the system dynamic performances and increases the current harmonics as well. Conventionally, a low-pass filter (LPF) is employed to filter out this ripple term. A very low cutoff frequency should be selected during the LPF design procedure to suppress the double-frequency ripple term completely, which causes a high phase delay in the control loop and hence, slows down the transient response. Therefore, extracting the DC value of the DC-link voltage signal with a low-frequency ripple component is challenging. In this work, ANF is employed to estimate the DC-value and provide better dynamic performance. The characteristic equations of the employed ANF are given as follows [90]

$$\ddot{x} + \theta^2 x = 2\zeta\theta(y(t) - \dot{x}) \tag{3.55}$$

$$\dot{\theta} = -\gamma x\theta(y(t) - \dot{x}) \tag{3.56}$$

$$\gamma = \frac{\varepsilon}{(A^2 + 1)(\theta^2\mu + 1)} \tag{3.57}$$

where $y(t)$ represents the input signal, θ denotes the estimated second harmonic frequency, γ denotes the adaptation gain parameter, ζ represents the depth of the notch and γ represents the adaptation speed, μ and ε are variable positive parameters, and A denotes amplitude of the signal. For a single sinusoid input signal ($n = 1$), the ANF has a unique periodic orbit located at

$$o = \begin{pmatrix} x \\ \dot{x} \\ \theta \end{pmatrix} = \begin{pmatrix} -\dfrac{A_1}{\omega_1}\cos(\omega_1 t + \varphi_1) \\ A\sin(\omega_1 t + \varphi_1) \\ \omega_1 \end{pmatrix} \tag{3.58}$$

Simulation studies have been conducted to evaluate the DC-value tracking performance of the employed ANF. As shown in Fig. 3.7, clearly, the employed ANF can accurately estimate the DC-value, and it shows fast transient performance in estimating the DC-value during any change in the DC-link voltage.

3.4 Experimental Results

This section presents the experimental results obtained by using the proposed control scheme. To verify the performance of the proposed control technique, a prototype of the 5L-T-AHB converter was built and tested with the specifications listed in Table 3.2. The experimental setup is shown in Fig. 3.8. The control algorithm is programmed in TMS320F28379D. The time required by the different control tasks of the proposed algorithm is presented in Table 3.3, which was measured by using the feature existing in the Code Composer Studio from Texas Instruments. A timer is programmed to acquire the voltage and current sensors data with a sampling frequency of 50 kHz. The experimental waveforms of the converter are illustrated in Fig. 3.9. As it can be seen that the maximum switching frequency of the converter is 25 kHz with the derived FCS-MPC control algorithm.

The performance of the proposed control technique was evaluated under the different scenarios, including (a) capacitor voltages balancing performance, b) voltage tracking performance under reference DC-link voltage step changes, (c) under external load step changes, and (d) reactive power compensation capability.

To provide a base for comparison, the performance of the proposed PI-ESO based control method is also compared with the traditional PI-based control method, where the PI parameters and the inner current control parameters are the same as used in the proposed method. For the traditional PI-based method, the PI control parameters are adjusted through trial and error method to achieve better performance in terms of the speed of convergence and smaller overshoot. The parameters of the PI controller and ESO are presented in Table 3.4.

To evaluate the capacitor voltage balancing performance of the derived FCS-MPC scheme, the reference DC-link voltage is set to 80 V. Therefore, each capacitor voltage should be divided into 40 V to generate five distinct voltage levels in the AC side. Fig. 3.10 shows the experimental results when the capacitor voltage balancing scheme is ignored in the cost function formulation. In this situation, the upper capacitor voltage level is decreased to around 10 V and the lower capacitor voltage is charged to around 70 V, as time goes by. Consequently, only three voltage levels are observed in the AC side. This is due to insufficient charging time to charge up the upper capacitor. Fig. 3.11 demonstrates the capacitor voltages with the

formulated cost function in the derived FCS-MPC algorithm. Clearly, each capacitor voltage is maintained at Vref/2, and consequently, five distinct voltage levels are observed in the AC-side.
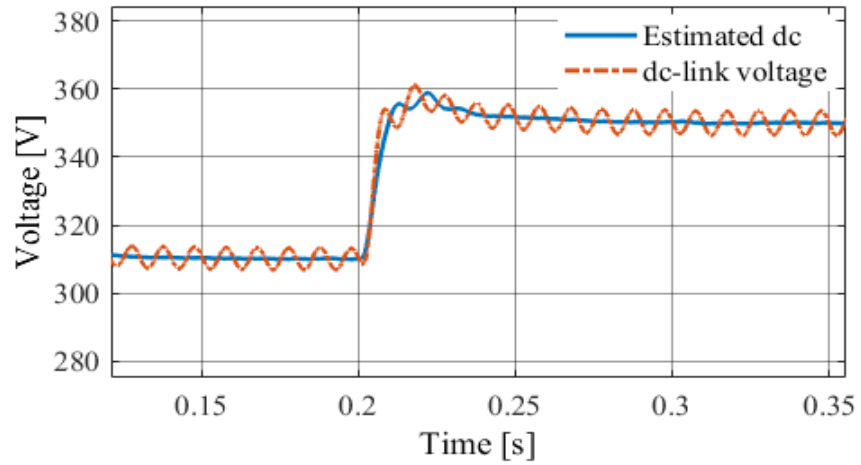
Fig. 3.7 ANF performance in estimating the DC value of the DC-link voltage.
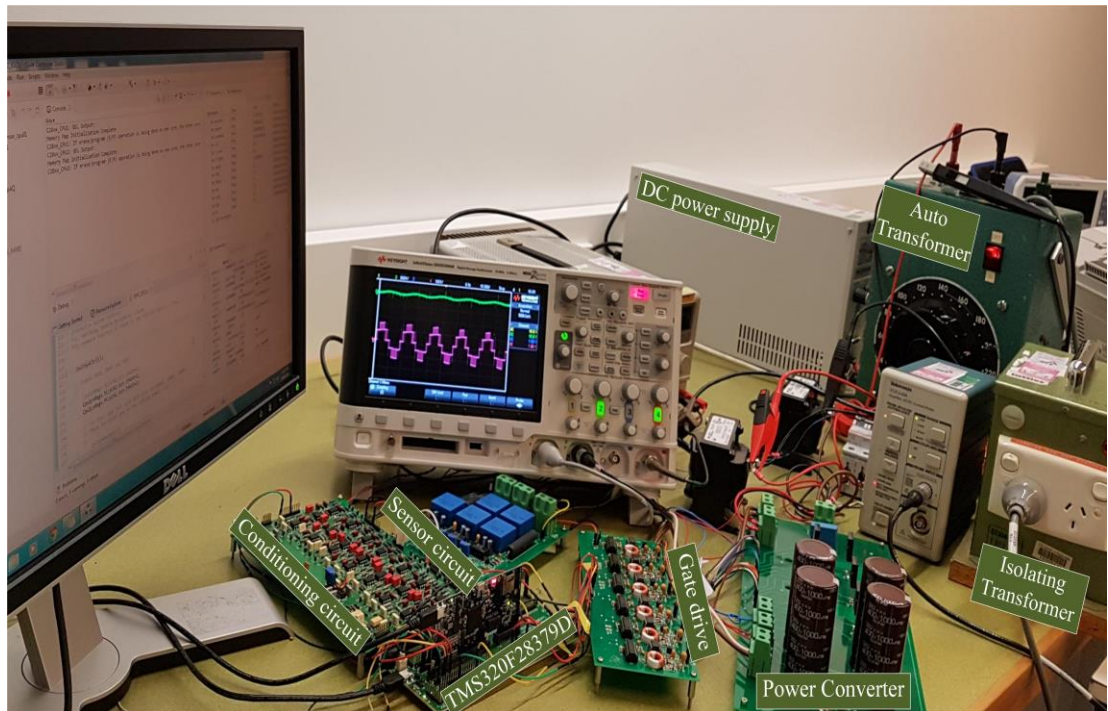
Fig. 3.8 Experimental setup.
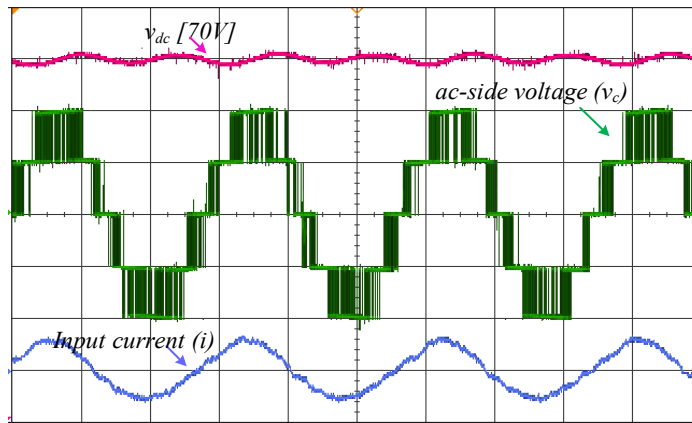
(a)
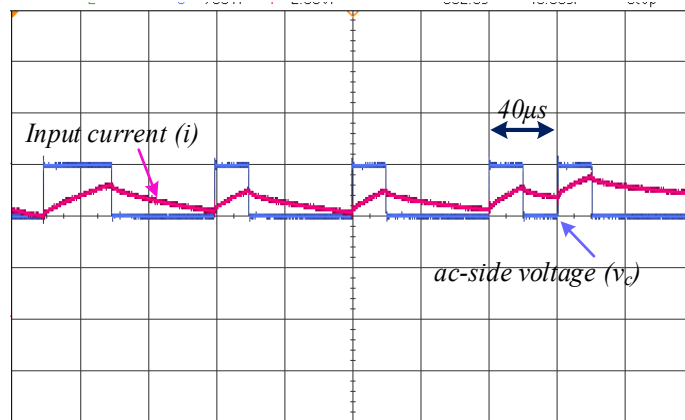
(b)

Fig. 3.9 (a) Experimental results of the voltage produced by the 5L-T-AHB AC/DC converter (vc: 35 V/div), input current (i: 4 A/div), and DC-link voltages (V_{DC}: 10 V/div), (b) magnified view of the voltage and current waveforms.
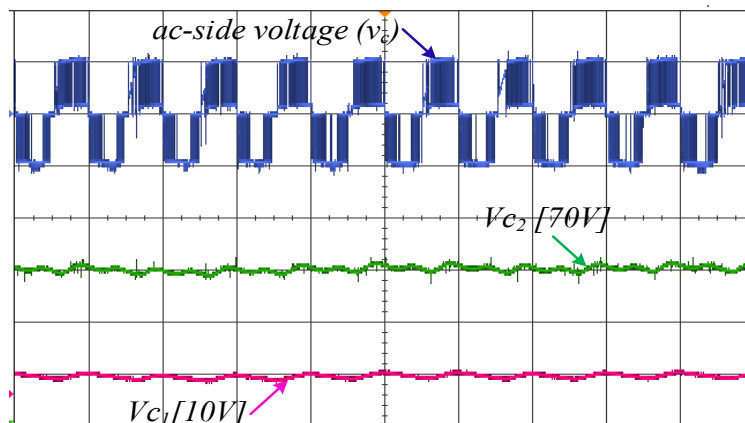
Fig. 3.10 Experimental performances with the general FCS-MPC scheme, and the capacitor voltages unbalancing and its influence on the output voltage levels, (vc: 70 V/div), (vc1,: 20 V/div), (vc2,: 23 V/div).
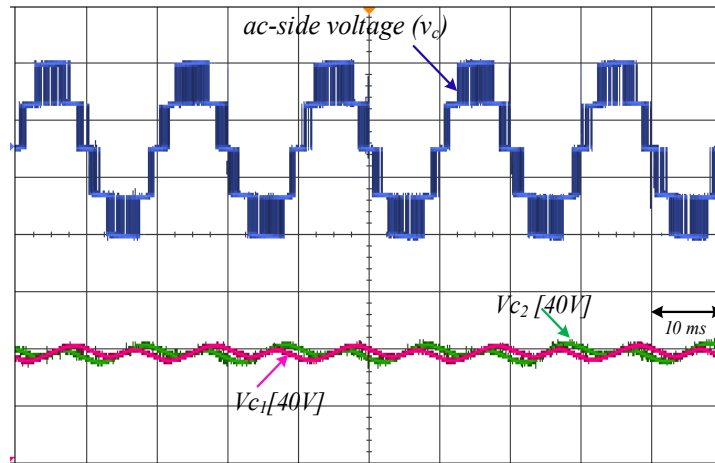
Fig. 3.11 Experimental performances with the proposed FCS-MPC scheme, (vc: 46 V/div), (vc1,: 20 V/div), (vc2,: 20 V/div).

To assess the dynamic performance of the DC-link voltage tracking controller, a step variation in the reference DC-link voltage is introduced from 70 to 80 V, and after that, the reference voltage is changed back to 70 V. The inner current tracking controller (FCS-MPC) remains the same. Figs. 3.12(a) and (b) show the results associated with the PI-ESO and PI methods, respectively for a step change in the reference DC-link voltage from 70 to 80 V. Both controllers can realize the DC-link voltage regulation. Comparing Fig. 3.12(a) with Fig. 3.12(b), a smaller overshoot is observed with the PI-based control method. To evaluate the dynamic behavior of DC-link voltage under external step load change, the DC-link voltage is set to 70 V and a step resistive load changes from 70 Ω to 50 Ω, and after that 50 Ω to 70 Ω is connected to the DC-link. Figs. 3.13(a) and (b) show the results associated with the PI-ESO and PI methods, respectively, for a step resistive load changes from 70 Ω to 50 Ω. Clearly, the proposed PI-ESO demonstrates the best disturbance-rejection performance to regulate the DC-link voltage with the less voltage drop compared to the traditional PI controller, and shows zero steady state error. Whereas for the PI controller, the settling time is roughly double compared to PI-ESO based control scheme, and a steady-state error is also observed for this step load changes. Figs. 3.13(c) and (d) show the results for a step resistive load changes from 50 Ω to 70 Ω with the PI-ESO and PI methods, respectively. It can be observed that the PI-ESO method achieves a better transient response while the PI-based method shows a steady-

state error, which points out that the ESO disturbance observer improves the DC-link voltage control performance. Moreover, the series connected capacitor voltages are kept balanced. Fig. 3.14 shows the experimental results of the proposed controller when the employed converter is realizing the expected reactive power compensation operation while keeping the DC-link voltage to its desired reference value.
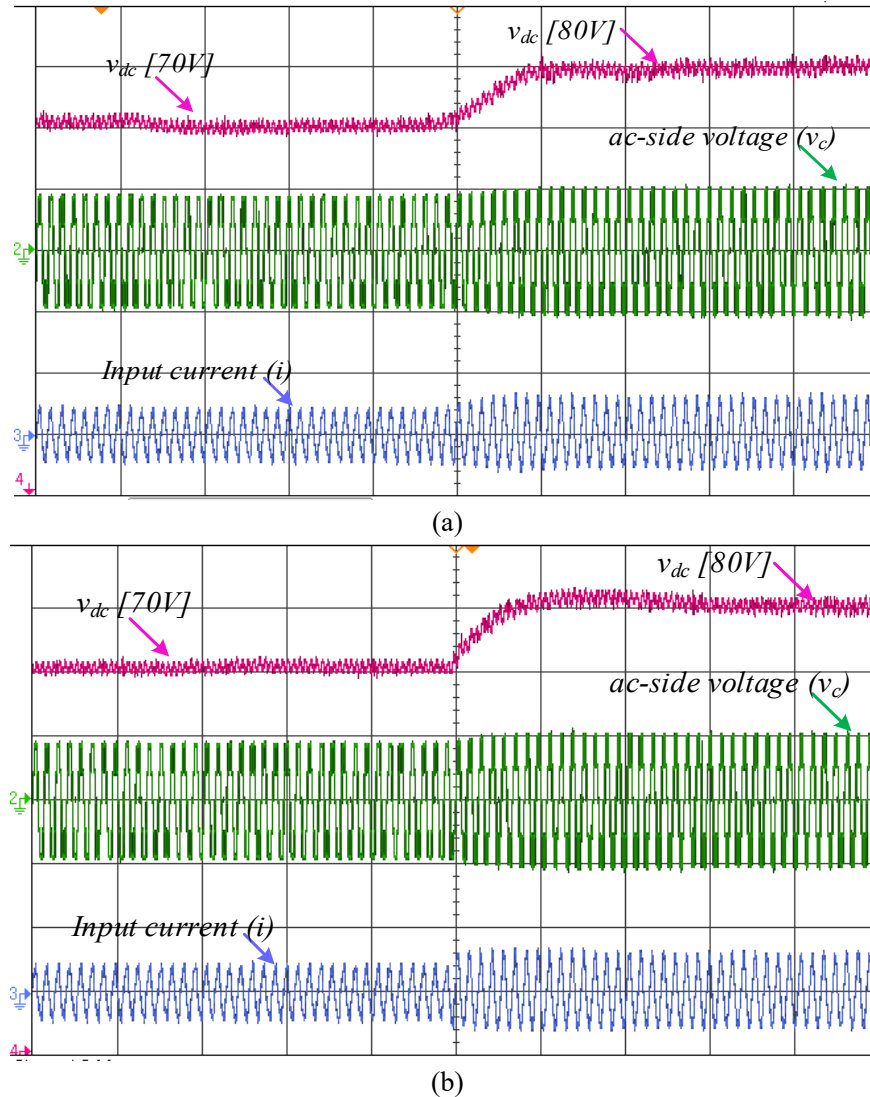
Fig. 3.12 Comparative study of the proposed PI-ESO-based control strategy, and PI control strategy when a step change in the DC-link voltage references is introduced, (vc: 70 V/div), (i: 4 A/div), (V$_{DC}$: 10 V/div), (a) PI-ESO (70 V to 80 V), (b) PI (70 V to 80 V).

Table 3.2 Specification of the Experimental Setup

Parameters	Value	Unit
Sampling frequency	50	kHz
Maximum switching frequency	25	kHz
DC-link capacitor	2.0	mF
Filter capacitor	1.0	μF
Filter inductor	3.0	mH
Input AC voltage (V_m)	70	V
Grid Frequency	50	Hz
Main control chip	TMS320F28379D	
Voltage sensor	LV 25-P/SP5	
Current sensor	LA 25-NP	
Switch	SCT3022ALGC11	
Diode	HFA15PB60	

Table 3.3 Time Required by the Different Tasks of the Control Algorithm

Task	Value	Unit
PLL Synchronization	197	ns
Adaptive notch filter	78	ns
MPC	514	ns
PI-controller	26	ns
Current reference generation	29	ns
ESO	53	ns
ADCs reading	48	ns
Gate pulses	163	ns

Table 3.4 Controller Design Parameters

Parameters	Values
PI parameters	$k_p = 0.2$, $k_i = 5$
ESO parameters	$\beta_1 = 0.4$, $\beta_2 = 20$
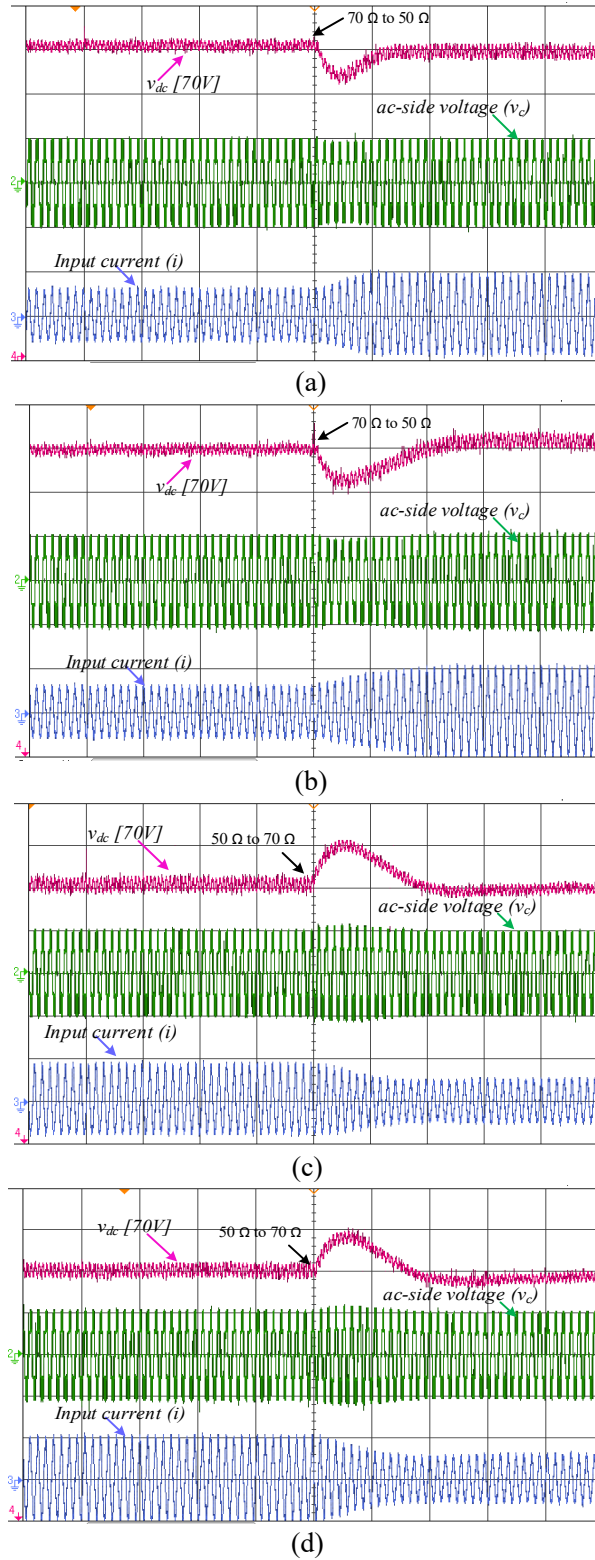
Fig. 3.13 Comparative study of the proposed PI-ESO-based control strategy, and PI control strategy when a step change in the DC-link load references is introduced; (v_c: 70 V/div), (i: 4 A/div), (V_{DC}: 10 V/div), (a) PI-ESO (70 Ω to 50 Ω), (b) PI (70 Ω to 50 Ω), (c) PI-ESO (50 Ω to 70 Ω), (d) PI (50 Ω to 70 Ω).
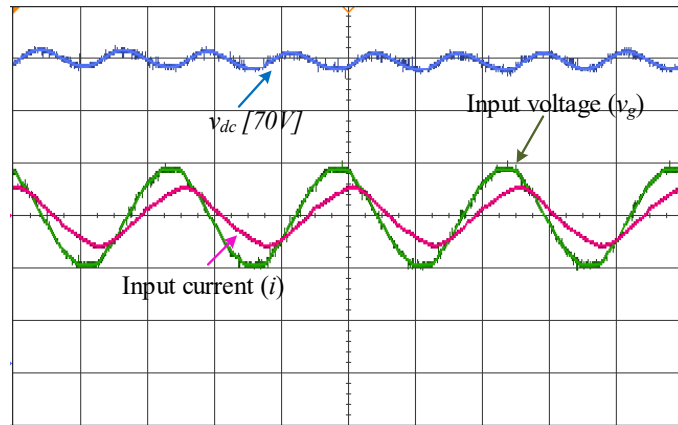
Fig. 3.14 Experimental waveforms for reactive power compensation of the 5L-T-AHB AC/DC converter, (v_g: 70 V/div), (i: 4 A/div), (V_{DC}: 10 V/div).

3.5 Conclusion

A cascaded control scheme consisting of an FCS-MPC with the PI-ESO to drive a single-phase 5L-T-AHB converter was proposed to improve the disturbance rejection capability. With the proposed control strategy, the current control loop was designed to track the reference currents by using the derived FCS-MPC algorithm, while maintaining the balanced capacitor voltages and reactive power reference. The key novelty of this approach is the active power reference design with the ESO-based disturbance observer to improve the DC-link voltage tracking performance in the presence of external disturbances. Compared with the traditional PI-based controller, this scheme presents a faster dynamic response in reducing settling time, and presents zero steady-state error under an unexpected step load condition and a step variation in the DC-link voltage reference. The effectiveness of the proposed control scheme has been verified by the experimental results.

4 Disturbance Rejection Based Control Scheme for Hybrid Five-level Converters in Microgrid Applications

4.1 Introduction

Single-phase voltage-source converters (VSCs) are the main component to integrate DC-bus microgrids comprised of electric vehicles (EVs), energy storages (ESs), and renewable energy sources (RESs) into the distribution grid. As the active front end (AFE) rectifiers, they can control the power factor through power flow control to provide ancillary services when required [4-6]. It is thus of great importance to design a robust control system for these converters. In such a single-phase power conditioning system, the DC-bus voltage has a significant impact on the control of current and power flow between the microgrid and the distribution grid. The DC-bus voltage control is a challenging task due to the presence of the double-grid frequency ($2\omega_o$) pulsating power component that flows through the DC side of the converter and causes double-line frequency voltage ripple in the DC-bus voltage. The presence of this voltage ripple in the DC-bus is inherent in both inverters and rectifiers [14]. This ripple voltage in a feedback control system degrades the quality of AC current by adding additional harmonics, and therefore, must be removed in order to achieve high-quality power conversion. A low bandwidth filter is usually used to remove this low frequency ripple component completely. The low bandwidth filter, however, introduces a significant phase delay in the DC-bus voltage control loop. As a result, the control performance to regulate the DC-bus voltage is affected during transients. To regulate effectively the DC-bus voltage, a high bandwidth is desired, and thus, a trade-off should be made between the conflicting constraints, such as the grid current quality and dynamic performances [16].

Various methods have been proposed to address the difficulties associated with the DC-bus ripple voltage [6-14]. The coupled inductor and loop compensator based approaches are presented in [54, 91, 92]. However, these approaches require a high order filter with poles and zeros at low frequencies. Several active filter based techniques have been introduced in

[14, 93-97]. These techniques require additional energy storage devices and converters in the DC side, which increases the cost and control complexity, and decreases the overall efficiency. To remove this ripple, a notch filter (NF) and a finite impulse response (FIR) filter tuned at $2\omega_o$ were reported in [16, 98], and [98], respectively. However, a low bandwidth must be selected during the filter design for complete elimination of this ripple, which results in slower dynamic response during transients. To settle the conflicting constraints of the grid current distortion and dynamic performance, a new method is required that can improve the AC current quality while realizing fast dynamic performance during transients.

This research introduces a new filter-less approach to remove the double grid-frequency voltage ripple component from the measured bus voltage. By analyzing the DC-bus voltage, an expression of the DC-bus ripple voltage component is obtained. Instead of using an additional filter or hardware, the new method uses the existing phase-locked-loops (PLLs) information to calculate the DC-bus ripple voltage. The DC component can then be deduced by subtracting the estimated ripple from the measured DC-bus voltage. Since the proposed approach can eliminate the need for filter or additional hardware, the difficult trade-off between the conflicting constraints (i.e. grid current harmonics and transient performance) can be avoided, enabling the simple design of the voltage control loop. The proposed approach can improve the transient performance without distorting the AC current.

Another essential control aim is to self-support the DC-bus voltage under disturbances such as sudden variation of the active power drawn by the converters due to the load changes. The bus voltage regulation is usually done by the outer voltage controller, where a feedback loop is used to update the control input (the active power reference). Numerous control techniques have been reported in the literature to achieve this control objective. The most commonly employed methods are the proportion-integration (PI) based controllers due to their simple structures. These controllers employ PI with constant gain parameters for both the outer voltage controller and inner current controller [99]. Several PI-based methods have been reported in [3, 54, 100-104]. The performance of these methods depends on the PI controller gain parameters that need to be updated under different operating conditions. However, most of these methods do not consider these variations. Thus, the dynamic performance will be affected by using constant PI gain parameters under different operating

conditions. A PI-based method was presented in [54], which considers both conflicting constraints, such as the AC grid current quality and the DC-bus voltage fluctuations. However, this method increases the grid current distortion at low bus capacitor value.

To reduce the DC-bus voltage fluctuations during external disturbances, the feedforward control approaches are reported in [101, 105, 106]. These methods feed forward the external power to reduce the voltage fluctuation. However, these methods require additional sensors to measure the external power, which increases the cost and decreases the reliability. Nevertheless, these approaches increase the grid current harmonics due to the coupling between the DC and AC sides. The major drawback of the PI-based strategy is the dependence of dynamic and steady-state performances on the tuning of PI gain parameters in both the outer voltage controller and the inner current tracking controller. Therefore, the overall system behavior will be affected by using the constant PI gain parameters during external disturbances.

The other commonly studied approaches are the direct power control (DPC) [61], DPC based on Fuzzy method [107], and model predictive DPC [63, 108]. Among these methods, the predictive control method provides the best performance, but the parameter sensitivity is the major problem of the predictive controller [99, 108]. Recently, several advanced methods have been proposed in three-phase applications to improve the control performance such as the multiple-vector model predictive power control [109], predictive current control [110], model predictive DPC [111], and model predictive DPC with finite control set [112]. These control methods are usually governed by the conventional PI-based outer voltage control loop. Therefore, the control performance of these methods still suffer from poor dynamic behaviour or overshoot during system parameter uncertainties. Moreover, these control approaches are not studied in single-phase applications, where the control performances are affected by the DC-bus voltage ripple elimination methods. Therefore, it is much desired to design an advanced control method to improve the dynamic and steady state performance against the disturbances, and system parameter fluctuations.

In order to overcome the limitations of the existing methods, this research proposes a sliding mode control (SMC) incorporated with an extended state observer (ESO) as the outer voltage controller. The SMC-ESO significantly improves the dynamic and steady state

performance in the presence of disturbances. The available literature shows that single-phase applications traditionally employ the three-level H-bridge converter. By contrast, this project adopts the five-level T-type converter in order to improve the AC grid current quality, and reduce the required voltage rating of the semiconductor devices and EMI filter size. However, realizing the multilevel voltage at the AC side will be affected by the use of series connected capacitor in the converter structure if further control action is not taken into account. In this work, a finite control set model predictive control (FCS-MPC) algorithm is derived to track the desired current references. A cost function is formulated to balance the voltages across the capacitors connected in series in the DC-bus of the converter.

4.2 System Model and Problem Statement

4.2.1 Analysis of the DC-bus voltage

The presence of double grid frequency AC voltage ripple component on the top of the DC-bus voltage is inherent in a single-phase grid-connected AC/DC power converter. Since a feedback loop is used to regulate the DC-bus voltage, this ripple component modulates the generated output AC current of the converter if the voltage ripple is not filtered properly. Consequently, the converter current is distorted by this ripple component. This ripple voltage should be managed properly in order to avoid the adverse effect on the control performances such as slow dynamic performance during transients and increased harmonic content in the generated grid current. The value of the DC-bus voltage and its double grid frequency ripple component can be calculated by balancing the input and output power of the converter as presented below.

The grid voltage $v_g(t)$ and current $i_g(t)$ are assumed as

$$v_g(t) = V_m \sin(\omega t) \tag{4.1}$$

$$i_g(t) = I_m \sin(\omega t + \varphi) \tag{4.2}$$

where V_m and I_m are the peak values of the input voltage and current of the converter, respectively, ω is the angular frequency and φ the phase angle difference between the grid voltage and current.
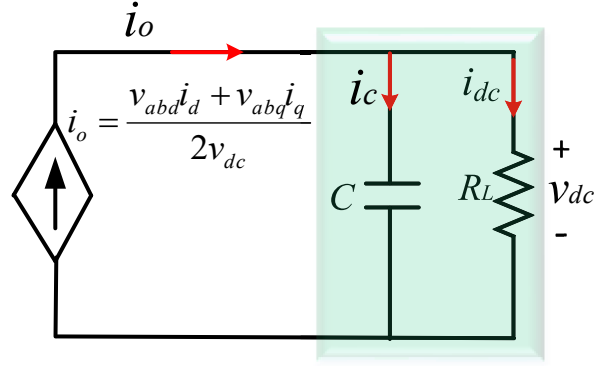
Fig. 4.1 Equivalent circuit of a single-phase AC/DC converter.

To simplify the analysis, the single-phase AC/DC converter can be represented by an equivalent circuit, as shown in Fig. 4.1 and the power losses in the circuit are neglected. Thus, the instantaneous input power at the grid-side can be calculated as

$$P(t) = v_g(t)i_g(t) = \frac{V_m I_m}{2}\cos\varphi - \frac{V_m I_m}{2}\cos(2\omega t + \varphi) \tag{4.3}$$

The ripple voltage Δv is small compared to the DC bus voltage when a large capacitor is used in the DC-bus. Therefore, the input power $P(t)$ operates at approximately constant voltage. The output current can be calculated as

$$i_0(t) \cong \frac{P(t)}{V_{dc}} = \frac{V_m I_m}{2V_{dc}}\cos\varphi - \frac{V_m I_m}{2V_{dc}}\cos(2\omega t + \varphi) \tag{4.4}$$

The AC part of $i_o(t)$ flows through the DC-bus capacitor and the DC component flows through the load resistor R_L.

The current through the bus capacitor can be expressed as

$$C\frac{dv_{dc}(t)}{dt} = i_o(t) - \frac{v_{dc}(t)}{R_L} \tag{4.5}$$

Multiplying both sides of (4.5) by $v_o(t)$, we have

$$Cv_{dc}(t)\frac{dv_{dc}(t)}{dt} = P(t) - \frac{v_{dc}^2(t)}{R_L} \tag{4.6}$$

From (4.6), it can be concluded that the power flowing into the bus capacitor C is the difference between the input power and the power consumed by the load resistor, R_L.

The energy stored in the bus capacitor can be given as

$$E(t) = \frac{1}{2}Cv_{dc}^2(t) \tag{4.7}$$

Thus, the power flowing through the bus capacitor can be written as

$$\frac{dE(t)}{dt} = Cv_{dc}(t)\frac{dv_{dc}(t)}{dt} \tag{4.8}$$

Substituting (4.7) and (4.8) into (4.6), we have

$$\frac{dE(t)}{dt} = P(t) - \frac{2E(t)}{R_L C} \tag{4.9}$$

Solving (4.9), we obtain

$$E(t) = E(0)e^{-\frac{2t}{R_L C}} + e^{-\frac{2t}{R_L C}}\int_0^t e^{\frac{2\tau}{R_L C}}P(\tau)d\tau \tag{4.10}$$

Considering that the grid voltage and current are in phase and substituting (4.10) into (4.7), one obtains the expression of the DC-bus voltage as given as

$$v_{dc}(t) = \sqrt{\frac{2\left(E(0)e^{-\frac{2t}{R_L C}} + e^{-\frac{2t}{R_L C}}\left(\frac{CV_m R_L I_m\left(e^{\frac{2t}{R_L C}}-1\right)}{4} - I_m V_m\left(\frac{k}{2}\right) + \frac{C^2 R_L^2 \omega e^{\frac{2t}{R_L C}}\sin(2\omega t)}{2\left(C^2 R_L^2 \omega^2 + 1\right)}\right)\right)}{C}}$$

$$\tag{4.11}$$

where $\quad k = CR_L\left(e^{\frac{2t}{R_L C}}\cos(2\omega t) - 1\right)$

Fig. 4.2 shows a typical bus voltage waveform during turn-on obtained from (4.11).
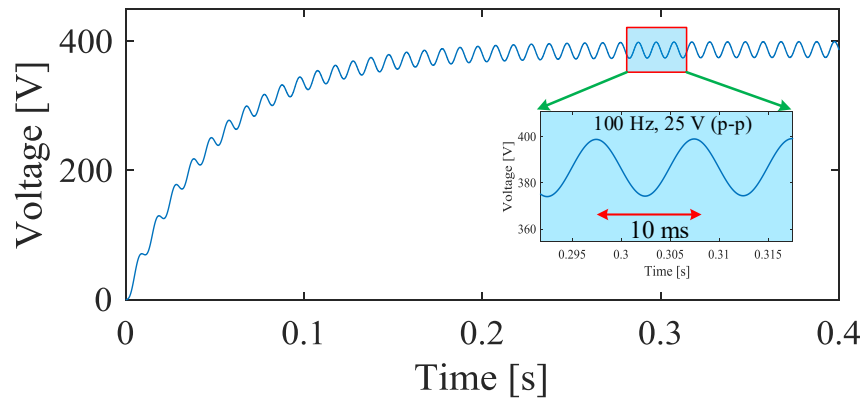
Fig. 4.2 DC-bus voltage waveform of a single-phase converter during turn-on transient, as given by (4.11).

As shown, the bus voltage waveform consists of double grid frequency ripple, steady-state DC and transient components. In a closed loop control system, the measured DC-bus voltage should be filtered to estimate the DC component of the bus voltage in order to avoid the harmonic distortion in the generated AC grid current by this ripple voltage. Moreover, the filtering method should provide a fast dynamic performance in calculating the DC component during the transients with zero steady-state error.

4.2.2 Dynamic System Model

Fig. 4.3 shows the power circuit of the single-phase five-level hybrid power converter under consideration, where the converter is connected to the power grid through a smoothing inductor with inductance, L, in series with winding resistance, r. Two capacitors, C_1 and C_2, connected in series and a resistive load R_L, are connected to the DC-bus. A step change of the load resistance, R_L, would cause a sudden variation of active power drawn by the converter from the power grid. In this work, the step variation of the load resistance R_L is considered as the unknown external disturbance to the converter.
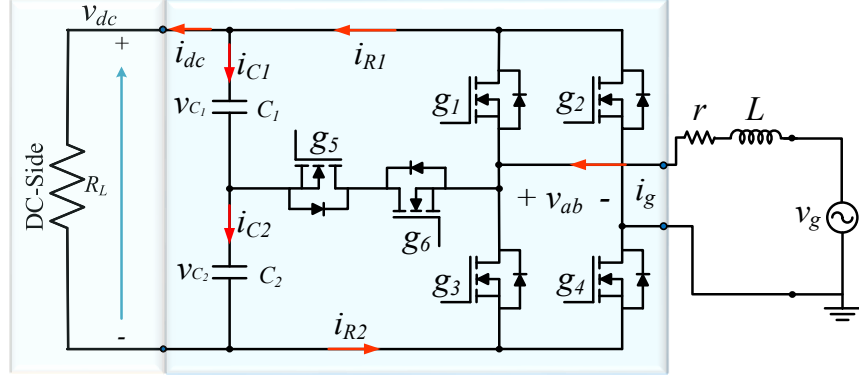
Fig. 4.3 Topology of the adopted single-phase T-type hybrid power converter.

According to the Kirchhoff's voltage and current laws, the dynamics of the grid current $i_g(t)$ and the DC-bus series connected capacitor voltages, $v_{C_1}(t)$ and $v_{C_2}(t)$, are governed by the following equations

$$L\frac{di_g(t)}{dt} = v_g(t) - v_{ab}(t) - i_g(t)r \tag{4.12}$$

$$C_1\frac{dv_{C_1}(t)}{dt} = i_{R_1}(t) - i_{dc}(t) = i_{R_1}(t) - \frac{v_{dc}(t)}{R_L} \tag{4.13}$$

$$C_2\frac{dv_{C_2}(t)}{dt} = i_{R_2}(t) - i_{dc}(t) = i_{R_2}(t) - \frac{v_{dc}(t)}{R_L} \tag{4.14}$$

where v_{ab} is the converter output voltage, i_{R_1} and i_{R_2} are the internal current of the converter, and i_{dc} is the DC-bus current.

Resolving the grid voltage, v_g, the converter voltage, v_{ab}, the inductor current, i_L, and the DC-bus voltage, v_{dc} into their d and q components at the power grid frequency ω_o, we can express the system dynamics model as follows

$$\frac{di_d}{dt} = \frac{v_d}{L} - \frac{v_{abd}}{L} - \frac{r}{L}i_d + i_q\omega_o \tag{4.15}$$

$$\frac{di_q}{dt} = \frac{v_q}{L} - \frac{v_{abq}}{L} - \frac{r}{L}i_q - i_d\omega_o \tag{4.16}$$

$$\frac{C}{2}\frac{dv_{dc}}{dt} = \frac{v_{abd}i_d + v_{abq}i_q}{2v_{dc}} - \frac{v_{dc}}{R_L} \tag{4.17}$$

where i_d, v_d and v_{abd} are the d-axis, and i_q, v_q and v_{abq} are the q-axis parts in dq rotating frame of i_g, v_g, and v_{ab}, respectively.

This nonlinear system consists of three state variables i_d, i_q and v_{dc} and two control inputs v_{abd} and v_{abq}. For simplification, the winding resistance r is neglected in this analysis. When the system is at the equilibrium point, (4.15)-(4.17) can be simplified as

$$v_{abd} = v_d + i_q \omega_o L \tag{4.18}$$

$$v_{abq} = -i_d \omega_o L \tag{4.19}$$

$$\frac{v_{dc}^2}{R_L} = \frac{v_d i_d}{2} \tag{4.20}$$

From (4.18)-(4.20), it can be concluded that the DC-bus voltage depends on the d-axis component, i_d, of the grid current. The q-axis component of the grid current, i_q, controls the power factor. For unity power factor operation, the q-axis component must be set to zero (i.e. $i_q = 0$).

4.2.3 Necessity of Modelling Uncertainties

To simplify the controller design, during system modelling, various assumptions are often made to ignore the non-ideal factors, including the inductor winding resistance, switching losses, DC-bus capacitance variation, and external disturbances due to the load variations, resulting in inaccurate prediction of the actual system behavior under different operating conditions, and affecting effectiveness of the DC-bus voltage controller. Therefore, in order to design a robust controller, these system uncertainties must be considered properly.

4.3 Proposed Control Scheme

The proposed control approach aims to improve the steady-state and transient performances in regulating the DC-bus voltage under unexpected external disturbances, and achieving the highest grid current quality. The controller design is based on the cascaded structure. Fig. 4.4 illustrates the controller block diagram, including an outer voltage controller and an inner current controller. The outer voltage regulation loop consists of a sliding mode controller (SMC), an extended state observer (ESO), and a DC-bus voltage ripple estimator. The ESO is designed to estimate the disturbances to the converter, and an SMC is employed in parallel with the ESO to calculate the reference active power value for the internal current tracking controller. In this work, a filter-less method is used to estimate the DC value of the bus voltage, which provides a fast transient performance in approximating the DC-value. Besides that, the inner current tracking controller is designed based on a finite control set-model predictive control (FCS-MPC) algorithm.
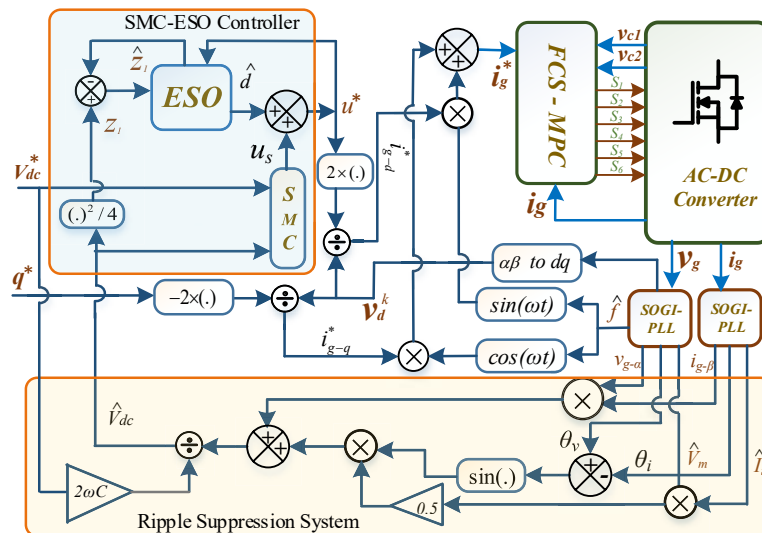
Fig. 4.4 Proposed control system of the hybrid power converter.
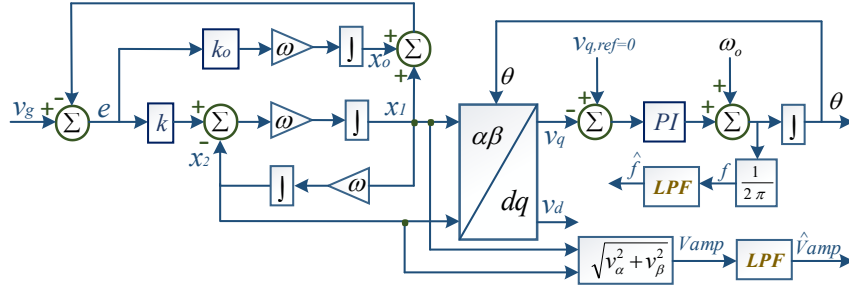
Fig. 4.5 Block diagram of the PLL.

4.3.1 Proposed Ripple Voltage Estimation Method

In the proposed method, the DC-bus ripple voltage is calculated based on the estimated quantities obtained from the PLLs. The block diagram of the PLL is illustrated in Fig. 4.5. The estimated ripple is then subtracted from the measured bus voltage to acquire the DC component of the bus voltage. From (4.4), the current through the DC-bus capacitor can be expressed as

$$C\frac{dv_{dc}(t)}{dt} = -\frac{V_m I_m}{2V_{dc}}\cos(2\omega t + \varphi) \tag{4.21}$$

where $v_{dc} = V_{dc} + \Delta v$.

By integrating (4.21), the magnitude of the ripple voltage component can be approximately as

$$\Delta v \cong \frac{V_m I_m}{4V_{dc}\omega C} \tag{4.22}$$

Therefore, the bus voltage and its ripple component can be approximated as

$$v_{dc}(t) \approx V_{dc,avg} + \frac{V_m I_m}{4V_{dc,avg}\omega C}\sin(2\omega t + \varphi) \tag{4.23}$$

where $V_{dc,avg}$ is the average bus voltage.

According to (4.23), the value of $\sin(2\omega t+\phi)$, the magnitude of the grid voltage V_m and current I_m are required to estimate the ripple component of the DC-bus voltage. In the proposed method, the α component of the grid voltage $v_{g\text{-}\alpha}$ and the β component of the grid current $i_{g\text{-}\beta}$ are multiplied to generate the grid double-frequency component.

Multiplying $v_{g\text{-}\alpha}(t)$ and $i_{g\text{-}\beta}(t)$, we have

$$V_m \sin(\omega t) \times I_m \cos(\omega t + \varphi) = \frac{V_m I_m}{2} \sin(2\omega t + \varphi) - \frac{V_m I_m}{2} \sin(\varphi) \qquad (4.24)$$

Thus, the ripple component can be calculated by adding $(V_m.I_m /2)\sin\phi$ in (4.24) and multiplied by $1/(2V_{dc,avg}\omega C)$.

4.3.2 Sliding Mode Control

According to (4.20), an inherent relationship is presented between the DC-bus voltage and the *d*-axis component of the grid current. In other words, the DC-bus voltage depends on the active power. In this project, an SMC is employed to calculate the reference active power value.

A. Sliding surface

The sliding surface S is chosen as a linear combination of two state variables, i.e.

$$S = \alpha_1 x_1 + \alpha_2 x_2 \qquad (4.25)$$

where α_1 and α_2 represent the sliding coefficients.

The controlled state variables are defined as the DC-link voltage error, x_1, and the integral of the voltage error, x_2, which can be expressed as

$$x_1 = V_{dc} - V_{dc,ref} \qquad (4.26)$$

$$x_2 = \int (V_{dc} - V_{dc,ref})dt \qquad (4.27)$$

Thus, the sliding surface can be given as

$$S = \alpha_1(V_{dc} - V_{dc,ref}) + \alpha_2 \int (V_{dc} - V_{dc,ref})dt = \lambda(V_{dc} - V_{dc,ref}) + \int (V_{dc} - V_{dc,ref})dt = 0 \qquad (4.28)$$

where $\lambda = \alpha_1/\alpha_2$ is a positive constant, which should be tuned in order to achieve the optimal results of settling time, steady state error, and overshoot.

The time derivative of (4.28) is given as [56]

$$\dot{S} = \lambda \dot{V}_{dc} + (V_{dc} - V_{dc,ref}) \qquad (4.29)$$

B. Control law

Rearranging (4.6), we can express the input power in the DC-bus as

$$P_{dc}(t) = Cv_{dc}(t)\frac{dv_{dc}(t)}{dt} + \frac{v_{dc}^2(t)}{R_L} \tag{4.30}$$

where $Cv_{dc}(t)\frac{dv_{dc}(t)}{dt}$ is the power flowing into the DC-bus capacitor C and $\frac{v_{dc}^2(t)}{R_L}$ is the power

consumed by the load resistor R_L.

By ignoring the switching losses, i.e. assuming the converter as lossless, the input active

power $P(t)$ at the grid-side of the power converter is equal to the output power $P_{dc}(t)$ in the

DC-bus. Thus, the control law is designed as

$$u = \begin{cases} P_{inst.}^+(t), & S > 0 \\ P_{inst.}^-(t), & S < 0 \end{cases} \tag{4.31}$$

where $P_{inst.}^+(t)$ and $P_{inst.}^-(t)$ denote the instantaneous input active power when the

corresponding control decision will be directed toward the desired equilibrium point.

Therefore, (4.30) can be rewritten as

$$\frac{dV_{dc}(t)}{dt} = \frac{u}{CV_{dc}} - \frac{V_{dc}}{R_L C} + \delta \tag{4.32}$$

where δ is the disturbance in the DC-bus voltage of the converter. The bound of the external

disturbance, ρ_s, is considered as $|\delta| \leq \rho_s < 1$,, where ρ_s is a positive constant [56].

Thus, the control output can be obtained by [56]

$$u_S = \left[\left(\frac{1}{R_L C} - \frac{1}{\lambda} \right) V_{dc} + \frac{1}{\lambda} V_{dc,ref} - (\rho_s + k).sign(S_V) \right] V_{dc} C \tag{4.33}$$

The stability study of the SMC is given in [56].

4.3.3 Observer Design

While the SMC law is designed according to the system model, the dynamic performance

is still affected by the system parameter uncertainties (e.g., external load variation). In order

to overcome the limitations of SMC, an ESO is designed and applied in parallel with the SMC

to calculate the reference active power and compensate the system uncertainties, such as the

external load variation and plant dynamic variation. Thus, the control output of the proposed

scheme can be given as

$$u = u_S + \hat{d} \tag{4.34}$$

where u_S is the SMC controller output obtained by (4.33), and $\hat{d}$ the observed value by the observer.

From (4.17), the capacitor voltage dynamic can be written as

$$\frac{C}{2}\frac{dv_{dc}}{dt} = \frac{1}{v_{dc}}\left(p^* - p_t\right) \tag{4.35}$$

where $p^* = \frac{v_{abd}i_d + v_{abq}i_q}{2}$, $p_t = \frac{v_{dc}^2}{R_P} + \frac{v_{dc}^2}{R_L}$, and R_P is the equivalent resistance connected in parallel with the load resistor, R_L, which stands for the switching losses of the converter.

Defining a new variable $z_1 = \frac{(v_{dc})^2}{4}$, one can rewrite (4.35) as

$$C\frac{dz_1}{dt} = u - d(t) \tag{4.36}$$

where $d(t) = p_t = z_2$, $p^* = u$, and the disturbance z_2 is considered as the extended state.

The derivative of z_2 is defined as h, and it can be expressed as

$$\frac{dz_2}{dt} = h(t) \tag{4.37}$$

The ESO can be designed as

$$C\dot{\hat{z}}_1 = u - \hat{z}_2 + \beta_1\left(z_1 - \hat{z}_1\right) = u - \hat{z}_2 + \beta_1 e \tag{4.38}$$

$$\dot{\hat{z}}_2 = -\beta_2\left(z_1 - \hat{z}_1\right) = -\beta_2 e \tag{4.39}$$

where $e = z - \hat{z}$, β_1 and β_2 are the positive gain parameters of the ESO, $\hat{z}_1$ and $\hat{z}_2$ the estimated parameters of z_1 and z_2, respectively.

The error dynamics are given by

$$C\dot{e} = -\beta_1 e - e_d \tag{4.40}$$

$$\dot{e}_d = h(t) + \beta_2 e \tag{4.41}$$

where $h(t) = \dot{\hat{d}}$ is defined as the load power change rate, and $e_d = d - \hat{d}$.

The systems expressed in (4.40) and (4.41) can be rewritten as

$$\begin{bmatrix} \dot{e} \\ \dot{e}_d \end{bmatrix} = \begin{bmatrix} -\dfrac{\beta_1}{C} & -\dfrac{1}{C} \\ \beta_2 & 0 \end{bmatrix} \begin{bmatrix} e \\ e_d \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} h(t) \tag{4.42}$$

To make the error dynamics converge to the equilibrium point, the values of the gain parameters, β_1 and β_2, are required to be chosen so that the polynomial of (4.42), i.e. $\lambda^2 + (\beta_1/C)\lambda + \beta_2/C$ is Hurwitz stable. Finally, the estimated disturbance to the converter, $\hat{d}$ is added to the control output obtained from the SMC controller to deduce the reference active power value.

4.3.4 FCS-MPC

In order to predict the grid current and the DC-bus capacitor voltages, (4.12)-(4.14) are converted into the form of discrete time by applying the Euler's discretization technique as

$$i_g[k+1] = \left(1 - \frac{rT_s}{L}\right) i_g[k] + \left(v_g[k] - v_{ab}[k]\right)\frac{T_s}{L} \tag{4.43}$$

$$v_{C_1}[k+1] = v_{C_1}[k] + \frac{T_s}{C_1} i_{R_1}[k] - \frac{T_s}{C_1} i_{dc}[k] \tag{4.44}$$

$$v_{C_2}[k+1] = v_{C_2}[k] + \frac{T_s}{C_2} i_{R_2}[k] - \frac{T_s}{C_2} i_{dc}[k] \tag{4.45}$$

The output voltage of the converter, v_{ab}, is obtained from Table 4.1 for different switching states. The internal currents of the converter, i_{R_1} and i_{R_2}, can be obtained from the grid current measurement, i_g, for individual switching states, as shown in Table 4.1. As a result, the unnecessary current measurement can be avoided, which can reduce the cost and complexity of the system. In the proposed system, the current reference of the converter is calculated by

$$i_g = \frac{2p}{v_{gd}} \sin(\omega t) - \frac{2q}{v_{gd}} \cos(\omega t) \tag{4.46}$$

where the value of ωt is calculated from the PLL, v_{gd} the d-axis component of the grid voltage, p the control output obtained from the SMC-ESO controller, and q the reference reactive power value.

Table 4.1 Possible States of the Converter

	g_1	g_2	g_3	g_4	g_5	g_6	i_{R_1}	i_{R_2}	v_{ab}
$v_g > 0$	0	0	0	0	0	0	i_g	i_g	$+(v_{C_1} + v_{C_2})$
	0	0	0	0	1	0	0	i_g	$+v_{C_2}$
	0	0	1	0	0	0	0	0	0
$v_g < 0$	0	0	0	0	0	0	i_g	i_g	$-(v_{C_1} + v_{C_2})$
	0	0	0	0	0	1	i_g	0	$-v_{C_1}$
	0	0	0	1	0	0	0	0	0

In the FCS-MPC method, to realize the desired grid current and balanced voltages across the DC-bus capacitors, the cost function is formulated as

$$g_{c.} = \left(i_g^*[k+1] - i_g[k+1]\right)^2 + \frac{p}{V_{ref.}^2}\left(v_{C_1}[k+1] - v_{C_2}[k+1]\right)^2 \tag{4.47}$$

where $v_{ref.}$ is the reference value of the desired DC-bus voltage.

4.3.5 Stability analysis
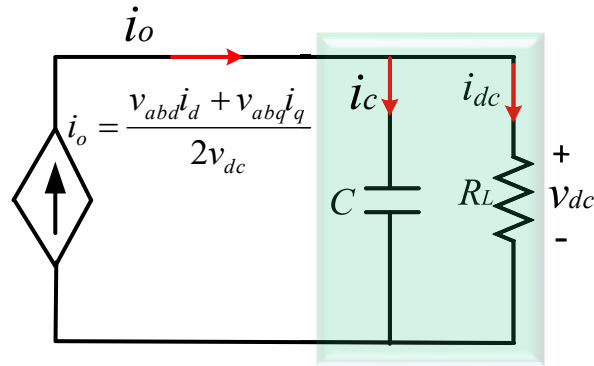
Fig. 4.6 Equivalent transfer function of ESO.

Rearranging (4.35), we have

$$\frac{dz_1}{dt} = \frac{p^*}{C} - \frac{p_{ext.}}{C} - \frac{4z_1}{CR_p} \tag{4.48}$$

where $p_{ext.}$ is the external disturbance.

Applying Laplace transformation, (4.48) can be written as

$$z_1(s) = \frac{R_p}{(CsR_p + 4)} p^*(s) - \frac{R_p}{(CsR_p + 4)} p_{ext.}(s) \qquad (4.49)$$

By using Laplace domain of (4.38) and (4.39), and from Fig. 4.6, the expression for $G_{d\text{-}u}$ can be given as

$$G_{d-u}(s) = \frac{d(s)}{u(s)} = \frac{\beta_2}{Cs^2 + \beta_1 s + \beta_2} \qquad (4.50)$$

Similarly, the expression for G_{d-z_1} can be given as

$$G_{d-z_1}(s) = \frac{d(s)}{z_1(s)} = \frac{\beta_1 \beta_2}{Cs^2 + \beta_1 s + \beta_2} - \frac{\beta_2(\beta_1 + Cs)}{Cs^2 + \beta_1 s + \beta_2} \qquad (4.51)$$

Therefore, based on Fig. 4.6, the expression for $\hat{d}(s)$ can be obtained as

$$\hat{d}(s) = \frac{\beta_2 / C}{s^2 + \dfrac{\beta_1}{C} s + \dfrac{\beta_2}{C}} u(s) - \frac{\beta_2 s}{s^2 + \dfrac{\beta_1}{C} s + \dfrac{\beta_2}{C}} z_1(s) \qquad (4.52)$$

The transfer function of the modified model can be derived as

$$G_p(s) = \frac{R_p}{(R_p Cs + 4)\left[1 + \left(\dfrac{\beta_2 R_p Cs}{(R_p Cs + 4)(Cs^2 + \beta_1 s + \beta_2)}\right) - \left(\dfrac{\beta_2}{(Cs^2 + \beta_1 s + \beta_2)}\right)\right]} \qquad (4.53)$$

The system stability and performance are affected by the converter parameter variations, particularly by the DC-link capacitance changes. To evaluate the stability of the system, the closed loop poles of the modified model are examined to confirm the robustness for a range of the DC-bus capacitance variations. In the proposed system, the nominal value of the capacitance is 1 mF. The root loci of the model G_p with a large capacitance variation from 1.0 mF to 2 mF are shown in Fig. 4.7. It can be observed from the root loci that the closed loop pole moves toward the imaginary axis due to the increase of the DC-bus capacitance value, and thus the system becomes comparatively more oscillatory with reduced damping. However, the closed loop poles are far away from the imaginary axis even when the capacitance value reaches 2 mF, and the system still shows robustness against this variation. The root loci of the

modified model G_p with a variation of R_p from 700 Ω to 200 Ω are shown in Fig. 4.8. As shown, the closed loop poles are far away from the imaginary axis for this variation, showing robustness for this changes as well.
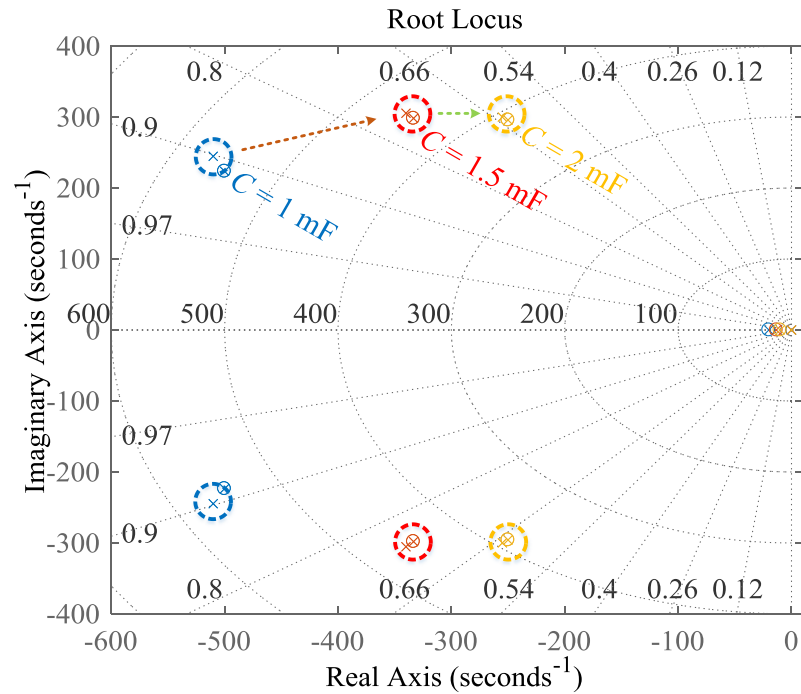
Fig. 4.7 Root loci of the modified model G_p for the variation of DC-bus capacitance.
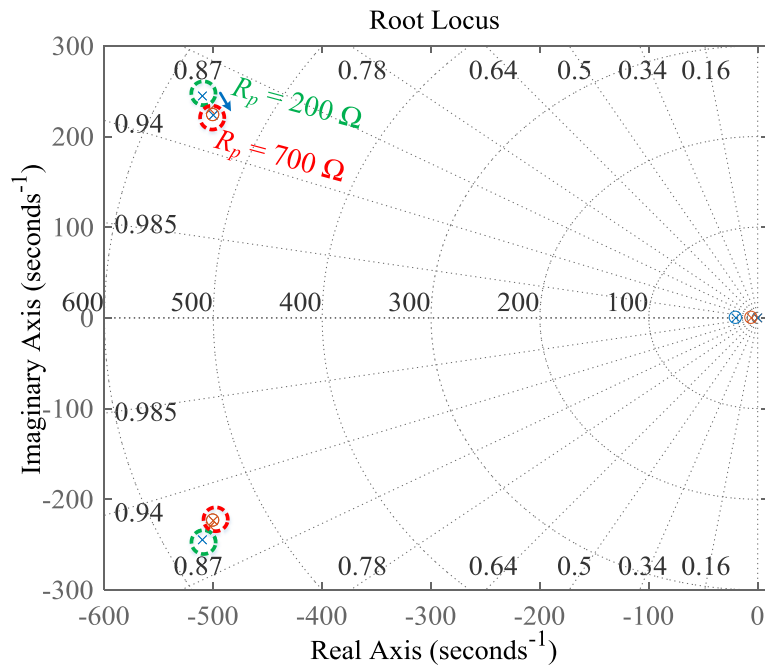
Fig. 4.8 Root loci of the modified model G_p for the variation of R_p.

Table 4.2 System and Controller Parameters

Paremeter	Value
Sampling frequency	50 kHz
Switching frequency (Max.)	25 kHz
Line frequency	50 Hz
AC input voltage (V_m)	325 V
DC-bus voltage (v_{dc})	350 V
DC-bus capacitor ($C_1 = C_2$)	2 mF
Grid side inductor	5 mH
R_p (Nominal)	700 Ω
PI parameters	$k_p = 0.08$, $k_i = 0.2$
ESO parameters	$\beta_1 = 1$, $\beta_2 = 300$
SMC parameters	$k = 20$, $\rho = 0.5$, $\lambda = 0.005$

4.4 Performance Evaluation

To verify the proposed control scheme, the adopted converter with the specifications listed in Table 4.2 is tested. The sampling frequency is set to 50 kHz. The observed maximum switching frequency with the employed FCS-MPC based inner current tracking controller is 25 kHz. To demonstrate the feasibility of the proposed control approach, several test scenarios are implemented and compared with the existing approaches. The inner current control loop remains the same for fair comparison. Fig. 4.9 shows the AC component of the DC-bus ripple voltage, the estimated ripple voltage with the proposed method, and the calculated DC-value of the bus voltage. It can be observed that the proposed method can accurately estimate the DC-bus ripple voltage component. To evaluate the transient performance of the proposed ripple estimation method, a test scenario consists of a step change in the desired DC-bus voltage from 400 V to 350 V. In this test case, the outer voltage and the inner current control loops remain the same, and a 150 Ω load resistance is connected to the DC-bus.
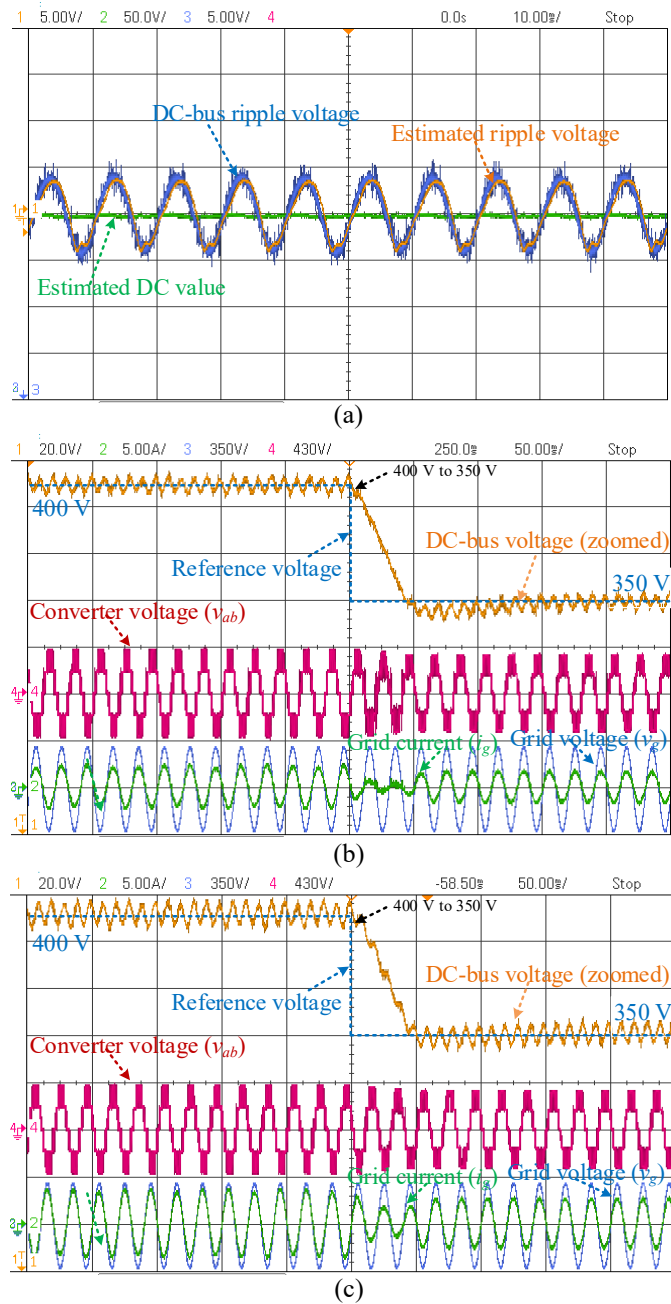
Fig. 4.9 Performance comparison of the ripple estimation methods: (a) DC-bus voltage ripple tracking performance of the proposed method, (b) reference DC-bus voltage tracking performance of the conventional NF based method, and (c) reference DC-bus voltage tracking performance of the proposed ripple estimation method.

Figs. 4.9(b) and (c) show the measurement results associated with the traditional notch filter (NF) and the proposed DC-bus ripple estimation methods, respectively, in realizing the reference voltages during this step variation. The traditional NF-based method presents offset

error during the transient to estimate the DC-bus ripple voltage. As a result, it degrades the dynamic performance during transients, and shows overshoot, as shown in Fig. 4.9(b). As shown, the settling time with the traditional NF based method is ~150 ms and the observed DC-bus voltage overshoot 5 V. Fig. 4.9(c) shows the measurement results associated with the proposed filter-less ripple voltage estimation method during the transient. As shown, the settling time with the proposed method is ~50 ms, which is significantly shorter than that with the NF-based method, and no overshoot is observed.

The second test scenario is designed to compare the external disturbances rejection capability of different DC-bus voltage controllers. A step variation in the active power drawn by the converter is considered as the external disturbance, which is realized by the step changes of the DC-bus load. In this case, the proposed ripple estimation method is used to estimate the DC component of the DC-bus voltage. Figs. 4.10(a)-(d) show the measurement results obtained with the traditional PI controller, the PI combined with the ESO, SMC, and the proposed SMC-ESO approaches, respectively, for the step-up load variations from 200 Ω to 150 Ω. The test results show clearly that the PI-based requires 140 ms to reach the steady-state, and the observed steady-state error is ~7 V. Moreover, the observed maximum voltage fluctuation is ~13 V for this step load change. By contrast, the PI incorporated with the ESO presents an improved transient performance during the step-up load change. This method requires ~120 ms to reach the steady-state and presents zero steady-state error for this step variation. Fig. 4.10(c) shows the results obtained by the traditional SMC method. The result shows that a steady-state error is observed for this uncertain load variation with the SMC method. Fig. 4.10(d) shows the results obtained with the proposed SMC-ESO method. As shown, the proposed method presents the best performance during the load uncertainties. This method requires ~20 ms to reach the steady-state and the observed voltage fluctuation is ~3 V in the transient. Similar set of tests were conducted for step-down load variations from 150 Ω to 200 Ω. The measured waveforms are presented in Fig. 4.11. It can be observed that the conventional PI controller requires 140 ms to reach the steady-state, and presents a voltage overshoot of ~14 V and apparent steady-state error. Comparably, the PI-ESO requires ~120 ms to reach the steady-state and presents an improved transient performance with a voltage overshoot of ~9 V during the step-load change.
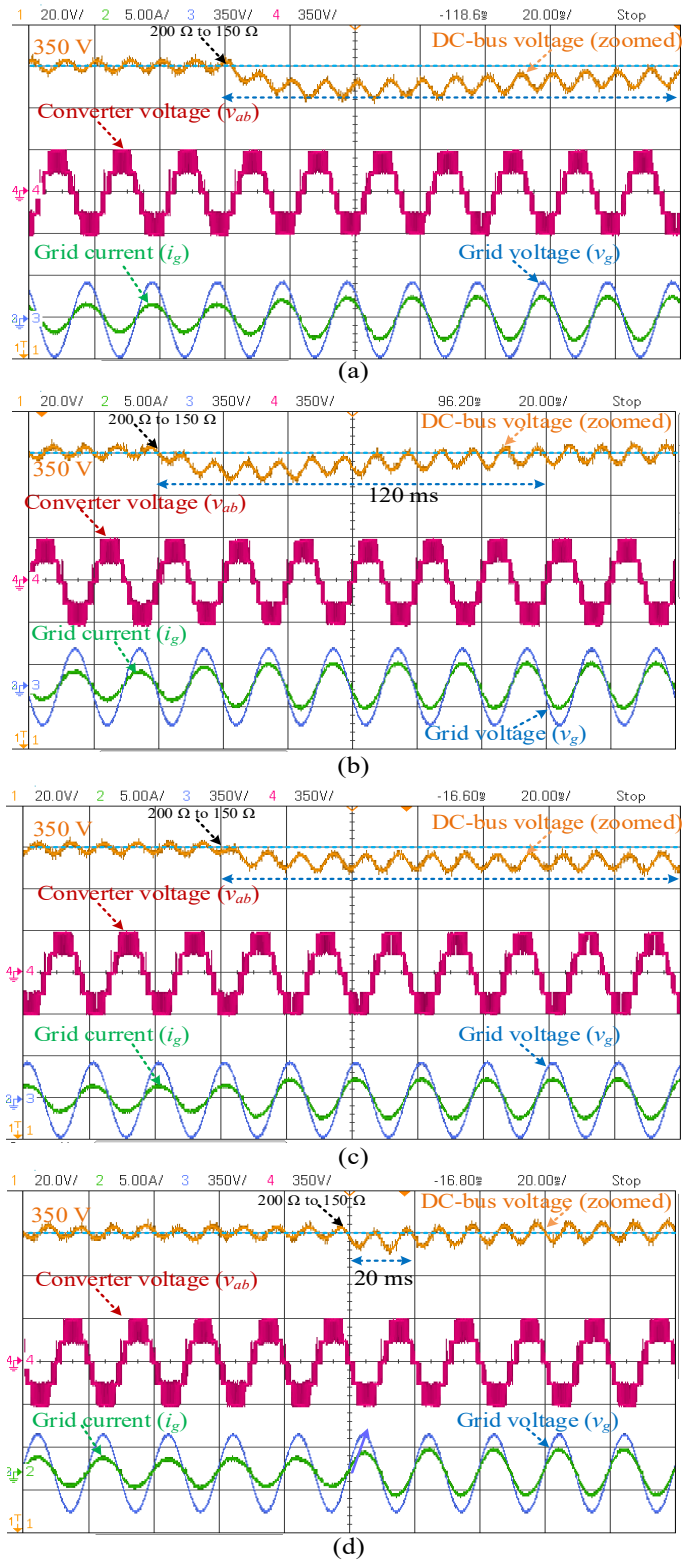
Fig. 4.10 Performance comparison of the control methods under step-up load condition, (a) PI, (b) PI-ESO, (c) SMC, and (d) SMC-ESO.
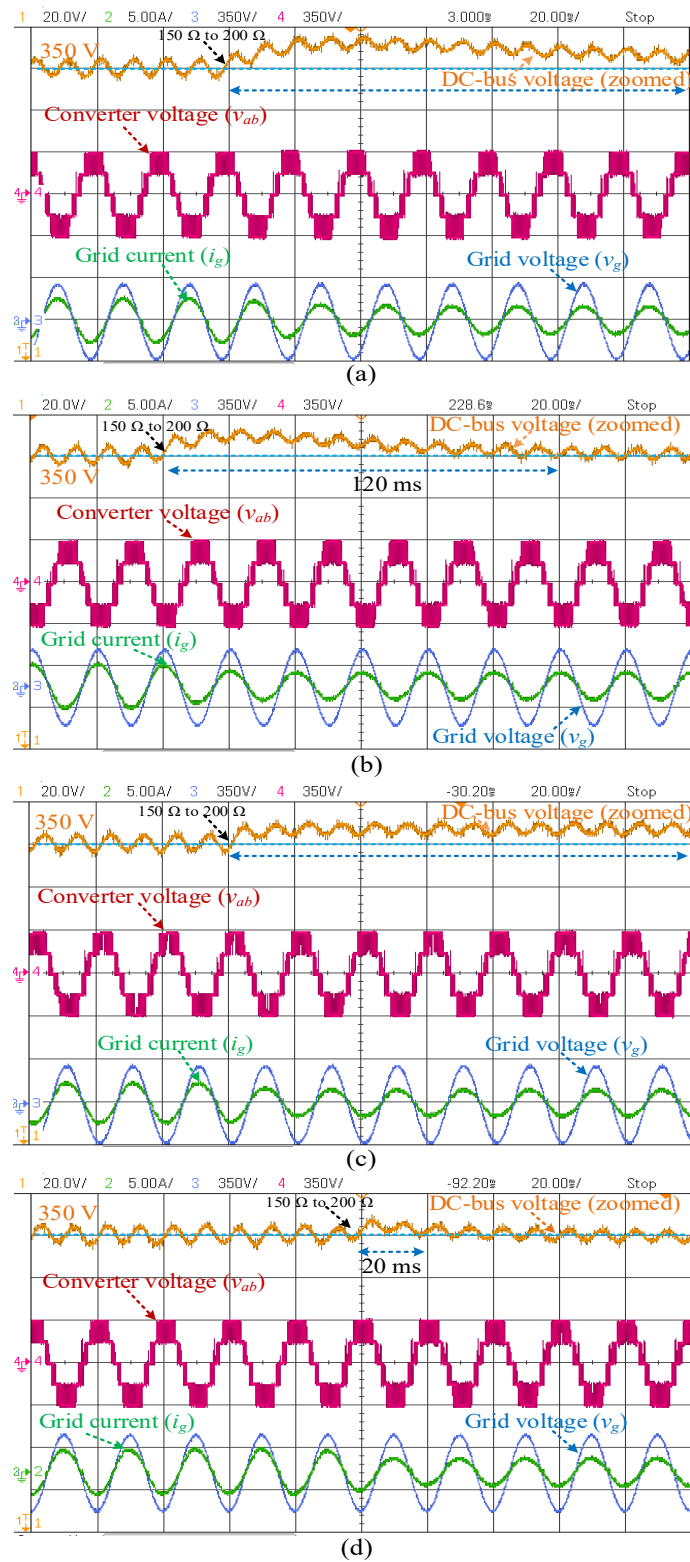
Fig. 4.11 Performance comparison of the control methods under step-down load condition, (a) PI, (b) PI-ESO, (c) SMC, and (d) SMC-ESO.
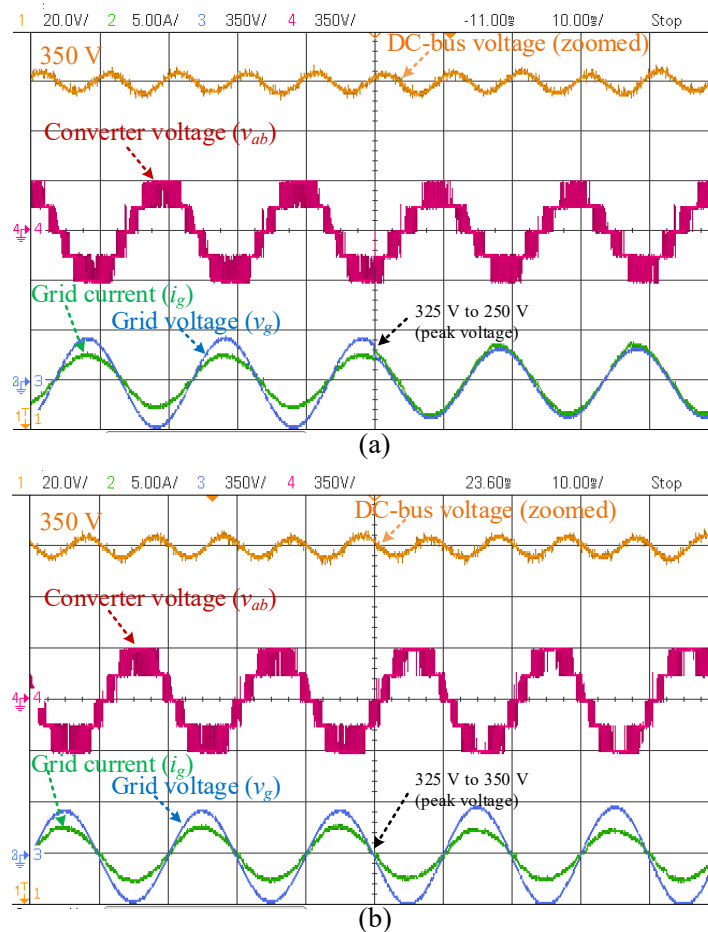
Fig. 4.12 Performance of the proposed method under grid voltage variations, (a) amplitude step changes from 325 V to 250 V, and (b) amplitude step changes from 325 V to 350 V.

Fig. 4.11(c) shows the results obtained by the traditional SMC method during this step-down load variation, and an apparent steady-state error of 8 V is observed during this variation. By contrast, the proposed SMC-ESO method presents the best performance during the load step-down. It takes ~20 ms to reach the steady state with no visible overshoot. Form the results, it is shown clearly that the SMC-ESO presents the best performance in rejecting the uncertain external disturbances to the converter. In addition, the proposed SMC-ESO method also shows improved grid current quality compared to the traditional PI-based method. The observed grid current THD with the proposed method is 4.0%, whereas the conventional PI shows 4.7% THD in the generated grid current. Moreover, the proposed controller performances are also evaluated for the grid disturbance conditions. In the test scenarios, the converter DC-bus reference voltage is set to 350 V. The normal condition is suddenly changed

by varying the peak value of the grid voltage from 325 V to 250 V, and from 325 V to 350 V. The measurement results are given in Fig. 4.12. As shown, the generated grid current shows an increment or decrement to compensate those variations on the grid voltage while maintaining the desired DC-bus voltage.

4.5 Conclusion

The major works of this chapter is summarized below:

- A new DC-bus ripple estimation method has been proposed for single-phase grid-connected power converters.
- A filter-less method for eliminating this ripple to estimate the DC value of the bus voltage has been presented, which improves the dynamic performance of the DC-bus voltage controller.
- A robust DC-bus voltage control scheme based on sliding mode controller (SMC) incorporated with an extended state observer (ESO) has been developed to regulate the DC-bus voltage in the presence of external disturbances and system parameter variations.
- The detailed stability analysis of the proposed controller has been presented for a wide range of system parameter variations.
- The effectiveness of the proposed controller has been demonstrated and verified through measurement results on prototypes.

In single-phase AC/DC converters, the main challenge associated with the designing of DC-bus voltage controller is a trade-off between the generated grid current quality and the DC-bus voltage dynamic performance. This trade-off becomes more difficult when the DC-bus ripple voltage is high due to the use of small bus capacitor. This research provides an expression for the DC-bus ripple component and introduces a filter-less method to remove this component from the measured voltage completely. Consequently, it enables the reduction of the grid current distortion and presents fast dynamic performance in regulating the DC-bus voltage during the transient. To improve the dynamic performance during the external disturbances, a robust control approach based on the SMC incorporated with an ESO is proposed as the DC-bus voltage controller. The SMC-ESO control approach presents a

superior dynamic performance under external disturbances compared to the traditional controllers. A predictive controller is employed as the inner current controller that ensures the equal voltages across the DC-bus capacitors and generates five-level voltages in the grid-side.

5 Designing a Robust Grid Parameter Estimation Method for Power Converters

5.1 Introduction

Accurate and fast estimation of grid voltage fundamental parameters is crucial for the robust control of grid-connected power converters. The fundamental parameters of single-phase grid voltage include the amplitude, phase angle, and frequency. These critical pieces of information are often required for different purposes such as measurement, islanding, fault detection, protection, monitoring, and control applications. The grid parameters are usually acquired by a grid synchronization unit [19-23]. This unit plays a significant role in the operation of power converters interfaced into the grid. It is responsible for delivering high-quality power into the grid from renewable energy-based generation systems like grid-connected PV inverters, and providing other ancillary services. The grid synchronization system is also responsible for keeping the smooth connection of the power converter to the grid, especially under grid faults. A robust synchronization method should respond fast and accurately to the common disturbances faced by the equipment interfacing with the electrical grid. The disturbances can be line notching, phase jump, frequency variation, voltage unbalance, line dips, and noises.

Several commonly used synchronization methods have been reported in the literature. All these methods work accurately in extracting the grid voltage parameters under the ideal grid condition. However, in practice, the real-life electrical power system is affected by the presence of various disturbances, which causes the power quality issues. The disturbances include the presence of DC offset, noises (harmonics, subharmonics), line dips, phase jump, frequency variations, and voltage unbalance. These disturbances can be caused by various eventualities such as continuous load changes, power system faults and switching effects, electrical equipment operational faults, resonance phenomena, injected DC currents by grid-connected PV inverters, and nonlinear power electronics-based loads [88, 113-119]. Therefore, the grid voltage parameters cannot be considered as ideal values, and the performance of the synchronization methods are adversely affected by these power system

disturbances. These uncertainties in the power grid cause oscillatory and offset errors in the estimated parameters by the synchronization methods [25, 120, 121].

Several advanced synchronization methods have been reported to mitigate these problems. However, these methods are complex in their structure and suffer from many difficulties such as (1) requiring long computation time, (2) modeling and tuning difficulties, (3) ineffectiveness under wide frequency variations, and (4) implementation difficulty. A brief discussion of the different class of synchronization methods is presented in the following.

The grid synchronization methods employed to control power converters can be primarily classified into two main groups: open-loop methods and closed-loop methods. The open-loop synchronization methods do not require any feedback loop in their structure to work accurately. However, these methods are not popular due to the poor performances at off-nominal frequencies [122-124]. On the other hand, the closed-loop methods require one or more feedback signals in their structures. The estimated phase angle is updated adaptively in the closed-loop structures by using a loop mechanism. It locks the estimated phase angle value to its original phase angle value [123]. The closed-loop synchronization methods can be classified into two main categories, such as phase-locked loops (PLLs) and frequency-locked loops (FLLs). The diagram presented in Fig. 5.1 shows the major classification of the synchronization methods.
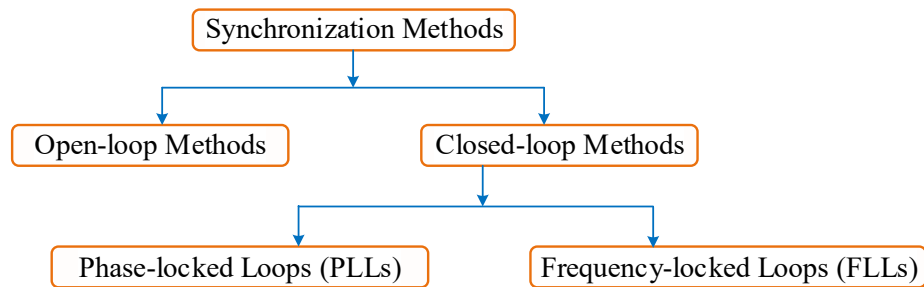
Fig. 5.1 A classification of synchronization methods.

5.1.1 Phase-locked loop (PLL)

A PLL is a closed-loop control system, where a feedback loop is used to control the phase of an internal reference signal to synchronize it with the fundamental component of the grid voltage [119]. Fig. 5.2 illustrates the basic structure of a PLL.
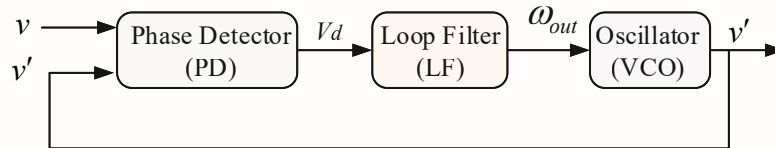
Fig. 5.2 Basic structure of a PLL.

The PLL consists of three basic parts. The first part in their structures is the phase detector (PD). This part generates a phase error signal, which is proportional to the phase difference between the actual input signal and the estimated output signal. The second part is the loop filter (LF). This part shows a low-pass filtering characteristic and makes the phase error signal to zero. The third part is the voltage-controlled oscillator (VCO). This part generates a synchronized output signal. The frequency of the generated signal is shifted according to the known central frequency as a function of the output given by the LF [119, 125, 126].

5.1.2. Single-phase pPLL

In recent years, phase-locked loops (PLLs) have attracted much attention for grid voltage parameter estimation. Several attractive single-phase PLL methods have been reported in the literature. Based on their structures, they can be classified as power-based PLL (pPLL) and quadrature signal generation-based PLL (QSG-PLL) [11]. The main advantage of pPLL methods is their simple structure [127-129]. As a result, the parameter tuning and stability analysis become more straightforward compared to QSG-PLLs [25]. Regardless of their different structures, they have three fundamental blocks, such as a phase detector (PD), a loop filter (LF), and a voltage- controlled oscillator (VCO). The basic functional diagram of a pPLL is illustrated in Fig. 5.3.
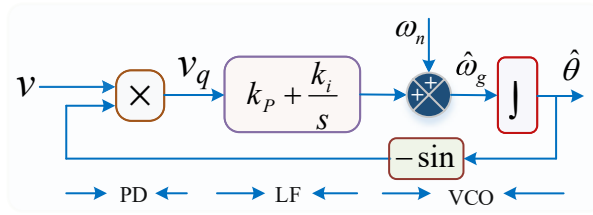
Fig. 5.3 Basic pPLL structure.

Focusing on pPLLs, they have a product-type PD to generate the phase error information [125, 130]. However, the product type PD has a high amplitude double grid-frequency (2ω) ripple component in its output with the phase error information [125, 131]. Many strategies have been suggested to remove this component to estimate the phase error. The main difference among these strategies lies in their filtering methods employed to remove the 2ω component.

Several single-phase low pass filters (LPF) based pPLLs have been reported in the literature. The basic schematic diagram of the LPF-pPLL is illustrated in Fig. 5.4.
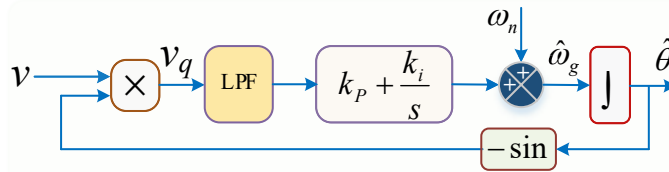
Fig. 5.4 Block diagram of LPFpPLL structure.

In [125], an infinite impulse response (IIR) low-pass filter (LPF) was employed inside the PLL control loop to remove the 2ω ripple. The LPF filter should be designed with a low cutoff frequency in order to remove the low frequency component. However, a low cutoff frequency introduces a high phase delay in the PLL control loop. Consequently, this structure presents slow dynamic behavior during transient conditions. Nevertheless, this method presents a high harmonic filtering capability and noise immunity [25, 132].

Compared to the LPF based filtering methods, the notch filters (NFs) are more suitable to remove a low and specific frequency component without distorting the input signal. Several NF based pPLL structures have been reported in the literature. The basic structure of this PLL type is shown in Fig. 5.5.
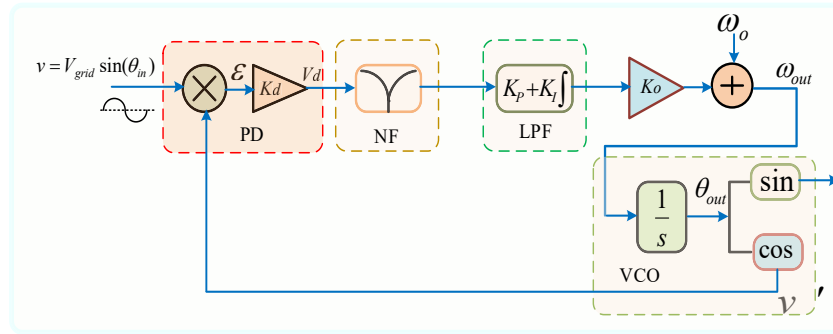
Fig. 5.5 Block diagram of NFpPLL structure.

A simple non-adaptive NF based pPLL (NFpPLL) was suggested in [133]. This PLL causes an oscillatory error in the estimated grid frequency when a large grid frequency variation occurs. To make NFpPLL frequency adaptive for a large frequency variation, a wide bandwidth must be considered during NF design for the complete elimination of the 2ω ripple. The NF with wide bandwidth can effectively remove this ripple. However, it introduces a high phase delay in the PLL control loop, and consequently, degrades the transient performance. To improve the harmonic filtering capability of NF-based PLL, in [134], several NFs were employed in a serial configuration, and in [135], several NFs were engaged in a parallel arrangement. However, the use of multiple NFs in their structures increases implementation complexity. To make the NFpPLL frequency adaptive, an adaptive notch filter (ANF) based pPLL, or ANF-pPLL was presented in [136]. Nevertheless, this technique is sensitive to power system disturbances to estimate the grid frequency, especially when the grid voltage amplitude varies and phase step occurs. In [137], a finite impulse response (FIR) based notch filter (FIR-NF) was reported to remove the 2ω term. The structure of the FIRNF-pPLL is presented in Fig. 5.6.
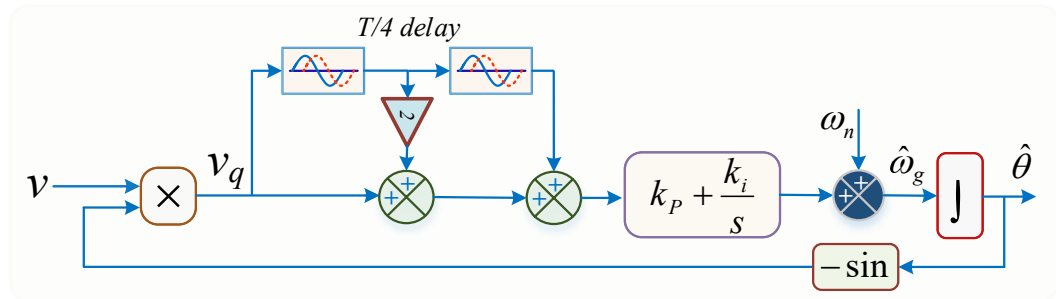
Fig. 5.6 Structure of the FIRNF-pPLL.

This technique yields satisfactory result in blocking the ripple component even when a large frequency variation occurs. However, a wide bandwidth filter design is required to work effectively for a wide frequency range, which results in significant in-loop phase delay, and thus degrades its transient performance. A non-adaptive infinite impulse response (IIR) NF based PLL was reported in [138, 139]. The IIR filter provides better notch capability compared with the FIR filters. The bandwidth (BW) of the IIR-NF must be reduced to have a good double-frequency component blocking capability. However, a wide bandwidth selection is required for the NF where a large frequency variation occurs in the grid frequency. A wide bandwidth filter causes a high phase delay, and therefore, slows the PLL transient response. Numerous pPLLs based on moving average filter (MAF) (MAFpPLLs) have been reported for removing the double grid-frequency component from the PD output [140-143]. The MAF filter behaves as an ideal LPF. The main drawback of the MAF-based PLL methods is the slow transient performance. Moreover, these methods are not frequency adaptive. To make this PLL frequency adaptive, some frequency-adaptive MAF based pPLLs are also developed. The proposed method in [142] adjusts the window length of the MAF filter according to the input signal frequency variation. However, this filter causes a large in-loop phase delay in the control loop, which varies proportionally to the MAF window length. An alternative method was proposed in [140] to achieve frequency adaptability by using adjustable PLL sampling frequency. However, varying sampling increases its implementation complexity.

An adaptive filter based pPLL method was reported in [131]. This method is known as a modified mixer phase detector based pPLL (MMPDpPLL). This technique uses a feedback loop to the phase detector to make the PLL frequency adaptive. Nevertheless, this method requires amplitude normalization to work accurately, which is a difficult task. The structure of the MMPD-pPLL is presented in Fig. 5.7.
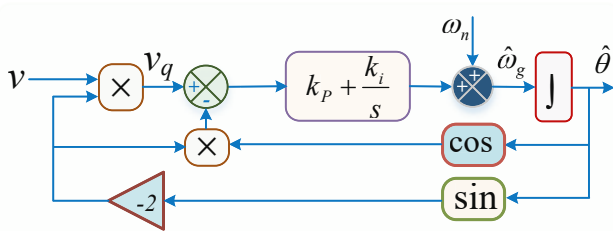
Fig. 5.7 Structure of the MMPD-pPLL.

As mentioned before, the advantage of pPLL methods is their simple structure, and thus, the parameter tuning and analysis becomes more straightforward compared to other PLL families [25]. However, the main disadvantage of the pPLLs is that these methods do not provide any knowledge about the grid voltage amplitude. Moreover, these methods suffer from oscillatory error in the estimated grid frequency at off-nominal frequencies. Since pPLLs do not provide the information about the grid voltage amplitude, it is not possible to make PLL dynamics decoupled from the grid voltage amplitude changes [25].

Some other common drawbacks of the pPLL methods are the frequency adaptability problem at off-nominal frequencies and slow transient performances under adverse grid conditions. For these reasons, the pPLLs have not received much attention. To take advantage of the simple structure of the pPLL with easy parameter tuning and straightforward analysis, addressing the shortcomings of the pPLL structure has become the main motivation behind developing more advanced pPLL. This research proposes a new pPLL structure as a solution to such problems including estimation of grid voltage amplitude. A modified weighted-frequency Fourier linear combiner (MWFLC) algorithm is used inside the pPLL control loop for eliminating the 2ω ripple, estimating the grid frequency and voltage amplitude. The proposed algorithm provides an accurate estimation of these parameters even under adverse grid conditions. Experimental studies are conducted to validate the proposed MWFLC-pPLL.

5.2 Proposed PLL Structure

This section covers the demonstration of the proposed PLL method. The proposed PLL employs a modified WFLC algorithm in the output of PD, which is used to extract the phase error information from the high amplitude 2ω ripple component. In addition to removing this ripple, the proposed algorithm also estimates the amplitude and frequency of the input signal. The block diagram of the PLL is illustrated in Fig. 5.8. In this structure, the phase angle of the input signal is directly estimated by the PLL, whereas the amplitude and frequency are calculated indirectly by the employed algorithm. The fundamental of the proposed algorithm is the Fourier linear combiner (FLC) algorithm, which acts as a non-adaptive notch filter (NF). The use of FLC filter presents an enhanced performance in removing a specific frequency

component compared to the NF [144]. To provide frequency flexibility, Riviere and Thakor developed a frequency adaptive FLC, which is also known as weighted-frequency Fourier linear combiner (WFLC) [145]. The frequency adaption is achieved based on the weighted least squares estimation (WLSE) method. Notice that both FLC and WFLC algorithms are based on the least mean square (LMS) algorithm [146]. The WFLC filter has been used for tremor cancelation in microsurgery [144]. In this work, a modified WFLC is used to improve the pPLL performance including its capability to estimate the input signal amplitude. The MWFLC controls the notch frequency and the notch depth to block the 2ω ripple completely even at off-nominal grid frequencies. It behaves as a zero-phase time-varying adaptive notch/band-stop filter. In the proposed structure, the unknown grid voltage amplitude is estimated by the modified algorithm. Before demonstrating the proposed method, a basic understanding of the FLC algorithm is presented as follows.
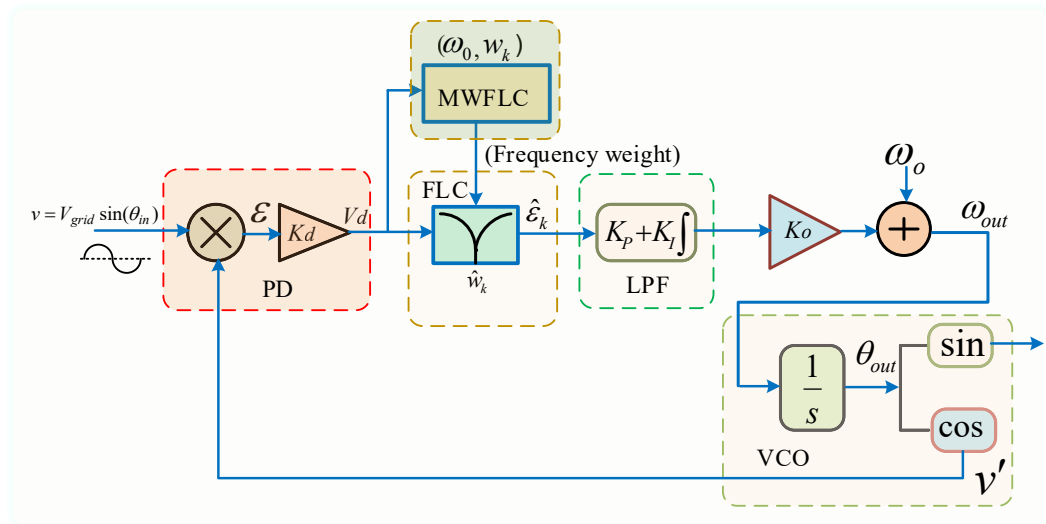
Fig. 5.8 Proposed MWFLC-pPLL structure.

5.2.1 Fourier Linear Combiner

The FLC algorithm is an adaptive filter and consists of an infinite null. It can effectively eliminate any known frequency component from the input signal. It is also computationally inexpensive. The FLC algorithm adjusts to the phase and amplitude of an oscillation

component in the input signal and tracks any changes. This algorithm generates a dynamic truncated Fourier series model of an input signal [144, 147].

The series model can be expressed as

$$y_k = \sum_{r=1}^{M} \left[a_r \sin(r\omega_c k) + b_r \cos(r\omega_c k) \right] \tag{5.1}$$

where a_r and b_r are the adapter filter weights.

The FLC is based on the LMS algorithm and operates by tracking the Fourier coefficients.
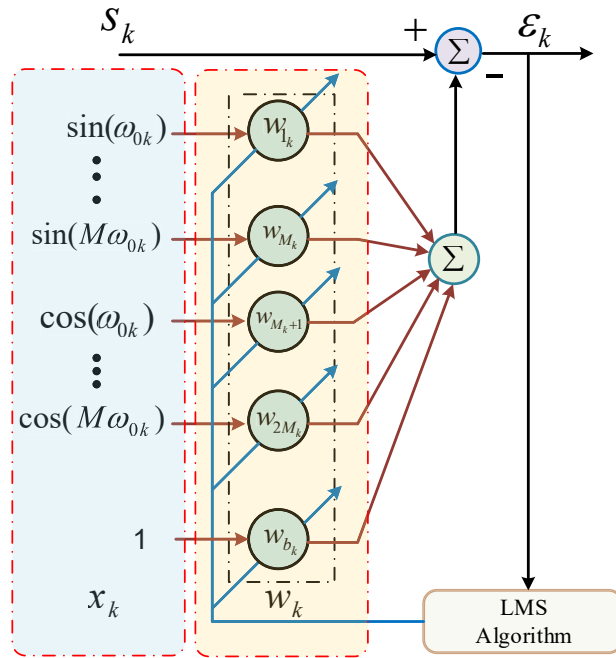
Fig. 5.9 Block diagram of the Fourier linear combiner.

Fig. 5.9 illustrates the block diagram of FLC, which can be represented by the algorithm as the following [148]

$$x_{r_k} = \begin{cases} \sin(r\omega_c k), & 1 \le r \le M \\ \cos[(r-M)\omega_c k], & M+1 \le r \le 2M \end{cases} \tag{5.2}$$

$$\varepsilon_k = s_k - w_k^T x_k \tag{5.3}$$

$$w_{k+1} = w_k + 2\mu x_k \varepsilon_k \tag{5.4}$$

where s_k is the input signal, $w_k = \left[w_{1_k}, w_{2_k}, \ldots, w_{2M_k} \right]^T$ the adaptive weight vector that generates harmonic orthogonal sinusoidal components, μ an adaptive gain parameter, and M the number of harmonics in the model.

The FLC algorithm can be considered as an ANF for $M = 1$, and the width of the notch generated at ω_c is proportional to μ [144, 148]. The FLC can effectively remove the 2ω ripple from the PD output of pPLL if the grid frequency does not vary. However, at off-nominal frequencies, this filter cannot effectively extract the phase error information from the 2ω component. As a result, an oscillatory error is observed in the estimated grid frequency by the PLL. Suppression of the ripple using FLC algorithm requires an accurate estimation of the ripple frequency. Therefore, to make the FLC for suppressing the 2ω ripple requires modification in the algorithm to adapt the variations at the grid signal frequency.

5.2.2 Modified Weighted-Frequency Fourier Linear Combiner

This section present the proposed algorithm. As mentioned before, complete elimination of the ripple from PD by FLC requires an adaption to the input signal frequency. To provide the frequency flexibility in FLC, an adaptive weight ω_{ok} was introduced in the WFLC algorithm by Riviere and Thakor. The block diagram of WFLC is illustrated in Fig. 5.10 [148]. The WFLC acquires the input signal frequency by using the LMS algorithm, whereas the FLC weights acquire the input signal amplitudes. In the proposed PLL, the WFLC acts as a self-adaptive notch filter which tracks the input signal frequency changes during grid frequency drift and adjusts the notch to block the 2ω ripple from the PD. As discussed earlier, the pPLLs cannot estimate the input signal amplitude, which is the major problem of these methods. Therefore, to acquire the input signal amplitude, the WFLC algorithm is modified in the proposed PLL structure. The simplified block diagram of the proposed modified WFLC algorithm is illustrated in Fig. 5.11. The modification of the algorithm in achieving the required flexibility for varying grid frequency and estimating the grid voltage amplitude is presented below.
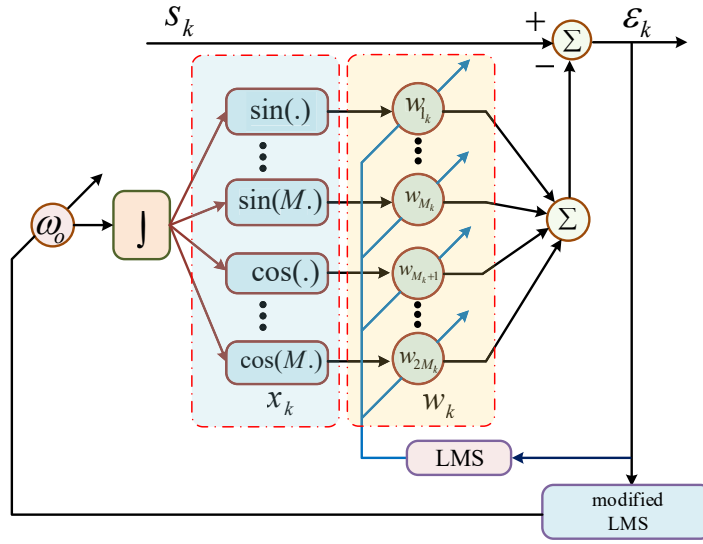
Fig. 5.10 Block diagram of the weighted-frequency Fourier linear combiner.
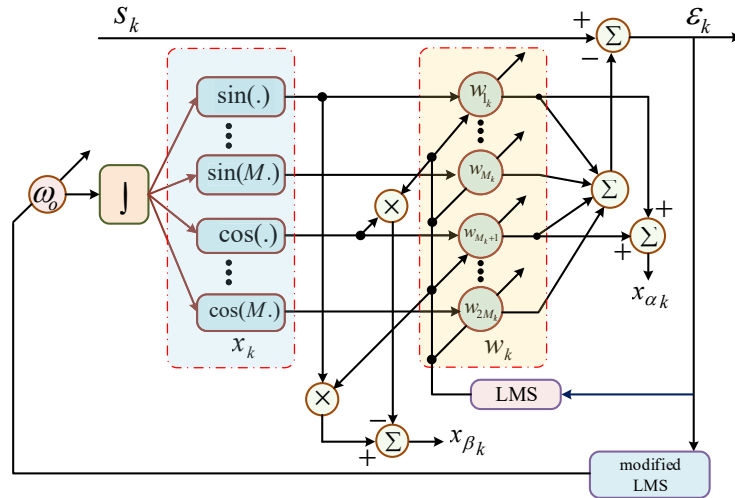
Fig. 5.11 Block diagram of the proposed MWFLC for n=1.

The fixed frequency ω_c of the FLC is modified by including an adaptive weight ω_{ok} [144, 148]. Therefore, (5.3) can be rewritten as

$$\varepsilon_k = s_k - \sum_{r=1}^{M}[\omega_{rk}\sin(r\omega_{0k}k) + \omega_{r+Mk}\cos(r\omega_{0k}k)] \tag{5.5}$$

An adaptive recursion for ω_{ok} is built using the modified LMS algorithm as

$$\omega_{0_{k+1}} = \omega_{0_k} - 2\mu_0\varepsilon_k\frac{\partial e_k}{\partial \omega_{ok}} \tag{5.6}$$

From (5.5) and (5.6), we have

$$\frac{\partial e_k}{\partial \omega_{ok}} = -k \sum_{r=1}^{M} r \left[\omega_{rk} \cos(r\omega_{0k}k) - \omega_{r+Mk} \sin(r\omega_{0k}k) \right] \tag{5.7}$$

Since the leading time index k in (5.7) affects the magnitude, it must be removed for the sake of stability. The sinusoidal arguments ω_{ok} are changed according to the running sums suitable to frequency modulation [148]. Therefore, to make ω_{ok} adaptive by using its own gain, μ_o, the frequency recursion of WFLC is given as

$$\frac{\partial e_k}{\partial \omega_{ok}} = -k \sum_{r=1}^{M} r \left[\omega_{rk} \cos\left(r \sum_{t=1}^{k} w_{0_t} \right) - \omega_{r+Mk} \sin\left(r \sum_{t=1}^{k} w_{0_t} \right) \right] \tag{5.8}$$

The adaptive weight ω_{ok} can be expressed by using its own gain μ_o and thus, it can provide the frequency recursion of WFLC as [144]

$$x_{r_k} = \begin{cases} \sin\left(r \sum_{t=1}^{k} \omega_{0_t} \right), & 1 \le r \le M \\ \cos\left(\sum_{t=1}^{k} \omega_{0_t} \right), & M+1 \le r \le 2M \end{cases} \tag{5.9}$$

$$\varepsilon_k = s_k - w_k^T x_k \tag{5.10}$$

$$\omega_{0_{k+1}} = \omega_{0_k} + 2\mu_0 \varepsilon_k \sum_{r=1}^{M} r \left(\omega_{r_k} x_{M+r_k} - \omega_{M+r_k} x_{r_k} \right) \tag{5.11}$$

The 2ω ripple component amplitude can then be tracked by using the adaptive weight as

$$w_{k+1} = w_k + 2\mu x_k \varepsilon_k \tag{5.12}$$

where μ is the adaptive gain, and x_{r_k} denotes the rth element of the vector x_k.

The double harmonic ripple frequency is estimated by an adaptive weight vector ω_{ok}. The error is calculated between the reference sine wave and the harmonic component at every step, and then the frequency and amplitude of the reference signal are changed accordingly. A second set $\hat{w}_k$ of amplitude weights operate on the input signal s_k by using the input signal frequency information learned from the reference vector x_k and perform the zero-phase ripple canceling. The proposed second harmonic ripple filtering system can be presented as a WFLC and FLC algorithm combination, as given by

$$\hat{s}_k = nw_{k+1} x_{k+1} + nw_k x_k \tag{5.13}$$

$$\hat{\varepsilon}_k = \hat{s}_k - \hat{w}_{1_k}^T x_{1_k} \tag{5.14}$$

$$\hat{w}_{1_{k+1}} = \hat{w}_{1_k} + 2\hat{\mu}x_{1_k}\hat{\varepsilon}_k \tag{5.15}$$

The overall system removes the double frequency ripple term from the PD of the proposed pPLL structure like an adaptive notch filtering approach that tracks any variations in the ripple frequency when the grid frequency variation happens. In the proposed method, the grid voltage amplitude is estimated by a new algorithm, as given by

$$\hat{x}_{\alpha_k} = \hat{w}_{1_k} x_{1_k} + \hat{w}_{2_k} x_{2_k} \tag{5.16}$$

$$\hat{x}_{\beta_k} = \hat{w}_{2_k} x_{1_k} - \hat{w}_{1_k} x_{2_k} \tag{5.17}$$

$$\hat{V}_{p_k} = 2\sqrt{\hat{x}_{\alpha_k}^2 + \hat{x}_{\beta_k}^2} \tag{5.18}$$

The expression of the estimated grid signal frequency can be obtained from (5.11) as the following

$$\omega_g = \frac{1}{2}\left(\omega_{0_k} + 2\mu_0\varepsilon_k\sum_{r=1}^{M} r\left(\omega_{r_k} x_{M+r_k} - \omega_{M+r_k} x_{r_k}\right)\right) \tag{5.19}$$

5.3 Small-Signal Modelling and Stability Analysis of the Proposed PLL Method

To analyze the dynamics of the proposed PLL, the detailed small signal modelling and stability analysis are presented in this section. A PI-controller is considered as the LPF in this structure. The measured grid voltage signal can be presented by the following expression

$$v_i(t) = V_1\sin(\omega_i t + \theta_1) + V_3\sin(3\omega_i t + \theta_3) + \cdots \tag{5.20}$$

where v_n and θ_n (n = 1, 3, 5, . . .) are the input signal amplitude and phase angle of the n_{th} harmonic component, respectively, and ω is the angular frequency.

The PD multiplies the VCO output by the measured input signal. Therefore, the input of the MWFLC block can be expressed as

$$v_i(t) \times \cos(\omega_o t + \theta_o) = \frac{1}{2}V_1 \sin(\omega_i t + \theta_1 - \omega_o t - \theta_o) + \frac{1}{2}V_1 \sin(\omega_i t + \theta_1 + \omega_o t + \theta_o) + f(2\omega_i, 4\omega_i, 6\omega_i, \cdots)$$

$$(5.21)$$

Note that the output of PD has the locking error information. However, this information is not linear. The system can be linearized by considering that the proposed PLL is locked during the steady-state condition (i.e. when $\theta_1 = \theta_0$ and $\omega_i = \omega_0$). Thus, (5.21) can be rewritten as

$$v_i(t) \times \cos(\omega_o t + \theta_o) \approx \frac{1}{2}V_1 \sin(\theta_1 - \theta_o) + \frac{1}{2}V_1 \sin(2\omega_i t + 2\theta_1) + f(2\omega_i, 4\omega_i, 6\omega_i, \cdots) \quad (5.22)$$

For small values of θ, $\sin(\theta) = \theta$, or $(\theta_i - \theta_0 \approx \theta_e)$. Therefore, (5.22) can be approximated as

$$v_i(t) \times \cos(\omega_o t + \theta_o) \approx \frac{1}{2}V_1 \theta_e + \frac{1}{2}V_1 \sin(2\omega_i t + 2\theta_1) + f(2\omega_i, 4\omega_i, 6\omega_i, \cdots) \quad (5.23)$$

The small-signal model of the proposed PLL can be obtained from (5.23) and Fig. 5.8, as shown in Fig. 5.12. The signal flow diagram of the FLC is illustrated in Fig. 5.13 [144]. The control parameter tuning of the proposed system is obtained in the z-domain as the proposed method is realized in a discrete device. The transfer function of the FLC system for the path $y_k = 2\mu u(k-1)\cos(k\omega_o)$ in Fig. 5.13 is presented in the z domain as [144]

$$G(z) = 2\mu \frac{z^2 - z\cos\omega_0}{z^2 - 2z\cos\omega_0 + 1} - 2\mu \quad (5.24)$$

After simplification, (5.24) can be rewritten as

$$G(z) = \left[\frac{2\mu z \cos\omega_0 - 2\mu}{z^2 - 2z\cos\omega_0 + 1} \right] \quad (5.25)$$
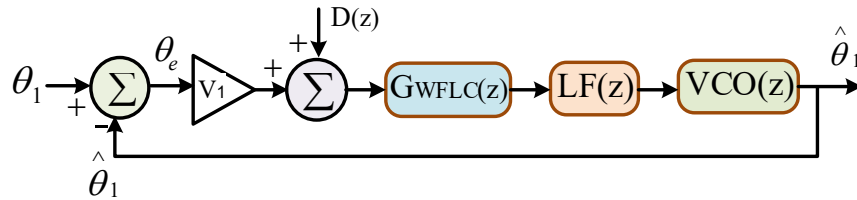
Fig. 5.12 Small-signal model of the WFLCPLL method.
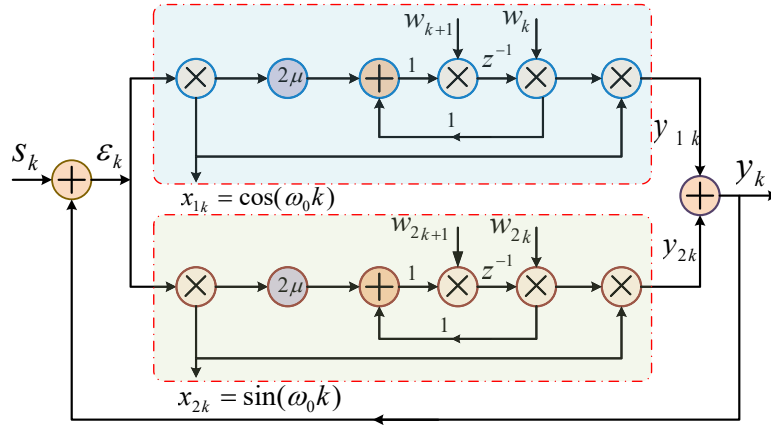
Fig. 5.13 Signal flow diagram presenting signal propagation in FLC.

Since it has a feedback loop, the feedback formula can be given by [144]

$$H(z) = \frac{z^2 - 2z\cos\omega_0 + 1}{z^2 - 2\mu z\cos\omega_0 - 2\mu - 1} \tag{5.26}$$

The linearization process of the proposed MWFLC-PLL method is similar to that of the standard pPLL method. The transfer function of the equivalent linear MWFLC-pPLL system can be expressed as

$$H_m(z) = \frac{255.4z - 254.6}{z - 1} \times \frac{z^2 - 2z\cos\omega_0 + 1}{z^2 - 2\mu z\cos\omega_0 - 2\mu - 1} \times \frac{0.00004}{z - 1} \tag{5.27}$$

The frequency response of the MWFLC-pPLL is presented in Fig. 5.14. The detailed parameter tuning procedure of the proposed PLL is described in the following section. With the designed PLL parameters, a phase margin of 62.33° and a gain margin of 18.96 dB can be obtained, which can guarantee the stability of the proposed PLL. The transient responses of the actual MWFLC-pPLL and the derived model are also compared to verify the accuracy of the derived small-signal model. The numerical analysis shows the responses, as shown in Fig. 5.15, under a +10° phase jump and a +2 Hz frequency step, which verifies the equivalence numerically, and thus confirms the validity of the derived small-signal model.
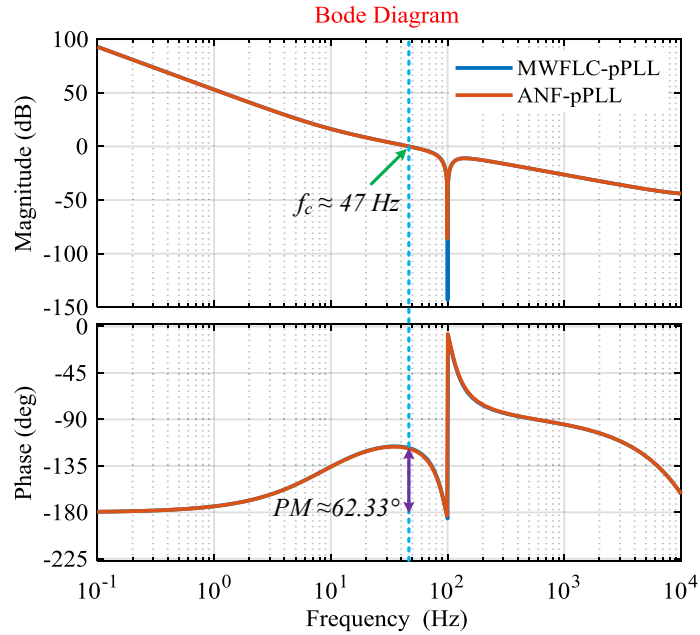
Fig. 5.14 Bode plot of open-loop transfer function (5.27) and (5.30), ($Ts = 0.00004$ s, $\mu = 0.006$, $k_p = 255$, and $k_i = 20000$).
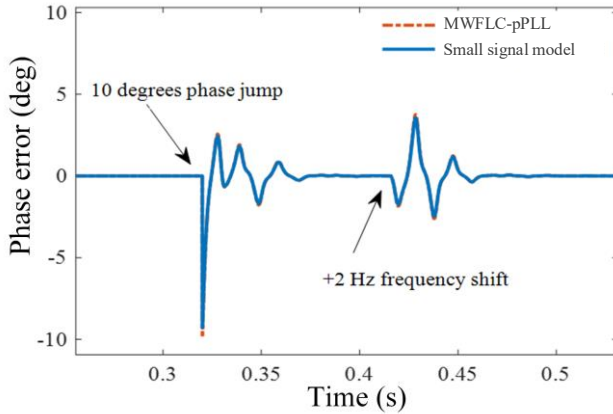
Fig. 5.15 Accuracy assessment of the proposed PLL with sampling period $T_s = 0.00004$ s, $\mu = 0.006$, $k_p = 255$, and $k_i = 20000$, when a +10° phase jump and a +2 Hz frequency shift occur.

5.4 Design Example of the Proposed Method

This section describes the proposed PLL design methodology, parameter tuning procedure, and designing a platform to provide a fair comparison with an advanced pPLL

version. By inspecting the open loop Bode plot, the parameter μ is set to 0.006 to achieve fast transient performances, as well as damped. The values of the PI filter coefficients (k_p and k_I) are set to 255 and 20000, respectively, by inspecting the Bode plot for realizing good performance in terms of the speed of convergence, smaller overshoot, higher stability margin, and filtering performance. With this selection, a phase margin of 62.33° and a gain margin of 18.96 dB are obtained, which implies that the designed parameters offer a smooth dynamic performance of the proposed PLL. As shown in the figure, the notch depth of the MWFLC-pPLL is 149.20 dB, which results in complete rejection capability of the 2ω ripple from the PD in steady-state.

Since the MWFLC filter behaves like an adaptive notch filter, the performance comparison has been carried out with the ANF-pPLL method. Moreover, the ANF-pPLL shows satisfactory performance for a wide grid frequency variation and provides good transient performance during grid disturbances. The structure of the conventional ANF consists of a NF with an additional frequency estimation loop [136]. The dynamic behavior of the standard ANF is characterized by the following set of differential equations [27]

$$\ddot{x} + \theta^2 x = 2\zeta\theta(y(t) - \dot{x}) \tag{5.28}$$

$$\dot{\theta} = -\gamma x\theta(y(t) - \dot{x}) \tag{5.29}$$

where $y(t)$ is the input signal, θ the estimated second harmonic frequency, ζ the damping ratio that determines the depth of the notch, and γ the adaptation gain. The parameters of the ANF are set to $\zeta = 0.5$, and $\gamma = 1 \times 10^6$.

The open loop transfer function of the notch filter based pPLL can be obtained as

$$H_n(z) = \frac{255.4z - 254.6}{z - 1} \times \frac{z^2 - 1.999z + 1}{z^2 - 1.987z + 0.9875} \times \frac{0.00004}{z - 1} \tag{5.30}$$

As mentioned before, the design parameter μ of the proposed method is set to 0.006. Therefore, the value of the ζ of notch filter should be selected to have similar crossover response to provide a base for comparison. Fig. 5.14 shows the $H_m(z)$ and $H_n(z)$ frequency responses. It can be observed from the open loop Bode plot that they have a close crossover response. The obtained phase margin of the proposed and notch filter based pPLL are 62.33°,

61.83°, respectively. Thus, it denotes that the parameter selection for both PLLs provides a fair comparison. The obtained notch depth of the proposed and the notch filter based PLLs are 149.20 dB, 85.90 dB, respectively. It implies that the proposed method has the higher ripple cancellation capability than the notch filter based method in steady state.

The PLL parameters can be calculated by using the linear control design relation [149] and inspecting the frequency response. The settling time t_s can be estimated from the cutoff frequency f_c and the phase margin (PM) by using the following expression

$$t_s \approx \frac{100}{P_m \cdot f_c} \tag{5.31}$$

where the value of f_c is 47 Hz, which is obtained with the assigned PLL parameters.

5.5 Experimental Results

This section demonstrates the proposed PLL performance in estimating the grid voltage parameters under different grid scenarios. The detailed performance comparison with the ANF-pPLL is also provided to highlight its superior dynamic performance. The PLL algorithms have been implemented in a 32-bit floating point DSP chip (TMS320F28379D). Experimental studies have been conducted considering a sampling frequency of 25 kHz. The main advantage of the proposed PLL is the grid voltage amplitude estimation capability. Several grid scenarios are also generated to evaluate their performance to estimate the grid voltage amplitude.
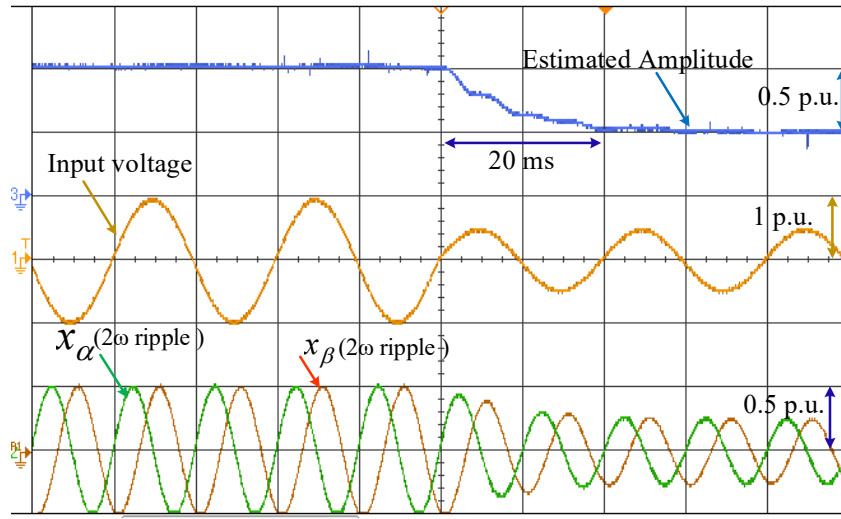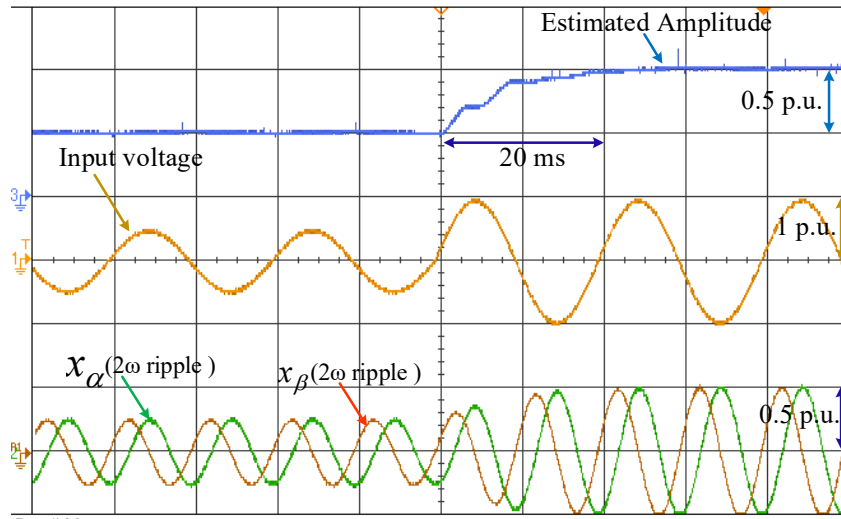
Fig. 5.16 Estimated input voltage amplitude in response to: (a) 50% voltage sag condition, and (b) when the input voltage is changed back to the nominal value.

Fig. 5.16(a) and Fig. 5.16(b) show the obtained results in response to 50% input voltage sag, and when the input voltage is changed back to the nominal value. It can be observed that the proposed method could accurately estimate the grid voltage amplitude and provide fast transient performance during grid voltage amplitude variations. As shown, it requires only one grid cycle (20 ms) to estimate the grid voltage amplitude during these transient conditions.

100
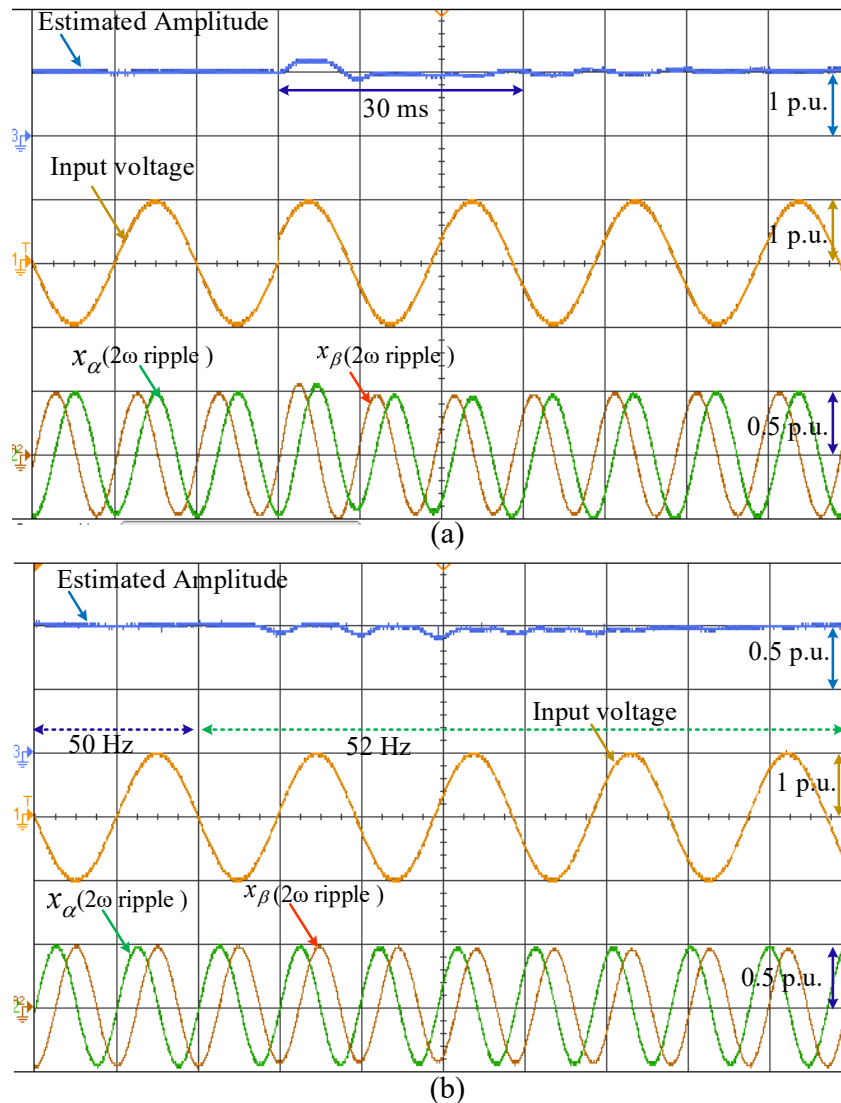
Fig. 5.17 Estimated input voltage amplitude in response to: (a) 20° phase jump condition, and (b) +2 Hz frequency jump condition.

Fig. 5.17(a) and Fig. 5.17(b) show the obtained results in response to 20° phase step and +2 Hz frequency jump, respectively. The proposed method precisely estimates the grid voltage amplitude, and requires 30 ms and 50 ms, respectively to obtain zero steady-state error during these transient cases. From the dynamic performance point of view, it can be concluded that the proposed method shows fast response to estimate the grid voltage amplitude. The frequency estimation capability of the proposed method has also been evaluated under distorted grid conditions and compared with the conventional ANF-pPLL method.
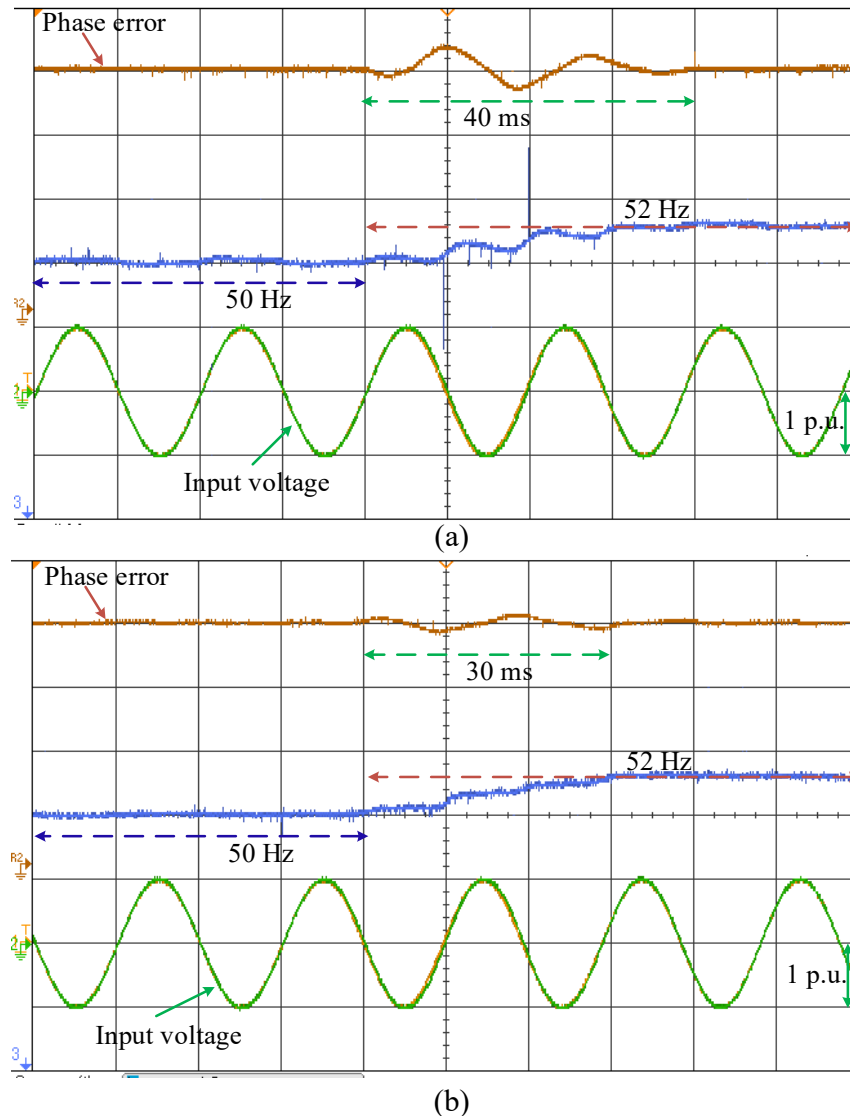
Fig. 5.18 Performance comparison between the MWFLC-pPLL and ANF-pPLL in response to +2 Hz frequency jump, (a) MWFLC-pPLL, and (b) ANF-pPLL.

Fig. 5.18(a) and (b) show the responses with the proposed and conventional methods, respectively, for a +2 Hz frequency jump of the grid voltage. It can be seen that the proposed method can accurately estimate the grid frequency during this transient condition, and the transient lasted for 30 ms, whereas for the ANF-pPLL the transient lasted for 40 ms (two grid cycles). Fig. 5.19(a) and Fig. 5.19(b) show the obtained results corresponding to 90° phase step in the input voltage. As can be seen, the proposed method achieved faster transient

performance in estimating the grid frequency in comparison to the traditional method. Fig. 5.20(a) and Fig. 5.20(b) demonstrate the performance of the PLLs in estimating the grid frequency for 50% voltage sag.

(a)

(b)
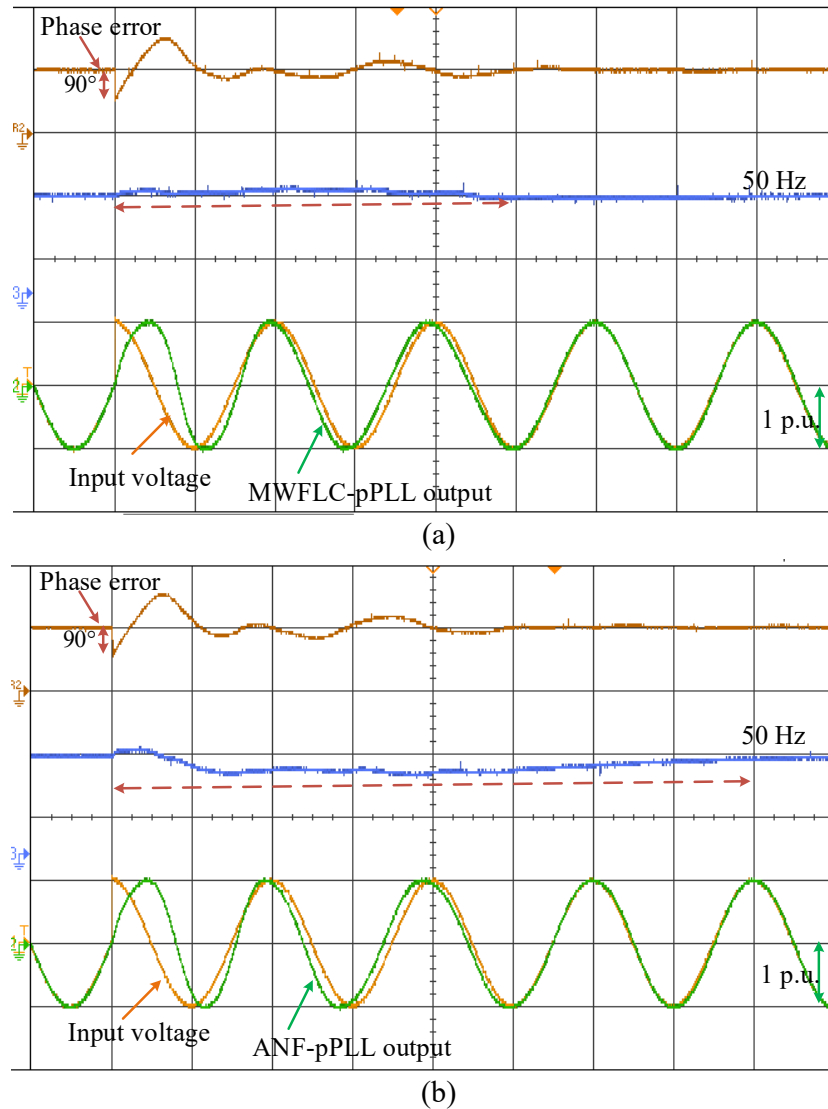
Fig. 5.19 Performance comparison between the MWFLC-pPLL and ANF-pPLL in response to 90° phase jump condition, (a) MWFLC-pPLL, and (b) ANF-pPLL.

The obtained results show that the proposed method presents a better performance in estimating the grid frequency from the dynamic performance point of view. The settling time of the proposed method is less than 20 ms, while the estimated frequency with the ANF-pPLL shows longer transient time (70 ms).
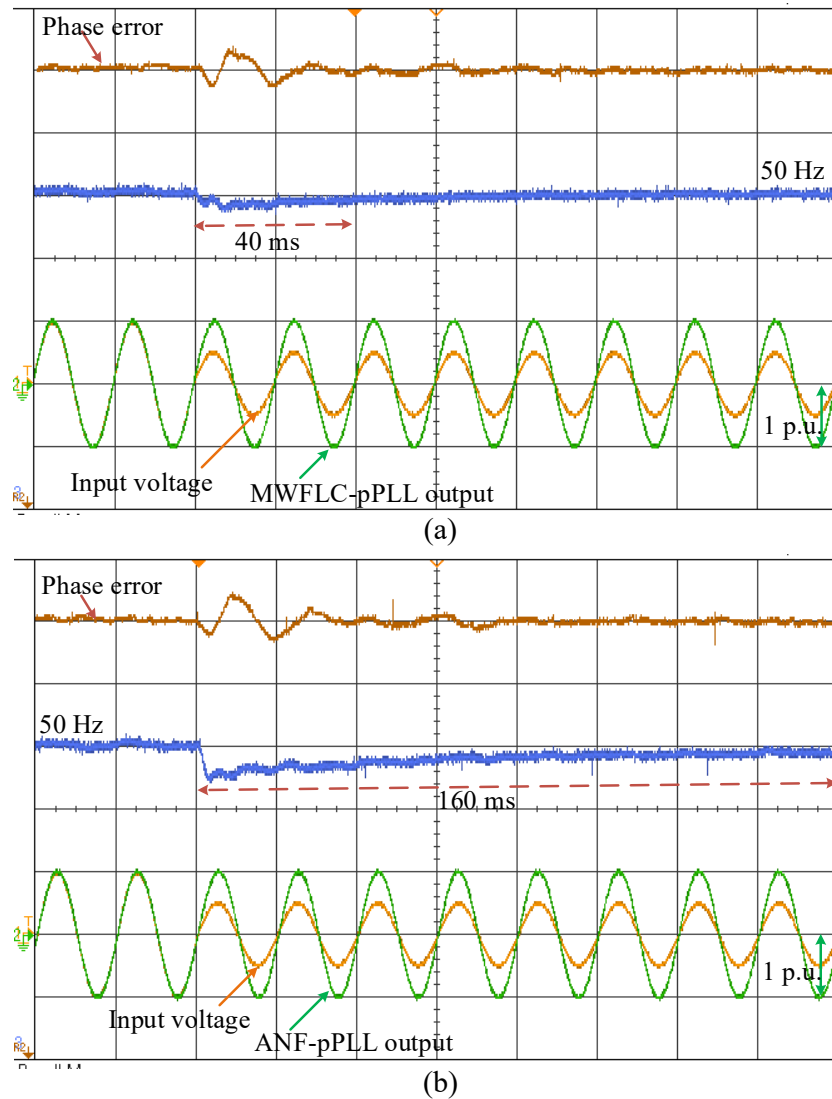
Fig. 5.20 Performance comparison between the MWFLC-pPLL and ANF-pPLL in response to 50% voltage sag condition, (a) MWFLC-pPLL, and (b) ANF-pPLL.

Finally, considering the input signal with significant harmonics (10% third harmonic and 5% fifth harmonic), both PLLs can provide similar harmonic elimination robustness to estimate the grid information, as shown in Fig. 5.21. The performance is similar due to the use of the same loop filter inside the PLLs control loop.
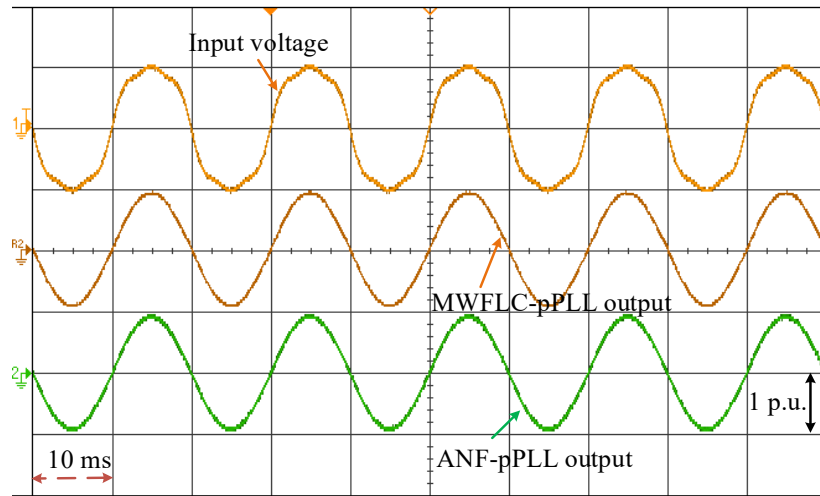
Fig. 5.21 Performance comparison between the MWFLC-pPLL and ANF-pPLL in response to harmonically-distorted grid condition (10% third harmonic and 5% fifth harmonic).

5.6 Conclusion

The major works of this chapter is summarized below.

- A new frequency adaptive pPLL structure has been proposed for single-phase grid-connected applications.
- The proposed MWFLC-pPLL technique is capable of estimating the grid voltage amplitude.
- It can estimate the grid parameters at off-nominal frequencies.
- This method presents a faster dynamic performance under distorted grid conditions than the traditional ANF-pPLL method.
- Experimental results have been presented and compared with the traditional ANF-pPLL method.

A new pPLL structure which is capable of estimating the grid voltage amplitude is proposed in this project. This PLL has shown superior dynamic performance in estimating the grid frequency under adverse grid conditions. The proposed structure employs an MWFLC filter to remove the 2ω ripple component from the PD. This filter functions as a self-adaptive notch filter which can completely remove the large 2ω component from the PD even when a large grid frequency variation occurs. The adopted filter can track the variation of the input signal frequency during a grid frequency variation and adjust the notch to block the 2ω

ripple from the PD. In this proposed structure, the phase angle of the input signal is directly estimated by the pPLL, whereas the amplitude and frequency are calculated indirectly from the PD output signal by using the modified algorithm. This method does not require any feedback loop to make its frequency adaptive. As a result, it offers enhanced stability. The proposed method can provide higher immunity to power system disturbances to estimate the frequency, especially during the grid voltage amplitude variation and phase step conditions, than the traditional methods. The detailed small-signal modeling and stability studies are presented, together with experimental results, to validate the robustness. The advancement of the MWFLC-pPLL is also compared with the conventional methods to highlight its advantages.

6   Modeling, Analysis, and Design of a QSG-PLL Method for Power Converters

6.1 Introduction

Single-phase voltage source converters (VSCs) are generally used as the grid-side converters to integrate DC-bus microgrid, energy storages (ESs), renewable energy sources (RESs), and electric vehicles (EVs) into the distribution grid [11, 85]. Integration of these components into the grid must follow the international standards. For example, the grid-side converters must limit the DC-current injection and harmonics. According to IEEE and IEC standards, the injected DC-current must be less than 0.5% (IEEE 1547-2003 [150]) and 1% (IEC61727 [151]), respectively, of the nominal current of the VSCs. To meet these requirements, the control unit of the converters requires the fast and accurate estimation of the grid voltage fundamental parameters. Therefore, the controller requires a robust grid synchronization method to acquire the grid voltage parameters. Among the different categories of the synchronization methods, the quadrature signal generation (QSG) based PLLs are the most widely used methods in the area of grid-connected power converters applications.

The QSG-PLLs are single-phase version of the conventional synchronous reference frame (SRF-PLL) [26, 119]. Most of the QSG-PLLs generate a quadrature (β-axis) signal from the input single-phase voltage signal. This fictitious signal can be used to calculate the active and reactive powers, sequence components in three-phase systems, and estimate the amplitude of the sinusoidal voltage and current signals. Therefore, the QSG-PLLs have achieved more attention than the other PLL categories [25, 26]. The quadrature signal of the single-phase voltage can be generated in different ways such as transfer delay, second-order generalized integrator (SOGI), all-pass filter, inverse Park transformation (IPT), SRF-MAF, Hilbert transform, and differentiator [25, 125, 152-161]. The main difference among the single-phase QSG-PLLs lies in their different QSG methods. The SOGI-based QSG method may be the most popular method among all the QSGs, which is also the main component of the most frequency locked loops (FLLs).

Most QSGs can accurately generate the fundamental and quadrature components of the grid voltage as long as the grid is in the ideal condition (e.g., the grid frequency is always fixed and not polluted by harmonic, subharmonics, and DC component). Nevertheless, this perfect situation of the electrical grid may not always exist, particularly in microgrids and distribution systems [26]. The QSGs require accurate estimation of the grid frequency to generate the fundamental and its quadrature component. The grid voltage can be polluted by harmonics, inter-harmonics, and DC-offset. Most QSGs do not provide sufficient filtering of these components and thus suffer from oscillatory error in the estimated quantities. A brief description of some QSG-PLLs is provided in the following.

6.1.1 Single-Phase QSG-PLLs

The single-phase QSG-PLLs are the single-phase version of the standard three-phase synchronous reference frame (SRF) SRF-PLL [25]. The structure of the basic SRF-PLL is illustrated in Fig. 6.1.
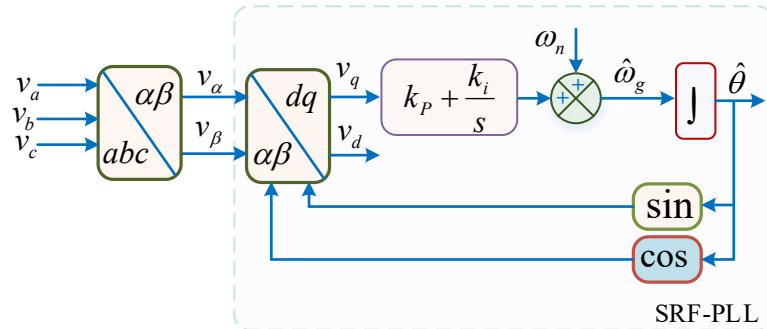
Fig. 6.1 Standard structure of the SRF-PLL.

A large number of advanced QSG-PLLs have been reported in recent literature. The detailed description of some QSG-PLLs will be presented in the following.

A. Standard transfer delay (TD) TD-PLL

The standard form of QSG-PLL is the transfer delay (TD) PLL. The structure of the TD-PLL is illustrated in Fig. 6.2. In this structure, the quadrature signal is generated by delaying the input signal by T/4, where T is the grid frequency fundamental period. This technique may be the easiest technique to generate the quadrature signal. This method works effectively if the grid voltage is in ideal condition with the nominal grid frequency. The limitation of the

standard TD-PLL is that the delayed signal is not orthogonal at off-nominal frequencies. At off-nominal frequencies, this structure generates double frequency and offset error in the estimated grid parameters. Moreover, this method does not provide any filtering of the input signal. Therefore, if the grid voltage contains any harmonics or subharmonics, the *T/4* delay block will not be able to generate the orthogonal signals of each frequency component [119].
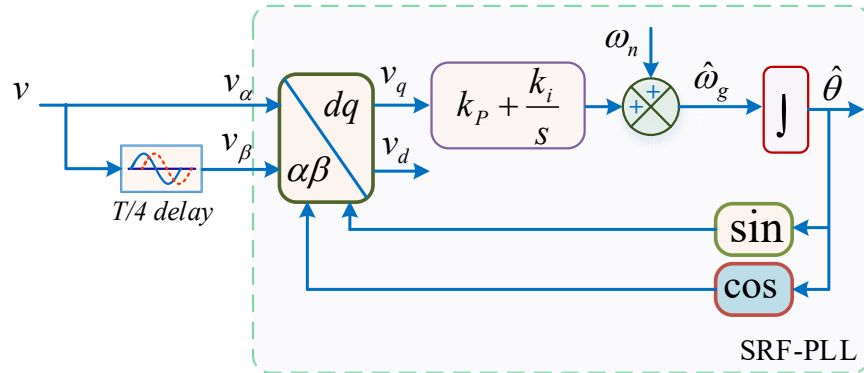
Fig. 6.2 Structure of the standard TD-PLL.

Several advanced PLL structures have been reported in the recent literature to overcome the limitations of the standard TD-PLL [119].

B. Non-Frequency Dependent TD-PLL (NTD-PLL)

To overcome the limitation of the TD-PLL, a non-frequency dependent TD-PLL (NTD-PLL) method is suggested in [162, 163]. The schematic diagram of the structure is shown in Fig. 6.3. In this method, a non-orthogonal signal is generated between the estimated sine term and the cosine term of the Park's transformation at off-nominal frequency, which is used to overcome the phase offset error. Nevertheless, this PLL structure cannot eliminate the double-frequency problem of the TD-PLL.
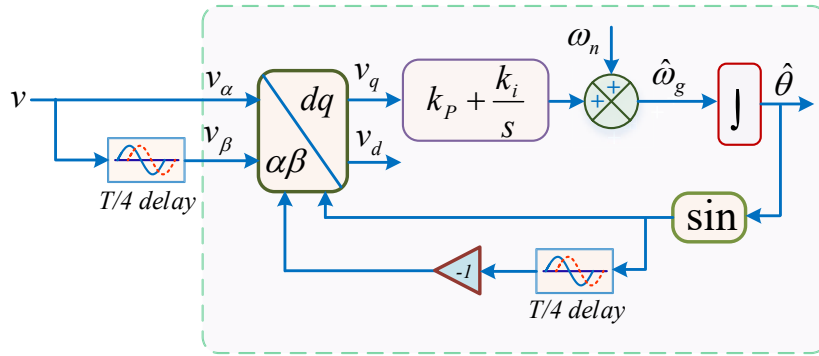
Fig. 6.3 Structure of the NTD-PLL.

C. Inverse Park Transformation-Based PLLs (IPT-PLLs)

The structure of the IPT-PLL is shown in Fig. 6.4. This method is popular and widely used in single-phase applications. In this structure, the IPT is introduced to the filtered dq-axis components to generate the fictitious orthogonal component [119].
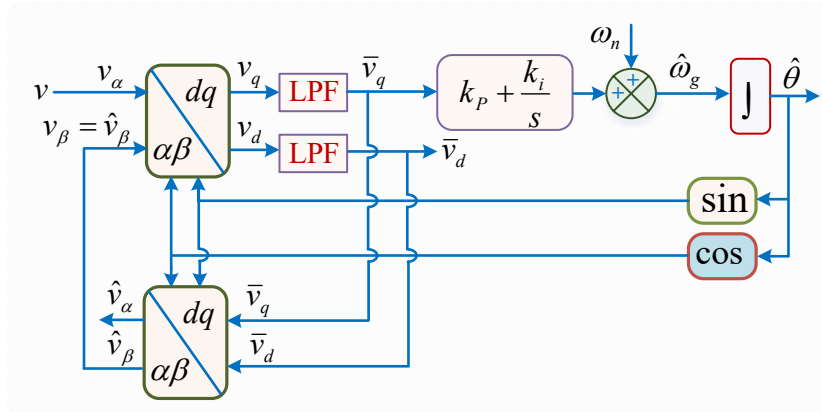
Fig. 6.4 Structure of the IPT-PLL.

D. Second-Order Generalized Integrator-Based PLLs (SOGI-PLLs)

The second-order generalized integrator-based PLLs (SOGI-PLLs) are highly popular and widely used methods for grid synchronization. A functional diagram of SOGI-PLL for single-phase application is shown in Fig. 6.5. The advantage of this method is that it provides the filtered version of orthogonal and in-phase components. In this method, a double feedback loop is used to the SOGI structure to make it frequency adaptive at off-nominal grid frequencies [25, 119].
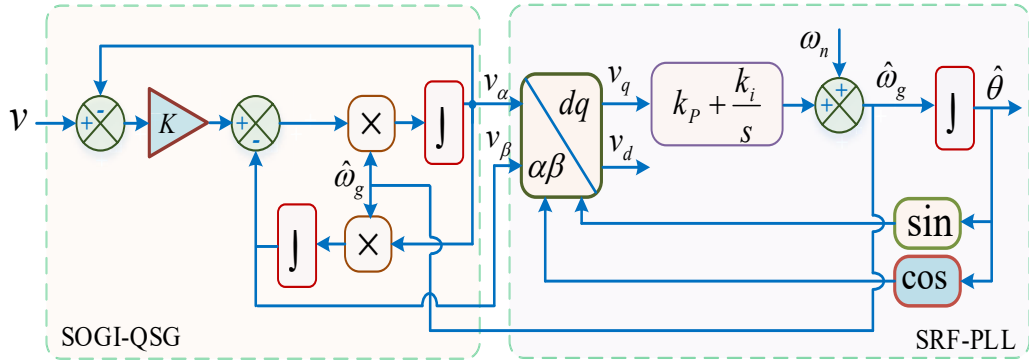
Fig. 6.5 Structure of the SOGI-PLL.

The small-signal modeling and control design guidelines for the SOGI-PLL can be found in [26].

E. Frequency-Fixed SOGI-PLLs (FFSOGI-PLLs)

As discussed earlier, feedback is used in the traditional SOGI-PLL structure to make the PLL frequency adaptive during grid frequency variations. In recent years, some frequency fixed SOGI-PLL structures have also been reported in the literature. For example, in [127], the β-axis component of the SOGI-QSG is multiplied by the ratio of estimated and nominal grid frequency in order to generate two components with the same phase shift (90° phase difference) and the same signal amplitude. In this method, a phase error compensator is employed to correct the phase error, which is generated due to the phase difference between the grid voltage and the α-axis component under off-nominal frequencies [25]. The schematic diagram of the PLL is illustrated in Fig. 6.6.
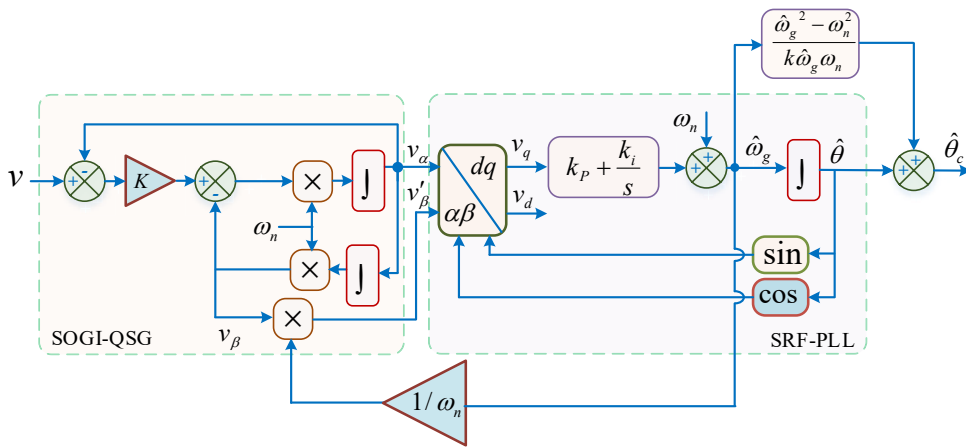
Fig. 6.6 Structure of the frequency fixed SOGI-PLL-1.

Another frequency fixed SOGI-PLL structure is proposed in [164]. The structure is illustrated in

Fig. 6.7. In this structure, an additional SOGI-QSG is used in the feedback loop to generate the same phase difference (90° phase shift) with the same amplitude in the generated sine and cosine components of the Park's transformation at off-nominal frequencies [25].
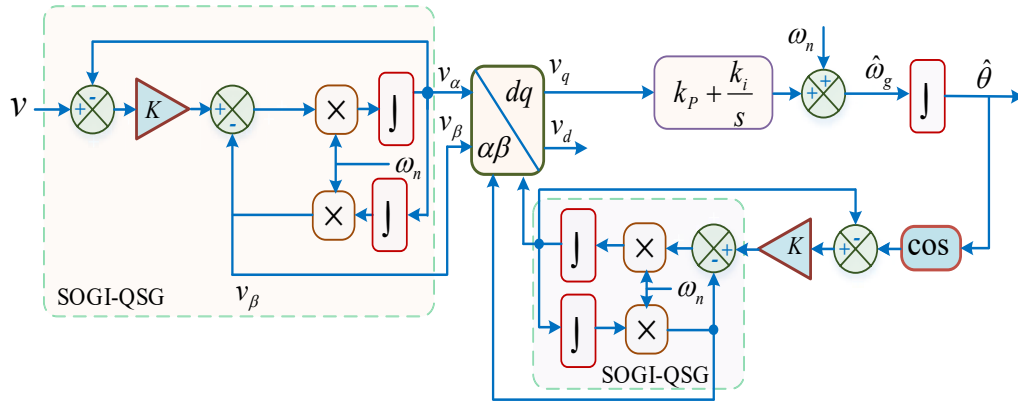
Fig. 6.7 Structure of the frequency fixed SOGI-PLL-2.

6.1.2 Single-phase QSG -FLLs

The block diagram of the standard SOGI-FLL is illustrated in Fig. 6.8. The FLL is a nonlinear closed-loop control system. In this structure, the SOGI is employed as the quadrature signal generator (QSG), which is the main component of most FLLs. In addition to extracting grid voltage phase, frequency and amplitude, it also provides filtering of the in-phase and quadrature components of the input signal. In this structure, the input grid frequency is directly estimated by the FLL, whereas the phase angle and amplitude are calculated indirectly [119, 165].
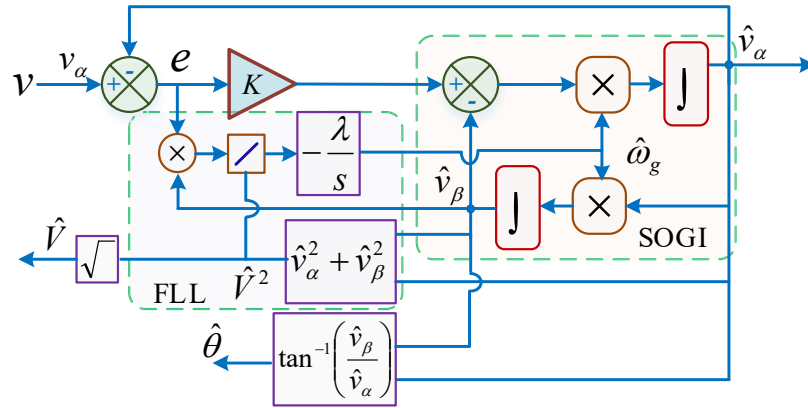
Fig. 6.8 Structure of the SOGI-FLL.

The main limitation of the standard SOGI-FLL is that it does not provide sufficient filtering for subharmonics and DC-offset. As a result, this method suffers from oscillatory error in the estimated quantities if subharmonics and DC-offset pollute the input signal.

To improve the performance of the SOGI-FLLs in the presence of these disturbances, several advanced methods have been reported in recent years. In [88], a DC-offset estimation capability-based loop is employed inside the SOGI-FLL. In addition to removing DC-offset, it improves the capability to remove subharmonics. Nevertheless, this improved structure does not make it immune to the harmonic components. Another similar DC-offset rejection capability-based structure has been suggested in [166]. To enhance harmonic elimination capability, a multiple SOGIs based structure has been suggested in [167]. The SOGI units are tuned at low-order harmonic frequencies and have operated in a cooperative manner to make it immune to these components. However, the use of multiple SOGIs increases its computational burden, and therefore, a significant improvement on harmonic, subharmonics and unknown harmonics may not be possible with this structure [165]. The use of multiple SOGIs in parallel to remove harmonics is not suitable to implement due to the high computational burden. To overcome this limitation, an adaptive BPF based SOGI-FLL is suggested in [168]. The schematic diagram of this FLL is illustrated in Fig. 6.9. In this structure, a SOGI-QSG is used as the adaptive prefilter, whose α-axis part is only used for the filtering purpose. In this structure, a frequency feedback loop is also used to update the centre frequency of the employed filter to adapt any variation in the input signal frequency. This

method completely removes DC-offset and significantly enhances harmonics and subharmonics rejection capability based on bandwidth selection.
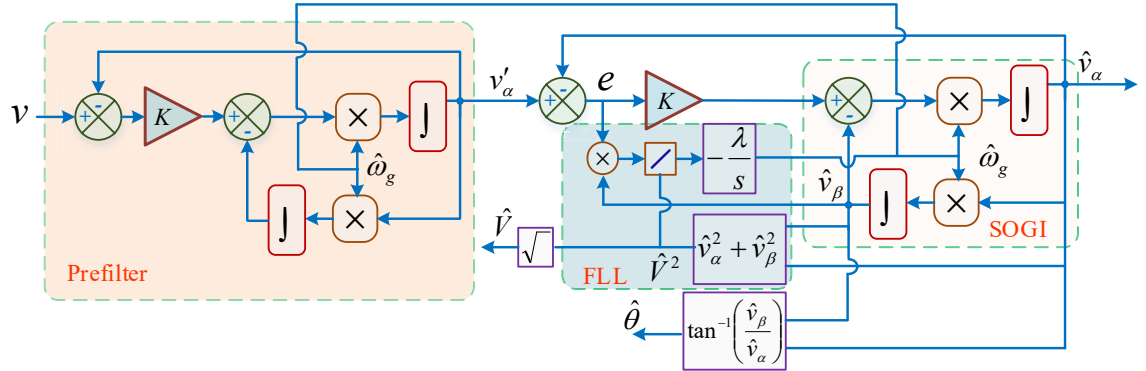
Fig. 6.9 Structure of the SOGI-FLL with prefilter.

A fourth-order generalized integrator based FLL (FOGI-FLL) is presented in [169, 170]. The FOGI-FLL shows enhanced harmonic/subharmonic rejection capability compared to SOGI-QSG, and completely rejects the DC-component in the input signal [170]. A modified FOGI-FLL structure is presented in [165], which is also called SOGI-FLL with in-loop filter. The schematic diagram of this structure is shown in Fig. 6.10.
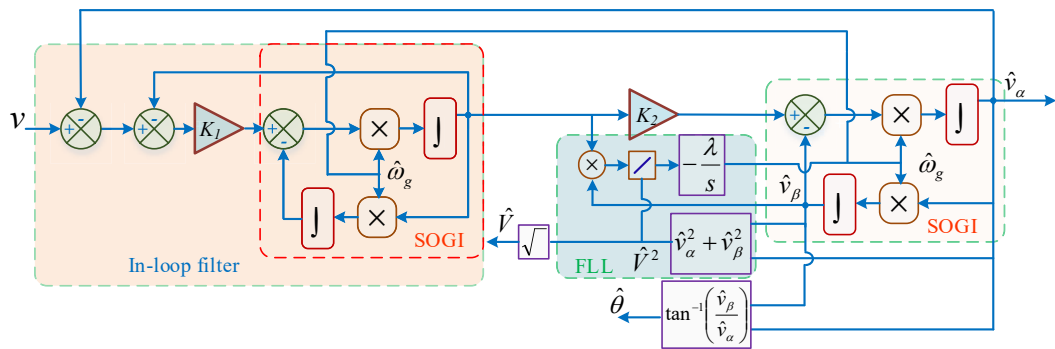
Fig. 6.10 Structure of the SOGI-FLL with in-loop filter.

The SOGI-PLL with in-loop and pre-loop filter-based methods shows improved filtering capability, but these approaches increase implementation complexity and computational burden. To improve the transient performance of the SOGI-FLL, a soft start-up based adaptive method is suggested in [171]. This method presents a significant improvement to achieve faster and smoother transient response during the start-up or and phase jump conditions.

However, this improvement has no effect on the filtering capability [26, 171]. To improve filtering capability of the SOGI-FLL, a different FLL, called the comb-FLL is suggested in [172]. This FLL presents a higher filtering capability. However, when the sampling frequency is high, it requires a large memory to store data samples of a complete grid cycle, and consequently, increases implementation complexity. In [173], an extremum seeking-based FLL is presented. This method suffers from high computational burden, poor performance, and implementation complexity compared with the SOGI-FLL. In [174], a limit-cycle oscillator-based FLL is suggested. In this structure, two feedback loops are employed in the SOGI-FLL structure and eliminate the amplitude normalization from the SOGI-FLL. However, this method suffers from oscillatory error under grid voltage sag [26]. To overcome the limitation of the limit-cycle oscillator-based FLL during input voltage sag, a circular limit-cycle oscillator based FLL is suggested in [19]. This structure overcomes the offset error problem during input voltage amplitude variations. However, this method does not show any improvement over the standard SOGI-FLL [26].

Based on the above analysis, the common drawbacks of the QSG-PLLs and QSG-FLLs include: (1) frequency-adaptive problem under off-nominal frequencies, (2) increased implementation complexity, and (3) oscillatory errors in the presence of DC-offset, harmonics and subharmonics. Addressing the shortcomings of the existing QSG-PLLs and QSG-PLLs has become the main motivation behind developing more advanced PLL.

6.2 Proposed PLL Structure

This project introduces a new quadrature signal generation (QSG) based PLL method to estimate the grid parameters. The block diagram of the proposed PLL is illustrated in Fig. 6.11. This PLL method presents an enhanced performance under adverse grid conditions. It mitigates the drawbacks of the existing approaches to work accurately in the presence of harmonics, subharmonics and DC-offset, and at off-nominal frequencies. This method employs a modified Fourier linear combiner (MFLC) algorithm to generate the filtered version of the input signal and its quadrature signal component. To generate the quadrature signal components at the varying grid frequency, this method uses the modified weighted frequency FLC (MWFLC) algorithm. This algorithm estimates the fundamental frequency

component of the input signal, which acts as a self-tuned adaptive filter algorithm to estimate the signal frequency. This method does not require any feedback loop from the SRF-PLL block to work accurately at off-nominal frequencies. As a result, it shows enhanced stability. The detailed simulation and experimental studies are conducted under distorted grid conditions to verify the robustness. The performance of the proposed technique is also compared with the traditional approaches to show its advantages.
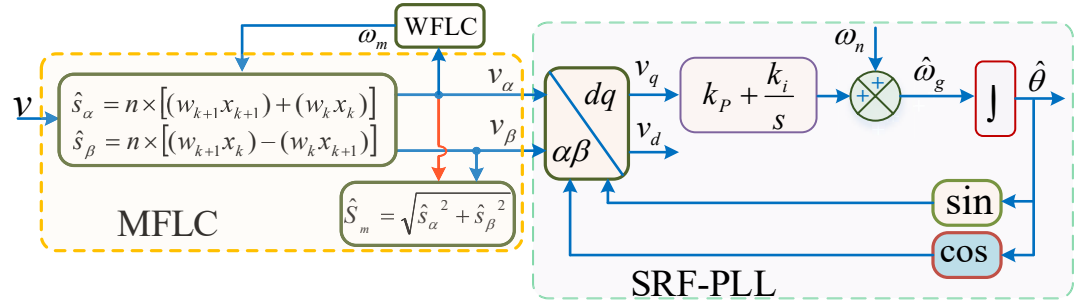
Fig. 6.11 Proposed QSG-PLL structure.

6.2.1 Proposed QSG Algorithm

In the proposed PLL structure, a modified FLC (MFLC) algorithm is used to generate the quadrature signal components of the input signal. The generated signals are then used as the inputs of the SRF-PLL. It can be observed that the QSG block and the SRF-PLL are decoupled in the proposed structure, and thus, provides enhanced stability and ensures simple implementation. The MFLC algorithm is used to extract the fundamental component of the input signal which provides the sufficient filtering to eliminate the harmonics. The basic FLC algorithm is presented in Section 5.2, and the block diagram is illustrated Fig. 5.9. In the MFLC structure, the value of the centre frequency ω_m is obtained from the proposed MFLC algorithm.

The proposed algorithm is given by

$$x_{n_k} = \begin{cases} \sin(\omega_m k), & 1 \le n \le N \\ \cos(\omega_m k), & N+1 \le n \le 2N \end{cases} \tag{6.1}$$

$$\varepsilon_k = s_i - w_k^T x_k \tag{6.2}$$

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$$w_{k+1} = w_k + 2\mu x_k \varepsilon_k \tag{6.3}$$

where ω_m is the adaptive value of the centre frequency, ε_k is the error signal, s_i is the input signal which comprises the fundamental component of the grid voltage and noises, w_k is the adaptive weight vector, N is the number of harmonics in the model, and μ is the adaptive gain.

The fundamental component of the input grid signal is given as

$$\hat{s}_\alpha = n \times \left[(w_{k+1} x_{k+1}) + (w_k x_k) \right] \tag{6.4}$$

The quadrature component of the input grid signal is given as

$$\hat{s}_\beta = n \times \left[(w_{k+1} x_k) - (w_k x_{k+1}) \right] \tag{6.5}$$

The reference signals x_{1_k} is given by

$$x_{1_k} = \begin{cases} \sin(\omega_m k) \\ \cos(\omega_m k) \end{cases} \tag{6.6}$$

The error signal ε_{1_k} is obtained by

$$\varepsilon_{1_k} = n \times \left[(w_{k+1} x_{k+1}) + (w_k x_k) \right] - w_{1_k}^T x_{1_k} \tag{6.7}$$

The adaptive weight vector is calculated as

$$w_{1_{k+1}} = w_{1_k} + 2\mu x_{1_k} \varepsilon_{1_k} \tag{6.8}$$

The frequency of the fundamental component of the input signal is given by

$$\omega_{m_{k+1}} = \omega_{m_k} - 2\mu_m \varepsilon_{1_k} \left(w_{k+1} x_k - w_k x_{k+1} \right) \tag{6.9}$$

where μ_m is the adaptive gain.

The amplitude of the fundamental component of grid voltage is estimated by

$$\hat{S}_m = \sqrt{\hat{s}_\alpha^{\,2} + \hat{s}_\beta^{\,2}} \tag{6.10}$$

6.2.2 Parameter Tunning of the Proposed PLL

In the traditional PLL structures, the frequency and phase angle are usually estimated in the same control loop. As a result, the PLL methods suffer from poor dynamic performance in estimating the frequency under phase jump [171]. In the SOGI-PLL structure, the large

frequency transient causes the direct and quadrature signals oscillatory which are generated in the SOGI block, and also propagates to the SRF-PLL. As a result, the PLL turns into oscillatory state and may become unstable under a large phase-step condition in the input signal. To mitigate this problem, smaller values of proportional-integral (PI) controller gains (k_p and k_i) are selected in the SRF-PLL design to have improved dynamic performance [127]. By contrast, the frequency is calculated in the QSG generation block in the proposed PLL structure. Since the frequency and phase are estimated in different control loops in the proposed structure, the larger PI gain can be chosen to have faster dynamic performances. In the proposed design, the settling time (t_s) is set to 30 ms, the error band (δ) and damping ratio (ζ) are set to 5% and 0.707, respectively. The calculated natural frequency (ω_n) is 157.5745 rad/s. These parameters result in $k_p = 222.8$ and $k_i = 24830$. For the 25 kHz sampling frequency, the calculated digital loop filter coefficients (β_0 and β_0) are 223.2966 and -222.3034, respectively. The parameters of the QSG block are chosen to have improved dynamic performance in terms of settling time and overshoot/undershoot in the estimated grid frequency. The parameters n, μ, and μ_m are set to 5, 0.004, and 0.4, respectively. The system stability analysis and developing the QSG parameter tunning method will be among the focuses of future works.

6.3 Experimental Results

This section presents some experimental results to investigate the performance of the proposed PLL method. The conventional SOGI-PLL and SOGI-FLL are also implemented to provide a comparison. Several grid fault scenarios are generated to verify the robustness of the proposed method, which includes +2 Hz frequency shift, 20° phase step, 50% voltage sag, 20% 1 Hz subharmonic, 10% third harmonic and 5% fifth harmonic, and 0.1 p.u. DC offset. A floating-point DSP (TMS320F28379D) is used to generate the grid faults in real-time by using its internal digital to analog converter (DAC) modules. The sampling frequency is fixed at 25 kHz. Fig. 6.12 depicts the experimental results for +2 Hz frequency shift in the input grid signal. As shown, the proposed method and SOGI-FLL methods show zero phase and frequency error in steady state, whereas the traditional SOGI-PLL shows oscillatory error in the estimated frequency and phase. The proposed and SOGI-FLL methods show nearly the

same speed of response in estimating the frequency of the input signal. It implies that the proposed PLL method works effectively under grid frequency variation.

(a)

(b)

(c)
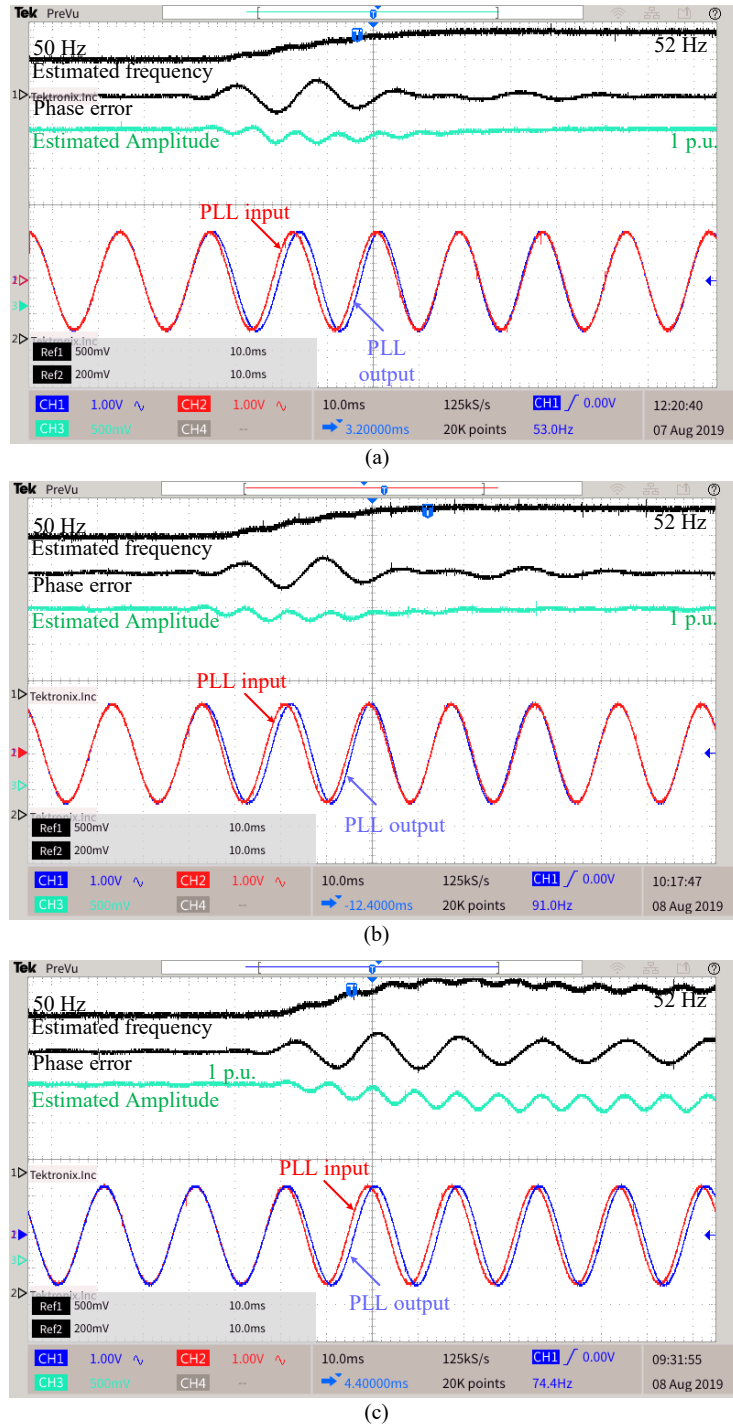
Fig. 6.12 Experimental results under +2 Hz frequency shift, (a) proposed PLL, (b) SOGI-FLL, and (c) SOGI-PLL.

Fig. 6.13 illustrates the experimental results for 20° phase step in the input signal. All PLLs present zero phase error in steady state, but the proposed method has a shorter settling time and less overshoot compared with the other PLLs in estimating the frequency for this step change.
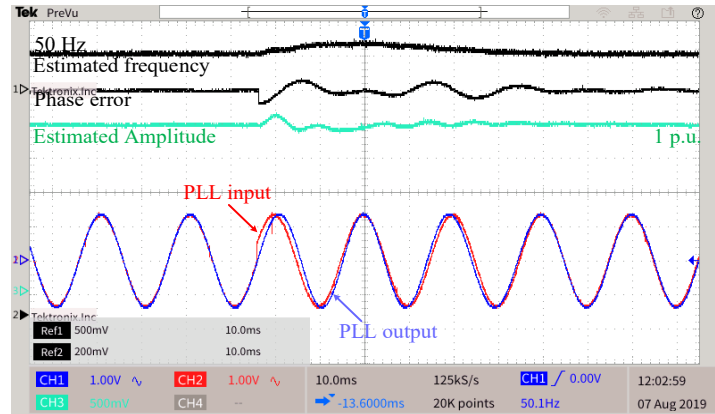
(a)
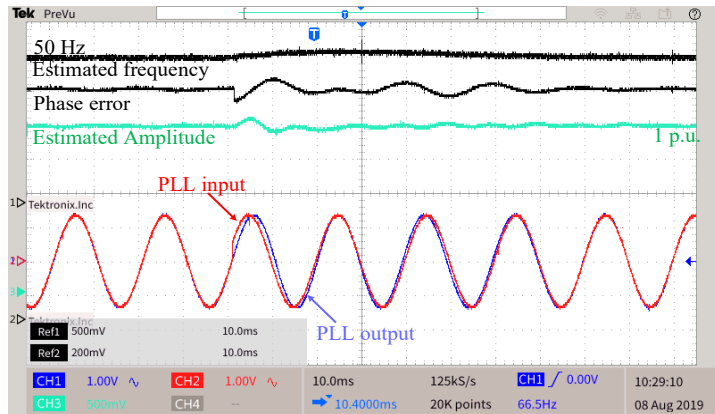
(b)
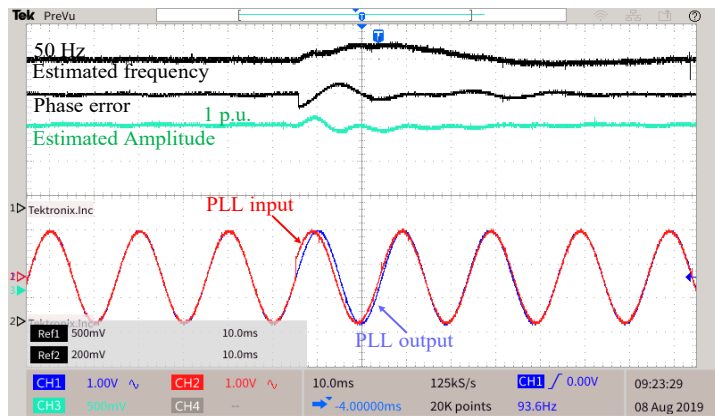
(c)

Fig. 6.13 Experimental results under 20° phase step in the input signal, (a) proposed PLL, (b) SOGI-FLL, and (c) SOGI-PLL.

The SOGI-FLL requires 65 ms to obtain zero steady-state error, whereas the SOGI-PLL requires 60 ms, but a higher overshoot is observed in the estimated frequency. By contrast, the proposed method requires 55 ms, and a less overshoot is also seen in the estimated frequency.
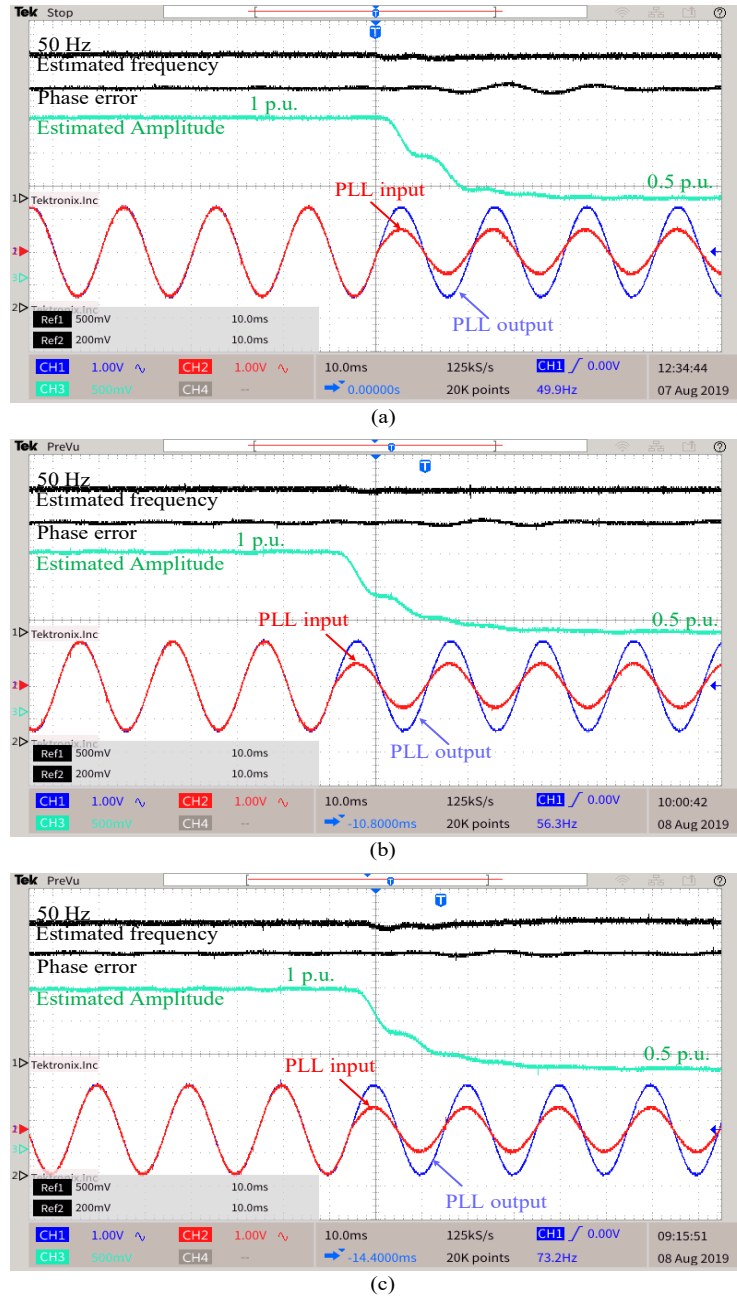
Fig. 6.14 Experimental results under 50% voltage sag, (a) proposed PLL, (b) SOGI-FLL, and (c) SOGI-PLL.

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Fig. 6.14 compares the performance of the PLLs in response to 50% voltage sag in the input signal. As shown, the proposed method shows improved dynamic performance in estimating the grid voltage amplitude. The SOGI-PLL and SOGI-FLL require 60 ms. In contrast, the proposed method requires 50 ms to obtain zero steady-state error.

(a)

(b)

(c)
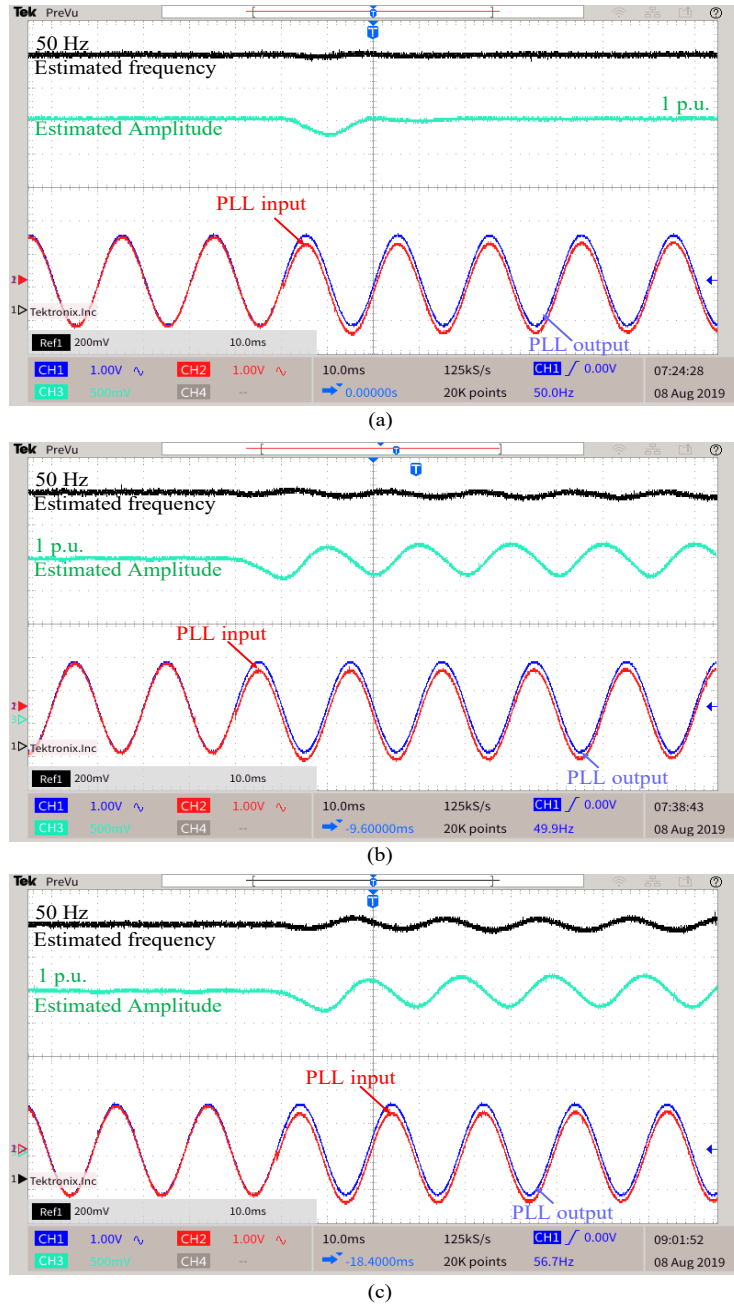
Fig. 6.15 Experimental results under subharmonic distortion, (a) proposed PLL, (b) SOGI-FLL, and (c) SOGI-PLL.

Fig. 6.15 shows the obtained results of the PLL techniques under harmonically distorted grid (20% 1 Hz subharmonic). The proposed method offers a significantly improved performance in filtering capability compared to traditional SOGI-PLL and SOGI-FLL.
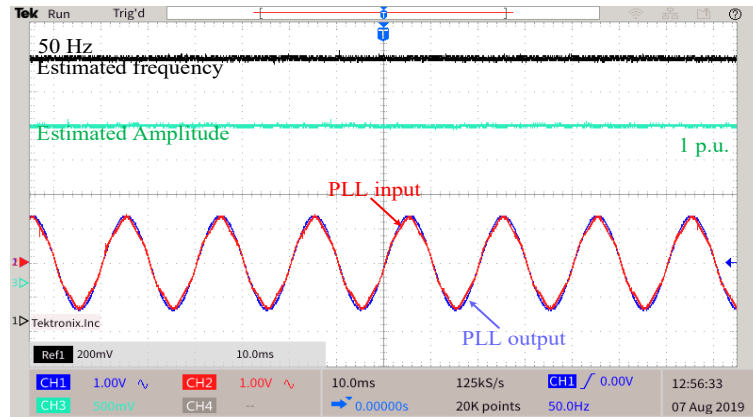
(a)
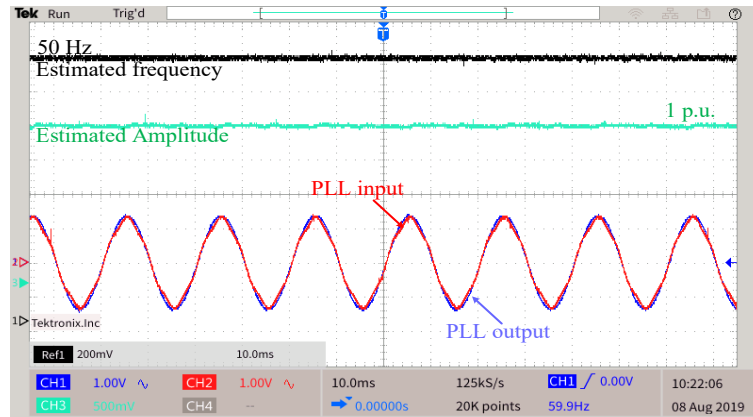
(b)
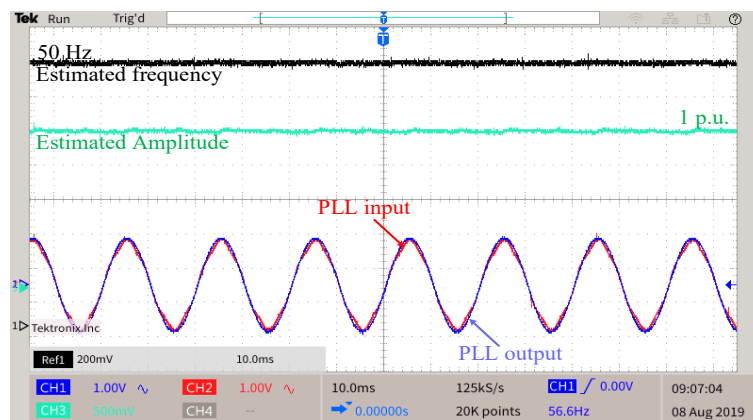
(c)

Fig. 6.16 Experimental results in response to the presence of high order harmonics, (a) proposed PLL, (b) SOGI-FLL, and (c) SOGI-PLL.

As shown, the SOGI-FLL presents less error in the estimated frequency compared with SOGI-PLL. However, both SOGI-based methods are highly sensitive to the subharmonic in estimating the grid voltage amplitude. It can be seen that the estimated amplitude contains a large oscillatory error with those methods. By contrast, the proposed method effectively eliminates this subharmonic component to estimate the ripple-free grid parameters.

Fig. 6.16 depicts the experimental results in response to high order harmonics (10% third harmonic and 5% fifth harmonic). As shown, all the methods perform well in the presence of high-order harmonics.

Fig. 6.17 compares the performance of the traditional SOGI-based methods and the proposed one in response to the presence of DC-offset (0.1 p.u. DC value) in the input signal. The SOGI-PLL and SOGI-FLL techniques are highly sensitive to the DC component in the input signal. As shown, the SOGI-FLL shows less error in the estimated frequency compared with the SOGI-PLL. However, both methods show high oscillatory error in the estimated amplitude in the presence of the DC component. In contrast, the proposed method successfully mitigates this disturbance and shows ripple-free estimated quantities after the transient. Thus, it can be concluded that the proposed PLL method presents significantly improved filtering capability under DC-offset and low order harmonics, and presents acceptable dynamic performance.
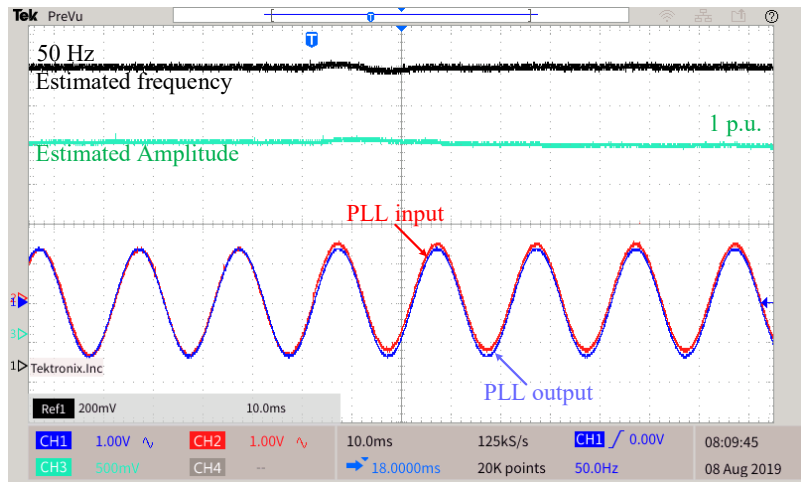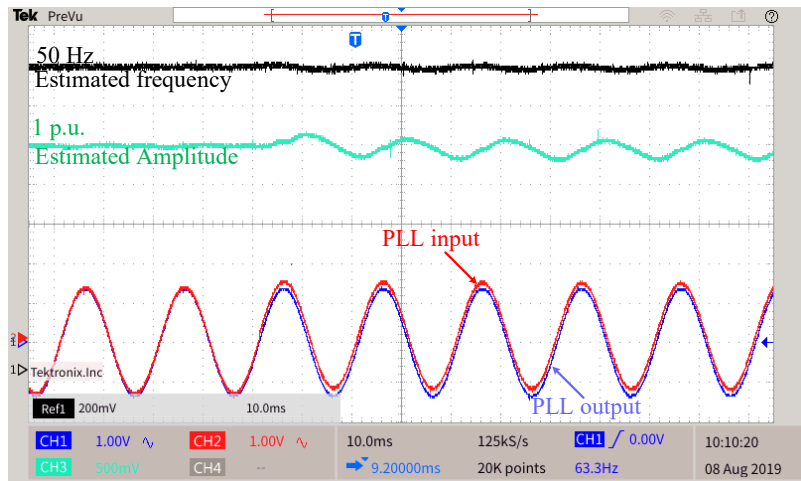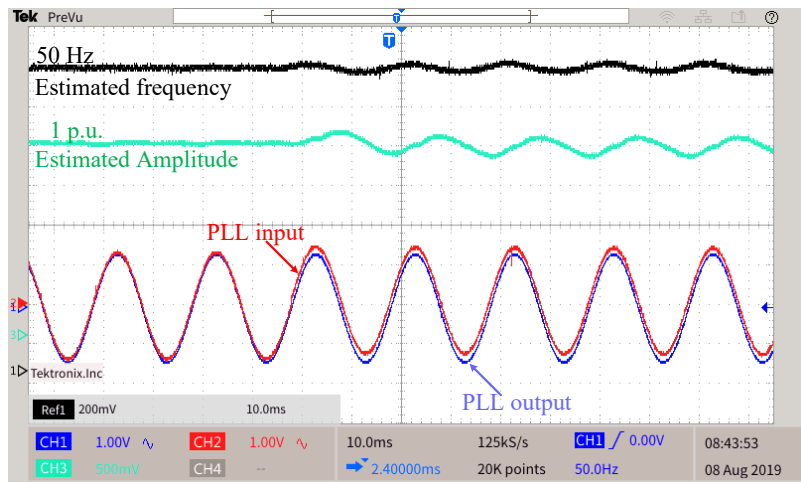
Fig. 6.17 Experimental results in response to the presence of DC-offset, (a) proposed PLL, (b) SOGI-FLL, and (c) SOGI-PLL.

6.4 Conclusion

The major works of this chapter is summarized below.

- A new frequency adaptive quadrature signal generation based PLL method has been proposed for single-phase applications.
- The proposed technique is capable of eliminating subharmonics and DC-offset.
- It works accurately under a wide range of grid frequencies.
- The QSG method has enhanced harmonic elimination capability, and thus, the loop filter can be designed with high bandwidth to improve the dynamic performances of the PLL.
- Experimental results have been presented and compared with the traditional methods.

The control unit of the grid-interfaced power converter requires a robust method to estimate the grid parameters when the grid is affected by disturbances and impurities. The presence of DC-offset, grid frequency variation, and harmonically distorted grid degrades the performance of the traditional PLLs in estimating the grid parameters. A new QSG generation based PLL method has been proposed in this thesis, which presents an enhanced performance in estimating the grid parameters in the presence of those disturbances. In this method, the grid frequency is estimated in the QSG generation block, and it has improved harmonic elimination capability. Thus, the PI filter in the SRF-PLL can be designed with high bandwidth. Consequently, it improves dynamic performance under adverse grid conditions. Experimental tests are conducted in the presence of grid disturbances to verify the robustness of the proposed method.

7 Topology, Modelling and Control Scheme Design for Multilevel Power Converters

7.1 Introduction

Renewable energy sources (RESs) are the long-term sustainable energy sources. Nowadays, they are gaining more and more popularity due to the environmental and global sustainability concern, which encourages to harvest more power from the clean RESs like photovoltaic (PV) and wind energy (WE) sources. Consequently, these energy sources have been considered as a possible mainstream way of electric power generation over the fossil fuel-based centralized generation systems. To overcome the energy crisis, RESs are used in conjunction with the centralized electrical power generators to support the utility grid as well as to improve grid stability. Fig. 2.1 in Chapter 2 shows the typical structure of hybrid microgrid, which demonstrates the integration of PV and wind energy into the AC-subgrid. The grid-connected power converter plays a crucial enabling technology for the integration of those energy sources to the electricity network. Such interfacing can be realized through the single-phase or three-phase power converters. These converters are generally cost-driven. Thus, the major limitation that prevents the high penetration of RESs into the grid is the cost of the power conversion system. The main challenge is to provide a high-quality AC voltage at low cost. The DC/AC voltage source inverter (VSI) is the main component used as an interface between the PV and the AC network. The PV panels can be directly connected to the VSI or through a boost stage, which depends on the employed VSI topology and the PV panel voltage level. For grid-connected applications, VSIs are responsible for dealing with increasingly stringent grid connection standards, power quality, reliability, and robustness as well as to perform other ancillary services.

For residential and commercial applications, the common VSI structures usually used to interface RESs with the grid are the two-level ones. In recent years, multilevel inverters (MLIs) have received much attention over the two-level VSIs. They are potentially attractive and

have been extensively used in a wide range of power conversion applications ranging from low to high voltage applications, especially in renewable energy applications [24, 175, 176]. A higher number of output voltage levels enables higher quality output waveforms, which leads to reduced filter size, and lower electromagnetic compatibility (EMC), and switching losses. Meanwhile, MLIs have less dv/dt stress on the semiconductor devices, which enables the use of low-cost switching devices, and consequently, increases their efficiency [177-179].

Many MLI structures have been reported in the literature with some basic concepts [175]. Still new structures with various application-oriented approaches are being presented and investigated. Fig. 7.1 illustrates this classification of the multilevel converters, which is mainly based on main submodules used in their structures. Among these multilevel converter topologies, the cascaded-H-bridge (CHB) is the most employed topology to synthesize multilevel output voltage, which first appeared in the 1970s. This topology has emerged as a prominent one due to its modularity and symmetric structure [180-185].
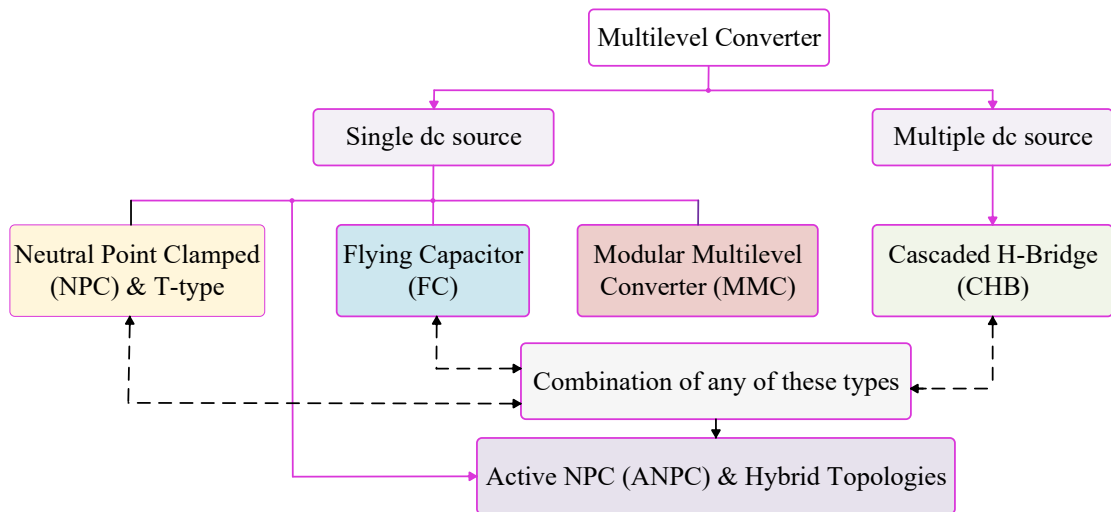
Fig. 7.1 A broad classification of multilevel converter structures.

Another widely used topology is the neutral point clamped (NPC) converter, which first appeared in the1980s and it has been extensively used for decades [182, 186, 187]. These two classic topologies are considered as the base structures to derive many other multilevel converters that have been proposed in recent years [175]. Some other popular topologies include the flying-capacitor (FC) converter [177, 188-190], T-Type converter [176, 183],

active NPC (ANPC) [191], hybrid multilevel NPC converter [177, 187, 192, 193], modular multilevel converters (MMC) [183, 194], and hybrid topologies based on the combination of CHB, FC, and NPC [195-197]. One phase leg of the popular seven-level inverter architecture is illustrated in Fig. 7.2. The CHB converter can generate a large number of output voltage levels by employing cascaded H-bridge structures and provide loss equalization by using a simple pulse width modulation (PWM) technique. Due to its high redundancy states and modularity, this structure is suitable for the fault-tolerant applications.

Nevertheless, it requires a large number of power devices and independent DC-links in higher voltage level generation, and hence, increases the cost, volume and control complexity remarkably. Moreover, in the CHB structure, each DC-link requires a large electrolytic capacitor to absorb the ripple power component, which is generated in the H-bridge structures. Consequently, it reduces the reliability and lifetime of the converter [24, 183, 185, 194, 203, 204]. Similar to CHB structure, FC converter can achieve a fault-tolerant operation by programming the redundancy states of the converter [205]. However, this structure requires a large number of capacitors when a large number of voltage levels are synthesized. This topology also suffers from capacitor voltage unbalancing problem, and consequently, it requires a complex control strategy to realize balanced capacitor voltages [189, 190, 206, 207]. By contrast, the control of NPC converter is easy and popular in industrial applications. Nevertheless, this converter suffers from DC-link capacitor voltage unbalancing as the number of voltage levels increases, and thus, increases the control complexity [175, 183, 201]. The T-type converter requires less number of components compared to the NPC converter topologies. The control of the T-type converter is simple. However, a higher voltage stress is observed across the power devices in the T-type converter [175, 176, 183]. Similar to the FC converter, the MMC converter requires a complex control strategy due to the use of a large number of capacitors in their structures [24, 194]. For grid-connected inverter system, the DC-link voltage should be higher than the peak of the AC voltage output. The voltage requirements can be up to double the AC output voltage for some topologies like traditional NPC inverter. Fig. 7.3 and Table 7.1 present a comparative study of different topologies in terms of the level of output voltage and its magnitude in p.u. for a specific DC-link voltage.
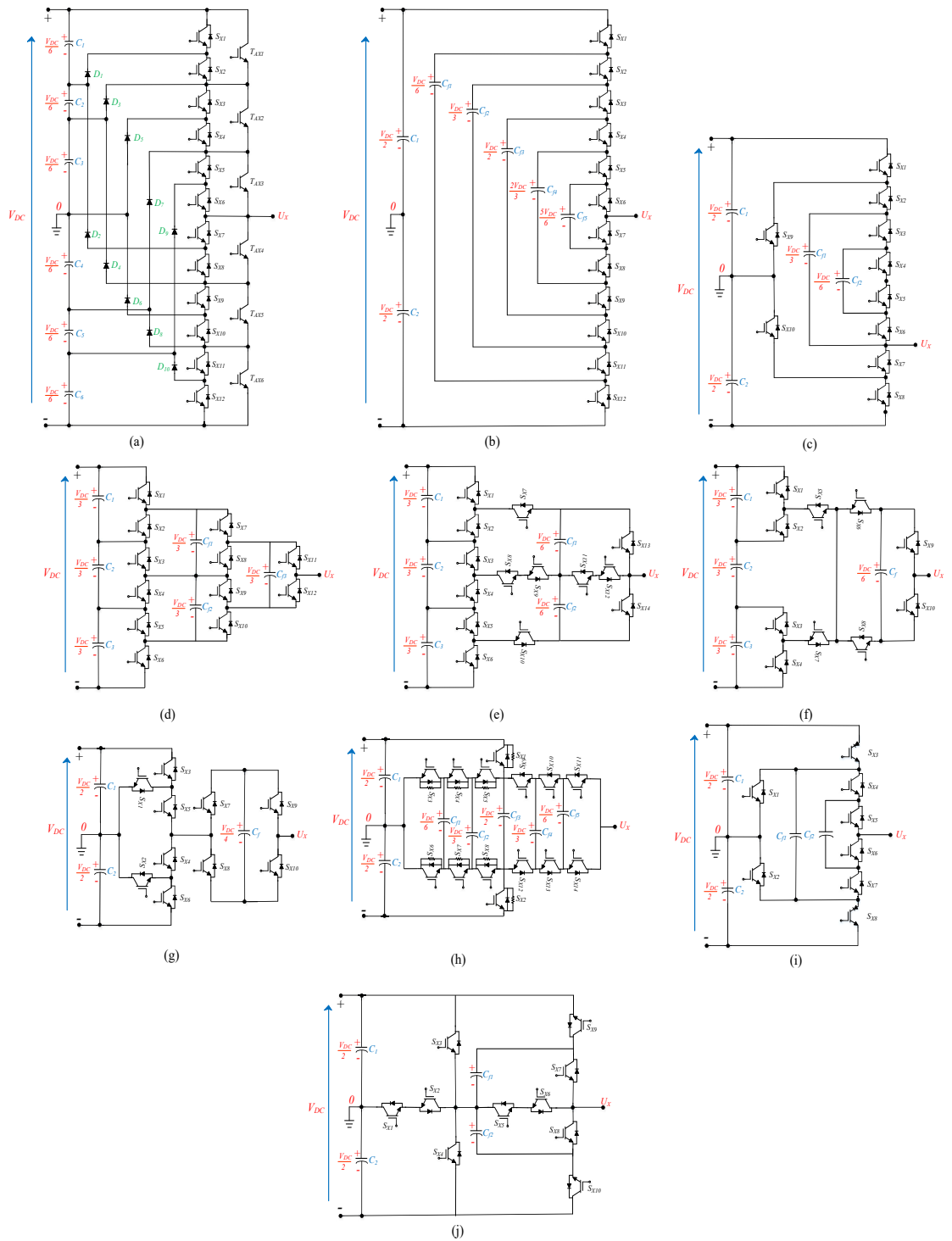
Fig. 7.2 Phase legs of the traditional seven-level inverter structures: (a) seven-level NPC [198, 199], (b) seven-level flying capacitor [189], (c) seven-level ANPC-I [187], (d) generalized seven-level [190], (e) hybrid seven-level ANPC-I [193], (f) hybrid clamped seven-level-ANPC [200], (f) hybrid 7L-ANPC-I [14], (g) hybrid seven-level ANPC-III [201], (h) hybrid seven-level-ANPC-II [187], (i) seven-level ANPC-II [24], and (j) DTT-7L-BANPC inverter [202]. Here X ∈ (R, Y, B) phases.
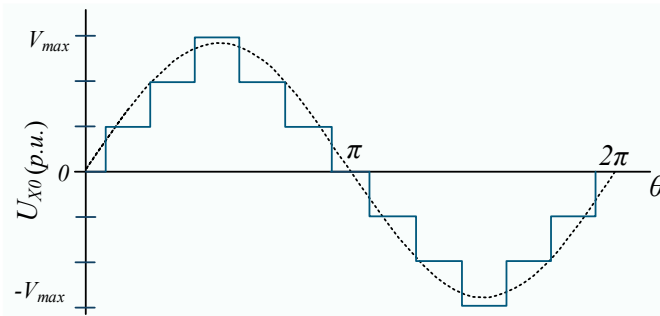
Fig. 7.3 Output voltage levels of different seven-level inverter topologies (for $V_{dc-link} = V_{DC} = 1\ p.u.$).

Table 7.1 Maximum positive voltage level (phase-phase) of different seven-level inverters (for $V_{DC} = 400 = 1\ p.u.$).

Mid-point clamped	Hybrid active-clamped			Switched Capacitor	ANPC		Proposed
(Fig. 7.2 (a, b, c, g, h))	Fig. 7.2(d)	Fig. 7.2(f)	Fig. 7.2(e)	[202]	[208]	[24]	
1/2	1	1/2	3/4	3/2	3/2	1	2

It can be observed that the hybrid clamped topologies require the equal or less DC-link voltage compared to mid-point clamped topologies for the same maximum voltage level generation. Therefore, in some applications like grid-connected PV system, a high boost DC/DC stage is required to provide the required voltage level to feed the mid-point clamped topologies, which can be realized by using an additional DC/DC boost converter, or a large number of series-connected PV panels. Fig. 7.4 illustrates the circuit structures of some typical DC/DC stages, which are generally used as the front-end DC-link voltage supply for multilevel inverters [24].

The use of multiple converters as the front-end converter reduces the overall system efficiency and reliability. Moreover, it increases system cost, converter size and control complexity. For PV applications, alternately, a series of PV panels can be employed to eliminate extra boost stage to provide the desired DC-link voltage levels. However, the series connection of PV panels can cause mismatch among the PV panels, which reduces the amount of energy extracted from the PV panels. Thus, a single-stage DC/AC inverter with voltage boosting capability can be an interesting way compared to a multi-stage power conversion system [190].
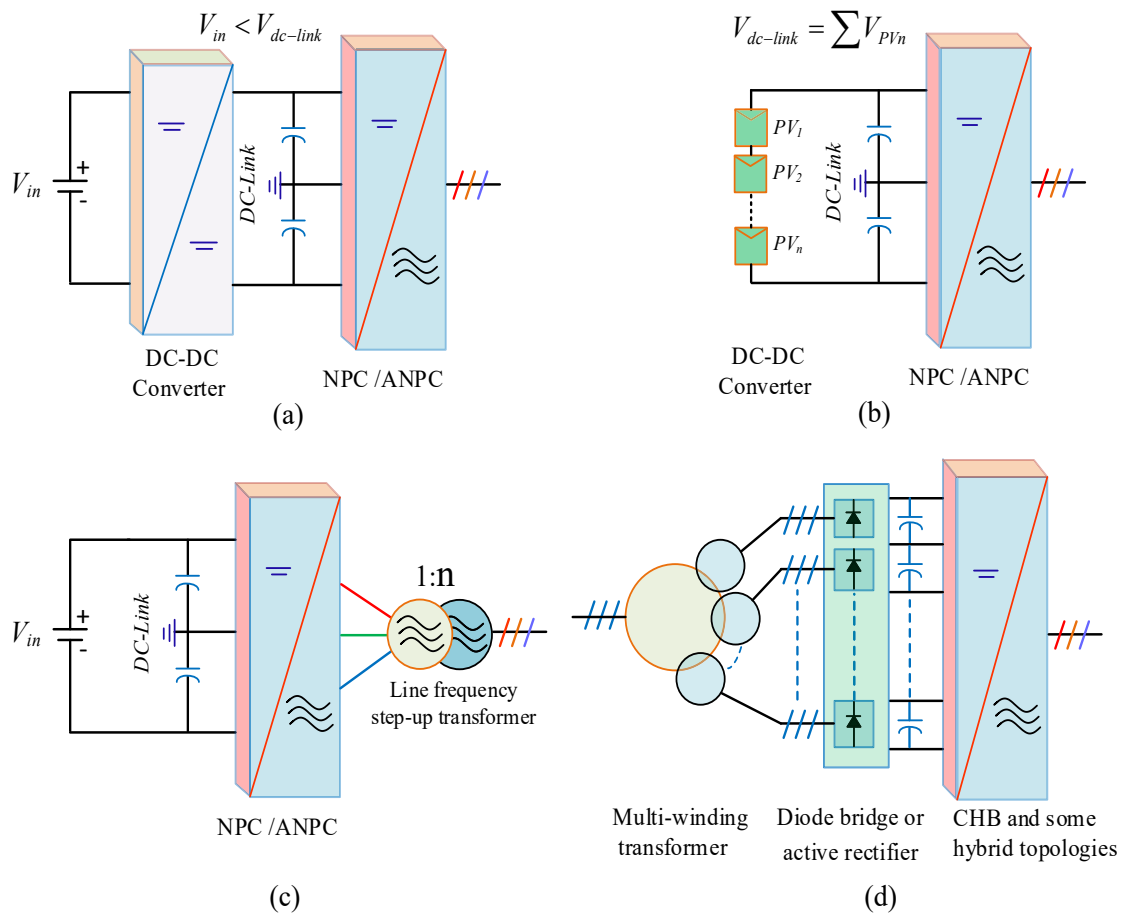
Fig. 7.4 Different front end converter topologies for the common MLIs: (a) front-end step-up DC/DC converter, (b) series-connected PV modules, (c) low frequency step-up transformer-based system, and (d) multi-winding transformer-based isolated system.

In recent years, the hybrid and ANPC converter topologies have achieved much attention in medium power applications. The reason behind the popularity is that these topologies combine the advantages of classical topologies such as FC, CHB, and NPC converters [193, 209, 210]. Nevertheless, these structures still require a large number of components and high DC-link voltage, which are the major drawbacks of these topologies. Considering this aspect, addressing the shortcomings of the classical topologies has been the main motivation behind developing more attractive converter circuits. In this regard, a novel multilevel inverter topology is investigated in this chapter, which is suitable for many applications like grid-connected renewable energy conversion system. The proposed topology reduces the number

of active and passive components as well as their voltage stress, and the DC-link voltage requirement significantly.

7.2 Proposed Circuit Structure

Fig. 7.5 illustrates the phase-leg of the proposed switched-capacitors (SCs) based three-phase multilevel inverter structure with voltage boosting capability. For seven level operation, this structure consists of eight active switches, two capacitors, and a single DC source. As depicted in Fig. 7.5, S_{X1}, S_{X2}, S_{X3}, …, S_{X8} (X ∈ (R, Y, B) phases) are the active switches, where two switches (SX_2 and SX_5) are reverse blocking IGBT (RB-IGBT) and the other six switches are standard unipolar voltage devices (MOSFET/IGBT). Alternately, the employed two reverse blocking switches can be replaced by standard IGBT/MOSFET with a series diode. In the proposed structure, two switched capacitors (C_{X1} and C_{X2}) are incorporated with the input DC source to achieve a voltage gain of 3. In other words, the proposed structure is capable of generating up to $3V_{DC}$ at the output terminal (before the filter) with the input DC voltage magnitude of V_{DC}. Nevertheless, it is also worthy to mention that the rated voltage of the capacitors is the same as the input DC voltage. The switching states of the converter are designed to charge the switched capacitors C_{X1} and C_{X2} to V_{DC} from the input supply voltage through the switches S_{X3} and S_{X6}, respectively, and to achieve balanced voltage around the reference value V_{DC}. For further analysis and providing a base for comparison, the maximum level (line to line) voltage is defined as 1 p.u. The line and phase voltages of the proposed topology are shown in Fig. 7.5(b). The advantage of the proposed structure is that the number of output levels can be increased by cascading similar units in series. The switching states of the proposed circuit for different level generation and the corresponding current paths are presented in Table 7.2 and Fig. 7.6, respectively. It can be seen that each state has a distinct effect on the switched capacitor charging. Fig. 7.7 illustrates the gate signals of the switches in the proposed inverter structure.

(a)

(b)
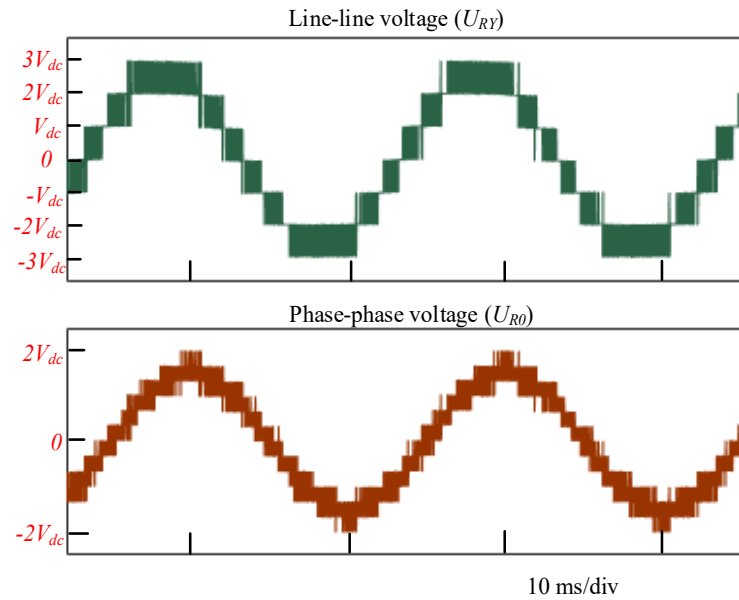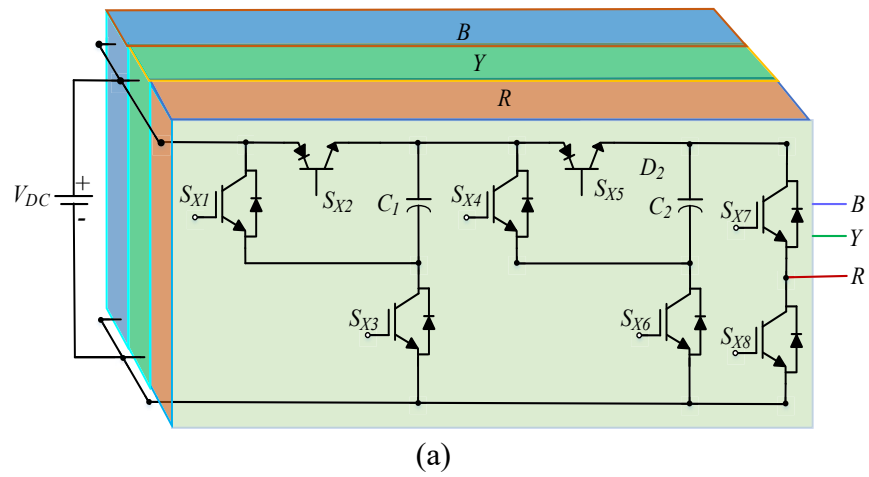
Fig. 7.5 (a) Proposed three-phase inverter circuit for seven-level operation, (b) output line voltage (U_{RY}), and phase voltage (U_{R0}).

Table 7.2 Switching states of the proposed converter.

Switching States	Level	U_{XO}	S_{X1}	S_{X2}	S_{X3}	S_{X4}	S_{X5}	S_{X6}	S_{X7}	S_{X8}	i_{C1}	i_{C2}	V_{C1}	V_{C2}
A	1	0	0	1	1	0	1	1	0	1	i_{c1f}	i_{c2f}	↑	↑
B	2	$+V_{DC}$	0	1	1	0	1	1	1	0	i_{c1f}	i_{c2f}	↑	↑
C	3	$+2V_{DC}$	0	1	1	1	0	0	1	0	i_{c1f}	$-i_x$	↑	↓
D	4	$+3V_{DC}$	1	0	0	1	0	0	1	0	$-i_x$	$-i_x$	↓	↓
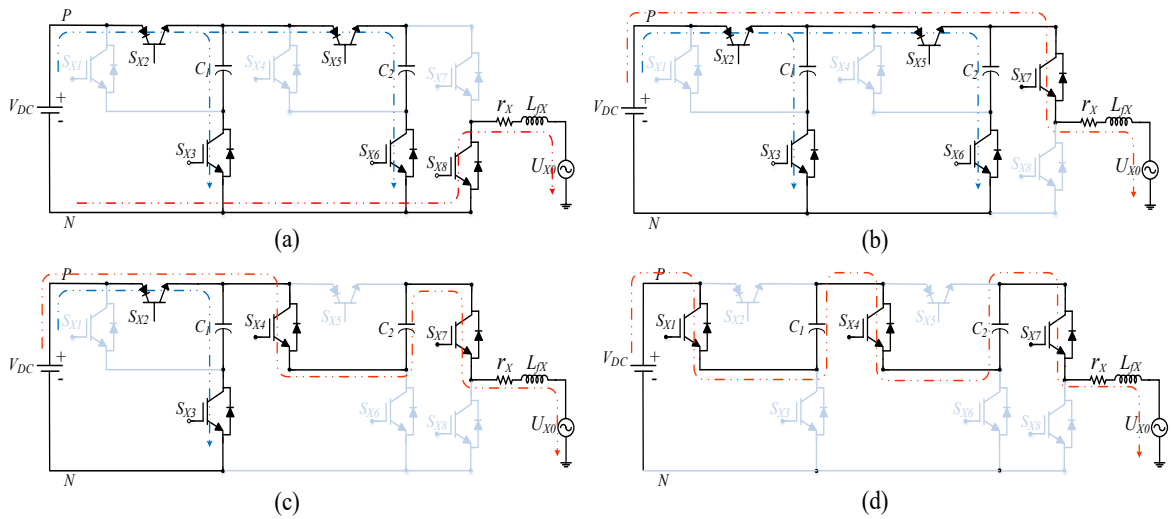
Fig. 7.6 Four switching states of the proposed inverter: (a) State A: 0, (b) State B: +1, (c) State C: +2, and (d) State D: +3.
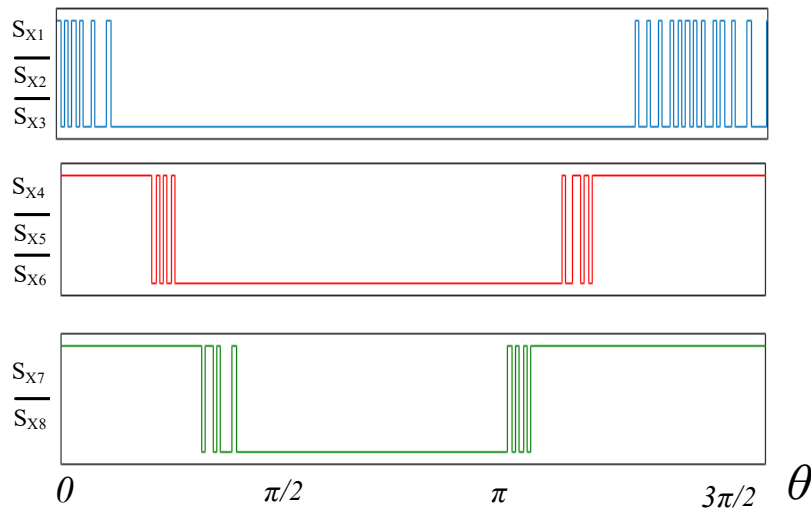
Fig. 7.7 Gate signals of the switches.

The prominent features of the proposed MLI structure include the following aspects:

(1) The proposed structure requires a minimum DC supply voltage compared to existing topologies.

(2) It reduces the number of components compared to the NPC, ANPC, and FC converter categories. For seven-level operation, this topology requires only eight active switches and two capacitors per-phase.

(3) The voltages stress on the switched capacitors do not exceed the input DC voltage. As a result, it reduces the size of capacitors.

(4) The proposed circuit does not require any additional sensor or control strategy to balance the capacitor voltages.

(5) The voltage stress across the power switches is less compared to the traditional topologies.

(6) The MLI can operate under both of the leading and lagging power factors. Thus, it can provide reactive power to the grid when necessary.

7.3 Proposed Control Scheme

Fig. 7.6 illustrates the structure of the proposed three-phase seven-level inverter. The circuit is connected to the grid through an L-type filter with inductance L, and its equivalent series resistance is r. The input DC source voltage is represented by V_{DC}, which is employed to feed the inverter. Fig. 7.8 illustrates the switching states in the $dq0$ plane of the proposed three-phase seven-level switched capacitor inverter.
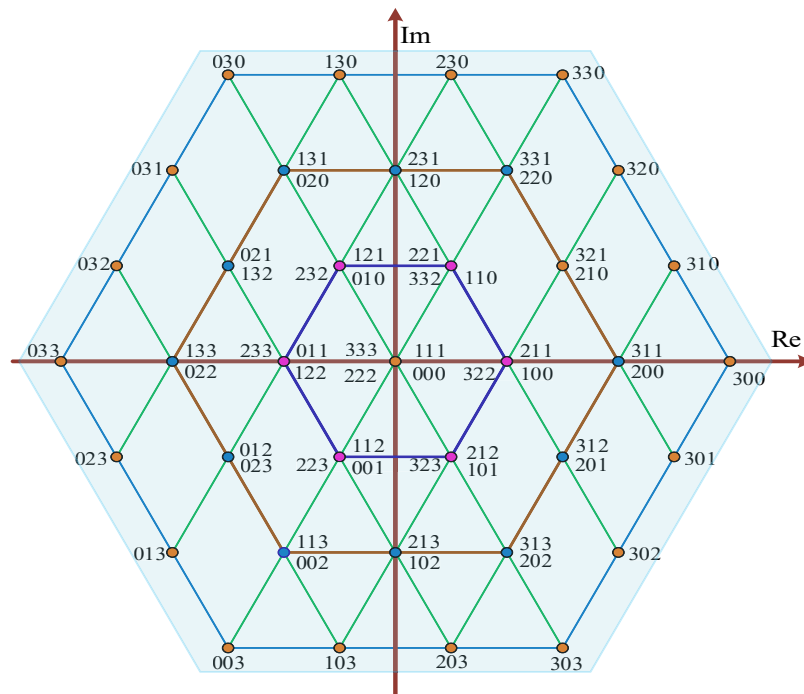
Fig. 7.8 Three-phase seven-level inverter switching states in $dq0$ plane.

Based on the different switching combinations, one phase-leg in the structure can have four states: '0' state, '1' state, and '2' state, and '3' state.

The voltage vectors can be described in the $\alpha\beta$ frame, given by

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \tag{7.1}$$

The converter current can also be expressed in the $\alpha\beta$ frame as

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{7.2}$$

The switching states of the converter can be described in the two-phase stationary $\alpha\beta$ orthogonal coordinate system as the following

$$\vec{S}_{\alpha\beta} = \begin{bmatrix} S_\alpha \\ S_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \tag{7.3}$$

The output voltage space vector of the inverter can be expressed as follows

$$\vec{v}_{con.} = \frac{2}{3} \left(v_{ao} + \vec{\omega} v_{bo} + \vec{\omega}^2 v_{co} \right) \tag{7.4}$$

where $\vec{\omega} = e^{j2\pi/3} = -1/2 + j\frac{\sqrt{3}}{2}$ is a unitary vector that denotes the 120° phase shift between the phases.

According to the switching matrix, the dynamic model of the inverter output voltage can be expressed with the DC-link voltage, as

$$\vec{V}_{\alpha\beta} = \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \vec{S} V_{DC} \tag{7.5}$$

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Based on the switching combinations of the four level inverter, it generates $4^3 = 64$ voltage vectors from the 64 consequence switching states. Due to the redundancy of some voltage vectors that generate equal voltage vectors, only 37 space vectors are available in the finite-control set of the three-phase seven level inverter. The list of these 37 voltage space vectors and their spatial positions are presented in Fig. 7.8.

The mathematical model (continuous time) of the three-phase inverter in the *abc* reference frame is given as

$$\frac{d}{dt}\begin{bmatrix} i_{ga}(t) \\ i_{gb}(t) \\ i_{gc}(t) \end{bmatrix} = \begin{bmatrix} \frac{1}{L} & 0 & 0 \\ 0 & \frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{L} \end{bmatrix}\begin{bmatrix} v_{ga}(t) \\ v_{gb}(t) \\ v_{gc}(t) \end{bmatrix} - \begin{bmatrix} \frac{R}{L} & 0 & 0 \\ 0 & \frac{R}{L} & 0 \\ 0 & 0 & \frac{R}{L} \end{bmatrix}\begin{bmatrix} i_{ga}(t) \\ i_{gb}(t) \\ i_{gc}(t) \end{bmatrix} \tag{7.6}$$

where $v_{ga}(t)$, $v_{gb}(t)$, and $v_{gc}(t)$ are the grid voltages of phases a, b, and c, respectively; $i_a(t)$, $i_b(t)$, and $i_c(t)$ the output currents of phases a, b, and c, respectively.

The discrete time predictive model of (7.6) can be obtained by using the Forward Euler's approximation method as the following

$$\begin{bmatrix} i_{ga}^{k+1} \\ i_{gb}^{k+1} \\ i_{gc}^{k+1} \end{bmatrix} = \begin{bmatrix} 1-\frac{RT_s}{L} & 0 & 0 \\ 0 & 1-\frac{RT_s}{L} & 0 \\ 0 & 0 & 1-\frac{RT_s}{L} \end{bmatrix}\begin{bmatrix} i_{ga}^{k} \\ i_{gb}^{k} \\ i_{gc}^{k} \end{bmatrix} - \begin{bmatrix} \frac{T_s}{L} & 0 & 0 \\ 0 & \frac{T_s}{L} & 0 \\ 0 & 0 & \frac{T_s}{L} \end{bmatrix}\begin{bmatrix} v_{ga}^{k} \\ v_{gb}^{k} \\ v_{gc}^{k} \end{bmatrix} \tag{7.7}$$

The main objective of the controller is to track the reference current. Therefore, the cost function can be defined as the difference between the predictive and reference values of the system variables.

The converter current dynamics of the inverter can be represented in the α-β orthogonal coordinates as

$$\frac{d\vec{i}_{g,\alpha\beta}}{dt} = -\frac{R_s}{L_f}\vec{i}_{g,\alpha\beta} + \frac{1}{L_f}\vec{v}_{\alpha\beta} - \frac{1}{L_f}\vec{v}_{g,\alpha\beta} \tag{7.8}$$

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where $v_{g,\alpha\beta}$ and $i_{g,\alpha\beta}$ are the grid voltage and current vectors, respectively.

The discrete-time model of the grid current at $(k+1)^{th}$ instant for a sample time T_S can be expressed as

$$\vec{i}_{g,\alpha\beta}^{\,k+1} = \frac{1}{R_s T_s + L_f}\left[L_f \vec{i}_{g,\alpha\beta}^{\,k} + T_s\left(\vec{V}_{\alpha\beta}^{\,k} - \vec{V}_{g,\alpha\beta}^{\,k}\right)\right] \tag{7.9}$$

The active and reactive powers of this system can be calculated as

$$P = \frac{3}{2}\operatorname{Re}\left(v_g i_g^*\right) = \frac{3}{2}\left(v_{g,\alpha}i_{g,\alpha} + v_{g,\beta}i_{g,\beta}\right) \tag{7.10}$$

$$Q = \frac{3}{2}\operatorname{Im}\left(v_g i_g^*\right) = \frac{3}{2}\left(v_{g,\beta}i_{g,\alpha} - v_{g,\alpha}i_{g,\beta}\right) \tag{7.11}$$

For the active and reactive power control, the cost function J can be defined as

$$J_{Cost.} = \frac{\left(P - P_{ref}\right)^2}{P_{ref}} + \frac{\left(Q - Q_{ref}\right)^2}{Q_{ref}} \tag{7.12}$$

where P_{ref} and Q_{ref} are the active and reactive power references, respectively.

7.4 Comparative Summary

Table 7.3 and Table 7.4 represent a comparative analysis of the proposed topology with some popular existing topologies. The topologies under study are selected to have the same number of voltage level generations with a single DC source. The study is performed to evaluate the pros and cons of the proposed topology over the existing topologies in terms of number of semiconductor devices, capacitors used in their structures, the required DC-link voltage for the same output voltage generation, total blocking voltage by the switches in p.u. and total voltage across the capacitors in p.u. The study is performed for one phase leg. The number of semiconductor switches used in the proposed topology is 8, which is the minimum number compared to the topologies presented in this comparison. In terms of reliability of the converters, the capacitors are the most critical component used in the converter structures. The number of capacitors used in the structure and their voltage ratings should be minimum

to reduce converter volume and space requirement [211]. As it can be seen that the proposed topology requires minimum number of capacitors compared to its counterparts.

Table 7.5 shows the maximum voltage stress across the components of the proposed circuit, and Table 7.6 shows the comparison of voltage stress across the components of the different topologies. It is worth noting that the total voltage stress across the capacitors is less compared to other inverter families, which is the notable contribution compared to traditional converter families. Notice that each capacitor voltage does not exceed its input DC-link voltage. The proposed topology presents enhanced structural merits from the point view of the voltage boosting capability. It reduces the DC-link voltage requirement by 75% compared to conventional NPC and ANPC with mid-point grounding, and 50% compared to hybrid topologies. It is obvious that the total blocking voltage by the semiconductor switches in the proposed topology is significantly lower than the NPC, CHB or some hybrid topologies, which results in cost saving for the overall system design.

Table 7.3 Comparison of the Proposed Topology with the Traditional Topologies (Max. phase voltage = 400V = 1 $p.u.$).

Parameters	Fig. 7.2(a)	Fig. 7.2(b)	Fig. 7.2(c)	Fig. 7.2(d)	Fig. 7.2(e)	Fig. 7.2(f)	Fig. 7.2(g)	Fig. 7.2(h)	Fig. 7.2(i)	Fig. 7.2(j)	Proposed
No. of active switches	18	12	10	12	14	10	10	14	8	10	8
No. of capacitors	6	7	4	6	5	4	3	7	4	4	2
DC- link voltage required for the same phase voltage	2	2	2	1	1.5	2	2	2	1	0.66	0.5

Table 7.4 Comparison of Total Voltage Stress across the Switches and Capacitors (Max. phase voltage = 400V =1 $p.u.$).

Parameters	Fig.7. 2(a)	Fig.7. 2(b)	Fig.7. 2(c)	Fig.7. 2(d)	Fig.7. 2(e)	Fig.7. 2(f)	Fig.7. 2(g)	Fig.7. 1(h)	Fig.7. 2(i)	Fig.7. 2(j)	Proposed
Total blocking voltage (p.u.) by active switches	6	8	6	8	6.66	5.33	8	8	5	7.25	5.5
Total voltage across the capacitors (p.u.)	2	7	3.33	4	2.66	2.33	2.5	3	3.25	2	1

Table 7.5 Maximum Voltage Stress on the Components of the Proposed Circuit (Max. phase voltage = 400 V =1 $p.u.$).

Devices	S_{X1}	S_{X2}	S_{X3}	S_{X4}	S_{X5}	S_{X6}	S_{X7}	S_{X8}	C_{X1}	C_{X2}
Voltage stress (p.u.)	0.5	0.5	0.5	0.5	0.5	1	0.5	1.5	0.5	0.5

Table 7.6 Maximum Voltage Stress on the Components of Conventional Topologies (Max. phase voltage = 400 V =1 $p.u.$).

Device	Fig.7. 2(b)	Fig.7. 2(c)	Fig.7. 2(d)	Fig.7. 2(e)	Fig.7. 2(f)	Fig.7. 2(g)	Fig.7. 2(h)	Fig.7. 2(i)	Fig.7. 2(j)
S_{X1}	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$
S_{X2}	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$
S_{X3}	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\pm\frac{1}{4}V_{DC}$
S_{X4}	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{3}{8}V_{DC}$
S_{X5}	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{8}V_{DC}$
S_{X6}	$\frac{5}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{8}V_{DC}$
S_{X7}	$\frac{5}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{4}V_{DC}$	$\frac{3}{8}V_{DC}$
S_{X8}	$\frac{1}{6}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{4}V_{DC}$	$\pm\frac{1}{4}V_{DC}$
S_{X9}	$\frac{1}{6}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{4}V_{DC}$	—
S_{X10}	$\frac{1}{6}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{4}V_{DC}$	—
S_{X11}	$\frac{1}{6}V_{DC}$	—	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	—	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	—	—
S_{X12}	$\frac{1}{2}V_{DC}$	—	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	—	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	—	—
S_{X13}	—	—	—	$\frac{1}{6}V_{DC}$	—	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	—	—
S_{X14}	—	—	—	$\frac{1}{6}V_{DC}$	—	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	—	—
C_1	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{4}V_{DC}$
C_2	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{4}V_{DC}$
C_3	—	—	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	—	$\frac{1}{3}V_{DC}$	—	—
C_{f1}	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{4}V_{DC}$	$\frac{1}{2}V_{DC}$
C_{f2}	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	—	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	—	$\frac{1}{8}V_{DC}$
C_{f3}	$\frac{1}{2}V_{DC}$	—	$\frac{1}{3}V_{DC}$	—	—	$\frac{1}{2}V_{DC}$	—	—	—
C_{f4}	$\frac{2}{3}V_{DC}$	—	—	—	—	$\frac{1}{3}V_{DC}$	—	—	—
C_{f5}	$\frac{5}{6}V_{DC}$	—	—	—	—	$\frac{1}{6}V_{DC}$	—	—	—

7.5 Simulation Results

The detailed simulation studies have been carried out using MATLAB/Simulink with PLECS component libraries to validate the proposed converter circuit and the derived control algorithm. The grid parameters and the converter specification for this study are listed in Table 7.7. Fig. 7.9 shows the voltages across the switched capacitors (C_{X1} and C_{X2}), the generated output line and phase voltages before the filter inductors, and the output current of the converter in the steady-state condition. It can be observed that a natural voltage balance is achieved across the switched capacitor voltages, and maintained around its reference value (i.e., $V_{C1} = V_{C2} = V_{DC}$), without using any voltage balancing controller. Also, it is evident that the voltage across the capacitors does not exceed its input DC-source voltage. The fourth and fifth traces in the figure shows the unfiltered line voltage and phase voltage, respectively, for unity power factor operation. The sixth and seventh traces in in the figure shows the grid voltage and the injected current, respectively, which are maintained in phase during unity power factor operation.

Table 7.7 Converter Specification and Grid-Parameters.

Description	Value/Parameter Used
Input voltage (V_{DC})	200 V
Output voltage (v_{ac})	230 V
Sampling frequency (f_s)	50 kHz
Max. switching frequency	25 kHz
Line frequency (f)	50 Hz
Switched capacitors (C_{X1} & C_{X2})	1.5 mF, 250 V
Filter inductor (L_f)	2.5 mH
Switches ($S_{X1} - S_{X6}$)	SCT3022AL
Diode (D_3 & D_6)	C5D50065D
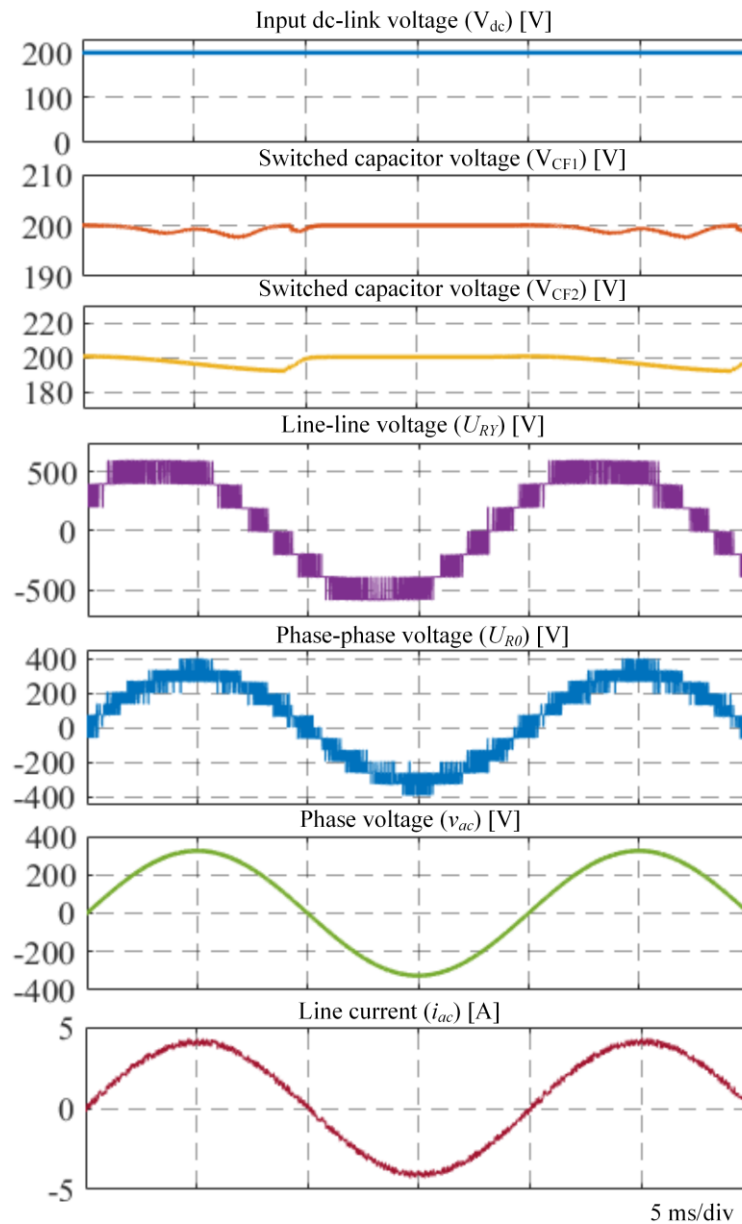
Fig. 7.9 Some important simulated waveforms of the proposed inverter for seven-level operation: input DC source voltage, switched capacitor voltages, line and phase voltages, grid voltage, and inverter output current waveforms.

The voltage and current stress across the semiconductor switches are shown in Fig. 7.10 and Fig. 7.11, respectively. The simulated results show that the voltage stress across the switches (S_{X1}-S_{X5}, S_{X7}) does not exceed the DC input voltage. The maximum voltage stresses across the switch S_{X6} and S_{X8} are 2 and 3 times of the input DC source voltage, respectively.
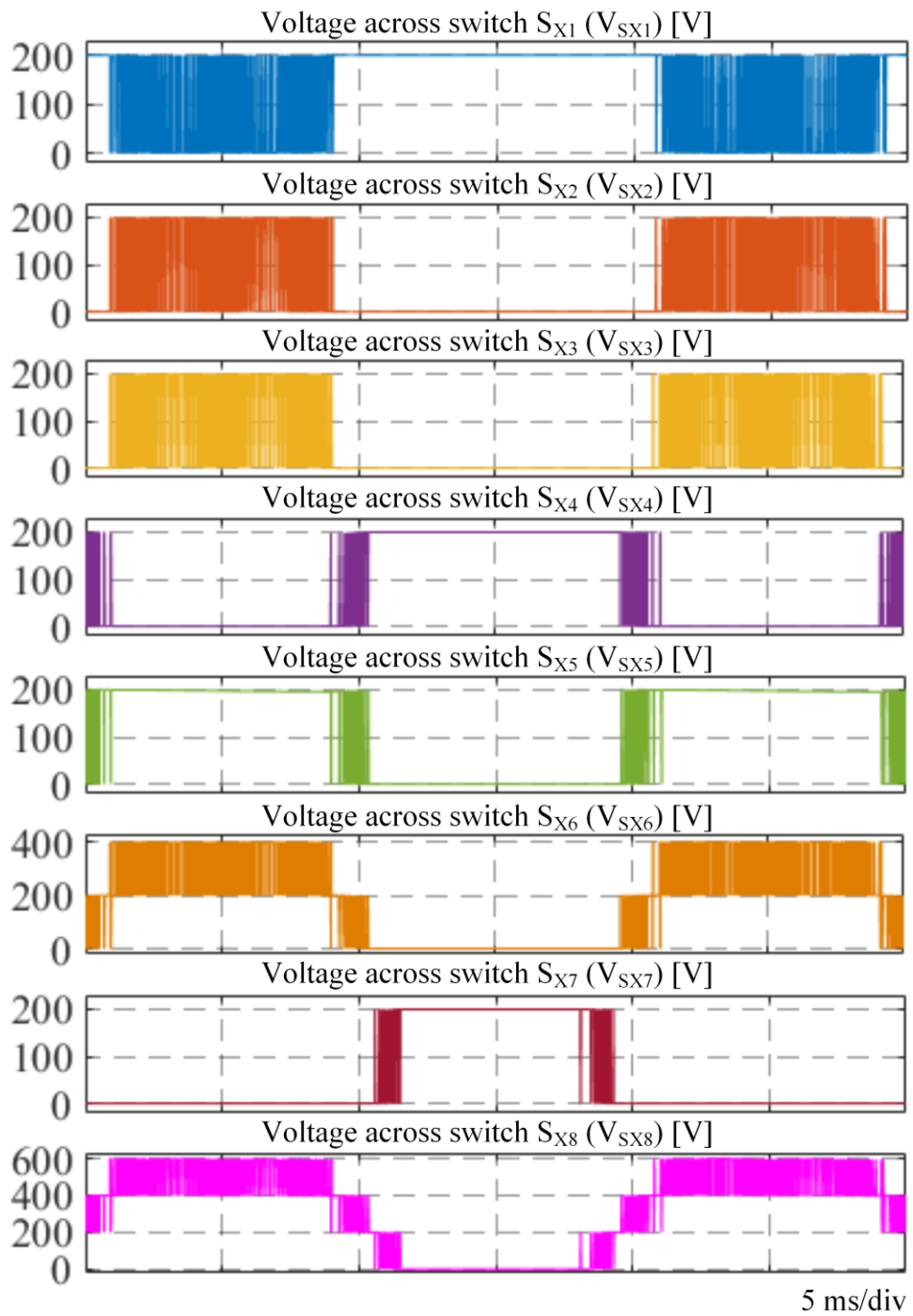
Fig. 7.10 Voltage stress across the switches.
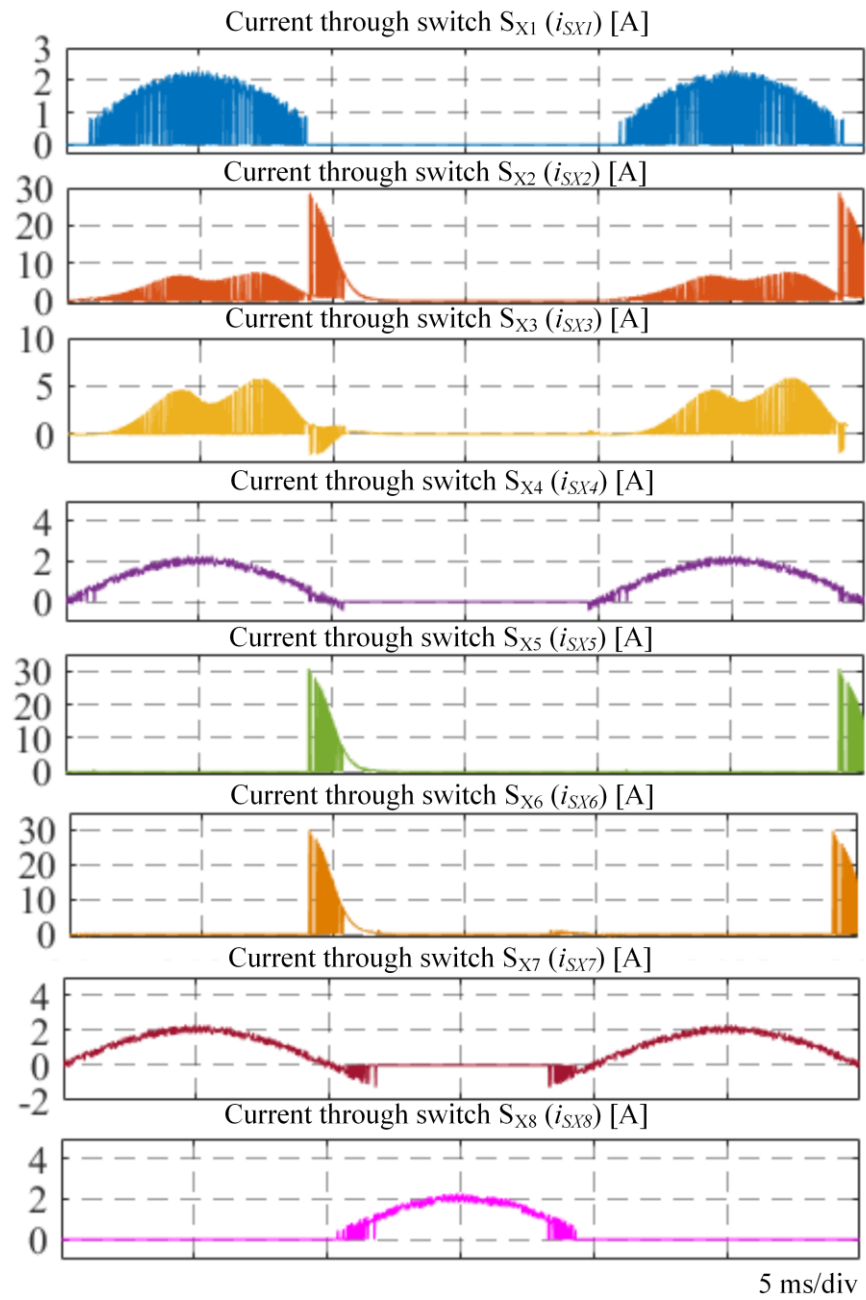
Fig. 7.11 Current stress across the switches.

Fig. 7.12 shows the simulated waveforms during lagging and leading power factor operations. As shown, the balanced voltages are observed across the switched capacitors

during leading and lagging power factors realization. It is also observed that the generated output current does not show any distortion in the negative power region.
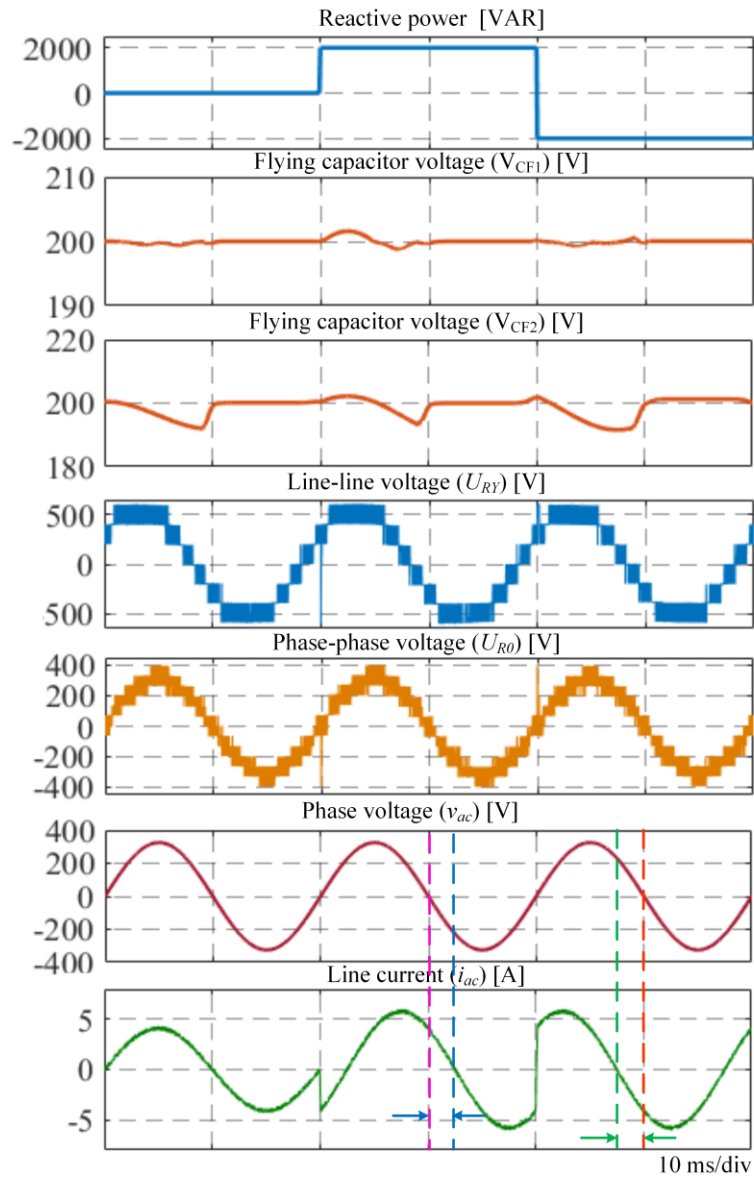
Fig. 7.12 Some simulated waveforms of the proposed inverter during lagging and leading power factors: reactive power references, switched capacitor voltages, line and phase voltages, grid voltage, and inverter output current waveforms.

Fig. 7.13 shows the steady state operating junction temperature of the semiconductor devices.
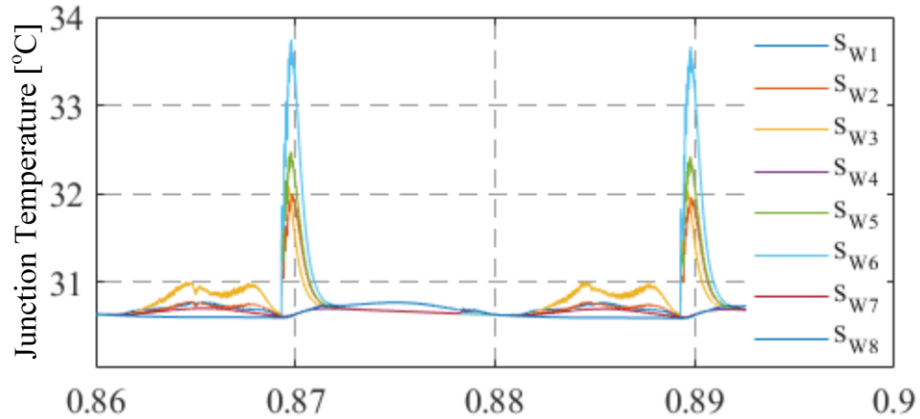
Fig. 7.13 Steady state operating junction temperature of the semiconductor devices.

7.6 OPAL-RT Results

The model of the proposed multilevel inverter concept is validated in OPAL-RT based environment. The line-to-line voltage (before filter) and grid current waveforms are shown in Fig. 7.14 under unity power factor operation. The phase voltage (before filter) and grid voltage waveforms are shown in Fig. 7.15. It can be observed that the proposed topology is capable of generating sinusoidal output current and clean seven-level (line-line) output voltage. The voltage stress across the semiconductor switches are shown in Fig. 7.16. The measurement results show that the voltage stress across the switches (S_{X1}-S_{X5}, S_{X7}) does not exceed the DC input voltage. The maximum voltage stresses across the switch S_{X6} and S_{X8} are two and three times of the input DC source voltage, respectively, which agrees with the analysis presented in the previous simulation section. Fig. 7.17 shows the voltage across the switched capacitors of the proposed topology. As shown, the voltage across the capacitors does not exceed the input DC supply voltage, and a balanced voltage is also observed without using any controller. Note that a 200 V DC voltage supply is sufficient to generate 230 Vrms. By contrast, the conventional and some hybrid topologies require 800 V and 400 V, respectively.

Fig. 7.18 illustrates the obtained results for unity, lagging, and leading power factor modes operation. As shown, the proposed inverter is capable of generating clean sinusoidal current and seven-level voltage even in negative power region. The reference power is

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changed from 1000 W to 1500 W to analyse the transient performance of the predictive controller. The result obtained during this transient operation is shown in Fig. 7.19. As shown, the converter current is instantly changed to realize the reference power value, and a distinct seven-level voltage is also observed during this transient.
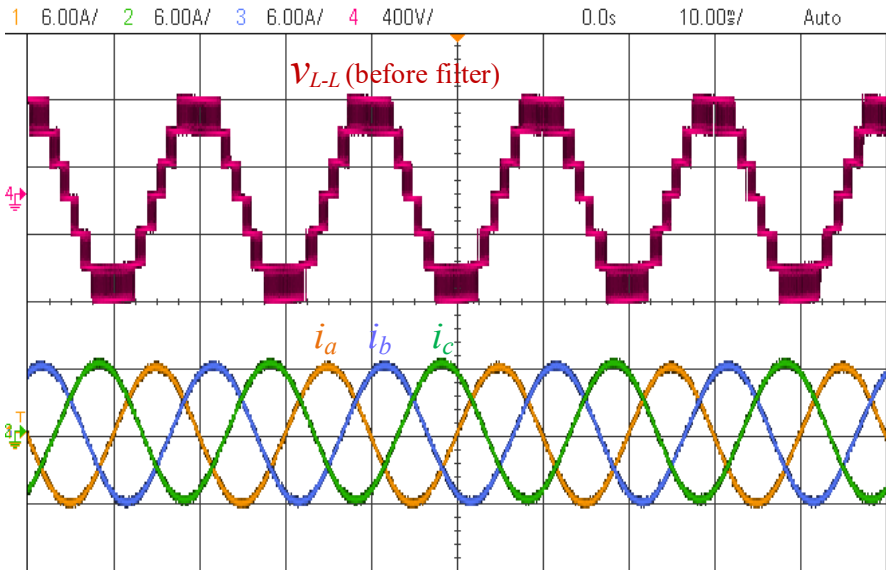
Fig. 7.14 Line voltage and grid current waveforms.
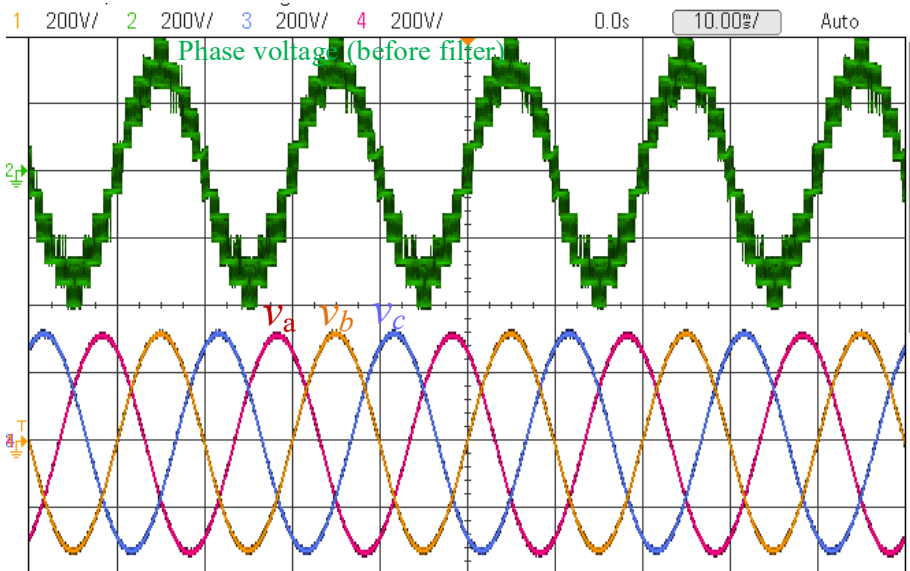
Fig. 7.15 Phase voltage before filter and grid voltage waveforms.
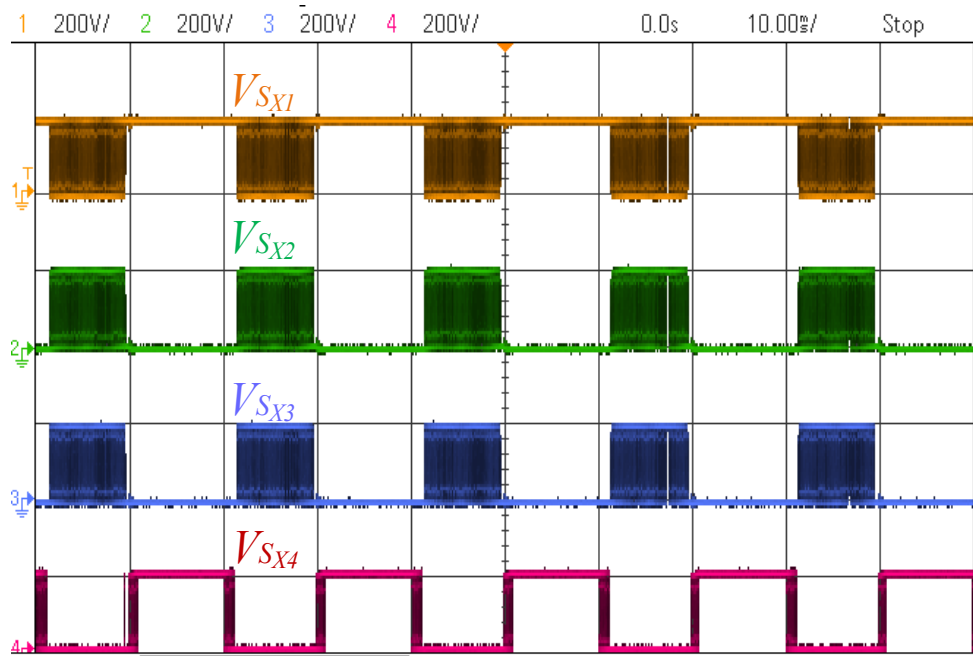
(a)
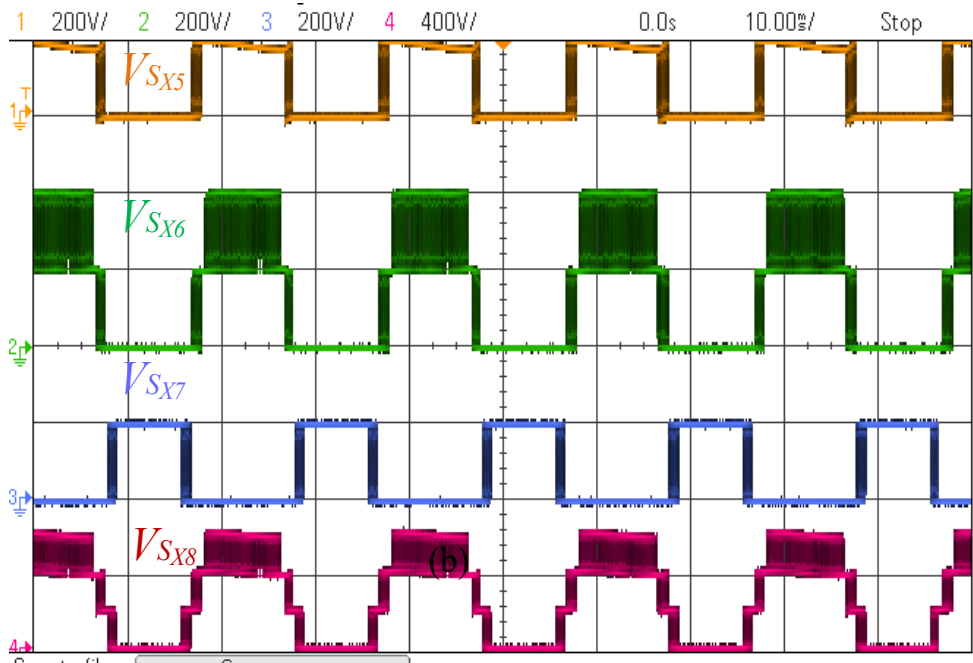
(b)

Fig. 7.16 Voltage stress across the switches.
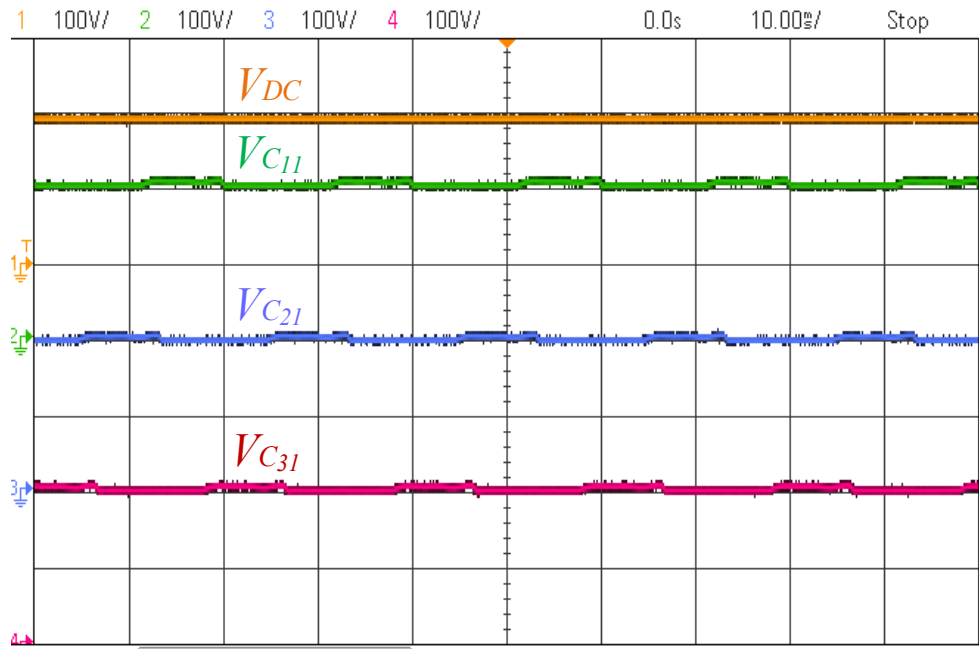
(a)
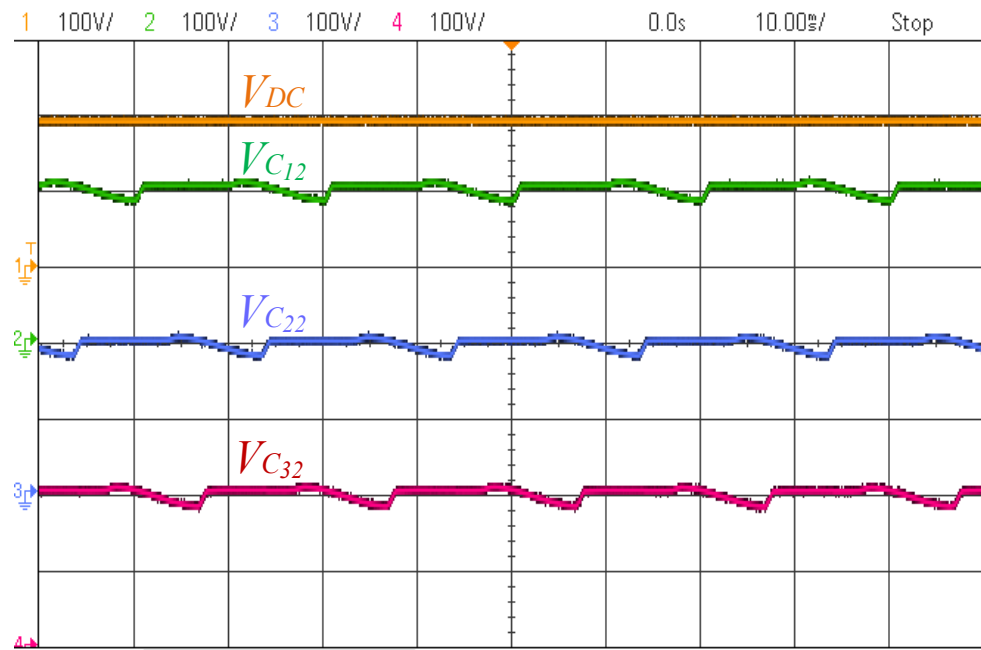
(b)

Fig. 7.17 Voltage across the switched capacitors.
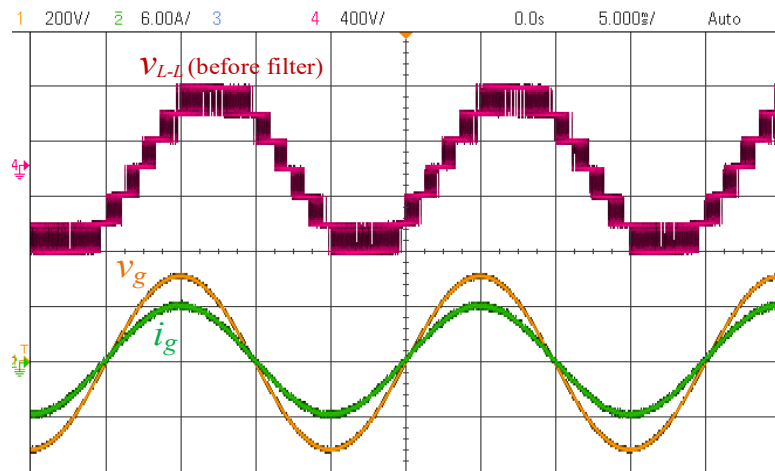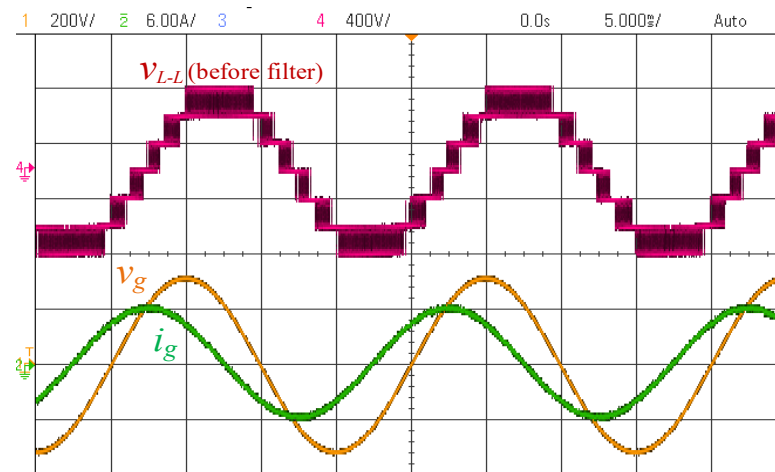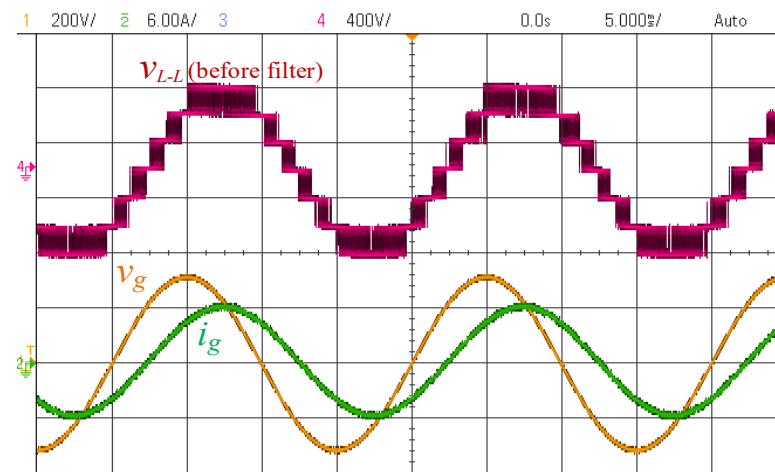
Fig. 7.18 Grid voltage and current waveforms in different power factor, (a) unity power factor, (b) lagging power factor, and (c) leading power factor.
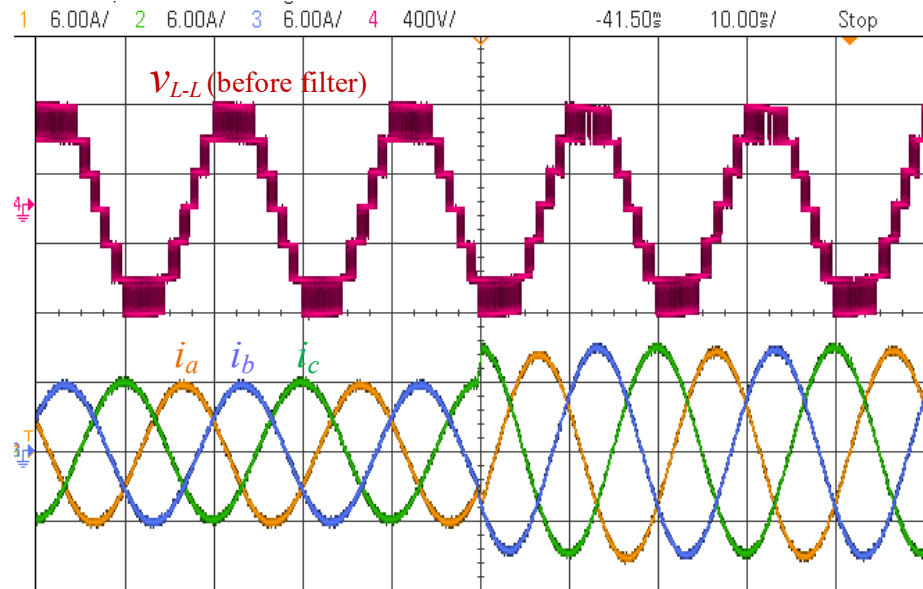
Fig. 7.19 Line to line voltage and current waveforms under transient condition.

7.7 Conclusion

The major works of this chapter is summarized below.

- A new voltage boosting capability-based multilevel inverter topology is presented in this project, which is suitable for grid-connected PV applications.

- The proposed inverter requires a reduced number of components compared to the existing topologies.

- The voltage stresses across the components of the inverter is also less compared to the traditional topologies, which enables the reduction of the system cost and losses.

- This inverter can operate at leading or lagging power factor, and therefore it can be used in grid-connected applications to provide reactive power into the grid.

- A predictive control algorithm is derived to control the inverter, which can realize the desired active and reactive power reference values.

- A benchmarking of multilevel converters is also provided in terms of voltage stress, component count, and DC-bus voltage requirement.

A novel voltage boosting capability-based three-phase multilevel inverter topology is proposed in this research. This topology requires eight active switches and two switched-capacitors for seven-level voltage generation, which is the minimum component count compared to the existing topologies. The voltage stress across the capacitors and switches is minimum compared to the traditional topologies. This topology reduces the DC supply voltage requirement by 75% compared to the existing NPC, ANPC, and CHB topologies, and by 50% compared to hybrid topologies. This feature eliminates the multi-stage DC/DC power conversion system of the grid-connected PV system. In this topology, the number of output voltage levels can be increased by cascading more switched-capacitor units/cells. To control the converter, a finite control set model predictive control algorithm is derived, where a cost function is formulated to operate at any power factor. The inherent self-balanced capacitor's voltage reduces the control complexity and additional sensor circuit requirement. The MATLAB/Simulink and OPAL-RT based environment are used to validate the proposed topology and the associated control scheme.

8 Summary and Future Work

This chapter is the conclusion of the Ph.D. thesis and it consists of a summary as well as some future research directions. The objectives of this chapter are to summarize the works, which have been conducted throughout this Ph.D. project, and proposes some works for future investigation on this research. This section highlights the main contribution of this project – development of robust grid synchronization methods, advanced DC-bus voltage control strategies with disturbance rejection capability, and multilevel converter with voltage boosting capability. Finally, this section ends with future research directions to improve future research outcomes.

8.1 Summary of Research Contributions

This Ph.D. project has addressed the research challenges regarding the robust control of grid-connected multilevel converter systems and high-performance converter topology design. The developed control strategies combine advanced PLLs design for the converter's control unit for estimating the grid parameters under distorted grid conditions, and robust control scheme design to implement disturbance rejection capability-based converter drive. The proposed pPLL structure is capable of estimating the grid voltage amplitude and works effectively at varying grid frequency. Besides, the developed QSG-PLL provides an enhanced filtering capability. The proposed DC-bus voltage control schemes are highly effective in estimating the DC value of the DC-bus voltage without employing any additional filters and realizing regulated DC-bus voltage under uncertain disturbances. The system robustness has been analyzed through detailed mathematical modeling and stability analysis. The proposed system performance has been validated through simulation studies as well as experimental results. Moreover, a voltage boosting capability-based multilevel converter structure and its control techniques have been proposed in this research project, which is suitable for grid-connected PV applications. The developed structure significantly reduces the DC supply voltage requirements, the number of components, and their voltage stresses.

8.1.1 Disturbance Rejection Capability Based Control Scheme

In single-phase AC/DC grid-connected converters, following the desired reference DC-bus is critical under uncertain load disturbances and system parameter variations. The system modeling error and parameter uncertainty has a significant impact on system stability, particularly the DC-bus capacitance variation. This research presents a disturbance rejection capability-based control scheme to compensate the system uncertainty and modeling error. In the proposed control scheme, an extended state observer is applied in parallel with the proportional-integral and sliding mode control scheme to improve the system dynamic and steady-state performances.

8.1.2 Filter-less DC-bus Voltage Ripple Estimation

In single-phase grid-connected converters, the DC-bus voltage consists of a double grid frequency voltage ripple, which must be removed in a closed-loop control system to improve the generated grid current quality. In this thesis, a filter-less method has been presented to estimate the DC-bus voltage ripple. In the proposed method, two SOGI-PLLs were used to estimate the DC-bus voltage ripple. This method shows improved dynamic performance to achieve regulated DC-bus voltage.

8.1.3 Grid Synchronization

In this thesis, two new grid synchronization methods have been presented to estimate the grid voltage fundamental parameters for the grid-tied power converters. A frequency adaptive pPLL structure based on modified WFLC algorithm has been developed in this project. The proposed WFLC-pPLL structure has the capability to estimate the grid voltage amplitude. This method works effectively even under frequency drift. The WFLC-pPLL presents a faster dynamic performance during the grid faults. The detailed experimental studies have been presented under distorted grid conditions and also compared with the traditional ANF-pPLL method. The performance of the proposed method has been compared in terms of frequency tracking under various grid disturbances. In this thesis, a new QSG-PLL has also been presented. The proposed PLL consists of a new modified FLC-based frequency adaptive quadrature signal generator. The proposed QSG presents high-performance in eliminating the

harmonics, sub-harmonics and DC-offset. Therefore, the loop filter in the SRF-PLL can be designed with high bandwidth. As a result, this method shows superior dynamic performance under adverse grid conditions. The proposed PLL works effectively for a wide range of grid frequency. The detailed experimental results have been presented, and the performance has been compared with the popular SOGI-PLL and SOGI-FLL methods.

8.1.4 Voltage Boosting Capability-Based Multilevel Converter

In order to penetrate more power into the grid from renewable energy sources like PV system, advanced converter structure and control strategy have to be developed. The grid-connected PV system should also follow the required grid connection standards, e.g., power quality, reactive power control, and fault ride-through capability. The cost minimization, converter efficiency, and converter size should also be considered during converter design. Multilevel converters have lots of advantages compared to two-level converters. However, those converters required a high DC-link voltage. Thus, a multi-stage DC/DC converter is required, which increases system cost and converter size. A DC voltage boosting capability-based multilevel converter has been proposed in this work, which reduces the DC-bus voltage requirements significantly, the number of components and their voltage stresses. Possible active and reactive power control method using a finite control set model predictive control has been explored with the proposed topology. A benchmarking of multilevel converters was also provided. These comparison results show that the proposed topology presents the best performance in terms of DC-bus voltage requirements, the number of component requirement, and their voltage stresses.

8.2 Possible Future Works

In this thesis, several aspects have been documented for single-phase and three-phase grid-connected power conversion systems. However, there are still many possible works which may improve the system performance. Some important issues which are highly interesting for future studies are listed below:

(1) Regarding the proposed pPLL method, the performance has been verified in the presence of grid harmonics. However, this method suffers from oscillatory errors if the grid voltage is affected by the sub-harmonic. The development of pPLLs with DC-

offset rejection capability is also a challenging task. Hence, this would be an interesting point for future investigation, when the advanced pPLL functionalities are enabled in the future.

(2) Regarding the proposed QSG-PLL method, the small-signal modelling and stability analysis of the proposed method has not yet been conducted. As a whole system, the parameter tuning and stability analysis of the WFLC-PLL might be challenged due to multiple FLC filters in the structure. Hence, this would be an interesting point to investigate.

(3) Regarding the DC-bus voltage control of the single-phase AC/DC converters, the effect of DC-bus capacitance variation in the study of system robustness and stability analysis has been presented. As a complete system, the stability might also be challenged due to grid impedance and A-side filter parameters variation. This might be an interesting topic to look into how those changes affect the system robustness and therefore, to develop a control method as a potential solution. Moreover, the detailed parameter tuning and stability analysis have been carried out for ESO in this thesis. It also calls for a method to calculate the SMC parameters to realize optimized results in terms of settling time, and the stability assessment, which could be another interesting study.

(4) The voltage boosting capability-based three-phase inverter, and its control strategy for PV applications have been proposed in this project. The proposed topology stimulates an issue of inrush current during switched capacitors charging modes. In this case, the power losses might increase and even affect the thermal behavior due to power loss distribution. This issue could be an interesting study to look into and thus to develop an advanced controller as the potential solution to reduce the inrush current. Also, to analyze the proposed topology feasibility from an economic point of view, a detailed benchmark of different state of art topologies is worthy to investigate.

(5) The use of multiple switched capacitor units in a cascaded manner to realize boosted and multilevel output voltage initiates some critical issues to investigate, e.g., fault-tolerant capability and some power device have to block the higher than the DC supply voltage. Also, the common-mode voltage (CMV), low voltage ride through (LVRT)

capability, unsymmetrical loading of power devices, and losses distribution across the power devices might be the interesting research directions.

Besides these interesting study areas, the development of three-phase PLL using FLC filter and its feasibility investigation, application of second-order sliding mode observer for robust DC-bus control might be the interesting research topics. Moreover, applying those control techniques to drive the single-phase and three-phase AC/DC and DC/DC converters is still open, and might be the interesting research direction.

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