DC-Link Voltage Balancing Strategy Based on Optimal Switching Sequences Model Predictive Control for Single-Phase H-NPC Converters

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***Abstract*—In this paper, a model predictive control (MPC) strategy based on the optimal switching sequence (OSS) concept for a single-phase grid-connected H-bridge neutral-point-clamped (HNPC) power converter is presented. The proposed OSS-MPC algorithm considers both the grid current tracking error and the dc-link capacitor voltage balance. Special emphasis is placed on the power converter control region in order to design suitable switching sequence candidates for this multi-objective control problem. Additionally, based on an analysis of the weighting factor effect over closed-loop performance, it is possible to demonstrate that this controller parameter is relatively easy to adjust. In fact, the weighting factor only affects the peak current during transients, with no effect over the steady-state performance. As a result, the proposed OSS-MPC provides a fast closed-loop dynamic to the H-NPC converter, which operates with a fixed switching frequency at all times. This predictive control strategy is experimentally validated in a 3.5 kVA laboratory setup.**

I. Introduction

POWER converters are key components for the penetration of technologies such as renewable energy, energy storage, etc [1], [2]. Among these applications, low-power renewable energy generation, like rooftop photovoltaic (PV), and high-power railway traction systems use single-phase power converters as grid and catenary interface [3]–[5]. One interesting topology for these applications is the single-phase H-bridge neutral-point-clamped (H-NPC) converter. Compared to the conventional H-Bridge converter, an H-NPC can generate up to five output voltage levels and presents high efficiency and compact design as main features.

The research community has paid special attention to develop advantageous control strategies for single-phase grid-connected power converters, including nonlinear control solutions [6], [7]. Among them, model predictive control (MPC) has emerged as an interesting alternative for power converters. This control strategy can manage multiple control targets while including system constraints in the optimal control formulation [8], [9]. In essence, an MPC strategy uses a system model to predict the future behavior of the system outputs up to a finite prediction horizon based on their present values. Then, the predicted system output behavior is evaluated in a cost function to quantify its predicted closed-loop performance. Afterwards, an optimization algorithm is used to solve the resulting optimal control problem defined by the cost function and system constraints. The solution to this optimal control problem results in the control action to be applied to the system. This process is repeated at each sampling instant using a receding horizon policy [10].

On the other hand, one of the most popular MPC control strategies for power converters is the, so-called, finite control set MPC (FCS-MPC). This control methodology considers a finite number of possible control inputs to handle the optimal control problem, e.g., the power converter output voltage vectors. The main advantage is that the optimal control problem can be easily solved, even for multi-objective optimization problems that include system constraints, by evaluating all the possible control inputs in a cost function. Despite this advantage, the main drawback of FCS-MPC is that the power converter being controlled operates with a non-constant switching frequency [11]. As a result, the adoption of FCS-MPC for grid-connected power converter applications is discouraged due to the harmonic content limit imposed by grid codes [12]. For this reason, several modifications have been proposed for FCS-MPC to overcome this problem, which is still an ongoing research [13]–[15].

In this work, the focus is on the recently proposed approach called optimal switching sequence MPC (OSS-MPC) [16]. This consists in defining the control set by using a limited number of possible switching sequences. Then, the optimal control problem is formulated by considering the instant when

The authors gratefully acknowledge the financial support provided by the Spanish Science and Innovation Ministry under project TEC2016-78430-R. This work was also supported by the Chilean Government under Project CONICYT/FONDECYT 1191520.

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power switches change state as control input, which in a way embeds the modulator into the optimization problem. Therefore, OSS-MPC presents two main features: first, as in the conventional FCS-MPC approach, it allows one to work with a multi-objective optimization problem, including system constraints while keeping a limited computational burden; second, by contrast to the FCS-MPC method, it provides a fixed switching frequency, making the approach suitable for grid-connected power converter applications.

This paper adopts the OSS-MPC strategy presented in [17] for a single-phase grid-connected full-bridge H-NPC power converter connected to a unipolar dc-bus. Although the H-NPC can be used to obtain a bipolar dc-bus, allowing the connection of different loads at each dc-link, early studies have shown that there are some limitations in the values of the loads that can be connected to each dc-link [18]. Despite this, some works have proposed some control strategies to address the balance problem in the stable region of the converter [19]. However, to increase the operational range of the bipolar dc-bus, additional circuitry should be added [20], [21]. For this reason, the most common situation is to work with the H-NPC as a unipolar dc-bus. Thus, the load is connected between the positive and negative terminals of the dc-link, while the capacitor middle point is left electrically floating. Under this situation, two main approaches have been presented in the literature to address the dc-link voltage balancing problem. A conventional solution applied to multilevel converters with a modulator stage consists of using the redundant output voltage vectors [22]. This procedure can be also adapted to work with MPC strategies [23]–[25]. Additionally, MPC allows one to formulate a multi-objective optimization problem where both the current control tracking and the dc-link voltage balance problems are included in the cost function. This approach has been extensively used since early works of FCS-MPC for NPC power converters [26] and is the most common solution to this problem when MPC is adopted as control strategy, because it provides the optimal solution for the multi-objective problem [27], [28].

In [17], the OSS-MPC was designed only to track a given current reference. Therefore, the control strategy proposed in [17] is not able to deal with the dc-link voltage unbalance problem [19]. In the paper at hand, OSS-MPC is extended to also balance the dc-link capacitor voltages in an H-NPC. As will be elucidated, incorporating the dc-link problem into the OSS-MPC is not straightforward. To do this, firstly a multi-objective optimization problem is adopted. Then, a careful analysis of the control region to evaluate the effect of the converter voltage vectors over the dc-link balance error is carried out. From this understanding, suitable switching sequence candidates (SSCs) are designed. Moreover, explicit optimal application times expressions for the multi-objective control problem considering the input constraints are obtained off-line. This reduces the computational burden since in a real-time implementation the complexity is reduced to only evaluate these expressions for each SSC. Extensive simulation and experimental results are provided to validate the closed-loop performance of the proposed OSS-MPC strategy for an H-NPC converter.

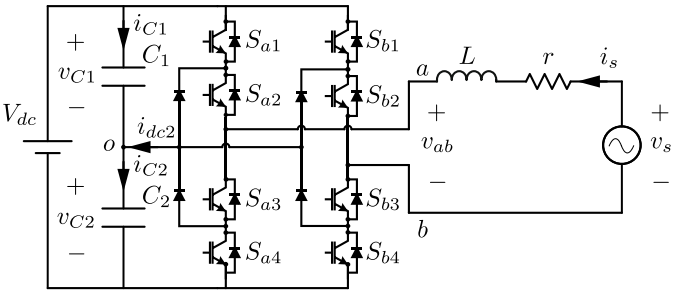

Fig. 1. Schematic circuit of a single-phase grid-connected H-NPC converter fed by a constant dc-voltage source.

II. Single-Phase H-NPC Converter

This section briefly describes a grid-connected single-phase H-NPC converter. The schematic circuit of this converter is depicted in Fig. 1. This converter is electrically fed by a dc-source, V_{dc}, connected in parallel to two dc-link capacitors, C_1 and C_2, to generate a clamping point, o. Ideally, both capacitor voltages should be balanced, i.e., $v_{C1} = v_{C2} = V_{dc}/2$. If achieved, the converter can generate five distinctive voltage levels in the output voltage, v_{ab}, formed between both converter legs.

A. Two-Dimensional Vector Control Region

In an H-NPC converter, the combination of each individual switches, $S_{\chi 1}, \ldots, S_{\chi 4}$, in a leg $\chi \in \{a, b\}$ can be represented by the following switching functions:

$$S_a, S_b \in \{-1, 0, 1\}. \tag{1}$$

Therefore, the combination of these switching functions leads to a two-dimensional control region depicted in Fig. 2, which is formed by nine output voltage vectors, $v_{ab\rho}$, where $\rho \in \{0, \ldots, 8\}$; see Table I. Consequently, similarly to a space vector modulation strategy, the converter output voltage, v_{ab}, can be modulated by properly applying a switching sequence formed with vectors from this finite voltage vector set.

B. System Dynamics

Before selecting a switching sequence, it is convenient to introduce the system dynamics in terms of the output voltage vector, $v_{ab\rho}$. Based on [17], the continuous-time dynamic model of the grid current is given by:

$$\frac{di_s}{dt} = \frac{1}{L}\left(v_s - r i_s - v_{ab\rho}\right) \tag{2}$$

where, L and r are the inductance and resistance of the output filter, and v_s is the grid voltage. Considering that the capacitances of both capacitors are equal, $C_1 = C_2 = C$ then, according to [29], the continuous-time dynamic model for the capacitor voltage balance, $\Delta_v = v_{C2} - v_{C1}$, is represented by:

$$\frac{d\Delta_v}{dt} = \frac{\Delta_i}{C} \tag{3}$$

where Δ_i is expressed by:

$$\Delta_i = \left(S_b^2 - S_a^2\right) i_s. \tag{4}$$

Table I also presents the set of possible Δ_i values.

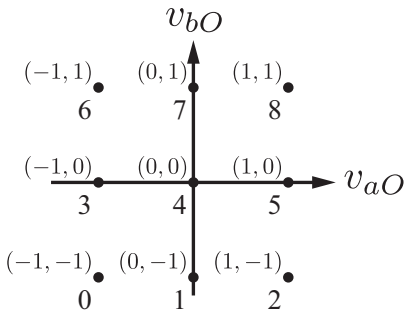

Fig. 2. Finite voltage vector set for a single-phase H-NPC converter. Each vector $\rho \in \{0,\dots,8\}$ is represented by its pair (S_a, S_b)

TABLE I
VOLTAGE VECTORS FOR THE SINGLE-PHASE H-NPC CONVERTER

Vector ρ	0	1	2	3	4	5	6	7	8
$v_{ab\rho}$	0	$\frac{V_{dc}}{2}$	V_{dc}	$\frac{-V_{dc}}{2}$	0	$\frac{V_{dc}}{2}$	$-V_{dc}$	$\frac{-V_{dc}}{2}$	0
Δ_i	0	i_s	0	$-i_s$	0	$-i_s$	0	i_s	0

TABLE II
VOLTAGE VECTOR EFFECT OVER Δ_v

Voltage vector	$i_s > 0$	$i_s < 0$
$\{0,2,4,6,8\}$	–	–
$\{1,7\}$	$\uparrow$	$\downarrow$
$\{3,5\}$	$\downarrow$	$\uparrow$

III. SSCs DESIGN

As proposed in [17], an H-NPC converter can be controlled by selecting a switching sequence, Seq, composed by three voltage vectors from the finite voltage vector set, i.e.:

$$Seq = \{v_{abj,1}, v_{abk,2}, v_{abl,3}\} \tag{5a}$$
$$T = \{t_1, t_2, t_3\}\,. \tag{5b}$$

where the $j,k,l \in \{0\cdots 8\}$. Moreover, T is the vector which contains the application times, t_n with $n \in \{1,2,3\}$, that each vector in Seq is applied during a sampling period T_s, i.e., $T_s = t_1 + t_2 + t_3$.

In [17], SSCs were designed with the aim of controlling the converter output current. However, the work at hand also aims to balance the dc-link capacitor voltages. Therefore, new SSCs need to be designed accordingly. To address this issue, the effect of the voltage vectors, $v_{ab\rho}$, over the signal Δ_v is analyzed in Fig. 3 for $i_s > 0$. Taking into account (4) and the fact that the current i_s is defined as being injected to the inverter in Fig. 1, the voltage vectors represented by a square (■) do not produce any variation on Δ_v. The vectors represented by an upward-pointing triangle (▲) produce an increase on Δ_v, whereas those represented by downward-pointing triangles (▼) decrease the value of Δ_v. An equivalent analysis can be done for $i_s < 0$, where similar conclusions can be drawn but in this case the effect over the signal Δ_v

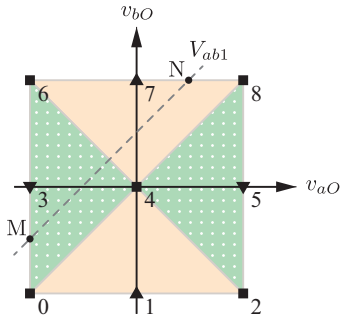

Fig. 3. Effect of voltage vectors over Δ_v for $i_s > 0$.

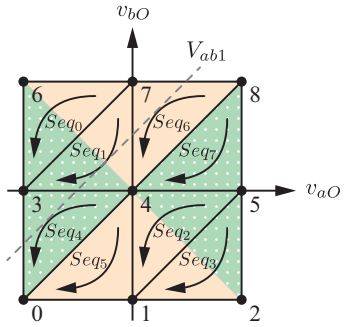

Fig. 4. Voltage vector sequences for the balancing problem.

is the opposite. Table II summarizes the voltage vector effect over Δ_v. Hereafter, only the analysis for $i_s > 0$ is described in detail.

When $i_s > 0$, the control region can be split into four different areas depending on how Δ_v varies. These areas are marked in Fig. 3. Now, it is convenient to introduce an equivalent control signal, v_m, to represent the average value of these voltage vectors, i.e.:

$$v_m = \frac{1}{T_s}\left(v_{abj,1}t_1 + v_{abk,2}t_2 + v_{abl,3}t_3\right). \tag{6}$$

Any resulting equivalent control signal, v_m, that lies in the dotted area, formed by voltage vectors $\{0,3,4,6\}$ and $\{2,4,5,8\}$, decreases the value of Δ_v. On the contrary, any v_m that lies in the solid area, constituted by $\{0,1,2,4\}$ and $\{4,6,7,8\}$, increases the value of Δ_v. Also, any v_m that belongs to a line with a slope of $45°$ provides the same average output voltage in the inverter [30]. This is illustrated in Fig. 3, where all the points located over the segment $\overline{MN}$ generate an average output voltage equal to $v_m = V_{ab1}$. This implies that it is possible to control the grid current and balance the dc-link capacitor voltages independently.

Based on the above analysis, the proposed SSCs are presented in Fig. 4 and listed in Table III. These eight SSCs are designed with the aim to only switch between two adjacent voltage levels. For instance, if sequence Seq_0 is finally selected then, v_{ab} will vary between $-V_{dc}/2$ and $-V_{dc}$. Additionally, any equivalent control signal, v_m, can be generated using an area that increases or decreases Δ_v. For example, in Fig. 4 the equivalent control signal $v_m = V_{ab1}$ can be produced by the sequences Seq_1, Seq_4 and Seq_6. Note that, as shown in Table II, Seq_4 tends to decrease Δ_v because it is composed by vector 3, that decreases the value of Δ_v for $i_s > 0$, and vectors

0 and 4, that do not affect Δ_v. Therefore, any combination of these vectors will decrease Δ_v. Similarly, any combination of voltage vectors from Seq_6 leads to increase Δ_v. Finally, since vectors 7 and 3 are inside Seq_1, then the effect of using Seq_1 over Δ_v will depend on the final application times for the voltage vectors therein. As a conclusion, the proposed set of SSCs guarantees that the dc-link capacitor voltages can always be balanced.

Furthermore, the set of SSCs can be reduced as follows. If $\Delta_v > 0$ then, SSCs Seq_5 and Seq_6 could be not evaluated since they will further increase Δ_v. Similarly, if $\Delta_v < 0$ then, Seq_4 and Seq_7 could be not considered. Under this consideration, only six SSCs have to be evaluated instead of the original eight SSCs, providing a reduction of roughly 25% in the computational cost of the algorithm compared to the original implementation, without affecting its performance. Finally, the SSCs evaluated in the algorithm are summarized in Table IV.

TABLE III
VOLTAGE VECTORS SEQUENCE FOR THE BALANCING PROBLEM

m	Seq_m	m	Seq_m
0	$\{7,6,3\}$	4	$\{4,3,0\}$
1	$\{7,4,3\}$	5	$\{4,1,0\}$
2	$\{5,4,1\}$	6	$\{8,7,4\}$
3	$\{5,2,1\}$	7	$\{8,5,4\}$

TABLE IV
SEQUENCE CANDIDATES FOR THE BALANCING PROBLEM

	$\Delta_v \geq 0$	$\Delta_v < 0$
$i_s \geq 0$	$\left\{ \begin{matrix} Seq_0, Seq_1, Seq_2, \\ Seq_3, Seq_4, Seq_7 \end{matrix} \right\}$	$\left\{ \begin{matrix} Seq_0, Seq_1, Seq_2, \\ Seq_3, Seq_5, Seq_6 \end{matrix} \right\}$
$i_s < 0$	$\left\{ \begin{matrix} Seq_0, Seq_1, Seq_2, \\ Seq_3, Seq_5, Seq_6 \end{matrix} \right\}$	$\left\{ \begin{matrix} Seq_0, Seq_1, Seq_2, \\ Seq_3, Seq_4, Seq_7 \end{matrix} \right\}$

IV. OSS-MPC FORMULATION FOR A SINGLE-PHASE H-NPC CONVERTER

An H-NPC converter is operated to simultaneously track a grid current reference and balance the dc-link capacitor voltages. In this work, the OSS-MPC strategy presented in [17] is adapted to achieve these control targets. Since this is a multivariable control problem, the following quadratic cost function is chosen as part of the problem formulation:

$$J = e_{i,k+1}^2 + \lambda e_{\Delta_v,k+1}^2, \tag{7}$$

where $e_{i,k+1} = i_{s,k+1}^\star - i_{s,k+1}$ is the grid current tracking error, while $e_{\Delta_v,k+1} = \Delta_{v,k+1}^\star - \Delta_{v,k+1}$ is the dc-link voltage balance error at the next sampling instant, $k+1$. Moreover, by using an ℓ_2-norm, stability of OSS-MPC may be studied using approaches like the ones in [31] or [32]. The weighting factor $\lambda \geq 0$ is a tuning parameter that adjusts the trade-off (relative importance) between both control targets. Then, the key idea in an OSS-MPC formulation is to represent these tracking errors as a function of an SSC, Seq_m, and its associated an application time vector T_m. Therefore, the OSS-MPC strategy should provide the optimal pair $\{Seq^{\text{opt}}, T^{\text{opt}}\}$.

A. Grid Current Tracking Error

Considering (2), the rate of change of the grid current caused by each output voltage vector in an SSC, Seq_m, is given by:

$$f_{i_s n} = \left.\frac{di_s}{dt}\right|_{v_{ab\rho,n}} = \frac{1}{L}\left(v_s - r i_s - v_{ab\rho,n}\right), \forall \rho \in \{0 \cdots 8\}. \tag{8}$$

with $n \in \{1,2,3\}$. Following the steps in [17], the predicted grid current tracking error, $e_{i,k+1}$, can be computed as:

$$e_{i,k+1} = e_{i0} - \Big(\left(f_{i_s 1} - f_{i_s 3}\right) t_1 + \left(f_{i_s 2} - f_{i_s 3}\right) t_2 + f_{i_s 3} T_s \Big), \tag{9}$$

where $e_{i0} = i_{s,k+1}^\star - i_{s,k}$, in which $i_{s,k}$ is the measured grid current at the sampling instant k. Moreover, t_n, are the application times as per (5b).

B. DC-Link Capacitor Voltage Balance

Similarly to the grid current case and taking into account (3), the rate of change of the dc-link capacitor voltage balance, Δ_v, caused by each output vector in an SSC, Seq_m, is represented by:

$$f_{\Delta_v n} = \left.\frac{d\Delta_v}{dt}\right|_{v_{ab\rho,n}}. \tag{10}$$

Then, following the OSS-MPC principle, the next step dc-link voltage balanced error, $e_{\Delta_v,k+1}$, generated by an SSC, Seq_m, can be predicted by calculating the following expression:

$$e_{\Delta_v,k+1} = e_{\Delta_v 0} + \left(f_{\Delta_v 1} - f_{\Delta_v 3}\right) t_1 + \left(f_{\Delta_v 2} - f_{\Delta_v 3}\right) t_2 + f_{\Delta_v 3} T_s \tag{11}$$

where $e_{\Delta_v 0} = \Delta_{v,k+1}^\star - \Delta_{v,k}$, in which $\Delta_{v,k} = v_{C2,k} - v_{C1,k}$ represents the dc-link capacitor voltage difference value at the instant k and $\Delta_{v,k+1}^\star$ is the desired dc-link voltage balance error at the next sampling instant $k+1$, which generally is 0.

C. OSS-MPC Problem

Considering (9) and (11), for each SSC, Seq_m, the cost function (7) can be expressed as a function of the application times, t_n, as per (5b). Consequently, both the OSS and optimal application times are obtained by solving, at each sampling instant k, the following problem:

$$\{Seq^{\text{opt}}, T^{\text{opt}}\} = \arg\min_{Seq_m} \left\{ \min_{T_m} \ \{J(Seq_m, T_m)\} \right\} \tag{12a}$$

$$\text{subject to:} \quad t_n \geq 0, \ \forall n \in \{1,2,3\} \tag{12b}$$

$$T_s = t_1 + t_2 + t_3. \tag{12c}$$

Note that the OSS-MPC problem considers two optimizations. Firstly, for each Seq_m, an optimal application time vector, T_m^{opt}, is obtained (internal optimization). Then, considering these optimal times, each pair $\{Seq_m, T_m^{\text{opt}}\}$ is evaluated into the cost function. Finally, the OSS, Seq^{opt}, is the Seq_m that

$$t_1\Big|_{Seq_m} = \frac{e_{i0}\,(f_{\Delta_v 3}-f_{\Delta_v 2})+e_{\Delta_v 0}\,(f_{i_s 3}-f_{i_s 2})+T_s\,(f_{i_s 3}f_{\Delta_v 2}-f_{i_s 2}f_{\Delta_v 3})}{(f_{i_s 1}\,(f_{\Delta_v 3}-f_{\Delta_v 2})+f_{i_s 2}\,(f_{\Delta_v 1}-f_{\Delta_v 3})+f_{i_s 3}\,(f_{\Delta_v 2}-f_{\Delta_v 1}))} \tag{17}$$

$$t_2\Big|_{Seq_m} = \frac{e_{i0}\,(f_{\Delta_v 1}-f_{\Delta_v 3})+e_{\Delta_v 0}\,(f_{i_s 1}-f_{i_s 3})+T_s\,(f_{i_s 1}f_{\Delta_v 3}-f_{i_s 3}f_{\Delta_v 1})}{(f_{i_s 1}\,(f_{\Delta_v 3}-f_{\Delta_v 2})+f_{i_s 2}\,(f_{\Delta_v 1}-f_{\Delta_v 3})+f_{i_s 3}\,(f_{\Delta_v 2}-f_{\Delta_v 1}))} \tag{18}$$

$$t_3\Big|_{Seq_m} = T_s - t_1 - t_2. \tag{19}$$

provides the minimum cost (external optimization), being its associated application times the optimal one, i.e., T^{opt}.

V. Solution to the OSS-MPC Problem

A. Unconstrained Optimal Application Times

In OSS-MPC, it is firstly required to solve the internal optimization, i.e., to obtain the optimal applications time, T_m^{opt} for each Seq_m. To do this, the constrains (12b)-(12c) can be firstly neglected, i.e., $t_n \in \mathbb{R}$. Since these application times are continuous variables, one can perform a partial derivative of the cost function to obtain the unconstrained optimal times, i.e.:

$$\frac{\partial J}{\partial t_1}\Big|_{Seq_m} = 0 \;\;;\;\; \frac{\partial J}{\partial t_2}\Big|_{Seq_m} = 0. \tag{13}$$

Considering (9), (11) and (7), the equation system (13) yields:

$$-2\,(f_{i_s 1}-f_{i_s 3})\,A + 2\lambda\,(f_{\Delta_v 1}-f_{\Delta_v 3})\,B = 0 \tag{14a}$$
$$-2\,(f_{i_s 2}-f_{i_s 3})\,A + 2\lambda\,(f_{\Delta_v 2}-f_{\Delta_v 3})\,B = 0, \tag{14b}$$

where

$$A \triangleq e_{i0} - (f_{i_s 1}-f_{i_s 3})\,t_1 - (f_{i_s 2}-f_{i_s 3})\,t_2 - f_{i_s 3}T_s \tag{15}$$
$$B \triangleq e_{\Delta_v 0} + (f_{\Delta_v 1}-f_{\Delta_v 3})t_1 + (f_{\Delta_v 2}-f_{\Delta_v 3})t_2 + f_{\Delta_v 3}T_s. \tag{16}$$

By analyzing the equation system (14a)-(14b), it is possible to observe that this system has a unique solution only if $A = B = 0$. Therefore, it can be concluded that the weighting factor, λ, does not have any effect over the unconstrained optimal solution of the problem (13). Finally, solving (15)-(16) with $A = B = 0$ leads to the unconstrained optimal application time vector, $T_m = \{t_1, t_2, t_3\}$, where each application times, t_n, is explicitly represented by (17)-(19).

B. Constrained Application Times

If for a given Seq_m, its application time vector, T_m, computed from (17)-(19) fulfills (12b)-(12c) then, its associated equivalent control signal, v_m, calculated from (6) will be located inside its corresponding sector. On the contrary, if these constraints are not satisfied then, v_m will lie outside the sector limits. Therefore, the equivalent control signal cannot be generated by the inverter in practice. To solve this problem, a new application time vector, T_m, should be obtained taking into account system constraints and the effect of v_m over both i_s and Δ_v. This situation is shown in Fig. 5 for an equivalent control signal generated by the voltage vectors in Seq_0 and $i_s \geq 0$. A similar analysis can be carried out for the other SSCs and $i_s < 0$. However, for the sake of brevity, the study is only presented for Seq_0.

TABLE V
Constrained Time Intervals for Sequence Seq_0 when $i_s \geq 0$

Condition	t_1	t_2	t_3
$v_m < -V_{dc}$	0	T_s	0
$v_m > -V_{dc}/2$ and $\Delta_v > 0$	0	0	T_s
$v_m > -V_{dc}/2$ and $\Delta_v < 0$	T_s	0	0
$-V_{dc} < v_m < -V_{dc}/2$ and $\Delta_v < 0$	$T_s - t_2$	$-\left(\frac{2v_m}{V_{dc}}+1\right)T_s$	0
$-V_{dc} < v_m < -V_{dc}/2$ and $\Delta_v > 0$	0	$-\left(\frac{2v_m}{V_{dc}}+1\right)T_s$	$T_s - t_2$

Four different situations are highlighted in Fig. 5 for the sequence Seq_0. The first one appears when $v_m < -V_{dc}$. As the minimum output voltage that the inverter can produce is $-V_{dc}$. Then, during the whole sampling period only the output voltage vector 6 is applied (Fig. 5(a)). The second scenario arises if $v_m > -V_{dc}/2$. If the largest output voltage that sequence Seq_0 can produce is $-V_{dc}/2$ then, the output should be limited to this value. To produce this voltage value, output voltage vectors 3 and 7 can be used. If $\Delta_v \geq 0$ then voltage vector 3 is used; otherwise, 7 is selected (Fig. 5(b)). Finally, when condition $-V_{dc} < v_m < -V_{dc}/2$ holds, it is possible to generate the same average output voltage located in one of the edge of Seq_0. For this purpose, a combination of output voltage vectors in the sets $\{7, 6\}$ or $\{6, 3\}$ (Figs. 5(c) and 5(d)) can be used. The set $\{6, 3\}$ is chosen when $\Delta_v \geq 0$, otherwise, $\{7, 6\}$ is used. This analysis leads to the modified application times for Seq_0 when $i_s \geq 0$ presented in Table V.

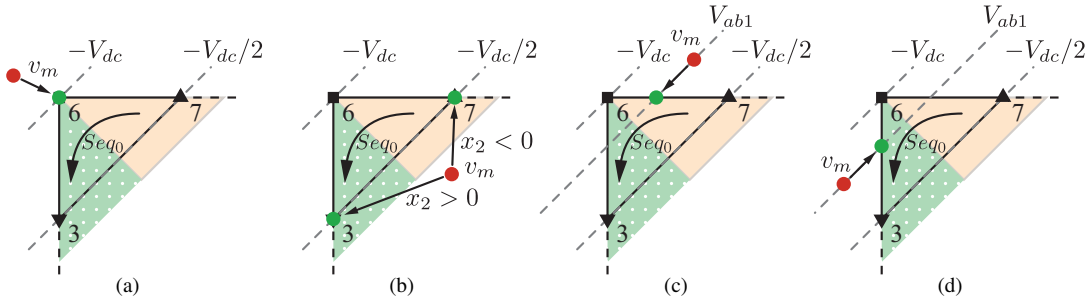

Fig. 5. Computation of time intervals for sequence Seq_0 according to system constraints when $i_s \geq 0$: (a) $v_m < -V_{dc}$, (b) $v_m > -V_{dc}/2$, (c) $-V_{dc} < v_m < -V_{dc}/2$ and $\Delta_v < 0$, (d) $-V_{dc} < v_m < -V_{dc}/2$ and $\Delta_v > 0$.

C. Analysis of the Weighting Factor Effect

In general, weighting factors have an important effect over the MPC performance, specially when FCS-MPC is adopted. Although there are some proposals to design these values it is still an open issue [33], [34]. Here, to analyze the effect of the weighting factor λ over the optimal application times, (15) and (16) should be studied. Note that $A = e_{i,k+1}$ and $B = e_{\Delta_v,k+1}$. Therefore, independently of λ, the cost function designed in (7) will become 0 whenever the application times computed from (17)-(19) fulfill (12b)-(12c). This is an important advantage over the FCS-MPC approach. FCS-MPC only considers a finite set of output voltage vectors applied during the whole sampling period. Thus, in general, there is no guarantee that the cost function will become zero for any of the output voltage vectors candidates. By contrast, the proposed OSS-MPC will always choose a pair $\{Seq_m, T_m\}$, that satisfies this condition, when available, as the optimal one, since this is the minimum possible value for the cost function. This will be the most common situation during a steady state operation of the H-NPC converter, as long as the converter actual power is equal or less than its rated power. Therefore, the steady-state performance of an H-NPC converter governed by the proposed OSS-MPC strategy is independent of the control design parameter, λ. In this sense, the value of λ may have an effect over the closed-loop performance only during transients, when the pair $\{Seq_m, T_m\}$ may not fulfill the optimal problem constraints and the constrained application times computed in Section V-B should be used. This is an important feature of the proposed control strategy compared to other approaches. In general, for other control strategies, the weighting factor also affects to the system performance in steady state. Therefore, the proposed control strategy eases the design process of λ.

D. OSS-MPC Implementation

Once suitable application time vectors, T_m, are calculated for each Seq_m then, the second optimization stage needs to be addressed to obtain the OSS, Seq^{opt}. Since the number of SSCs is finite, 8 in this case, the cost function (7) can be evaluated for each pair $\{Seq_m, T_m\}$, in a similar fashion than FCS-MPC. Therefore, the OSS and its associated application time vector, $\{Seq^{\text{opt}}, T^{\text{opt}}\}$, are selected as the ones that minimize J in (7). Finally, implementation of the OSS, Seq^{opt}, can be performed as described in Table VI, where δ_{1a} and δ_{2a} stand

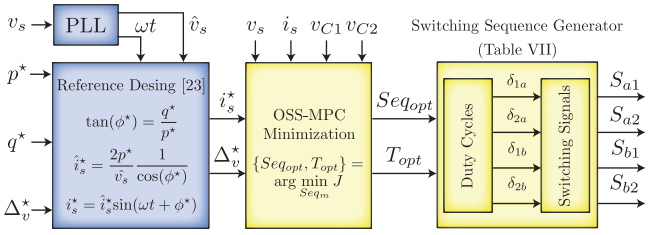

Fig. 6. Block diagram of the proposed OSS-MPC strategy.

for the duty cycles of the power switches S_{a1} and S_{a2} in the converter leg a, respectively, while δ_{1b} and δ_{2b} represent the duty cycles of the power switches S_{b1} and S_{b2} in the converter leg b, respectively. Fig. 6 represents the block diagram of the proposed strategy, where the reference design [35] and PLL, [36] are used to generate the reference current.

VI. Results

A. Simulation Results

Simulation results of a single-phase grid-connected H-NPC converter using the proposed dc-link voltage balancing OSS-MPC strategy are presented to analyze the weighting factor effect over the closed-loop response. The following results are obtained to match the parameters shown in Table VII of the experimental setup. All the results reported are designed to obtain a converter output voltage with dominant harmonic components fixed around 5 kHz, while the switching frequency (f_{sw}) is 2.5 kHz. Figure 7 shows results for the OSS-MPC using $\lambda = 1$. The weighting factor λ can be used for defining the time needed to achieve the capacitor voltage balance. However, large values of λ will increase the peak current during the transient. In addition, the settling time will depend on the system parameters. To avoid this situation, it is proposed to define a dynamic reference for the dc-link unbalance reference $\Delta^\star_{v,k+1}$. The approach defines a ramp that decays from its initial value $\Delta^\star_{v,k+1} = v^\star_{C2,k+1} - v^\star_{C1,k+1}$ to $\Delta^\star_{v,k+1} = 0$ in a given time. The main advantage with this approach is that the settling time is independent of λ. In that case, λ will only have an affect over the peak current value during the transient. Here, the ramp slope is set to achieve the balanced condition in 250 ms starting from an arbitrary unbalanced voltage difference equal to 20 V. Smaller values for the settling time can be used but there is a limit for which the dc-link voltage balancing performance is affected by the

TABLE VI
SWITCHING DUTY CYCLES FOR THE BALANCING PROBLEM

Sequence	$v_{ab\rho}$	S_a S_b	S_{a1} S_{a2}	S_{b1} S_{b2}	Duty
0	7	0 1	0 1	1 1	$\delta_{1a}=0$
	6	−1 1	0 0	1 1	$\delta_{2a}=\frac{t_1}{T_s}$
	3	−1 0	0 0	0 1	$\delta_{1b}=\frac{t_1+t_2}{T_s}$
					$\delta_{2b}=1$
1	7	0 1	0 1	1 1	$\delta_{1a}=0$
	4	0 0	0 1	0 1	$\delta_{2a}=\frac{t_1+t_2}{T_s}$
	3	−1 0	0 0	0 1	$\delta_{1b}=\frac{t_1}{T_s}$
					$\delta_{2b}=1$
2	5	1 0	1 1	0 1	$\delta_{1a}=\frac{t_1}{T_s}$
	4	0 0	0 1	0 1	$\delta_{2a}=1$
	1	0 −1	0 1	0 0	$\delta_{1b}=0$
					$\delta_{2b}=\frac{t_1+t_2}{T_s}$
3	5	1 0	1 1	0 1	$\delta_{1a}=\frac{t_1+t_2}{T_s}$
	2	1 −1	1 1	0 0	$\delta_{2a}=1$
	1	0 −1	0 1	0 0	$\delta_{1b}=0$
					$\delta_{2b}=\frac{t_1}{T_s}$
4	4	0 0	0 1	0 1	$\delta_{1a}=0$
	3	−1 0	0 0	0 1	$\delta_{2a}=\frac{t_1}{T_s}$
	0	−1 −1	0 0	0 0	$\delta_{1b}=0$
					$\delta_{2b}=\frac{t_1+t_2}{T_s}$
5	4	0 0	0 1	0 1	$\delta_{1a}=0$
	1	0 −1	0 1	0 0	$\delta_{2a}=\frac{t_1+t_2}{T_s}$
	0	−1 −1	0 0	0 0	$\delta_{1b}=0$
					$\delta_{2b}=\frac{t_1}{T_s}$
6	8	1 1	1 1	1 1	$\delta_{1a}=\frac{t_1}{T_s}$
	7	0 1	0 1	1 1	$\delta_{2a}=1$
	4	0 0	0 1	0 1	$\delta_{1b}=\frac{t_1+t_2}{T_s}$
					$\delta_{2b}=1$
7	8	1 1	1 1	1 1	$\delta_{1a}=\frac{t_1+t_2}{T_s}$
	5	1 0	1 1	0 1	$\delta_{2a}=1$
	4	0 0	0 1	0 1	$\delta_{1b}=\frac{t_1}{T_s}$
					$\delta_{2b}=1$

TABLE VII
SYSTEM PARAMETERS

Variable	Description	Value	p.u.
S_r	Total rated apparent power	3.5 kVA	1
v_s	Grid voltage	230 V	1
V_{dc}	DC-link voltage	400 V	1
C_1, C_2	DC-link capacitors	2475 μF	0.085
L	Filter inductor	10 mH	0.20
r	Filter resistance	2.01 mΩ	0.013
f_s	Sampling frequency	5 kHz	1
f_{sw}	Switching frequency	2.5 kHz	0.5
T_e	Execution time	26.2 μs	0.13T_s

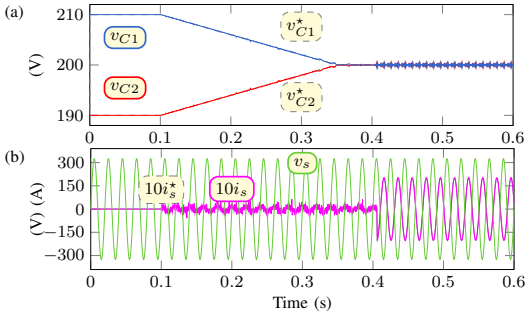

Fig. 7. Capacitor voltage balancing (OSS-MPC): (a) capacitor voltages and (b) grid voltage and grid current.

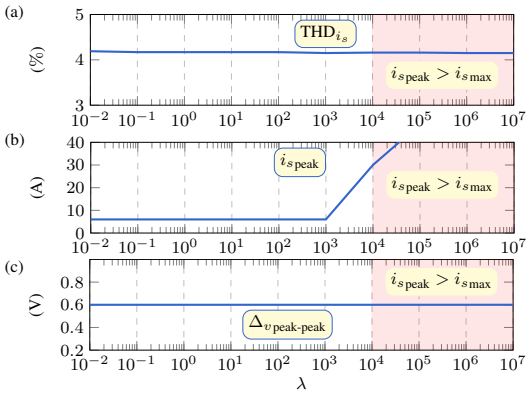

Fig. 8. Weighting factor effect over (OSS-MPC): (a) THD of i_s, (b) peak value of i_s during the balancing transient, and (c) steady-state Δ_v ripple.

system parameters. Therefore, from the practical point of view, it is recommended to define the settling time in the range from 60 ms to 300 ms. Note that this ramp resembles a standard start-up procedure for grid-connected inverters, so $i_s^\star$ is set to zero. This is an extreme condition for the controller because it has to balance v_{C1} and v_{C2} without loosing the tracking of $i_s \approx 0$. In addition, the trade-off between the THD of i_s, its peak value during the balancing transient and the steady-state Δ_v ripple for different values of λ is analyzed in Fig. 8. This figure shows that the range of possible values for λ is only limited by the current peak value during the balancing transient. Therefore, λ must be chosen to keep i_{speak} below the maximum converter current i_{smax}.

For comparison purposes, same results and analysis for FCS-MPC [35] considering the cost function in (7) are shown in Fig. 9 and Fig. 10 respectively. Here, the sampling frequency $f_s = 1/T_s = 12$ kHz and $\lambda = 700$ are set to achieve a similar steady-state performance compared to OSS-MPC, i.e., $\text{THD}_{i_s} = 4.20\%$. The axes limits in Fig. 10 are intentionally set as per Fig. 8 in order to demonstrate that FCS-MPC achieves similar results. However, there is a lower limit for λ in which the steady-state Δ_v ripple is increased. Below this limit, FCS-MPC is not able to balance i.e. $v_{C1} \not\approx v_{C2}$. Note that OSS-MPC also extends the upper limit for λ for the same i_{smax}. As a result, the OSS-MPC performance is almost

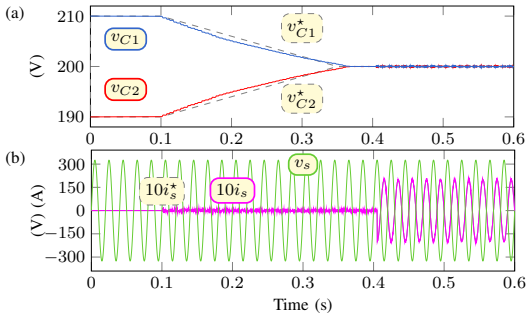

Fig. 9. Capacitor voltage balance (FCS-MPC): (a) capacitor voltages and (b) grid voltage and grid current.

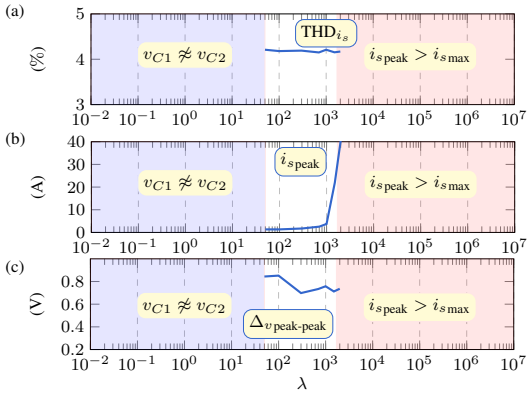

Fig. 10. Weighting factor effect over (FCS-MPC): (a) THD of i_s, (b) peak value of i_s during the balancing transient, and (c) steady-state Δ_v ripple.

independent of λ in a larger range of values. Therefore, the tuning process of the OSS-MPS is easier compared with the FCS-MPC approach.

So far, the inductance and capacitance have been assumed to be fixed and known values. However, in most applications these values typically vary in an unknown manner, resulting in parameters uncertainty. To study this situation, it has been carried out a sensibility analysis of the controller against errors of inductance and capacitance values used in the prediction model compared to the actual ones in the circuit. In general, the results from this study pointed out that the proposed control algorithm can be considered robust against variations on these parameters. In fact, only large deviations on the values used in the prediction model produce a noticeable degradation on the control performance. From a practical point of view, it can be stated that errors on these parameters in the range of -20% to $+20\%$ do not produce a significant variation of the OSS-MPC performance. This result is similar when compared against conventional FCS-MPC under this kind of situation [23], [35].

B. Experimental Results

The proposed control algorithm was implemented in a dSPACE DS1106 with f_s equal to 5 kHz. Although the formulation of the proposed control strategy was done in $k+1$, the implementation considers delay compensation using estimated values for $k+1$ and predictions in $k+2$. A double updated symmetrical PWM method was used for implementing the modulation stage on the dSPACE's DS5203 FPGA board. A bidirectional controlled dc-voltage source (REGATRON TC.4.1200.80.Q14), governed by its internal controller and connected to the dc-link of the H-NPC, is used to generate V_{dc}.

C. DC-Link Voltage Balancing Dynamic Performance

To verify the balancing capability of the proposed controller, the dc-link capacitor voltages are forced to present an initial unbalance. To do so, it is taken into account that the term $e_{\Delta_v,k+1}$ in (7) regulates the actual unbalance value $\Delta_{v,k+1}$ to a predetermined reference $\Delta^{\star}_{v,k+1}$. In general, $\Delta^{\star}_{v,k+1}$ is set to zero to balance the dc-link capacitor voltage values. However, one can set a different value to this reference. As an initial test, a change in the value of the capacitor voltage difference reference $\Delta^{\star}_{v,k+1}$ from 20 V to 0 V at $t = 0.07$ s is introduced as depicted in Fig. 11. At this moment, the actual value of $\Delta^{\star}_{v,k+1}$ start to decay with a ramp slope of 166.6 V/s. Thus, a settling time of 60 ms is expected. For the sake of clarity in the scopes, in this test, the settling time has been set to 60 ms compared to the 250 ms from the simulation results, while $p^{\star}$ and $q^{\star}$ equal to -3.25 kW ($i^{\star}_s = 20$ A and $\phi^{\star} = \pi$) and 0 VAr, respectively. Note that the grid-voltage, v_s, is affected by the grid-current ripple due to the fact that v_s was generated using a controlled ac-voltage source (REGATRON TC.ACS.50) in series with a 10 kVA isolation transformer. The effect of these harmonic components is mitigated by implementing a reconstructed version of $v_{s,k}$ and their estimated values from a PLL as described in detail in [17]. Since the proposed dc-link voltage balancing algorithm is based on V_{dc} as a constant or slowly variant value, both capacitor voltages were filtered using a first order discrete low-pass filter with a cut-off frequency of 25 Hz. The capacitor voltages from Fig. 11(c) reach the balanced condition after three grid voltage cycles as expected, where no undesired spikes in the grid-current are observed. Note that the dc source power supply generates a low frequency dc voltage ripple which depends on its the internal controller performance and not on the H-NPC controller itself. This situation forces the proposed controller to deal with a non-constant V_{dc}. The experimental results show that the proposed OSS-MPC is robust against this disturbance and is able to work properly under such situation.

D. Grid-Current Tracking Dynamic Performance

A step change in the active power reference $p^{\star}$ from -0.81 to -3.25 kW, equivalent to $\hat{i}^{\star}_s$ from -5 to -20 A and $\phi^{\star} = \pi$ was introduced as depicted in Fig. 12. Fig. 12(a) includes a zoom view of the results showing the grid-current tracking performance. Note that the current slope is limited by L and the maximum converter output voltage during the transient operation, which in this case is V_{dc}. The proposed controller is able to quickly provide this voltage. The dc-link voltage balancing dynamic performance remains constant ($\Delta_v \approx 0$) despite the low-frequency transient oscillation due to the internal dc-link voltage controller, as shown in Fig. 12(c). This test resembles the operation of a back-to-back converter

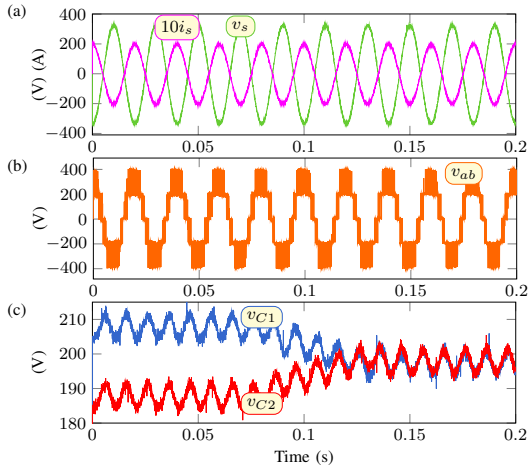

Fig. 11. Capacitor voltage balance: (a) grid voltage and grid current, (b) converter output voltage, and (c) capacitor voltages.

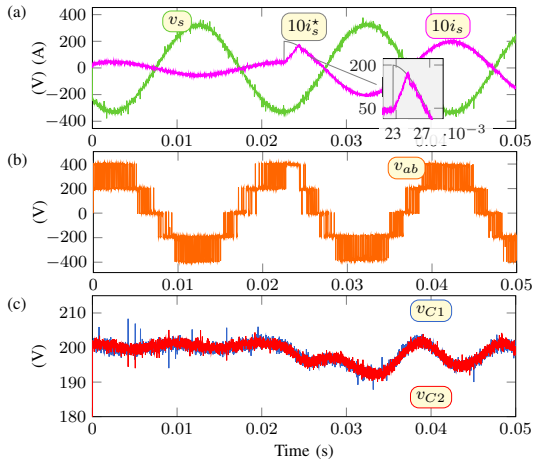

Fig. 12. Current reference step change from 5 to 20 A: (a) grid voltage and current, (b) converter output voltage, and (c) capacitor voltages.

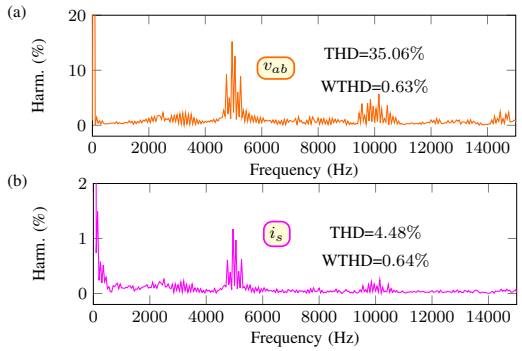

Fig. 13. Steady state spectrum analysis of: (a) v_{ab}, and (b) i_s.

where the dc-link inverter voltage is provided by an ac-dc rectifier stage, which in this case the dc-voltage source is set at 400 V.

E. Steady-State Performance

Finally, Fig. 13 shows the steady-state spectrum of v_{ab} and i_s. Each associated spectrum presents dominant harmonic components around 5 kHz. The low-frequency harmonic content in the grid current is characterized by a magnitude less than 0.5 % of the fundamental component, which is in concordance with the recommendations of the IEEE Std. 519, [12].

VII. Conclusion

In this work, an OSS-MPC for a single-phase grid-connected H-NPC power converter was presented. Besides the control of the grid current, the proposed multi-objective OSS-MPC also considers the dc-link capacitor voltage balancing problem. To do this, the control region of the power converter was carefully analyzed. From this study, suitable SSCs were designed by considering the effect of each converter voltage vector over the dc-link balance error. A simulation study of the weighting factor effect over the closed-loop performance was provided, showing that this only has an impact over the peak current during transients, with no effect over the steady-state performance. This is a major advantage when compared to FCS-MPC. The proposed strategy was experimentally validated in a 3.5 kVA laboratory setup. The control strategy was able to effectively track the desired grid current reference and balance the dc-link capacitor voltages. Despite the benefits of the proposed control strategy, future work can be carried out to develop a theoretical stability analysis for OSS-MPC strategies and to improve its performance. Two main characteristics can be study. On one hand, if one can find first the optimal switching sequence, then the computational burden of the algorithm could be reduced. On the other hand, output constraints could be considered to solve the optimal control problem with constraints and compute the application times expressions off-line. This will allow the converter to work closer to its operational limits. Both are open research issues that will improve the features of the proposed OSS-MPC.

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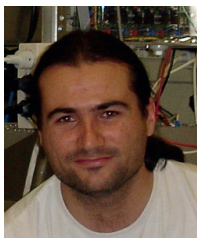

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