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To cite this article: Hiroto Mukai *et al* 2020 *New J. Phys.* **22** 043013

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Deutsche Physikalische Gesellschaft DPG
IOP Institute of Physics

Published in partnership with: Deutsche Physikalische Gesellschaft and the Institute of Physics

OPEN ACCESS

RECEIVED
26 November 2019

REVISED
5 March 2020

ACCEPTED FOR PUBLICATION
6 March 2020

PUBLISHED
21 April 2020

PAPER

Pseudo-2D superconducting quantum computing circuit for the surface code: proposal and preliminary tests

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Keywords: superconducting quantum circuit, quantum information, airbridge, surface code, resonator

Abstract

Among the major hardware platforms for large-scale quantum computing, one of the leading candidates is superconducting quantum circuits. Current proposed architectures for quantum error-correction with the promising surface code require a two-dimensional layout of superconducting qubits with nearest-neighbor interactions. A major hurdle for the scalability in such an architecture using superconducting systems is the so-called wiring problem, where qubits internal to a chipset become difficult to access by the external control/readout lines. In contrast to the existing approaches which address the problem through intricate three-dimensional wiring and packaging technology, leading to a significant engineering challenge, here we address this problem by presenting a modified microarchitecture in which all the wiring can be realized through a newly introduced pseudo two-dimensional resonator network which provides the inter-qubit connections via airbridges. Our proposal is completely compatible with current standard planar circuit technology. We carried out experiments to examine the feasibility of the new airbridge component. The measured quality factor of the airbridged resonator is below the simulated surface-code threshold required for a coupling resonator, and it should not limit simulated gate fidelity. The measured crosstalk between crossed resonators is at most −49 dB in resonance. Further spatial and frequency separation between the resonators should result in relatively limited crosstalk between them, which would not increase as the size of the chipset increases. This architecture and the preliminary tests indicate the possibility that a large-scale, fully error-corrected quantum computer could be constructed by monolithic integration technologies without additional overhead or special packaging know-how.

1. Introduction

Recently, architectural designs for large-scale quantum computers have became increasingly comprehensive. This area of research requires a large amount of quantum engineering to specify how qubits will be manufactured, controlled, characterized, and packaged in a modular manner for fault-tolerant, error-corrected quantum computation [1–5]. The vast majority of architectures base their designs on the surface code because it has one of the highest fault-tolerant thresholds of any error-correction code, easing the physical fidelity requirements on the hardware, and is defined over a 2D, nearest neighbor array of physical qubits.

[4] H M, K S, S J D, and J S T designed the architecture. H M, R W, and Y N designed the samples, R W and Y N fabricated the samples. H M and Y Z carried out the experiments and analyzed the data. K S carried out the numerical calculations. H M, K S, S J D, and J S T wrote the paper with feedback from all authors. J S T designed and supervised the project
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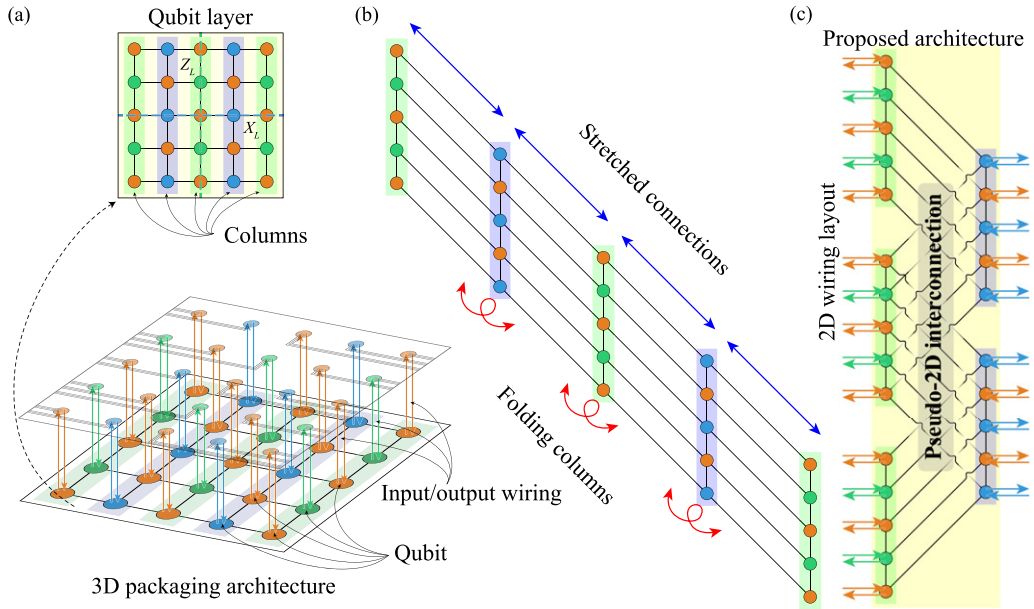

Figure 1. Standard circuit architecture and our proposed architecture for surface codes with 5 × 5 qubit array. (a) Standard system utilizing global multi-layer structures, a separated qubit layer (top figure), and a control/readout layer (clear layer in bottom figure). Qubits are divided into data qubits (orange circles) and X (blue circles) and Z (green circles) syndrome qubits, and all nearest-neighbor qubits are connected by inter-qubit wiring. Vertical arrows indicate input/output wiring. (b) Folding operation of proposed architecture. In the horizontal direction, interconnections of the 2D qubit array are stretched out while maintaining the resonator frequency. At each qubit column, the interconnection is folded. (c) Proposed planar architecture for surface code. After process (b), the proposed architecture has completely planar external wiring (no arrow intersect any wiring, external lines, and inter-qubit connections) with the help of pseudo-2D interconnections.

Superconducting quantum circuits have emerged as a major contender as a scalable hardware model for the surface code [6, 7]. Superconducting qubits are fabricated with inter-qubit wiring for nearest-neighbor interactions, and each qubit requires external physical access for bias lines, control lines, and measurement devices. However, as two-dimensional (2D) arrays are scaled up, planar accessibility for control lines becomes a problem. Such challenges are sometimes referred to as the wiring problem, where physical qubits in the interior are no longer accessible in-plane from the edge [8].

Compared with classical silicon integrated circuits, it is much more difficult to achieve such wiring in superconducting quantum circuits. To individually access every qubit in a 2D qubit array, standard multi-layer wiring technologies for silicon integrated circuits simply cannot be embraced as they generally require the introduction of decoherence enhancing and low-quality interlayer insulators [9, 10]. Therefore, many groups have been forced to utilize non-monolithic bulky three-dimensional (3D) wiring technologies in current superconducting systems (see figure 1(a)), such as flip-chip bonding, pogo pins, and through-silicon vias (TSVs) [11–19].

2. Proposed architecture

2.1. Concept

Our new architecture for the surface code is obtained by transforming a 2D qubit-array to a dual 1D qubit-array (we call it bi-linear array of qubits). Figure 1 shows the mapping before and after this transformation. The square lattice in figure 1(a) is divided into its constituent columns. Next, connections between columns, which take shape as resonators, are stretched (figure 1(b)) and then folded on top of each other successively, as shown in figure 1(c). As the connections are stretched out, the frequencies of the resonators are maintained, and it is a sign of scalability of our architecture. Such invariable frequencies do not survive in another 2D-array transformation [20]. Therefore, the circuits before and after the transformation both occupy approximately the same area, as shown by the yellow areas in figures 1(a) and (c). The resulting equivalent surface code circuit is a bi-linear array of the original 2D structure.

The folding operations liberate the columns locked deeply inside the original 2D lattice and bring them out to the edges of the bi-linear array. Therefore, the external control/readout lines connected to each qubit are accessible from the edges of the chip. This novel arrangement allows all these external connections to be prepared in a completely standard 2D layout.

The advantage gained in the external wiring as a result of the transformation, however, has a small cost in terms of the inter-qubit wiring between columns. These inter-qubit connections between neighboring columns require multilevel crossings. Nonetheless, these 3D structures only need to locally hop over inter-qubit connection lines. Thus, the cross-connections between the columns can be described as pseudo-2D.

In comparison, for the original surface code architecture, the multi-layer wiring grid involves an inter-qubit connection layer and an input/output wiring layer. Therefore, a global multi-layer structure, as shown in figure 1(a), is often adopted, which utilizes non-monolithic bulky 3D wiring technologies as mentioned earlier. Compared with the standard surface code arrangement, the new architecture has the following advantages.

(a) The complete separation of the input/output wiring and inter-qubit wiring will help suppress crosstalk between external lines and qubits as well as that between external lines and inter-qubit connection lines. Therefore, it is possible that the undesired decoherence of qubits owing to the external wiring will also be reduced.

(b) 2D planar layout of the input/output wiring which connects qubits to external electronics can be constructed by utilizing the standard 2D wide-band (microwave) technology. Superconducting resonators for the readout of qubits can also be prepared with the standard 2D co-planar design.

(c) For local 3D (psuedo-2D) wiring, the ends of the inter-qubit connection lines always end up on the same qubit layer, regardless of the number of 3D hops involved in the connection. In such a case, the multi-layer crossing for this new architecture could be realized simply by using local monolithic 3D structures, such as superconducting airbridges.

Moreover, even though the original square lattice architecture can adopt a local 3D structure (airbridges) for the wire crossings between input/output and inter-qubit connections, compared with the new architecture, such an arrangement would produce strong crosstalk between external wiring and inter-qubit connection lines [cf point (1) above].

Consequently, this architecture straightforwardly solves the challenging 3D external wiring problem. As mentioned, a convenient technology to realize cross wiring is an airbridge: a monolithic microstructure developed as low-loss wiring for superconducting qubits that can be fabricated in several ways, including a well-established standard fabrication process [21, 22]. It should be noted that, in standard superconducting architecture designs, a much larger number of airbridges—compared with the number additionally required for this proposed architecture—are already needed to maintain the uniform ground potential for all co-planar waveguide-based architectures.

2.2. Scaling estimation

To scale-up integration, one needs to consider that increasing the number of qubits M in a column will give rise to an increased number of airbriges in the scaled-up structure of this architecture (figure 2(a)). Therefore, one should limit M to the minimum required for the surface-code-based computer in an effective 2D array. This is the arrangement before the transformation shown in figure 2(d). This limitation posed by the number of airbridges results in a subtle change in the design compared with the standard 2D array for a surface-code design.

The typical logical structure of a computer shown in figure 2(b) is a 2D array of qubits used for the surface code computing utilizing braid-based logic [7]. Logical information is introduced by strategically switching on/off parts of the array to create and manipulate defects, which encode the logical qubits within the computer. The larger the 2D array at the physical layer, the more defects can be introduced for a given number of logically encoded qubits in the computer—or the error-correction strength of each logical qubits can be increased. Logic operations are then performed by topological braiding of the defects around each other. In figure 2(b), we illustrate a lattice that encodes two logical qubits via four pairs of defects (shaded regions), where two pairs are utilized for each logical qubit. The defects are encoded using a $d = 3$ surface code, which can correct an arbitrary single qubit error on either of the two encoded defect-based qubits. In order to realize this defect-based structure without significantly compromising the capability to efficiently enact arbitrary error-corrected circuits, scaling up is required in two dimensions.

In our new design the length of columns in the effective 2D array is limited owing to the number of airbridged crossings in an inter-qubit connection, but an arbitrary number of columns is allowed. Therefore, we envisage that a lattice-surgery-encoded logic will be used instead of the braid-based logic (shown in figure 2(c) for the $d = 3$ surface code) [24]. The lattice-surgery-encoded logic also can aid the realization of sufficiently fast classical error-correction decoding [25, 26]. In lattice surgery, isolated square patches of the planar code (*single logical qubit*, which is a surface code analogue that can encode a single piece of logical information) interact along a boundary to enact multi-qubit logic gates. This reduces the

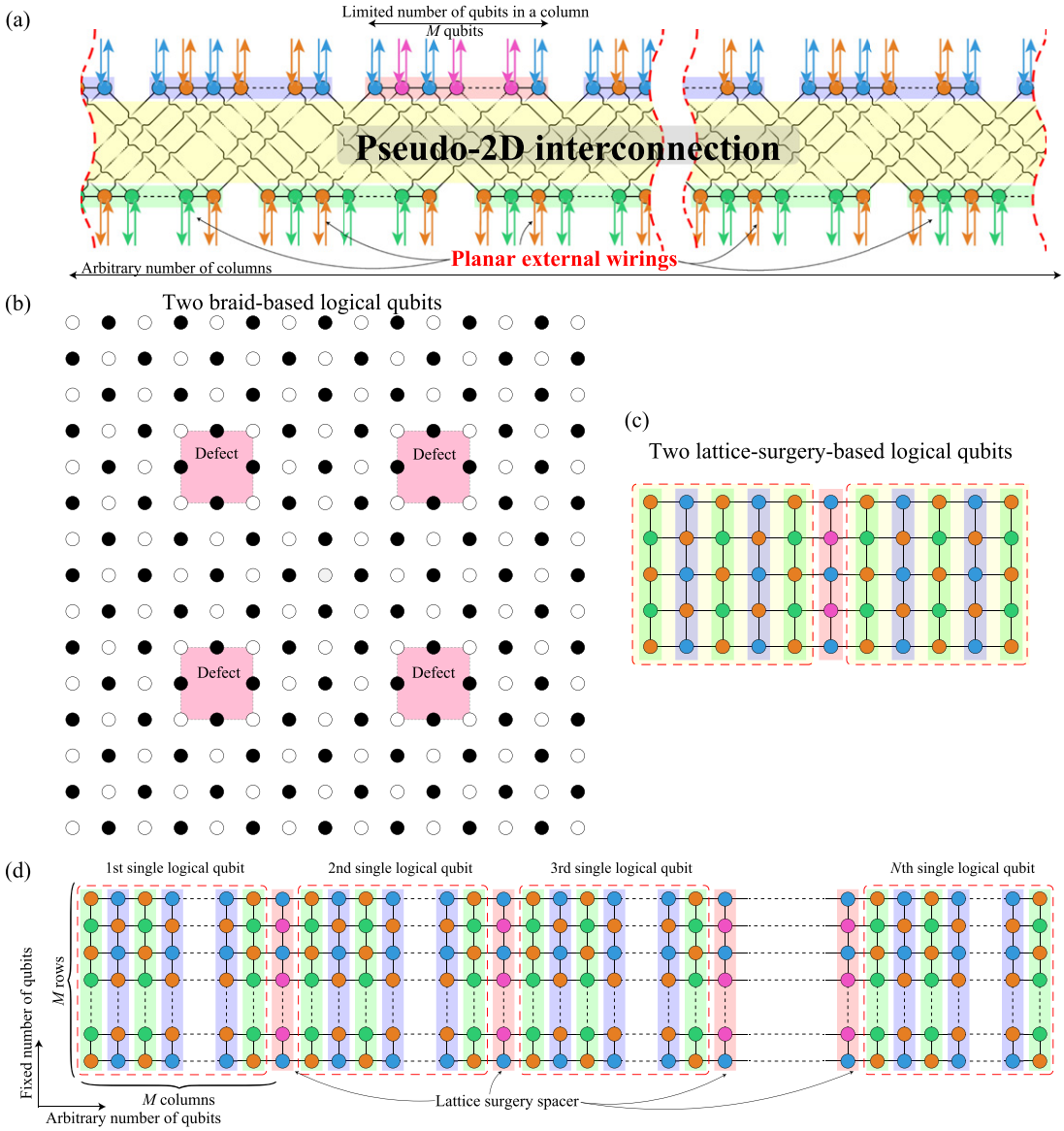

Figure 2. (a) Physical layout of the new architecture. An arbitrarily long but fixed-width surface code can be created using a bi-linear arrangement of superconducting qubits that are cross-coupled with airbridged resonators. The fixed width of the surface code ensures that the airbridged resonators have a finite length and number of airbridged crossings. Each superconducting qubit can be accessed in the plane for the control, initialisation, and readout technology. (b) Standard braid-based arrangement of the surface code sufficient for encoding two logical qubits of information with a distance $d = 3$. (c) Standard arrangement of two lattice-surgery-based square patch as sufficient for encoding two logical qubits of information with a distance $d = 3$. (d) New logical qubit layout consisting of square patches of the surface code, each encoding a single logical qubit of information. Between the square patches there are spacer regions (red columns) to allow lattice-surgery-based logic operations. This layout maintains a small, fixed width of the physical lattice and converts the computer into an LNN logical qubit array. A technique for logical compilation and operation can include a single extra row of physical qubits stretching the length of the computer to enact a new data bus technique for logic operations using planar codes and lattice surgery [23].

overall physical resource cost of each logical qubit, and results of several recent studies suggesting that lattice surgery techniques will always be more resource-efficient when implementing large-scale algorithms [27–29]. For a single logical qubit encoded with the planar code, a square 2D array of physical qubits is needed. For a quantum code with a distance d, $(2d-1) \times (2d-1)$ array of physical qubits is sufficient, the number of which can be reduced further by utilizing rotated planar lattices [24, 28] (see appendix A). This results in a linear nearest-neighbor (LNN) logical layout of encoded qubits (shown in figure 2(d)), requiring less physical resources than defect-based logical qubits. As shown in figure 2(d), there are additional columns of physical qubits (red columns) that are spacers between the encoded qubits, which are required to perform the lattice surgery operations.

It should be noted that the current methods for circuit compilation using lattice surgery still assume a 2D nearest-neighbor arrangement of logically encoded qubits [27–29]. This is because lattice surgery has two basic classes of operations (merges and splits) over two types of boundary for each planar code qubit

(rough and smooth). As merge and split operations can only occur at a single boundary between logical qubit regions, we need to be able to convert between smooth and rough boundaries (as described in detail in reference [24]), and hence compilation into this LNN logical structure using a layout of pseudo-2D physical qubits will require some slight modifications over current techniques [27, 28]. However, a recent result of introducing additional rows of physical qubits to act as a data bus for logic operations can be used and is completely compatible with an LNN arrangement of qubits at the logical level [23].

Generally, to realize a square logical encoded qubit with given distance d of the surface code, a physical array contains $2d-1$ columns with $2d-1$ qubits for each column. Consequently, for a quantum computer containing N logical qubits on the planar code, an array of $M \times [NM + (N-1)]$ should be utilized. Here, $M = 2d-1$ is the number of qubits in a column, NM is the number of columns in the array for N logical qubits, and the extra factor of $(N-1)$ is the spacing region between adjacent logical qubits—needed for the lattice surgery (or a bus system [30]). This translates into a bi-linear array of $2 \times \frac{1}{2}(2d-1)(2dN-1)$ (shown in figure 2(a)). The number of crossing points by interconnections is at most half the number of qubits in a column, at most $\lceil[(2d-1)-1]/2\rceil = d-1$, representing the number of airbridges per resonator. The factor of $1/2$ originates from the fact that alternate resonators (interconnections) are shared by two qubits. Hence, although the number of columns NM linearly increases with the number of logical qubits, the number of airbridges contained in a resonator will only be half the number of qubits in a column (which is fixed for a given code distance d).

In practice, the width of this array is related to the number of logical qubits, whereas its length is given by the distance of the planar code used to encode each logical qubit. For a large error-correcting code, each logical qubit requires $d = 15$–20 to be capable of correcting up to 7–10 errors (sufficient to heavily suppress the logical error rate). For a heavily error-corrected logical qubit with $d = 15$–21, the total number of qubits in a column will be $M = 29$–41 with a maximum number of airbridges for a given resonator of 14–20. By utilizing planar code encoding and lattice surgery [24] for fault-tolerant logic, we can define our computer as a long, rectangular structure consisting of an LNN array of *logical* qubits (requiring compilation of the high-level quantum algorithm with LNN constraints [23, 27, 30]).

3. Preliminary tests

As a feasibility study of this new circuit scheme, we carried out preliminary evaluations of its most important new component, namely, the pseudo-2D interconnection consisting of crossed resonators with airbridges. We studied the dependence of the gate fidelity on the quality factor of resonators, where the centerline contains airbridges. We also studied the crosstalk between crossed co-planar resonators in the pseudo-2D interconnection network.

To examine whether airbridges can be used while still satisfying the error requirements for the surface code, we carried out an experimental test on chips containing the coupling airbridged resonator without qubits and a numerical simulation on a system containing a lossy resonator and two qubits without decoherence. Conventional research on superconducting quantum circuits employs a lossless resonator to eliminate its contribution. However, there has been little research related to the dependence of the gate fidelity on the resonator quality factor. Our numerical simulation reveals the lower limit of the internal quality factor, and the experimental test illustrates the possibility that this proposed architecture will be viable using current technology without special 3D techniques.

3.1. Quality factor of airbriged resonator

We prepared chips using a standard fabrication method for airbridges [21], with each chip containing both an airbriged resonator and a reference resonator made out of a 50 nm-thick Nb film. The film is sputtered on cleaned surface of non-doped Si substrate and etched by reactive ion etching (RIE). The airbridge design of each chip, including the interval between airbridge positions, is identical, and the only difference in fabrication is related to the number of airbridges (15 or 20). Each wafer was treated under the same conditions but wafers were not fabricated at the same time.

Figure 3(a) shows the measured internal quality factor, Q_i, of resonators containing 15 (black symbols) or 20 (red symbols) airbridges along the center conducting line (figure 3(b)), with the reference resonators also illustrated in figure B1 (measurement setup are described in B). The quality factor of the resonators with airbridges along the centerline exceeds $> 2.3 \times 10^4$ at the power of a single photon level. In comparison with the reference co-planar resonators, which do not have airbridges, the quality factor of the resonators with airbridges is about one order of magnitude lower. However, the quality factor of the resonator with 20 airbridges is higher than that of the resonator with 15 airbridges. These two resonators were fabricated in different wafers, so the result probably reflect imperfect reproducibility and parameter

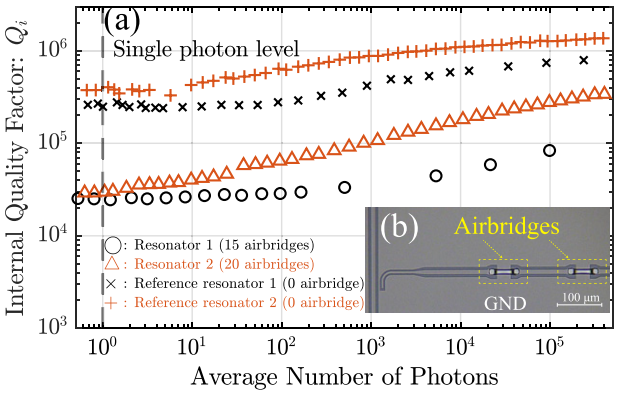

Figure 3. Measured internal quality factor versus average number of photons in resonators (a). Four datasets of measured coplanar resonator are shown in figure; resonator with 15 airbridges along the centerline (○), resonator with 20 airbridges along the centerline (△), reference resonator with no airbridge for 15-airbriged resonator (×), and reference resonator with no airbridge for 20-airbriged resonator (+). We fabricated two chips; resonators ○ and × were fabricated on one chip, △ and + were fabricated on the other chip. The dashed line corresponds to averaged single photon level. Q_i are fitted by standard methods [31]. In detail, a continuous ground plane is paved under the airbridge, which is forming a microstrip structure locally (b). Coupling quality factor Q_c and frequency of each resonator $\omega_r/2\pi$; $(Q_c, \omega_r/2\pi) = [\circ : (3.141 \times 10^5, 10.132\,56\,\text{GHz}), \triangle : (5.273 \times 10^5, 7.804\,65\,\text{GHz}), \times : (3.959 \times 10^5, 9.431\,47\,\text{GHz}), + : (5.162 \times 10^5, 7.234\,19\,\text{GHz})]$.

scattering in our fabrication process. Compare the airbridged resonators with the reference resonators fabricated on the same wafer, it shows a similar deviation trend in the quality factors.

3.2. Simulation of gate fidelity with lossy resonator

To appraise the effect of the extra loss resulting from the insertion of airbridges, we simulated the average gate infidelity of a CZ gate in our system, where two transmon-type qubits are coupled through a damped (lossy) resonator [32]. In the simulated system, each qubit has three energy levels and anharmonicity, η_i, the resonator has five energy levels with photon leakage rate $\kappa_i = \omega_r/Q_\text{i}$, and the coupling constant between each qubit and the resonator is g_i. In the system, we ignored the qubit–qubit direct coupling.

We adjusted the state of the system to the condition for the CZ gate, which is that the energy difference from the ground level to the first excited level on one qubit is the same as the energy difference from the first excited level to the second excited level on the other qubit. Then, we calculated the time evolution of this system and finally obtained the average gate fidelity F (for more detail see the C). To simplify the simulation, we ignore the pulse shape of the CZ gate operation. The leakage from the whole system to the external environment was also assumed to be entirely due to the resonator and not due to qubit decoherence, in order to leave no doubt that the error is caused by resonator loss. These assumptions were made to evaluate the dependence of the fidelity on the quality factor of the resonators.

Figure 4 shows the dependence of the infidelity on the quality factor of the resonator, Q_i, obtained by simulation. The result indicates that the value of Q_i required for the infidelity threshold of the surface code $(1 - F < 0.75\%)$ is 2×10^3, and the infidelity is saturated at $Q_\text{i} > 10^4$.

The experimental internal quality factor of a resonator with airbridges at the centerline is one order of magnitude greater than what is required according to our simulation. In this experiment, ordinally airbridge technology were used. Therefore, this result strongly indicates that our proposed system, with realistic parameters, is feasible.

3.3. Crosstalk test

The crosstalk between two crossed resonator lines is also evaluated using another chip as shown in figure 5(a). A feed line crosses a resonator vertically using an airbridge (figure 5(b)).

The frequency of the resonator ω_{r1} was measured by port 3. We subsequently measured the crosstalk between the feed line and the resonator around the resonant frequency ω_{r1}. The crosstalk is due to the airbridge structure that connects the center signal line of the resonator across the feed line. A continuous microwave signal reference was applied through the feed line from input port 1 to output port 2 in figure 5(a). Then, the signal was absorbed at the resonant frequency ω_{r1} of the airbridge resonator, which resulted in a small dip. In figure 5(c), the normalized measured data $|S_{21}|$ with the dip is shown (blue circles), and the crosstalk defined by $20\log_{10}(1 - |S_{21}|)$ dB is also shown (red crosses). The result shows that the crosstalk due to the crossing airbridge was at most -49 dB when the frequencies are resonant.

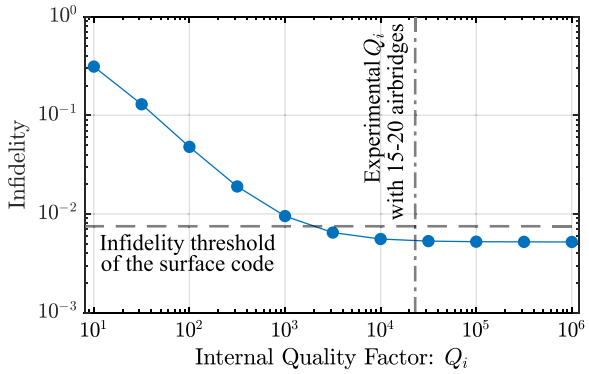

Figure 4. Simulated average gate infidelity of the CZ gate, via the resonator, versus the quality factor of the resonator. Frequency of the ith qubit between the ground and first excited levels: $\omega_i^{01}/2\pi = 5.6$ GHz and 5.8 GHz; anharmonicity of the ith qubit: $\eta_i/2\pi = -200$ MHz; resonator frequency: $\omega_r/2\pi = 6$ GHz; coupling constant between the ith qubit and resonator: $g_i/2\pi = 81.2$ MHz; effective coupling strength between qubits: $g_{\rm eff}/2\pi = 3$ MHz; gate time; 117.9 ns. The dashed line shows the threshold of the surface code. The dash-dotted line indicates the experimental Q_i with 15–20 airbridges.

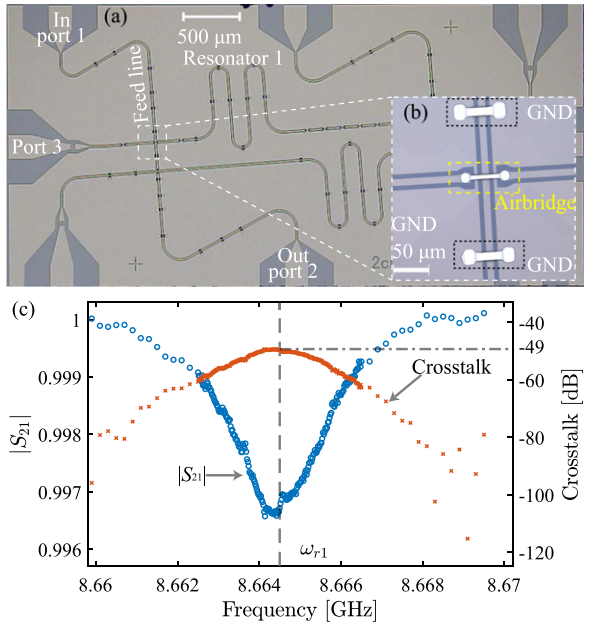

Figure 5. (a) Optical image of the chip for crosstalk measurements. The two parallel horizontal lines are half-wavelength resonators. The two parallel vertical lines are feed lines used to measure closstalk to the resonators at cross points via airbridges. (b) Detailed image of the cross point utilizing an airbridge. The center airbridge connects the left to right signal lines of the resonator over the vertical feed line. The top and bottom airbridges connect ground (GND) planes, which are separated. The width of the coplanar waveguide resonator is 10 μm and the gap to the ground is 6 μm. The width of the airbsidges is 9 μm, the length is 42.6 μm, and the height is 3 μm. (c) Datasets of $|S_{21}|$ (shown on left axis by blue circles) and crosstalk (shown on right axis by red crosses). The center vertical dashed line indicates the resonant frequency of the resonator 1, $\omega_{r1} = 8.6645$ GHz, evaluated at port 3. The horizontal dash-dotted line indicates the maximum value of the crosstalk.

Therefore, to realize the pseudo-2D interconnection network with airbridges, we should detune all frequencies of crossed resonators sufficiently. This will suppress the effective crosstalk to an small value, even smaller than the characteristic background damping in a typical microwave measurement system.

4. Conclusion

To conclude, we proposed a novel scalable architecture of superconducting quantum circuits for the surface codes, where standard planar 2D wiring can be adopted for the external wiring, with the help of an airbridge-incorporated inter-qubit pseudo-2D resonator network. We also carried out an experimental feasibility study of the pseudo-2D resonator network and showed that there are no fundamental difficulties in realizing it. Our results indicate that it may be possible to build a fault-tolerant, large-scale quantum

computer using simple monolithic integration technologies. We are planning to construct a small-scale circuit to further examine and explore this possibility.

Competing interests

The authors declare that there are no competing interests.

Acknowledgments

We thank F Nori, O V Astafiev, A Tomonaga, and D Zhang for discussions. We also thank M Hidaka for providing wafers with a Nb film. This work was supported by CREST, JST (Grant No. JPMJCR1676), the New Energy and Industrial Technology Development Organization (NEDO), and the ImPACT Program of Council for Science, Technology and Innovation (Cabinet Office, Government of Japan).

Appendix A. Using the rotated lattice for logical qubit encoding

In the main text, we described the architectural layout using encoded qubits formed from a square lattice of $(2d-1)^2$ physical qubits. This number can be reduced by utilizing the rotated lattice encoding introduced in reference [24]. A rotated lattice will reduce the number of physical qubits in a logical block from $(2d-1)^2$ to $2d^2-1$, which can result in significant resource savings for large values of d.

Regarding the hardware architecture itself, there are no changes required for the underlying hardware. In figure A1 we illustrate how two encoded qubits in the rotated lattice are translated to the bi-linear design. Unlike the case when the encoded qubits are square patches, the airbridge connections become non-uniform. However, the maximum number of airbridges within a single resonator does not change between the cases of square encoding and rotated encoding, the square lattice encoding represents the upper bound for the rotated lattice. Consequently, the design in the main text is completely compatible with that using rotated lattice encoding.

Appendix B. Extra information on the experiment

We utilized a vector network analyzer (VNA) to measure the internal quality factor and crosstalk. To evaluate the internal quality factor of resonators, we prepare the chip with 15 airbridges shown in figure B1. The spectrum of the resonators was measured using the input and output ports of the feed line coupled to each resonator.

Appendix C. Information on the simulation

We modeled a part of our system as two qubits coupled via a damped resonator without leakage from qubits, so the Hamiltonian is

$$\mathcal{H}/\hbar = \omega_r a^\dagger a + \sum_{i=1,2}\left[\omega_i^{01} b_i^\dagger b_i + \frac{\eta_i}{2} b_i^\dagger b_i (b_i^\dagger b_i - 1) + g_i (a^\dagger b_i + a b_i^\dagger)\right], \tag{C.1}$$

and this indirect interaction of qubits (last term) is used for the CZ gate. The quantum map $\mathcal{E}$ can be derived solving by the Lindblad master equation, and then we calculate the average gate (in)fidelity in the computational subspace $|\psi_s\rangle$ between the map $\mathcal{E}$ and an ideal CZ gate map $\mathcal{E}_{CZ}$, which is defined as [33, 34]

$$\overline{F}(\mathcal{E}, \mathcal{E}_{CZ}) = \int d\psi_s \langle\psi_s|\mathcal{E}_{CZ}^{-1} \circ \mathcal{E}(\psi_s)|\psi_s\rangle, \tag{C.2}$$

averaged over the Haar measure $d\psi_s$. This simulation is performed using Quantum Toolbox in Python (QuTiP) [35].

Appendix D. Qubit chip fabrication feasibility

The new architecture might suggest that, as the number of the qubit scales up, the chip would become longer and longer. One may wonder if it is actually possible to fabricate such a chip. We consider the issue for a realistic logical qubit chips, in terms of its design and its fabrication feasibility. To circumvent the

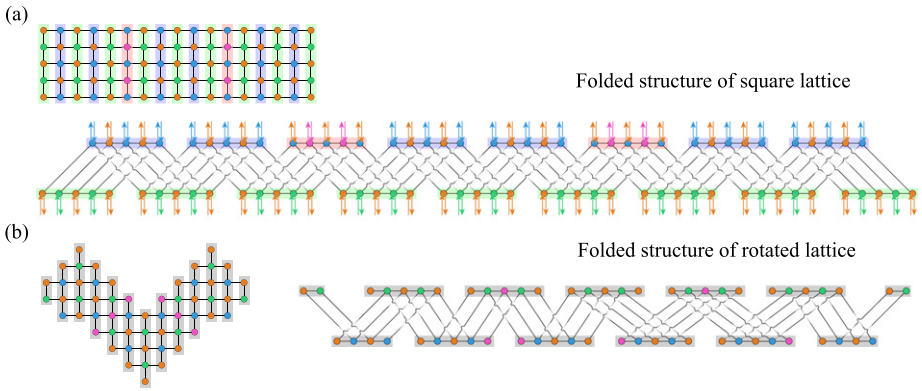

Figure A1. (a) LNN arrangement of three logical qubits of the square patch for the surface code with the distance 3. (b) LNN arrangement of three logical qubits of the rotated patch for the surface code with the distance 3.

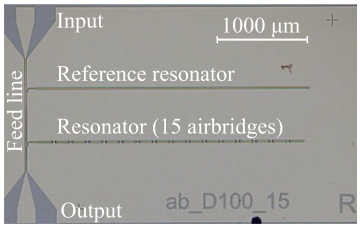

Figure B1. Measured chip for the resonator with 15 airbridges (top) and the reference resonator (bottom), which are capacitively coupled to the feed line. The resonators are made of Nb film on a non-doped Si wafer.

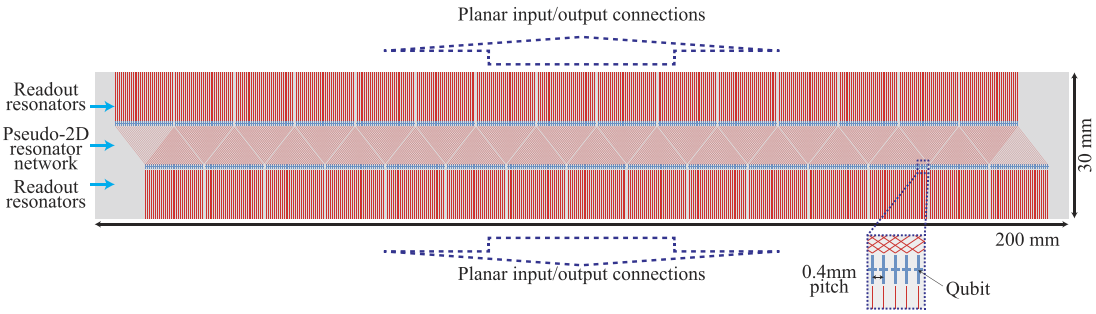

Figure D1. A design of single-logical-qubit chip consists of 30 × 30 physical qubits, arranged according to the proposed pseudo-2D coupling network architecture. Qubits are depicted as blue crosses (inset) and resonators are as red lines. All the external input and output connections can be achieved by the conventional planer wiring technology. The resulted chip size is approximately 30 mm × 200 mm rectangular.

increasing chip length as it scales, we consider a case where inter-qubit coupling within qubit array in each column are achieved by a direct coupling manner, instead of coupled via resonators as in figure 1(c). Such coupling scheme was shown to be very effective and able to achieve a highly accurate gate operations [36].

We considered an implementation of a 30 × 30 physical qubit array, for it is a sound logical qubit for a surface-code based quantum computer. Using realistic physical parameters, such logical qubit can be prepared on a 30 mm × 200 mm chip, including readout resonators, as shown in figure D1, where qubits are arranged within the inline 1D array, with a pitch of 0.4 mm. The resulted chip size, especially its length, would easily fit within the size of the largest chip of the day, the wafer scale processor chip having an area of approximately 46 000 mm^2 [37]. The input/output wirings of the chips can all be arranged in the ordinary 2D manner. Moreover, the above estimation was based on a preliminary design concept without any sort of area optimization, and the chip size could be further reduced in the future. Therefore, fabrication of such logical qubit chip should be possible with the current technology, in principal.

Then, many of these logical qubit chips could be assembled and packaged further as a quantum computer. The inter logical qubit chip connections can be achieved using 'quantum bus' architecture [23] for example. In this case, connection between two logical qubit chips could be established only with limited numbers of classical connection lines. It seems there is no immediately foreseeable fundamental physical limit preventing the chip fabrication and its packaging, at least now.

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