A Novel Boost Cascaded Multilevel Inverter

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Abstract—This paper presents a novel cascaded multilevel inverter as an alternative to the cascaded H-bridge (CHB). By adopting two H-bridges integrated with two inductors and two power switches, the proposed topology is able to generate a five-level voltage with merely a single dc source. Voltage-boosting capability is guaranteed despite its single-stage operation. A corresponding modulation technique is also established to charge the boost inductors with a constant duty-cycle, while simultaneously generating a 5-level ac voltage. Therefore, the proposed topology outperforms the CHB in reducing the isolated dc source count, enhancing the voltage gain, and lowering the dc source voltage magnitude. In addition, the modularity is preserved, where the proposed topology can be extended by cascading multiple modules. The operation and feasibility of the proposed cascaded multilevel inverter is analyzed and validated through simulation and experimental results.

Index Terms—Boost inverter, cascaded multilevel inverter, five level, voltage-boosting.

I. INTRODUCTION

THE concept of the cascaded H-bridge (CHB) was firstly introduced by McMurry in 1971 [1]. The incredible development of power semiconductor devices over the last few decades has made the practical implementation of the CHB possible while maintaining high performance. Today, the CHB has been deployed in various industrial applications and renewable energy systems [2]–[4]. Despite its maturity, significant research attempts should be made for further improvement from various aspects, in particular, the power conversion efficiency and compactness by reducing the number of components but increasing the voltage levels. Therefore, there are remarkable studies devoted to designing promising hybrid topologies based on the CHB concept [5].

The switch count can be effectively reduced by using a two-stage configuration, i.e., a multi-input single-output dc-dc converter and an H-bridge. In this regard, the front-end dc-dc converter is dedicated to the generation of a multilevel dc voltage across the dc-link of the H-bridge, whereas the rear-end H-bridge which operates at the line frequency is dedicated to the polarity control of the ac output. This type of topology is referred to as a multilevel dc-link inverter [6], where cascaded half-bridges are employed to control the dc sources. Several variants of the multilevel dc-link inverter have been reported recently in the literature. For example, a cascaded switched-diode inverter proposed in [7] replaces one switch of each half-bridge with a diode to form its front-end dc-dc converter. Alternatively, the front-end dc-dc converter in [8] is constituted by an improved 4-level submodule. Subsequently, the idea of replacing the rear-end H-bridge with a T-type inverter for the polarity generation was studied in [9].

A trend indicates the establishment of new cascaded multilevel inverters with the exploitation of T-type inverters. Without compromising the compactness, two T-type inverters connected in a back-to-back structure is capable of generating a multilevel ac voltage within a single-stage configuration [10], [11]. This concept is further generalized in [12] and an optimized cascaded multilevel inverter with the least switch count is presented. A similar concept is also recently applied to the multilevel dc-link inverter [13]. Although integrating multiple dc sources for a hybrid inverter module achieves switch count reduction, their main challenge is the power balancing between dc sources. Each module requires a minimum of four isolated dc sources that supply the load with uneven durations. This brings many practical limitations.

Similar to the CHB, voltage gains for all the aforementioned topologies are limited to unity. Therefore, they require the same number of dc sources as that in the CHB. This drawback has inspired recent efforts on the switched-capacitor (SC) type cascaded multilevel inverter [14]–[22] which features voltage-boosting capability. Likewise, the concept of the multilevel dc-link inverter is adopted by replacing the cascaded half-bridges with an SC circuit, which is adopted as the front-end dc-dc converter to generate a multilevel unipolar voltage higher than the dc source voltage across the rear-end H-bridge. However, due to the high voltage stress across the H-bridge, there are recent attempts to establish a single-stage SC topology that can generate bipolar voltage levels without the rear-end H-bridge [23].

Despite the various SC topologies in the literature, their

practical implementations remain ambiguous due to several crucial issues. During steady-state operation, the SCs are charged by connecting them in parallel with the dc source, where large current spikes are induced. This may adversely reduce the reliability of capacitors and switches. Besides, an additional capacitor charging circuit is essential to pre-charge the SCs to prevent from short circuiting during the startup. Large SCs are also required to ensure that sufficient energy is stored for supplying the load.

Aimed to overcome the drawbacks of the existing cascaded multilevel inverters, this paper proposes a novel topology which is able to accomplish their respective merits concurrently. The proposed topology is termed as a boost 5-level inverter (B5LI). The most attractive feature of the proposed B5LI is that it enables the generation of five voltage levels with a single dc source, while preserving the voltage-boosting capability within single-stage operation. Moreover, it overcomes the current spikes issue in prior-art SC topologies by soft-charging the dc-link capacitors through boost inductors. The rest of the paper is organized as follows: Section II presents the steady-state analysis of the proposed B5LI and its pulse width modulation (PWM) technique. Section III benchmarks the proposed B5LI with the existing cascaded multilevel inverters. Simulation and experimental results are provided in Sections IV and V, respectively and finally, Section VI draws the conclusion.

II. PROPOSED BOOST 5-LEVEL INVERTER (B5LI)

Fig. 1 shows the circuit diagram of the proposed boost 5-level inverter (B5LI). It consists of two identical sub-converters which share a single dc source, as observed in Fig. 1. A boost inductor in each sub-converter is used to boost the voltage across the respective dc-link capacitors. The single-stage dc-ac power conversion with 5-level generation is achieved using ten power switches controlled by a newly established PWM technique. The steady-state analysis of the proposed B5LI topology and its PWM technique are presented in the following sections.
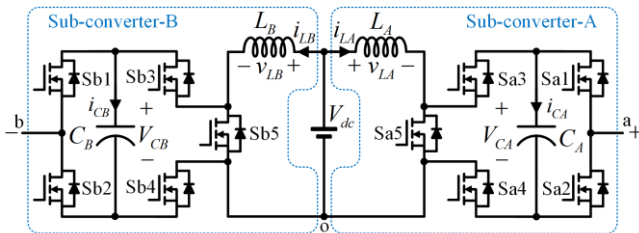

Fig. 1. Circuit diagram of the proposed boost 5-level inverter (B5LI).

A. Steady-state analysis and PWM technique

Considering the neutral of the dc source "o" as the reference point, the circuit analysis is conducted. The circuit and its operation are symmetric about the source V_{dc}. As the same analysis can be applied for each sub-converter, a generalized symbol "x" is used to represent "a" and "b". Fig. 2 shows the equivalent circuit for each switching state with their operations being summarized in Table I. Table II shows the voltage and current stress of each power switch.
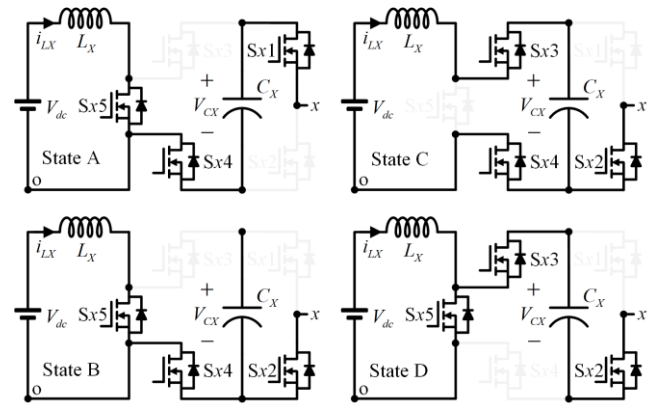

Fig. 2. Steady-state analysis for each sub-converter of the proposed B5LI.

There are two redundant states at the zero-voltage level that can be feasibly used to charge or discharge the boost inductor. As the discharging of the boost inductor is not possible during positive and negative voltage levels, its maximum discharging duration is confined within the period of the zero-voltage level. Accordingly, a PWM technique depicted in Fig. 3 is then established to achieve a single-stage power conversion, where a constant duty-cycle D is used to charge the boost inductor, and a variable duty-cycle d is used to generate the 5-level ac voltage.

TABLE I.
Switching States of the Proposed B5LI.

States	$Sx1$	$Sx2$	$Sx3$	$Sx4$	$Sx5$	v_{xo}	L_X
A	1	0	0	1	1	V_{CX}	Charging
B	0	1	0	1	1	0	Charging
C	0	1	1	1	0	0	Discharging
D	0	1	1	0	1	$-V_{CX}$	Charging

$x = \{a, b\}, X = \{A, B\}$

TABLE II.
Voltage and Current Stress of Power Switches

Switch	Current Stress	Voltage Stress
$Sx1$	$\hat{I}_{o,1}$	V_{CX}
$Sx2$	$\hat{I}_{o,1}$	V_{CX}
$Sx3$	$0.5I_{dc}$ or $\hat{I}_{o,1}$	V_{CX}
$Sx4$	$0.5I_{dc} + \hat{I}_{o,1}$	V_{CX}
$Sx5$	$0.5I_{dc} + \hat{I}_{o,1}$	V_{CX}

$x = \{a, b\}, X = \{A, B\}$, $\hat{I}_{o,1}$ is the peak of ac load current, I_{dc} is the dc source current.

Referring to the key modulation waveforms shown in Fig. 3, two references and two triangular carriers are used to control the proposed B5LI. The triangular carriers v_{tri-a} and v_{tri-b} are used for sub-converter-A and sub-converter-B, respectively. Comparing a constant reference V_{dc-ref} with the triangular carrier generates a constant duty-cycle for boost inductor charging,

$$D = \frac{V_{dc-ref}}{\hat{V}_{tri}} \tag{1}$$

where D denotes the constant duty-cycle for boost inductor charging and $\hat{V}_{tri}$ denotes the peak of triangular carriers. Considering the volt-second balance of the boost inductor $L =$

$L_A = L_B$, the average voltage across the dc-link capacitor $C = C_A = C_B$ can be obtained as

$$V_{CA} = V_{CB} = V_C = \frac{1}{1-D}V_{dc}. \tag{2}$$

The sinusoidal duty-cycle generated by the sinusoidal reference for controlling the ac voltage can be written as

$$d = M\left|\sin(\omega t)\right| \tag{3}$$

where $M = \hat{V}_{\sin e} / \hat{V}_{tri}$ is the modulation index. The ac voltage at the fundamental frequency controlled by the sinusoidal duty-cycle d is

$$v_{o,1} = MV_{\max}\sin\left(\omega t\right) \tag{4}$$

in which $v_{o,1}$ is the fundamental component of ac voltage and $V_{\max}$ is the maximum voltage level ($2V_C$):

$$V_{\max} = 2V_C = \frac{2V_{dc}}{1-D}. \tag{5}$$

The peak of the fundamental ac voltage can be obtained by substituting (5) into (4) as

$$\hat{V}_{o,1} = MV_{\max} = \frac{2MV_{dc}}{1-D}. \tag{6}$$

The gain of the proposed B5LI considering the ratio between the peak of the fundamental ac voltage to the dc source voltage is

$$G = \frac{\hat{V}_{o,1}}{V_{dc}} = \frac{2M}{1-D}. \tag{7}$$

As the minimum $V_{dc\text{-ref}}$ is constrained to $\hat{V}_{\sin e}$, the minimum D is M, i.e. $D_{\min} = M$ with a critical gain of $2M/(1-M)$.
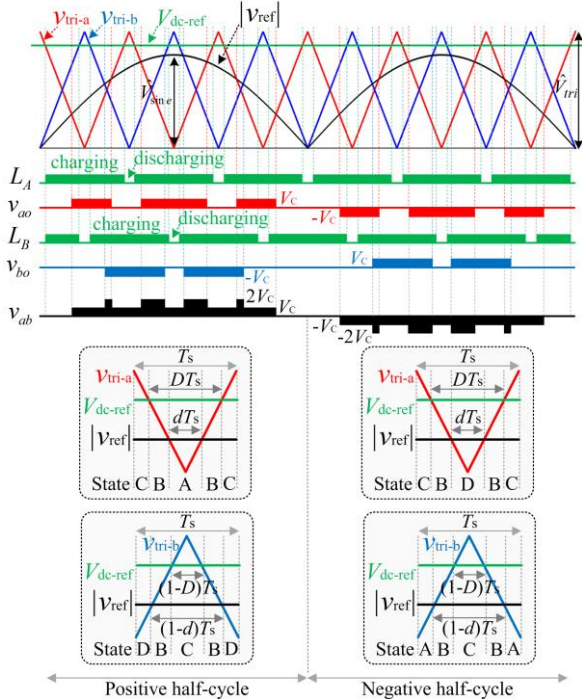
Fig. 3. Pulse width modulation (PWM) technique of the proposed B5LI.

B. Capacitor voltage ripple

The voltage ripple of dc-link capacitors C_A and C_B ($C = C_A = C_B$ is considered) consists of low frequency components at double-line frequency induced by single-phase load currents, and high frequency components induced by PWM switching:

$$\Delta V_C = \Delta V_{C,2f_o} + \Delta V_{C,f_s} \tag{8}$$

where ΔV_C is the total voltage ripple of each dc-link capacitor, $\Delta V_{C,2f_o}$ indicates the low frequency voltage ripple at the double-line frequency $2f_o$, and $\Delta V_{C,f_s}$ denotes the high frequency voltage ripple at the switching frequency f_s. Considering the charge balance of capacitor over each switching cycle, the high frequency ripple is

$$\Delta V_{C,f_s} = \frac{D(1-D)I_{dc}}{2Cf_s} \tag{9}$$

where I_{dc} is the average dc source current. Notice that the average input current for each sub-converter (average current of each boost inductor) is half of the total dc source current owing to their symmetrical circuit structure and operation.

To derive the low frequency ripple of the dc-link capacitor, the load current supplied by the capacitor $i_{c,o}$ shown in Fig. 4 is investigated. Averaging over each switching period T is considered so as to obtain the current without high frequency switching ripples:

$$\left\langle i_{c,o} \right\rangle = \frac{1}{T}\int_t^{t+T} i_{c,o}\,dt = \begin{cases} di_o, & 0 < \omega t < \pi \\ -di_o, & \pi < \omega t < 2\pi \end{cases}. \tag{10}$$

Substituting (3) and the load current $i_o = \hat{I}_{o,1}\sin\left(\omega t - \varphi\right)$ into (10) gives

$$\left\langle i_{c,o} \right\rangle = M\hat{I}_{o,1}\sin(\omega t)\sin(\omega t - \varphi). \tag{11}$$

By performing the trigonometric simplification in (11), the peak of the ac current at the double-line frequency flowing through the capacitor is expressed as

$$\hat{I}_{c,2f_o} = \frac{M\hat{I}_{o,1}}{2}. \tag{12}$$

The low frequency voltage ripple of the dc-link capacitor is the peak-to-peak voltage at the double-line frequency:

$$\Delta V_{C,2f_o} = 2\hat{I}_{c,2f_o}X_{c,2f_o} = \frac{M\hat{I}_{o,1}}{4\pi f_o C}. \tag{13}$$

The total voltage ripple of the dc-link capacitor can be obtained by substituting (9) and (13) into (8) as

$$\Delta V_C = \frac{M\hat{I}_{o,1}}{4\pi f_o C} + \frac{D(1-D)I_{dc}}{2Cf_s}. \tag{14}$$
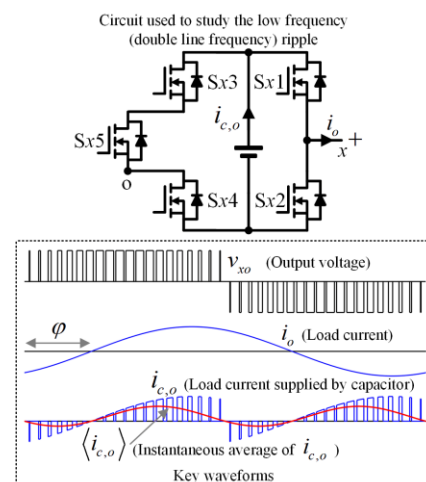
Fig. 4. Analysis for the low frequency (double-line frequency) ripple.

C. Inductor current ripple

Similar to the capacitor voltage ripple, the current ripple of boost inductors L_A and L_B ($L = L_A = L_B$ is considered) also consists of low frequency components at the double-line frequency and high frequency ripples at the switching frequency:

$$\Delta I_L = \Delta I_{L,2f_o} + \Delta I_{L,f_s} \qquad (15)$$

where ΔI_L is the total current ripple of each boost inductor, $\Delta I_{L,2f_o}$ denotes the low frequency current ripple at the double-line frequency $2f_o$, and $\Delta I_{L,f_s}$ represents the high frequency current ripple at the switching frequency f_s. Considering the volt-second balance of inductor during steady-state, the high frequency current ripple is expressed as

$$\Delta I_{L,f_s} = \frac{DV_{dc}}{Lf_s}. \qquad (16)$$

The peak ac voltage across the boost inductor at the double-line frequency is

$$\hat{V}_{L,2f_o} = \frac{M\hat{I}_{o,1}(1-D)}{8\pi f_o C}. \qquad (17)$$

The low frequency inductor current ripple is the peak-to-peak magnitude of the ac current at the double-line frequency:

$$\Delta I_{L,2f_o} = \frac{2\hat{V}_{L,2f_o}}{X_L} = \frac{M\hat{I}_{o,1}(1-D)}{16\pi^2 f_o^2 LC}. \qquad (18)$$

Substituting (16) and (18) into (15), the total current ripple of boost inductors can be represented as

$$\Delta I_L = \frac{M\hat{I}_{o,1}(1-D)}{16\pi^2 f_o^2 LC} + \frac{DV_{dc}}{Lf_s}. \qquad (19)$$

D. Cascaded extension

The proposed topology can be extended by cascading n modules controlled by the same reference signals v_{ref} and $V_{dc\text{-}ref}$. The phase shift of triangular carriers ($\theta_{tri\text{-}a,m}$ and $\theta_{tri\text{-}b,m}$ for sub-converter-A and sub-converter-B, respectively) for the mth module is

$$\theta_{tri-a,m} = \frac{360^o}{2n}(m-1), \ m = \{1,.....,n\} \qquad (20)$$

$$\theta_{tri-b,m} = \theta_{tri-a,m} + 180^o, \ m = \{1,.....,n\} \qquad (21)$$

The maximum number of voltage levels N_{level} for n cascaded modules is expressed as

$$N_{level} = 4n+1. \qquad (22)$$

III. COMPARISON WITH OTHER CASCADED MULTILEVEL INVERTERS

Table III compares the performance of the proposed B5LI against other cascaded multilevel inverter topologies which can be classified into three main categories, namely the classical CHB, reduced-switch modules, and switched-capacitor modules. Being more compact than the H-bridge, the various reduced-switch modules in the literature increase the number of levels generation per switch count by integrating several dc sources through new circuit structures. However, the power

sharing among dc sources are unbalanced, as mentioned previously. In addition, they require the same number of isolated dc sources as that in the classical CHB. They also made no contribution in enhancing the voltage gain.

The recently explored switched-capacitor modules, on the other hand, require only a single dc source in each module while the voltage-boosting capability is made possible by integrating switched-capacitors. By discharging the switched-capacitors in series with the dc source, voltage levels higher than the dc source voltage can be generated. However, the switched-capacitors have a limited charging duration when they are not supplying the load. This leads to significant capacitor voltage ripples, although large electrolytic capacitors are used. Another challenging issue of switched-capacitor modules is the occurrence of current spikes during the charging of switched-capacitors. This is because the switched-capacitors are charged by switching them in parallel with the dc source, rendering them infeasible in practical applications.

In contrast, the proposed B5LI is distinct from all the previous topologies such that it retains the advantages of each categorized cascaded multilevel inverters in Table III. The novelty herein is that the proposed B5LI can simultaneously achieve the goals of voltage-boosting, power balancing among cascaded modules, soft-charging for dc-link capacitors, and continuous dc-link capacitors charging during operation.

The merits of the proposed B5LI can be better illustrated by presenting a further comparative analysis with topologies which do not face issues associated with power balancing and current spikes. A classical cascaded H-bridge (CHB) with 5-level generation in Fig. 5 is considered as a benchmark. Note that the classical CHB is a buck type inverter where its maximum ac voltage level is essentially equal to the total dc source voltage $2V_{dc}$. For this reason, its maximum voltage gain is limited to unity. This constraint, however, is conveniently catered for by adding a boost converter to each H-bridge, as shown in Fig. 5(b). In this instance, the voltage gain is extended to $M/(1-D)$. Although the duty-cycle D can be adjusted for voltage-boosting purpose, this CHB in Fig. 5(b) still requires the same number of isolated dc sources as that in a classical CHB.

Table IV demonstrates the superiority of the proposed B5LI over the two existing CHB variants. The proposed B5LI requires only a single dc source to generate 5 voltage levels, as opposed to two dc sources in the CHBs. In addition, when taken into comparison with the CHB with boost converter, the switch count is reduced from 12 to 10 and a twofold increase in the voltage gain is achieved.

To investigate the significance of voltage-boosting capability, the same maximum voltage level V_{max} is considered for the classical CHB and the proposed B5LI:

$$V_{max} = 2V_{dc,CHB} \qquad (23)$$

$$V_{max} = \frac{2V_{dc,B5LI}}{1-D} \qquad (24)$$

where $V_{dc,CHB}$ and $V_{dc,B5LI}$ are the dc source voltage of the classical CHB (Fig. 5(a)) and the proposed B5LI (Fig. 1), respectively. By taking the ratio of (24) to (23), the dc source voltage of the proposed B5LI in relative to that of a classical

CHB can be deduced as

$$V_{dc,B5LI} = (1-D)V_{dc,CHB} \ . \tag{25}$$

It is apparent from the expression that despite the single dc source, the high voltage-boosting gain in the proposed topology also contributes to its significantly lower dc source voltage.

TABLE III.
Comparison among different type of Cascaded Multilevel Inverters.

	Classical CHB	Reduced-switch modules [1]	Switched-capacitor modules [2]	**Proposed B5LI**
(a)	no	no	yes	yes
(b)	yes	no	yes	yes
(c)	yes	yes	no	yes
(d)	-	-	no	yes

[1] Reduced-switch modules use multiple dc sources for high levels generation.
[2] Switched-capacitor modules use single dc source with switched-capacitors integration.
(a) voltage boosting capability, (b) achieved power balancing among dc sources in all cascaded modules, (c) no current spikes issue, (d) continuous charging of capacitor during operation.

Classical CHB (5-level)

(a)

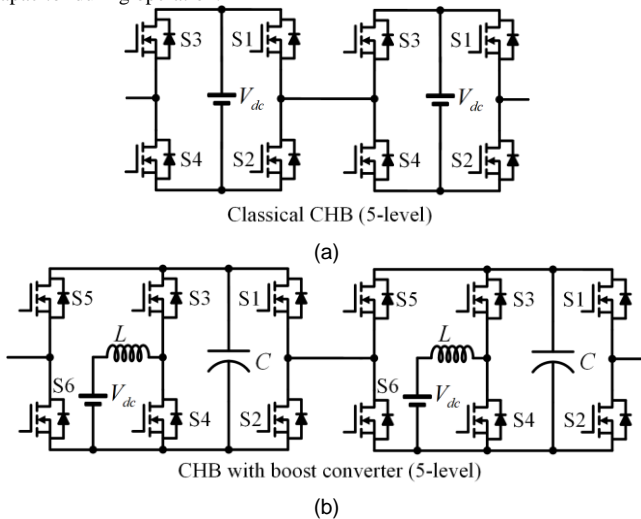CHB with boost converter (5-level)

(b)

Fig. 5. 5-level cascaded H-bridge (CHB): (a) a classical CHB and, (b) a CHB with boost converter.

TABLE IV.
Comparison among the proposed B5LI and 5-level CHBs.

	Fig. 5(a)	Fig. 5(b)	**Fig. 1 (proposed B5LI)**
Maximum level	$2V_{dc}$	$\dfrac{2V_{dc}}{1-D}$	$\dfrac{2V_{dc}}{1-D}$
Voltage gain	M	$\dfrac{M}{1-D}$	$\dfrac{2M}{1-D}$
Inductor	-	2	2
Switch count	8	12	10
Isolated dc source	2	2	1

Voltage gain is the ratio between the peak of fundamental ac voltage and the total dc source voltage.

IV. SIMULATION RESULTS

In this section, simulations are presented at $M = 0.6$ to validate the operation of the proposed topology. Fig. 6 shows that the output voltage consists of five symmetrical levels in between 588 V and – 588 V, where its maximum voltage level of 588 V matches well with its calculated value from (5). The output voltage obtained from the fast Fourier transform (FFT) analysis shows a fundamental peak voltage of 353.1 V which is

approximated to its calculated value of 352.9 V from (6). The total harmonic distortion (THD) and harmonic spectrum of the output voltage are also presented in Fig. 6. Notice that the harmonics of the ac output voltage begin at around twice the triangular carrier frequency. Fig. 7 continues to show that the efficiency of the proposed topology is 97.3% at 1 kW.
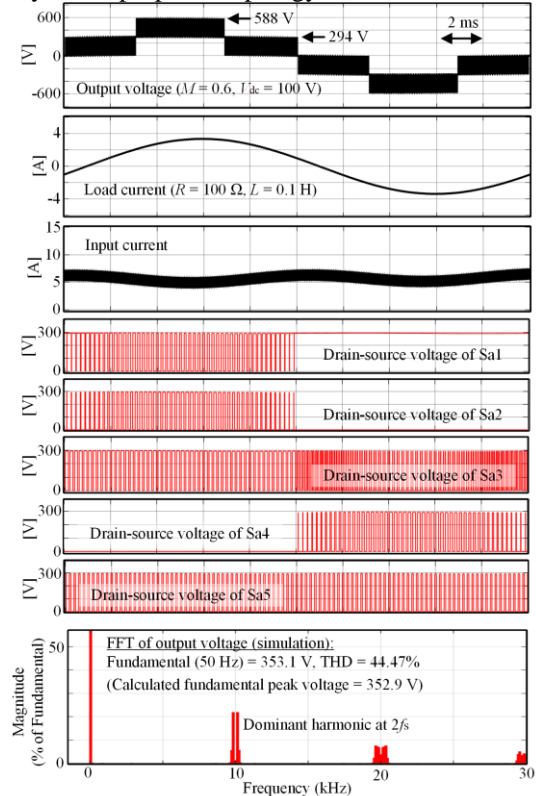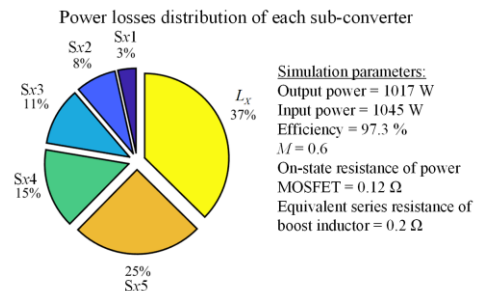

Fig. 6. Simulation results.

Fig. 7. Simulated power losses distribution of each sub-converter.

V. EXPERIMENTAL RESULTS

A laboratory prototype of the proposed B5LI was built for hardware verification. Fig. 8 shows the implementation of the proposed PWM technique using an FPGA. The experimental setup and the corresponding parameters are depicted in Fig. 9 and Table V, respectively.

The steady-state waveforms in Fig. 10 are measured when a purely resistive load, *R,* and a series resistive-inductive load, *RL,* are considered at $M = 0.8$. Similar ac voltage waveforms are observed in both load conditions. In either case, it is apparent that the dc-link capacitor voltages are boosted to 120 V from a 15-V single dc source, and the attainable maximum ac output voltage level is 240 V. The peak current for the *RL* load

is approximately 1.2 A. Considering the RL load with impedance of 153.3 Ω, the peak ac voltage at the fundamental frequency is approximately 184 V, and it implies a voltage gain that exceeds 12. The input current is shared equally among the two sub-converters and similar current waveforms are observed in boost inductors L_A and L_B. The measured currents which flow into each dc-link capacitor signifies that continuous charging of the dc-link capacitors and ac voltage generation can be attained concurrently. As the dc-link capacitor in each sub-converter is charged from their respective boost inductor, soft-charging of the capacitors is achieved in the proposed B5LI. Most importantly, the results show that the current spikes issue exists in all switched-capacitor type topologies [24] is not a concern in the proposed B5LI.
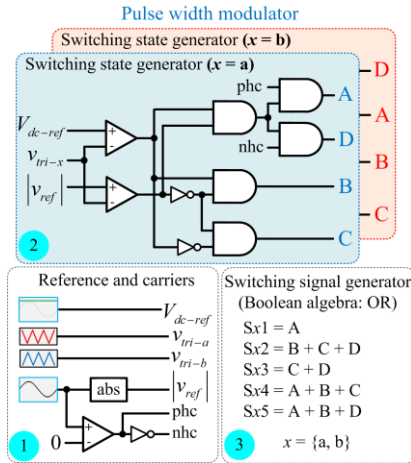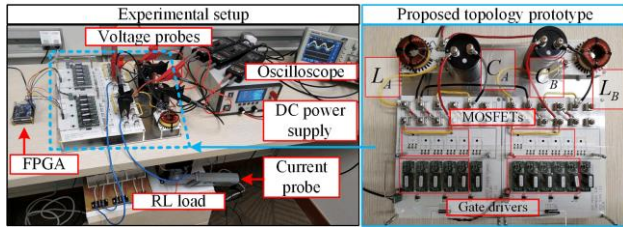

Fig. 8. PWM implementation.

Fig. 9. Experimental prototype and setup.

TABLE V.
Parameters of the Experimental Prototype

Symbol	Value
V_{dc}	15 V
D	$1.1M$
$L = L_A = L_B$	3 mH
$C = C_A = C_B$	1000 μF
Carrier frequency	5 kHz
Output frequency	50 Hz
Load resistor	150 Ω
Load inductor	100 mH
Power MOSFET	C3M0120090D

Experiments were next repeated at $M = 0.7$ to further validate the practicality of the proposed B5LI. It can be seen in Fig 11. that all the measured waveforms are identical to those in Fig. 10. Five symmetrical voltage levels are clearly illustrated in the ac output, where the maximum voltage level of 126 V is twice the voltage across the dc-link capacitors. The peak of the fundamental ac voltage computed from the measured waveforms is approximately 92 V. A voltage gain of 6 which is in good agreement with the theoretical analysis in (7) is therefore confirmed. The reactive power capability of the proposed topology is also studied by considering a purely inductive load, where the load current with a 90º phase delay is clearly observed. To validate the proposed PWM technique, Fig. 12 shows the zoomed-in view of the measured boost inductor current and ac voltage of each sub-converter. The results exhibit excellent agreement with the theoretical analysis in Fig. 3.

Figs. 13 and 14 continue to evaluate the dynamic responses of the proposed B5LI during load transients at $M = 0.8$ and 0.7, respectively. As demonstrated, the load current changes instantaneously when there is a load change between R and RL loads. The load current is sinusoidal for the RL load, and it is proportional to the ac voltage for the R load. It is important to note that neither the ac voltage waveform nor the voltage across dc-link capacitor undergoes any deterioration in performance when the transients are triggered.
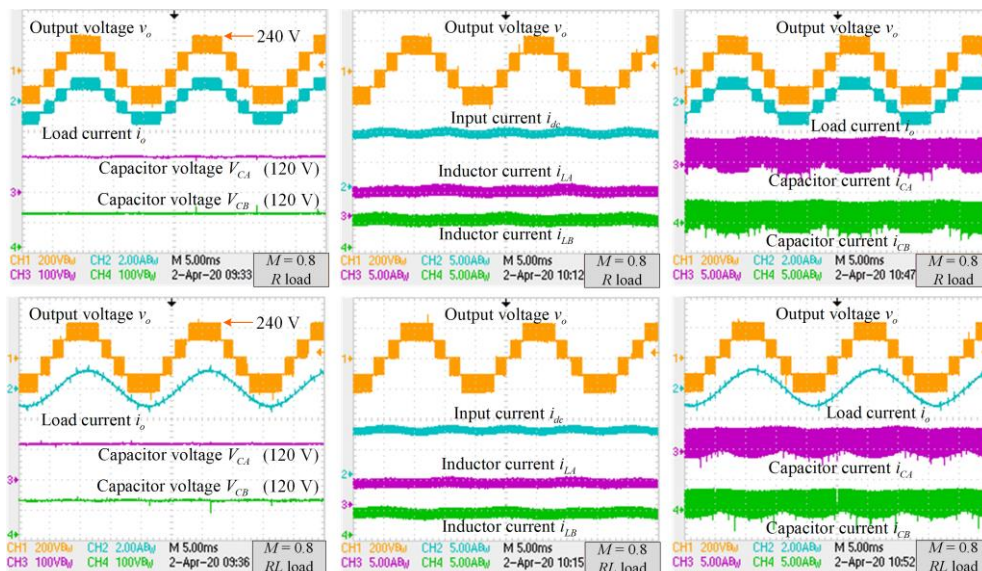

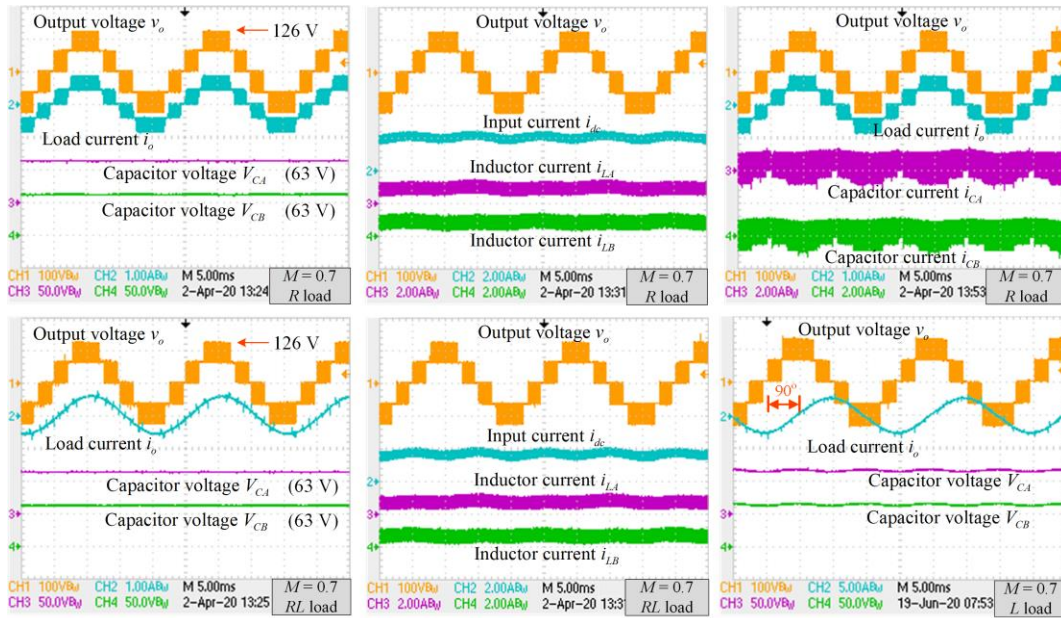Fig. 10. Measured steady-state waveforms at $M = 0.8$.

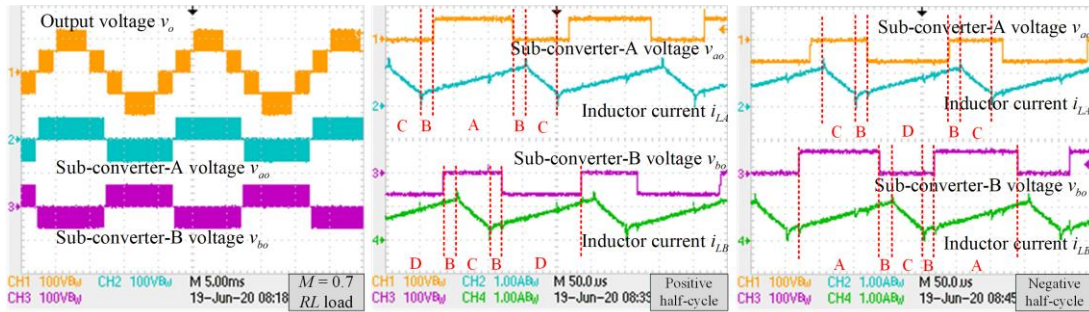Fig.11. Measured steady-state waveforms at $M = 0.7$.

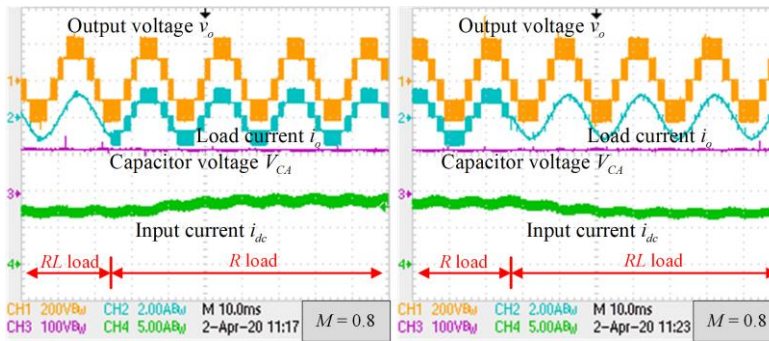Fig.12. Experimental validation of the PWM technique.

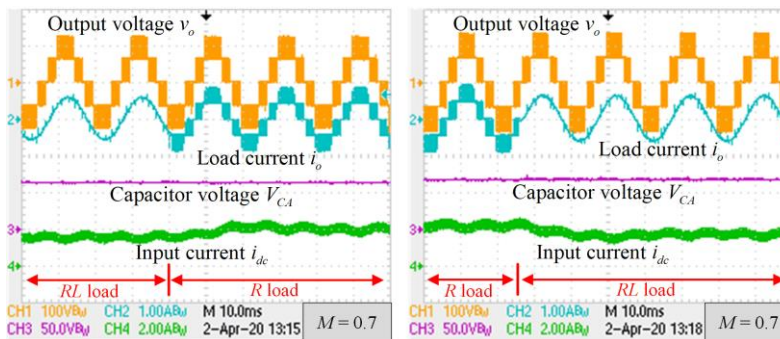Fig. 13. Measured load transient responses at $M = 0.8$.

Fig. 14. Measured load transient responses at $M = 0.7$.

VI. CONCLUSION

A novel cascaded multilevel inverter which is capable of voltage-boosting is proposed in this paper. With a merely single dc source, the proposed topology is able to achieve high voltage gain by boosting the dc-link capacitors voltage through their respective boost inductor. Besides, its reliability is guaranteed as it is not subjected to high current spikes suffered by the existing switched-capacitor type topologies. A new PWM technique for a single-stage dc-ac power conversion has also been developed, where the boost inductors can be charged with a constant duty-cycle while generating a 5-level ac voltage simultaneously. Experimental tests have confirmed the validity and feasibility of the proposed topology and its PWM technique. A good agreement is found among the theoretical analysis, simulations, and experimental results, proving that the proposed B5LI could be a viable and promising alternative to the established CHB multilevel inverter for industrial applications such as battery energy storage systems.

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