Fabrication of free-standing silicon carbide on silicon microstructures via massive silicon sublimation

Mojtaba Amjadipour[1], Jennifer MacLeod[2], Nunzio Motta[2], and Francesca Iacopi[1*]

[1] School of Electrical and Data Engineering, Faculty of Engineering and Information Technology, University of Technology Sydney, NSW, Australia

[2] School of Chemistry and Physics, Science and Engineering Faculty, Queensland University of Technology (QUT), QLD, Australia

[*] Electronic mail: francesca.iacopi@uts.edu.au

Abstract

Heteroepitaxial thin films of cubic silicon carbide (3C-SiC) on silicon offer a promising platform for leveraging the properties of SiC, such as a wide bandgap, high mechanical strength, and chemical stability, on a silicon substrate. Such heteroepitaxial films also attract considerable interest as pseudo-substrates for the growth of GaN as well as graphene on silicon wafers. However, due to a substantial lattice mismatch, the growth of 3C-SiC on silicon leads to a considerable amount of stresses, defects and diffusion phenomena at the heterointerface. We show here that the extent of such interface phenomena and stresses is so large that after patterning of the SiC, a massive sublimation of the silicon underneath the SiC/Si interface is promoted via a high temperature anneal, either in high or medium vacuum ambient. A micron-thick air gap can be formed below the SiC structures, making them suspended. Hence, the described approach can be used as a straightforward methodology to form free-standing silicon carbide structures without the need for wet or anisotropic etching and could be of great interest

for devices where suspended moving parts are needed, such as micro- and nano-electromechanical systems.

I. Introduction

Heteroepitaxial 3C-SiC/Si has considerable potential for a variety of applications such as micro-electro-mechanical systems (MEMS), high-voltage, high-frequency diodes, and transistors [1-4]. In addition, the epitaxial graphene growth on SiC on silicon enables direct graphene growth on Si wafers, which makes it compatible with semiconductor industry fabrication methods [5-7]. This methodology eliminates the need for transferring graphene to a semiconductor substrate, as is required following chemical vapor deposition (CVD) on a metal or for exfoliated graphite [6, 8]. GaN growth on the 3C-SiC/Si pseudo-substrates also has the potential interest for electronics and optoelectronics [9-10]. The use of heteroepitaxial thin films on silicon as opposed to the use of bulk SiC substrates leads to a cost reduction and enhanced micromachining and integration capabilities, which is desired for a variety of applications such as sensors, energy storage, and nanoelectronics [11-16]. However, the significant lattice mismatch between SiC and Si substrate, accompanied by atomic inter-diffusion, defects generation, and stress relaxation, adversely affect the stability of the SiC/Si interface [17-18]. Pradeepkumar et al. [19] reported a significant intermixing at the heterointerface, which takes place at high temperatures either upon SiC growth or subsequent annealing. They pointed out that the high compressive stress concentration at the heterointerface undergoes substantial relaxation above 1000°C, caused by a significant carbon diffusion microns-deep into the silicon substrate. Substantial diffusion of atomic carbon is expected to create considerable amounts of interstitial C in the silicon lattice, leading to a leaky p-n SiC/Si heterojunction as well as propagating compressive stresses deeper into the silicon substrate, microns away from the heterointerface [19-22].

Patterning plays a crucial role in semiconductor technologies [23-28]. We have extensively investigated the epitaxial graphene fabrication on patterned heteroepitaxial thin films of cubic silicon carbide (3C-SiC) on silicon [28-29]. Conventional patterning techniques include photolithography, electron-beam lithography, and focused ion beam (FIB) milling. Fabrication of SiC structures such as microcantilevers and bridges is of great importance in sensing and MEMS applications [1, 30]. Fabricating these structures using 3C-SiC on silicon thin films generally involves patterning the carbide layer followed by chemical wet etching to release the structures from the Si substrate. The wet etching step is quite time-consuming and demands the use of hazardous chemicals [1, 29, 31-32]. Therefore, developing a method to eliminate the need for a wet etching would be highly beneficial.

Here, we take advantage of the stresses generated microns deep into the silicon substrate and show an alternative path to fabricating suspended microstructures of 3C-SiC on silicon, based on a simple high-temperature anneal after patterning of the silicon carbide film.

II. Experimental Details

3C-SiC films grown on Si(111) and Si(100) were purchased from NOVASIC (France) [33-35]. The heteroepitaxial growth was carried out in a horizontal hot-wall CVD system at temperatures in the range of 1300-1400 °C by NOVASIC (France) [33]. Chemical and mechanical polishing were conducted to reduce the surface roughness to less than 1 nm (StepSiC® by NOVASIC (France)) [36]. The cubic polytype of SiC is the only type that can be heteroepitaxially grown on the readily-available, large-diameter silicon substrates [37]. The wafer was cleaned by successive 10' sonications in acetone, isopropanol, and de-ionized water, respectively.

An FEI SCIOS Dual Beam scanning electron microscopy (SEM)/focused ion beam (FIB) system was used for ion-beam patterning the first series of samples. All patterns were fabricated with a Ga beam energy of 30 keV, a dwell time of 1 µs, a beam overlap of 50 %, and a beam current of 0.1 nA. The FEI SCIOS Dual Beam system was also used for scanning transmission electron microscopy (STEM) sample preparation and measurement; beam energies between 2 and 30 keV with a range of beam current from 0.1 to 7 nA were employed. During sample preparation, a pt layer has been deposited on the area of interest to protect it against unwanted milling. A thin lamella was cut, lifted out, and welded to a copper grid using Pt deposition. The transferred sample was then thinned to about 100 nm thickness to make it transparent to electrons for STEM imaging. High-temperature annealing was conducted using an Omicron Multiprobe system with a base pressure of 10^{-10} mbar. Joule heating was employed for the high-temperature annealing at 1250 ± 15 °C for 10 minutes. The temperature was controlled using an optical pyrometer (IRCON Ultimax UX-20P with emissivity = 0.9).

The cantilever and bridge structures were patterned using electron-beam lithography followed by plasma etching. Poly(methyl methacrylate) (PMMA) 950K was used as the photoresist layer. The resist layer was spin-coated (3000 rpm, 1 minute) and baked (180 °C, 3 minutes). A Zeiss Supra 55VP SEM with a beam energy of 15 keV was used for photoresist exposure. A reactive ion etcher with 60 sccm of SF6 and 100 W power was employed for etching the SiC layer. High-temperature annealing for silicon sublimation was conducted using a Carbolite Gero furnace at ~ 1200 °C for 30 minutes with a base pressure of 10^{-6} mbar.

III. Results and Discussions

We investigated the SiC/Si interface of ion-beam patterned 3C-SiC before and after high-temperature annealing. Figure 1 shows SEM images of the SiC thin film in the as-patterned condition (Figure 1a) and after annealing to ~1200 °C for 10 minutes (Figure 1b and c). Four parallel structures (~1 µm wide and ~4 µm long) were ion-beam milled through the SiC layer thickness with a depth of ~1 µm (Figure 1a). After high-temperature annealing of the patterned samples, the SiC structures appear close to detached from the underlying substrate (Figure 1b and c). In Figure 1c, the detachment is more obvious due to different sizes and geometry, and produces a displacement of the structures from their original position.

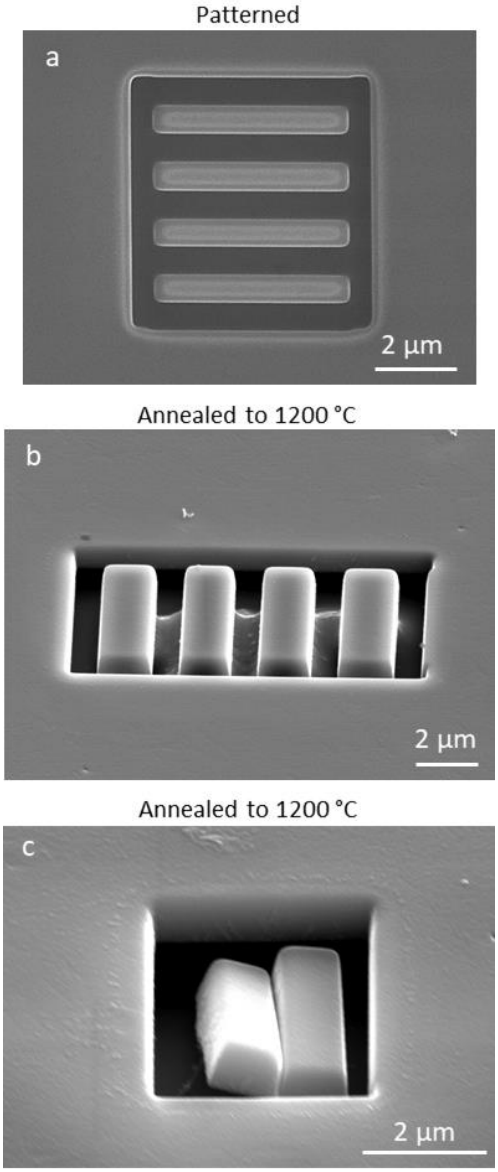

Figure 1. SEM images (a) pristine 3C-SiC/Si(111) sample patterned with four structures, 1.5 µm wide and 5 µm long. (b) same patterned sample as in (a) after high-temperature annealing to ~1200 °C for 10 minutes. (c) 3C-SiC/Si(111) patterned with structures 1 µm wide and 5 µm long, after the high-temperature annealing. Note the detachment of the two structures from the substrate.

The 3C-SiC/Si interface was further studied with cross-sectional STEM imaging. A pristine 3C-SiC/Si in as-received condition was investigated before and after the high-temperature annealing. Figure 2a shows the presence of some initial voids at the as-received 3C-SiC/Si interface; these interfacial voids are caused by silicon out-diffusion during the SiC layer growth and are often

visible through microscopy [20, 38-41]. After annealing the pristine 3C-SiC/Si sample to ~1200 ˚C for 10 minutes, the average void size at the interface was noticeably larger (Figure 2b). Figure 2c shows the 3C-SiC/Si sample, with a patterned SiC layer before high-temperature annealing. The SiC/Si interface for the sample after patterning, and before annealing, appears similar to the as-received one. However, the annealing of the patterned sample at high temperatures (~1200 ˚C for 10 minutes) produces a dramatic change (Figure 2d), with the formation of a massive gap between the SiC and the Si substrate. This gap is strongly anisotropic as it extends for about a micron depth, and in-plane, up to ~8 µm away from the patterned SiC trenches, as shown in Figure 2d.

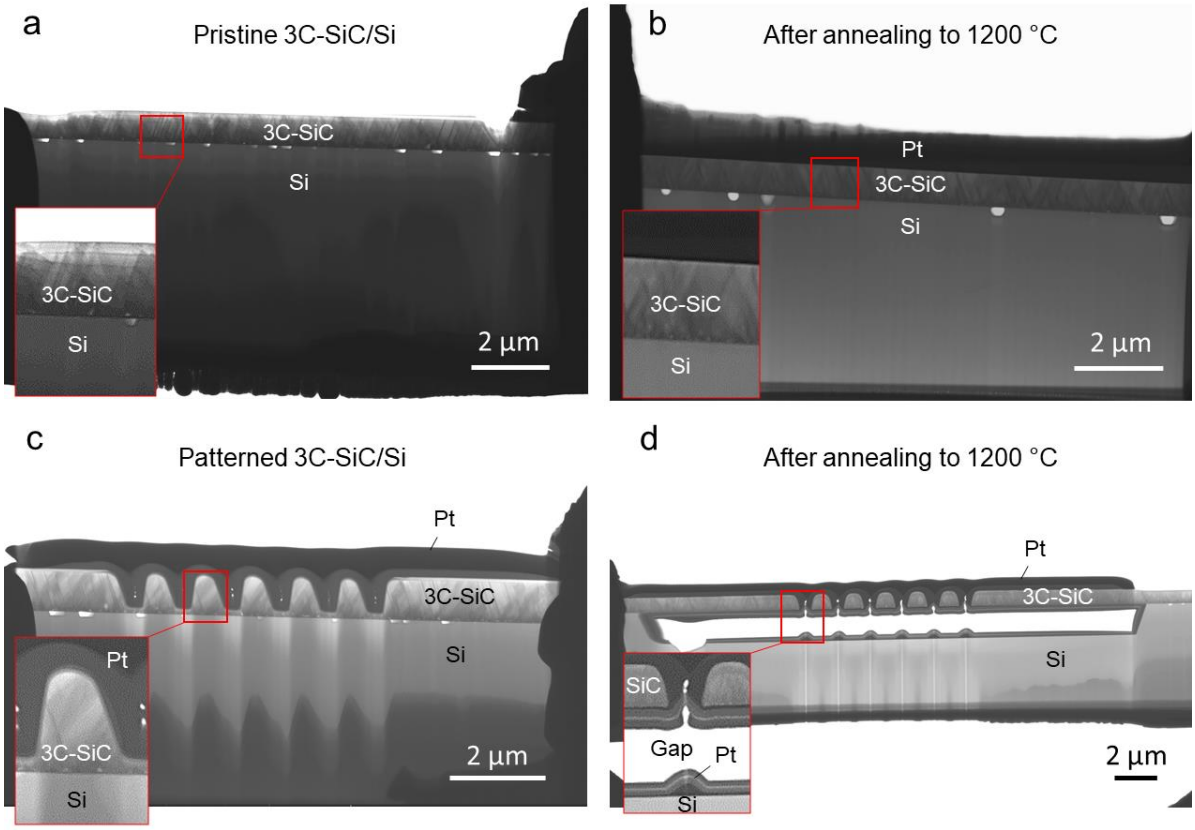

Figure 2. STEM image of 3C-SiC/Si(111) cross-sections (a) for an as-received sample, (b) the as-received sample after annealing to ~1200 ˚C for 10 minutes, (c) a patterned 3C-SiC/Si(111), and (d) the patterned 3C-SiC/Si after annealing to ~1200 ˚C for 10 minutes.

To further investigate this phenomenon, a 3C-SiC/Si sample was patterned with a depth of about only half of the SiC layer thickness (~0.5 µm). Following annealing to ~1200 ˚C for 10 minutes, the interface for the sample does not show the formation of an air gap after annealing (Figure 3). This indicates that the massive sublimation can only happen when the regions of the silicon substrate are exposed to the ambient through openings patterned in the SiC layer.

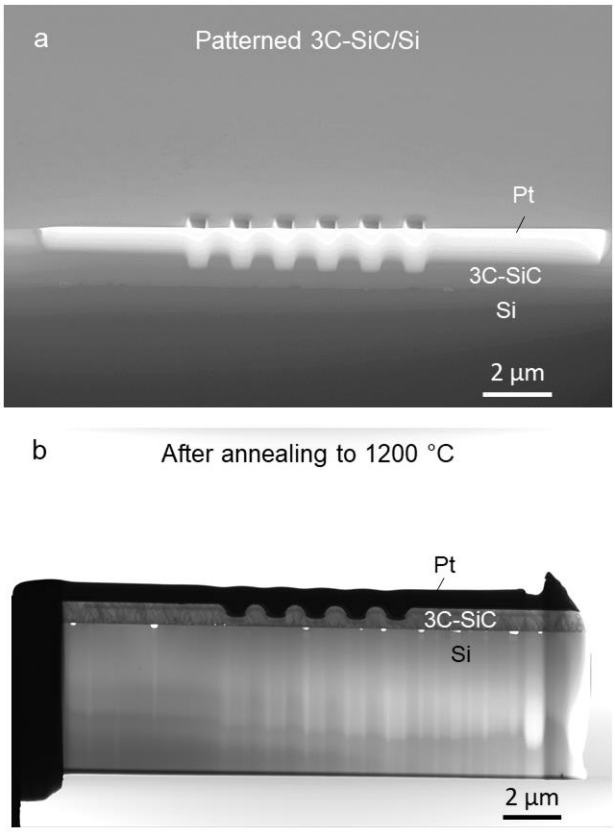

Figure 3. (a) SEM image of the cross-section of a 3C-SiC/Si(111) film only etched half-way through its thickness, before high-temperature annealing, (b) STEM cross-section image after annealing of the sample to ~1200 ˚C for 10 minutes, indicating no large gap formation under the SiC film, but only small-sized voids.

In Figure 4 a and c, we show cantilever and bridge structures of 3C-SiC/Si(100), patterned using electron-beam lithography followed by plasma etching. Figure 4 b and d indicate that after annealing of the patterned samples to ~1200 ˚C, the structures appear suspended from the Si substrate. Although a higher amount of stress is expected for the (111) orientation as compared

to (100) [17, 42], the phenomenon of massive sublimation occurs in both 3C-SiC/Si(100) and 3C-SiC/Si(111) systems. We emphasize once more that this massive sublimation is not observable in samples where the SiC has not been fully opened to expose the silicon substrate.

The observed phenomenon is hence exemplified in the schematic in Figure 5. The silicon underneath the SiC film is weakened by the compressive stresses discussed earlier, up to microns away from the interface. Therefore, when brought to high temperatures, the silicon in the top portion of the substrate has a strong tendency to sublimate. When a continuous SiC film is present above the substrate, the carbide acts as a barrier, so that a high temperature anneal can only induce small-scale sublimation of the silicon through (Figure 5, a and b). In this case, silicon can only leave the substrate through stacking faults or other defects of the heteroepitaxial SiC [41]. When patterns are fully opened in the SiC layer, the surface of the silicon substrate becomes exposed to the ambient (Figure 5c), enabling a massive sublimation upon annealing, and the formation of an anisotropic gap at the interface (Figure 5d). The strong anisotropy of this process is explained by the fact that the compressive stresses underpinning the driving force for this massive sublimation are directly related to the diffusion depth into the silicon of the atomic carbon from the heterointerface, which obeys Fick's law [43-44]. The annealing temperature, the annealing time, and the geometry of the microstructures are all expected to affect the formation of the air-gap.

This phenomenon can hence be employed to fabricate various suspended SiC structures without any chemical wet-etching. In addition, when necessary, this process may be engineered further to fabricate SiC structures which are electrically insulated from its silicon substrate.

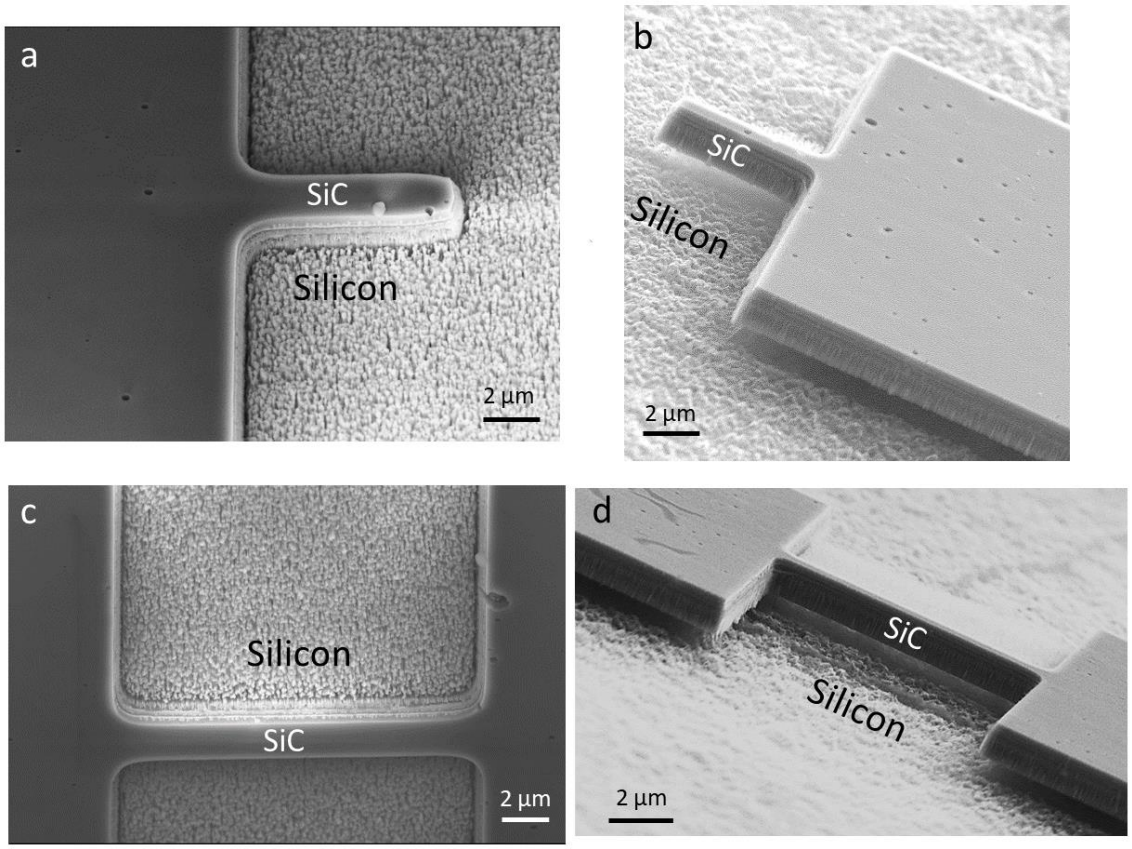

Figure 4. (a) a cantilever structure patterned on a ~2 µm thick SiC/Si(100) thin-film using electron-beam lithography and plasma etching procedure, (b) the cantilever structure after high-temperature annealing to ~1200 °C, a gap has created under the structure. (c) a bridge structure patterned on SiC/Si substrate using electron-beam lithography procedure, (d) the bridge structure after high-temperature annealing to ~1200 °C, a gap has created under the structure.

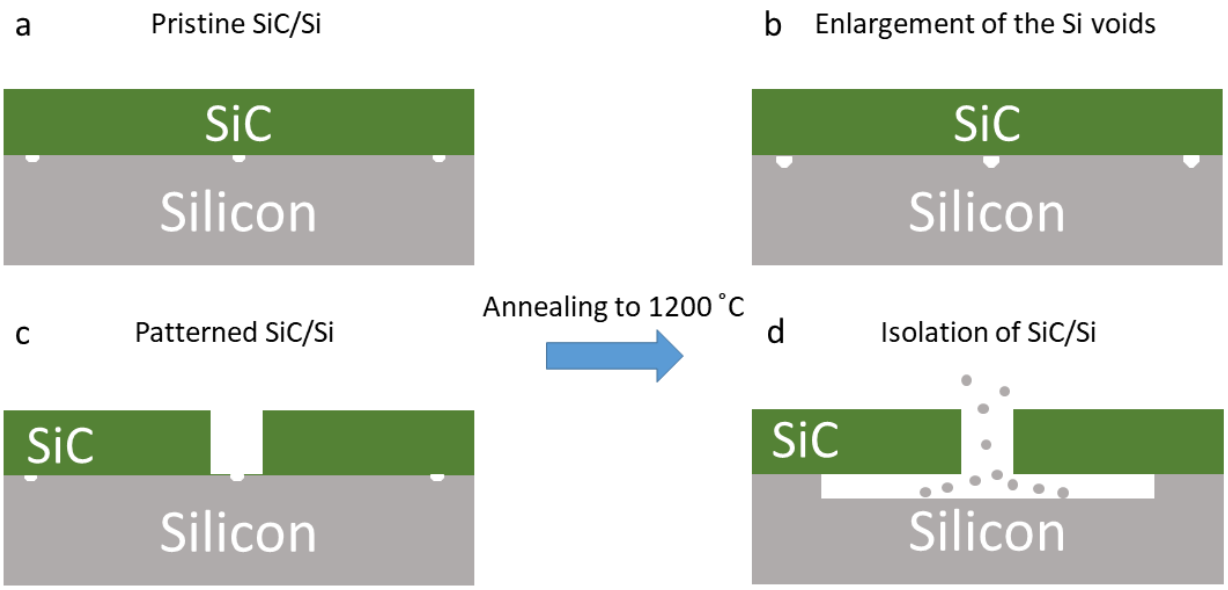

Figure 5. Schematic representation of the patterning effect on the SiC/Si interface after the high-temperature annealing (a) pristine thin film of SiC/Si with visible interfacial voids sometimes visible during the SiC growth, (b) after high-temperature annealing: enlargement of the interfacial voids, (c) patterning of the SiC/Si exposes the silicon to the atmosphere (d) high-temperature annealing leads to a massive Si sublimation, resulting in the formation of an anisotropic gap extending for microns.

IV. Conclusions

We have shown that we can induce a massive silicon sublimation underneath the interface of a heteroepitaxial SiC layer on silicon, by patterning the SiC layer to expose the silicon surface and annealing the system to either high or medium vacuum ambient. We suggest that the driving force of this massive sublimation is given by significant compressive stresses generated deep in the silicon substrate by the presence of interstitial carbon diffused from the heterointerface.

This massive sublimation is anisotropic and extends for about a micron depth and several microns in each in-plane direction from the open SiC pattern, which results in the formation of an air gap between the SiC structures and the silicon substrate.

Employing this phenomenon, we have fabricated free-standing structures of 3C-SiC on a silicon substrate. This process eliminates the need for any chemical etching step to fabricate free-standing SiC structures on Si substrate. We propose this methodology as a pathway to directly fabricate free-standing micro- and nano-structures of crystalline 3C-SiC on silicon, which are, for example, the basis for MEMS resonators with very high-quality factors [45-46]. In addition, released structures made of epitaxial graphene on SiC can be fabricated using this process. The epitaxial graphene/SiC material combination is of great relevance and benefit, particularly for mechanical [47-49] and optical/photonic applications [50-52].

Acknowledgments

Funding from the Air Force Office for Scientific Research through grants 18IOA052 is kindly acknowledged. The authors thank the support of the Queensland Government through the Q-CAS Collaborative Science Fund 2016. This work was enabled by the Central Analytical Research Facility hosted by the Institute for Future Environments at QUT and was performed in part at the Queensland node of the Australian National Fabrication Facility. The UTS MAU labs are acknowledged for providing access to the fabrication facilities. We acknowledge the technical support of Dr. Annalena Wolff, Dr. Josh Lipton-Duffin, Dr. Hui Diao, Dr. Mark Lockrey, and Mr. Geoff McCredie.

References

[1]P. S. Waggoner, H. G. Craighead, Lab on a Chip, **7**, 1238-1255, (2007).
[2]S. Nishino, Y. Hazuki, H. Matsunami, T. Tanaka, J. Electrochem. Soc., **127**, 2674-2680, (1980).
[3]J. Casady, R. W. Johnson, Solid·State Electron., **39**, 1409-1422, (1996).
[4]X. She, A. Q. Huang, O. Lucia, B. Ozpineci, IEEE Transactions on Industrial Electronics, **64**, 8193-8205, (2017).
[5]A. Van Bommel, J. Crombeen, A. Van Tooren, Surf Sci., **48**, 463-472, (1975).

[6]C. Berger, Z. Song, X. Li, X. Wu, N. Brown, C. Naud, D. Mayou, T. Li, J. Hass, A. N. Marchenkov, E. H. Conrad, P. N. First, W. A. De Heer, Science, **312**, 1191-1196, (2006).
[7]B. Gupta, M. Notarianni, N. Mishra, M. Shafiei, F. Iacopi, N. Motta, Carbon, **68**, 563-572, (2014).
[8]C. Riedl, U. Starke, J. Bernhardt, M. Franke, K. Heinz, Physical Review B, **76**, 245406, (2007).
[9]D. As, T. Frey, D. Schikora, K. Lischka, V. Cimalla, J. Pezoldt, R. Goldhahn, S. Kaiser, W. Gebhardt, Appl. Phys. Lett., **76**, 1686-1688, (2000).
[10]D. K. Wickenden, K. Faulkner, R. Brander, B. Isherwood, J. Cryst. Growth, **9**, 158-164, (1971).
[11]M. Suemitsu, Y. Miyamoto, H. Handa, A. Konno, e-Journal of Surface Science and Nanotechnology, **7**, 311-313, (2009).
[12]V. Y. Aristov, G. Urbanik, K. Kummer, D. V. Vyalikh, O. V. Molodtsova, A. B. Preobrajenski, A. A. Zakharov, C. Hess, T. Hänke, B. Buchner, Nano Lett., **10**, 992-995, (2010).
[13]A. Ouerghi, R. Belkhou, M. Marangolo, M. Silly, S. El Moussaoui, M. Eddrief, L. Largeau, M. Portail, F. Sirotti, Appl. Phys. Lett., **97**, 161905, (2010).
[14]A. Ouerghi, A. Kahouli, D. Lucot, M. Portail, L. Travers, J. Gierak, J. Penuelas, P. Jegou, A. Shukla, T. Chassagne, Appl. Phys. Lett., **96**, 191910, (2010).
[15]B. Gupta, E. Placidi, C. Hogan, N. Mishra, F. Iacopi, N. Motta, Carbon, **91**, 378-385, (2015).
[16]N. Mishra, J. Boeckl, N. Motta, F. Iacopi, Physica Status Solidi (a), **213**, 2277-2289, (2016).
[17]F. Iacopi, R. E. Brock, A. Iacopi, L. Hold, R. H. Dauskardt, Acta Mater., **61**, 6533-6540, (2013).
[18]V. Cimalla, J. Pezoldt, O. Ambacher, J. Phys. D: Appl. Phys., **40**, 6386, (2007).
[19]A. Pradeepkumar, N. Mishra, A. R. Kermany, J. J. Boeckl, J. Hellerstedt, M. S. Fuhrer, F. Iacopi, Appl. Phys. Lett., **109**, 011604, (2016).
[20]A. Pradeepkumar, M. Zielinski, M. Bosi, G. Verzellesi, D. K. Gaskill, F. Iacopi, J. Appl. Phys., **123**, 215103, (2018).
[21]A. Pradeepkumar, M. Amjadipour, N. Mishra, C. Liu, M. S. Fuhrer, A. Bendavid, F. Isa, M. Zielinski, H. I. Sirikumara, T. Jayasekera, ACS Applied Nano Materials, (2019).
[22]N. Motta, F. Iacopi, C. Coletti, *Growing graphene on semiconductors* (Pan Stanford, 2017).
[23]Y. M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H. Y. Chiu, A. Grill, P. Avouris, Science, **327**, 662-662, (2010).
[24]M. Sprinkle, M. Ruan, Y. Hu, J. Hankinson, M. Rubio-Roy, B. Zhang, X. Wu, C. Berger, W. A. De Heer, Nature Nanotechnology, **5**, 727-731, (2010).
[25]A. Celis, M. Nair, A. Taleb-Ibrahimi, E. Conrad, C. Berger, W. De Heer, A. Tejeda, J. Phys. D: Appl. Phys., **49**, 143001, (2016).
[26]M. Terrones, A. R. Botello-Méndez, J. Campos-Delgado, F. López-Urías, Y. I. Vega-Cantú, F. J. Rodríguez-Macías, A. L. Elías, E. Muñoz-Sandoval, A. G. Cano-Márquez, J.-C. Charlier, H. Terrones, Nano Today, **5**, 351-372, (2010).
[27]Z. Li, F. Chen, Applied Physics Reviews, **4**, 011103, (2017).
[28]M. Amjadipour, M. MacLeod, J. Lipton-Duffin, F. Iacopi, N. Motta, Nanotechnology, **28**, 345602, (2017).
[29]B. V. Cunning, M. Ahmed, N. Mishra, A. R. Kermany, B. Wood, F. Iacopi, Nanotechnology, **25**, 325301, (2014).
[30]J. S. Ponraj, S. C. Dhanabalan, G. Attolini, G. Salviati, Crit. Rev. Solid State Mater. Sci., **41**, 430-446, (2016).

[31]H. P. Phan, T. K. Nguyen, T. Dinh, A. Iacopi, L. Hold, M. J. Shiddiky, D. V. Dao, N. T. Nguyen, Adv. Eng. Mater., **20**, 1700858, (2018).
[32]S. S. Verbridge, J. M. Parpia, R. B. Reichenbach, L. M. Bellan, H. Craighead, J. Appl. Phys., **99**, 124304, (2006).
[33]M. Zielinski, M. Portail, S. Roy, T. Chassagne, C. Moisson, S. Kret, Y. Cordier, Materials Science and Engineering: B, **165**, 9-14, (2009).
[34]J. Meziere, M. Ucar, E. Blanquet, M. Pons, P. Ferret, L. Di Cioccio, J. Cryst. Growth, **267**, 436-451, (2004).
[35]D. Chaussende, L. Latu-Romain, L. Auvray, M. Ucar, M. Pons, R. Madar In *Large Area DPB free (111) β-SiC thick layer grown on (0001) α-SiC nominal surfaces by the CF-PVT method*, Mater. Sci. Forum, Trans Tech Publ: 2005; pp 225-228.
[36]B. Gupta, I. Di Bernardo, P. Mondelli, A. Della Pia, M. G. Betti, F. Iacopi, C. Mariani, N. Motta, Nanotechnology, **27**, 185601, (2016).
[37]L. Wang, S. Dimitrijev, J. Han, A. Iacopi, L. Hold, P. Tanner, H. B. Harrison, Thin Solid Films, **519**, 6443-6446, (2011).
[38]N. Becourt, J. Ponthenier, A. Papon, C. Jaussaud, *Influence of temperature on the formation by reactive CVD of a silicon carbide buffer layer on silicon* (Elsevier, 1993), p. 79-84.
[39]K. C. Kim, C. I. Park, J. I. Roh, K. S. Nahm, Y. H. Seo, Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, **19**, 2636-2641, (2001).
[40]S. Jiao, Y. Murakami, H. Nagasawa, H. Fukidome, I. Makabe, Y. Tateno, T. Nakabayashi, M. Suemitsu, Materials Science Forum, **806**, 89-93, (2015).
[41]M. Suemitsu, S. Jiao, H. Fukidome, Y. Tateno, I. Makabe, T. Nakabayashi, J. Phys. D, **47**, 094016, (2014).
[42]F. Iacopi, G. Walker, L. Wang, L. Malesys, S. Ma, B. V. Cunning, A. Iacopi, Appl. Phys. Lett., **102**, 011908, (2013).
[43]J. Pelleg, *Diffusion in ceramics* (Springer, 2016).
[44]A. Paul, T. Laurila, V. Vuorinen, S. V. Divinski, *Thermodynamics, diffusion and the kirkendall effect in solids* (Springer, 2014), p. 115-139.
[45]E. Romero, V. M. Valenzuela, A. R. Kermany, L. Sementilli, F. Iacopi, W. P. Bowen, Phys. Rev. Appl., **13**, 044007, (2020).
[46]A. R. Kermany, G. Brawley, N. Mishra, E. Sheridan, W. P. Bowen, F. Iacopi, Appl. Phys. Lett., **104**, 081901, (2014).
[47]M. Mehregany, C. A. Zorman, Thin Solid Films, **355**, 518-524, (1999).
[48]T. Dinh, H. P. Phan, N. Kashaninejad, T. K. Nguyen, D. V. Dao, N. T. Nguyen, Advanced Materials Interfaces, **5**, 1800764, (2018).
[49]A. R. M. Foisal, H.-P. Phan, T. Dinh, T.-K. Nguyen, N.-T. Nguyen, D. V. Dao, RSC advances, **8**, 15310-15314, (2018).
[50]Y. Jiang, J. Li, Z. Zhou, X. Jiang, D. Zhang, Sensors, **16**, 1660, (2016).
[51]F. Martini, A. Politi, Appl. Phys. Lett., **112**, 251110, (2018).
[52]P. Rufangura, T. Folland, A. Agrawal, J. D. Caldwell, F. Iacopi, Journal of Physics: Materials, (2020).

List of the figure captions

Figure 6. SEM images (a) pristine 3C-SiC/Si(111) sample patterned with four structures, 1.5 µm wide and 5 µm long. (b) same patterned sample as in (a) after high-temperature annealing to ~1200 °C for 10 minutes. (c) 3C-SiC/Si(111) patterned with structures 1 µm wide and 5 µm long, after the high-temperature annealing. Note the detachment of the two structures from the substrate.

Figure 7. STEM image of 3C-SiC/Si(111) cross-sections (a) for an as-received sample, (b) the as-received sample after annealing to ~1200 ˚C for 10 minutes, (c) a patterned 3C-SiC/Si(111), and (d) the patterned 3C-SiC/Si after annealing to ~1200 ˚C for 10 minutes.

Figure 8. (a) SEM image of the cross-section of a 3C-SiC/Si(111) film only etched half-way through its thickness, before high-temperature annealing, (b) STEM cross-section image after annealing of the sample to ~1200 ˚C for 10 minutes, indicating no large gap formation under the SiC film, but only small-sized voids.

Figure 9. (a) a cantilever structure patterned on a ~2 µm thick SiC/Si(100) thin-film using electron-beam lithography and plasma etching procedure, (b) the cantilever structure after high-temperature annealing to ~1200 °C, a gap has created under the structure. (c) a bridge structure patterned on SiC/Si substrate using electron-beam lithography procedure, (d) the bridge structure after high-temperature annealing to ~1200 °C, a gap has created under the structure.

Figure 10. Schematic representation of the patterning effect on the SiC/Si interface after the high-temperature annealing (a) pristine thin film of SiC/Si with visible interfacial voids sometimes visible during the SiC growth, (b) after high-temperature annealing: enlargement of the interfacial voids, (c) patterning of the SiC/Si exposes the silicon to the atmosphere (d) high-temperature annealing leads to a massive Si sublimation, resulting in the formation of an anisotropic gap extending for microns.