A Disturbance Rejection Based Control Strategy for Five-Level T-Type Hybrid Power Converters with Ripple Voltage Estimation Capability

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***Abstract*—This paper proposes a robust control strategy for five-level T-type (5L-T) hybrid power converters to achieve superior dynamic performance for regulating effectively the DC-bus voltage under external disturbances and generating high-quality grid current at the same time. A new filter-less DC-bus ripple voltage estimation method and a simple technique to remove this ripple component from the measured DC-bus voltage of a single-phase converter are developed. A sliding-mode control (SMC) incorporated with an extended-state observer (ESO) is employed for the outer voltage control loop, and to calculate dynamically the input (i.e. the active power reference) for the inner current tracking controller. The proposed SMC-ESO approach presents a high disturbance rejection capability and robustness against the DC-bus load variation, and thus, significantly improves the dynamic and steady-state performance during system uncertainties. Moreover, a finite control set-model predictive control algorithm is derived as the inner current controller to track their references while balancing the DC-bus capacitor voltages. The effectiveness of the proposed controller is demonstrated and verified through measurement results.**

***Index Terms*—Disturbance rejection, FCS-MPC, power quality, ripple voltage, single-phase, voltage control.**

I. Introduction

SINGLE-PHASE voltage-source converters (VSCs) are the main component to integrate DC-bus microgrids comprised of electric vehicles (EVs), energy storages (ESs), and renewable energy sources (RESs) into the distribution grid. As the active front end (AFE) rectifiers, they can control the power factor through power flow control to provide ancillary services when required [1]–[3]. It is thus of great importance to design a robust control system for these converters. In such a single-phase power conditioning system, the DC-bus voltage has a significant impact on the control of current and power flow between the microgrid and the distribution grid. The DC-bus voltage control is a challenging task due to the presence of the double-grid frequency ($2\omega_o$) pulsating power component that flows through the DC side of the converter and causes double-line frequency voltage ripple in the DC-bus voltage. The presence of this voltage ripple in the DC-bus is inherent in both inverters and rectifiers [4]. This ripple voltage in a feedback control system degrades the quality of AC current by adding additional harmonics, and therefore, must be removed in order to achieve high-quality power conversion. A low bandwidth filter is usually used to remove this low frequency ripple component completely. The low bandwidth filter, however, introduces a significant phase delay in the DC-bus voltage control loop. As a result, the control performance to regulate the DC-bus voltage is affected during transients. To regulate effectively the DC-bus voltage, a high bandwidth is desired, and thus, a trade-off should be made between the conflicting constraints, such as the grid current quality and dynamic performances [5].

Various methods have been proposed to address difficulties associated with the DC-bus ripple voltage [6]–[14]. The coupled inductor and loop compensator based approaches are presented in [6]–[8]. However, these approaches require a high order filter with poles and zeros at low frequencies. Several active filter based techniques have been introduced in [4], [9]–[13]. These techniques require additional energy storage devices and converters in the DC side, which increases the cost and control complexity, and decreases the overall efficiency. To remove this ripple, a notch filter (NF) and a finite impulse response (FIR) filter tuned at $2\omega_o$ were reported in [5] [15], and [14], respectively. However, a low bandwidth must be selected during the filter design for complete elimination of this ripple, which results in slower dynamic response during transients. To settle the conflicting constraints of the grid current distortion and dynamic performance, a new method is required that can improve the AC current quality while realizing fast dynamic performance during transients.

This paper introduces a new filter-less approach to remove the double grid-frequency voltage ripple component from the measured bus voltage. By analyzing the DC-bus voltage, an expression of the DC-bus ripple voltage component is obtained.

Instead of using an additional filter or hardware, the new method uses the existing phase-locked-loops (PLLs) information to calculate the DC-bus ripple voltage. The DC component can then be deduced by subtracting the estimated ripple from the measured DC-bus voltage. Since the proposed approach can eliminate the need for filter or additional hardware, the difficult trade-off between the conflicting constraints (i.e. grid current harmonics and transient performance) can be avoided, enabling the simple design of the voltage control loop. The proposed approach can improve the transient performance without distorting the AC current.

Another essential control aim is to self-support the DC-bus voltage under disturbances such as sudden variation of the active power drawn by the converters due to the load changes. The bus voltage regulation is usually done by the outer voltage controller, where a feedback loop is used to update the control input (the active power reference). Numerous control techniques have been reported in the literature to achieve this control objective. The most commonly employed methods are the proportion-integration (PI) based controllers due to their simple structures. These controllers employ PI with constant gain parameters for both the outer voltage controller and inner current controller [16]. Several PI-based methods have been reported in [7], [17]–[22]. The performance of these methods depends on the PI controller gain parameters that need to be updated under different operating conditions. However, most of these methods did not consider these variations. Thus, the dynamic performance will be affected by using constant PI gain parameters under different operating conditions. A PI-based method is presented in [7], which considers both conflicting constraints, such as the AC grid current quality and the DC-bus voltage fluctuations. However, this method increases the grid current distortion at low bus capacitor value.

To reduce the DC-bus voltage fluctuations during external disturbances, the feedforward control approaches are reported in [18], [23], [24]. These methods feed forward the external power to reduce the voltage fluctuation. However, these methods require additional sensors to measure the external power, which increases the cost and decreases the reliability. Nevertheless, these approaches increase the grid current harmonics due to the coupling between the DC and AC sides. The major drawback of the PI-based strategy is the dependence of dynamic and steady-state performances on the tuning of PI gain parameters in both the outer voltage controller and the inner current tracking controller. Therefore, the overall system behavior will be affected by using the constant PI gain parameters during external disturbances.

The other commonly studied approaches are the direct power control (DPC) [25], DPC based on Fuzzy method [26], and model predictive DPC [27], [28]. Among these methods, the predictive control method provides the best performance, but the parameter sensitivity is the major problem of the predictive controller [16], [27]. Recently, several advanced methods have been proposed in three-phase applications to improve the control performance such as the multiple-vector model predictive power control [29], predictive current control [30], model predictive DPC [31], and model predictive DPC with finite control set [32]. These control methods are usually governed by the conventional PI-based outer voltage control loop. Therefore, the control performance of these methods still suffer from poor dynamic behaviour or overshoot during system parameter uncertainties. Moreover, these control approaches are not studied in single-phase applications, where the control performances are affected by the DC-bus voltage ripple elimination methods. Therefore, it is much desired to design an advanced control method to improve the dynamic and steady state performance against the disturbances, and system parameter fluctuations.

In order to overcome the limitations of the existing methods, this paper proposes a sliding mode control (SMC) incorporated with an extended state observer (ESO) as the outer voltage controller. The SMC-ESO significantly improves the dynamic and steady state performance in the presence of disturbances. The available literature shows that single-phase applications traditionally employ the three-level H-bridge converter. In contrast, this paper adopts the five-level T-type converter in order to improve the AC grid current quality, and reduce the required voltage rating of the semiconductor devices and EMI filter size. However, realizing the multilevel voltage at the AC side will be affected by the use of series connected capacitor in the converter structure if further control action is not taken into account. In this work, a finite control set model predictive control (FCS-MPC) algorithm is derived to track the desired current references. A cost function is formulated to balance the voltages across the capacitors connected in series in the DC-bus of the converter.

II. System Model and Problem Statement

A. Analysis of the DC-bus voltage

The presence of double grid frequency AC voltage ripple component on the top of the DC-bus voltage is inherent in a single-phase grid-connected AC-DC power converter. Since a feedback loop is used to regulate the DC-bus voltage, this ripple component modulates the generated output AC current of the converter if the voltage ripple is not filtered properly. Consequently, the converter current is distorted by this ripple component. This ripple voltage should be managed properly in order to avoid the adverse effect on the control performances such as slow dynamic performance during transients and increased harmonic content in the generated grid current. The value of the DC-bus voltage and its double grid frequency ripple component can be calculated by balancing the input and output power of the converter as presented below.

The grid voltage $v_g(t)$ and current $i_g(t)$ are assumed as

$$v_g(t) = V_m \sin(wt) \tag{1}$$

$$i_g(t) = I_m \sin(wt + \phi) \tag{2}$$

where V_m and I_m are the peak values of the input voltage and current of the converter, respectively, ω is the angular frequency and ϕ the phase angle difference between the grid voltage and current.

To simplify the analysis, the single-phase AC-DC converter can be represented by an equivalent circuit, as shown in Fig. 1, and the power losses in the circuit are neglected. Thus, the

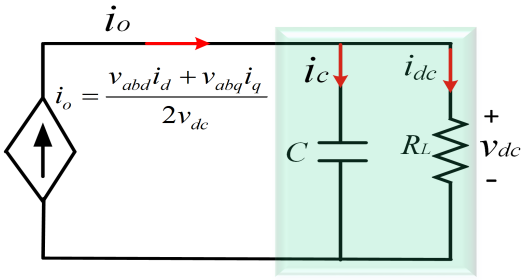

Fig. 1. Equivalent circuit of a single-phase AC-DC converter.

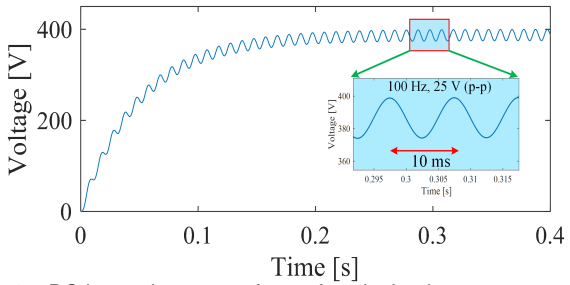

Fig. 2. DC-bus voltage waveform of a single-phase converter during turn-on transient, as given by (11).

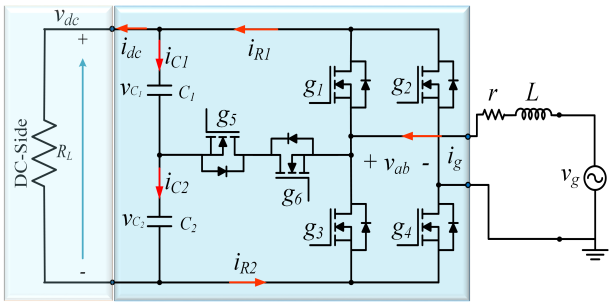

Fig. 3. Topology of the adopted single-phase T-type hybrid power converter.

instantaneous input power at the grid-side can be calculated as

$$P(t) = v_g(t) i_g(t) = \frac{V_m I_m}{2} \cos\phi - \frac{V_m I_m}{2} \cos(2\omega t + \phi) \tag{3}$$

The ripple voltage Δv is small compared to the DC bus voltage when a large capacitor is used in the DC-bus. Therefore, the input power $P(t)$ operates at approximately constant voltage. The output current can be calculated as

$$i_0(t) \cong \frac{P(t)}{V_{dc}} = \frac{V_m I_m}{2V_{dc}} \cos\phi - \frac{V_m I_m}{2V_{dc}} \cos(2\omega t + \phi) \tag{4}$$

The AC part of $i_o(t)$ flows through the DC-bus capacitor and the DC component flows through the load resistor R_L. The current through the bus capacitor can be expressed as

$$C \frac{dv_{dc}(t)}{dt} = i_0(t) - \frac{v_{dc}(t)}{R_L} \tag{5}$$

Multiplying both sides of (5) by $v_o(t)$, we have

$$C v_{dc}(t) \frac{v_{dc}(t)}{dt} = P(t) - \frac{v_{dc}^2(t)}{R_L} \tag{6}$$

From (6), it can be concluded that the power flowing into the bus capacitor C is the difference between the input power and the power consumed by the load resistor, R_L. The energy stored in the bus capacitor can be given as

$$E(t) = \frac{1}{2} C v_{dc}^2(t) \tag{7}$$

Thus, the power flowing through the bus capacitor can be written as

$$\frac{dE(t)}{dt} = C v_{dc}(t) \frac{v_{dc}(t)}{dt} \tag{8}$$

Substituting (7) and (8) into (6), we have

$$\frac{dE(t)}{dt} = P(t) - \frac{2E(t)}{R_L C} \tag{9}$$

Solving (9), we obtain

$$E(t) = E(0) e^{-\frac{2t}{R_L C}} + e^{-\frac{2t}{R_L C}} \int_0^t e^{\frac{2\tau}{R_L C}} P(\tau) d\tau \tag{10}$$

Considering that the grid voltage and current are in phase and substituting (10) into (7), one obtains the expression of the DC-bus voltage as given in (11). Fig. 2 shows a typical bus voltage waveform during turn-on obtained from (11).

As shown, the bus voltage waveform consists of double grid frequency ripple, steady-state DC and transient components. In a closed loop control system, the measured DC-bus voltage should be filtered to estimate the DC component of the bus voltage in order to avoid the harmonic distortion in the generated AC grid current by this ripple voltage. Moreover, the filtering method should provide a fast dynamic performance in calculating the DC component during the transients with zero steady-state error.

B. Dynamic System Model

Fig. 3 shows the power circuit of the single-phase five-level hybrid power converter under consideration, where the converter is connected to the power grid through a smoothing inductor of inductance, L, in series with winding resistance, r. Two capacitors, C_1 and C_2, connected in series and a resistive load R_L, are connected to the DC-bus. A step change of the load resistance, R_L, would cause a sudden variation of active power drawn by the converter from the power grid. In this paper, the step variation of the load resistance R_L is considered as the unknown external disturbance to the converter.

According to the Kirchhoff's voltage and current laws, the dynamics of the grid current $i_g(t)$ and the DC-bus series connected capacitor voltages, $\left(v_{c_1}(t) \text{ and } v_{c_2}(t)\right)$, are governed by the following equations

$$L \frac{di_g(t)}{dt} = v_g(t) - v_{ab}(t) - i_g(t) r \tag{12}$$

$$C_1 \frac{dv_{C_1}(t)}{dt} = i_{R_1}(t) - i_{dc}(t) = i_{R_1}(t) - \frac{v_{dc}(t)}{R_L} \tag{13}$$

$$C_2 \frac{dv_{C_2}(t)}{dt} = i_{R_2}(t) - i_{dc}(t) = i_{R_2}(t) - \frac{v_{dc}(t)}{R_L} \tag{14}$$

where v_{ab} is the converter output voltage, i_{R_1} and i_{R_2} are the internal current of the converter, and i_{dc} is the DC-bus current.

$$v_{dc}(t) = \sqrt{\frac{2\left(E(0)e^{-\frac{2t}{R_L C}} + e^{-\frac{2t}{R_L C}}\left(\frac{CV_m R_L I_m\left(e^{\frac{2t}{R_L C}}\right)}{4} - \frac{I_m V_m\left(\frac{CR_L\left(e^{\frac{2t}{R_L C}}\cos(2\omega t)-1\right)}{2}\right) + \frac{C^2 R_L^2 \omega e^{\frac{2t}{R_L C}}\sin(2\omega t)}{2}}{2(C^2R_L^2\omega^2+1)}\right)\right)}{C}} \tag{11}$$

Resolving the grid voltage, (v_g), the converter voltage, (v_{ab}), the inductor current, (i_L), and the DC-bus voltage, (v_{dc}) into their d and q components at the power grid frequency (ω_o), we can express the system dynamics model as follows:

$$\frac{di_d}{dt} = \frac{v_d}{L} - \frac{v_{abd}}{L} - \frac{r}{L}i_d + i_q\omega_o \tag{15}$$

$$\frac{di_q}{dt} = \frac{v_q}{L} - \frac{v_{abq}}{L} - \frac{r}{L}i_q - i_d\omega_o \tag{16}$$

$$\frac{C}{2}\frac{dv_{dc}}{dt} = \frac{v_{abd}i_d + v_{abq}i_q}{2v_{dc}} - \frac{v_{dc}}{R_L} \tag{17}$$

where i_d, v_d and v_{abd} are the d-axis, and i_q, v_q and v_{abq} are the q-axis parts in dq rotating frame of i_g, v_g, and v_{ab}, respectively.

This nonlinear system consists of three state variables i_d, i_q and v_{dc} and two control inputs v_{abd} and v_{abq}. For simplification, the winding resistance r is neglected in this analysis. When the system is at the equilibrium point, (15)-(17) can be simplified as

$$v_{abd} = v_d + i_q\omega_o L \tag{18}$$

$$v_{abq} = -i_d\omega_o L \tag{19}$$

$$\frac{v_{dc}^2}{R_L} = \frac{v_d i_d}{2} \tag{20}$$

From (18)-(20), it can be concluded that the DC-bus voltage depends on the d-axis component, i_d, of the grid current. The q-axis component of the grid current, i_q, controls the power factor. For unity power factor operation, the q-axis component must be set to zero (i.e. i_q = 0).

C. Necessity of Modelling Uncertainties

To simplify the controller design, during system modelling, various assumptions are often made to ignore the non-ideal factors, including the inductor winding resistance, switching losses, DC-bus capacitance variation, and external disturbances due to the load variations, resulting in inaccurate prediction of the actual system behavior under different operating conditions, and affecting effectiveness of the DC-bus voltage controller. Therefore, in order to design a robust controller, these system uncertainties must be considered properly.

III. Proposed Control Scheme

The proposed control approach aims to improve the steady-state and transient performances in regulating the DC-bus voltage under unexpected external disturbances, and achieving the highest grid current quality. The controller design is based on the cascaded structure. Fig. 4 illustrates the controller block

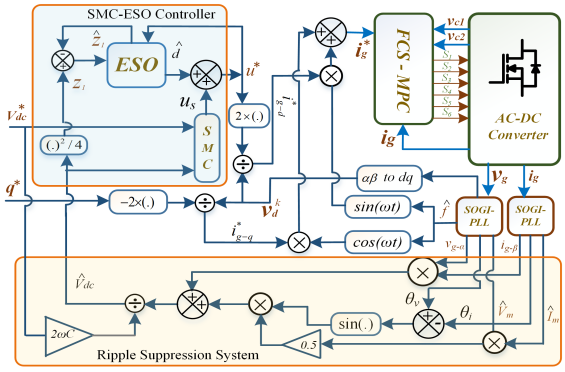

Fig. 4. Proposed control system of the hybrid power converter.

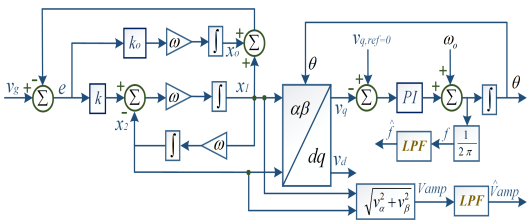

Fig. 5. Block diagram of the PLL.

diagram, including an outer voltage controller and an inner current controller. The outer voltage regulation loop consists of a sliding mode controller (SMC), an extended state observer (ESO), and a DC-bus voltage ripple estimator. The ESO is designed to estimate the disturbances to the converter, and an SMC is employed in parallel with the ESO to calculate the reference active power value for the internal current tracking controller. In this paper, a filter-less method is used to estimate the DC value of the bus voltage, which provides a fast transient performance in approximating the DC-value. Besides that, the inner current tracking controller is designed based on a finite control set-model predictive control (FCS-MPC) algorithm.

A. Proposed ripple voltage estimation method

In the proposed method, the DC-bus ripple voltage is calculated based on the estimated quantities obtained from the PLLs. The block diagram of the PLL is illustrated in Fig. 5. The estimated ripple is then subtracted from the measured bus voltage to acquire the DC component of the bus voltage. From (4), the current through the DC-bus capacitor can be expressed as

$$C\frac{dv_{dc}(t)}{dt} = -\frac{V_m I_m}{2V_{dc}}\cos(2\omega t + \phi) \tag{21}$$

where $v_{dc} = V_{dc} + \Delta v$.

By integrating (21), the magnitude of the ripple voltage component can be approximately as

$$\Delta v \cong -\frac{V_m I_m}{4V_{dc}\omega C} \tag{22}$$

Therefore, the bus voltage and its ripple component can be approximated as

$$v_{dc}(t) \approx V_{dc,avg} + \frac{V_m I_m}{4V_{dc,avg}\omega C}\sin(2\omega t + \phi) \tag{23}$$

where $V_{dc,avg}$ is the average bus voltage.

According to (23), the value of $\sin(2\omega t+\phi)$, the magnitude of the grid voltage V_m and current I_m are required to estimate the ripple component of the DC-bus voltage. In the proposed method, the α component of the grid voltage $v_{g-\alpha}$ and the β component of the grid current $i_{g-\beta}$ are multiplied to generate the grid double-frequency component. Multiplying $v_{g-\alpha}$ and $i_{g-\beta}$, we have

$$\begin{aligned} V_m \sin(\omega t) \times I_m \cos(wt+\phi) = \frac{V_m I_m}{2}\sin(2\omega t+\phi) \\ - \frac{V_m I_m}{2}\sin\phi \end{aligned} \tag{24}$$

Thus, the ripple component can be calculated by adding $(V_m.I_m/2)\sin\phi$ in (24) and multiplied by $1/(2V_{dc,avg}\omega C)$.

B. Sliding mode control

According to (20), an inherent relationship is presented between the DC-bus voltage and the d-axis component of the grid current. In other words, the DC-bus voltage depends on the active power. In this paper, an SMC is designed to calculate the reference active power value.

1. Sliding surface

The sliding surface S is chosen as a linear combination of the two state variables, i.e.

$$S = \alpha_1 x_1 + \alpha_2 x_2 \tag{25}$$

where α_1 and α_2 represent the sliding coefficients.

The controlled state variables are defined as the DC-link voltage error, x_1, and the integral of the voltage error, x_2, which can be expressed as

$$x_1 = V_{dc} - V_{dc,ref} \tag{26}$$

$$x_2 = \int (V_{dc} - V_{dc,ref})dt \tag{27}$$

Thus, the sliding surface can be given as

$$\begin{aligned} S &= \alpha_1(V_{dc} - V_{dc,ref}) + \alpha_2 \int (V_{dc} - V_{dc,ref})dt \\ &= \lambda(V_{dc} - V_{dc,ref}) + \int (V_{dc} - V_{dc,ref})dt = 0 \end{aligned} \tag{28}$$

where $\lambda = \alpha_1/\alpha_2$ is a positive constant, which should be tuned in order to achieve optimized results of settling time, steady state error, and overshoot.

The time derivative of (28) is given as

$$\dot{S} = \lambda \dot{V}_{dc} + (V_{dc} - V_{dc,ref}) \tag{29}$$

2. Control law

Rearranging (6), we can express the input power in the DC-bus as

$$P_{dc}(t) = C v_{dc}(t)\frac{v_{dc}(t)}{dt} + \frac{v_{dc}^2(t)}{R_L} \tag{30}$$

where $Cv_{dc}(t)\frac{v_{dc}(t)}{dt}$ is the power flowing into the DC-bus capacitor C and $\frac{v_{dc}^2(t)}{R_L}$ is the power consumed by the load resistor R_L.

By ignoring the switching losses, i.e. assuming the converter as lossless, the input active power $P(t)$ at the grid-side of the power converter is equal to the output power $P_{dc}(t)$ in the DC-bus. Thus, the control law is designed as

$$u = \begin{cases} P_{inst.}^{+}(t), & S > 0 \\ P_{inst.}^{-}(t), & S < 0 \end{cases} \tag{31}$$

where $P_{inst.}^{+}(t)$ and $P_{inst.}^{-}(t)$ denote the instantaneous input active power when the corresponding control decision will be directed toward the desired equilibrium point.

Therefore, (30) can be rewritten as

$$\frac{v_{dc}(t)}{dt} = \frac{u}{CV_{dc}} - \frac{V_{dc}}{R_L C} + \delta \tag{32}$$

where δ is the disturbance in the DC-bus voltage of the converter. The bound of the external disturbance, ρ_s, is considered as $|\delta| \le \rho_s < 1$, where ρ_s is a positive constant [16].

Thus, the control output can be obtained by

$$u_s = \left[\left(\frac{1}{R_L C} - \frac{1}{\lambda}\right)V_{dc} + \frac{1}{\lambda}V_{dc,ref} - (\rho_s + k).sign(S)\right]CV_{dc} \tag{33}$$

C. Observer

While the SMC law is designed according to the system model, the dynamic performance is still affected by the system parameter uncertainties (e.g., external load variation). In order to overcome the limitations of SMC, an ESO is designed and applied in parallel with the SMC to calculate the reference active power and compensate the system uncertainties, such as the external load variation and plant dynamic variation. Thus, the control output of the proposed scheme can be given as

$$u = u_s + \hat{d} \tag{34}$$

where u_s is the SMC controller output obtained by (33), and $\hat{d}$ the observed value by the observer.

From (17), the capacitor voltage dynamic can be written as

$$\frac{C}{2}\frac{dv_{dc}}{dt} = \frac{1}{v_{dc}}\left(p^* - p_t\right) \tag{35}$$

where $p^* = \frac{v_{abd}i_d + v_{abq}i_q}{2}$, $p_t = \frac{v_{dc}^2}{R_p} + \frac{v_{dc}^2}{R_L}$, and R_P is the equivalent resistance connected in parallel with the load resistor, R_L, which stands for the switching losses of the converter.

Defining a new variable $z_1 = \frac{v_{dc}^2}{4}$, one can rewrite (35) as

$$C\frac{dz_1}{dt} = u - d(t) \tag{36}$$

where $d(t) = p_t = z_2$, $p^* = u$, and the disturbance z_2 is considered as the extended state.

TABLE I
POSSIBLE STATES OF THE CONVERTER

	g_1	g_2	g_3	g_4	g_5	g_6	i_{R1}	i_{R2}	v_{ab}
$v_g > 0$	0	0	0	0	0	0	i_g	i_g	$+(v_{c1}+v_{c2})$
	0	0	0	0	1	0	0	i_g	$+v_{c2}$
	0	0	1	0	0	0	0	0	0
$v_g < 0$	0	0	0	0	0	0	i_g	i_g	$-(v_{c1}+v_{c2})$
	0	0	0	0	0	1	i_g	0	$-v_{c1}$
	0	0	0	1	0	0	0	0	0

The derivative of z_2 is defined as h, and can be expressed as

$$\frac{dz_2}{dt} = h(t) \tag{37}$$

The ESO can be designed as

$$C\dot{\hat{z}}_1 = u - \hat{z}_2 + \beta_1(z_1 - \hat{z}_1) = u - \hat{z}_2 + \beta_1 e \tag{38}$$

$$\dot{\hat{z}}_2 = -\beta_2(z_1 - \hat{z}_1) = -\beta_2 e \tag{39}$$

where $e = z_1 - \hat{z}_1$, β_1 and β_2 are the positive gain parameters of the ESO, $\hat{z}_1$ and $\hat{z}_2$ the estimated parameters of z_1 and z_2, respectively.

The error dynamics are given by

$$C\dot{e} = -\beta_1 e - e_d \tag{40}$$

$$\dot{e}_d = h(t) + \beta_2 e \tag{41}$$

where $h(t) = \hat{d}$ is defined as the load power change rate, and $e_d = d - \hat{d}$.

The systems expressed in (40) and (41) can be rewritten as

$$\begin{bmatrix} \dot{e} \\ \dot{e_d} \end{bmatrix} = \begin{bmatrix} -\frac{\beta_1}{C} & -\frac{1}{C} \\ \beta_2 & 0 \end{bmatrix} \begin{bmatrix} e \\ e_d \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} h(t) \tag{42}$$

To make the error dynamics converge to the equilibrium point, the value of the gain parameters, β_1 and β_2, are required to be chosen so that the polynomial of (42), i.e. $\lambda^2 + \frac{\beta_1}{C}\lambda + \frac{\beta_2}{C}$ is Hurwitz stable. Finally, the estimated disturbance to the converter, $\hat{d}$, is added to the control output obtained from the SMC controller to deduce the reference active power value.

D. FCS-MPC

In order to predict the grid current and the DC-bus capacitor voltages, (12)-(14) are converted into the form of discrete time by applying the Euler's discretization technique as

$$i_g[k+1] = \left(1 - \frac{rT_s}{L}\right) i_g[k] + \big(v_g[k] - v_{ab}[k]\big)\frac{T_s}{L} \tag{43}$$

$$v_{c_1}[k+1] = v_{c_1}[k] + \frac{T_s}{C_1} i_{R_1}[k] - \frac{T_s}{C_1} i_{dc}[k] \tag{44}$$

$$v_{c_2}[k+1] = v_{c_2}[k] + \frac{T_s}{C_2} i_{R_2}[k] - \frac{T_s}{C_2} i_{dc}[k] \tag{45}$$

The output voltage of the converter, v_{ab}, is obtained from Table I for different switching states. The internal currents of the converter, i_{R_1} and i_{R_2}, can be obtained from the grid current measurement, i_g, for individual switching states, as shown in Table I. As a result, the unnecessary current measurement can be avoided, which can reduce the cost and complexity of the system. In the proposed system, the current reference of the converter is calculated by

$$i_g = \frac{2p^*}{v_{gd}} \sin(\omega t) - \frac{2q^*}{v_{gd}} \cos(\omega t) \tag{46}$$

where the value of ωt is calculated from the PLL, v_{gd} the d-axis component of the grid voltage, p the control output obtained from the SMC-ESO controller, and q the reference reactive power value.

In the FCS-MPC method, to realize the desired grid current and balanced voltages across the DC-bus capacitors, the cost function is formulated as

$$g = \big(i_g^*[k+1] - i_g[k+1]\big)^2 + \frac{p^*}{v_{ref.}^2}\big(v_{c_1}[k+1] - v_{c_2}[k+1]\big)^2 \tag{47}$$

where v_{ref} is the reference value of the desired DC-bus voltage.

E. Stability analysis

Rearranging (35), we have

$$\frac{dz_1}{dt} = \frac{p^*}{C} - \frac{p_{ext.}}{C} - \frac{4z_1}{CR_p} \tag{48}$$

where $p_{ext.}$ is the external disturbance.

Applying Laplace transformation, (48) can be written as

$$z_1(s) = \frac{R_p}{(CsR_p + 4)} p^*(s) - \frac{R_p}{(CsR_p + 4)} p_{ext.}(s) \tag{49}$$

By using Laplace domain of (38) and (39), and from Fig. 6, the expression for G_{d-u} can be given as

$$G_{d-u}(s) = \frac{d(s)}{u(s)} = \frac{\beta_2}{Cs^2 + \beta_1 s + \beta_2} \tag{50}$$

Similarly, the expression for G_{d-z_1} can be given as

$$G_{d-z_1}(s) = \frac{d(s)}{z_1(s)} = \frac{\beta_1\beta_2}{Cs^2 + \beta_1 s + \beta_2} - \frac{\beta_2(\beta_1 + Cs)}{Cs^2 + \beta_1 s + \beta_2} \tag{51}$$

Therefore, based on Fig. 6, the expression for $\hat{d}(s)$ can be obtained as

$$\hat{d}(s) = \frac{\beta_2/C}{s^2 + \frac{\beta_1}{C}s + \frac{\beta_2}{C}} u(s) - \frac{\beta_2 s}{s^2 + \frac{\beta_1}{C}s + \frac{\beta_2}{C}} z_1(s) \tag{52}$$

The transfer function of the modified model can be derived as

$$G_p(s) = \frac{R_p}{(R_p cs + 4)} \times \frac{1}{\left(1 + \left(\frac{\beta_2 R_p cs}{(R_p cs+4)(Cs^2+\beta_1 s+\beta_2)}\right) - \left(\frac{\beta_2}{(Cs^2+\beta_1 s+\beta_2)}\right)\right)} \tag{53}$$

The system stability and performance are affected by the converter parameter variations, particularly by the DC-link capacitance changes. To evaluate the stability of the system, the closed loop poles of the modified model are examined to confirm the robustness for a range of the DC-bus capacitance variations. In the proposed system, the nominal value of the capacitance is 1 mF. The root loci of the model G_p with a

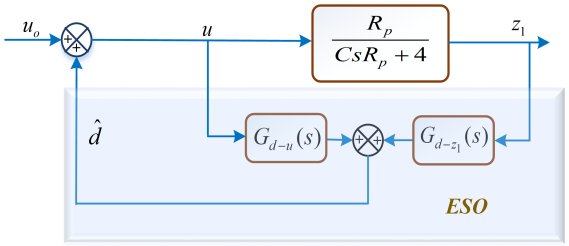

Fig. 6. Equivalent transfer function of ESO.

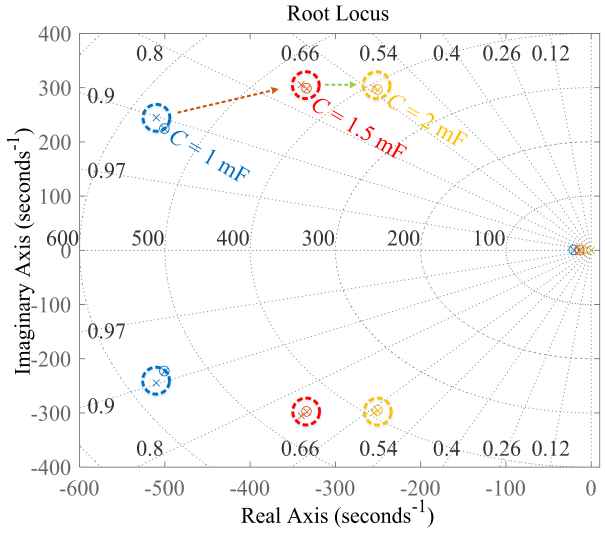

Fig. 7. Root loci of the modified model (G_p) for the variation of DC-bus capacitance.

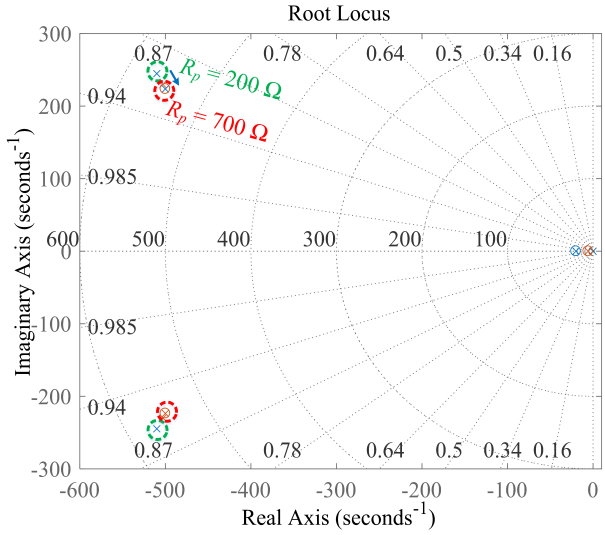

Fig. 8. Root loci of the modified model (G_p) for the variation of R_p.

large capacitance variation from 1.0 mF to 2 mF is shown in Fig. 7. It can be observed from the root loci that the closed loop pole moves toward the imaginary axis due to the increase of the DC-bus capacitance value, and thus the system becomes comparatively more oscillatory with reduced damping. However, the closed loop poles are far away from the imaginary axis even when the capacitance value reaches 2 mF, and the system still shows robustness against this variation.

TABLE II
SYSTEM AND CONTROLLER PARAMETERS

Paremeter	Value
Sampling frequency	50 kHz
Switching frequency (Max.)	25 kHz
Line frequency	50 Hz
AC input voltage (V_m)	325 V
DC-bus voltage (v_{dc})	350 V
DC-bus capacitor (C_1 = C_2)	2 mF
Grid side inductor	5 mH
R_p (Nominal)	700 Ω
PI parameters	k_p = 0.08, k_i = 0.2
ESO parameters	β_1 = 1, β_2 = 300
SMC parameters	k = 20, ρ = 0.5, λ = 0.005

The root loci of the modified model G_p with a variation of R_p from 700 Ω to 200 Ω is shown in Fig. 8. As shown, the closed loop poles are far away from the imaginary axis for this variation, and shows robustness for this changes as well.

IV. PERFORMANCE EVALUATION

To verify the proposed control scheme, the adopted converter with the specifications listed in Table II is tested. The sampling frequency is set to 50 kHz. The observed maximum switching frequency with the employed FCS-MPC based inner current tracking controller is 25 kHz. To demonstrate the feasibility of the proposed control approach, several test scenarios are implemented and compared with the existing approaches. The inner current control loop remains the same for fair comparison. Fig. 9(a) shows the AC component of the DC-bus ripple voltage, the estimated ripple voltage with the proposed method, and the calculated DC-value of the bus voltage. It can be observed that the proposed method can accurately estimate the DC-bus ripple voltage component. To evaluate the transient performance of the proposed ripple estimation method, a test scenario consists of a step change in the desired DC-bus voltage from 400 V to 350 V. In this test case, the outer voltage and the inner current control loops remain the same, and a 150 Ω load resistance is connected to the DC-bus. Figs. 9(b) and (c) show the measurement results associated with the traditional notch filter (NF) and the proposed DC-bus ripple estimation methods, respectively, in realizing the reference voltages during this step variation. The traditional NF-based method presents offset error during the transient to estimate the DC-bus ripple voltage. As a result, it degrades the dynamic performance during transients, and shows overshoot, as shown in Fig. 9(b). As shown, the settling time with the traditional NF based method is ∼150 ms and the observed DC-bus voltage overshoot ∼5 V. Fig. 9(c) shows the measurement results associated with the proposed filter-less ripple voltage estimation method during the transient. As shown, the settling time with the proposed method is ∼50 ms, which is significantly shorter than that with the NF-based method, and no overshoot is observed.

The second test scenario is designed to compare the external disturbances rejection capability of different DC-bus voltage

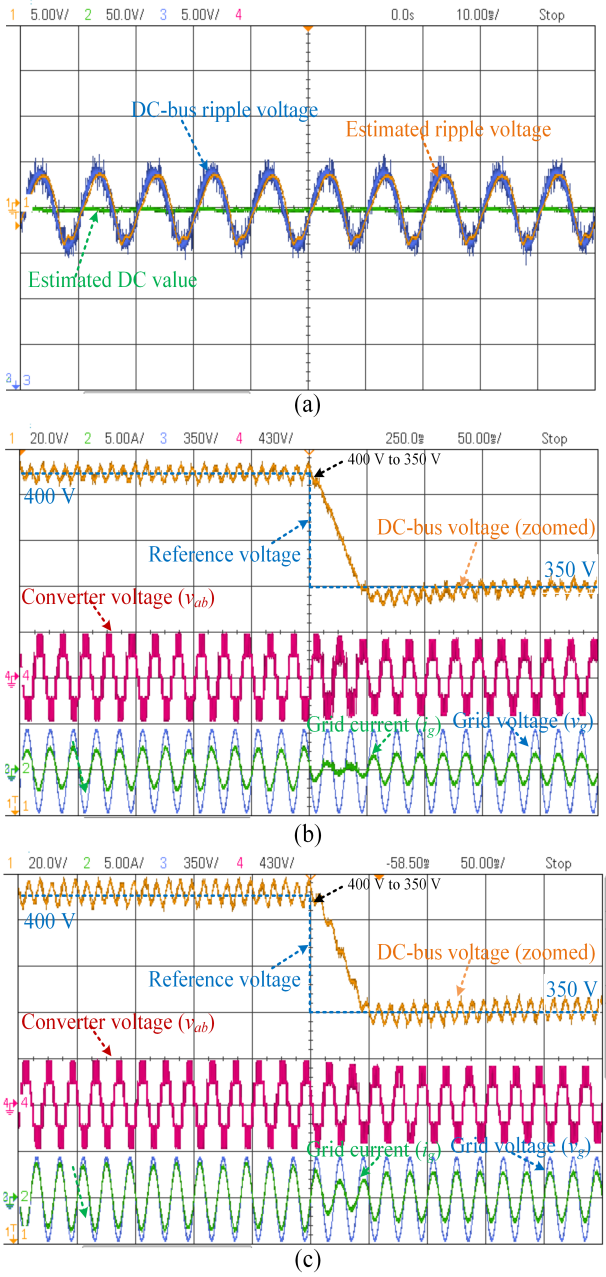

Fig. 9. Performance comparison of the ripple estimation methods, (a) DC-bus voltage ripple tracking performance of the proposed method, (b) reference DC-bus voltage tracking performance of the conventional NF based method, (c) reference DC-bus voltage tracking performance of the proposed ripple estimation method.

controllers. A step variation in the active power drawn by the converter is considered as the external disturbance, which is realized by the step changes of the DC-bus load. In this case, the proposed ripple estimation method is used to estimate the DC component of the DC-bus voltage. Figs. 10(a)-(d) show the measurement results obtained with the traditional PI controller, the PI combined with the ESO, SMC, and the proposed SMC-ESO approaches, respectively, for the step-up load variations from 200 Ω to 150 Ω. The test results show clearly that the PI-based requires 140 ms to reach the steady-state, and the observed steady-state error is ∼7 V. Moreover, the observed maximum voltage fluctuation is ∼13 V for this step load change. In contrast, the PI incorporated with the

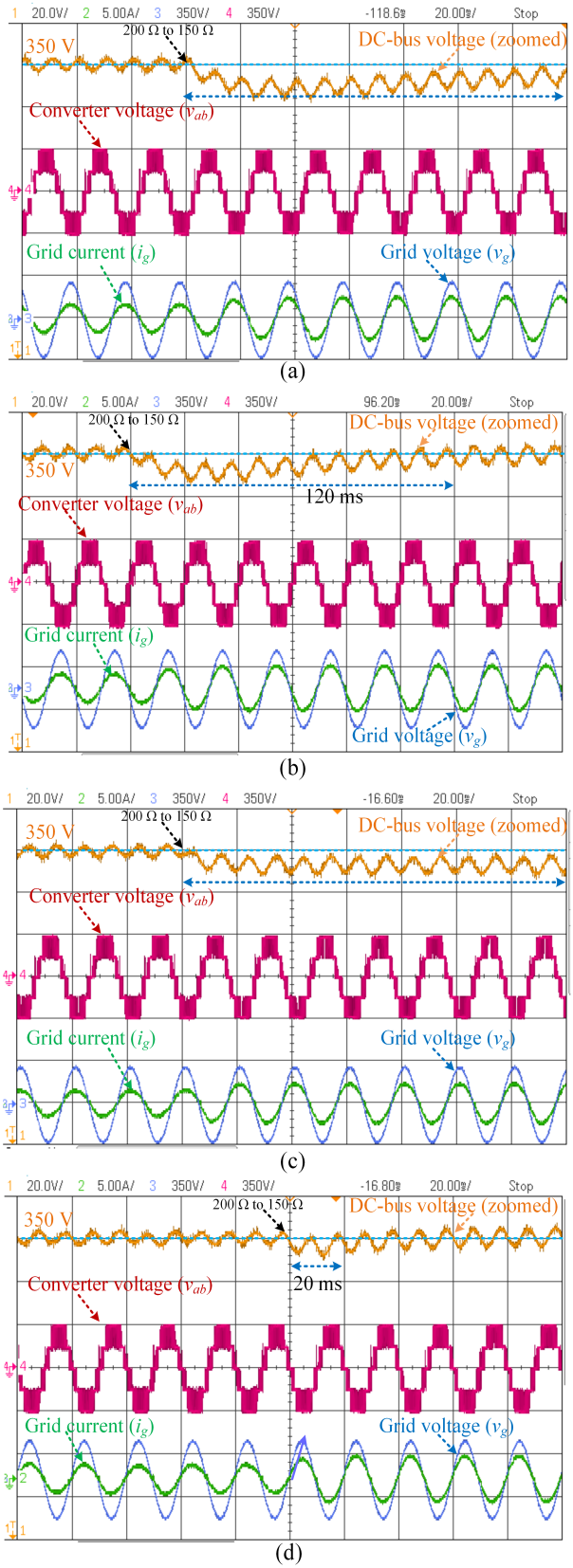

Fig. 10. Performance comparison of the control methods under step-up load condition, (a) PI, (b) PI-ESO, (c) SMC, (d) SMC-ESO.

ESO presents an improved transient performance during the step-up load change. This method requires ∼120 ms to reach the steady-state and presents zero steady-state error for this

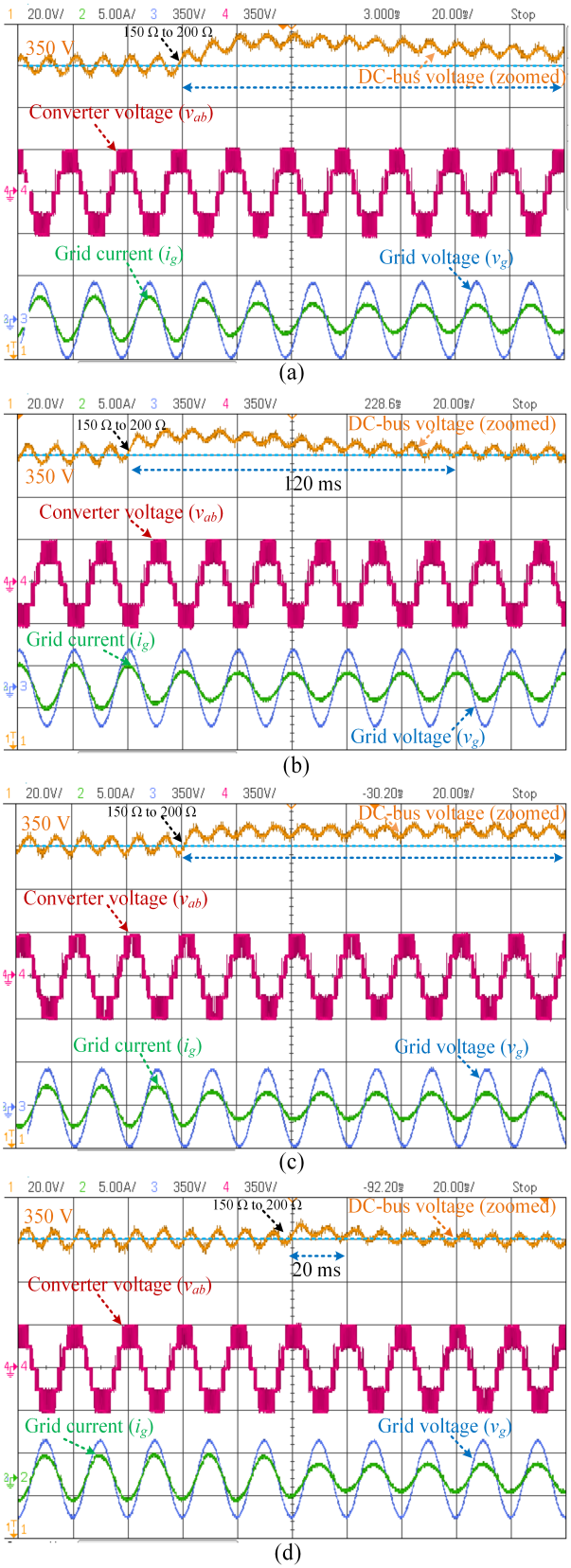

Fig. 11. Performance comparison of the control methods under step-down load condition, (a) PI, (b) PI-ESO, (c) SMC, (d) SMC-ESO.

step variation. Fig. 10(c) shows the results obtained by the traditional SMC method. The result shows that a steady-state error is observed for this uncertain load variation with the

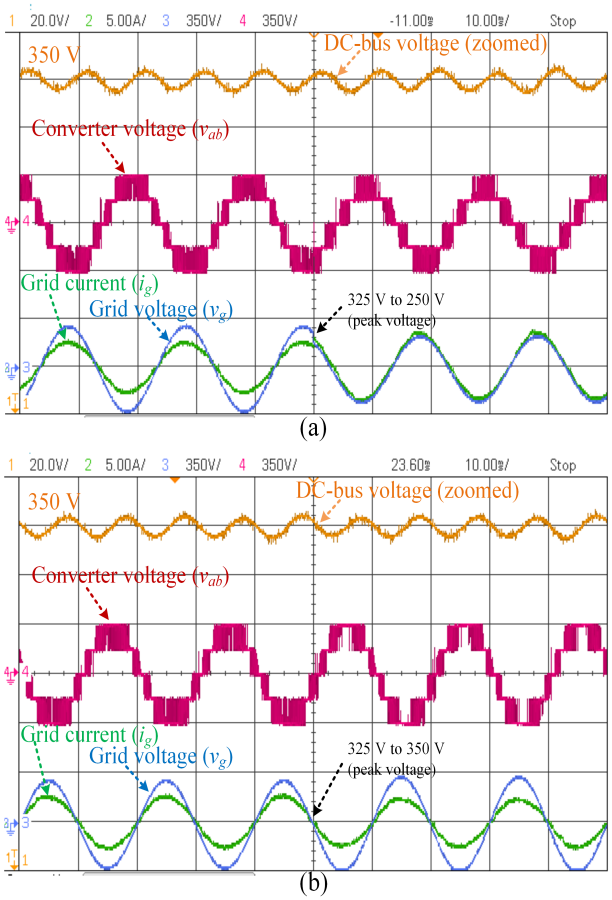

Fig. 12. Performance of the proposed method under grid voltage variations, (a) amplitude step changes from 325 V to 250 V, (b) amplitude step changes from 325 V to 350 V.

SMC method. Fig. 10(d) shows the results obtained with the proposed SMC-ESO method. As shown, the proposed method presents the best performance during the load uncertainties. This method requires ∼20 ms to reach the steady-state and the observed voltage fluctuation is ∼3 V in the transient. Similar set of tests were conducted for step-down load variations from 150 Ω to 200 Ω. The measured waveforms are presented in Fig. 11. It can be observed that the conventional PI controller requires 140 ms to reach the steady-state, and presents a voltage overshoot of ∼14 V and apparent steady-state error. Comparably, the PI-ESO requires ∼120 ms to reach the steady-state and presents an improved transient performance with a voltage overshoot of ∼9 V during the step-load change. Fig. 11(c) shows the results obtained by the traditional SMC method during this step-down load variation, and an apparent steady-state error of 8 V is observed during this variation. In contrast, the proposed SMC-ESO method presents the best performance during the load step-down. It takes ∼20 ms to reach the steady state with no visible overshoot. Form the results, it is shown clearly that the SMC-ESO presents the best performance in rejecting the uncertain external disturbances to the converter. In addition, the proposed SMC-ESO method also shows improved grid current quality compared to the traditional PI-based method. The observed grid current THD with the proposed method is 4.0%, whereas the conventional PI shows 4.7% THD in the generated grid current. Moreover,

the proposed controller performances are also evaluated for the grid disturbance conditions. In the test scenarios, the converter DC-bus reference voltage is set to 350 V. The normal condition is suddenly changed by varying the peak value of the grid voltage from 325 V to 250 V, and from 325 V to 350 V. The measurement results are given in Fig. 12. As shown, the generated grid current shows an increment or decrement to compensate those variations on the grid voltage while maintaining the desired DC-bus voltage.

V. Conclusion

In single-phase AC-DC converters, the main challenge associated with the designing of DC-bus voltage controller is a trade-off between the generated grid current quality and the DC-bus voltage dynamic performance. This trade-off becomes more difficult when the DC-bus ripple voltage is high due to the use of small bus capacitor. This paper provides an expression for the DC-bus ripple component and introduces a filter-less method to remove this component from the measured voltage completely. Consequently, it enables the reduction of the grid current distortion and presents fast dynamic performance in regulating the DC-bus voltage during the transient. To improve the dynamic performance during the external disturbances, a robust control approach based on the SMC incorporated with an ESO is proposed as the DC-bus voltage controller. The SMC-ESO control approach presents a superior dynamic performance under external disturbances compared to the traditional controllers. A predictive controller is employed as the inner current controller that ensures the equal voltages across the DC-bus capacitors and generates five-level voltages in the grid-side.

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