Design, Implementation, and Stability Analysis of a Space Vector Modulated Direct Matrix Converter for Power Flow Control in a More Reliable and Sustainable Microgrid

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Abstract: This paper presents a detailed study on technical points of design, control, stability analysis, and hardware development of a direct matrix converter with power flow control for microgrid applications. The converter is used as an interface between a microgrid AC bus and a variable-frequency load, e.g., an induction machine. The main steps of the converter design include the design of input filter, stabilization, commutation, and protection techniques. Practical guidelines are provided for the direct conversion and transmission of modulation and control procedures to the logic processing devices. Through a detailed study of stabilization technique using damping resistors, the stability region of the converter is determined by using the linearized state-space equations. A prototype direct matrix converter has been developed by the proposed design procedures, and experimentally tested for a variable frequency load.

Keywords: space vector modulation; power flow control; prototype design; stability; matrix converter

1. Introduction

The matrix converter (MC) has been an attractive research topic over the past few decades due to its advantages such as direct AC to AC conversion, low harmonic input and output sinusoidal currents, bidirectional power-flow control capability, and compact structure. In this regard, the research on MCs is mainly focused on topologies [1], modifications to the modulation techniques [2], stability analysis [3–5], loss reduction [6], commutation [7,8], and control methods, such as model predictive [9–11], sensorless and direct torque control [12].

The overall characteristics of the MC provide a context for a wide range of applications such as the induction motor drives, and grid-connected microgrids, which are traditionally driven by the voltage-source inverters [13]. The research on MCs for microgrid applications has attracted more attention due to the recent development of distributed generation and renewable energy systems. Because of their compact and simple power circuits with high power density and low maintenance requirements, MCs are particularly appealing for microgrids with AC common buses integrating the AC sources and loads with variable frequencies [14].

MCs have been used as interfaces between the AC bus and variable-frequency wind turbine generators and high-frequency turbine generators [15,16]. In [17], a three-phase dual input MC is proposed for the simultaneous integration of two renewable energy resources to an AC bus with

high efficiency and low cost. In [18], a direct MC (DMC) with bidirectional power flow control is proposed as a direct interface between a microgrid to another microgrid or the utility grid. Besides the topologies, different control techniques have also been studied in the literature. A review is presented in [19] on different topologies of direct MCs with model predictive control (MPC) that can be employed as a power interface in ac, dc, and hybrid microgrids in islanded and grid-connected modes. The modulation and control method for a bidirectional isolated ac/dc MC for application in a hybrid ac/dc microgrid is reported in [20]. The application of MC as a power interface has also been proposed for DC and hybrid microgrids [21]. This paper presents a practice to use the converter to link the AC loads or AC sources to the common AC bus in microgrids to meet the frequency requirement.

The first modulation strategy for MCs was the direct transfer function method, which proposed by Alesina and Venturini [22–24]. In this approach, the output voltages are obtained by the multiplication of the modulation matrix with the input voltages, and the maximum voltage transfer ratio is $q = 0.5$. The most common modulation method which has improved the maximum voltage transfer ratio is the space vector modulation (SVM), and is based on the instantaneous vector representation of the input and output voltages of the converter [25,26]. However, these modulation techniques are not able to directly control the input current, resulting in high risk of creating unstable resonances and distorted input current in the system. Therefore, stabilization techniques play an important role in MC control. The main proposed solutions for the stability issue are using damping resistor in the input filter [27], and filtering the measured input voltage using a low-pass filter [4,28,29]. Moreover, a combination of the methods presents a better performance as suggested in [18].

Despite the attractive features, it is a challenging task to develop effective MC modulation and control techniques to be implemented in digital signal processors (DSPs) and field-programmable gate arrays (FPGAs). Generation of switching signals with proper duty cycles, complicated commutation process of the bidirectional switches, and generation of the control codes for the digital processors are some of the issues that need to be discussed and clarified in more detail. Furthermore, practical problems such as protection of the converter is another issue, and since there is no energy storage, the MC is very sensitive to the grid disturbances [30].

While the analysis and experimental results for different aspects of MCs and improvements with respect to the performance are well presented in the literature, the practical challenges to the converter design are rarely addressed. The practical aspects of MC prototype development have never been studied as a whole, and the references that consider both the design and control of MCs in detail are very limited. The first application of MC to a frequency converter-motor prototype for industry application was reported in [31]. The paper mostly deals with the implementation of the MC, which leads to a compact regenerative drive solution. Design considerations for adjustable-speed drives have been presented in [32], which mostly concentrates on the protection issues, especially the clamp circuit. Reference [33] presents the development of reliable matrix converters for real applications, and studies the hardware of the MC to improve the converter performance.

In contrast to the existing literatures, this paper provides a complete, detailed and updated study of different technical aspects of design and implementation of a DMC. The study includes the modulation, control, stability, protection, and hardware design. The SVM and the general switching patterns are explained step by step to make the DSP and FPGA duties clear. To overcome the problem of over-voltage or over-current spikes generated by the simultaneous commutation of the bidirectional switches, the current direction based four-step commutation technique is carried out, and a simple method of its implementation by the FPGA is presented. As a further contribution, stability analysis of the converter considering the effect of the input filter parameters is studied. The experimental tests are conducted to verify the theoretical analysis.

The paper is organized as follows. The next section will introduce the technical points that should be considered in MC prototype development, including the stabilization, modulation, output current control, and commutation. Section 3 is dedicated to reviewing the hardware development, protection

and measurement, and control procedure. The results of the experimental tests are presented in Section 4. Finally, a summary of relevant remarks is included in the conclusion in Section 5.

2. System Design and Technical Considerations

One of the essential points of designing a laboratory prototype converter is the hardware troubleshooting. For this purpose, it is logical to design different parts of the converter on a separate board to make the troubleshooting easier. In case of changing any part of the circuits, replacement of a small board is more economical. Figure 1 shows a simplified block diagram of the DMC prototype. As shown, the converter consists of the following main parts:

1. The power section which includes the power modules, driver boards, input filter, and a clamp circuit,
2. The voltage and current sensor boards with over-voltage and over-current protection circuits, and
3. The control section which consists of the FPGA, the DSP, and a PC.

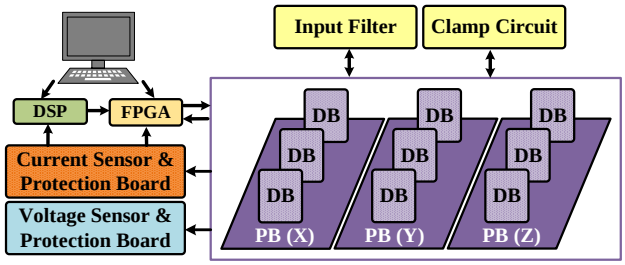


Figure 1. Overall structure of the prototype matrix converter (MC).

The power board is separated into three parts for each output leg, and each bidirectional switch has a separate driving board. In the same way, the current and voltage sensors, and the clamp circuit are placed on separate boards. Regarding the modulation and control process, the main idea is to use the numerical simulation blocks for generation of the codes for the DSP and FPGA. This facilitates the code generation procedure resulting in fast and precise transfer of changes to the digital controllers. Monitoring and debugging the control process is one of the main concerns of the prototype MC. In this prototype, PSIM software has been used for modulation and generating the C code for the DSP, and the 'DSP oscilloscope' provided by PSIM (SimCoder) is used for real-time monitoring of the control variables, and displaying the data on the computer. This allows the modulation and control parts to be observed, and monitored continuously, and any necessary changes can be transferred to the DSP immediately (using an external RS-232 cable). More details of the design of each board, as well as the modulation, closed-loop control, and stability problem of the converter will be explained in the following sections.

2.1. The System Stability Analysis

A small LC low-pass filter is commonly used at the input side of the converter to eliminate the input current spikes. The input LC filter can significantly impact the stability of the electrical power system when the output variables of the power electronic converters are tightly regulated. In this case, the converter behaves like a constant power load (CPL) and presents a negative incremental input resistance, which can destabilize the input LC filter and the converter depending on the system parameters [34,35]. The instability related to the negative input resistance can be improved by changing the input filter parameters; however, as the MC is known as an all-silicon converter and does not require any energy storage component, the size of the input filter components should be minimized, and set the input PF to the unity. The resultant instability can be resolved by different logical methods. At first, using a proper filter design, the LC parameters are determined, and then the selected stability method is applied.

2.1.1. Input Filter Design

In the MC input filter design, the parameters which should be considered are the filter size, the cost, the total harmonic distortion (THD) of the grid current and the unity input power factor. Considering optimal cost and size, a simple LC filter can adequately attenuate the high order harmonics to an acceptable level. As the harmonic contents of the input current are introduced at the integer multiples of the sampling frequency (f_s), it is possible to smooth the supply current by proper selection of the input filter parameters. The input filter design of the MC has been discussed in different literatures [36–38]. One of the advantages of MCs is the possibility of operation with unity input PF. In fact, because of the input LC filter, the displacement angle between the input voltage and current (φ_i) can be more than zero. Therefore, the unity input power factor is adjusted for the maximum voltage transfer ratio ($q = 0.866$), and hence the minimum PF is limited to the case of the minimum output power ($P_{o,min}$). In this paper, the minimum input PF is considered as 0.9 for the minimum output power of 10% rated input power $P_{i,n}$. The maximum input filter capacitance can then be determined by [36]:

$$C_f \leq \frac{P_{o,min} \tan(\varphi_{i,max})}{3\omega_i V_{i,n}^2} \quad (1)$$
$$PF_{i,min} = cos(\varphi_{i,max}) = 0.9$$
$$P_{o,min} = 0.1 P_{i,n}$$
$$P_{i,n} = 3 V_{i,n} I_{i,n}$$

where $V_{i,n}$ and $I_{i,n}$ are the rated input phase voltage and current of the MC, and $\varphi_{i,max}$ is the maximum displacement angle between them. Therefore, for a 240 V/50 Hz, 7.5 kW MC, C_f should be less than 6.69 µF, and 6.6 µF is selected. Then, the filter inductance L_f can be selected from the cut-off frequency $f_c = 1/(2\pi\sqrt{L_f C_f})$, considering that the resonant frequency is more than twenty times the input frequency f_i, and less than one-third of the sampling frequency f_s [39]. When selecting L_f, it should be noted that for gaining the maximum voltage ratio, the voltage drop across the input filter inductance at the rated input current should be minimized, and thus $L_f = 3mH$ has been selected. While higher sampling frequencies can lead to filter size reduction, it will be in the cost of increasing the power loss.

2.1.2. The Stabilization Technique

A common method to overcome the instability is to add a damping resistor (R_d) in parallel with the filter inductor for compensating the negative incremental resistance of the MC, so as to increase the stability range, as shown in Figure 2a [3,40]. The damping factor of the input filter is normally small due to the negligible value of the input filter inductor resistance R_f. By adding the parallel damping resistors, the cut-off frequency stays almost the same as that of the LC filter and the damping factor of the filter assuming $R_d \gg R_f$ increases to $\zeta_d = \frac{1}{2R_d}\sqrt{L_f/C_f}$. Using a small R_d can increase the damping property of the filter, but it would increase the power loss and THD of the input current [27].

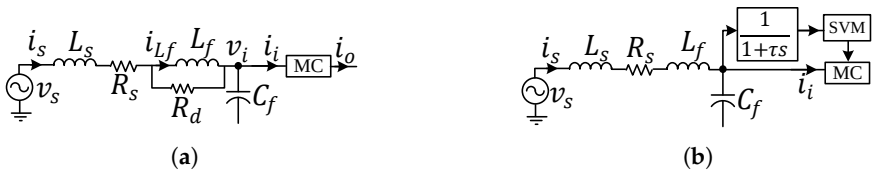


Figure 2. Input filter scheme of a single phase with, (**a**) parallel damping resistor R_d, and (**b**) digital input filter with time constant τ.

Active damping techniques can also act as a virtual resistor to damp the input filter by modifying the controller and overcome the negative impedance instability problem caused by the tightly regulated

converters [35,41]. The stabilization method using a digital filter as suggested in [4,28,29] is an active method. In this method, a low-pass digital filter with the time constant τ is implemented in the main processor to filter out the measured input voltage, as shown in Figure 2b. An advantage of the method is it has no extra cost and power loss as it is implemented in a software form. It can filter out the steady state high-frequency harmonics of the input voltage around the resonant frequency of the input filter. However, there is a possibility for the input voltage disturbances to be reflected in the output voltage, proportional to the filter time constant [4]. By increasing the filter time constant, the cut-off frequency can be reduced, and hence the low-frequency harmonics attenuated. However, this can transfer more high-frequency harmonics of the input voltage to the output side. Furthermore, the transient oscillations at the time of a power step are the other negative aspects of this strategy.

In this prototype MC, three parallel damping resistors have been added to the input filter inductors. Since the discontinuous switching behavior of MCs makes the stability analysis more complicated, the small-signal modeling using the state-space averaging method can be utilized to find the mathematical model of the converter in the form of a state matrix. To determine the stability limit of the converter, the linearized state space equations of the converter, including the added damping resistor, can be presented in a matrix form referring to the circuit presented in Figure 2a as:

$$\frac{d\Delta X_d}{dt} = A_d \Delta X_d \tag{2}$$

$$X_d = \begin{bmatrix} i_{s(d)} & i_{s(q)} & v_{i(d)} & v_{i(q)} & i_{Lf(d)} & i_{Lf(q)} & i_{o(d)} & i_{o(q)} \end{bmatrix}^T \tag{3}$$

$$A_d = \begin{bmatrix} k & \omega_i & \frac{-1}{L_s} & 0 & \frac{R_d}{L_s} & 0 & 0 & 0 \\ -\omega_i & k & 0 & \frac{-1}{L_s} & 0 & \frac{R_d}{L_s} & 0 & 0 \\ \frac{1}{C_f} & 0 & k_1 & \omega_i & 0 & 0 & -\frac{q}{C_f} & 0 \\ 0 & \frac{1}{C_f} & -\omega_i & -k_1 & 0 & 0 & 0 & 0 \\ \frac{R_d}{L_f} & 0 & 0 & 0 & -\frac{R_d}{L_f} & \omega_i & 0 & 0 \\ 0 & \frac{R_d}{L_f} & 0 & 0 & -\omega_i & -\frac{R_d}{L_f} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{R_l}{L_l} & \omega_o \\ 0 & 0 & 0 & 0 & 0 & 0 & -\omega_o & -\frac{R_l}{L_l} \end{bmatrix}$$

$$k = -\frac{R_s + R_d}{L_s} \tag{4}$$

where X_d includes the direct-quadrature (d-q) components of the space vectors of the input source current ($\vec{i}_s$), input voltage ($\vec{v}_i$), output current ($\vec{i}_o$), and input filter inductor current ($\vec{i}_{Lf}$). L_s and R_s are the input line inductance and resistance, respectively. The system stability region can be found by numerical analysis of the eigenvalues of the state matrix A_d, and determining the dominant eigenvalue that is the closest eigenvalue to the imaginary axis [4,29,40]. When the dominant eigenvalue is negative, the converter remains stable. In fact, the eigenvalues are the poles of the transfer function [42], and determine the maximum voltage transfer ratio limit for stable operation of the MC as a function of the system parameters.

Figure 3 illustrates the effect of damping resistor on the limit of the voltage transfer ratio. As can be seen, without the damping resistor ($R_d = inf$), the system stability is limited to the small range of voltage transfer ratio less than 0.3, and reducing R_d results in the higher voltage ratio limit. However, there is a limitation for this reduction, and an optimal value of R_d can be found for a system with certain

parameters. Furthermore, it should be considered that smaller parallel damping resistance leads to a larger THD of the input current, in addition to a higher power loss. Figure 4 illustrates how the input filter parameters can affect the stability region of the system. The 3D surfaces determine the stability margin, and the stability region is under the surfaces. As can be seen in the figures, the maximum voltage transfer ratio is accessible using a wider range of R_d when C_f or L_f are assigned larger values. Therefore, as the filter parameters cannot be over enlarged, referring to the filter designation criteria, the damping resistor needs to be reduced to a specified value to keep the system stable [18].

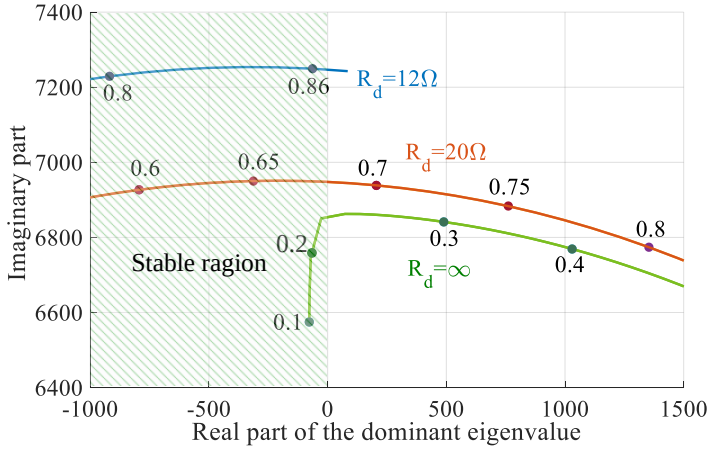
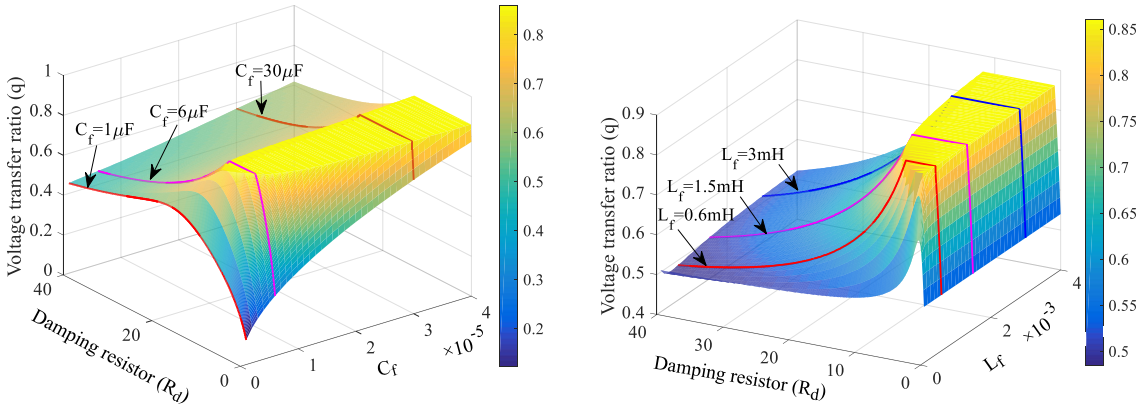


Figure 3. Position of the dominant eigenvalue of the state matrix A_d in the complex plane as a function of the voltage transfer ratio (q) for different values of R_d.



(**a**) (**b**)

Figure 4. Stability region of the converter (under the surfaces) based on the voltage ratio (q), and damping resistance (R_d), for different values of, (**a**) filter capacitance C_f, and (**b**) filter inductance L_f.

According to the system parameters listed in Table 1, and Figure 3, R_d = 12 Ω is a suitable value to keep the system stable over the whole range of the voltage transfer ratio. However, there are some other factors that can affect the system stability and are not possible to be included in the stabilization analysis using the small-signal modeling. Some of these factors are the switching frequency, the switching period delay, the converter power losses, the digital implementation of the modulation process, the commutation process of switching devices, and the number of branch switch overs (BSOs) [4,28,43]. Considering these factors, the experimental results show that damping resistance R_d = 20 Ω is a proper selection, which leads to less harmonic distortion of the input current, and less power loss arising from the damping resistors.

Table 1. Matrix converter parameters

Source voltage (phase to phase)	140 Vrms
Input frequency	f_i = 50 Hz
Output frequency	f_o = 60 Hz
Input filter inductance	L_f = 3 mH
Input filter capacitance	C_f = 6.6 μ F
Input filter resistance	R_f = 0.5 Ω
Load inductance	L_l = 6 mH
Load resistance	R_l = 10 Ω
Damping resistance	R_d =20 Ω
Input line inductance	L_s = 0.2 mH
Input line resistance	R_s = 0.5 Ω
Clamp capacitance	C_c = 3.2 μF
Clamp resistance	R_c = 50 kΩ
Sampling period	T_s = 100 μs

2.2. Space Vector Modulation

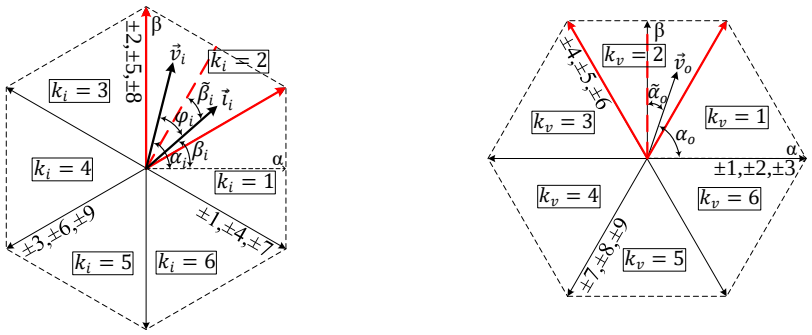
Modulation is one of the main issues of converters including the MCs. Modulation methods are the open-loop control strategies of MCs, which control the converter to generate the desired reference waveform. On the other hand, the closed-loop control strategies include a combination of both modulation and control of desired variables, such as current, voltage, and power. Different modulation methods for direct and indirect MCs have been introduced in the literature [22,23,25,37,44–48]. The modulation process determines how the bidirectional switches, which are arranged to connect the input phases to the output legs, should be switched to generate the reference waveform.

One of the most preferred modulation techniques for MCs is the SVM. There are two versions of SVM known as, direct SVM (DSVM) and indirect SVM (ISVM). The ISVM utilizes the rectifier-inverter concept and considers the MC as a two-stage converter, which is easier to understand [49]. The DSVM strategy, unlike ISVM, does not make use of any imaginary dc-link, and the output voltages are directly generated from the input voltages [25,26]. However, the ISVM can also be applied to the DMC with the same results of the DSVM, using the final vector duty cycles that are deduced for the entire matrix converter. Some of the advantages of SVM are controllable input power factor, obtaining the maximum voltage transfer ratio ($q = 0.866$), minimizing the switching numbers using a proper switching pattern, operating under the unbalanced and distorted conditions.

The SVM is based on the instantaneous space vectors of the currents and voltages to present three-phase time-variant quantities in a complex plane [45,46,50]. For a sinusoidal and balanced three-phase system, the space vectors of the input current ($\vec{i}_i(t)$) and output voltage ($\vec{v}_o(t)$) can be written as:

$$\begin{cases} \vec{i}_i(t) = \vec{I}_i e^{j\omega_i t} = I_{im} e^{j\beta_i} e^{j\omega_i t} \\ \vec{v}_o(t) = \vec{V}_o e^{j\omega_o t} = V_{om} e^{j\alpha_o} e^{j\omega_o t} \end{cases} \quad (5)$$

where β_i and α_o are the angles of the vectors $\vec{i}_i(t)$ and $\vec{v}_o(t)$ respectively at the instant $t = 0$, as shown in Figure 5. In this paper, variable '$\bar{x}$' with a bar sign over stands for a vector whose components represent the values of the three-phase system variables, and variable '$\vec{x}$' with a vector sign over, stands for its space vector.



(**a**) (**b**)

Figure 5. (**a**) Input voltage and current vectors in the second sector, (**b**) Output voltage reference vector in the second sector.

In a DMC with nine bidirectional switches, considering the rules of avoiding input short circuit, and output open circuit, to avoid the voltage spikes, there are only 27 safe 'switching configurations' as illustrated in Table 2. Each 'switching configuration' or 'switching state' includes three switches that are connected simultaneously for a specified time interval $t_n, \{n = 1, ..., 4\}$, to connect the output legs to the input phases. The target of the SVM control technique is to generate the output voltage vector according to the reference output voltage vector, and to control the input power factor by controlling the phase angle of the input current vector $\vec{i}_i(t)$. For this purpose, the conventional DSVM method can be applied to the DMC using 21 states of the safe switching configurations [26]. In the case of 18 first switching configurations, the input current and output voltage space vectors have fixed directions and variable amplitudes, and are called 'active vectors'. In the next three configurations, all output phases are connected to the same input phase. Therefore, the input current and output voltage space vectors have zero amplitude, and are called 'zero vectors'. In the last six states, the input current and output voltage space vectors are called 'rotating vectors' with constant amplitudes and variable directions that are not used in the conventional SVM. According to Table 2, both the input current and output voltage active vectors can be shown in six different directions which form two hexagons. Figure 5 shows the vectors in the second sector of the hexagons.

Table 2. Safe switching configurations of direct MC (DMC), and the output voltage and the input current space vectors associated with them.

Switch. Config.	**XYZ**	**Conducting Switches**	**Output Voltage vec.**		**Input Current vec.**	
			$\lvert\vec{v}_o\rvert$	α_o	$\lvert\vec{i}_i\rvert$	β_i
+1	ABB	S_{XA},S_{YB},S_{ZB}	$\frac{2}{3}v_{AB}$	0	$2/\sqrt{3}\ i_X$	$-\pi/6$
−1	BAA	S_{XB},S_{YA},S_{ZA}	$-\frac{2}{3}v_{AB}$	0	$-2/\sqrt{3}\ i_X$	$-\pi/6$
+2	BCC	S_{XB},S_{YC},S_{ZC}	$\frac{2}{3}v_{BC}$	0	$2/\sqrt{3}\ i_X$	$\pi/2$
−2	CBB	S_{XC},S_{YB},S_{ZB}	$-\frac{2}{3}v_{BC}$	0	$-2/\sqrt{3}\ i_X$	$\pi/2$
+3	CAA	S_{XC},S_{YA},S_{ZA}	$\frac{2}{3}v_{CA}$	0	$2/\sqrt{3}\ i_X$	$7\pi/6$
−3	ACC	S_{XA},S_{YC},S_{ZC}	$-\frac{2}{3}v_{CA}$	0	$-2/\sqrt{3}\ i_X$	$7\pi/6$
+4	BAB	S_{XB},S_{YA},S_{ZB}	$\frac{2}{3}v_{AB}$	$2\pi/3$	$2/\sqrt{3}\ i_Y$	$-\pi/6$
−4	ABA	S_{XA},S_{YB},S_{ZA}	$-\frac{2}{3}v_{AB}$	$2\pi/3$	$-2/\sqrt{3}\ i_Y$	$-\pi/6$

Table 2. *Cont.*

Switch. Config.	XYZ	Conducting Switches	Output Voltage vec.		Input Current vec.	
			$\lvert\vec{v}_o\rvert$	α_o	$\lvert\vec{i}_i\rvert$	β_i
+5	CBC	S_{XC},S_{YB},S_{ZC}	$\frac{2}{3}v_{BC}$	$2\pi/3$	$2/\sqrt{3}\ i_Y$	$\pi/2$
−5	BCB	S_{XB},S_{YC},S_{ZB}	$-\frac{2}{3}v_{BC}$	$2\pi/3$	$-2/\sqrt{3}\ i_Y$	$\pi/2$
+6	ACA	S_{XA},S_{YC},S_{ZA}	$\frac{2}{3}v_{CA}$	$2\pi/3$	$2/\sqrt{3}\ i_Y$	$7\pi/6$
−6	CAC	S_{XC},S_{YA},S_{ZC}	$-\frac{2}{3}v_{CA}$	$2\pi/3$	$-2/\sqrt{3}\ i_Y$	$7\pi/6$
+7	BBA	S_{XB},S_{YB},S_{ZA}	$\frac{2}{3}v_{AB}$	$4\pi/3$	$2/\sqrt{3}\ i_Z$	$-\pi/6$
−7	AAB	S_{XA},S_{YA},S_{ZB}	$-\frac{2}{3}v_{AB}$	$4\pi/3$	$-2/\sqrt{3}\ i_Z$	$-\pi/6$
+8	CCB	S_{XC},S_{YC},S_{ZB}	$\frac{2}{3}v_{BC}$	$4\pi/3$	$2/\sqrt{3}\ i_Z$	$\pi/2$
−8	BBC	S_{XB},S_{YB},S_{ZC}	$-\frac{2}{3}v_{BC}$	$4\pi/3$	$-2/\sqrt{3}\ i_Z$	$\pi/2$
+9	AAC	S_{XA},S_{YA},S_{ZC}	$\frac{2}{3}v_{CA}$	$4\pi/3$	$2/\sqrt{3}\ i_Z$	$7\pi/6$
−9	CCA	S_{XC},S_{YC},S_{ZA}	$-\frac{2}{3}v_{CA}$	$4\pi/3$	$-2/\sqrt{3}\ i_Z$	$7\pi/6$
0_A	AAA	S_{XA},S_{YA},S_{ZA}	0	—	0	—
0_B	BBB	S_{XB},S_{YB},S_{ZB}	0	—	0	—
0_C	CCC	S_{XC},S_{YC},S_{ZC}	0	—	0	—
R_1	ABC	S_{XA},S_{YB},S_{ZC}	V_{im}	$\omega_i t$	I_{om}	$\omega_o t+\varphi_o$
R_2	ACB	S_{XA},S_{YC},S_{ZB}	V_{im}	$-\omega_i t$	I_{om}	$-\omega_o t-\varphi_o$
R_3	BAC	S_{XB},S_{YA},S_{ZC}	V_{im}	$-\omega_i t+\frac{2\pi}{3}$	I_{om}	$-\omega_o t+\frac{2\pi}{3}-\varphi_o$
R_4	BCA	S_{XB},S_{YC},S_{ZA}	V_{im}	$\omega_i t+\frac{4\pi}{3}$	I_{om}	$\omega_o t+\frac{4\pi}{3}+\varphi_o$
R_5	CAB	S_{XC},S_{YA},S_{ZB}	V_{im}	$\omega_i t+\frac{2\pi}{3}$	I_{om}	$\omega_o t+\frac{2\pi}{3}+\varphi_o$
R_6	CBA	S_{XC},S_{YB},S_{ZA}	V_{im}	$-\omega_i t+\frac{4\pi}{3}$	I_{om}	$-\omega_o t+\frac{4\pi}{3}-\varphi_o$

Each input current or output voltage space vector can be located in any of the resultant sectors k_i and k_v, and can be constructed using a combination of the two adjacent vectors in its related sector. For example, if both input current and output voltage vectors are in sector 2, as shown in Figure 5, the active switching configurations are +5, −6, −8, +9 which form a switching sequence for a sampling period T_s. Considering six sectors of k_i and k_v, there are 36 switching sequences, as shown in Table 3. As the application time of the switching configurations (the time intervals t_0, ..., t_4) are variable, a fixed sampling period (T_s) is selected, and a sequence of the switching configurations are applied within the sampling period. The fixed sampling period results in the fixed average switching frequency f_{sw}, and improves the input filter size, switching loss, and harmonic performance. The durations of the selected switching configurations in a sampling period are known as the vector duty-cycles, and according to the DSVM, are calculated as the following [25,26]:

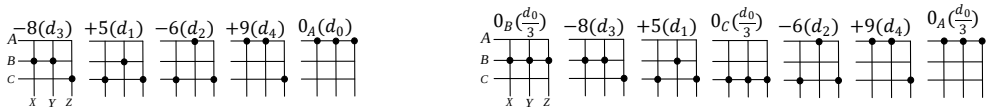
$$
\begin{aligned}
d_1 &= \frac{t_1}{T_s} = \frac{2}{\sqrt{3}} q \frac{\cos(\tilde{\alpha}_o - \frac{\pi}{3}) \cos(\tilde{\beta}_i - \frac{\pi}{3})}{\cos \varphi_i} \\
d_2 &= \frac{t_2}{T_s} = \frac{2}{\sqrt{3}} q \frac{\cos(\tilde{\alpha}_o - \frac{\pi}{3}) \cos(\tilde{\beta}_i + \frac{\pi}{3})}{\cos \varphi_i} \\
d_3 &= \frac{t_3}{T_s} = \frac{2}{\sqrt{3}} q \frac{\cos(\tilde{\alpha}_o + \frac{\pi}{3}) \cos(\tilde{\beta}_i - \frac{\pi}{3})}{\cos \varphi_i} \\
d_4 &= \frac{t_4}{T_s} = \frac{2}{\sqrt{3}} q \frac{\cos(\tilde{\alpha}_o + \frac{\pi}{3}) \cos(\tilde{\beta}_i + \frac{\pi}{3})}{\cos \varphi_i} \\
d_0 &= \frac{t_0}{T_s} = 1 - (d_1 + d_2 + d_3 + d_4) \\
q &= \frac{V_{om}}{V_{im}}
\end{aligned}
\tag{6}
$$

where $\tilde{\beta}_i$ and $\tilde{\alpha}_o$ are the phase angles of the input current and the output voltage vectors respectively with referred to the bisecting line of the corresponding sector ($-\frac{\pi}{6} < (\tilde{\alpha}_o, \tilde{\beta}_i) < +\frac{\pi}{6}$) as illustrated in Figure 5, and V_{im} is the amplitude of the input voltage, $\bar{v}_i = [v_A, v_B, v_C]$.

Table 3. Four "active configurations" selected for any combinations of k_i and k_v.

K_i \ K_v	**1**				**2**				**3**				**4**				**5**				**6**			
1	+9	-7	-3	+1	-6	+4	+9	-7	+3	-1	-6	+4	-9	+7	+3	-1	+6	-4	-9	+7	-3	+1	+6	-4
2	-8	+9	+2	-3	+5	-6	-8	+9	-2	+3	+5	-6	+8	-9	-2	+3	-5	+6	+8	-9	+2	-3	-5	+6
3	+7	-8	-1	+2	-4	+5	+7	-8	+1	-2	-4	+5	-7	+8	+1	-2	+4	-5	-7	+8	-1	+2	+4	-5
4	-9	+7	+3	-1	+6	-4	-9	+7	-3	+1	+6	-4	+9	-7	-3	+1	-6	+4	+9	-7	+3	-1	-6	+4
5	+8	-9	-2	+3	-5	+6	+8	-9	+2	-3	-5	+6	-8	+9	+2	-3	+5	-6	-8	+9	-2	+3	+5	-6
6	-7	+8	+1	-2	+4	-5	-7	+8	-1	+2	+4	-5	+7	-8	-1	+2	-4	+5	+7	-8	+1	-2	-4	+5
duty cycles	d_1	d_2	d_3	d_4	d_1	d_2	d_3	d_4	d_1	d_2	d_3	d_4	d_1	d_2	d_3	d_4	d_1	d_2	d_3	d_4	d_1	d_2	d_3	d_4
Number	I	II	III	IV	I	II	III	IV	I	II	III	IV	I	II	III	IV	I	II	III	IV	I	II	III	IV

As $(d_1+d_2+d_3+d_4) \leq 1$, for completing the sampling period T_s, one zero configuration or more (up to three) is applied. As the duty cycle of the zero configuration is d_0, to distribute it over the sampling period, it is divided into two or three depending on the number of the utilized zero vectors, and their position in the switching pattern. In the case of applying just one zero configuration, five switching configurations construct the 'switching pattern' for each sampling period T_s. The 'switching pattern' shows the order of the switching configurations and the number of zero configurations. Selecting the suitable zero configuration(s) and the distribution of the active configurations are very important to reduce the number of switchings in each sampling period that leads to a reduction in the switching losses and less harmonic distortion [51,52]. This order depends on the sectors k_i and k_v. If k_i+k_v is 'even', the order is III, I, II, IV, but if k_i+k_v is 'odd', it is I, III, IV, II. For example, if $k_i = k_v = 2$, the switching configurations, according to Table 3, are +5, −6, −8 and +9. It means that for a sampling period T_s the outputs X,Y,Z are connected to the inputs A,B, and C in five steps, as presented in Figure 6a.



(**a**) (**b**)

Figure 6. Connected switches in case of using, (**a**) one zero vector, and (**b**) three zero vectors.

Selecting the zero configuration 0_A and switching sequence as above for a sampling period T_s, minimizes the number of switchings as the shift from one switching configuration to the other one is performed by changing only one switch. Similarly, the switching sequence with three zero configurations can be shown in seven steps as illustrated in Figure 6b.

The switching pattern with three zero vectors presents less THD in the output current, although there is a negligible difference between THDs of the input source current [53]. Moreover, the number of the zero vectors does not have any effect on the input power factor.

The final switching table can be prepared considering the switching pattern, and all 36 switching sequences in Table 3, for even or odd values of k_i+k_v, as illustrated in Table 4 for $k_v=2$ and all six possible values of k_i. Table 4 can be completed for all 36 switching sequences. It should be noted that by taking advantage of the symmetries, 18 of the switching sequences presented in Tables 3 and 4 are repetitions of the other 18 states, which can reduce the coding. For example, when $k_v=2$ and $k_v=5$, the same active configurations and switching pattern are selected.

Table 4. Thirty-six possible switching sequences defined by the input and output hexagon sectors.

K_v	K_i	XYZ	XYZ	XYZ	XYZ	XYZ	XYZ	XYZ	k_i+k_v
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
2	1	CCC S_{XC},S_{YC},S_{ZC}	ACC S_{XA},S_{YC},S_{ZC}	AAC S_{XA},S_{YA},S_{ZC}	AAA S_{XA},S_{YA},S_{ZA}	AAB S_{XA},S_{YA},S_{ZB}	ABB S_{XA},S_{YB},S_{ZB}	BBB S_{XB},S_{YB},S_{ZB}	*odd*
	2	BBB S_{XB},S_{YB},S_{ZB}	BBC S_{XB},S_{YB},S_{ZC}	CBC S_{XC},S_{YB},S_{ZC}	CCC S_{XC},S_{YC},S_{ZC}	CAC S_{XC},S_{YA},S_{ZC}	AAC S_{XA},S_{YA},S_{ZC}	AAA S_{XA},S_{YA},S_{ZA}	*even*
	3	AAA S_{XA},S_{YA},S_{ZA}	ABA S_{XA},S_{YB},S_{ZA}	BBA S_{XB},S_{YB},S_{ZA}	BBB S_{XB},S_{YB},S_{ZB}	BBC S_{XB},S_{YB},S_{ZC}	CBC S_{XC},S_{YB},S_{ZC}	CCC S_{XC},S_{YC},S_{ZC}	*odd*
	4	CCC S_{XC},S_{YC},S_{ZC}	CCA S_{XC},S_{YC},S_{ZA}	ACA S_{XA},S_{YC},S_{ZA}	AAA S_{XA},S_{YA},S_{ZA}	ABA S_{XA},S_{YB},S_{ZA}	BBA S_{XB},S_{YB},S_{ZA}	BBB S_{XB},S_{YB},S_{ZB}	*even*
	5	BBB S_{XB},S_{YB},S_{ZB}	BCB S_{XB},S_{YC},S_{ZB}	CCB S_{XC},S_{Yc},S_{ZB}	CCC S_{XC},S_{YC},S_{ZC}	CCA S_{XC},S_{YC},S_{ZA}	ACA S_{XA},S_{YC},S_{ZA}	AAA S_{XA},S_{YA},S_{ZA}	*odd*
	6	AAA S_{XA},S_{YA},S_{ZA}	AAB S_{XA},S_{YA},S_{ZB}	BAB S_{XB},S_{YA},S_{ZB}	BBB S_{XB},S_{YB},S_{ZB}	BCB S_{XB},S_{YC},S_{ZB}	CCB S_{XC},S_{YC},S_{ZB}	CCC S_{XC},S_{YC},S_{ZC}	*even*
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
k_i+k_v: *even*		t_{01}	t_3	t_1	t_{02}	t_2	t_4	t_{03}	—
k_i+k_v: *odd*		t_{01}	t_1	t_3	t_{02}	t_4	t_2	t_{03}	—

In Section 3.4, the implementation method of the modulation process, and the sections that are included in the DSP and FPGA will be discussed in more detail.

2.3. Closed-Loop Output Current Control

As the SVM is considered as an open-loop control method, a closed-loop control based on the voltage oriented control (VOC) strategy is utilized to control the output current [54,55] as shown in Figure 7. The output currents are transformed into their equivalent *d-q* synchronous reference frame, and are compared to the reference values to determine the errors. The resultant errors then

are processed by the decoupled proportional-integral (PI) controllers to generate the three-phase output reference voltages ($\bar{v}_o^r$), which are finally transferred to the modulation process to obtain the switching signals. For the purpose of unity input PF, the *d-q* elements of the output reference current are selected as $i_{o(d)}^r = I_o^r$ and $i_{o(q)}^r = 0$, where I_o^r is the amplitude of the output reference current. Moreover, v_{oa}, v_{ob}, v_{oc} are the initial output reference voltages which determine the output frequency (ω_o) and the angle δ for the closed-loop control of the output current as shown in Figure 7.

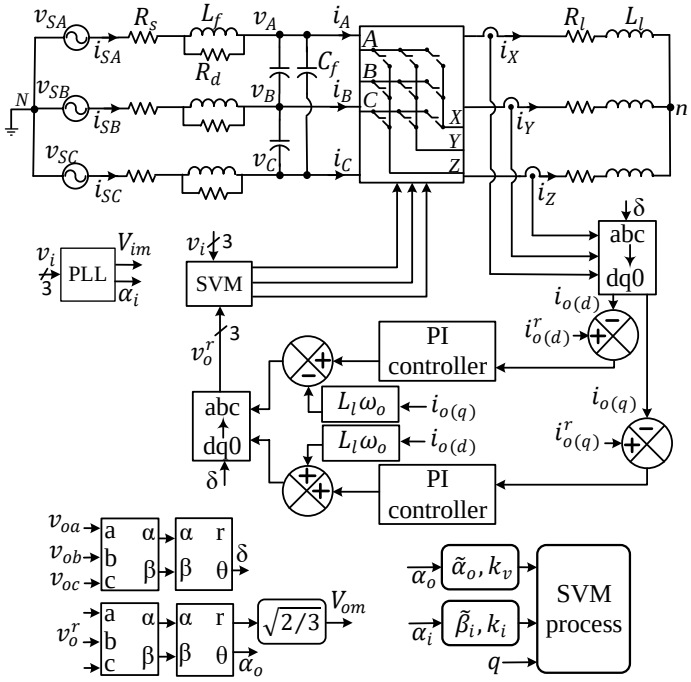


Figure 7. The control scheme of the DMC scheme with closed-loop control of the output current.

In order to tune the PI parameters, various combinations of the PI coefficients have been tested in the simulation, to achieve the optimum response with low overshoot, rise time, and settling time [56]. The PI controller can eliminate the steady-state error, although it has a negative impact on the overall stability of the system. When a large transient occurs at the input of the PI controller, which causes a large error, the integrator accumulates a non-zero error during the transients. This problem is referred to as integrator windup or integrator saturation. If the accumulated error is unwound, an overshoot happens, and the controller loses the ability to regulate the process and has no longer an impact on it. Therefore, the anti-windup PI controllers with the limiters can be utilized, as shown in Figure 8, which by selecting the appropriate upper and lower limits, reduces the overshoot at the step change time and help the system to remain stable [57,58].

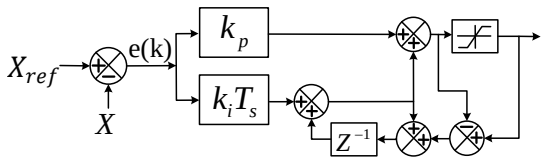


Figure 8. Anti-windup proportional-integral (PI) controller.

2.4. Safe Commutation Technique

All the existing switching devices have a non-ideal characteristic, and there is a delay in switching during turn-on and off. When two switches are changing their states at the same time, these delays

cause both of them to be 'on' or 'off' simultaneously, and as a result, a short- or open-circuit happens. To ensure the safe switching, a commutation strategy is required. The one-, two- and four-step commutations are the methods which are applied to the bidirectional switches. They can operate based on the output current direction or the input voltage polarity [8]. The commutation process is performed by a programmable logic device like FPGA which consists of programmable logic components and interconnections that can operate in parallel [59]. It allows the switching commutations of all three output legs of the MC to be performed simultaneously in parallel (not in turn which happens in the DSP).

The four-step commutation, which is used in the prototype, is one of the first commutation methods proposed based on the knowledge of the output current direction which flows through the conducted bidirectional switch. This knowledge is important as it defines which insulated-gate bipolar transistor (IGBT) carries the current and which one is idle. Therefore, the current direction determines the switching order. Current direction detection can be done by a hardware method using a non-inverting comparator with hysteresis at the current measurement and protection board. Moreover, it can be done by a software method using a comparator in the DSP. Current sensing using the existing sensors like Hall effect ones is difficult at very low current levels or when the current crossing the zero level while is distorted. In these situations the result of the current direction detection is inaccurate, and it can cause an open-circuit in the output path. The over-voltage caused by the output open-circuit can be handled by the clamp circuit and snubbers as it happens at very low currents.

Logic gates and the state machines designed for implementation of the 4-step commutation strategy can be programmed into the FPGA using a very high speed integrated circuit hardware description language (VHDL) code. Figure 9 illustrates a simple implementation of the soft-switching four-step commutation strategy for one output phase(X) (referring to Figure 10a) using synchronizing D flip-flops, that can be used instead of the state machines [60]. The clock frequency of the FPGA needs to be adjusted for a proper commutation, considering the turn-on and turn-off intervals of the IGBTs, and must be much lower than the sampling frequency [7]. The clock frequency of the Xilinx FPGA used in the prototype has been adjusted to 25 MHz which provides the commutation time of 40 ns. As can be seen from the timing diagram in Figure 11, a proper commutation has been carried out.

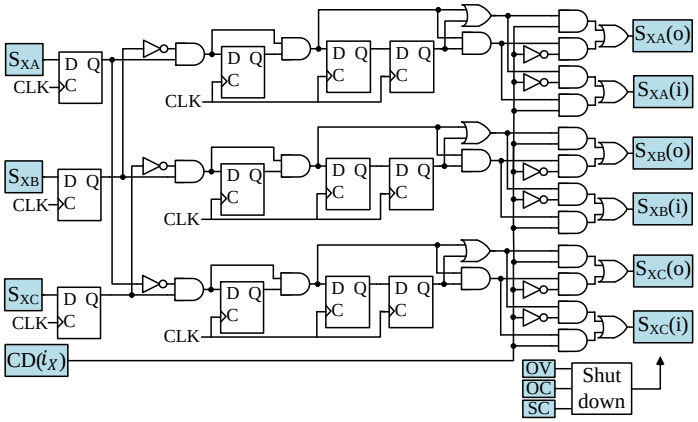
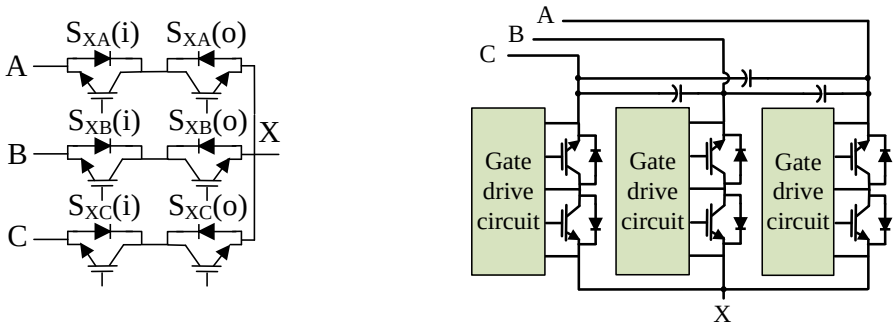


Figure 9. Schematic of the current direction based four-step commutation strategy for a three-phase to single-phase DMC using the logic elements [60].



(**a**) (**b**)

Figure 10. (**a**) Output leg X of the converter using bidirectional switches, and (**b**) the schematic of the power module with driver boards.

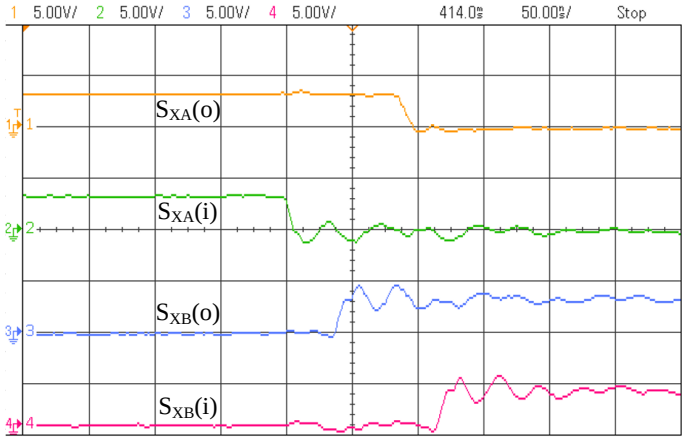


Figure 11. Experimental result of the four-step semi-soft commutation.

3. Hardware Development

This section provides a detailed discussion on the technical consideration and hardware design of the prototype matrix converter.

3.1. Switching and Drive Circuits

The schematic of the single-phase power module has been shown in Figure 10b (output leg X). The main parts of the power module of the DMC are the bidirectional switches which are based on the common-collector configuration of the IGBTs. The power circuit consists of three separated PCB boards on the three heat-sinks, each of which consists of six IGBTs (IRG7PH42UD1-EP) containing an antiparallel connected diode (rated current 30A and voltage 1200 V at 100 °C temperature), a snubber circuit for each switch, three on-board drivers (VLA567-01R) and three filter capacitors. Figure 12 shows the experimental setup of the DMC prototype.

In order to reduce the filter size, the filter capacitors can be placed in a delta connection. Moreover, for better decoupling of the converter from the input side and minimizing the effect of the parasitic inductances, each filter capacitor is split into three capacitors which are connected directly to the bidirectional switches on each board. Therefore, the total required capacitance is shared between all of the nine bidirectional switches in each leg. The input filter inductors with damping resistors are located between the input three-phase AC supply and the power boards as shown in Figure 12.

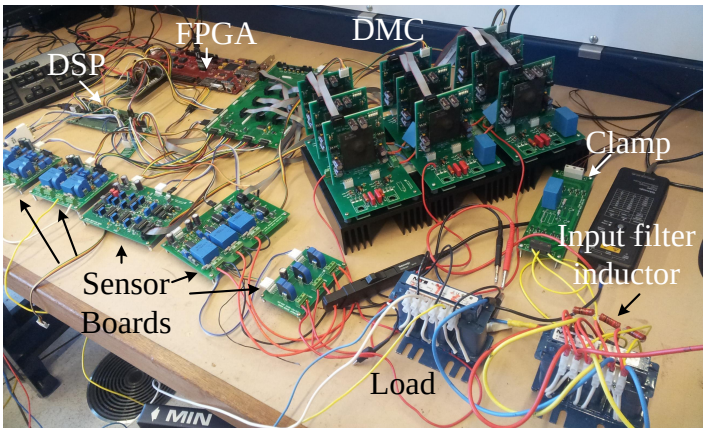


Figure 12. Experimental setup of the DMC prototype.

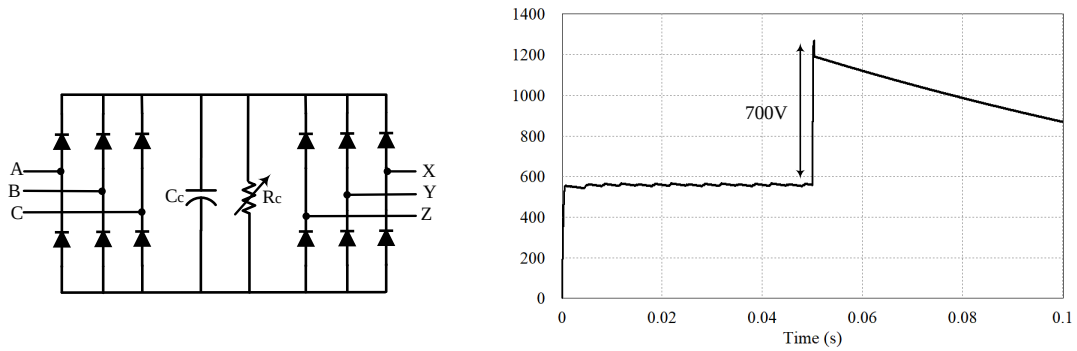
As the traditional electrolytic capacitors have a limited lifetime, they are replaced with film capacitors. It was possible to build the power module using a large multi-layered printed circuit board but separating them into three PCBs, each for one output phase is more convenient for maintenance. While a commutation method is applied for safe current commutation of the bidirectional switches, an *RC* snubber circuit is also connected across each bidirectional switch for more protection of the switches.

The driver board is designed to drive the IGBTs of the bidirectional switches on the power boards. The drive signals are applied to the switches through a hybrid integrated circuit (IC), VLA567-01R made by Powerx. Each IC can drive two IGBTs at the same time (one bidirectional switch), and because it has a built-in isolated dc-dc converter required for the gate drive, it can be used in both, the common-collector and common-emitter configurations of the bidirectional switches. The isolation voltage between the inputs, and between input and output is 2500 V-rms.

To protect the switches from failure under short circuit (SC) condition, the collector to emitter voltage should be monitored continuously. The driver IC includes a built-in short circuit protection that provides gate lockout to maintain a reverse bias for a predetermined time after the short circuit detection. The failure signals are sent to the FPGA, and a shutdown command is sent from the FPGA to the drivers. To achieve the minimum distance between the switches and gate drive signals, each gate driver board is directly plugged into the power board, on top of IGBT switches, as can be seen in Figures 1 and 12.

3.2. Clamp Circuit

A clamp circuit is a simple protection circuit which provides a freewheeling path to protect the converter against over-voltages caused by the forced shutdown of the converter or any other unpredictable disturbances. The circuit diagram of a simple clamp circuit connected to the input and output of the MC is shown in Figure 13a which includes two fast recovery diode bridges, a clamp capacitor C_c and a resistor R_c for discharging the capacitor. If any sudden shutdown happens to the converter for any reason, or one of the switches fails, or switches improperly due to the commutation problem, the current will be able to flow through the clamp circuit and the clamp capacitor. Moreover, elimination of the dc-link energy storage capacitor, causes the MC to be more sensitive and susceptible to disturbances and line perturbations. By this way, any voltage spike that occurs due to the energy stored in the inductors, can be stopped by the clamp capacitor that has been fully charged to the amplitude of the line voltage of the supply in normal operating conditions. The clamp circuit for the prototype is built on a separate PCB and connected to the input and output sides of the power boards to limit the over-voltage level on both supply and load sides.



(**a**) (**b**)

Figure 13. (**a**) Schematic of the clamp circuit, and (**b**) voltage across the clamp capacitor when a shutdown happens (v_s = 400 V line to line, and q = 0.86).

Under normal conditions, the clamp capacitor is charged to the maximum input line voltage. Under a faulty condition, when an error signal is generated by any protection circuits or the driver boards, the FPGA sends a shutdown command to the drivers to shutdown all the switches at the same time. At this instant, the voltage across the clamp capacitor steps up due to the energy stored in the inductors, and the clamp circuit is the way for discharging the load energy, as can be seen in Figure 13b. The clamp capacitor C_c can be calculated by [32]:

$$C_c = \frac{\frac{3}{2} L_l I_{om}^2}{V_{C_c,max}^2 - V_{im,ll}^2} \tag{7}$$

where L_l is the load inductance, I_{om} the amplitude of the output current, $V_{im,ll}$ the maximum input line voltage, and $V_{C_c,max}$ the maximum voltage across the clamp capacitor after charging by the stored energy of the load, which can be determined by:

$$V_{C_c,max} = V_{im,ll} \sqrt{\frac{\frac{1}{2}\frac{C_c}{L_l} + \frac{3}{4}(\frac{I_{om}}{V_{im,ll}})^2}{\frac{1}{2}\frac{C_c}{L_l}}} \tag{8}$$

As shown, for a given $I_{om}/V_{im,ll}$ ratio, a small C_c/L_l ratio would result in a large voltage surge.

3.3. Voltage and Current Measurements with the Protection Circuits

The sensor and protection boards include the current and voltage transducers, and over-voltage (OV) and over-current (OC) protection circuits. It is preferred to place the current sensors on a separate board from the protection circuits to increase the noise immunity.

According to the SVM strategy, the angle of the input current space vector (β_i) is required to determine the duty cycles and switching sequences. On the other hand, to reach the unity input power factor, the generated input currents must be synchronized with the input voltages. As a result, measuring the phase of the input voltage vector is enough for obtaining the phase of the input current ($\beta_i = \alpha_i$). For this purpose, three LEM voltage-transducers are utilized to measure the input phase voltages. Moreover, over-voltage (OV) fault signals are generated by a window comparator circuit for monitoring by the FPGA. Furthermore, three inline current transducers LEM, are used to measure the output currents. To ensure protection against over-current (OC), the output currents should be continuously monitored by a window comparator that generates OC fault signals to the FPGA.

The measured input voltage and output current sinusoidal waveforms are amplified, and level shifted to meet the required level for transfer to the DSP, and finally are limited by zener diodes with proper cut off voltages to clamp the outputs to the safe level for DSP. OC and OV signals can be

sent to the FPGA through the optocouplers, in order to provide the electrical isolation between the measurement circuit and the control platform, as well as the voltage level compatibility.

3.4. Matrix Converter Control Procedure

The control unit comprises a DSP board and an FPGA board. In this paper the simulation blocks are used for generating the *C* code for the DSP, and also the VHDL code for the FPGA. The C code can be generated using PSIM or MATLAB, but the VHDL code is generated by MATLAB software. The modulation calculations and control functions are performed by the DSP as the main processing unit. In this prototype, the TMS320F28335 Experimenter Kit manufactured by Texas Instruments is used as the central processor. In the following the control process is divided into two parts, the DSP and the FPGA parts.

A double-sided symmetrical switching pattern is selected for a better performance, which can include one zero configuration or more. Figure 14a illustrates the generation of the PWM pulses with three zero configurations, by comparing to a triangular waveform (a simplified C block with the duty cycles, k_v and k_i, and the triangular waveform as the inputs). As can be seen, in case of using three zero configurations, there are 12 switching state changes in each sampling period for all nine bidirectional switches. Therefore, the average switching frequency (f_{sw}: number of switchings per second) for nine bidirectional switches is $12/T_s$. This value is $10/T_s$ and $8/T_s$, for applying two or one zero configurations, respectively [51,53].

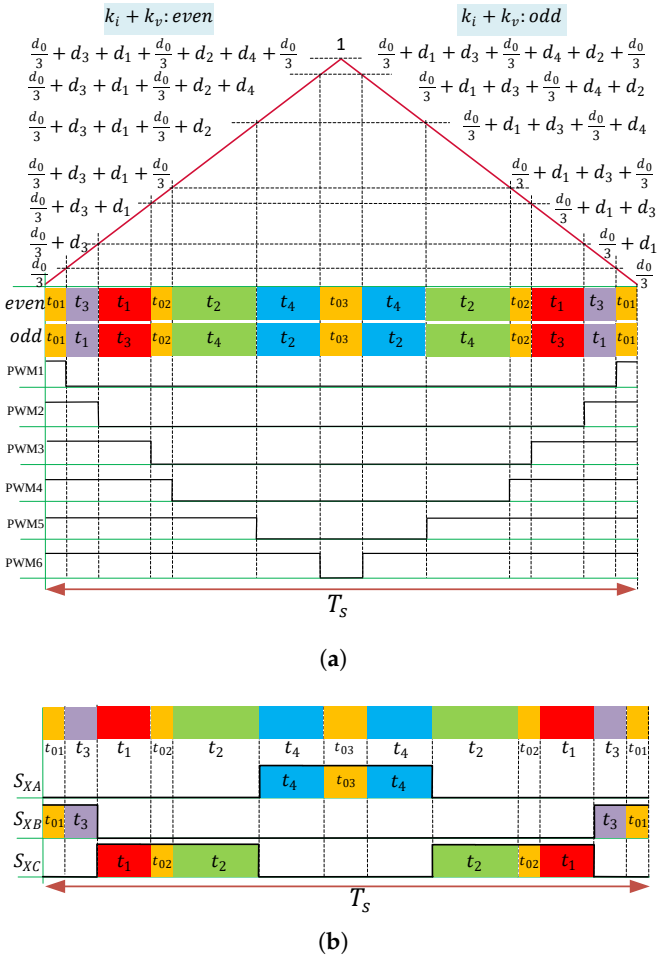


Figure 14. (**a**) Generation of double-sided symmetrical switching pattern with the application of 3 zero switching configurations, when $k_i + k_v$ is even or odd, and (**b**) generation of the switching signals using the time intervals of the switching configurations within a sampling period, for output leg X when $k_i = k_v = 2$.

As the goal of the control system is the unity input PF ($\varphi_i = 0$), the input current is kept in-phase with the input voltage ($\beta_i = \alpha_i$). Therefore, by measuring the input voltage, the angle of the input current vector (β_i) can be found. The DSP handles the following tasks:

1. Generating the output voltage reference when is required.
2. Determining the instantaneous amplitude and angle of the input source voltage and output reference voltage vectors to calculate the modulation index 'm', and the sector codes of k_i and k_v.
3. Calculating the duty cycles $d_0, ..., d_4$ by (6).
4. Generating the PWM pulses according to the switching pattern, as presented in Figure 14a.
5. Generating the current-direction code using a comparator.
6. Transferring the PWM signals, the sector codes of k_i and k_v, and current-direction code to the FPGA (one sampling-period delay of the PWM generators must be considered).

The generated PWM signals are sent to the FPGA, (the number of signals that depends on the switching pattern, number of the zero vectors and their location in the switching pattern, can be 4, 5 or 6 signals). In the FPGA, the modulation process is completed by generating nine switching signals from the received PWM signals of the DSP. The essential function of the FPGA is the commutation process and generating eighteen gate control signals for the bidirectional switches. An FPGA consists of programmable logic components and their interconnections. The architecture of FPGA is parallel; it means that different parts of the implemented control algorithm in an FPGA can be executed in parallel so that the execution time is very short [59]. Therefore, due to the fast computational capability of FPGAs, it is reasonable to put a part of the modulation algorithm as well as the commutation process in the FPGA to improve the performance of the control part and reduce the DSP load. On the other hand, the commutation process needs to be performed simultaneously and in parallel for the active switching devices.

The time intervals of the switching configurations within the sampling period can be determined in the FPGA as follows:

$$\begin{array}{ll} k_i+k_v: even & k_i+k_v: odd \\ t_{01} = PWM1 & t_{01} = PWM1 \\ t_3 = \overline{PWM1} \cdot PWM2 & t_1 = \overline{PWM1} \cdot PWM2 \\ t_1 = \overline{PWM2} \cdot PWM3 & t_3 = \overline{PWM2} \cdot PWM3 \\ t_{02} = \overline{PWM3} \cdot PWM4 & t_{02} = \overline{PWM3} \cdot PWM4 \\ t_2 = \overline{PWM4} \cdot PWM5 & t_4 = \overline{PWM4} \cdot PWM5 \\ t_4 = \overline{PWM5} \cdot PWM6 & t_2 = \overline{PWM5} \cdot PWM6 \\ t_{03} = \overline{PWM6} & t_{03} = \overline{PWM6} \end{array} \quad (9)$$

Finally, nine switching signals are generated using the time intervals of the switches referring to Table 4, as shown in Figure 14b for output X. For instance, when $k_i = k_v = 2$, the switching signals are:

$$\begin{array}{lll} S_{XA} = t_4 + t_{03} & S_{YA} = t_2 + t_4 + t_{03} & S_{ZA} = t_{03} \\ S_{XB} = t_{01} + t_3 & S_{YB} = t_{01} + t_3 + t_1 & S_{ZB} = t_{01} \\ S_{XC} = t_1 + t_{02} + t_2 & S_{YC} = t_{02} & S_{ZC} = t_3 + t_1 + t_{02} + t_2 + t_4 \end{array} \quad (10)$$

According to Figures 15 and 16, which illustrate the overall control structure of the converter, the FPGA board handles the following tasks:

1. Receiving the PWM signals, sector codes of k_i and k_v, and the current direction signals from the DSP, and generating the pulses that show the time intervals of the switching configurations within the sampling period ($t_0, ..., t_4$) using (9).

2. Generating all nine switching signals for any combination of k_i and k_v, using Table 4, and the example shown in (10).
3. Performing the current commutation process using the switching signals and current-direction code, and generating 18 switching pulses for the driver boards.
4. Turning off all the switches if there is any fault condition considering the over-voltage, over-current and short-circuit signals from protection circuits.

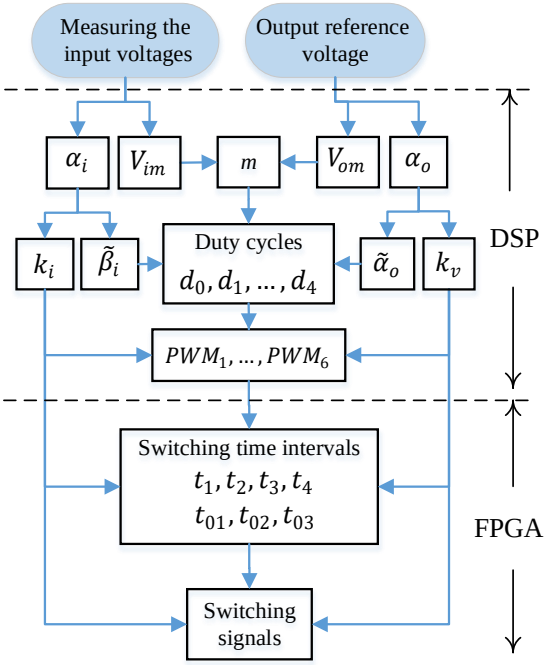


Figure 15. Flowchart of the space vector modulation (SVM) process for generating the switching signals.

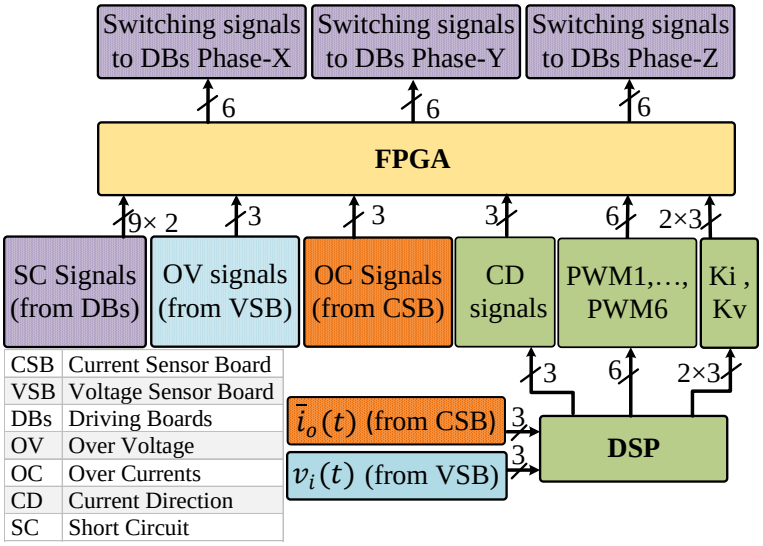


Figure 16. Overall structure of the control platform.

The final VHDL code includes four files. The VHDL code for generating the nine switching signals (can be generated by MATLAB software), as shown in Figure 15, and the VHDL code of the commutation process. The commutation circuit code can be generated by MATLAB or by the related software of the FPGA that is 'ISE Xilinx Design Tools'. A user constraints file (UCF) also is needed to

determine the utilized FPGA pins and applied clock frequency. Finally, a top-level file connects the three files together. Figure 17 illustrates the overall view of the VHDL code for the FPGA.

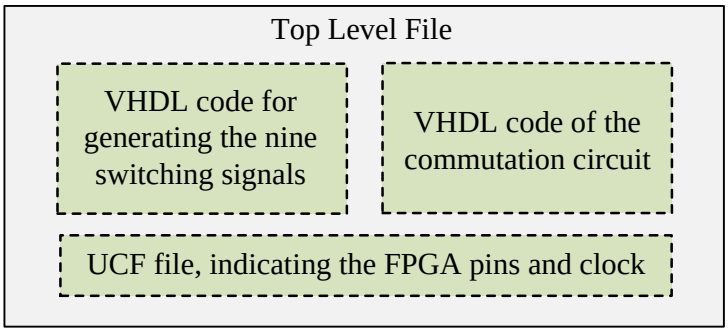


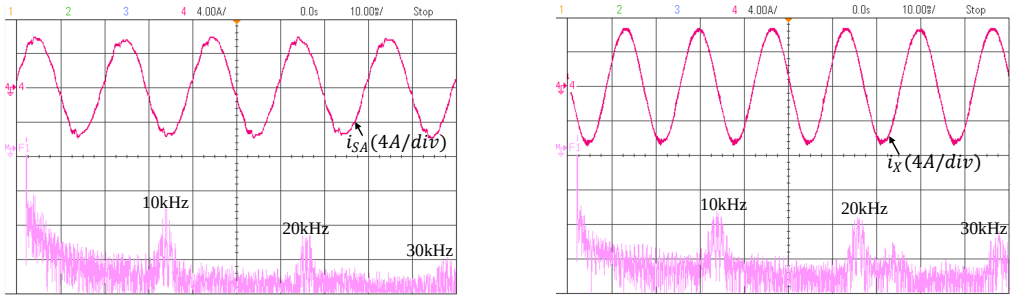
Figure 17. Generating the programming code of the field-programmable gate array (FPGA).

Some manipulation is needed to provide the simulation for generating the codes of the DSP and FPGA. At first ADC block must be added, and proper scaling factor should be applied to the input voltages and currents, (amplify and shift) using the functions to reach the original values. In purpose of generating the C code for the DSP using the simulation, the PWM generators are used, instead of comparing the duty cycles with a triangular waveform. As the PWM generators include one sampling period delay internally, k_v and k_i have to be delayed one sampling period before converting to the three-digit codes. As illustrated in the flowchart shown in Figure 15, the PWM pulses in addition to the k_i and k_v codes are sent to the FPGA from the DSP.

The output voltage level of the DSP is compatible with the FPGA, and both are 3.3 V, so the DSP output ports can be connected directly to the input connector of the FPGA without converting the logic level. However, the level conversion is necessary for connecting the outputs of the current and voltage protection boards (over-voltage and over-current signals), and the driver boards (short-circuit signals) to the FPGA, as their output voltages are 5 V. Furthermore, the FPGA output switching signals should be stepped up to 5 V before connecting to the driver boards. Wherever isolation is needed between the analog and digital circuits (to prevent affecting the control boards from high voltages), an optocoupler can be used for this purpose as well as the voltage level shifting. Moreover, dual-supply bus transceivers with configurable voltage translation ($SN74LVC16T245DLR$) can be used for bidirectional translation between 3.3 V and 5 V.

4. Experimental Results

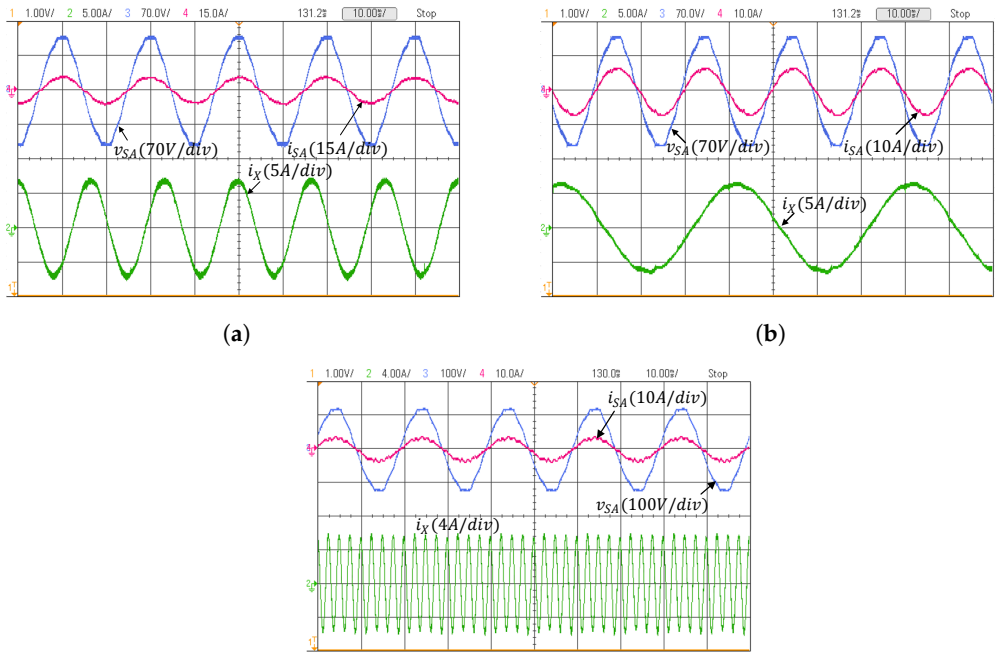
The performance of the designed MC and the proposed control technique for output current control and the stability method has been validated by using the prototype. The model of the DMC shown in Figure 7 with a three-phase Y-connected R-L load, has been tested, based on the specifications presented in Table 1. The experimental results have been displayed in the following figures. Figure 18a shows the input source current (i_{SA}) and its frequency spectrum, when the output reference current amplitude has been set on 7A-peak ($i^r_{o(d)} = I^r_o = 7$ and $i^r_{o(q)} = 0$). It can be seen that harmonics are introduced at integer multiples of the sampling frequency $f_s = 10kHz$ and their sidebands. The same results are obtained for the output current i_X and its spectrum, as shown in Figure 18b. THDs of the input and output currents are about 3.5% and 2.8% respectively.



(**a**) (**b**)

Figure 18. Experimental results of the direct space vector modulation (DSVM), (**a**) input source current with its frequency spectrum, and (**b**) output current with its frequency spectrum.

Figure 19a presents the input source current and voltage, and the output current for output frequency of 60 Hz. As can be seen, the input current and voltage are in phase, and the input PF is about 0.98. The test has been carried out for output frequency of 25 Hz and 400 Hz in order to show the converter performance for output frequency less than the input frequency and much more than it, and the results have been displayed in Figure 19b,c. Moreover, Figure 20 shows the dynamic response to a step change of the load current. The output reference current steps up from 4A-peak to 8A with 25 Hz frequency. As can be seen, output current regulation has been met with proper reference tracking and dynamic responses. Furthermore, the overvoltage at the transient time has been damped perfectly. The same results are achieved in Figure 21 when the output reference current steps down with 60 Hz frequency, which along with Figure 20 shows stability of the system for different conditions and frequencies. The output line voltage (v_{XZ}), and the output phase voltage with respect to the output neutral point (v_{Xn}) have been shown in Figure 22. In all experimental tests the system presents a stable performance, as the stabilization has been established using 20 Ω damping resistors. Instability of the system has been shown in Figure 23 when non of the stabilization techniques are applied, and as a result the source current is distorted.



(**a**) (**b**)

(**c**)

Figure 19. Experimental results of the DSVM, input source current and phase voltage, with the output current when, (**a**) f_o = 60 HZ, (**b**) f_o = 25 HZ, and (**c**) f_o = 400 Hz.

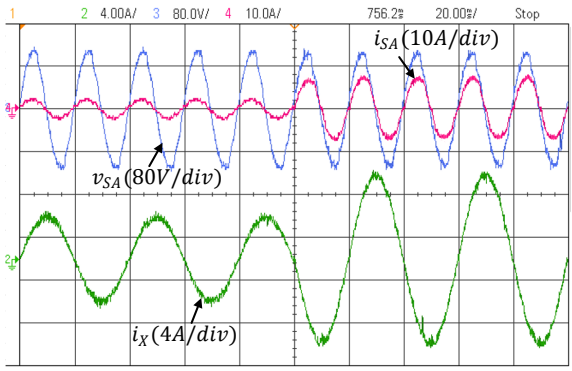


Figure 20. Experimental results of the DSVM, input source current and phase voltage, with the output current, when the output reference current steps up from $4A$ to $8A$ with 25 Hz frequency.

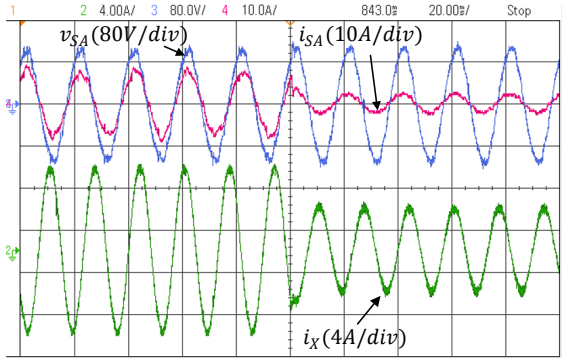
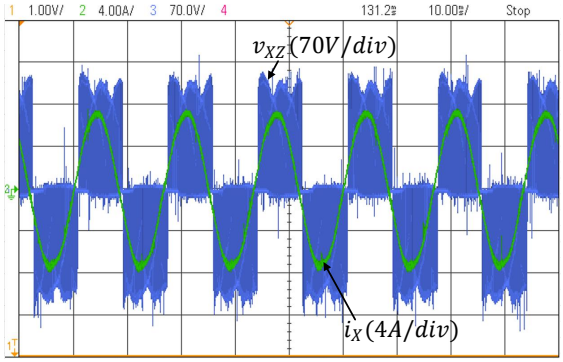
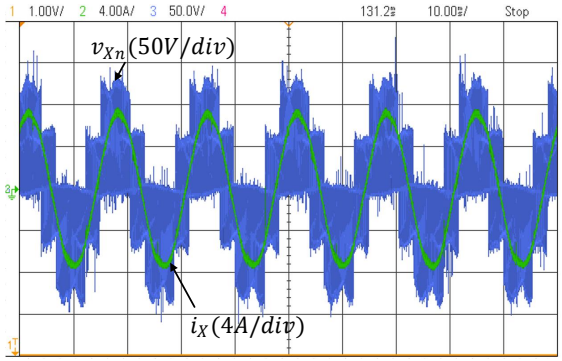


Figure 21. Experimental results of the DSVM, input source current and phase voltage, with the output current, when the output reference current steps down from $8A$ to $4A$ with 60 Hz frequency.



(**a**)



(**b**)

Figure 22. Experimental results of the DSVM, (**a**) Output line voltage and current, and (**b**) Output phase voltage with respect to the output neutral point, with the output current.

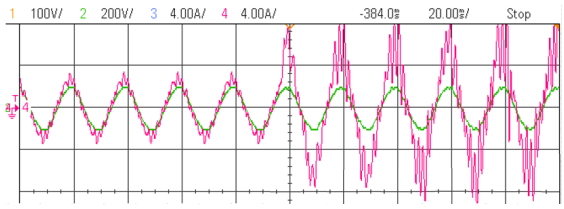


Figure 23. Experimental results of the input current without applying any stabilization technique.

5. Conclusions

Technical considerations of design and implementation of a DMC using the SVM modulation technique and the closed-loop power flow control method has been presented in this paper. The converter was stabilized by the damping resistor method, and the stability region was determined using the linearized state-space equations. The damping resistance is selected as 20 Ω based on the practical considerations. It was seen, although a lower damping resistance can yield a wider stability region and higher voltage gain, it generates a higher power loss. The technical points of the input filter design, safe commutation and protection methods, and realization of SVM and control system using DSP and FPGA were also presented. The designed MC was tested using a Y-connected R-L load, under different conditions including various amplitudes of the output reference current and different output frequencies. The experimental test results show that the proposed control method can generate sinusoidal input and output currents with low harmonic distortions (THD < 5%) for a wide range of output frequencies. Therefore, the designed matrix converter with the proposed control method can be used as an interface between a variable-frequency load and an AC microgrid.

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