A Broadband Doherty Power Amplifier With Hybrid Class-EFJ Mode

Zhiwei Zhang, Zhiqun Cheng, Hang Li, Huajie Ke, and Y. Jay Guo, *Fellow, IEEE*

***Abstract*—This paper proposes a method that employs novel hybrid continuous class-EFJ power amplifiers (PAs) as carrier PA to design a broadband high-efficiency Doherty power amplifier (DPA). Bandwidth characteristic of the proposed DPA is analyzed in detail. By proper selection of related parameter values, up to 78% fabrication bandwidth can be obtained. Post-harmonic tuning network is applied to improve the bandwidth and enhance the efficiency. Then, a closed design process is presented to design broadband DPA based on derived theories. For validation, a broadband DPA operating in 1.2-2.8 GHz is designed and fabricated. Measurements illustrate that the DPA can deliver saturated output power between 43.7 dBm and 44.1 dBm in 1.2-2.8 GHz, and the saturated drain efficiency from 60.5% to 74.2 % is achieved. Moreover, drain efficiency is 48.1%-57.6% at the 6 dB power back-off. Compared with conventional DPAs, the proposed DPA exhibits superior performance of bandwidth characteristics and power back-off efficiency over a wide bandwidth.**

***Index Terms*—Broadband, Class EFJ, Doherty power amplifier, high-efficiency.**

I. Introduction

With the rapid development of the wireless communication, the amount of information transmission is increased remarkably. In order to meet such data growth, signals with large bandwidth and high peak-to-average power ratio (PAPR) are generally used [1], [2]. In order to satisfy such requirements, the power amplifier (PA) has to be developed to amplify such signals. It means that PAs should have the ability to improve the efficiency at the output back-off (OBO) level in a large bandwidth. Some amplifier architectures have been proposed to amplify signals with high PAPR, such as Doherty [3], out-phasing [4], envelope tracking [5], and envelope elimination and restoration. Due to the simple structure and low cost, Doherty PAs (DPAs) are widely used in practical base stations. However, conventional DPAs have some inherent disadvantages, e.g., narrow bandwidth and only 6 dB OBO range [6], [7], which still deserve further research for improvement.

There are several factors that hinder DPAs broadband, including λ/4 transmission line, offset line, output matching networks (OMNs) and package parasitic parameters of devices [8]-[11]. For these limitations, some solutions have been proposed to increase the bandwidth of DPAs [12]-[19]. In [12] and [13], integrated compensating reactance is used in the peaking amplifier output to improve the back-off efficiency in a large bandwidth. Post-matching topology is presented to reduce the impedance transformation ratio [14]-[17]. Symmetrical DPAs with complex load impedances is demonstrated to obtain better load modulation in a wide bandwidth [18], [19]. In order to extend the OBO range, many methods have also been proposed [20]-[22]. In [20] and [21], the multiway is applied to extend OBO through using multiple peaking PA branches. The asymmetrical topology is used to make peak PA with larger saturated current than carrier PA, thus, increasing OBO [22]. All the above methods leverage the traditional class AB PAs as carrier PAs.

Recently, extended high efficiency operation modes PAs are exploited as carrier PAs to design broadband high-efficiency DPAs [23]-[25]. Although the bandwidth of DPAs is widened, the real part of the fundamental load impedance would decrease with frequency deviation from the center point [23]. As a result, the OBO drain efficiency would decline at both lower and higher operating frequency points. In [24] and [25], the carrier amplifier operates in continuous class-J at the OBO level, which can provide a fixed real part of the fundamental load impedance to maintain high-efficiency in a large bandwidth. Impedance conversion is needed to obtain fixed real part of the fundamental load impedance, while the required impedance conversion leads to the increase in the complexity of design.

A class-EFJ PA has been proposed in our previous work [26], which can effectively combine high-efficiency of class-EF PAs with large bandwidth of continuous class-J PAs at specific conditions, thereby being suitable for wideband and high efficiency purposes. The load impedance of class-EFJ PAs not only has variable imaginary part like the conventional continuous PAs, but also has inconsistent real part. Thus, such load impedance characteristics of class-EFJ PAs are highly applicable to DPAs' load modulation applications. In other words, the impedance conversion used in [24] and [25] to maintain fixed resistance can be negligible due to the load impedance characteristics of class-EFJ PAs.

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In this paper, we study continuous class-EFJ PAs in the DPAs' architecture to simplify the design process with larger bandwidth. The class-EFJ PA is used as the carrier PA of DPA. With the load impedance characteristics of the continuous class-EFJ PAs, the impedance conversion used in continuous modes DPAs to maintain fixed resistance can be simplified. The design parameters and bandwidth characteristics are derived in detail for DPAs. Up to 78% fabrication bandwidth can be obtained when class-EFJ PA is exploited as the carrier PA. Furthermore, a closed design process is presented for broadband high efficiency DPAs with the continuous class-EFJ PAs, which greatly enhances the drain efficiency at the OBO level. A high efficiency DPA with 78% fabrication bandwidth is designed and fabricated. Compared with traditional DPAs, the proposed DPA effectively enhances fabrication bandwidth, over which the drain efficiency at the OBO level is close to that of state-of-the-art.

The structure of this paper is as follows. The theories of conventional DPAs are analyzed in Section II. Then, the theories of the proposed DPA applying continuous EFJ are derived in Section III. The closed design method and process of the broadband high-efficiency DPA are detailed in Section IV. In Section V, simulations and measurements are given to demonstrate the performance of the proposed one, before concluding the paper in Section VI.

II. Analysis of DPAs Theories

The traditional DPA includes a carrier PA branch and a peak PA branch. At the combiner, there is a load of $R_L/2$. A transistor can be equivalent to an ideal current source. The equivalent traditional DPA topology is shown in Fig. 1(a). There is an impedance converter line in the carrier PA branch as shown in Fig. 1(a) [3]. Z_C, Z_P are the load impedances of devices for carrier and peak PAs, respectively. According to the principle of load modulation, several impedances are as follows:

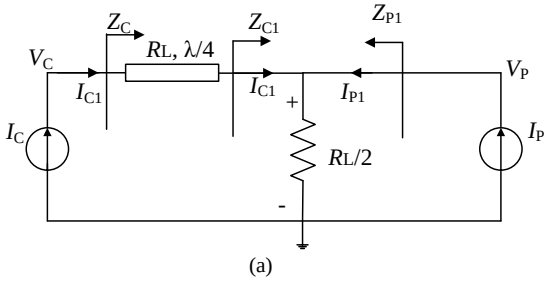
$$Z_{C1,SAT} = (1+\beta)\cdot R_L \quad (1)$$

$$Z_{C1,BACK} = R_L \quad (2)$$

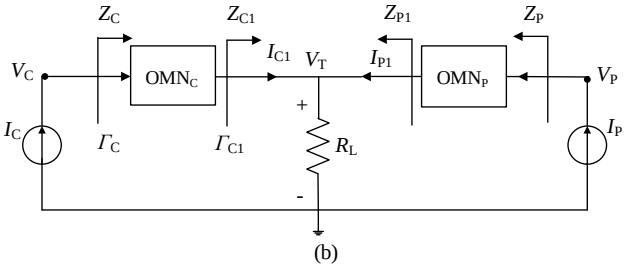
$$Z_{P1,SAT} = (1+1/\beta)\cdot R_L \quad (3)$$

$$Z_{P1,BACK} = \infty \quad , \quad (4)$$

where $Z_{C1,SAT}$ and $Z_{C1,BACK}$ refer to Z_{C1} at the saturation and power back-off levels, respectively. Similarly, $Z_{P1,SAT}$ and $Z_{P1,BACK}$ refer to Z_{P1} at the saturation and power back-off levels, respectively. Z_{C1} and Z_{P1} are the load impedances of carrier and peak PAs, respectively. Similarly, Z_C and Z_P represent the load impedances of carrier and peak PA transistors, respectively. β represents the current ratio of peak PA branch to carrier PA branch at the saturation level.



(a)



(b)

Fig. 1. DPA topology (a) Conventional DPA topology (b) Replaced topology.

Fig. 1(b) shows a more generalized topology of DPAs, where DPAs include a carrier PA branch and a peak PA branch [25]. OMN$_C$ and OMN$_P$ refer to output matching networks OMNs in the carrier PA branch and peak PA branch, respectively. At the combiner, there is a load of R_L.

Assuming that OMN$_C$ is a lossless network structure, its generalized scatter parameters can be expressed as

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} 0 & e^{j\theta_C} \\ e^{j\theta_C} & 0 \end{bmatrix}, \quad (5)$$

where θ_C represents the phase delay of the network. Generally, θ_C depends on the working frequency, and changes in linear and periodical with frequency. Here, we assume that one period is from -π to π. Hence, during one period, θ_C decreases from π to -π as the operating frequency increases. The traditional DPAs topology shown in Fig. 1(a) is consistent with the topology shown in Fig. 1(b) when θ_C is equal to π/4.

As shown in Fig. 1, Γ_{C1} is the reflection coefficient seen from OMN$_C$ to the carrier PA load Z_{C1}, and Γ_C is the reflection coefficient seen from carrier device into OMN$_C$. Then, we have

$$\Gamma_C = S_{11} + \frac{S_{12}\cdot S_{21}\cdot \Gamma_{C1}}{1 - S_{21}\cdot \Gamma_{C1}} \quad . \quad (6)$$

Substituting (5) into (6), we can rewrite (6) as

$$\Gamma_C = \Gamma_{C1}\cdot e^{j2\theta_C} \quad (7)$$

$$\Gamma_{C1} = \frac{Z_{C1} - (1+\beta)\cdot R_L}{Z_{C1} + (1+\beta)\cdot R_L} \quad . \quad (8)$$

At the saturation, combining (1), (7) and (8) can obtain

$$\Gamma_{C,SAT} = \Gamma_{C1,SAT} = 0 \quad , \quad (9)$$

where $\Gamma_{C1,SAT}$ and $\Gamma_{C,SAT}$ represent Γ_{C1} and Γ_C at the saturation power level, respectively. Equation (9) shows that the load impedance of the carrier transistor Z_C remains at R_{opt} over the entire operating frequency band.

At the OBO level, the load impedance of carrier PA, $Z_{C1,BACK}$ becomes R_L. Then, (8) can be calculated as

$$\Gamma_{C1,BACK} = \frac{R_L - (1+\beta)\cdot R_L}{R_L + (1+\beta)\cdot R_L} = -\frac{\beta}{2+\beta} \quad , \quad (10)$$

where $\Gamma_{C1,BACK}$ refers to Γ_{C1} at the OBO power level.

Combining (5), (6) and (10), the reflection coefficient, $\Gamma_{C,BACK}$, at the OBO power level can be derived as

$$\Gamma_{C,BACK} = \Gamma_{C1,BACK}\cdot e^{j2\theta_C} = -\frac{\beta}{2+\beta}\cdot e^{j2\theta_C} \quad . \quad (11)$$

Equation (11) reveals that when PA operating at the back-off power level, the load impedance of the carrier PA, $Z_{C,BACK}$ is not a constant but closely related to θ_C. The θ_C depends on the working frequency. It is obvious that $Z_{C,BACK}$ locates on the equal reflection. Specifically, β equals 1 for a symmetrical DPA. Then, it can be plotted in smith chart shown in Fig. 2.

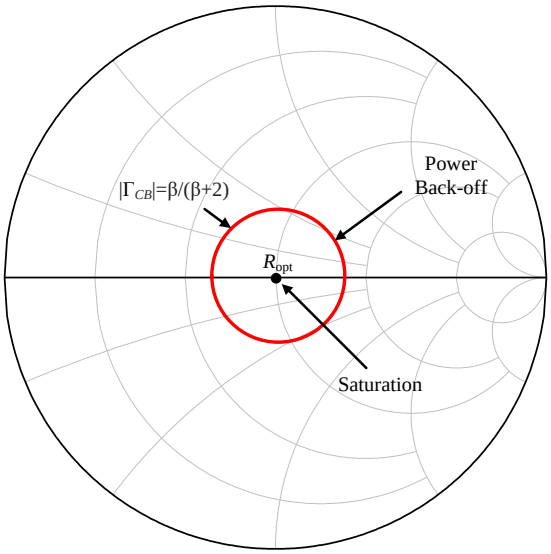


Fig. 2. The reflection coefficient Γ_C versus frequency.

As shown in Fig. 2, the load impedance of carrier transistor lies on a circle of constant reflection coefficient, which changes with the operating frequency at the OBO stage. Nevertheless, the load impedance of carrier PA is a constant (R_{opt}) in saturation, which shows that it is difficult to design a PA to satisfy the two impedance conditions at the same time. In next section, we will introduce a PA of which impedance is suitable for the impedance condition of carrier amplifier at the OBO stage.

III. Theory Analysis of The Proposed DPA

As discussed in Section II, the impedance condition of carrier PA prevents the realization of broadband DPAs. In this section, continuous class-EFJ PA is introduced to the DPA as its carrier PA. The analysis on Doherty with continuous class-EFJ PA in this paper is based on the ideal peak power amplifier branch. The fundamental impedance Z_{f0} of continuous class-EFJ PAs can be obtained from [26]

$$Z_{f_0} = (1 + \gamma j) * R^*, \tag{12}$$

where γ is a coefficient taking a value from -1 to 1. R^* is the load impedance. The available value range of R^* is located in between 15.89 Ω and 46.29 Ω for the CGH40010F GaN transistor.

Compared with the traditional continuous mode class-J PA, the impedance space of class-EFJ has better flexibility, that is R_{OPT} in class-J is a fixed value, and R^* in class-EFJ is an impedance space. In practical design, the appropriate value can be chosen according to different needs.

As discussed in the Section II, the load impedance of carrier PA at the OBO level is located as a constant reflection coefficient circle shown in Fig. 3. For comparison, the impedance of the continuous class-EFJ is also shown in Fig. 3. In this way, the overlapping area between the equal reflection coefficient circle and the available load impedance of the class-EFJ can be clearly displayed. Seen from Fig. 3, the load impedance of class-J has only an intersection with the circle of constant reflection coefficient. This indicates that impedance conversion has to be adopted to keep the load impedance Z_C a fixed value. For class-EFJ, the situation is very different. The impedance of the continuous class-EFJ covers almost the entire iso-reflection circle. Therefore, the carrier amplifier working in the continuous class-EFJ can be more easily implemented, which simplifies the impedance process, comparing with the continuous class-J previously reported in [24]. Moreover, it can expand Doherty's bandwidth due to the extensive impedance overlap between class-EFJ and equal reflection coefficient circles.

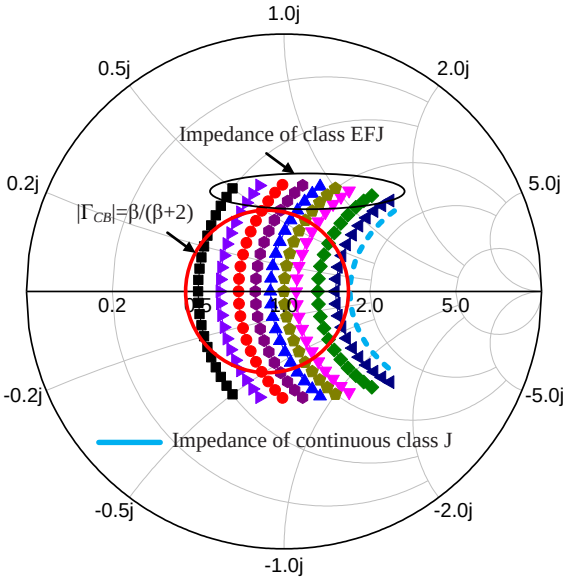


Fig. 3. Impedance of class-EFJ and continuous mode class-J.

We define the reflection coefficient corresponding to the load impedance of the continuous class-EFJ, Γ_{EFJ}, as

$$\Gamma_{EFJ} = \frac{Z_{EFJ} - R_{opt}}{Z_{EFJ} + R_{opt}}. \tag{13}$$

Setting the condition of carrier PA to be class-EFJ at the OBO level, we have

$$\Gamma_{\mathrm{EFJ}} = \Gamma_{\mathrm{C,BACK}}, \tag{14}$$

which can be rewritten as

$$\left|\Gamma_{\mathrm{C,BACK}}\right| = \left|\Gamma_{\mathrm{EFJ}}\right| \tag{15}$$

$$\left|\theta_{\mathrm{C,BACK}}\right| = \left|\theta_{\mathrm{EFJ}}\right|, \tag{16}$$

where $\theta_{\mathrm{C,BACK}}$ and θ_{EFJ} represent the phase of $\Gamma_{\mathrm{C,BACK}}$ and Γ_{EFJ}, respectively.

Substituting (11)-(13) to (15) and (16), we have

$$\left(\frac{\beta}{2+\beta}\right)^2 = \frac{R^{*2} - R_{opt}^2 + \gamma^2 \cdot R^{*2}}{\left(R^* + R_{opt}\right)^2 + \gamma^2 \cdot R^{*2}} \tag{17}$$

$$\tan 2\theta = \frac{2\gamma R^* R_{opt}}{R^{*2} - R_{opt}^2 + \gamma^2 \cdot R^{*2}}, \tag{18}$$

where

$$\theta = \frac{\pi}{2}\frac{f}{f_0}. \tag{19}$$

Combing (18) and (19), fractional bandwidth versus γ and R^* can be plotted in Fig. 4.

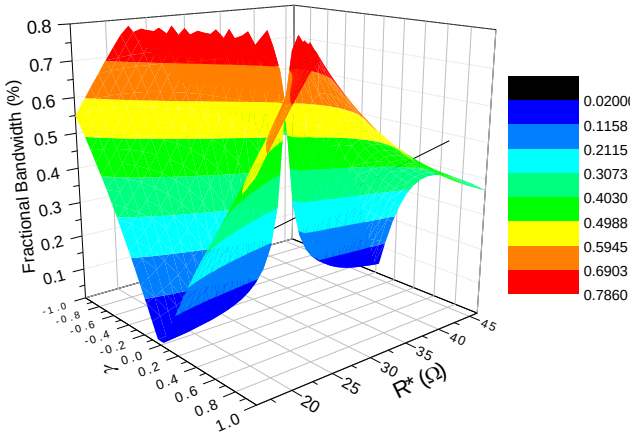


Fig. 4. Fractional bandwidth versus γ and R^*.

From Fig. 4, different combinations of parameter values can be obtained for different relative bandwidths. In practical design, the optimal value can be chosen according to different needs. For example, when γ and R^* are set to -0.74 and 25 Ω respectively, the maximum relative bandwidth is about 78%.

Similarly, the relationship between current ration β, γ and R^* can be plotted in Fig. 5 by using (17). As shown in Fig. 5, the current ratio β can be determined by γ and R^* got from Fig. 4. For example, when γ is -0.74 and R^* is 25 Ω, with maximum relative bandwidth of 78%, the current ration β should be set as 1.16. Also, the current ratio β has an influence on the relative bandwidth of DPAs, because different β requires different γ and R^*. At the same time, the relative bandwidth is determined by different γ and R^*.

Particularly when γ, R^* and β are fixed to be ±0.74, 25 Ω and 1.16 respectively, the bandwidth characteristics of DPAs at the OBO level are displayed in Fig. 6. It indicates that the proposed DPA can maintain high drain efficiency over a wider frequency band, compared with traditional DPAs [19]. It illustrates that the application of class-EFJ PA effectively improves the bandwidth characteristics of traditional DPAs. Next, in order to design the broadband high efficiency DPA using EFJ PAs, we derive the ABCD transmission matrix of the $(OMN)_C$ and $(OMN)_P$.

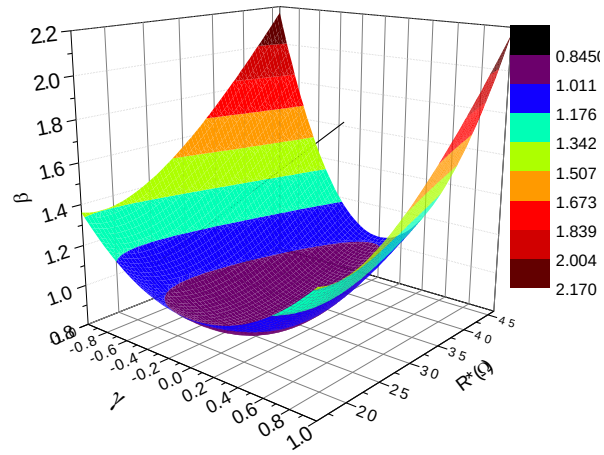


Fig. 5. Current ration β versus γ and R^*.

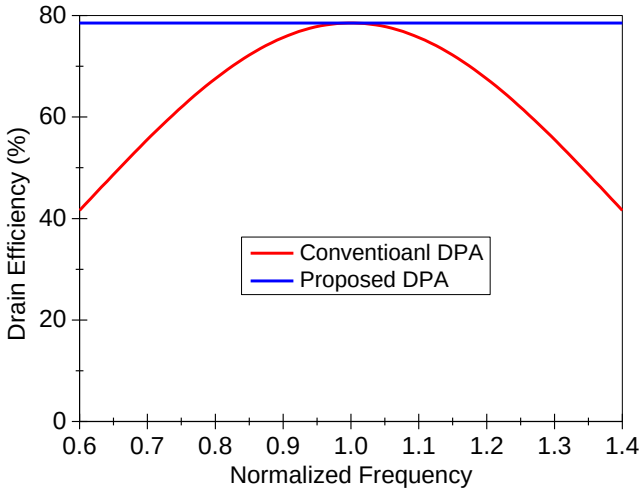


Fig. 6. Drain efficiency of the presented DPA and traditional DPA in normalized frequency of 0.6-1.4 at the OBO stage.

Fig. 7 displays impedance transformation of the DPA at the different power levels. The load impedance at the combiner Z_L is defined as $R_L{\cdot}(1+jX_L)$, where X_L refers to the normalized reactance of the R_L and is given by [27]

$$X_L = \mp\sqrt{(\alpha_1 - 2)(2\alpha_1 - 1)/\alpha_1}, \quad (20)$$

where α_1 is a coefficient. In this paper, as the load impedance of carrier PA is Z_{EFJ} rather than Z_{OPT}, α_1 is defined as

$$\alpha_1 = \frac{\alpha R_{OPT}}{R^*}, \quad (21)$$

where α represents the ratio of load impedance for carrier PA at the OBO stage to that at the saturation level.

Then, the OBO range can be derived by

$$OBO = 10\log(1+\beta)\cdot\alpha \quad . \quad (22)$$

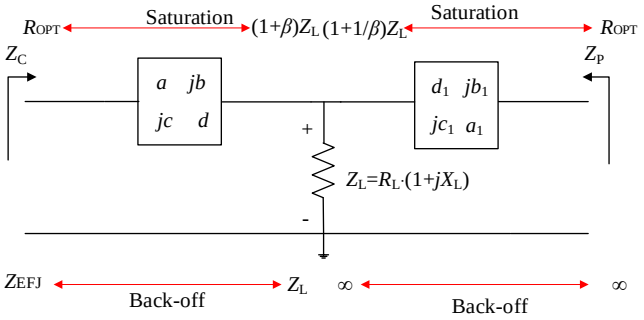


Fig. 7. Impedance conversion of the proposed DPA.

As shown in Fig. 7, in saturation, the impedance at the combiner seen from carrier branch is $(1+\beta)Z_L$, and the load impedance Z_C is R_{OPT}. The $(1+\beta)Z_L$ is transformed to R_{OPT} by using the OMN_C. Similarly, at the OBO stage, the impedance at the combiner seen from carrier branch is Z_L, and the load impedance Z_C is Z_{EFJ}. The Z_L is also transformed to Z_{EFJ} by using the OMN_C. It is noted that regardless of R_{OPT} at the saturation stage or Z_{EFJ} at the OBO stage, it always falls within the impedance range of the class-EFJ PAs. This reduces the impact of impedance variation of the designed OMN_C on the performance of the DPA due to frequency offset. Regarding the peak PA branch, the impedance at the combiner seen from peak branch is $(1+1/\beta)Z_L$, and the load impedance Z_P of peak transistor is R_{OPT} in saturation. The $(1+1/\beta)Z_L$ is transformed to

R_{OPT} by using the OMN_P. At the OBO level, the peak transistor is off, since the impedance Z_P is infinite. Accordingly, the impedance at the combiner seen from peak brand is also infinite. This impedance conversion is also achieved by using the OMN_P.

Based on the impedance conversion in Fig. 7, the parameters of OMN_C and OMN_P can be derived as

$$a = -R_{OPT}\left(\frac{\alpha}{\alpha_1}(1+\gamma)-2\right)c/((1+\beta)X_L/2) \quad (23)$$

$$b = R_{OPT}(1+\beta)R_L((\alpha/\alpha_1)(1+\gamma)-1)c \quad (24)$$

$$c = \sqrt{\frac{(2(\alpha/\alpha_1)(1+\gamma)-1)}{[R_{OPT}(1+\beta)R_L((\alpha/\alpha_1)(1+\gamma)-1)((\alpha/\alpha_1)(1+\gamma)+1)]}} \quad (25)$$

$$d = \frac{R_{OPT}c(1+\beta)X_L\left(\left(\frac{\alpha}{\alpha_1}\right)(1+\gamma)-1\right)}{\left(2\left(\frac{\alpha}{\alpha_1}\right)(1+\gamma)-1\right)} \quad (26)$$

$$a_1 = \sqrt{\frac{R_{OPT}}{(1+1/\beta)R_L}} \quad (27)$$

$$b_1 = -\sqrt{\left(1+\frac{1}{\beta}\right)R_L R_{OPT}}\left(1+\frac{1}{\beta}\right)X_L/2 \quad (28)$$

$$c_1 = 0 \quad (29)$$

$$d_1 = \sqrt{(1+1/\beta)R_L/R_{OPT}} \quad . \quad (30)$$

Using (23)-(30), the output networks parameters can be obtained and designed.

IV. Design of The Proposed DPA

In the following, a closed process is presented to design a DPA with working frequencies of 1.2-2.8 GHz based on the theories of Section III. To validate the presented means, a broadband high-efficiency DPA employing CGH40010F transistors is elaborated on Rogers R4350B substrate. The drain voltage V_{ds} is 28 V. The gate voltages V_{gs} for the carrier PA and the peak PA are -2.8 V and -6.0 V, respectively. The optimum load impedance R_{OPT} is determined as 32 Ω for the CGH40010F considering V_{knee}. To obtain the optimized load impedance Z_{OPT} in the package plane, load-pull simulation is processed using the ADS software for deriving package parameters. From [20], the package parameters of CGH40010F can be obtained as shown in Fig. 8, which will be used in practical design process.

A. Output Matching Network

The design process of output network can be performed as follows. The OBO and desired bandwidth are determined firstly, where a 6 dB OBO and maximum relative bandwidth of 78% are chosen. Then, the coefficient γ, current ratio β and R^* are given by ±0.74, 1.16 and 25 Ω from Fig. 4 and 5, respectively. It is calculated that α, α_1 and X_L are 1.85, 2.37 and 0.76 using (20)-(22), respectively. The load impedance at the combine node, Z_L, is fixed to be 15•(1±j 0.76) Ω. The general transistor CGH40010F is used in this work. The ABCD transfer matrix of OMN_C and OMN_P can be derived using (23)-(30). The designed OMN_C and OMN_P are shown in Fig. 8(a) by using network synthesis and optimization. Also, package parasitic parameters are absorbed in the output matching networks during optimizing the output matching circuits. In the analysis of Section III, the peak PA is assumed to be ideal. Of course, the actual peak PA may not be ideal. It may reduce the performance of Doherty. For Doherty PAs, the efficiency at the power back-off is more important. Especially at the power back-off, if the peak PA branch is not completely open, the power of the carrier PA would leak to the peak PA branch, resulting in reduced efficiency at the power back-off. Therefore, when optimizing the output network of the peak PA, the first thing is to ensure that the peak PA is in an open-circuit state at the power back-off. The simulated S11 of the designed OMN_C and OMN_P are shown in Fig. 8(b). It can be seen that the S11 of OMN_C and OMN_P is lower than -10 dB in 1.2-2.8 GHz, which indicates the effectiveness of the matching circuits.

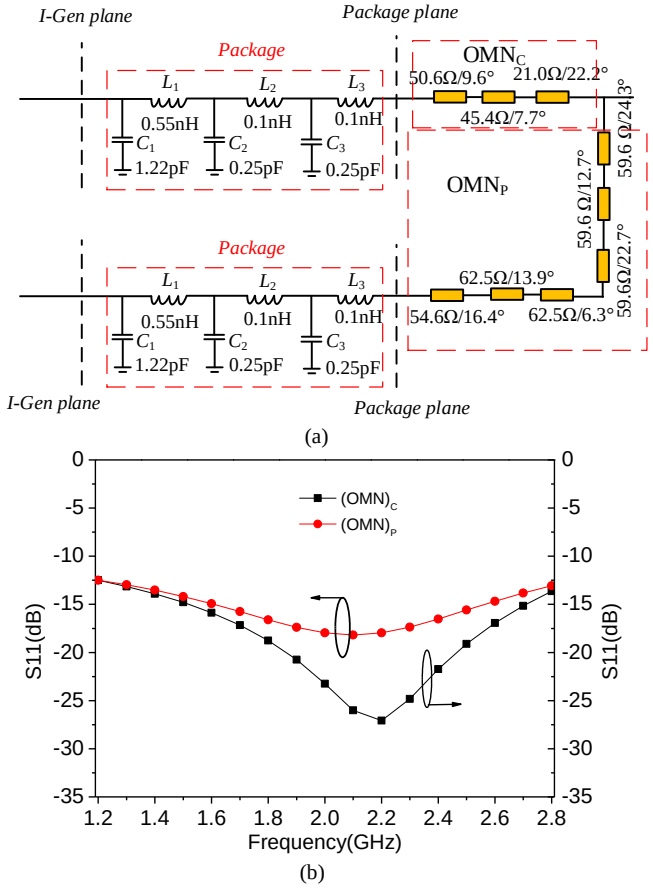


Fig. 8. Output matching networks with device parameters and simulated S11 (a) designed OMN_C and OMN_P (b) simulated S11.

B. Post Matching Network

The complete post matching circuit is shown in Fig. 9(a). Fig. 9(b) shows that the simulated input impedance is acceptable compared with the theoretical value of Z_L. As mentioned before, the load impedance Z_L is 15•(1±j 0.76) Ω. Post-matching circuits design aims to enable the load impedance to match the 50 Ω standards while the harmonic impedance is properly controlled. As shown in Fig. 9,

micro-strip lines TL1, TL2, TL3 and TL4 are used to adjust the harmonic impedances, which makes the second harmonic impedance close to zero and the third harmonic impedance approaching infinity. In addition, harmonic control circuit plays a role in the fundamental impedance transformation, and it can improve the efficiency of DPA. As we known, the harmonic networks would limit the bandwidth of PAs. It is noted that in this work, the harmonic networks are introduced after the combiner instead of in the carrier PA branch and peak PA branch, which is beneficial for broadband design.

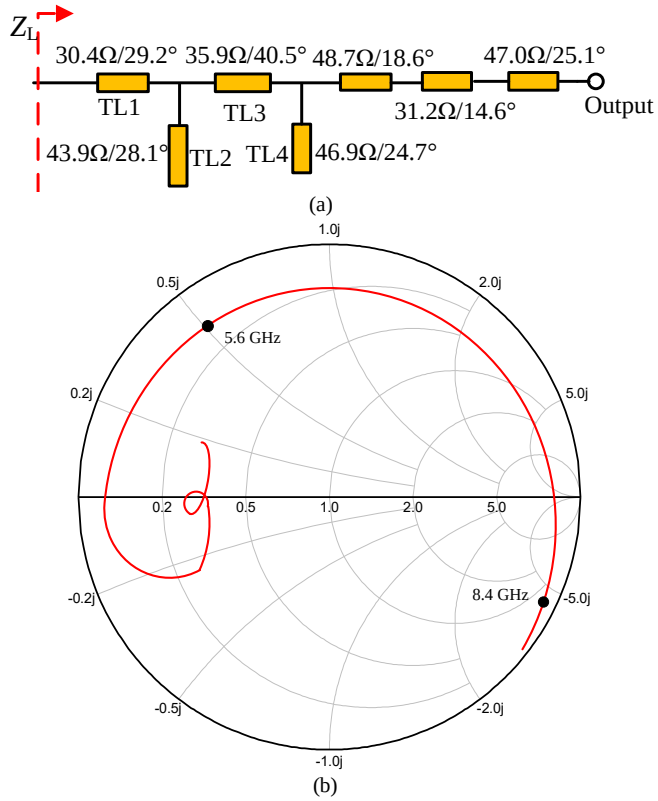
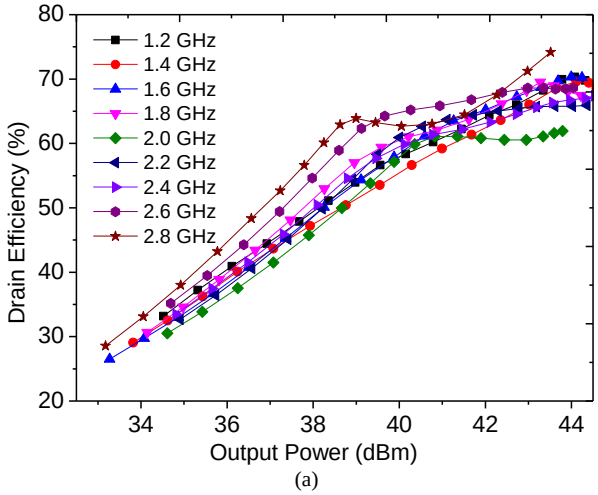


Fig. 9. (a) Post matching networks (b) Simulated impedance of the post matching networks (normalized 50 Ω).

C. *Input Matching Network and DPA Overall Circuit*

Stepped impedance topology is used to synthesize suitable input circuits, and provide a targeted saturation gain of around 10 dB. A resistor *R* is used to maintain the stability of DPAs. Before input matching networks of PAs, a three-stage Wilkinson divider is added to split the signal. In order to satisfy the bandwidth requirement, three stages are applied in the Wilkinson divider. Offset lines are also added in the input networks for ensuring that the signals' phases of the two branches are consistent at the combine node. After all networks are designed, these circuits are combined into a completed DPA. Of course, such a simple combination of DPA may not have the best performance, due to the mutual influence between different circuit networks, and/or non-ideal components. Optimized operation is necessary to optimize the performance of the DPA. The circuit of distributed parameters is finally optimized as shown in Fig. 10.

Fig .11(a) shows the drain efficiency versus output power in different target frequency bands by simulating the designed DPA circuits.



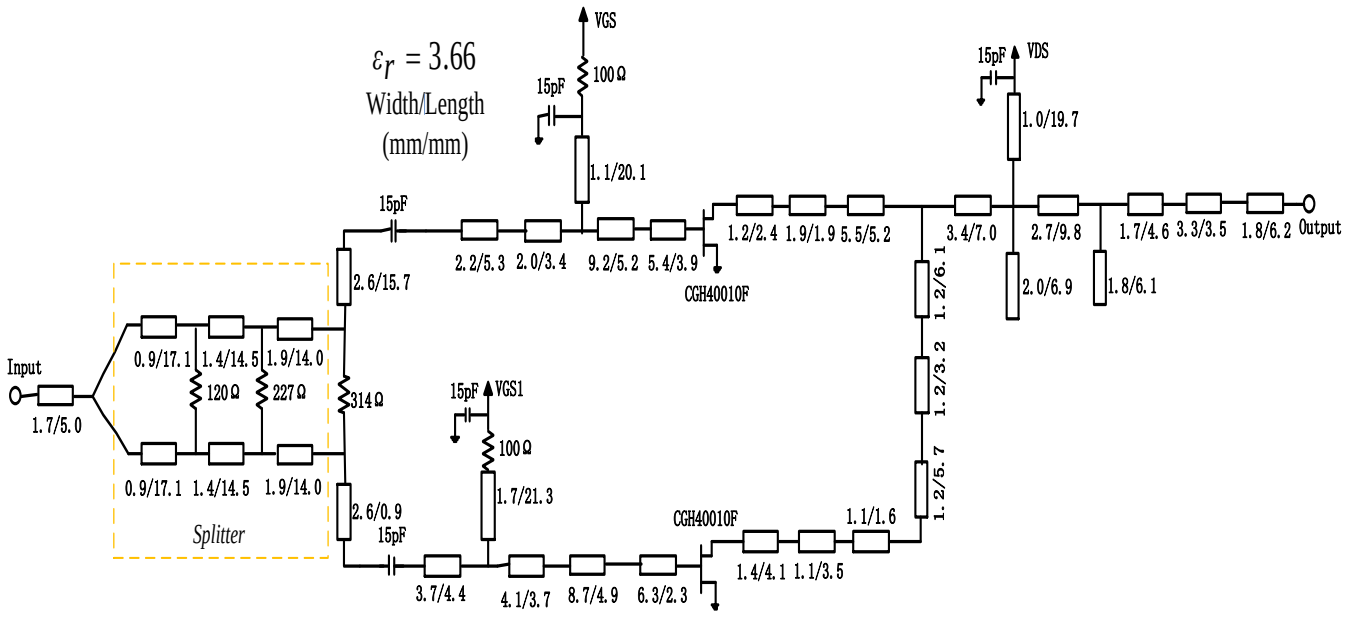
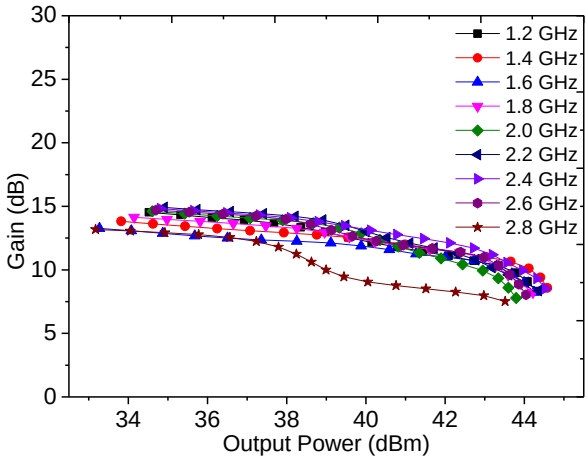


Fig. 10. Completed circuit schematic and parameters value.



(b)

Fig. 11. Simulated performance of the designed DPA(a) drain efficiency, and (b) gain.

Seen from Fig. 11, the designed DPA can get over 43% drain efficiency at the 6 dB OBO level in 1.2-2.8 GHz. It verifies the effectiveness of the proposed method. Fig. 12 shows simulated impedance traces of the carrier PA at different frequencies. The green line is the simulated impedance at the saturation level, which is closer to the R_{OPT}. It is consistent with the theorical value. The red line is the boundary line we calculated earlier, which roughly corresponds to γ of ±0.74, R^* of 25 Ω. Thus, the area on the right of the red line represents the theoretical values corresponding to the blue line in the figure. The dark red line represents the simulated impedance in the target frequency band at the OBO level, which roughly conforms to the theoretical value. The simulated load modulation trajectories of carrier PA and peak PA are shown in Fig. 13. Obviously, although there are some differences from the ideal conditions shown in Fig. 7, both the carrier and the peak PA can achieve load modulation well.

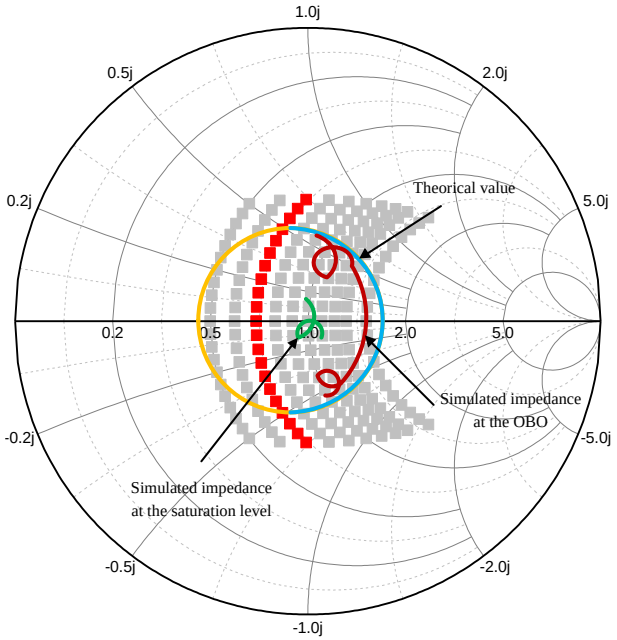
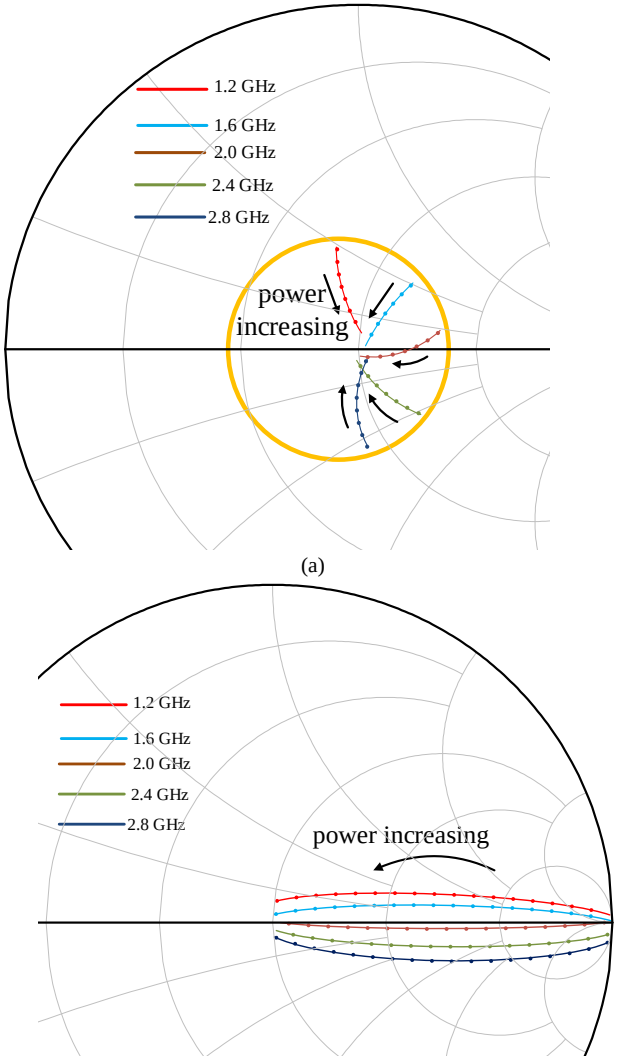


Fig. 12. Simulated load impedance of the carrier PA at the current plane.



(a)

(b)

Fig. 13. Load modulation trajectories of carrier PA and peak PA. (a) carrier PA (b) peak PA.

V. Experiment and Results Analysis

According to the circuits shown in Fig. 10, a DPA is fabricated by using Rogers R4350B (ε_r = 3.66, H = 30 mil) substrate. Fig. 14 shows a photo of the implemented DPA.

Then, measurements are done including S-parameters and large signal performance. The simulated and measured S-parameters are shown in Fig. 15. In 1.2-2.8 GHz, the measured S21 is between 13.5 dB and 16 dB. Correspondingly, the measured S11 is smaller than -10 dB.

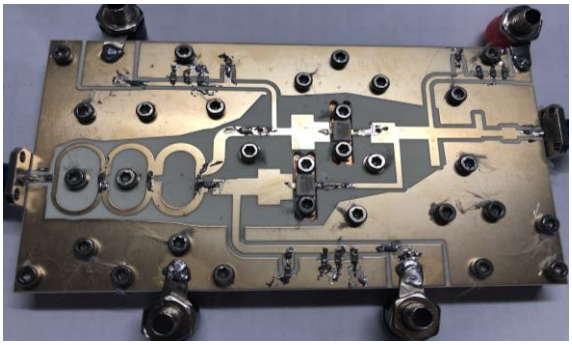


Fig. 14. Photo of the implemented DPA.

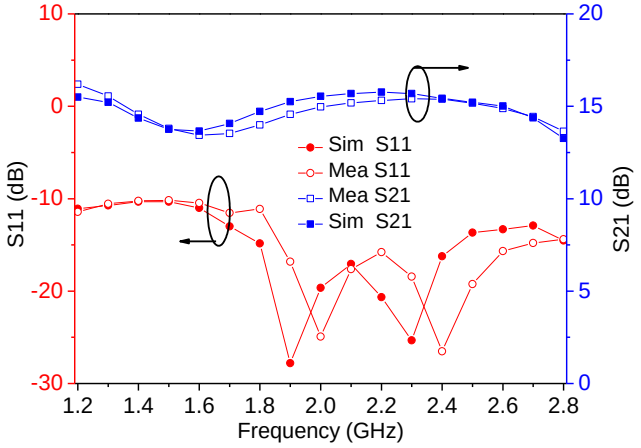


Fig. 15. Simulated and measured S11, S21 of the proposed DPA.

A. Continuous Wave Testing

Output power, drain efficiency and gain of the implemented DPA are measured by using continuous wave signals. The power of input signal is from 20 dBm to 36 dBm.

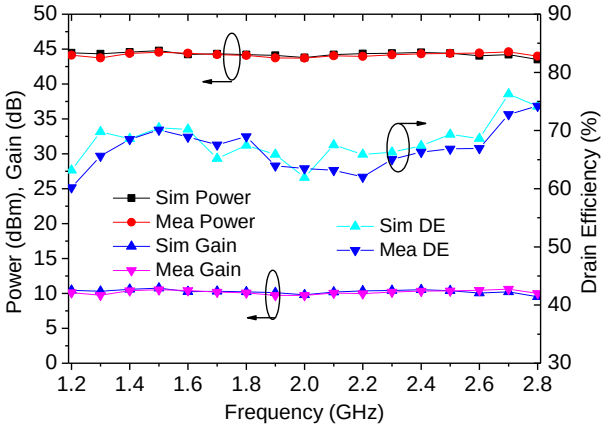


Fig. 16. Simulated and measured performance of the designed DPA at the saturation level.

Fig. 16 and 17 display the measured performances of the proposed DPA. As shown in Fig. 16, the DPA can deliver saturated output power of 43.7-44.1 dBm and saturated drain efficiency is from 60.5% to 74.2% in the frequency range of 1.2-2.8 GHz, while gain is between 9.7 dB and 10.5 dB. From Fig. 17(a), the drain efficiency at the 6 dB OBO level is 48.1-57.6%. As shown in Fig. 17(c), power added efficiency (PAE) can be achieved from 43.4% to 63.5% during load modulation in 1.2-2.8 GHz.

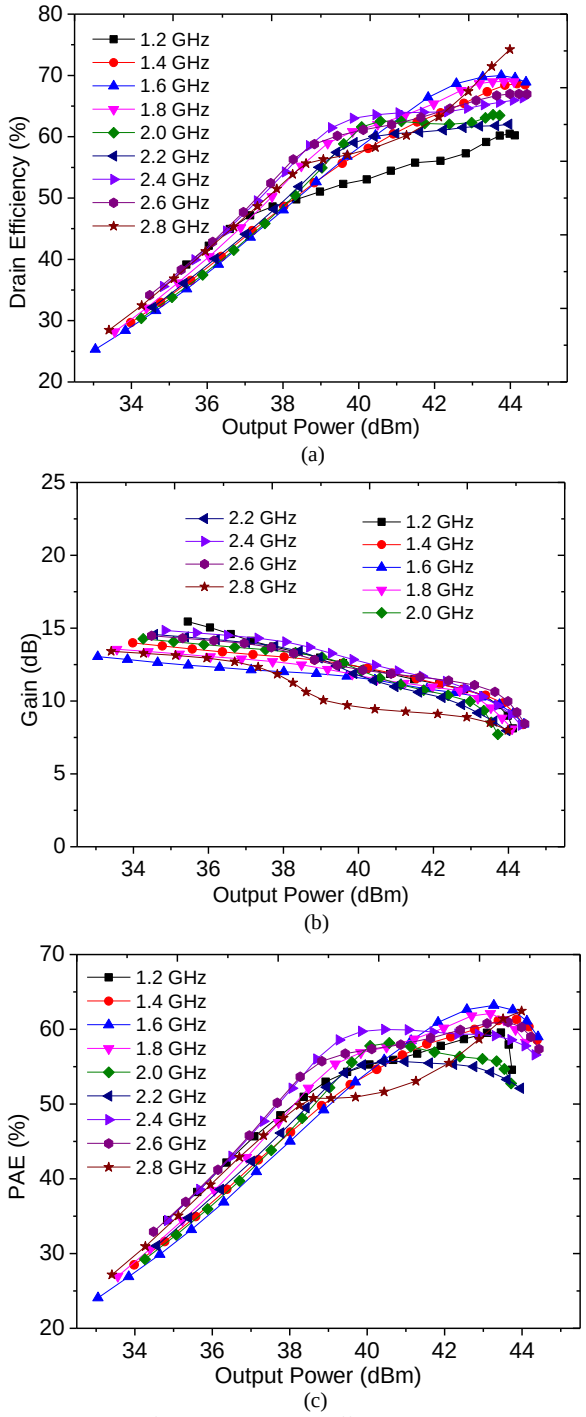


Fig. 17. Measured performances. (a) drain efficiency (b) gain and (c) PAE.

TABLE I
PERFORMANCES COMPARED WITH RECENT DPAS

Ref.	Freq (B.W.) (GHz)	Pout@SAT (dBm)	DE@SAT (%)	DE@ 6dB OBO (%)	Device
2019[19]	1.1-2.4 (74%)	43.3-45.4	55-68	43.8-54.9	2*13W GaN
2016[22]	1.7-2.8 (50%)	44.5-46.3	60-77	52-66	2*16W GaN
2018[23]	1.6-2.7 (51%)	43.8-45.2	56-75.3	46.5-63.5	2*13W GaN
2018[25]	3.3-3.75(13%)	48-48.5	58-71	47-59	2*16W GaN
2013[28]	1.5-2.6 (55%)	41.5-45	33-52	29-49	2*13W GaN
2018[29]	1.5-3.8 (87%)	42.3-43.4	42-63	33-55	2*13W GaN
2014[30]	1.0-2.5 (83%)	40-42	45-83	35-58	2*8W GaN
2018[31]	1.5-2.6 (54%)	41.8	40-45	31-35	2*13W GaN
2019[32]	1.2-2.4 (67%)	42-45	41.6-81	35-63	2*13W GaN
This work	1.2-2.8 (78%)	43.7-44.1	60.5-74.2	48.1-57.6	2*13W GaN

Table I compares the measured drain efficiency and power between the proposed DPA and those in [19], [22-23], [25], [28-32]. It is shown that the fabrication bandwidth of the proposed one, 78%, is larger than the others except the ones in [29] and [30]. Compared with [29] and [30], the drain efficiency in this work is higher than those of [29] and [30] at the saturation level and the OBO level. The proposed DPA is considered in terms of drain efficiency and bandwidth, which can provide a good performance balance and makes it more suitable for practical applications.

B. 2 0 *MHz 6.5dB LTE Testing*

In order to characterize the linearity of the implemented DPA, the adjacent channel ratio (ACLR) is tested by using an LTE signal with a bandwidth of 20 MHz and PAPR of 6.5 dB. The measured ACLR with an average 37.5 dBm output power is plotted in Fig. 18. It reveals that the ACLR is better than -27.4 dBc at 2 GHz. After adopting digital pre-distortion technology (DPD), the ACLR value is better than -48.6 dBc.

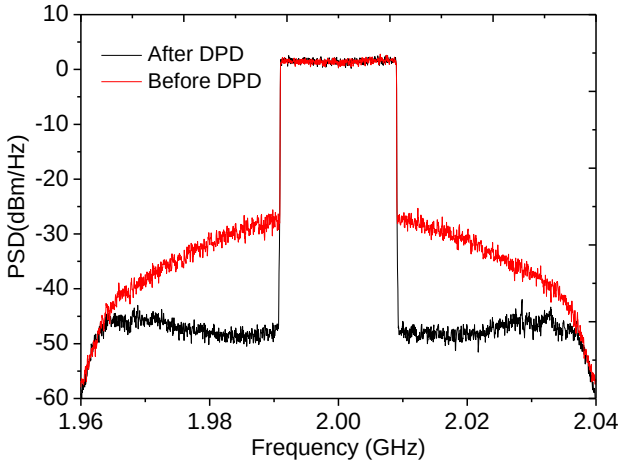


Fig. 18. Measured ACLR at 2.0 GHz with a 37.5 dBm average output power.

VI. CONCLUSION

This paper applies the class-EFJ PA as the carrier PA of DPAs. Bandwidth characteristic of the DPAs with the class-EFJ PA is analyzed. Maximum relative bandwidth of 78% can be achieved by properly selecting corresponding parameter values. The design parameters are derived, and the design process is described in detail. For validation, a broadband DPA operating in 1.2-2.8 GHz is designed and fabricated. Measurements show that the designed DPA based on the proposed theory and method can deliver over 43 dBm output power with over 60% drain efficiency in saturation in 1.2-2.8 GHz. Moreover, at the 6 dB OBO stage, the drain efficiency can be higher than 48.1% in 1.2-2.8 GHz.

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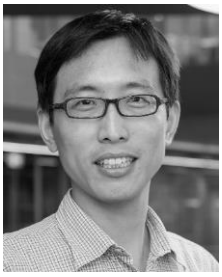

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