

Software Pipelining for Quantum Loop Programs

Guo Jingzhe

Department of Computer Science
and Technology
Tsinghua University
China
gjz20@mails.tsinghua.edu.cn

Mingsheng Ying

CQSI, FEIT, University of Technology Sydney
Australia
Institute of Software, CAS, China
Tsinghua University, China
mingshengying@gmail.com

Abstract

We propose a method for performing software pipelining on quantum for-loop programs, exploiting parallelism in and across iterations. We redefine concepts that are useful in program optimization, including array aliasing, instruction dependency and resource conflict, this time in optimization of quantum programs. Using the redefined concepts, we present a software pipelining algorithm exploiting instruction-level parallelism in quantum loop programs. The optimization method is then evaluated on some test cases, including popular applications like QAOA, and compared with several baseline results. The evaluation results show that our approach outperforms loop optimizers exploiting only in-loop optimization chances by reducing total depth of the loop program to close to the optimal program depth obtained by full loop unrolling, while generating much smaller code in size. This is the first step towards optimization of a quantum program with such loop control flow as far as we know.

Keywords: quantum program scheduling, quantum program compilation

1 Introduction

Quantum computer hardware has reached the so-called quantum supremacy showing that quantum computation can actually outperform classical computation for certain tasks, but it is still in the NISQ (Noisy-Intermediate-Scale-Quantum) era where there are no sufficient quantum bits (qubits, for short) for quantum error correction.

Program optimization is particularly important for executing a quantum program on NISQ hardware in order to reduce the number of required qubits, the length of gate pipeline, and to mitigate quantum noise. Indeed, there has already been plenty of work on optimization and parallelization of quantum programs. Theoretically, it was proved in [5] that compilation of quantum circuits with discretized time and parallel execution can be NP complete. Practically, quantum hardware architectures, especially those based on superconducting qubits, provide instruction level support for exploiting parallelism in quantum programs; for example, Rigetti’s Quil [20] allows programmers to explicitly specify multiple instructions that do not involve same qubits to be executed together, while in Qiskit, ASAP or ALAP

scheduling is performed implicitly [23]. Furthermore, several compilers have been implemented that can optimize quantum circuits by exploiting instruction level parallelism; for example, ScaffCC [11] introduces critical path analysis to find the “depth” of a quantum program efficiently, revealing how much parallelism there is in a quantum circuit; commutativity-aware logic scheduling is proposed in [18] to adopt a more relaxing quantum dependency graph than “qubit dependency” by taking in mind commutativity between the R_Z gates and $CNOT$ gates as well as high-level commutative blocks while scheduling circuits. There are also some more sophisticated optimization strategies reported in in previous works [10, 13, 19, 22].

Quantum hardware will soon be able to execute quantum programs with more complex program constructs, e.g. for-loops. However, most of the optimization techniques in previous work only deal with sequential quantum circuits. Some methods allow loop programs as their input, but those loops will be unrolled immediately and optimization will be performed on the unrolled code. Loop unrolling is the technique that allows optimization across all iterations of a loop, but comes at a price of long compilation time, redundant final code and run-time compulsory cache misses. As quantum hardware in the near future may allow up to hundreds of qubits, it will often be helpful to preserve loop structure during optimization since the growth in number of qubits will also lead to increment in total gate count, as well as increment in difficulty unrolling the entire program.

Software pipelining [12] is a common technique in optimizing classical loop programs. Inspired by the execution of an unrolled loop on an out-of-order machine, software pipelining reorganizes the loop by a software compiler instead of by hardware. There are two major approaches for software pipelining:

- Unrolling-based software pipelining usually unrolls loop for several iterations and finds repeating pattern in the unrolled part; see for example [2].
- Modulo scheduling guesses an initiation interval first and try to schedule instructions one by one under dependency constraints and resource constraints; see for example [12].

Our Contributions: We hereby presents a software pipelining algorithm for parallelizing a certain kind of quantum loop programs. Our parallelization technique is based on a

novel and more relaxed set of dependency rules on a CZ-architecture (Theorems 1 and 2). The algorithm is essentially a combination of unrolling-based software pipelining and modulo scheduling [12], with several modifications to make it work on quantum loop programs.

We carried out experiments on several examples and compared the results with the baseline result obtained by loop unrolling. Our approach proves to be a steady step toward bridging the gap between optimization results without considering across-loop optimization and fully unrolling results while restraining the increase in code size.

Organization of the Paper: In Section 2, we review some basic definitions used in this paper. The theoretical tools for defining and exploiting parallelism in quantum loop program are developed in Section 3. In Section 4, we present our approach of rescheduling instructions across loops, extracting prologue and epilogue so that depth of the loop kernel can be reduced. The evaluation results of our experiments are given in Section 5. The conclusion is drawn in the Section 6. [For conciseness, all proofs are given in the Appendices.]

2 Preliminaries and Examples

This section provides some backgrounds [14, 25] on quantum computing and quantum programming.

2.1 Basics of quantum computing

The quantum counterparts of bits are qubits. Mathematically, a state of a single qubit is represented by a 2-dimensional complex column vector $(\alpha, \beta)^T$, where T stands for transpose. It is often written in the Dirac's notation as $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$ with $|0\rangle = (1, 0)^T$, $|1\rangle = (0, 1)^T$ corresponding to classical bits 0 and 1, respectively. It is required that $|\psi\rangle$ be unit: $\|\alpha\|^2 + \|\beta\|^2 = 1$. Intuitively, the qubit is in a superposition of 0 and 1, and when measuring it, we will get 0 with probability $\|\alpha\|^2$ and 1 with probability $\|\beta\|^2$. A gate on the qubit is then modelled by a 2×2 complex matrix U . The output of U on an input $|\psi\rangle$ is quantum state $|\psi'\rangle$. Its mathematical representation as a vector is obtained by the ordinary matrix multiplication $U|\psi\rangle$. To guarantee that $|\psi'\rangle$ is always unit, U must be unitary in the sense that $U^\dagger U = I$ where U^\dagger is the adjoint of U obtained by transposing and then complex conjugating U . In general, a state of n qubits is represented by a 2^n -dimensional unit vector, and a gate on n qubits is described by a $2^n \times 2^n$ unitary matrix. [For convenience of the readers, we present the basic gates used in this paper in Appendix A.]

2.2 Quantum execution environment

Software pipelining is a highly machine-dependent approach of optimization. So we must give out some basic assumptions about the underlying machine that our algorithm requires. State-of-the-art universal quantum computers differ in many ways:

- **Instruction set:** A quantum computer chooses a universal set of quantum gates as its low-level instructions. For example, IBM Q[4] uses controlled-NOT $CNOT$ and three one-qubit gates U_1, U_2, U_3 , but Rigetti Quil[20] uses controlled-Z CZ and one-qubit rotations R_X, R_Z . We use the universal gate set $\{U_3, CZ\}$ for the reason that U_3 itself is universal for single qubit gates, which allows us to merge single qubit gates at compile time. [see Appendix A for the definition of these gates.]
- **Instruction parallelism:** Different quantum computers are implemented on different technologies, constraining their power to execute multiple instructions simultaneously. Usually superconductive quantum computers support parallelism while ion-trap ones do not. We assume qubit-level parallelism: instructions on different qubits can always be executed simultaneously.
- **Timing:** Different quantum computers may use different timing strategies, using continuous time or discrete time. Also execution time of different instructions may differ and is highly machine-dependent. Usually a two-qubit gate (e.g. CZ and $CNOT$) costs much longer time than single qubit gates. We use a discrete time model with every gate requiring 1 tick equally.
- **Qubit connectivity:** Different machines may have different qubit topologies. However, we assume that all gates in the input are directly executable, which may require a layout synthesis step before our optimization.
- **Classical control.** The support for classical control flow varies among different quantum computers; for example, IBM Q does not support any complex control flow, while Rigetti Quil supports branch statements. We assume such classical controls [see Appendix C].

The above assumptions do not fit into the existing quantum hardware architecture perfectly (for instance, IBM Q requires $CNOT$ and Quil disallows U_3), while the architecture of Google's devices[22] fits these requirements most. With some slight modifications, however, our method can be easily adapted to unsupported architectures [see Appendix L].

2.3 Quantum loop programs

We focus on a special family of quantum loop programs, called *one-dimensional for-loop programs*, defined as below:

```

program := header statement*
header := [(qdef | udef)*]
qdef := qubit ident[ $\mathbb{N}$ ];
udef := defgate ident[ $\mathbb{N}$ ] = gate;
gate := [( $\mathbb{C}^{2 \times 2}$ )*] |  $R_Z$  |  $R_Z^+$  | Unknown
gateref := ident[expr]
qubit := ident[expr]
op :=  $SQ$ (gateref) qubit |  $CZ$  qubit, qubit;

```

statement := **op** | *for ident* in \mathbb{Z} to $\mathbb{Z}\{\text{op}^*\}$
 | *for ident* in **ident** to **ident**{**op***}
expr := $\mathbb{Z} * \text{ident} + \mathbb{Z}$

where:

- The loop involves a group of one-dimensional qubit array variables defined by **qdef**.
- The loop has only one iteration variable i starting from a to b with stride 1. The range $[a, b]$ is completely known at compile time, or completely unknown until execution. This allows our algorithm to be performed on a program with parametric loop range.
- All array index expressions are in the form $(ki + b)$, where i is the iteration variable, and $k, b \in \mathbb{Z}$ are known constants.
- All operations in the loop body are either an one-qubit gate, or a CZ gate on two qubits. We don't consider measurement operations.
- One-qubit gates are defined by **udef**. They are given as known matrices, or "an element in an array of unknown matrices" when a hint on whether the matrix array is diagonal or antidiagonal can be given. This allows our algorithm to be performed on a program with parametric gates or performing different gates on different iterations.

At the very start of the entire program, all qubit arrays are initialized as $|0\rangle$. Our optimization may introduce some branch statements if the endpoints a and b are unknown before code execution. As a result, the output language of the compiler is a superset of the input language above, with support for branch statements [see Appendix C for one possible definition of output language]. To show versatility of the above loop, let us consider several popular quantum algorithms.

Example 1. Grover algorithm [9] is designed for the black-box searching problem: given a function $f : \{0, 1\}^n \rightarrow \{0, 1\}$, find a bitstring $x : \{0, 1\}^n$ such that $f(x) = 1$. While a classical algorithm requires $\Omega(n)$ calls to the oracle, Grover search can find a solution in $O(\sqrt{n})$ calls of quantum oracle $U_f(|x\rangle \otimes |b\rangle) = |x\rangle \otimes |b \oplus f(x)\rangle$. This is done by repeating a series of quantum gates, called Grover iteration. Grover search can be written as the loop program:

```

for  $i$  in 0 to  $N-1$  do
   $H[q[i]]$ 
end for
 $H[q_{work}]$ 
for  $i$  in 1 to  $O(\sqrt{N})$  do
   $U_f[q, q_{work}]; (2|\psi\rangle\langle\psi| - I)[q]$ 
end for

```

Example 2. A Quantum Approximate Optimization Algorithm (QAOA for short) is designed in [8] to solve the MaxCut problem on a given graph $G = \langle V, E \rangle$. It can be written as a parametric quantum loop program:

```

for  $i=0$  to  $(N-1)$  do
   $H[q[i]]$ 
end for
for  $i=1$  to  $p$  do
  for  $(a, b) \in E$  do
     $CNOT[q[a], q[b]]; U_B[i][q[b]]; CNOT[q[a], q[b]]$ 
  end for
  for  $j=0$  to  $(N-1)$  do
     $U_C[j][q[j]]$ 
  end for
end for

```

Here, we use parametric gate arrays $U_C[i] = R_X(\beta_i, j)$ and $U_B[i] = R_Z(-\omega_{ab} \gamma_i)$ of rotations. The two innermost loops can be unrolled to satisfy our input language requirements. Since QAOA repeatedly executes the circuit but each time with different sets of angles $\{\beta_i\}$ and $\{\gamma_i\}$, an optimizer has to support compilation of the circuit above without knowing all parameters in advance. Note that the compiler can know in advance that $U_B[i]$ are diagonal matrices, and this hint might be used during optimization. [for a further explanation of QAOA see see Appendix B]

3 Theoretical tools

In this section, we develop a handful of theoretical techniques required in our optimization. To start, let us identify some of the most critical challenges in optimizing quantum loop programs:

- Instructions may be **merged** together at compile time, potentially reducing the total depth. However, merging instructions needs to know which instructions may be adjacent in the unrolled pattern, thus requiring us to resolve all possible **qubit aliases**.
- **Data dependency** graph in a quantum program is usually much denser than that in classical program, since generally two matrices are not commutable, that is, $AB \neq BA$.
- **Resource constraint**, which prevents instructions that do not have dependency from executing together, is quite different in quantum case from classical case.

We will show how much optimization can be done by mitigating these challenges in loop reordering.

3.1 Gate merging

Our assumptions allow several instructions to be merged into a single instruction with the same effect:

- Two adjacent one-qubit gates on the same qubit can be merged, since we are using U_3 .
- Two adjacent CZ gates on the same qubits can cancel each other.

Example 3. Figure 1 is a simple case for periodical gate merging pattern. The two one-qubit gates in different iterations may

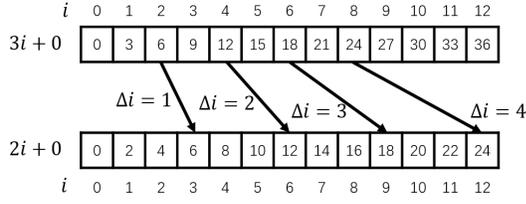


Figure 5. An example for across-loop qubit aliasing with $k_1 = 3$ and $k_2 = 2$. For $T = \mathbb{Z}$, $\Delta i = 1$, while for $T = [4, 10]$, $\Delta i = 2$.

To see the second problem, we note that detection of memory aliasing [1] is usually solved by an Integer Linear Programming (ILP) problem solver such as Z3[7]. However, a general ILP problem is NP-complete in theory and may take long time to solve in practice. Fortunately, we will see that all problems that we are facing can be solved efficiently in $O(1)$ time without an ILP solver.

We consider two references to a same qubit array: $q[k_1 i + b_1]$, $q[k_2 i + b_2]$, $i \in T$, where T is the loop interval when the loop range is known and \mathbb{Z} when unknown.

Definition 1. In-loop qubit aliasing: To check whether two instructions can always be executed together, we have to check if one qubit reference may be an alias of another, that is, $(\exists i \in T) (k_1 i + b_1 = k_2 i + b_2)$.

This problem can be easily solved by checking whether $(b_2 - b_1)$ is a multiple of $(k_1 - k_2)$ and $\frac{b_2 - b_1}{k_1 - k_2}$ lies in T .

Definition 2. Across-loop qubit aliasing: To check whether there is an across-loop dependency between two instructions, we have to check if one qubit reference may be an alias of another qubit reference **several iterations later**. Thus, we need to find the minimal increment $\Delta i \geq 1$, s.t.

$$(\exists i \in T) ((i + \Delta i \in T) \wedge (k_1 i + b_1 = k_2 (i + \Delta i) + b_2)). \quad (1)$$

This issue can be reduced to the Diophantine equation

$$(k_2 - k_1)i + k_2(\Delta i) = b_1 - b_2, i \in T, i + \Delta i \in T, \Delta i \geq 1, \quad (2)$$

which can be solved in $O(1)$ time [see Appendix D]. We solve the equation every time when needed rather than memorizing its solution. A visualization of across-loop qubit aliasing is presented in Figure 5.

3.3 Instruction data dependency

One most important step in rescheduling a loop is to find the data dependencies - instructions that can not be reordered while scheduling. Previous work mostly defined instruction dependency according to matrix commutativity: the order of two instructions can change if their unitary matrices satisfy $AB = BA$. This captures most commutativity between gates, but not all. Here, we relax this requirement by establishing several novel and more relaxed commutativity rules between quantum instructions. Since CZ gates is the only two-qubit

gate we use and any two CZ gates commute with each other, what we need to care about is commutativity between CZ gates and one-qubit gates.

Definition 3. (CZ conjugation) If for one-qubit gates U_A, U_B, V_A and V_B , we have $CZ U_A U_B CZ = V_A V_B$, we say CZ conjugates $U_A \otimes U_B$ into $V_A \otimes V_B$.

Conjugation allows us to swap a CZ gate with a pair of one-qubit gates, at the price of changing U_A and U_B to V_A and V_B correspondingly. The following theorem identifies all possible conjugations.

Theorem 1. (CZ conjugation of single qubit gates) CZ conjugates $U_A \otimes U_B$ into some $V_A \otimes V_B$ **if and only if** U_A and U_B are diagonal or anti-diagonal: $U_i = R_Z(\theta)$ or $U_i = R_Z^+(\theta)$ for $i \in \{A, B\}$.

Note 1. The antidiagonal rule has been named “EjectPhased-Paulis” in [22]. However we propose the rules for both necessity and sufficiency: no more commutation rules can be obtained at gate level.

Since identity matrix I is diagonal, U_A and U_B can be thought of as going under conjugation separately. Thus, we only need to consider two special cases: $I \otimes R_Z$ and $I \otimes R_Z^+$. Note that in conjugation rules R_Z^+ will always introduce a Z gate to the other qubit. This inspires us to generalize Theorem 1 for a generalized form of CZ defined in the following:

Definition 4. (Generalized CZ gates) For $x, y \in \{0, 1\}$, we define following variants of CZ gate:

$$\begin{aligned} CZ_{11}[a, b] &= CZ[a, b], & CZ_{00}[a, b] &= -Z[a]Z[b]CZ[a, b] \\ CZ_{10}[a, b] &= Z[a]CZ[a, b], & CZ_{01}[a, b] &= Z[b]CZ[a, b] \end{aligned}$$

Equivalently, CZ_{xy} can be defined as follows: $CZ_{xy}|ab\rangle = (-1)^{\delta_{ax}\delta_{by}}|ab\rangle$, where δ_{ij} is Kronecker delta. Now we have the following commutativity rules for generalized CZ:

Theorem 2. (Generalized CZ conjugation of single qubit gates) When exchanged with R_Z^+ , CZ gate changes into one of its variants by toggling the corresponding bit.

1. $R_Z(\alpha)[b]CZ_{xy}[a, b] = CZ_{xy}[a, b]R_Z(\alpha)[b]$;
2. $R_Z^+(\alpha)[b]CZ_{xy}[a, b] = CZ_{x(1-y)}[a, b]R_Z^+(\alpha)[b]$.

Since generalized CZ gates are also diagonal, they commute with each other and can be scheduled just as ordinary CZ gate and converted back to CZ by adding Z gates.

3.4 Instruction resource constraint

Qubits have properties that resemble both data and resource: qubits work as quantum data registers and carry quantum data; meanwhile, qubit-level parallelism allows all instructions, if they operate on different qubits, to be executed simultaneously. This results in a surprising property for quantum programs: the resources should be described using linear expressions, instead of by a static “resource reservation table” as in the classical case. Using the rules for detecting qubit

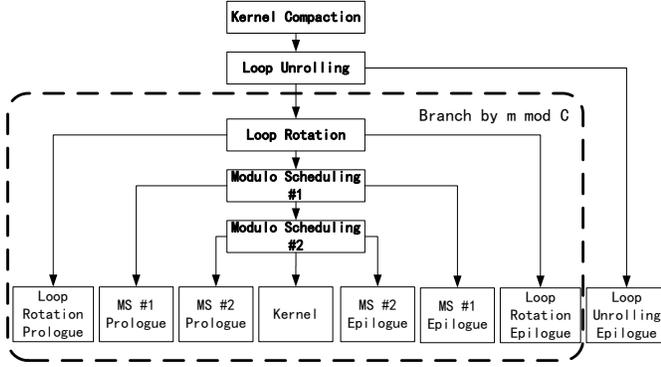


Figure 6. The entire compilation flow of our approach.

aliases, we simply check if there is an aliasing between the qubit references from two instructions, that is, the two instructions share a same qubit at some iteration and cannot be executed simultaneously.

4 Rescheduling loop body

Now we are ready to present the main algorithm for pipelining quantum loop programs. It is based on modulo scheduling via hierarchical reduction [3], but several modifications to the original algorithm are required to fit into scheduling quantum instructions on qubits. The entire flow of our approach is depicted in Figure 6. For simplicity we suppose the number of iterations is large enough so that we don’t worry about generating a long prologue/epilogue.

4.1 Loop body compaction

At first we compact the loop kernel to merge the gates that can be trivially merged, including: (a) adjacent single qubit gates; (b) diagonal or antidiagonal single qubit gates and their nearby single qubit gates, maybe at the other side of a CZ gate; and (c) adjacent CZ gates. To this end, we define the following compaction procedure, which considers the potential aliasing between qubits:

Definition 5. A greedy procedure for compacting loop kernel:

- Initialize all qubits with an identity gate.
- Place all instructions one by one. Initialize **operation** to “Blocked”. Check the new instruction (A) against all placed instructions (B). Update **operation** according to Table 1.
- Perform the last **operation** according to the table.
 - “Blocked” means the instruction is put at the end of the instruction list.
 - “Merge with B” means the single qubit instruction is merged with the placed single qubit gate B. If the placed gate is an antidiagonal, Z gates should be added for uncancelled CZ gates that occur earlier but are placed after the antidiagonal.

- “Cancelled” means two CZ gates are cancelled. Note that the added Z gates are not cancelled. Also, a third arriving CZ can “uncancel” a cancelled CZ, which we also call as “Cancelled”.

This compaction can be done in two directions: compacting to the left or to the right. They can be seen as the results of ASAP schedule and ALAP correspondingly. However, this procedure does not guarantee compacting once will converge: not all the outputs from the procedure are fixpoints of the procedure. For example, the circuit in Figure 7 only converges after three applications of left compaction. In general, we have the following:

Theorem 3. Compacting three times results in a fixpoint of the compaction procedure.

Note that we allow using unknown single-qubit gates. If all components are known to be diagonal or antidiagonal, the product of these matrices is also diagonal or antidiagonal [see Appendix F]. Otherwise, we can only see the product as a general matrix. However, this does not affect our result of three-time compaction. Also compacting in one direction does not capture all chances of merging. Figure 8 shows that some single-qubit merging changes are missed out. In practice we perform a left compaction after a right compaction.

4.1.1 Loop unrolling and rotation. Loop kernel compaction can only discover gate merging and cancellation in one iteration. However, gate merging and cancellation can also occur across iterations. For example, in Figure 4 the last H gate in the previous iteration can be merged and cancelled with the first H gate in the next iteration. This kind of cancellation cannot be discovered by software pipelining either, since it is a reordering technique and cannot cancel instructions out.

An instruction i in one iteration may merge or cancel with instruction j from $t \geq 1$ iterations later. All potential merging of single qubit gates and cancellable CZ gates can be written out by enumerating all pairs of instructions. Loop rotation[15] is an optimization technique to convert across-loop dependency to in-loop dependency (so that some variables can be privatized and optimized out). Consider a loop ranging from m to n : $\{A_i B_i C_i\}_m^n$. Here, A_i can be rotated to the tail of the loop: $A_m \{B_i C_i A_{i+1}\}_m^{n-1} B_n C_n$, and C_i and A_{i+1} are now in one iteration. If C_i writes into a temporary variable and A_{i+1} reads from it, this variable can be privatized. For merging candidates with $t = 1$, we can use a similar procedure:

Definition 6. An instruction is considered movable if it satisfies one of following conditions:

- The instruction is a single-qubit gate, and there are no gates on the same qubit or on an aliasing qubit before it; in this case the instruction can be rotated to the right.

A\B	SQ with same qubit	SQ with in-loop aliasing	CZ with same qubit	CZ with aliasing qubit
Diagonal SQ	Merge with B	Blocked		
AntiDiagonal SQ	Merge with B	Blocked		Blocked
General SQ	Blocked	Blocked	Blocked	Blocked
CZ	Blocked	Blocked	If exactly-same then Cancel	

Table 1. Operation table for loop kernel compaction. Empty cell means using previous operation. Check is performed from left to right, so antidiagonal can pass through CZ with a same qubit and an aliasing qubit.

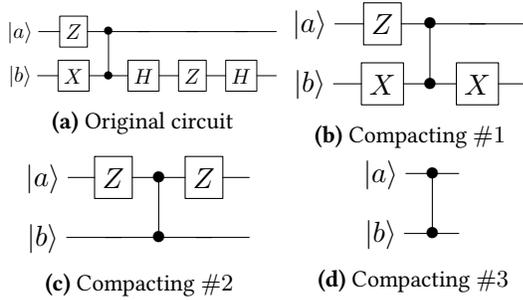


Figure 7. Compacting more than once yields better result.

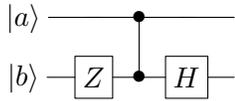


Figure 8. Left compaction will miss the chance of compacting the Z gate and the H gate.

- The instruction is a CZ gate, and there are no **single-qubit gates** on the same qubit or on aliasing qubits; in this case the instruction can be rotated to the right.
- The instruction is a CZ gate, and there are no **single-qubit gates** on the same qubit or on aliasing qubits **except** the CZ gate has only one linear offset reference with $k = 0$ and there is a single-qubit gate on this qubit. In this case, the instruction will be rotated to the right along with this single qubit gate.

This definition of movable instructions guarantees the programs before and after the rotation are equivalent. We use the following procedure to rotate one instruction from left to right:

1. Find the first **unmarked** movable instruction that, there exists another instruction to merge or cancel with $t = 1$.
2. **Mark** the chosen instruction, and rotate the instruction to the right. The instruction is added to prologue and the others added to epilogue.
3. Perform left compaction on the new loop kernel. Note that the left-compaction algorithm is modified, so that merging single-qubit gates or cancelling CZ gates will clear the mark.
4. If there is no rotatable instruction, stop the procedure.

Corollary 4. If the original loop has only candidates with $t = 1$ and no one-qubit gate merges with itself, this procedure eliminates all across-loop merging or cancellation. That is, if we unroll the loop after rotation, the unrolled quantum “circuit” should be a fixpoint of compaction procedure.

However, loop rotation can only handle potential gate merging across one iteration (i.e. from nearby iterations). To handle potential merging across many iterations, we adopt loop unrolling from classical loop optimization. While the major objective for loop unrolling is usually to reduce branch delay, Aiken et al. [2] also used loop unrolling to unroll first few iterations of loop and schedule them ASAP, so that repeating patterns can be recognized into an optimal software pipelining schedule. Our approach uses modulo scheduling instead of kernel recognition, but we can still exploit the power of loop unrolling to capture patterns that require many iterations to reveal. The key point is that unrolling decreases t . Suppose we use a graph to represent all “candidates for instruction merging”, with edge $A \xrightarrow{t} B$ indicating instruction A will merge with or cancel out instruction B from t iterations later, if we unroll the loop by C times, the weight of the edges in the graph will decrease.

Example 5. Figure 9 gives an example showing the connection between the “merging graph” before unrolling and the one after unrolling: if $\forall t, C \geq t$, there are no edges with $t > 1$.

There is a tradeoff between generated code length (determined by C) and remaining $t > 1$ edges. For example, if there is an edge with $t = 10000$, we are not likely to unroll the loop for 10000 times just to merge the two single qubit gates. Also for eliminating self-cancelling CZ gates (i.e. CZ gates on a pair of constant qubits), we may want $C \geq 2$ and C even. In the following discussion we use C as a configurable variable in our algorithm determining the maximal allowed unroll time (and the minimal time of iterations of the loop). The new unrolled loop will be in the form

$$\begin{aligned} \text{for}(i = m; i \leq n; i += C) \{op(k_i i + b_i)\} \\ \text{for}(i = m'; i \leq n; i + 1) \{op(k_i i + b_i)\} \end{aligned} \quad (3)$$

and the first loop should be written into

$$\text{for}(i = 0; i \leq n'; i + 1) \{op(Ck_i i + b_i + mk_i)\} \quad (4)$$

where $n' = \lfloor \frac{n-m+1}{C} \rfloor - 1$ and $m' = C(n' + 1) + m$. This step of transformation makes sure the loop stride is still 1 after

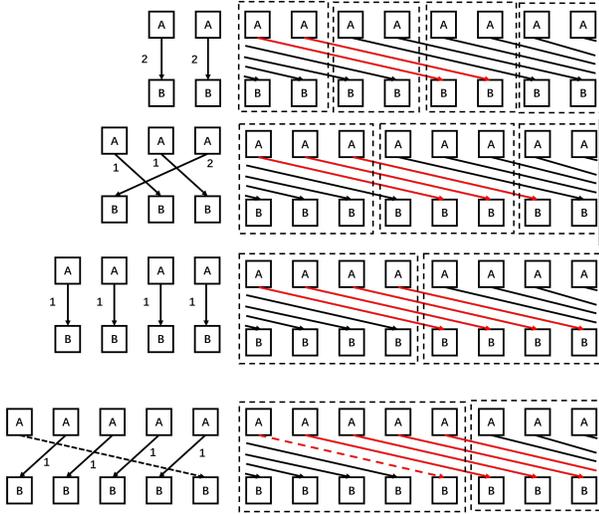


Figure 9. Example for the QDGs of loop “ $A \xrightarrow{4} B$ ” unrolled 2, 3, 4 and 5 times. Unrolling the loop decreases the edge weight t . When $C = \max \{t\}$ all edges will be decreased to weight 1.

loop unrolling. Note that item (mk_t) appears in every offset of the loop body. If m is unknown we can’t proceed with our algorithm. Fortunately, since $m = pC + q, q = m \bmod C$, we have $Ck_t i + b_t + mk_t = Ck_t(i + p) + b_t + qk_t$, showing that when the range is unknown, the results of array dependency depend only on the Euclidean modulo $q = m \bmod C$. In this case, we can generate C copies of code for each case of q , and perform following parts of the algorithm on each copy.

Let us briefly summarize our compilation flow till now: we compact the loop kernel, unroll the loop by C , and rotate some instructions in the unrolled loop kernel. The unrolling step may copy the loop by C times, and steps after unrolling (including rotation) will be performed on each copy.

4.2 Modulo scheduling

Our next step is modulo scheduling borrowed from [12]:

1. Find in-loop and loop-carried dependencies.
2. Estimate an initialization interval II . For simplicity we use binary search and the maximum II is total instruction count. Use Floyd to check validity.
3. Using Tarjan algorithm to find strong connected components and schedule all SCCs by in-loop dependency subgraph.
4. Merge every SCC in DDG into one node, obtaining a new DDG.
5. Schedule the new DDG by list scheduling.

There are some major differences between quantum programs and the classical programs considered in [12]:

4.2.1 Quantum dependency graph. The instruction dependency for quantum programs is described by a QDG

(Quantum Dependency Graph) as a generalization of DDG (Data Dependency Graph), where vertices represent instructions and edges represent precedence constraints that must be satisfied while reordering. In modulo scheduling, a dependency edge is described by two integers: min and dif . Suppose there is an edge pointing from instruction A to instruction B with parameter (min, dif) , it means “instruction B from dif iterations later should be scheduled at least min ticks later than instruction A in **this** iteration”. Recall from Section 3.2 and 3.3, our dependency is defined by the rules:

1. There are no dependencies between CZ gates, or between a CZ and a diagonal single qubit gate.
2. In-loop dependency: if two offsets are on the same qubit array and reveal in-loop qubit aliasing, there is a dependency edge $(1, 0)$ between the corresponding instructions. To unify with across-loop, we set $\Delta i = 0$.
3. Across-loop dependency: if two offsets are on the same qubit array and reveal across-loop qubit aliasing with Δi , there is a dependency edge $(1, \Delta i)$ between the corresponding instructions.
4. Exception on antidiagonal gates: if the qubit $(k_1 i + b_1)$ of an antidiagonal gate aliases with one operand $k_2 i + b_2$ of a CZ gate and $k_1 = k_2$, we remove the edge if there’s no aliasing on the other operand.
5. Exception on single qubit gates: if two single qubit gates operate on the same qubit array where offsets $(k_1 i + b_1)$ and $(k_2 i + b_2)$ aliases with each other and $k_1 = k_2$, we specify the dependency edge to be valued $(0, \Delta i)$, that is, $min = 0$ rather than $min = 1$.

There may be multiple edges in the graph connecting the same pair of instructions; for example, an in-loop dependency and an across-loop dependency between the two instructions. Since we are going to use Floyd algorithm on the graph to compute largest distance in modulo scheduling, we only need the edge with the maximal $(min - II \cdot dif)$ after assigning II . Fortunately we don’t need to save all multiple edges, since the following theorem guarantees that we can compare $(min - II \cdot dif)$ before assigning different II s.

Theorem 5. Suppose $(min_1, dif_1), (min_2, dif_2)$ are two edges with $min_1 \leq 1, min_2 \leq 1$ and $dif_1 > dif_2$. Then for all $II \geq 1$, we have: $min_1 - II \cdot dif_1 \leq min_2 - II \cdot dif_2$.

This theorem allows us to sort multiple edges by lexical ordering of $(dif, -min)$ (i.e. compare dif first, and compare $-min$ if $dif_1 = dif_2$) and the smallest one is exactly the edge with maximal $(min - II \cdot dif)$.

4.2.2 Resource conflict handling. Another important issue when inserting an instruction into modulo scheduling table or merging two strong connected components is resource conflict: there is no dependency between two CZ gates, yet they may not be executed together because they may share a same qubit. To solve this issue, let us first introduce several notations:

```

for x=m to n do
  CNOT q1[x-50], q0[x+0];
  CNOT q1[x-50], q0[x+0];
end for
    
```

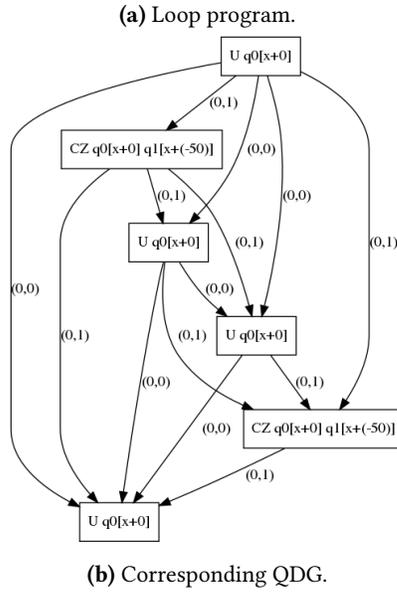


Figure 10. Quantum dependency graph example. Tuples represent (min, dif) .

1. II is the current iteration interval being tested.
2. L is the length of the original loop kernel.
3. The c -th instruction in the original loop is placed in the modulo scheduling table at tick $t = pII + q$, where $p \geq 0, 0 \leq q < II$.

Example 6. Figure 11 is a simple example for modulo scheduling. In this case, $II = 2$ and $L = 4$. Instructions are placed at time slot 0, 2, 3, 4. Thus, A from one iteration, B from a previous iteration, and D from previous 2 iterations are executed simultaneously, while C is executed alone.

We use the retrying scheme: if a resource conflict is detected, try next tick. The basic approach to detect resource conflict is detecting in-loop qubit aliasing. This leads to two new problems that do not exist in the classical case:

1. The array offsets of instruction operands may increase. As t increases, p also increase, and the instruction comes from one more iteration earlier, thus changing array offsets.
2. The pair of instructions for resource conflict checking may not both exist in some iterations. Increasing t leads to a long prologue and long epilogue, shrinking the range for loop kernel, and may eliminate the resource conflict that once existed (when the loop range is known).

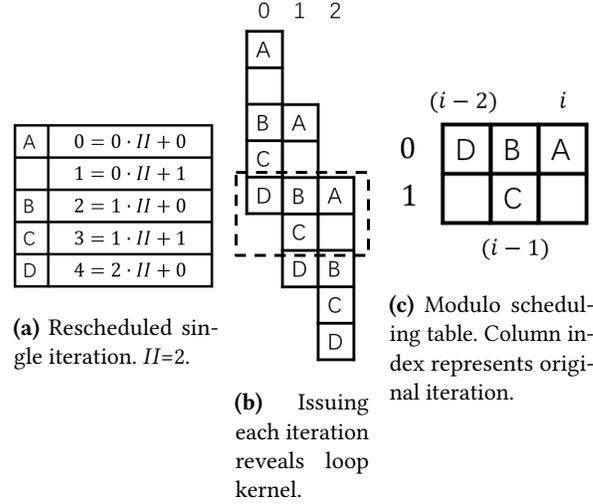


Figure 11. Example for modulo scheduling loop $A_i B_i C_i D_i$. In this case $II = 2, L = 4, T = [0, 2]$.

Example 7. Suppose when generating the schedule in Figure 11, we have inserted instructions A, B and C , and are ready to insert D at time slot 4.

1. Since $4 = 2II + 0$, the D in the loop kernel is from two iterations earlier compared with the iteration that the A is in. We have to decrease offset of D operands by $2i$. The offsetted index may no longer conflict with A .
2. When checking if there is resource conflict between D and A , we only need to check the case where both iterations are valid; that is, $i = 2$. This means the scheduling is still valid even if A_0 has a resource conflict with D_{-2} , since D_{-2} does not even exist.

In the original modulo scheduling and other classical scheduling algorithms, the retry strategy only allows II retries. For example, if there is not enough ALU or FPU for instruction A_i in modulo scheduling table tick q , there is also not enough resource for instruction A_{i-1} from previous iteration. However, this is not true for our case, and we have to modify the strategy.

Example 8. Suppose we perform modulo scheduling on the program in Figure 12. Since the three CZs are exactly the same, we may expect $II = 3$ due to resource conflict. However, if we allow more retries, these CZs can be separated into different iterations and can be executed concurrently with CZs from other iterations.

We consider the general case where loop range is unknown. When placing an instruction in the modulo scheduling table, we check its operands with all operands scheduled at this tick. Suppose now we check operand $(k_2(i-p_2)+b_2)$ with operand $(k_1(i-p_1)+b_1)$, and we find an aliasing, that is, $\exists i_0 \in \mathbb{Z}, k_2(i_0-p_2)+b_2 = k_1(i_0-p_1)+b_1$. In case $k_1 = k_2, \forall i \in \mathbb{Z}, k_2(i-p_2)+b_2 = k_1(i-p_1)+b_1$. When $k_1 = 0,$

```

for x=0 to 6 do
  CZ q[x], q[x+1];
  CZ q[x], q[x+1];
  CZ q[x], q[x+1];
end for

```

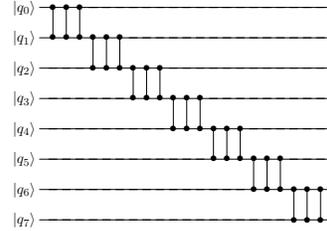
(a) Original Program.

```

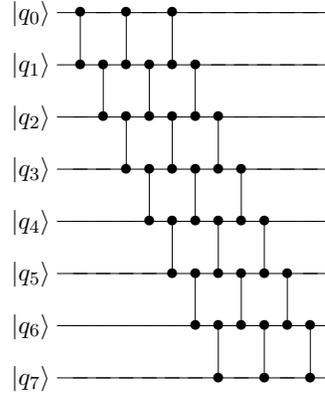
CZ q[0], q[1];
CZ q[1], q[2];
CZ q[0], q[1]; CZ q[2], q[3];
CZ q[1], q[2]; CZ q[3], q[4];
for x=4 to 6 parallel do
  CZ q[x-4], q[x-3];
  CZ q[x-2], q[x-1];
  CZ q[x], q[x+1];
end for
CZ q[3], q[4]; CZ q[5], q[6];
CZ q[4], q[5]; CZ q[6], q[7];
CZ q[5], q[6];
CZ q[6], q[7];

```

(c) Software pipelined version.



(b) Unrolled Program, for a clearer view.



(d) Software pipelined version, unrolled.

Figure 12. Three CZ gates in a row. Although there seems to be resource conflicts, the minimal $II = 1$.

this is the same as classical resource scheduling; otherwise, $\forall \Delta p \neq 0, \forall i \in \mathbb{Z}, k_2(i - p_2 - \Delta p) + b_2 \neq k_1(i - p_1) + b_1$. This means if we delay the instruction by $\Delta p II$ ticks, the conflict will be resolved. We call it **false conflict**. In case $k_1 \neq k_2$, after $\Delta p II$ ticks it will fall in the same time slot. There is still a conflict iff $\exists i_1 \in \mathbb{Z}, k_2(i_1 - p_2 - \Delta p) + b_2 = k_1(i_1 - p_1) + b_1$; that is, $i_1 = i_0 + \frac{\Delta p k_2}{k_2 - k_1}$, which means $(k_2 - k_1) | \Delta p k_2$. The conflict appears periodically as Δp increases. However, in the worst case where $(k_2 - k_1) | k_2$, there is always a conflict and can be seen as classical resource scheduling. We call it, together with the case where $k_1 = k_2 = 0$, **true conflict**.

We insert an instruction or an entire schedule into the modulo scheduling table in the following way: if there is no conflict, we insert the instructions; if there is only false conflict, we try next tick. As an exception, false conflicts between two single qubit gates are also seen as no conflict; and if there is true conflict, we start a “death countdown” before trying next tick: if next $(II - 1)$ retries do not succeed, give up, as we do in classical retry scheme.

4.2.3 Inversion pair correction. The commutativity between antidiagonal R_Z^+ gates and CZ gates comes at a price of a Z gate. In modulo scheduling stage we allowed them to commute freely, ignoring the generated Z gates. Now we have to fill them back to ensure equivalence. By the term

“inversion”, we mean that our scheduling alters the execution order of instructions **compared with original ordering**:

Definition 7. If the original c th instruction is modulo-scheduled at $t = pII + q$ in new loop (where the k th original loop is issued), we define the absolute order of the instruction to be $T = (k - p)L + c = kL + (c - pL)$.

Example 9. Suppose $L = 4$ and B in Figure 11 is the second instruction in the original loop ($c = 1$). B is placed in the modulo scheduling table at $p = 1$ and $q = 0$.

1. The first B instruction is issued in the prologue (incomplete loop kernel) where the second ($k = 1$) iteration is issued. Thus the absolute order of the instruction is $T = 1$.
2. The second B instruction is issued in the loop kernel where the third ($k = 2$) iteration is issued. Thus the absolute order is $T = 5$.
3. The third B instruction is issued in the epilogue (again incomplete loop kernel) where the fourth ($k = 3$) iteration is issued (or, should be issued). The absolute order is $T = 9$.

We see that the absolute order is exactly the time when the instruction is executed in the original loop.

Our idea is to check all inversion pairs in the modulo schedule. There are two kind of order-inversions:

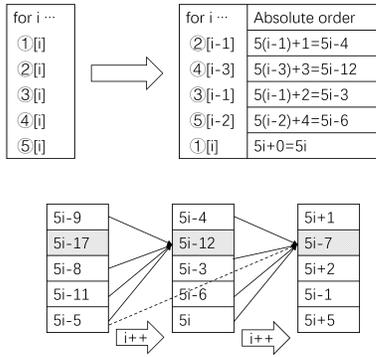


Figure 13. An example of inverted pairs of instructions across loop iterations.

- Definition 8.**
1. *In-loop inversion:* For two instructions in the k -iteration in new scheduling (i.e. the iteration where k th iteration of original loop is issued), if the first precedes the second while its absolute order succeeds the absolute order of the second instruction: $kL + (c_1 - p_1L) > kL + (c_2 - p_2L)$, there is an in-loop inversion.
 2. *Loop-carried inversion:* For two instructions in k -iteration and $(k + r)$ -iteration ($r \geq 1$), if $kL + (c_1 - p_1L) > (k + r)L + (c_2 - p_2L)$, there is an across-loop inversion.

Since the kL term can be cancelled, inversion pairs in modulo schedule also reveals periodicity. Figure 13 shows an example with periodic $r = 1$ inversions, and $r = 2$ inversions. Since the term $(k + r)L + (c_2 - p_2L)$ increases as r increases, there exists r_0 s.t. $\forall r > r_0$ there is no across-loop inversion. We can increase r and find pairs of inversion from iteration k and $(k + r)$, until there is no inversion pair. When finding all inversion pairs, we can check the pairs to see if one is CZ and the other is antidiagonal on one of CZ's operand. If so, we add a Z gate at the tick where CZ is placed.

4.2.4 Code generation for kernel, prologue and epilogue. We generate prologue and epilogue by removing non-existing instructions from the loop kernel.

Example 10. Consider in Figure 11 (remember $T = [0, 2]$), the iteration where k th original iteration is issued (or should be issued) by enumerating k from $-\infty$ to ∞ :

1. For $k < 0$, $\{k, k - 1, k - 2\} \cap T = \Phi$, no instruction is put.
2. For $k = 0$, $\{k, k - 1, k - 2\} \cap T = \{k\}$, only A is put.
3. For $k = 1$, $\{k, k - 1, k - 2\} \cap T = \{k, k - 1\}$, A, B, C are put.
4. For $k = 2$, $\{k, k - 1, k - 2\} \cap T = \{k, k - 1, k - 2\}$. This is the complete loop kernel.
5. For $k = 3$, $\{k, k - 1, k - 2\} \cap T = \{k - 1, k - 2\}$, B, C, D are put.
6. For $k = 4$, $\{k, k - 1, k - 2\} \cap T = \{k - 2\}$, D is put.

7. For $k > 4$, $\{k, k - 1, k - 2\} \cap T = \Phi$, no instruction is put.

For prologue and epilogue, we have to remove instructions from iterations that do not exist; for extra Z gates from the inversion of a CZ and an antidiagonal, removing either gate will make the Z gate disappear. After removing non-existing instructions, we perform compaction and ASAP schedule on the two parts.

For loop kernel, we need to merge the single qubit gates on the same qubit in the same time slot (from the resource conflict exception) by their absolute order.

4.3 Modulo scheduling again

In the first round of modulo scheduling, inversion of CZ and antidiagonal gates may introduce Z gates overlapping CZs, resulting an illegal schedule. To generate an executable schedule, we perform modulo scheduling again, but this time we no longer allow “commutativity” between antidiagonals and CZs, and thus the inversion-fix step can be skipped. The scheduled loop by this second round of modulo scheduling is directly executable on the device.

[An analysis on the complexity of our algorithm presented in this section is given in Appendix K.]

5 Evaluation

We have implemented our method and carried out experiments on several quantum programs. Some of them are intrinsically parallel, while others are not. Baselines for our evaluation come from the following sources:

- **Kernel-ASAP** performs compaction and ASAP scheduling on the loop kernel. We expect our work to outperform this naive approach.
- **Unroll** unrolls the loop and performs compaction as well as ASAP scheduling on the unrolled circuit. The software-pipelined version should generate a program with similar depth but much smaller code size.
- **Cirq** uses the optimization passes in [22] to unroll the loop. This gives another perspective of loop unrolling besides our implementation.

The experiment results are in Table 2. We hereby analyze some of the important examples:

5.1 Grover Search

Grover search is a test case with long dependency chain and little space for optimization. Yet our approach can reduce the overall depth by merging adjacent gates in iteration and across iterations. We use the CCNOT case from [6] and Sudoku solver from [4]. Since Grover search is a hard-to-optimize case, we inspected the optimized code and got the following findings:

Although examples do not reveal much optimization chance, there is a pitfall for ASAP optimizers that may cause a diagonal T^\dagger gate to be scheduled at the first tick alone. This

Test case	Input Loop			Output Loop			Known range results					
	ASAP	C	C-ASAP	Pre	K	Post	#Iter	K-ASAP	Unroll	Cirq	QSP#Iter	QSP
Cluster	4	2	5	4	1	4	200	800	203	203	96	104
Array 1	5	2	10	8	4	5	100	500	500	500	48	205
Array 2	3	2	5	4	1	4	100	300	201	201	46	54
Array 3	11	2	17	12	12	17	100	1100	605	606	48	605
Grover 1	13	2	26	26	24	871	99	1287	1287	1288	15	1257
Grover 2	71	2	141	141	135	40881	1000	71000	70001	71001	207	68967
QAOA-Hard 1	21	2	41	41	40	2021	1001	21021	20021	20021	449	20022
QAOA-Hard 2	21	2	41	41	40	2061	1001	21021	20021	20021	448	20022
QAOA-Hard 3	16	2	27	41	18	1121	1001	16016	11016	11016	448	9226
QAOA-Hard 4	33	2	47	60	31	3882	1000	33000	14019	14019	360	15102
QAOA-Par 1	15	2	26	46	20	943	201	3015	2215	2215	56	2109
QAOA-Par 2	15	2	26	45	20	1009	201	3015	2215	2215	53	2114
QAOA-Par 3	18	2	29	43	18	1080	201	3618	2218	2218	50	2023
QAOA-Par 4	15	2	29	29	25	3668	1000	15000	14001	14001	368	12897

Table 2. Evaluation results. ASAP is the minimal depth of original loop body. C-ASAP is the minimal depth of the original loop body unrolled by C times. Pre, K and Post represents prologue, kernel and epilogue. For each test case a range sized #Iter is assigned, and the span of the output loop is QSP#Iter.

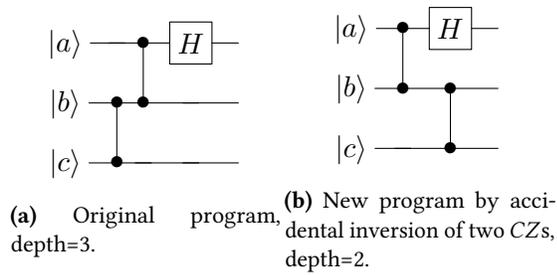


Figure 14. The accidental inversion of CZs reduced kernel depth by 1.

is prevented in our approach by performing bidirectional compactions. Moreover, the depth cut mainly comes from inversion of a pair of CZs while scheduling, which indeed our approach does not consider. (see Figure 14). This inspires us to find more optimization chances while placing instructions without dependency, like a program with many CZs.

5.2 QAOA

The QAOA programs in [8] (in Figure 15), as well as the QAOA example in [22] are used in our experiment, but with a p (i.e. the number of iterations) large enough. Since the decomposition of QAOA into gates affects how it can be optimized on our architecture, we consider two different ways: **QAOA-Par** where QAOA is decomposed to expose more commutativity (see the details in Appendix J), and **QAOA-Hard**, where QAOA is decomposed into a harder form, with a long dependency chain formed by cross-qubit operations that is unable to be detected by gate-level optimizers.

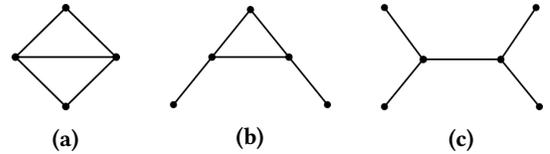


Figure 15. QAOA-MaxCut examples in [8].

The evaluation results in Table 2 show that in all cases, our approach can reduce the loop kernel size compared with **Kernel-ASAP**, and can sometimes outperform unrolling results. This advantage is more evident in the QAOA-Par cases than in the QAOA-Hard cases, since QAOA-Par reveals more commutativity chances than QAOA-Hard. Another finding is that QAOA-Hard generates larger code than QAOA-Par, and thus requires more iterations for software-pipelining to take effect.

[More discussions on examples are in Appendix M.]

6 Conclusion

We proposed a compilation flow for optimizing quantum programs with control flow of for-loops. In particular, data dependencies and resource dependencies are redefined to exposes more chances for optimization algorithms. Our approach is tested against several important quantum algorithms, revealing code-size advantages over the existing approaches while keeping depth advantage close to loop rolling. Yet there is still gap for optimization of more complex quantum programs, on different architectures, and with lower complexity, which could be filled in future works.

References

- [1] Alfred V. Aho, Monica S. Lam, Ravi Sethi, and Jeffrey D. Ullman. 2006. *Compilers: Principles, Techniques, and Tools (2nd Edition)*. Addison-Wesley Longman Publishing Co., Inc., USA.
- [2] Alexander Aiken and Alexandru Nicolau. 1988. *Optimal Loop Parallelization*. Technical Report. 308–317 pages. <https://doi.org/10.1145/53990.54021>
- [3] Vicki H. Allan, Reese B. Jones, Randall M. Lee, and Stephen J. Allan. 1995. Software Pipelining. *ACM Comput. Surv.* 27, 3 (1995), 367–432. <https://doi.org/10.1145/212094.212131>
- [4] Abraham Asfaw, Luciano Bello, Yael Ben-Haim, Sergey Bravyi, Nicholas Bronn, Lauren Capelluto, Almudena Carrera Vazquez, Jack Ceroni, Richard Chen, Albert Frisch, Jay Gambetta, Shelly Garion, Leron Gil, Salvador De La Puente Gonzalez, Francis Harkins, Takashi Imamichi, David McKay, Antonio Mezzacapo, Zlatko Minev, Ramis Movassagh, Giacomo Nannicini, Paul Nation, Anna Phan, Marco Pistotoia, Arthur Rattew, Joachim Schaefer, Javad Shabani, John Smolin, Kristan Temme, Madeleine Tod, Stephen Wood, and James Wootton. 2020. Learn Quantum Computation Using Qiskit. <http://community.qiskit.org/textbook>
- [5] Adi Botea, Akihiro Kishimoto, and Radu Marinescu. 2018. On the Complexity of Quantum Circuit Compilation. In *Proceedings of the Eleventh International Symposium on Combinatorial Search, SOCS 2018, Stockholm, Sweden - 14-15 July 2018*, Vadim Bulitko and Sabine Storandt (Eds.). AAAI Press, 138–142. <https://aaai.org/ocs/index.php/SOCS/SOCS18/paper/view/17959>
- [6] Patrick J. Coles, Stephan J. Eidenbenz, Scott Pakin, Adetokunbo Adeyoyin, John Ambrosiano, Petr M. Anisimov, William Casper, Gopinath Chennupati, Carleton Coffrin, Hristo Djidjev, David Gunter, Satish Karra, Nathan Lemons, Shizeng Lin, Andrey Y. Lokhov, Alexander Malyzhenkov, David Dennis Lee Mascarenas, Susan M. Mniszewski, Balu Nadiga, Dan O'Malley, Diane Oyen, Lakshman Prasad, Randy Roberts, Philip Romero, Nandakishore Santhi, Nikolai Sinitsyn, Pieter Swart, Marc Vuffray, Jim Wendelberger, Boram Yoon, Richard J. Zamora, and Wei Zhu. 2018. Quantum Algorithm Implementations for Beginners. CoRR abs/1804.03719 (2018). arXiv:1804.03719 <http://arxiv.org/abs/1804.03719>
- [7] Leonardo de Moura and Nikolaj Björner. 2008. Z3: An Efficient SMT Solver. In *Tools and Algorithms for the Construction and Analysis of Systems*, C. R. Ramakrishnan and Jakob Rehof (Eds.). Springer Berlin Heidelberg, Berlin, Heidelberg, 337–340.
- [8] Edward Farhi, Jeffrey Goldstone, and Sam Gutmann. 2014. A Quantum Approximate Optimization Algorithm. arXiv:quant-ph/1411.4028
- [9] Lov K. Grover. 1996. A Fast Quantum Mechanical Algorithm for Database Search. In *Proceedings of the Twenty-Eighth Annual ACM Symposium on Theory of Computing* (Philadelphia, Pennsylvania, USA) (STOC '96). Association for Computing Machinery, New York, NY, USA, 212–219. <https://doi.org/10.1145/237814.237866>
- [10] Gian Giacomo Guerreschi and Jongsoo Park. 2018. Two-step approach to scheduling quantum circuits. *Quantum Science and Technology* 3, 4 (Jul 2018), 045003. <https://doi.org/10.1088/2058-9565/aacfb0>
- [11] Ali JavadiAbhari, Shruti Patil, Daniel Kudrow, Jeff Heckey, Alexey Lvov, Frederic T. Chong, and Margaret Martonosi. 2015. ScaffCC: Scalable compilation and analysis of quantum programs. *Parallel Comput.* 45 (2015), 2–17. <https://doi.org/10.1016/j.parco.2014.12.001>
- [12] Monica S. Lam. 1988. Software Pipelining: An Effective Scheduling Technique for VLIW Machines. In *Proceedings of the ACM SIGPLAN'88 Conference on Programming Language Design and Implementation (PLDI), Atlanta, Georgia, USA, June 22-24, 1988*, Richard L. Wexelblat (Ed.). ACM, 318–328. <https://doi.org/10.1145/53990.54022>
- [13] Prakash Murali, David C. McKay, Margaret Martonosi, and Ali Javadi-Abhari. 2020. Software Mitigation of Crosstalk on Noisy Intermediate-Scale Quantum Computers. In *ASPLOS '20: Architectural Support for Programming Languages and Operating Systems, Lausanne, Switzerland, March 16-20, 2020 [ASPLOS 2020 was canceled because of COVID-19]*, James R. Larus, Luis Ceze, and Karin Strauss (Eds.). ACM, 1001–1016. <https://doi.org/10.1145/3373376.3378477>
- [14] Michael A. Nielsen and Isaac L. Chuang. 2011. *Quantum Computation and Quantum Information: 10th Anniversary Edition* (10th ed.). Cambridge University Press, USA.
- [15] Bill Pottenger. [n.d.]. *Loop Rotation*. <http://polaris.cs.uiuc.edu/projects/rec/node8.html>
- [16] Robert Raussendorf, Daniel E Browne, and Hans J Briegel. 2003. Measurement-based quantum computation on cluster states. *Physical review A* 68, 2 (2003), 022312.
- [17] Vivek V. Shende, Stephen S. Bullock, and Igor L. Markov. 2006. Synthesis of quantum-logic circuits. *IEEE Trans. on CAD of Integrated Circuits and Systems* 25, 6 (2006), 1000–1010. <https://doi.org/10.1109/TCAD.2005.855930>
- [18] Yunong Shi, Nelson Leung, Pranav Gokhale, Zane Rossi, David I. Schuster, Henry Hoffmann, and Frederic T. Chong. 2019. Optimized Compilation of Aggregated Instructions for Realistic Quantum Computers. In *Proceedings of the Twenty-Fourth International Conference on Architectural Support for Programming Languages and Operating Systems, ASPLOS 2019, Providence, RI, USA, April 13-17, 2019*, Iris Bahar, Maurice Herlihy, Emmett Witchel, and Alvin R. Lebeck (Eds.). ACM, 1031–1044. <https://doi.org/10.1145/3297858.3304018>
- [19] Seyon Sivarajah, Silas Dilkes, Alexander Cowtan, Will Simmons, Alec Edgington, and Ross Duncan. 2020. t|ket>: a retargetable compiler for NISQ devices. *Quantum Science and Technology* 6, 1 (nov 2020), 014003. <https://doi.org/10.1088/2058-9565/ab8e92>
- [20] Robert S. Smith, Michael J. Curtis, and William J. Zeng. 2016. A Practical Quantum Instruction Set Architecture. CoRR abs/1608.03355 (2016). arXiv:1608.03355 <http://arxiv.org/abs/1608.03355>
- [21] Bochen Tan and Jason Cong. 2020. Optimal Layout Synthesis for Quantum Computing. arXiv:cs.AR/2007.15671
- [22] Quantum AI team and collaborators. 2020. *Cirq*. <https://doi.org/10.5281/zenodo.4062499>
- [23] Qiskit Development Team. [n.d.]. *Qiskit Terra basic schedulers*. <https://qiskit.org/documentation/stubs/qiskit.scheduler.methods.basic.html#module-qiskit.scheduler.methods.basic>
- [24] Mingsheng Ying. 2009. Commutativity between CNOT and one-qubit gates (Unpublished notes). (2009).
- [25] Mingsheng Ying. 2016. *Foundations of Quantum Programming*. Morgan Kaufmann, Boston. <https://doi.org/10.1016/B978-0-12-802306-8.00002-1>

A Basic quantum gates

The following are the frequently-used one-qubit gates represented in 2×2 unitary matrices:

$$\text{Pauli gates : } X = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix},$$

$$Y = \begin{bmatrix} 0 & -i \\ i & 0 \end{bmatrix},$$

$$Z = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix},$$

$$\text{Hadamard gate : } H = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix},$$

$$\text{Phase and } \frac{\pi}{8} \text{ gates : } S = \begin{bmatrix} 1 & 0 \\ 0 & i \end{bmatrix},$$

$$T = \begin{bmatrix} 1 & 0 \\ 0 & e^{\frac{i\pi}{4}} \end{bmatrix},$$

$$\text{Pauli Rotations : } R_X(\alpha) = \begin{bmatrix} \cos \frac{\alpha}{2} & -i \sin \frac{\alpha}{2} \\ -i \sin \frac{\alpha}{2} & \cos \frac{\alpha}{2} \end{bmatrix},$$

$$R_Y(\alpha) = \begin{bmatrix} \cos \frac{\alpha}{2} & -\sin \frac{\alpha}{2} \\ \sin \frac{\alpha}{2} & \cos \frac{\alpha}{2} \end{bmatrix},$$

$$R_Z(\alpha) = \begin{bmatrix} e^{-\frac{i\alpha}{2}} & 0 \\ 0 & e^{\frac{i\alpha}{2}} \end{bmatrix}.$$

They combined with one of the (two-qubit) controlled gates

$$CNOT = \begin{bmatrix} 1 & & & \\ & 1 & & \\ & & 1 & \\ & & & 1 \end{bmatrix},$$

$$CZ = \begin{bmatrix} 1 & & & \\ & 1 & & \\ & & 1 & \\ & & & -1 \end{bmatrix}.$$

are universal for quantum computing; that is, they can be used to construct arbitrary quantum gate of any size.

Beside the above, we will use the following auxiliary gates to simplify the presentation of our approach:

$$R_X^-(\alpha) = \begin{bmatrix} \cos \frac{\theta}{2} & -i \sin \frac{\theta}{2} \\ i \sin \frac{\theta}{2} & -\cos \frac{\theta}{2} \end{bmatrix},$$

$$R_Z^+(\alpha) = \begin{bmatrix} 0 & e^{i\alpha/2} \\ e^{-i\alpha/2} & 0 \end{bmatrix} = XR_Z(\alpha),$$

$$H(\alpha) = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 1 \\ e^{i\alpha} & -e^{i\alpha} \end{bmatrix} = R_Z(\alpha)H,$$

$$H^-(\alpha) = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -1 \\ e^{i\alpha} & e^{i\alpha} \end{bmatrix} = R_Z(\alpha)HZ.$$

Note that parameter α in the above gates is a real number. The $R_Z^+(\alpha)$ gate can represent all single qubit gates that are anti-diagonal, i.e. only anti-diagonal entries are not 0. The other three notations are used in Appendix I.

For real-world quantum computers, a quantum device may only support a discrete or contiguous set of single qubit gates while keeping the device universal. For example, IBM's devices allow the following three kinds of single qubit gates to be executed directly[4]:

$$U_1(\lambda) = \begin{bmatrix} 1 & 0 \\ 0 & e^{i\lambda} \end{bmatrix},$$

$$U_2(\phi, \lambda) = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & -e^{i\lambda} \\ e^{i\phi} & e^{i\lambda+i\phi} \end{bmatrix},$$

$$U_3(\theta, \phi, \lambda) = \begin{bmatrix} \cos(\frac{\theta}{2}) & -e^{i\lambda} \sin(\frac{\theta}{2}) \\ e^{i\phi} \sin(\frac{\theta}{2}) & e^{i\lambda+i\phi} \cos(\frac{\theta}{2}) \end{bmatrix}$$

Note that $U_2(\phi, \lambda) = U_3(\frac{\pi}{2}, \phi, \lambda)$ and $U_1(\lambda) = U_3(0, 0, \lambda)$. Also note that gate U_3 itself is universal for single-qubit gates, and the main reasons for supporting U_1 and U_2 is to mitigate error, which is beyond our consideration.

B More Examples for quantum loop programs

We hereby presents more quantum algorithms that can be written into quantum loop programs and can thus be potentially optimized by our approach.

B.1 One-way quantum computing

Preparation circuit for simulating one-way quantum computation on quantum circuit is another example that allows each iteration to be performed on different qubits.

Example 11. *One-way quantum computing QC_C [16] is a quantum computing scheme that is quite different from the commonly used quantum-circuit based schemes. Instead of starting from $|0\rangle$, QC_C initializes all qubits (on a 2-dimensional qubit grid) in a highly-entangled state, called **cluster state**. After the preparation step, QC_C performs single-qubit measurements on all qubits and extract the computation result from these measurement outcomes.*

To simulate one-way quantum computing with quantum circuit, we first need to prepare the cluster state from $|0\rangle$. This can be done by first performing Hadamard gates on all qubits, then performing CZ gate on each pair of adjacent qubits on the qubit grid.

The preparation circuit can be written in a nested loop manner. If we assume the grid has a fixed width (3 in our case), we can unroll the innermost loop to get the flattened loop:

```

H[q[0]]
H[q[1]]
H[q[2]]
CZ[q[0], q[1]]
CZ[q[1], q[2]]
for i=1 to (L-1) do
  H[q[3i]]
  H[q[3i + 1]]
  H[q[3i + 2]]

```

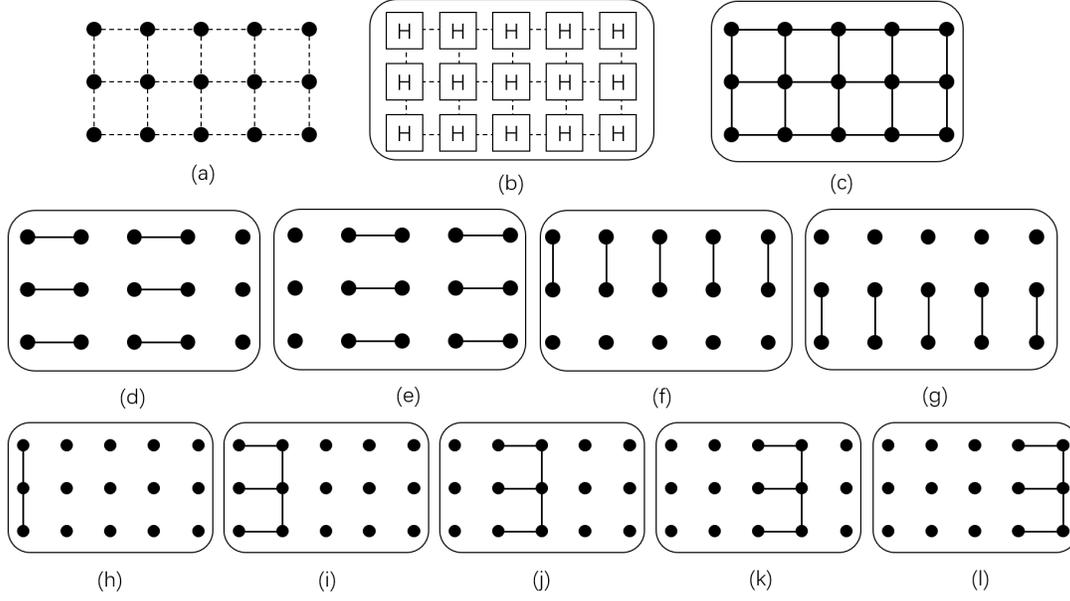



Figure 16. Converting cluster state preparation circuit into loop program. Fig (a) is a 3×5 two-dimensional qubit network. The preparation is done by performing a layer of Hadamard gates (Fig (b)) and a layer of CZ gates (Fig (c)). One way to perform those CZ gates without qubit conflict is to split them into four non-overlapping groups and execute each group separately, as in Fig (d) to Fig (g). The procedure can also be written into loop program, as in Fig (h) to Fig (l).

- The *expr* allows for more general indexing into qubit arrays and gate arrays. Note that the division and modulo operators are Euclidean, i.e. it always holds that

$$\begin{cases} \text{sign}(a \% b) = \text{sign}(b) \\ a \% b + (a/b) * b = a \end{cases} \quad (9)$$

D Solving Diophantine equations

In this appendix we focus on solving the Diophantine equation:

$$(k_2 - k_1)i + k_2(\Delta i) = b_1 - b_2, i \in T, i + \Delta i \in T, \Delta i \geq 1. \quad (10)$$

We rewrite it into:

$$ax + by = c, x \in T, x + y \in T, y \geq 1. \quad (11)$$

We recall the solutions S for linear Diophantine equations with two variables:

Lemma 1. Solutions for linear Diophantine equations with two variables

$$ax + by = c, x \in \mathbb{Z}, y \in \mathbb{Z}. \quad (12)$$

- If $a = 0$ and $b = 0$, $S = \Phi$ if $c \neq 0$ and $S = \mathbb{Z} \times \mathbb{Z}$ if $c = 0$.
- If $a = 0$ but $b \neq 0$ (similar for $b = 0$ but $a \neq 0$),
 - If $b|c$, $S = \mathbb{Z} \times \{\frac{c}{b}\}$.
 - Otherwise, $S = \Phi$.
- If $a \neq 0$ and $b \neq 0$:
 - If $c = d \cdot \text{gcd}(a, b)$,

- Special solution (x_0, y_0) where

$$ax_0 + by_0 = \text{gcd}(a, b) \quad (13)$$

can be solved using extended Euclidean algorithm.

- General solution $(k \frac{b}{\text{gcd}(a, b)}, -k \frac{a}{\text{gcd}(a, b)})$ for equation

$$ax + by = 0 \quad (14)$$

is known.

- The total solution space is

$$S = \left\{ \left(x_0 + k \frac{b}{\text{gcd}(a, b)}, y_0 - k \frac{a}{\text{gcd}(a, b)} \right) \mid k \in \mathbb{Z} \right\}. \quad (15)$$

We rewrite the equation into:

$$S = \{(x_0 + k\Delta x, y_0 + k\Delta y) \mid k \in \mathbb{Z}\}. \quad (16)$$

- Otherwise, $S = \Phi$.

For our original question with constraints, we only consider the cases where $a \neq 0$ and $b \neq 0$.

When $T = \mathbb{Z}$, the constraints no longer exist and we only need to find the minimal positive integer in set $\{y_0 + k\Delta y\}$, which can be solved by an Euclidean division. With loss of generality, we can just let $k = 0$ by choosing y_0 to be exactly the smallest positive integer in $\{y_0 + k\Delta y\}$ and adjust x_0 accordingly, without affecting the solution set S .

When $T = [a, b]$, the corresponding x_0 may not lie in T . In this case we may want to find a secondary-minimal positive integer. Without loss of generality we assume $\Delta y >$

0 (otherwise choose $\Delta x = -\Delta x$ and $\Delta y = -\Delta y$). Then the problem becomes: find minimal $k \in N_+$ s.t.

$$\begin{cases} x_0 + k\Delta x \geq a \\ x_0 + k\Delta x \leq b \end{cases}, \quad (17)$$

which is equivalent to

$$\begin{cases} k\Delta x \geq a - x_0 \\ k\Delta x \leq b - x_0 \end{cases} \quad (18)$$

which can thus be solved by a routine calculation: a minimal k exists, or does not exist at all.

E Proofs of Theorems 1 (CZ conjugation rules)

In this section we give out proof for our new rules of instruction data dependency. We will show that our definition of dependency is “sufficient and necessary” for quantum gate sets using CZ.

We first restate Theorem 1 as follows:

$$CZU_AU_B CZ = V_A V_B,$$

if and only if U_A and U_B are diagonal or anti-diagonal. That is, $U_i = R_Z(\theta)$ or $U_i = R_Z^+(\theta)$ for $i \in \{A, B\}$.

Proof. We here introduce our methodology of proving quantum gate algebra equations: first we give a necessary condition by trying several input states, and show that the condition is also sufficient for the equation to hold.

The first lemma is a criteria for deciding whether a state is separable or entangled:

Lemma 2. *Two-qubit state $|\psi\rangle = (a, b, c, d)^T$ is separable if and only if:*

$$ad - bc = 0. \quad (19)$$

Proof. (Necessity) If $|\psi\rangle$ is separable, there exists two single qubit states $|\psi_1\rangle$ and $|\psi_2\rangle$, s.t.

$$|\psi\rangle = |\psi_1\rangle \otimes |\psi_2\rangle \quad (20)$$

Suppose

$$|\psi_1\rangle = (\alpha_1, \beta_1)^T, \quad (21)$$

$$|\psi_2\rangle = (\alpha_2, \beta_2)^T, \quad (22)$$

We have

$$|\psi\rangle = (\alpha_1\alpha_2, \alpha_1\beta_2, \beta_1\alpha_2, \beta_1\beta_2)^T, \quad (23)$$

and it can be easily verified that $ad - bc = 0$.

(Sufficiency) If

$$|\psi\rangle = (a, b, c, d)^T \quad (24)$$

with $ad - bc = 0$,

1. If $b = 0$, this indicates $a = 0$ or $d = 0$. If $a = 0$, let

$$\begin{cases} |\psi_1\rangle = |1\rangle \\ |\psi_2\rangle = c|0\rangle + d|1\rangle \end{cases}; \quad (25)$$

otherwise $d = 0$, and let

$$\begin{cases} |\psi_1\rangle = a|0\rangle + c|1\rangle \\ |\psi_2\rangle = |0\rangle \end{cases}. \quad (26)$$

2. If $c = 0$, this indicates $a = 0$ or $d = 0$. If $a = 0$, let

$$\begin{cases} |\psi_1\rangle = b|0\rangle + d|1\rangle \\ |\psi_2\rangle = |1\rangle \end{cases}; \quad (27)$$

otherwise $d = 0$, and let

$$\begin{cases} |\psi_1\rangle = |0\rangle \\ |\psi_2\rangle = a|0\rangle + b|1\rangle \end{cases}. \quad (28)$$

3. Otherwise $a, b, c, d \neq 0$. Let

$$\begin{cases} |\psi_1\rangle = \left(\frac{b}{\sqrt{\|b\|^2 + \|d\|^2}}, \frac{d}{\sqrt{\|b\|^2 + \|d\|^2}} \right)^T \\ |\psi_2\rangle = \left(\frac{a}{b\sqrt{\|\frac{a}{b}\|^2 + \|1\|^2}}, \frac{1}{\sqrt{\|\frac{a}{b}\|^2 + \|1\|^2}} \right)^T \end{cases}. \quad (29)$$

It can be verified that $\| |\psi_1\rangle \| = \| |\psi_2\rangle \| = 1$, and that

$$|\psi_1\rangle \otimes |\psi_2\rangle = \frac{(a, b, c, d)^T}{\sqrt{(\|b\|^2 + \|d\|^2)(\|\frac{a}{b}\|^2 + \|1\|^2)}}, \quad (30)$$

which is exactly $(a, b, c, d)^T$ since tensor product preserves norm. \square

Lemma 3. (Necessity) *For the equation to hold, U_A and U_B have to be diagonal or anti-diagonal. This means U_i transforms $|0\rangle$ to $|0\rangle$ or $|1\rangle$, up to a global phase.*

Proof. Suppose $|\phi\rangle = U_A |0\rangle = (a, b)^T$, thus

$$CZU_AU_B CZ(|0\rangle \otimes (U_B^\dagger |\phi\rangle)) \quad (31)$$

$$= CZ |\phi\rangle \otimes |\phi\rangle \quad (32)$$

$$= (a^2, ab, ab, -b^2)^T, \quad (33)$$

which should be a separable state since this is also $V_A V_B(|0\rangle \otimes (U_B^\dagger |\phi\rangle))$, which is separable. Thus $a^2 b^2 = 0$, so $a = 0$ (R_Z^+ case) or $b = 0$ (R_Z case). This is the same for U_B . \square

Lemma 4. (Sufficiency) R_Z and R_Z^+ satisfies the conjugation rules.

Proof. Note that $R_Z^+ = XR_Z$ and $CZX_A = X_A Z_B CZ$. By simple computation we can see the conjugation holds. \square

F Proof of Theorem 3 (Convergence of compaction)

We show that compaction procedure will converge after applying the procedure three times.

If we look at the factors that prevents compaction procedure from reaching its fixpoint, there are two main reasons:

1. Single qubit merging results in new diagonal gates or antidiagonal gates, which is not recognized when the first gate is placed. Compacting #1 in Figure 7 shows an example where three gates merge into an antidiagonal X gate, which can merge through the CZ gate on next compaction.
2. Antidiagonal and CZ changing order will add Z gates to the circuit. Compacting #2 in Figure 7 shows an example.

Fortunately, these problems will not occur at the third time of compaction. This is because diagonal gates and antidiagonal gates forms a subgroup of U_2 :

Lemma 5. *Let*

$$G_Z = \{R_Z(\theta) | \theta \in [0, 2\pi)\}, \quad (34)$$

$$G_Z^+ = \{R_Z^+(\theta) | \theta \in [0, 2\pi)\}, \quad (35)$$

$$G = G_Z \cup G_Z^+, \quad (36)$$

thus G_Z, G are subgroups of U_2 , while $\forall g_1, g_2 \in G_Z^+, g_1 g_2 \in G_Z$.

Corollary 6. $\forall g_1 \in U_2 \setminus G, g_2 \in G, g_2 g_1 \in U_2 \setminus G$.

On #2 compaction, single qubit gates can only merge when they are on different sides of a CZ gate and one is diagonal or antidiagonal (otherwise they should have been merged on #1 compaction). According to corollary 6, this merging will not add new diagonals or antidiagonals, and all new gates from compaction #2 come from moving antidiagonal through CZ . The last compaction merges these additional Z gates to their left.

G Proof of Theorem 5 (Remove multiple edges)

In the QDG defined in Section 4, Theorem 5 is proposed so that multiple edges can be removed before II is assigned. The proof of Theorem 5 is listed below:

Proof. Since dif_1 and dif_2 are integers,

$$1 + dif_2 \leq dif_1, \quad (37)$$

Since $II \geq 1$,

$$-II \cdot dif_1 \leq -II - II \cdot dif_2 \leq -1 - II \cdot dif_2. \quad (38)$$

Since $min_1 \leq 1$ and $min_2 \leq 1$,

$$min_1 \leq min_2 + 1. \quad (39)$$

Adding up Equation 38 and 39 shows the result. \square

H Resource scheduling complexity analysis

In Secion IV we mentioned that we can keep retrying if there is a ‘‘resource conflict’’ and the death countdown is not timed-out (i.e. resource conflict are all caused by false conflicts), which may lead to too many retries that may dominate the complexity of the algorithm. This requires us to give an

upper bound of maximum number of retries to estimate the total complexity.

Recall how we perform resource checking when inserting instructions into the schedule:

- For every time slot, we have scheduled a bunch of instructions in this time slot.
- When adding an instruction or a group of instructions, we check the operands of each instruction to be added against instructions in the time slot where it will be added.
- If there is a resource conflict, we have to try next tick (and perhaps start a death countdown).

We first show that if there is only false conflict, the loop can be written into an equivalent form where all $k = 1$. In fact, this is achieved by the fact:

$$ki + b = k(i + (b/k)) + (b \bmod k), \quad (40)$$

where

$$(b \bmod k) \in [0, \|k\|), k(b/k) + (b \bmod k) = b. \quad (41)$$

According to this fact, the array can be split into $\|k\|$ slices, and resource conflict can occur if the two qubit references fall into the same slice. Figure 17 is an example for $k = 3$. Offsets $3i$ and $(3i - 1)$ will never conflict with each other, since they fall into different slices q_0 and q_2 .

This splitting allows us to use one integer $b' = (b/k)$ to represent an expression in the slice: in the Figure 17 case we can use 0 for $q[3i]$ in slice q_0 , 0 for $q[3i + 1]$ in slice q_1 , and (-1) for $q[3i - 1]$ in slice q_2 .

Corollary 7. *For the modulo scheduling, if a resource is scheduled II ticks later, the integer b' representing the resource decreases by 1.*

This allows to use a stricter model for upper-bound estimation:

- For the entire schedule, we use a universal set to store all integer representations $\{b'\}$ of linear expressions.
- When adding an instruction or a group of instructions, we check the operands to be added against the universal set, rather than the time-slot set. This means two instructions with the same operand but scheduled at different ticks will also be seen as conflicted.
- If the integer representation of operand is already in the set, there is a resource conflict. To find the worst case, we suppose the next $(II - 1)$ tries will definitely fail. The next retry that will possibly success is the II -th retry where the instruction is going to be placed in the same time slot again.
- The array index q and slice index $b \bmod k$ are ignored. For example, operands $q[3i]$ and $q[3i + 1]$ will be seen as conflicted since they have the same representation 0, even though the two expressions will never be equal to each other.

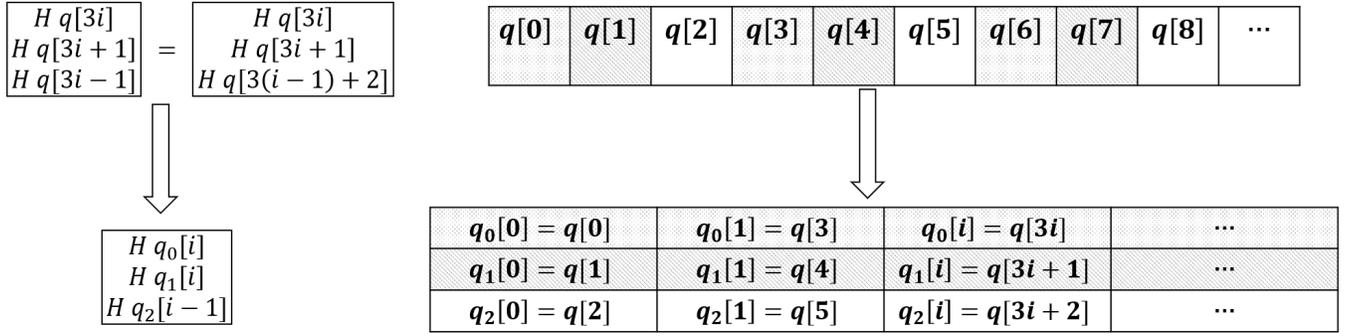


Figure 17. Example for splitting the qubit array when $k = 3$. Resource conflict can only occur inside each slice, and resources in each slice can be represented by one integer.

This strict set of rules reduces our upper bound problem to a clearer problem:

Theorem 8. For finite set $A \subset Z$ standing for resources (integers representing each resource) already scheduled, and $B \subset Z$ being resources to be scheduled. Define

$$B - (k \in N) = \{x - k | x \in B\} \quad (42)$$

to be the resource set of B after kII retries. Let k_{min} be the minimal k , s.t.

$$A \cap (B - k) = \Phi, \quad (43)$$

then $k_{min}II$ retries is required at most in our algorithm.

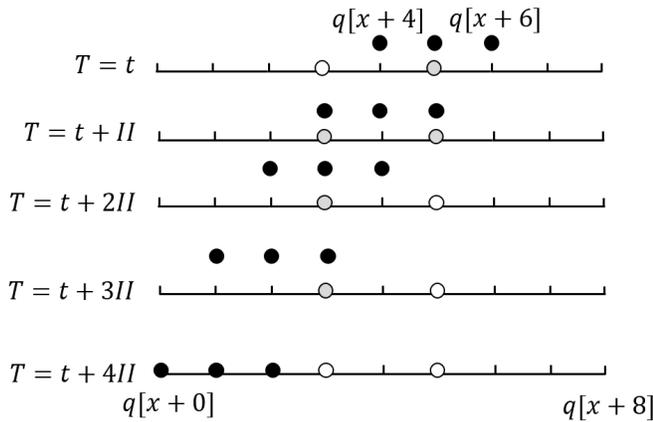


Figure 18. Resource $3(q[x+3])$ and $5(q[x+5])$ are now occupied, and resource 4 to 6 required to be scheduled. Now $k_{min} = 4$.

A naive estimation of k_{min} would be

$$k_{min} \leq \max(B) - \min(A), \quad (44)$$

which is not acceptable. Fortunately, we can give out a more precise estimation not in the values in A or B , but only in the size of sets.

Theorem 9. Let $\|S\|$ be size of set S ,

$$k_{min} \leq \|A\| \|B\|. \quad (45)$$

Proof. Consider the set

$$D = \{b - a | a \in A, b \in B, (b - a) \geq 0\}. \quad (46)$$

thus $k \notin D$ if and only if $A \cap (B - k) = \Phi$. Thus k_{min} is the first natural number not appearing in D . However, $\|D\| \leq \|A\| \|B\|$ according to its definition, so $k \leq \|A\| \|B\|$. \square

Corollary 10. Inserting m instructions at one time (e.g. merging to scheduled blocks) into a schedule with n instructions requires at most $O(mnII)$ retries. If each retry takes $O(mn)$ queries to find a conflict, the total complexity is at most $O(m^2 n^2 II)$.

According to the theorem, we can get some several important results on the complexity:

- Corollary 11.**
1. Inserting one instruction into the modulo scheduling table sized b requires $O(bII)$ retries and $O(b^2 II)$ time. Thus inserting all b instructions require $O(b^3 II)$ time.
 2. The span of the modulo scheduling table above is bounded by $O(b^2 II)$.
 3. Suppose the loop kernel sized n is split into $a \geq 2$ strong connected components sized b , the total complexity for scheduling all SCCs is $aO(b^3 II) = O(ab^3 II) = O(n^4)$, and the total time required to merge all SCCs together is

$$\sum_{i=1}^{a-1} O(b^2 (ib)^2 II) = O(a^3 b^4 II) = O(n^5). \quad (47)$$

4. The span of the total schedule is

$$aO(b^2 II) + \sum_{i=1}^{a-1} b(ib)II = O(ab^2 II + a^2 b^2 II) = O(n^2 II). \quad (48)$$

Thus we expect the length of prologue and epilogue to be

$$\sum_{i=1}^{O(n^2)} i \cdot II = O(n^3). \quad (49)$$

I CNOT conjugation rules

These results are taken directly from [24].

Theorem 12. (*CNOT conjugation*) *CNOT conjugates single qubit gates if and only if the conjugation satisfies one of the following eight cases:*

1.

$$\begin{array}{c} |a\rangle \\ |b\rangle \end{array} \begin{array}{c} \bullet \\ \oplus \end{array} \begin{array}{c} \bullet \\ \oplus \end{array} \begin{array}{c} R_Z(\alpha) \\ \\ \end{array} \begin{array}{c} \bullet \\ \oplus \end{array} \begin{array}{c} \bullet \\ \oplus \end{array} = \begin{array}{c} |a\rangle \\ |b\rangle \end{array} \begin{array}{c} R_Z(\alpha) \\ \\ \end{array} \quad (50)$$

2.

$$\begin{array}{c} |a\rangle \\ |b\rangle \end{array} \begin{array}{c} \bullet \\ \oplus \end{array} \begin{array}{c} \bullet \\ \oplus \end{array} \begin{array}{c} R_Z^+(\alpha) \\ \\ \end{array} \begin{array}{c} \bullet \\ \oplus \end{array} \begin{array}{c} \bullet \\ \oplus \end{array} = \begin{array}{c} |a\rangle \\ |b\rangle \end{array} \begin{array}{c} R_Z^+(\alpha) \\ X \end{array} \quad (51)$$

3.

$$\begin{array}{c} |a\rangle \\ |b\rangle \end{array} \begin{array}{c} \bullet \\ \oplus \end{array} \begin{array}{c} \bullet \\ \oplus \end{array} \begin{array}{c} R_X(\alpha) \\ \\ \end{array} \begin{array}{c} \bullet \\ \oplus \end{array} \begin{array}{c} \bullet \\ \oplus \end{array} = \begin{array}{c} |a\rangle \\ |b\rangle \end{array} \begin{array}{c} R_X(\alpha) \\ \\ \end{array} \quad (52)$$

4.

$$\begin{array}{c} |a\rangle \\ |b\rangle \end{array} \begin{array}{c} \bullet \\ \oplus \end{array} \begin{array}{c} \bullet \\ \oplus \end{array} \begin{array}{c} R_X^-(\alpha) \\ \\ \end{array} \begin{array}{c} \bullet \\ \oplus \end{array} \begin{array}{c} \bullet \\ \oplus \end{array} = \begin{array}{c} |a\rangle \\ |b\rangle \end{array} \begin{array}{c} Z \\ R_X^-(\alpha) \end{array} \quad (53)$$

5.

$$\begin{array}{c} |a\rangle \\ |b\rangle \end{array} \begin{array}{c} \oplus \\ \bullet \end{array} \begin{array}{c} \oplus \\ \bullet \end{array} \begin{array}{c} H(\alpha) \\ H(\beta)^\dagger \end{array} \begin{array}{c} \oplus \\ \bullet \end{array} \begin{array}{c} \oplus \\ \bullet \end{array} = \begin{array}{c} |a\rangle \\ |b\rangle \end{array} \begin{array}{c} H(\alpha) \\ H(\beta)^\dagger \end{array} \quad (54)$$

6.

$$\begin{array}{c} |a\rangle \\ |b\rangle \end{array} \begin{array}{c} \oplus \\ \bullet \end{array} \begin{array}{c} \oplus \\ \bullet \end{array} \begin{array}{c} H^-(\alpha) \\ H(\beta)^\dagger \end{array} \begin{array}{c} \oplus \\ \bullet \end{array} \begin{array}{c} \oplus \\ \bullet \end{array} = \begin{array}{c} |a\rangle \\ |b\rangle \end{array} \begin{array}{c} H^-(\alpha) \\ H(\beta + \pi)^\dagger \end{array} \quad (55)$$

7.

$$\begin{array}{c} |a\rangle \\ |b\rangle \end{array} \begin{array}{c} \oplus \\ \bullet \end{array} \begin{array}{c} \oplus \\ \bullet \end{array} \begin{array}{c} H(\alpha) \\ H^-(\beta)^\dagger \end{array} \begin{array}{c} \oplus \\ \bullet \end{array} \begin{array}{c} \oplus \\ \bullet \end{array} = \begin{array}{c} |a\rangle \\ |b\rangle \end{array} \begin{array}{c} H(\alpha + \pi) \\ H^-(\beta)^\dagger \end{array} \quad (56)$$

8.

$$\begin{array}{c} |a\rangle \\ |b\rangle \end{array} \begin{array}{c} \oplus \\ \bullet \end{array} \begin{array}{c} \oplus \\ \bullet \end{array} \begin{array}{c} H^-(\alpha) \\ H^-(\beta)^\dagger \end{array} \begin{array}{c} \oplus \\ \bullet \end{array} \begin{array}{c} \oplus \\ \bullet \end{array} = \begin{array}{c} |a\rangle \\ |b\rangle \end{array} \begin{array}{c} H^-(\alpha + \pi) \\ H^-(\beta + \pi)^\dagger \end{array} \quad (57)$$

It is easy to check that *CNOT* conjugation rules and *CZ* conjugation rules are equivalent to each other, by converting *CNOT* to *CZ* and vice versa.

J Parallel QAOA Decomposition

QAOA is one of the fashionable algorithms in NISQ era. We will use the QAOA program for solving MaxCut problems as our optimization test cases.

However, we face the problem of lacking commutativity when optimizing QAOA programs: our device can't execute $U(B, \beta_i)$ operation directly and it has to be decomposed into basic gates according to Equation 8, and the block-commutativity optimization chances by commutativity between $U(B, \beta_i)$ matrices are missed.

There have been different ways to optimize QAOA circuits with $U(B, \beta_i)$ commutable with each other in mind. For example, [18] detects all two-qubit diagonal structures in the circuit and aggregate them, so that commutativity detection can be performed on aggregated blocks. Another layout synthesis algorithm (scheduling considering device layout) QAOA-OLSQ[21] schedules QAOA circuits twice, the first time on a large granularity (named TB-OLSQ) and the second time on a small granularity (named OLSQ). The large-granularity pass allows block commutativity to be considered and gates are placed in blocks. The small-granularity pass finishes the scheduling.

However, these two approaches both require the optimization algorithm to perform coarse-grain block-level scheduling in addition to fine-grain gate-level scheduling. We may want to find another way to give commutativity hints to a gate-scheduling algorithm without modifying the algorithm itself.

Equation 8 inspires us with the fact that the shape of decomposed form of $U(B, \beta_i)$ is a bit like *CNOT* gate: it has a "controller" qubit and a "controlled" qubit; multiple blocks with the same "controller" qubit can be commuted and interleaved freely at gate level, and can be finished in 2 ticks on average instead of 3, as in Figure 19.

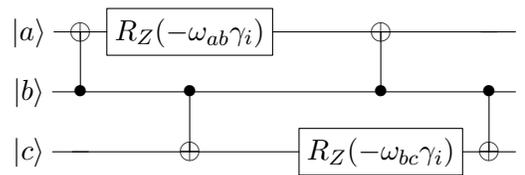


Figure 19. The two blocks can be executed interleavingly.

The level of "blocks" according to the discovery above can be derived by directing and coloring all edges in the undirected graph $G = \langle V, E \rangle$:

- First, we assign every edge with the direction in which we would perform the 8 decomposition (i.e. assign the graph with an orientation). Suppose the direction points from the controller qubit to the controlled qubit.
- Then, we colour all edges with minimal number of colours under the following constraints:

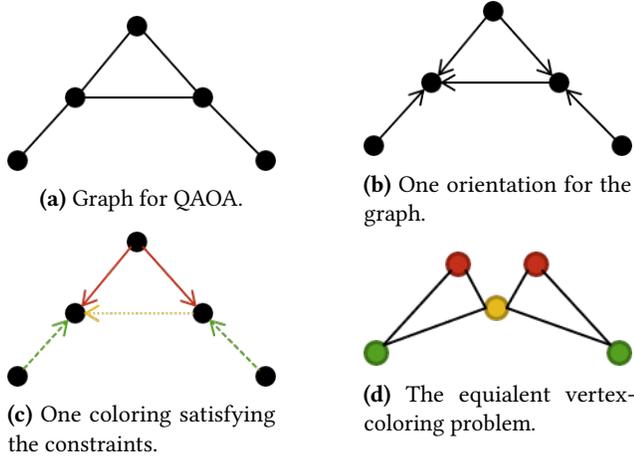


Figure 20. Example for one possible orientation and layering of a graph.

1. All in-degree edges of a vertex should be coloured differently from each other.
2. Out-degree edges of a vertex should be coloured differently from all in-degree edges of the vertex.

The minimal number of required colors over all possible orientations is the minimal number of layers we can put these gates into.

Note that finding the minimal edge colouring under the constraints can be reduced to the problem of finding minimal vertex colouring of a new graph. In the new graph, vertices represent original edges; vertices for out-degree edges are fully connected; vertices for in-degree edges are connected with those for out-degree edges. Figure 20 is an example of assigning directions and colours for edges in the graph, and the equivalent vertex-colouring problem to the edge-colouring one.

One direct way to compute the block placement strategy is to use an SMT solver, for example, QAOA – Par test cases in our evaluation are generated using Z3 Solver[7]. We leave it as an open problem whether there is an efficient approach.

K Complexity Analysis

In this section we give a rough estimation of complexity of the scheduling algorithm above. We put the main complexity results in table 3, with some notes below to explain.

K.1 Complexity of loop compaction

Complexity for compacting a piece of loop program sized $O(n)$ once is $O(n^2)$, since when adding every instruction we check it against all instructions that are previously added.

K.2 Complexity of loop unrolling

Finding merging or cancelling candidates requires $O(n^2)$ time. Suppose the loop range is unknown, we have to perform the following steps on C loops sized $m = O(Cn)$.

Step	Time	Code Size
Compaction	$O(n^2)$	$O(n)$
Unrolling	$O(n^2 + C^2n)$	C loops sized $O(Cn)$
For each loop sized $O(m)$		
Rotation	$O(m^3)$	$O(m^3)$
Try II	$O(\log m)$	-
Tarjan	$O(m^2)$	-
Floyd	$O(m^3)$	-
Scheduling	$O(m^5)$	Span= $O(m^3)$
Add Z	$O(m^4)$	-
Codegen	$O(m^6)$	$O(m^3)$
Total	$O(m^6)\log m$	$O(m^3)$
In Total		
Overall	$O(C^6n^6(\log Cn))$	$O(C^4n^3)$

Table 3. Complexity of our software pipelining approach.

K.3 Complexity of loop rotation

A loop sized $O(n)$ can be rotated for at most $O(n^2)$ times, since loop rotation will not introduce new “qubit” into the loop, and the $O(n)$ qubits can be placed in an partial order: $q_a < q_b$ if a single qubit gate on q_a will be on q_b after rotation.

This will create a prologue sized $O(n^2)$, an epilogue sized $O(n^3)$ and a new loop sized $O(n)$. Each rotation requires $O(n^2)$ time (to find a rotatable gate) so the total complexity is $O(n^4)$.

K.4 Complexity of modulo scheduling

We need $O(\log m)$ retries to binary-search the minimal II . Complexity of Tarjan algorithm on a dense graph is $O(m^2)$, and complexity of Floyd algorithm is $O(m^3)$.

We leave the proof of complexity from retrying due to resource conflict in Appendix H.

K.5 Inversion pair detection

The complexity for detecting in-loop inversion pair is $O(m^2)$. The complexity for detecting across-loop inversion depends on the span of the total schedule. Note that according to Definition 8:

$$r \leq (p_2 - p_1) + \frac{c_1 - c_1}{L}, \quad (58)$$

where $p_1, p_2 = O(m^2)$. Thus

$$r = O(m^2). \quad (59)$$

The total complexity of checking $O(m^2)$ pairs of instructions across r iterations is $O(m^4)$.

K.6 Code generation

The complexity for code generation is just the length of prologue and epilogue, $O(m^3)$. The compaction is of quadratic complexity so the total complexity is $O(m^6)$. However, for cases where the loop range is known, using a hash set to store

the last **operation** on each qubit can reduce the complexity to $O(m^3)$.

Theorem 13. *The total time complexity for our algorithm is*

$$O(C^6 n^6 (\log Cn)), \quad (60)$$

and the size of the generated code is

$$O(C^4 n^3). \quad (61)$$

L Adapting to existing architectures

Note that we are building our approach of optimization based on a specific quantum circuit model as specified in Section 2.2. Recall some of the features of the model that we use:

- Classical computation and loop guards can be carried out instantly.
- The hardware can execute arbitrary single qubit operations and CZ gates between arbitrary qubit pairs. All instructions can finish in one cycle.
- Instructions on totally different qubits can be carried out at the same time.

L.1 Powerful classical control

A quantum processor is usually split into classical part and quantum part, and all the classical logics (i.e. branch statements) are run on the classical part.

To implement fast classical guard for *for*-loops, we can use several classical architecture mechanisms, such as superscalar, classical branch prediction and speculative execution. As long as classical part commits instructions faster than quantum part executing instructions, we may keep the quantum part fully-loaded without introducing unnecessary bubbles.

If we want classical operations that affect the control flow of quantum part (e.g. classical branch statements), one way would be converting them to their quantum version. One practical example would be measurements with feedback: if we want to use the measurement outcome to control the following operations, we can just use a qubit array to replace classical memory, use $CNOT$ gate to replace measurement, and use controlled gate to replace classical control. The classical trick of register renaming can be adopted when converting measurement to quantum gates: different iterations can “measure to” different qubits to prevent unnecessary name dependency.

Also on real quantum processors the full-parallelism is not likely to be achieved, for example, there may be a limit of instruction issuing width on the device. For this case, we can just limit the maximal issuing width in resource conflict checking.

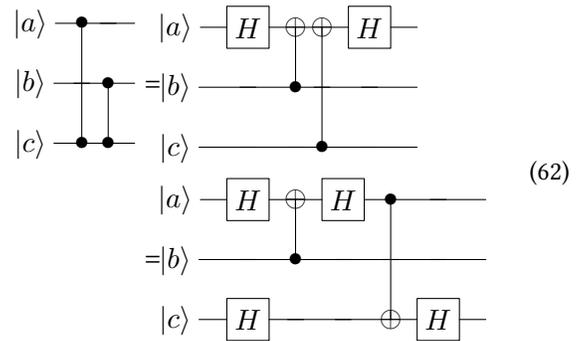
L.2 $CNOT$ -based instruction set

One major difference between our assumptions and the real-world architectures is that most existing models and architectures adopt a $CNOT$ -based instruction set, instead of a

CZ -based one. We provide two possible approaches for extending our method to the $CNOT$ -architecture case.

One approach is to convert the original circuit to CZ -version directly, using the equation $X[b]CZ[a, b]X[b] = CNOT[b]$. After optimization, an additional step is required to convert each CZ gate into $CNOT$ gates by adding Hadamard gates. Note that the way of adding Hadamard gates can affect the depth of the kernel.

Example 13. *Adding Hadamard gates on the same qubit of two adjacent CZ gates saves gate depth by 1, compared to the version adding Hadamard gates on different qubits of the two CZ gates.*



However, deciding all directions of $CNOT$ gates can be a hard problem. We can formulate the problem as an ILP problem. A rough description is as follows:

- Each CZ is given a boolean variable, indicating the direction of $CNOT$ (and where to add Hadamard gates).
- If one CZ is adjacent to a single qubit gate, the H can be absorbed.
- If one CZ is adjacent to another CZ and if they add Hadamard on the same qubit, the two Hadamard can be cancelled and no depth is added.
- Otherwise the depth is added by 1 from Hadamard. If there is an aliasing, the depth need to be added by more than 1 so that H gates on qubits with aliasing will be placed at two different ticks.
- The objective is to minimize the depth on all qubits.

We leave the best conversion from CZ program into $CNOT$ program with minimal depth as a remaining problem.

Another way to port our approach is to modify our QDG definition to the $CNOT$ -based instruction set. But in fact, the most commonly used $CNOT$ commutation rules that are based on intuition are only part of the complete $CNOT$ conjugation rules:

Lemma 6. (*$CNOT$ conjugation rules*)[24] *There are 8 rules in total for $CNOT$ conjugation rules, similar to CZ rules. See Appendix I.*

If we want to exploit full power of these rules, we have to consider all these rules while building QDG, instead of considering only the intuitive rules (usually the first 4 rules).

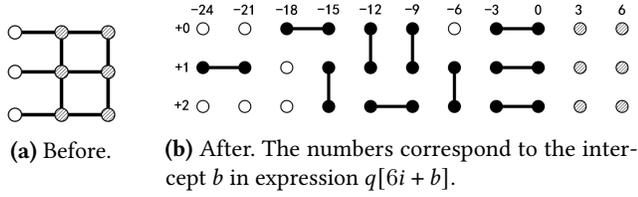


Figure 21. Loop kernel for cluster state preparation ($N = 3$). Shaded dots are qubits for Hadamard operands and closed dots are CZ operands.

But this time, the rewriting trick in Theorem 2 no longer works for *CNOT* rules. How to use these rules directly for QDG construction remains an open problem.

L.3 Working with device topology

One problem about a controlled-Z architecture is that it can be hard to perform long-distance CZ operation. For the *CNOT* case, a long distance *CNOT* gate with length k can be implemented using $(4k - 4)$ according to [17]. However, this is not true for CZ gates, as “amplitude” can’t propagate through CZ gates.

A direct conversion approach can be taken by converting CZ to *CNOT* and back forth. Since every *CNOT* is on critical path and no adjacent controlled bits can be found on critical path, this would require $(8k - 8 + 1) = (8k - 7)$ gates on critical path. The exception is $k = 2$, since the last *Hadamard* on the critical path should be removed and total depth is 8.

M Optimization of Cluster State Preparation, etc.

This chapter introduces the **Cluster** and **Array** test cases used in our evaluation.

Cluster is an example of cluster-state preparation program, which is a for-all loop: increasing count of iterations does not add to the overall depth of the program, which on the 2-dimensional grid is a constant 5 (4 for CZs in four directions and 1 for Hadamard). Despite that, we can still perform loop optimization on this program to get a loop with kernel sized 1.

For $C = 2$, the loop kernels before and after rotation followed by software-pipelining is given in Figure 21. Our approach split CZ gates that conflicts with each other into different iterations so that they can be executed together, and the kernel size is reduced to 1, the best result for any loop-optimization approach except fully-unrolling.

Array series are several artificially-crafted loop programs on qubit arrays. **Array 1** performs three CZ gates as in Figure 12, while two Hadamard gates are added between CZs to prevent cancellation. **Array 2** performs non-cancelling CZ gates so that they can be parallelized maximally. **Array 3** constructs a huge Toffoli gate using Toffoli gates and ancillas:

in each iteration, a Toffoli is performed on a source qubit, an ancilla and the next ancilla.

The instruction operands of these examples contain the iteration variable and are thus simpler to optimize compared with those on fixed set of qubits.