A novel single source three phase seven-level inverter topology for grid-tied photovoltaic application

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***Abstract*— This paper presents a novel single-source three-phase multilevel inverter structure with voltage boosting capability, which is suitable for medium-voltage photovoltaic (PV) applications. The proposed structure consists of switched-capacitors (SCs) based multilevel dc-link stages that boost-up the input DC-source voltage significantly. It reduces the dc-link voltage requirements by 75% compared to the traditional neutral point clamped (NPC), flying capacitors (FCs), active NPC (ANPC), hybrid and hybrid clamped ANPC and cascaded h-bridge (CHB) topologies, and 50% compared to advanced ANPC topologies. The proposed structure also reduces the number of required switches and capacitors as well as their voltages stresses compared to these state-of-the-art topologies. A robust control scheme based on finite control set model predictive control (FCS-MPC) is derived to control the converter. The capacitor voltage balancing is inherent of the proposed topology, and thus, eliminates the need for additional voltage balancing circuit and reduces the control complexity.**

Keywords— PV panel, multilevel inverter current, MPC controller.

I. INTRODUCTION

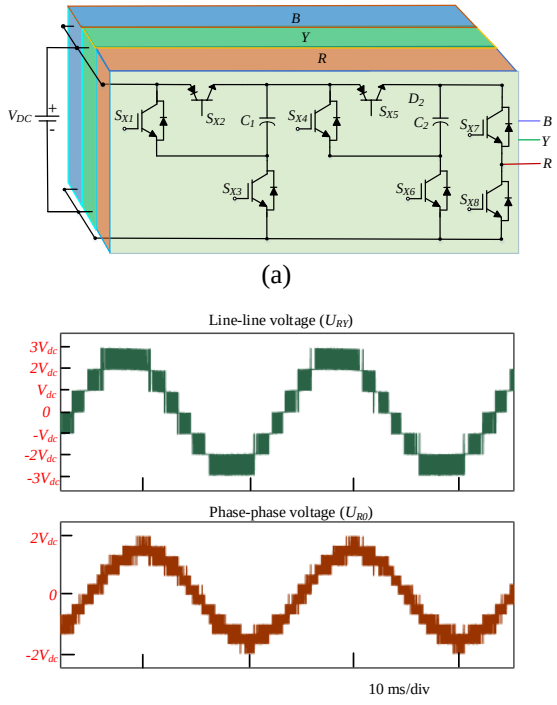
The key component used as an interface between renewable energy sources (RESs) like photovoltaic (PV) and power grid is the DC-AC voltage source inverters (VSIs). The PV panels can be directly connected to the VSIs or through a boost stage, which depends on the employed VSI topologies and the PV panel voltage level. For grid-connected applications, VSIs are responsible for dealing with increasingly stringent grid connection standards, power quality, reliability, and robustness as well as to perform other ancillary services. For residential and commercial applications, the common VSI structures usually used to interface RESs with the grid is the two-level VSIs. In recent years, multilevel inverters (MLIs) have received much attention over the two-level VSIs. They are potentially attractive and have been extensively used in a wide range of power conversion applications ranging from low to high voltage/power conversion systems, especially in renewable energy applications [1-3]. A higher number of output voltage levels enables higher quality output waveforms, which leads to reduced filter size, low electromagnetic compatibility (EMC), and low switching losses. Meanwhile, MLIs have less dv/dt stress on the semiconductor devices which enables the use of low-cost switching devices, and also increases their efficiency [4-6]. Many MLI structures have been reported in the literature with some basic concepts [1]. There are still newer structures are being presented and investigated in various applications.

The use of multiple converters as the front-end converter reduces the overall system efficiency and reliability. Moreover, it increases system cost, converter size, and control complexity. For PV applications, alternately, a series of PV panels can be employed to eliminate extra boost stage to provide the desired DC-link voltage levels. However, the series connection of PV panels can cause mismatch among the PV panels, which reduces the amount of energy extracted from the PV panels. Thus, a single-stage DC-AC inverter with voltage boosting capability can be an interesting way compared to a multi-stage power conversion system [7]. In this regard, a novel multilevel inverter topology is investigated, which is suitable for many applications like grid-connected renewable energy conversion system. The proposed topology reduces the number of active and passive components as well as their voltage stress, and the DC-link voltage requirement significantly.

This paper is organized as follows: Section II explains the proposed circuit structure and its prominent features. The proposed circuit operation modes and control strategy are described in Section III. Measurement results are provided in Section V for verification. Section VI summarizes key conclusions.

II. Circuit Structure and Operating Principle of the Novel Inverter

Fig. 1 illustrates the phase-leg of the proposed switched-capacitors (SCs) based three-phase multilevel inverter structure with voltage boosting capability. For the seven-level operation, this structure consists of eight active switches, two capacitors, and a single DC source. As depicted in Fig. 1, S_{X1}, S_{X2}, S_{X3}, …, S_{X8} (X ∈ (R, Y, B) phases) are the active switches, where two switches (S_{X2} and S_{X5}) are reverse blocking IGBT (RB-IGBT) and the other six switches are standard unipolar voltage devices (MOSFET/IGBT). Alternately, the employed two reverse blocking switches can be replaced by standard IGBT/MOSFET with a series diode. In the proposed structure, two switched capacitors (C_{X1} and C_{X2}) are incorporated with the input DC source to achieve a voltage gain of 3. In other words, the proposed structure is capable of generating up to $3V_{DC}$ at the output terminal (before the filter) with the input DC voltage magnitude. Nevertheless, it is also worthy to mention that the rated voltage of the capacitors is the same as the input DC voltage.



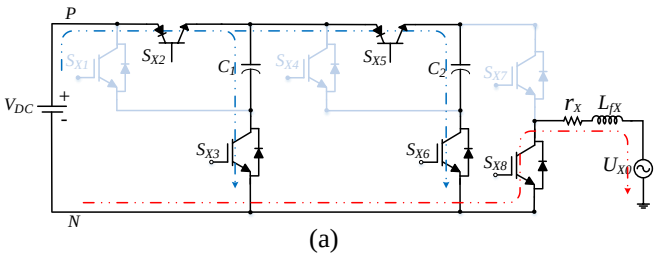
(a)

(b)

Fig. 1. Proposed three phase inverter: (a) circuit structure for seven-level operation, (b) output line voltage (U_{RY}), and phase voltage (U_{R0}).

The operation of the MLI consists of five switching states to generate one zero voltage and three positive voltage levels at the output of the converter. The MLI output voltage levels at different switching states and the charging states of the capacitors are presented in Table I, where U_{xo} denotes the output voltage of the converter, and output current is denoted as i_x. Considering the input DC supply voltage of V_{DC}, the switched capacitors (C_{X1} and C_{X2}) are charged to around V_{DC}.

Referring to Table I and Fig. 2, during 0 output voltage level, both the capacitors (C_{X1} and C_{X2}) are connected in parallel to the supply DC voltage and charged through the switches S_{X3} and S_{X6}, respectively, at an average of V_{DC}. In this state, the switch SX8 is turned on to create a zero-voltage switching state. Both the capacitors (C_{X1} and C_{X2}) are charged from the DC supply voltage in states A, and B, and discharged to generate the maximum voltage level in state E. To generate level 2, the reverse blocking IGBTs (S_{X2} and S_{X5}) and S_{X7} are conducted to directly connect to the DC-link voltage. There are two redundant switching states (C and D) to generate level 3. In state C, the series connection of the DC source and the capacitor C_{X1} results in its discharging. In this state, the parallel connection of C_{X2} with the series connection of C_{X1} and DC supply results in its charging. Secondly, in sate D, the capacitor C_{X1} is connected in parallel with the DC source and charges, and the series combination of DC supply and the capacitor C_{X2} generates the voltage level of 2 V_{DC}, which results in C_{X2} discharging. Also, notice that the time constant of the capacitor's charging paths is relatively small compared to the duration of different output voltage levels. As a result, the switched capacitors charge quickly.



(a)

TABLE I. Switching States of the Proposed Topology

Switching States	*Level*	U_{XO}	S_{X1}	S_{X2}	S_{X3}	S_{X4}	S_{X5}	S_{X6}	S_{X7}	S_{X8}	i_{C1}	i_{C2}	V_{C1}	V_{C2}
A	1	0	0	1	1	0	1	1	0	1	i_{c1f}	i_{c2f}	↑	↑
B	2	+ V_{dc}	0	1	1	0	1	1	1	0	i_{c1f}	i_{c2f}	↑	↑
C	3	+2V_{dc}	0	1	1	1	0	0	1	0	i_{c1f}	$-i_x$	↑	↓
D	4	+3V_{dc}	1	0	0	1	0	0	1	0	$-i_x$	$-i_x$	↓	↓

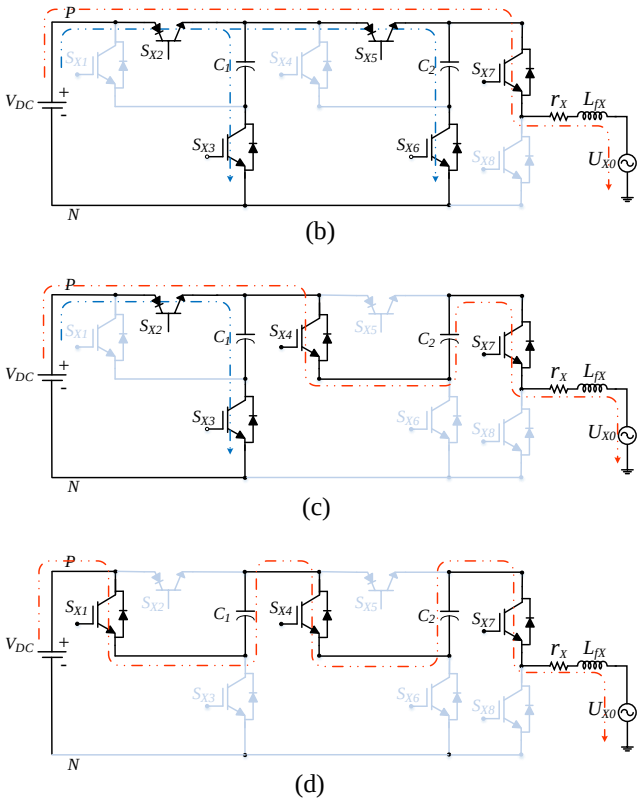


Fig. 2. Four switching states for the proposed inverter: (a) State A: 0, (b) State B: +1, (c) State C: +2, (d) State D: +3.

III. CONTROL STREATAGY

As shown in Fig. 1, the circuit is connected to the grid through an L-type filter with inductance *L*, and its equivalent series resistance is *R*. The input DC source voltage is represented by V_{DC}, which is employed to feed the inverter. Fig. 3 illustrates the switching states in *dq0* plane of the proposed three-phase four-level switched capacitor inverter. Based on the different switching combinations, one phase-leg in the structure can have four states: '0' state, '1' state, and '2' state, and '3' state.

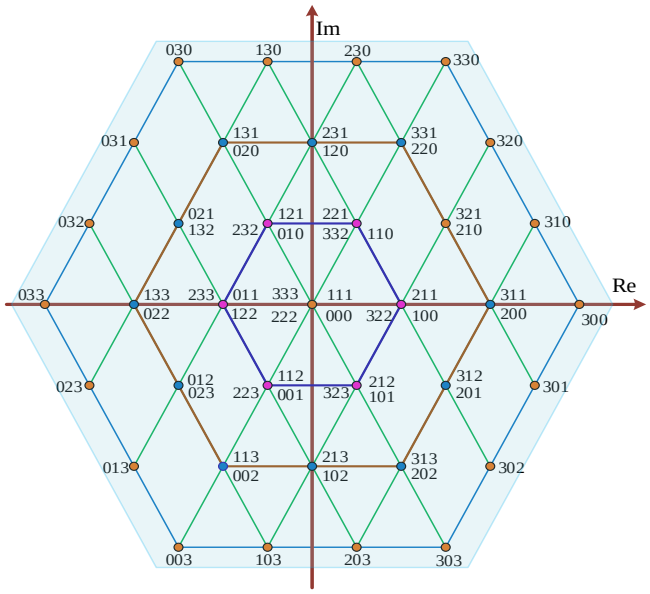


Fig. 3. Switching states in *dq0* plane.

The voltage vectors, converter current, and switching states of the converter can be described in the *αβ* frame given by (1), (2), and (3) respectively.

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \tag{1}$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{2}$$

$$\vec{S}_{\alpha\beta} = \begin{bmatrix} s_\alpha \\ s_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \tag{3}$$

The mathematical model (continuous time) of the three-phase inverter in the *abc* reference frame is given as (4)

$$\frac{d}{dt}\begin{bmatrix} i_{ga}(t) \\ i_{gb}(t) \\ i_{gc}(t) \end{bmatrix} = \begin{bmatrix} \frac{1}{L} & 0 & 0 \\ 0 & \frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{L} \end{bmatrix}\begin{bmatrix} v_{ga}(t) \\ v_{gb}(t) \\ v_{gc}(t) \end{bmatrix} - \begin{bmatrix} \frac{R}{L} & 0 & 0 \\ 0 & \frac{R}{L} & 0 \\ 0 & 0 & \frac{R}{L} \end{bmatrix}\begin{bmatrix} i_{ga}(t) \\ i_{gb}(t) \\ i_{gc}(t) \end{bmatrix} \tag{4}$$

where V_{ga}(t), V_{gb}(t), and V_{gc}(t) are the grid voltages of phase a, b, and c, respectively; i_a(t), i_b(t), and i_c(t) the output currents of phase a, b, and c, respectively.

The discrete time predictive model can be obtained by using Forward Euler's approximation method, as given below

$$\begin{bmatrix} i_{ga}^{k+1} \\ i_{gb}^{k+1} \\ i_{gc}^{k+1} \end{bmatrix} = \begin{bmatrix} 1-\frac{RT_s}{L} & 0 & 0 \\ 0 & 1-\frac{RT_s}{L} & 0 \\ 0 & 0 & 1-\frac{RT_s}{L} \end{bmatrix}\begin{bmatrix} i_{ga}^{k} \\ i_{gb}^{k} \\ i_{gc}^{k} \end{bmatrix} - \begin{bmatrix} \frac{T_s}{L} & 0 & 0 \\ 0 & \frac{T_s}{L} & 0 \\ 0 & 0 & \frac{T_s}{L} \end{bmatrix}\begin{bmatrix} v_{ga}^{k} \\ v_{gb}^{k} \\ v_{gc}^{k} \end{bmatrix} \tag{5}$$

The current dynamics can be represented in the *α-β* orthogonal coordinates as

$$\frac{d\vec{i}_{g,\alpha\beta}}{dt} = -\frac{R_s}{L_f}\vec{i}_{g,\alpha\beta} + \frac{1}{L_f}\vec{V}_{\alpha\beta} - \frac{1}{L_f}\vec{V}_{g,\alpha\beta} \tag{6}$$

where V_g,αβ and i_g,αβ are the grid voltage and current vectors, respectively.

The discrete-time model of the grid current at $(k+1)^{th}$ instant for a sample time Ts can be expressed as

$$\vec{i}_{g,\alpha\beta}^{\,k+1} = \frac{1}{R_s T_s + L_f}\left[L_f \vec{i}_{g,\alpha\beta}^{\,k} + T_s\left(\vec{V}_{\alpha\beta}^{\,k} - \vec{V}_{g,\alpha\beta}^{\,k}\right)\right] \tag{7}$$

Then, the active and reactive powers of this system can be calculated by (8), (9) accordingly.

$$P = \frac{3}{2}\mathrm{Re}\left(v_g i_g^*\right) = \frac{3}{2}\left(v_{g,\alpha} i_{g,\alpha} + v_{g,\beta} i_{g,\beta}\right) \tag{8}$$

$$Q = \frac{3}{2}\mathrm{Im}\left(v_g i_g^*\right) = \frac{3}{2}\left(v_{g,\beta} i_{g,\alpha} - v_{g,\alpha} i_{g,\beta}\right) \tag{9}$$

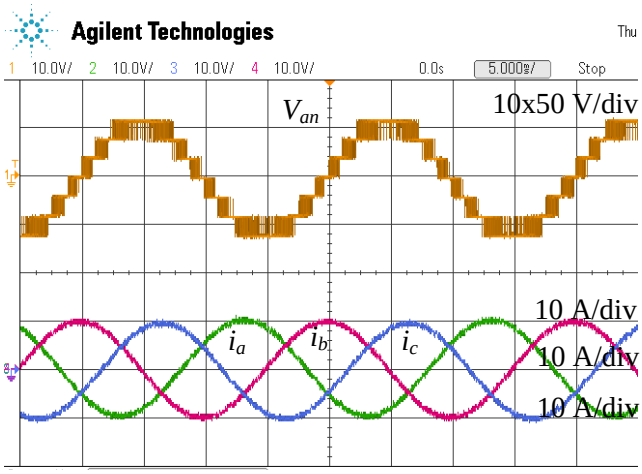
For the active and reactive power control, the cost function J can be defined as

$$J_{Cost.} = \sqrt{\frac{\left(P - P_{ref}\right)^2}{P_{ref}} + \frac{\left(Q - Q_{ref}\right)^2}{Q_{ref}}} \tag{10}$$

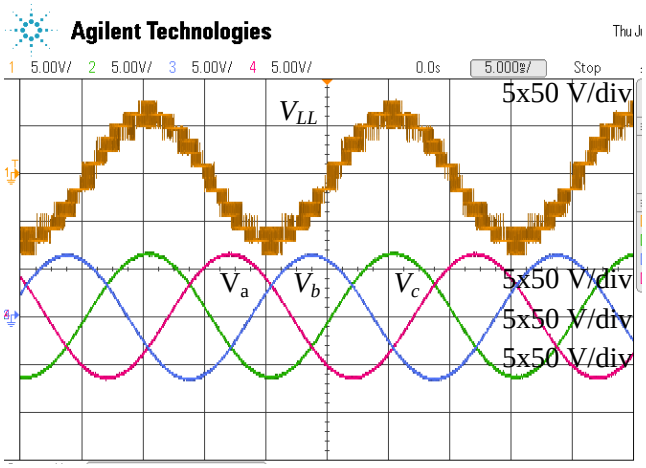
where P_{ref} and Q_{ref} are the active and reactive power references, respectively.

IV. Measurement Results

To validate the proposed converter circuit and the derived control algorithm, measurement studies have been carried out using MATLAB/Simulink with real-time results. Fig. 4 (a) shows the phase voltage and grid current waveforms. On the other hand, the line to line voltages with the grid voltages are shown in Fig. 4 (b). The voltage stress across the semiconductor switches are shown in Figs. 4 (c) and Figs. 4 (d). The measurement results show that the voltage stress across the switches (S_{X1}-S_{X5}, S_{X7}) does not exceed the DC input voltage. The maximum voltage stresses across the switch S_{X6} and S_{X8} are twice and third times of the input DC source voltage, respectively, which agrees the analysis presented in previous section. Fig. 4. Some waveforms of the proposed inverter: (a) Line voltage and grid currents, (b) phase voltage (before filter) and grid voltage, (c) voltage stress across the switches (S_{X1}-S_{X4}), and (d) voltage stress across the switches (S_{X5}-S_{X8}).



(a)



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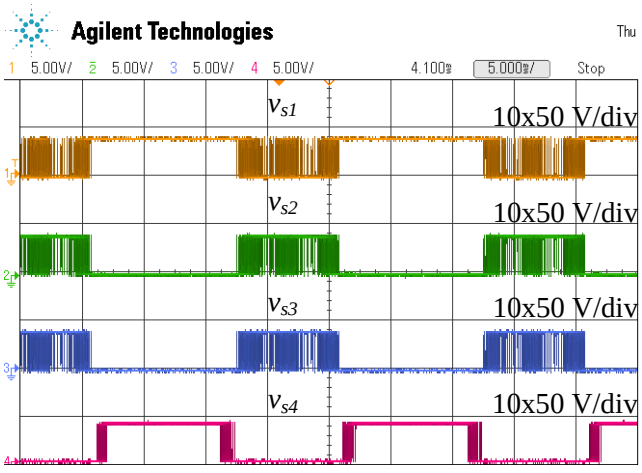
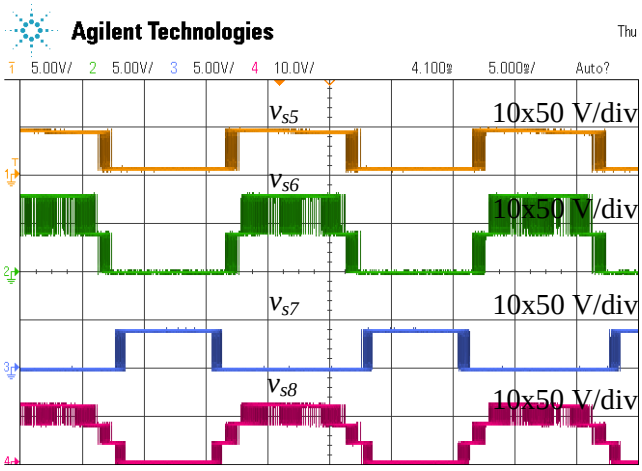


(c)



(d)

Fig. 4. Some waveforms of the proposed inverter: (a) Line voltage and grid currents, (b) phase voltage (before filter) and grid voltage, (c) voltage stress across the switches (S_{X1}-S_{X4}), and (d) voltage stress across the switches (S_{X5}-S_{X8}).

V. Conclusion

In this paper, a novel voltage boosting capability based three-phase switched capacitor multilevel inverter is proposed. To drive the converter, a finite control set model predictive control algorithm is derived. A cost function is formulated to operate at any power factor. It reduced voltage stresses across the switches and capacitors also reduce the system cost and converter size. Moreover, self-balanced capacitor voltages reduce the control complexity and additional sensor circuit requirement. The measurement results have validated the proposed topology and the associated control scheme.

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