A novel five-level switched capacitor type inverter topology for grid-tied photovoltaic application

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***Abstract*— This paper presents a novel five-level inverter topology and associated control scheme. The proposed structure consists of a capacitor, and eight active switching elements. It requires only one dc source and is capable of generating five voltage levels with double voltage boosting gain. On the other hand, it does not require any control scheme to balance the capacitor in the DC-bus due to inherent voltage balancing capability. As a result, the control complexity reduces a lot. Brief analysis followed by simulation and measurement results of a proposed 5-level inverter using the finite control set model predictive control (FCS-MPC) algorithm is presented. Detail of the analysis with more measurement result and comparison will be presented in the final paper.**

Keywords*— Photovoltaic system, FCS-MPC, Multilevel Inverter.

I. INTRODUCTION

Recently, multilevel inverters (MLIs) become popular in the industrial drives to use medium voltages to meet the high-power applications. Some of its advantages are: capable of synthesizing output voltages at more than two levels with the use of an array of semiconductor switches, low total harmonic distortion, low dv/dt stresses, mitigating electromagnetic interference, smaller or even no output filter is required and the average switching frequencies of the MLIs are much lower than those of the conventional two level inverters [1]-[2]. Besides these numerous advantages, the cost and size are still the main issue due to the high number of required semiconductor devices and control complexity with the increasing levels of output voltage [3]. The basic topologies of the existing MLIs are the cascaded multilevel inverter topology, the diode-clamped multilevel inverter topology, and the flying-capacitor multilevel inverter topology [4]-[6]. Among these topologies, the Cascaded Multilevel Converter (CMC) has attracted more attention due to its simple structure and individual DC power sources for each cascaded unit. However, CMC does suffer from requiring several isolated dc sources [2], [7]. Therefore, many topologies have been proposed to focus on single source with less required semiconductor devices and overcome this pressing issue [8]-[9]. Topologies with common-ground terminal significantly reduce the number of power devices, whilst nullifying the leakage current to the grid [2], [10]. Similarly, multilevel converters, which clamp the common mode voltage (CMV) during the freewheeling period, have received more attention in the recent time for medium power PV applications as they adopt the concept of common ground for effective elimination of leakage current. However, the requirement of high dc-link voltage (800 V) in same of the conventional multilevel converters (neutral-point-clamped (NPC), active NPC (ANPC) and T type [11]-[13] demand higher voltage boost converter at the front side. Inverter with integrated voltage boost capability has been alternatively seen as a potential candidate for PV applications due to its wide input voltage range.

This paper presents a switched capacitor type 5-level inverter, which uses a less number of semiconductor devices and has stepping-up feature suitable for PV applications. The paper is organized as follows. Section II shows the circuit configuration with operating principles. Section III explains the control strategy for the proposed topology. Section IV shows the comparison analysis of the proposed topology with existing topologies. Section V shows simulation waveforms in MATLAB-Simulink and the real time measurement results. The paper is summarized and concluded in Section VI.

II. CIRCUIT STRUCTURE AND OPERATING PRINCIPLE OF THE NOVEL FIVE-LEVEL INVERTER

The proposed inverter topology consists eight switches where six switches (S_11,S_14,and S_1-S_4) are unidirectional and other two is bidirectional, and a capacitor as shown in Fig. 1. The capacitor is used to attain different voltage levels by charging and discharging in predefined switching states. During the inverter's operation, the capacitor charges in zero state and discharges in 2nd level. The proposed inverter has five operating states as shown in Fig. 2. The status of the switches during each state and the corresponding output voltage is given in Table I. Each state will be described in the following subsections.

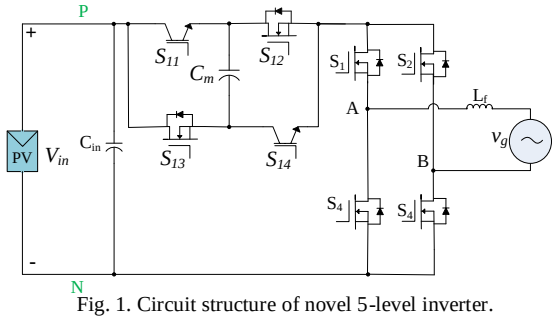


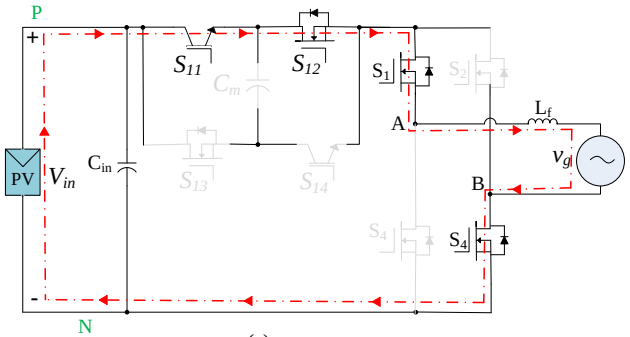
Fig. 1. Circuit structure of novel 5-level inverter.

State A, and B (±1 level):

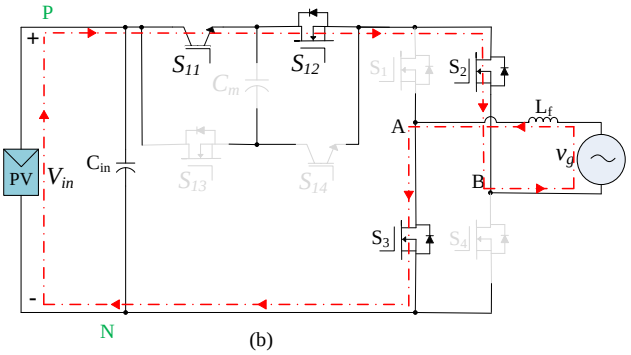
In the State A (see Fig. 2 (a)), the output of the inverter before the filter is + VPN. The grid current goes to the switches S_{11},S_{12},S_1 and S_4. However, in Fig. 2 (b) shows the State B where other two switches (S_2 and S_3) of the h-bridge are ON and the output of the inverter before the filter is - VPN.

State C,D (0 level):

The zero level shows in State C and D (see Fig. 2 (c) and Fig.2 (d)). The switches S_1 and S_3 are closed to form a bidirectional path for current flow during both the positive and negative cycle zero states. This leads to a zero voltage being applied before the output filter. The switches S_{11}, S_{14}, S_1 and anti-parallel diode of switch S_2 are ON during the positive half cycle while switches S_{11}, S_{14}, S_3 and anti-parallel diode of switch S_4 are ON for negative half cycle.



(a)



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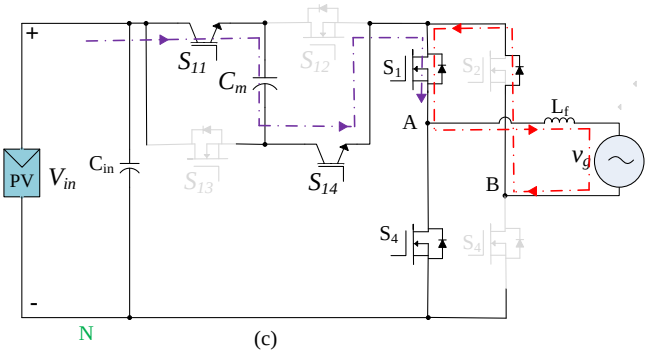

(c)

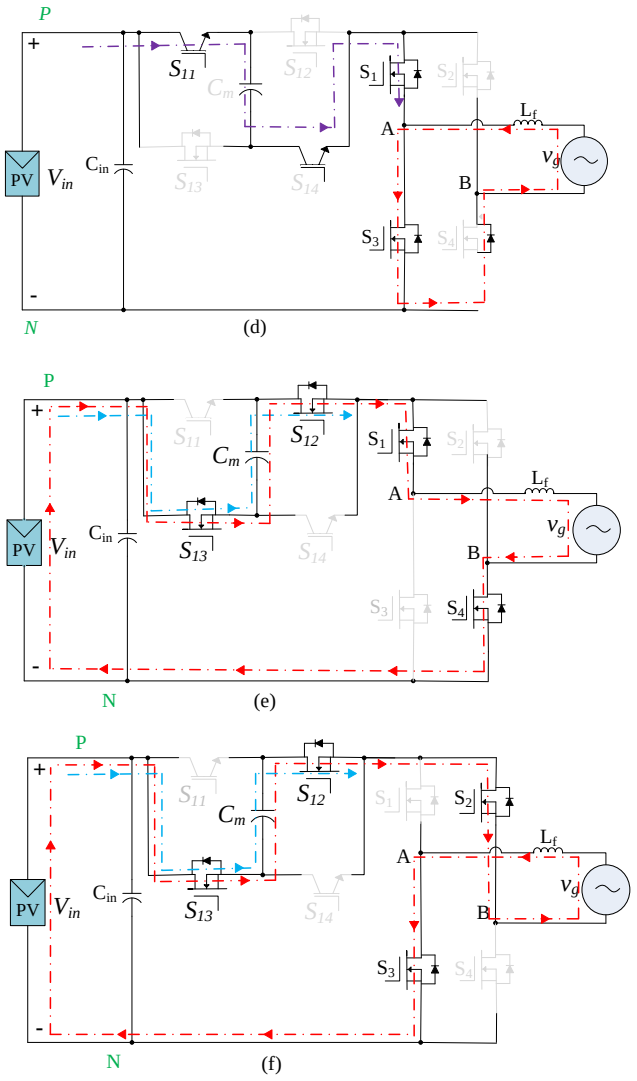

Fig. 2. Operation modes of proposed 5-level inverter: (a) Mode A ($+1\times V_{in}$), (b) Mode B ($-1\times V_{in}$), (c) Mode C ($+0\times V_{in}$), (d) Mode D ($-0\times V_{in}$), (e) Mode E ($+2\times V_{in}$), and (f) Mode F ($-2\times V_{in}$).

State E, F (±2 level):

Fig. 2(d) and Fig. 2(e) shows *State E*, and *State F* respectively. The capacitor C_m is discharged in series through the switches S_{12}, S_{13}, S_1 and S_4 for positive half cycle and output current flows through the same way to create positive two level (+ $2V_{PN}$). On the other hand, the capacitor C_m is discharged in series through the switches S_{13}, S_{12}, S_1 and S_4 for negative half cycle and output current flows through the same way to create negative two level (- $2V_{PN}$).

TABLE I
SWITCHING STATES OF THE PROPOSED TOPOLOGY

Mode	Switches								ψ	Output Voltage Level
	S_{11}	S_{12}	S_{13}	S_{14}	S_1	S_2	S_3	S_4		
A	1	1	0	0	1	0	0	1	1/2	+1
B	1	1	0	0	0	1	1	0	-1/2	−1
C	1	0	0	1	1	0	0	0	0	+0
D	1	0	0	1	0	1	0	0	0	−0
E	0	1	1	1	1	0	0	1	1	+2
F	0	1	1	1	0	1	1	0	-1	−2

III. CONTROL STRATEGY FOR PROPOSED TOPOLOGY

A finite control set model predictive control (FCS-MPC) algorithm is derived to drive the proposed multilevel converter. In the proposed control scheme, the predictive current control scheme is used. The proposed multilevel inverter can be modelled in the stationary reference frame as follows:

$$\frac{di_g(t)}{dt} = \frac{1}{L_f}\left(v_{AB}(t) - v_g(t) - i_{Lf}(t)R_{SR}\right) \quad (1)$$

$$v_{AB}(t) = \psi(t)v_{dc}(t) \quad (2)$$

where $i_g(t)$ is the grid current, i_{pc} represents the current at the point of common coupling, R_{SR} is the equivalent series resistance value of the L_f, $V_{AB}(t)$ is the input of the multilevel inverter, V_g(t) is the voltage at the point of common coupling, and $\psi(t)$ represents the control input obtained from the Table I.

By applying Euler forward method), the predictive values of the grid current can be expressed as follows:

$$i_g^{\,k+1} = i_K^{\,k} + \frac{T_s}{L_f}\left(v_{AB}^{\,k} - v_g^{\,k} - i_{Lf}^{\,k}R_{SR}\right) \quad (3)$$

Fig. 3 shows the block diagram of the diagram of the FSC-MPC control strategy with proposed topology where realize the desired active and reactive power with the proposed MLI during the grid-connected mode, the predictive grid current is calculated in terms of reference active and reactive power values.

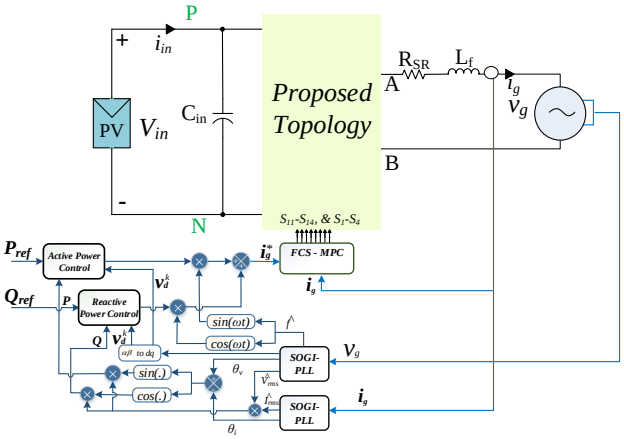

Fig. 3. The block diagram of the total control strategy with proposed topology.

The instantaneous active power value p^k and the instantaneous reactive power value q^k in a single-phase power system can be presented as follows:

$$\begin{bmatrix} p^k \\ q^k \end{bmatrix} = \frac{1}{2}\begin{bmatrix} v_{sd}^{\,k} & v_{sq}^{\,k} \\ v_{sq}^{\,k} & -v_{sd}^{\,k} \end{bmatrix}\begin{bmatrix} i_{sd}^{\,k} \\ i_{sq}^{\,k} \end{bmatrix} \quad (4)$$

where v_{sd}, v_{sq} are the *d*-axis and *q*-axis components of the power grid voltage v_s, and i_{sd} and i_{sq} are the *d*-axis and *q*-axis components of the grid current (i_s) in the *dq* rotating frame.

The utility voltage (v_s) is in phase with the *d*-axis component in synchronous reference frame. Therefore, p^k and q^k can be expressed as:

$$p^k = \frac{1}{2} v_{sd}{}^k i_{sd}{}^k \quad (5)$$

$$q^k = -\frac{1}{2} v_{sd}{}^k i_{sq}{}^k \quad (6)$$

Finally, by using (5) and (6), the current references can be expressed as:

$$i_g{}^k = \frac{2p^k}{v_{sd}{}^k}\sin(\theta) - \frac{2q^k}{v_{sd}{}^k}\cos(\theta) \quad (7)$$

The control objective of the proposed system is to inject the desired active and reactive powers into the grid. Based on the reference power values, the reference grid current is calculated from (7), where the value of the grid voltage angle is calculated from the phase-locked loop (PLL) algorithm.. In the proposed control scheme, the cost function formulation for the converter is given in the follow:.

$$g_{MLI.} = \left(i_g^{*k+1} - i_g{}^{k+1} \right)^2 \quad (8)$$

In contrast to the existing topologies, the proposed topology inherently overcomes the voltage unbalancing problems. Thus, it does not require any control scheme to generate balanced voltages in the DC link capacitors.

This cost function is valid for any number of voltage level generation with the proposed architecture. The proposed cost function does not include any weighting factor. Thus weighting factor tuning is not necessary for different operating conditions.Before you begin to format your paper, first write and save the content as a separate text file. Complete all content and organizational editing before formatting. Please note sections A-D below for more information on proofreading, spelling and grammar.

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IV. Comparison Analysis with Conventional Five-Level Topologies

Multilevel inverter is widely researched in both academia and industrial research institutes. However, the most challenging part is to reduce the number of semiconductor devices in the inverter topology to improve efficiency and power density. Table II illustrates the comparison of different single-phase multilevel inverter topologies in terms of the input voltage, Output voltage, power semiconductor devices, additional devices, boosting feature, required isolated DC source, and reactive power capability. The NPC inverter is constructed by eight power switches and four diodes to achieve five levels, while ANPC and T-type five-level inverter have no requirements of diodes. Instead, they require additional capacitors. Moreover, they require 2 V_PN input supply voltage to produce the 230 Vac RMS. DCC, FCC, and CMC use eight power switches; however, the DCC requires extra four capacitors and 12 diodes to achieve five levels in the output voltage. Moreover, CMC needs isolated DC sources. In summary, it is to be noted that the proposed topology needs only around 200 V dc-input voltage to obtain 230 V ac RMS. In addition, the required components for a 5-level inverter are one capacitor and eight power switches.

TABLE II.
COMPARISON TABLE OF EXISTING 1-Ø 5-L INVERTER TOPOLOGIES WITH PROPOSED TOPOLOGY

Topologies	Input voltage, (V_{in})	Output voltage, (V_{out})	Power devices		Additional devices		Step Up feature	Need isolated DC sources
			D	S	L	C		
Topology in [14]	V_{PN}	230/50 Hz	0	10	0	3	No	no
Topology in [15]	V_{PN}	230/50 Hz	0	10	0	3	Yes	no
Topology in [16]	V_{PN}	230/50 Hz	0	13	0	4	No	no
Topology in [17]	$\frac{V_{PN}}{2}$	220/50Hz	10	8	4	4	Yes	yes
Topology in [18]	V_{PN}	110/50 Hz	2	8	2	4	Yes	yes
Topology in [19]	V_{PN}	110/50 Hz	4	4	0	2	No	yes
Topology in [20]	V_{PN}	115/50 Hz	2	6	0	2	No	no
Topology in [21]	$\frac{V_{PN}}{2}$	120/60 Hz	3	8	2	4	Yes	yes
Proposed Inverter	$\frac{V_{PN}}{2}$	230/50 Hz	0	8	0	1	Yes	no

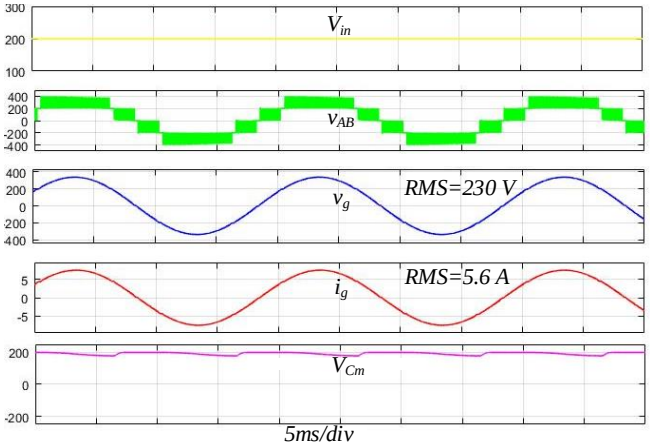
Note: D=diode, S=Switch, L=inductor, C= capacitor

V. Simulation and Measurement Results

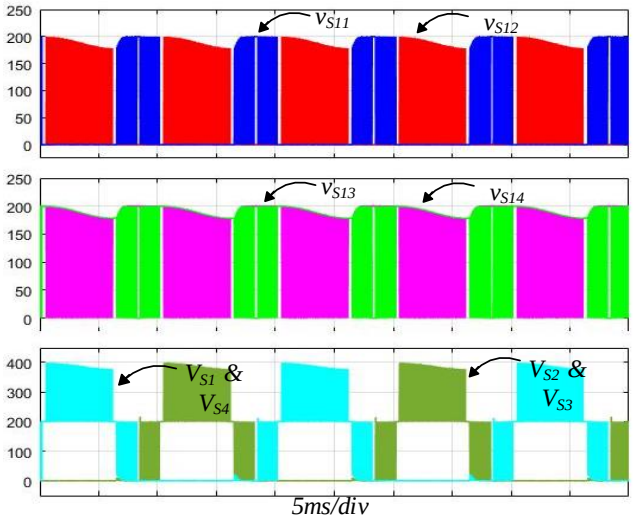
The proposed inverter is validated using a MATLAB simulation. Table III displays the list of components and parameters used for both simulations and measurements.

TABLE III.
PARAMETERS USED FOR SIMULATION AND EXPERIMENT.

Parameter	Value
Input Voltage (V_{in})	200 V-DC
Resistive Load	52 Ω
Output Voltage (V_{grid})	230 V AC
Line Frequency (f_g)	50 Hz
Output Current (i_o)	4.7 A
Modulation Index (M)	0.92
Rated Power	1 kW
Switching Frequency (f_{sw})	20 kHz
DC Bus Capacitor ($C_{dc1} = C_{dc2}$)	680 µF
Filter Capacitor (C_o)	2.2 µF
Filter Inductor (L_1, L_2)	2 mH



(a)



(b)

Fig.3. Simulated waveform of the proposed topology: (a) input and output waveforms, (b) voltage stress.

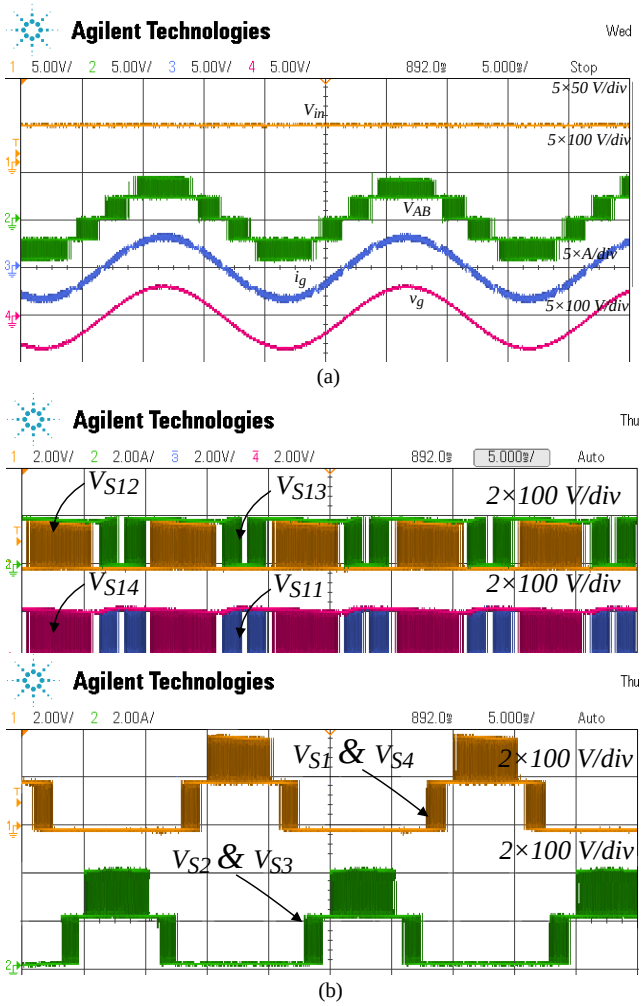


Fig. 4. Measurement results of the proposed topology: (a) input and output waveforms, (b) voltage stress

Fig. 3, and Fig. 4, show the waveforms of the proposed inverter with input voltage 200 V to obtain 230 Vac RMS as shown in Fig. 3(a). The 5L voltage is filter out by an L-type filter to get a pure sinusoidal voltage and current at the grid.

VI. Conclusion

A novel 5-level step up inverter for single-phase photovoltaic (PV) applications has presented with details control scheme. This topology does not require any control scheme to balance the series connected capacitor in the DC-bus due to inherent voltage balancing capability. Thus, it reduces the control complexity. Detailed analysis followed by simulation and real time measurement results of a proposed 5-level inverter by using the finite control set model predictive control (FCS-MPC) algorithm is presented.

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