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A new transformer-less step-up DC–DC converter with high voltage gain and reduced voltage stress on switched-capacitors and power switches for renewable energy source applications

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Abstract

In many modern applications such as renewable energy sources (RESs), DC–DC step-up converters can be used to regulate the input variable and/or low voltage to achieve the desired characteristics such as amplitude and ripples at the output voltage. This article proposes a new transformer-less step-up DC–DC converter which, compared to previously presented converter topologies in the same class, can provide a higher variable voltage conversion ratio besides benefits such as decreased voltage stress on the switched-capacitors and power switches. Since the proposed topology is expandable, it can generate much higher voltage conversion ratios with lower, non-extreme duty-cycles which can be provided by a simple and cheap control circuit. The aforementioned advantages make the converter a suitable candidate for numerous industrial applications such as RES applications. Besides the voltage regulation applications, the proposed converter can be employed to extract the maximum power from RESs such as photovoltaic panels. To prove the converter performance, comprehensive comparisons and experiments are performed.

1 | INTRODUCTION

Due to environmental concerns like global warming, increasing energy demand by consumers, and fossil fuel depletion, many countries have increased the share of renewable energy sources (RESs) in their power systems to supply the consumers. Because of the dependence of the output voltage of RESs like solar panels to the weather condition [1], it is necessary to regulate their output voltage. For the applications needing continuous and precise voltage regulation, one of the most popular option is to use the step-up/down DC–DC converters [2]. So far, many step-up/down converters such Zeta, Cuk, and Sepic structures have been introduced which are suitable for power applications [3]. But these converters have a serious drawback. They need an extreme value of duty-cycle to provide a high gain of voltage which in turn can decrease the efficiency, increase control system cost, cause malfunctions at high-frequencies [4]. As a solution, transformers can be used to increase the output voltage of these converters without using an extreme duty-cycle. However, using transformers has several drawbacks, making this solution unfavourable. First, by employing a large transformer turns ratio, the voltage stress on the primary elements will be increased which can remarkably reduce the efficiency of the whole system. Moreover, employing a transformer in the industry application where the DC isolation is not required will unfavourably increase the cost, volume, and losses of the conversion system. In addition, some of these converters like Zeta, due to their discontinuous input current, cannot be employed in the applications demanding the extraction of the maximum power from RESs like solar panels.

Up to now, several modified converters have been developed to solve the abovementioned drawbacks of the conventional structures. In [4], some modified hybrid DC–DC converter structures are presented which can provide required voltage gains by using more desirable values of duty-cycles. In [5], a modified Sepic topology is presented for renewable applications that provides higher voltage gain and efficiency compared to Sepic converter. In [6], a modified high gain DC–DC converter is introduced based on the conventional boost converter with a single switch. In [7, 8], two extendible topologies are introduced which are able to generate higher voltage gain than the conventional converters. However, these converters employ a large number of passive components, which are not desirable since it will cause increased cost and size for the converters. In [9],

a modified structure topology with high efficiency, high-gain, and low switching voltage stress is presented. In [10], a modified Cuk converter is developed to achieve decreased voltage drop and the parasitic effect of components. Besides, Kishore et al. developed a modified step-up/down topology based on the conventional Sepic converter with merits like higher voltage gain and lower components voltage stress compared to the conventional converter [11]. In [12], a high gain step-up non-isolated DC–DC Cuk-based converter is introduced which uses coupled inductor and voltage multiplier techniques. Due to the fact that the voltage stresses over the active switches are reduced in this converter, its magnetic devices have low volumes. In [13], a single-switch transformer-less buck-boost converter is developed. This converter is a common ground structure which can be used as a step-up or step-up/down converter to provide a quadratic voltage gain ratio without any complexity of magnetic utilizations. In [14], a semi-isolated high step-up converter with current-fed inputs is presented which can operate in both double- and single-input modes. The advantages of this structure are its high voltage gain, reduced number of power switches and improved efficiency. In [15], a high gain DC–DC converter is introduced consisting of capacitor-clamped circuits and coupled-inductor. This converter can be used to improve the voltage gain and achieve a continuous input current. In [16], a step-up DC–DC converter is developed for RES applications. This converter has a high-power density and provides benefits such as high voltage gain, recycled energy of leakage inductor, lower voltage stress on switches, and eliminated inrush current.

Switched-capacitor (SC) topologies are also one of the most popular types of DC–DC converters used in a wide range of applications [17, 18]. These converters' operation principles are the same, including two modes of charging and discharging for a group of interconnected capacitors. Many SC topologies have been developed and presented for various industrial applications [19]. Generally, the most popular conventional SC converters are charge pump type multilevel modular, Marx generator type voltage multiplier, and generalized multilevel type structures [20]. These topologies suffer from serious drawbacks such as remarkable switching losses and large size [21]. In [22], Abbasi et al. developed a new step-up SC structure providing many merits such as decreased cost, reduced control complexity, fewer components, less voltage stress on components, and smaller size over conventional structures. In [23], a bidirectional DC–DC topology is developed based on SC concept which provides advantages like higher voltage conversion ratio, lower component power rating, fewer number of power switches, and lower output capacitance ratings. In [24], an SC-based multilevel DC–DC power conversion system is presented which consists of multiple DC sources. By using this structure, changing the output voltage continuously is made possible. Besides, this system is a suitable candidate for high-temperature operations. In [25], a set of single-phase pulse-width modulation Sepic converters are developed based on conventional Sepic rectifier, three-state switch, and SC concepts. This set can provide benefits such as lower voltage stress on switches, higher output voltage, and a split-capacitor output voltage.

In 2019, a new type of step-up/down converter was introduced in [26–28] that can provide higher voltage gains by lower duty-cycles in comparison to other converters. In [26], a new family of non-isolated step-up/down and step-up converters is developed which are either hybrid or non-hybrid structures. In [27], new converter topologies are introduced which employ a fewer number of power switches compared to the converters presented in [27, 28]. Among these converters, the converter presented in [28] employs the highest number of power switches. The aforementioned converters impose lower voltage stresses on capacitors as compared with conventional topologies. Besides, these converters are developed based on two conventional structures, i.e., Zeta and Cuk converters. Generally, Zeta converter and the Zeta-based converters of [18–20] are not capable of extracting the maximum power from power generation devices such as PV panels. Hence, the Zeta-based converters are not suitable candidates for such applications. In [29], a high-gain step-up scalable voltage multiple cell-based DC–DC topology for offshore wind farms is introduced that has several features such as low and adjustable stresses on the components and automatic input-current sharing in each input phase. In [30], a step-up/down DC–DC converter is designed and introduced based on SC cells to increase the low voltage of RES to a relatively high bus voltage. Providing a high gain of voltage, a continuous input current, and also the possibility of maximum power point tracking are three of the most important advantages of this topology.

In this paper, a new step-up SC DC–DC converter is proposed. Due to multiple SC cells employed in the proposed converter, this converter can generate higher voltage conversion ratios by using lower duty-cycle and imposing lower voltage stress on its components, compared to the previously introduced DC–DC topologies. This makes the proposed topology suitable for applications with high power and/or voltage ratings, such as output voltage regulation of RESs. Unlike other step-up/down converters such as conventional Zeta and buck-boost converters, and Zeta-based SC converters of [26–28], the proposed converter can be used for maximum power extraction in RESs like solar panels. To validate the analysis, thorough comparisons, discussions, and experiments are conducted and presented.

2 | PROPOSED TRANSFORMER-LESS SC-BASED CONVERTER

In this section, the proposed SC converter topology, its operating principles, mathematical model, and efficiency analysis including the voltage stress on the components are given in the following three sub-sections.

2.1 | Proposed topology

Figure 1a presents the proposed converter structure that includes one DC voltage source (V_{in}), one output capacitor C_f, one charging capacitors C_c, N SCs (C_1, …, C_N), one inductor

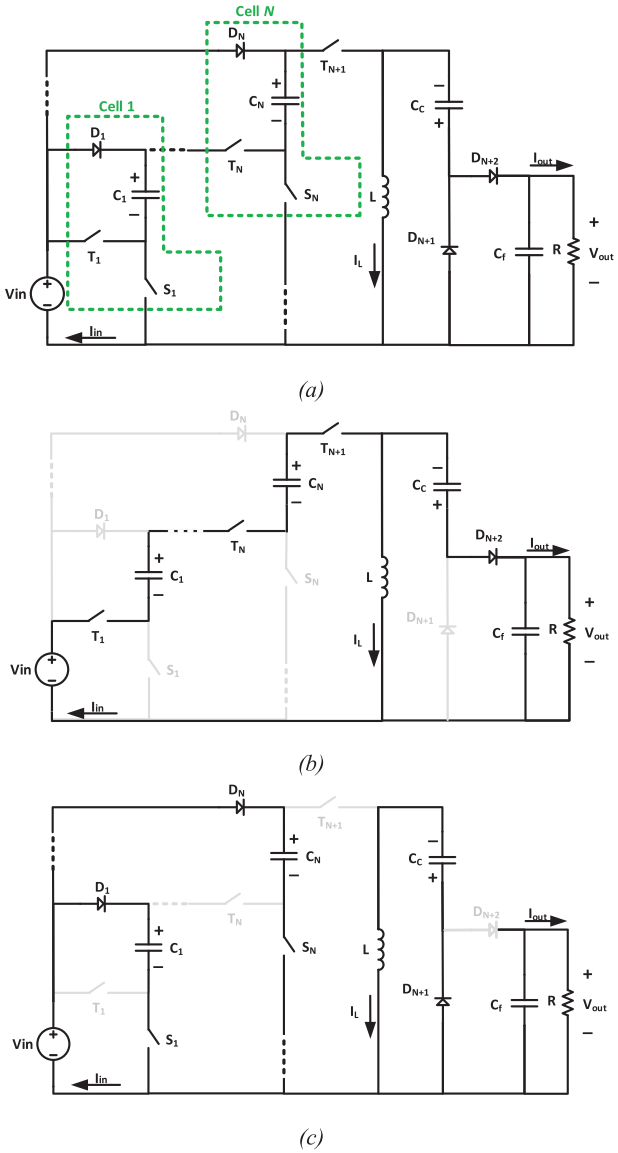

FIGURE 1 (a) Proposed converter and its operational (b) mode 1 (c) mode 2

(L), one pure-resistive load (R), ($2N$+1) switches (T_1, …, T_{N+1} and S_1, …, S_N), and (N+2) diodes (D_1, …, D_{N+2}). As seen, the proposed converter consists of several SC cells; each cell includes one diode, two switches, and one capacitor. In the following, the operating principles and the mathematical analysis of the proposed topology are presented in detail.

2.2 | Operating principles and mathematical model

Here, the operating principles, mathematical model and the sizing of the components of the proposed converter are discussed and presented. Two operational modes of the proposed converter are shown in Figure 1b, c. As seen in the first mode, since the T switches and D_{N+2} are ON, all of the capacitors are discharged while the inductor is charged. In mode 2, the inductor L is discharged into the capacitor C_C. Also, SCs are in the charging mode since the S switches are conducting. Table 1 summarizes the operational characteristics of the converter. It should be noted here that there is not any dead-time for the input current of the proposed converter since the input voltage source contributes to charging the passive components of the circuit in both modes. As seen in Figure 1b, the input source beside SCs charges the inductor L. Also, in the second operating mode shown in Figure 1c, the voltage source is parallel with SCs and charges these capacitors.

TABLE 1 The operational characteristics of the proposed DC–DC topology

Mode	Switching states: Switches		Switching states: Diodes		Charging (↑) and discharging (↓) states		
	T_1, …, T_{N+1}	S_1, …, S_N	D_1, …, D_{N+1}	D_{N+2}	C_1, …, C_N	C_c	L
1	1	0	0	1	↓	↓	↑
2	0	1	1	0	↑	↑	↓

At this step, the proposed converter is analysed. According to Figure 1a, b, the voltage across the inductor L can be presented as:

$$V_L(t) = \begin{cases} [V_{in} + NV_{CN}] = (N+1)V_{in} & t \in (0, dT] \\ -V_{Cc} & t \in [dT, T) \end{cases} \quad (1)$$

where d, V_{Cc}, V_{in}, and N are the duty cycle, charging capacitor voltage, and input DC source and the number of the SC cells, respectively. Also, T is the periodic time of switching pulses that is acquired by $T = (1/f)$. Note that f is the switching frequency. Considering that in the ideal-state, the average voltage of an inductor is zero in one full cycle, the voltage balance on the inductor gives:

$$d(N+1)V_{in} + (1-d)(-V_{Cc}) = 0 \quad (2)$$

Using Equation (2), the voltage across the charging capacitor (C_c) can be acquired as follows:

$$V_{Cc} = \frac{d(N+1)}{1-d} V_{in} \quad (3)$$

Based on Figure 1b, the following statement can be written as:

$$(N+1)V_{in} + V_{Cc} - V_{out} = 0 \quad (4)$$

By substituting Equation (3) in (4) and solving the equation, the voltage conversion ratio of the converter is attained as:

$$G = \left|\frac{V_{out}}{V_{in}}\right| = \frac{(N+1)}{1-d} \quad for\ 0 < d < 1 \quad (5)$$

Based on Equation (5), the average input current of the converter (I_{in}) is G times its output current (I_{out}). In the following, the size of the converter components is calculated. Generally, the inductor current can be formulated as given below:

$$i_L(t) = \frac{1}{L}\int_0^t V_L(t)dt + i_L(0) \tag{6}$$

Using Equations (1) and (6), the current ripple of this inductor for $t = dT$ can be expressed as given below:

$$\Delta i_L = \frac{1}{L}\int_0^{dT} (N+1)V_{in}dt \tag{7}$$

By solving Equation (7), the inductor size can be obtained by Equation (8).

$$L = \frac{d(N+1)}{f|\Delta i_L|}\left|V_{in}\right| \tag{8}$$

By using similar capacitors in SC cells, the charging and discharging currents of these capacitors will also be similar, resulting in having identical voltages across them ($V_{C1} = V_{C2} = \ldots = V_{CN}$). Since in mode 1, the average current of SCs is equal to I_{in}, the voltage ripples of these capacitors for $t = dT$ can be written as:

$$\Delta V_{Ci} = \frac{1}{C_i}\int_0^{dT} (-\frac{(N+1)}{1-d}I_{out})dt \qquad \text{for} \quad i = 1, 2, \ldots, N \tag{9}$$

By considering $I_{out} = (V_{out}/R)$ and solving (9), SCs can be sized as follows:

$$C_i = \frac{(N+1)d}{(1-d)\,|\Delta V_{Ci}|\,fR}\,|V_{out}| \qquad \text{for} \quad i = 1, 2, \ldots, N \tag{10}$$

Similarly, the size of the charging and filtering capacitors can be respectively calculated as given below:

$$C_C = \frac{d\,|V_{out}|}{|\Delta V_{Cc}|\,fR} \tag{11}$$

$$C_f = \frac{d\,|V_{out}|}{\left|\Delta V_{Cf}\right|\,fR} \tag{12}$$

where the voltage ripples of the charging and filtering capacitors are denoted by ΔV_{Cc} and ΔV_{Cf}.

2.3 | Efficiency and power loss analysis

In the following, the efficiency analysis of the converter is presented, and the power losses of the converter components are calculated, according to the following guidelines. It should be noted that the voltage stress on the components is also given in this section.

Initially, the power losses of the switching devices are obtained. As a rule, power losses of switches and diodes consist of the conduction and switching losses, i.e., $P_{device} = P_{Conduction} + P_{Swiching}$. The conduction losses can be acquired by Equation (13).

$$P_{Conduction} = R_d I_{RMS}^2 + V_F I_A \tag{13}$$

where R_{d}, V_{F}, I_{RMS}, I_{A} denote the switching device's internal resistance, on-state voltage, current root mean square (RMS), and average values, respectively.

Moreover, the switching power loss can be calculated as follows:

$$P_{Switching} = (E_{ON} + E_{OFF})f \tag{14}$$

where the switching energy losses of the devices while turning it on and off are presented by E_{ON} and E_{OFF}.

Based on Equations (13) and (14), the power losses of all switches and diodes of the converter are presented in the following. Generally, the current of the T switches can be written as:

$$i_T(t) = \begin{cases} I_{in} & t \in (0, dT] \\ 0 & t \in (dT, T) \end{cases} \tag{15}$$

By using Equations (15) and (13), the conduction power loss of the switch T_{N+1} is calculated as:

$$P_{T(N+1)(c)} = R_{d(sw)}\left(\sqrt{d}I_{in}\right)^2 + V_{F(sw)}dI_{in} \tag{16}$$

where $R_{d(sw)}$ and $V_{F(sw)}$ are the internal equivalent resistance and on-state voltage of the switches. By using Equation (14) and considering that the blocking voltage of the switch T_{N+1} is equal to $(V_{in}+V_{Ci})$, its switching power loss is expressed as:

$$P_{T(N+1)(s)} = \frac{V_{in}I_{in}f\,(Nd+1)}{6\,(1-d)}(t_{on}+t_{off}) \tag{17}$$

Hence, the total power loss of the switch is obtained as follows:

$$P_{T(N+1)} = R_{d(sw)}\left(\sqrt{d}I_{in}\right)^2 + V_{F(sw)}dI_{in} + \frac{V_{in}I_{in}f\,(Nd+1)}{6\,(1-d)}(t_{on}+t_{off}) \tag{18}$$

By using Equations (15) and (13), the conduction power loss of the switch T_k, $k = 1, \ldots, N$, is calculated as:

$$P_{T(k)(c)} = R_{d(sw)}dI_{in}^2 + V_{F(sw)}dI_{in} \tag{19}$$

By considering that the blocking voltage of these switches is equal to (V_{in}), the switching power loss of the switch T_k, $k = 1, \ldots, N$, is expressed as:

$$P_{T(k)(s)} == \frac{V_{in}I_{in}f}{6}(t_{on}+t_{off}) \tag{20}$$

Hence, the total power loss of the switch T_k, $k = 1, \ldots, N$, is obtained as follows:

$$P_{T(k)} = R_{d(sw)}dI_{in}^2 + V_{F(sw)}dI_{in} + \frac{V_{in}I_{in}f}{6}(t_{on}+t_{off}) \tag{21}$$

The voltage stress of the S switches in OFF-state can be written as below:

$$V_{Sk} = kV_{in} \quad \text{for} \quad k = 1, 2, \ldots, N \tag{22}$$

Moreover, the current of these switches can be expressed by (23).

$$i_S(t) = \begin{cases} 0 & t \in (0, dT] \\ \frac{I_{in}}{N} & t \in (dT, T) \end{cases} \tag{23}$$

Similar to the procedure done previously, the total power loss of the switch S_k, $k = 1, \ldots, N$, is obtained as follows:

$$P_{S(k)} = R_{d(sw)}\left[\frac{(\sqrt{1-d})I_{in}}{N}\right]^2 + V_{F(sw)}\left[\frac{(1-d)I_{in}}{N}\right] + \frac{kV_{in}f}{6}\left(\frac{I_{in}}{N}\right)(t_{on}+t_{off}) \tag{24}$$

Generally, the current and voltage stresses of the diodes D_1, …,D_N can be respectively obtained from Equations (23) and (22) since in the same cell, these diodes and the S switches have similar voltage stresses and currents. As a result, the conduction power loss of the diode D_k, $k = 1, \ldots, N$, is gained as follows:

$$P_{D(k)(c)} = R_{d(D)}\left[\frac{(\sqrt{1-d})I_{in}}{N}\right]^2 + V_{F(D)}\left[\frac{(1-d)I_{in}}{N}\right] \tag{25}$$

where $R_{d(D)}$ and $V_{F(D)}$ are the internal equivalent resistance and on-state voltage of the diodes. Based on Equation (14), the switching power loss of the diode D_k, $k = 1, \ldots, N$, can be obtained as:

$$P_{D(k)(s)} = \frac{kV_{in}f}{6}\left(\frac{I_{in}}{N}\right)(t_{on}+t_{off}) \tag{26}$$

where t_{on} and t_{off}, respectively, denote the diodes on- and off-transients. Using Equations (25) and (26), the total power loss of the diode D_k, $k = 1, \ldots, N$, can be expressed as:

$$P_{D(k)} = \frac{kV_{in}f}{6}\left(\frac{I_{in}}{N}\right)(t_{on}+t_{off}) + R_{d(D)}\left[\frac{(\sqrt{1-d})I_{in}}{N}\right]^2 + V_{F(D)}\left[\frac{(1-d)I_{in}}{N}\right] \tag{27}$$

The current of the diodes D_{N+1} and D_{N+2} are respectively presented in Equations (28) and (29).

$$i_{D(N+1)}(t) = \begin{cases} 0 & t \in (0, dT] \\ I_{L1} & t \in (dT, T) \end{cases} \tag{28}$$

$$i_{D(N+2)}(t) = \begin{cases} I_o & t \in (0, dT] \\ 0 & t \in (dT, T) \end{cases} \tag{29}$$

In addition, these two diodes have similar voltage stress in OFF-state which is equal to the output voltage. By performing the procedure done previously for other diodes, the total power losses of the diodes D_{N+1} and D_{N+2} are acquired respectively as follows:

$$P_{D(N+1)} = \frac{f(N+1)V_{in}}{6(1-d)}I_L\left(t_{on}+t_{off}\right) + R_{d(D)}\left((\sqrt{1-d})I_L\right)^2 + V_{F(D)}(1-d)I_L \tag{30}$$

$$P_{D(N+2)} = \frac{f\,V_{in}I_{in}}{6}\left(t_{on}+t_{off}\right) + R_{d(D)}\left(\frac{\sqrt{d}(1-d)I_{in}}{1+N}\right)^2 + V_{f(D)}\left(\frac{d(1-d)I_{in}}{1+N}\right) \tag{31}$$

At this step, the power losses of the passive components are calculated based on the following equation.

$$P_{LOSS} = R_{ESR}I_{RMS}^2 \tag{32}$$

where the equivalent series resistance (ESR) is denoted by R_{ESR}. Accordingly, the power losses of all passive components are obtained as expressed below:

$$P_L = R_{ESR(L)}\left(\left[1+\frac{(N+1)}{1-d}\right]I_{out}\right)^2 \tag{33}$$

$$\sum P_{Ci} = \sum_{i=1}^{N}\left[R_{ESR(Ci)}\left(I_{in}\sqrt{\frac{(N-1)d+1}{N}}\right)^2\right] \tag{34}$$

$$P_{Cc} = R_{ESR(Cc)}I_{out}^2 \tag{35}$$

where P_{L}, P_{Ci}, and P_{Cc} are the power losses of the inductor L, SCs, and charging capacitor, respectively. Also, $R_{\mathrm{ESR(L)}}$, $R_{\mathrm{ESR(Ci)}}$, and $R_{\mathrm{ESR(Cc)}}$ are the internal resistances of the inductor L, SCs, and charging capacitor. Note that the current of the output capacitor $\mathrm{C_f}$ is neglected.

The total power loss (P_{T}) of the proposed converter can be obtained using Equations (13)–(35). As a result, the converter efficiency can be calculated by Equation (36).

$$\%\eta = \frac{P_{out}}{P_{out}+P_T} \times 100 \tag{36}$$

where P_{out} denotes the output power of the converter.

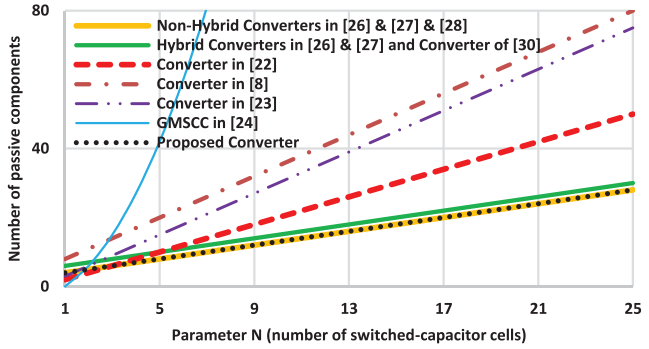

FIGURE 2 Comparing number of passive components

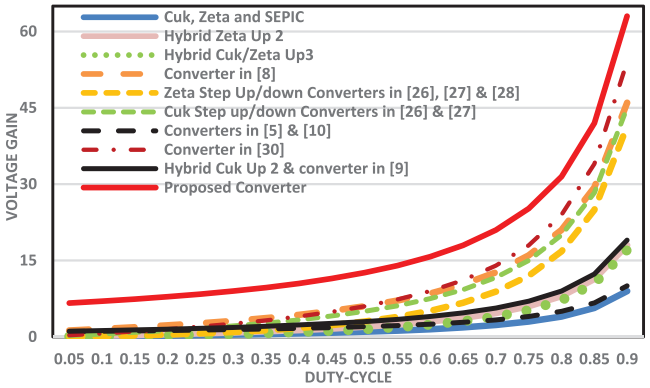

FIGURE 3 Comparing voltage gains between proposed converters and others ($N = 5$)

3 | COMPARISONS

Here, the proposed converter is compared with other converter topologies in terms of the number of components, voltage conversion ratio, maximum voltage stress on SCs and switches, and efficiency. Table 2 lists the major specifications of the compared extendible in this section.

3.1 | Comparison results

The compared converters are all based on SC cells including passive components. In these structures, the more the number of cells, the more the passive components will be employed. Hence, this can be an important criterion since it can increase the size and cost of the converters remarkably. Figure 2 compares the total number of passive components used by different topologies. As seen, along with the non-hybrid step-up/down converters presented in [18–20], the proposed converter employs the fewest number of passive components, which is a merit for these converters. Besides, the highest number of passive components belongs to the converter presented in [24]. Moreover, according to Table 2, the total number of components of the proposed converter is desirable since its value is close to that of other topologies.

Figure 3 shows the voltage conversion ratio of various structures for $N = 5$. As seen, the proposed converter generates the highest voltage gain, which makes it the best option for modern applications requiring high voltage gains. As seen in this figure, the second place in terms of the highest voltage gain belongs to the converter in [30].

In order to compare the maximum voltage stresses on the SCs and power switches of different converters, the parameter VR_{max}, i.e., the ratio of the maximum voltage stress on the device to the output voltage, is defined as expressed below [28]:

$$VR_{Max} = \frac{V_{(MaxStress)}}{V_{out}} \tag{37}$$

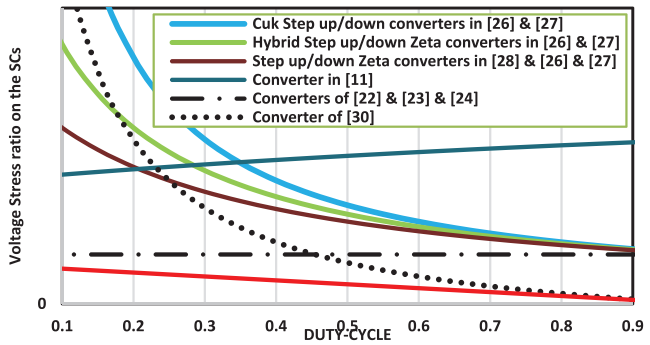

FIGURE 4 Comparing voltage stress on SCs of different topologies ($N = 5$)

In the above equation, the maximum voltage stress imposed on the device (i.e., SC or the switches) is presented by $V_{(MaxStress)}$. The parameter V_{out} denotes the output voltage of the converter. Using Equation (37), the voltage stress on SCs and power switches of extendible topologies are calculated and shown in Figures 4 and 5, respectively. Note that the number of SC cells are considered $N = 5$. As seen in Figure 4, among the compared converters, the lowest voltage stress imposed on the SCs belongs to the proposed converter. Moreover, the second place belongs to the converters in [22–24] for $0.25 < D < 0.5$ and the converter in [30] for $D > 0.5$. Figure 5 shows that for all duty-cycles lower than 0.75, the proposed converter is the superior one since it can provide the lowest voltage stress on the switches. As seen, for $D > 0.75$, the step-up/down Zeta converters presented in [18–20] have the best performance. However, it should be noted that for $D > 0.75$, the proposed converter is able to show a very close performance to these converters.

Since the efficiency of converters can be regarded as one of the important criteria to prove their effectiveness, the efficiencies of different expandable SC converters are presented in Figure 6 by considering $N = 2$. As shown, the proposed converter has a completely desirable efficiency, even compared to the other converters.

TABLE 2 Characteristics of diverse extendible SC DC–DC converters

		Max. voltage stress on component		Number of power component					
Converter topology	**Voltage gain**	**Switched-capacitors**	**Power switches**	**Capacitor**	**Inductor**	**Passive**	**Switch**	**Diode**	**Total**
Topology in [8]	$[1+(N-1)d]/(1-d)$	–	–	$2N$+3	N+1	$3N$+4	1	N+3	$4N$+8
Converter in [22]	N	V_{in}	–	N	N	$2N$	N	$2N$−1	$5N$−1
Converter in [23]	N	V_{in}	–	N	$2N$	$3N$	2	0	$5N$
GMSCC [24]	N	V_{in}	–	$\frac{(N+1)N}{1^2}-$	$N(N+1)-2$	$\frac{3(N+1)N}{2}-3$	$\frac{(N+1)N}{1^2}-$	0	$\frac{5(N+1)N}{2}-5$
Converter of [30]	$(N+1)d/(1-d)$	V_{in}	$(1+Nd)V_{in}/(1-d)$	N+2	2	N+4	$2N$+1	N+1	$4N$+6
Zeta topology of [26]	$[d+(N-1)d^2]/(1-d)$	$dV_{in}/(1-d)$	$(N-1)dV_{in}/(1-d)$	N+1	2	N+3	$2N$−1	N	$4N$+2
Zeta hybrid topology [26]	$[d+(2N-1)d^2]/(1-d)$	$2dV_{in}/(1-d)$	$2(N-1)dV_{in}/(1-d)$	N+1	3	N+4	$2N$−1	N+3	$4N$+6
Cuk topology of [26]	$Nd/(1-d)$	$V_{in}/(1-d)$	$(N-1)V_{in}/(1-d)$	N+1	2	N+3	$2N$−1	N	$4N$+2
Cuk hybrid topology [26]	$Nd(1+d)/(1-d)$	$(1+d)V_{in}/(1-d)$	$(N-1)(1+d)V_{in}/(1-d)$	N+1	3	N+4	$2N$−1	N+3	$4N$+6
Zeta topology of [27]	$[d+(N-1)d^2]/(1-d)$	$dV_{in}/(1-d)$	$(N-1)dV_{in}/(1-d)$	N+1	2	N+3	N+1	$2N$−1	$4N$+3
Zeta hybrid topology [27]	$[d+(2N-1)d^2]/(1-d)$	$2dV_{in}/(1-d)$	$2(N-1)dV_{in}/(1-d)$	N+1	3	N+4	N+1	$2N$+2	$4N$+7
Cuk topology of [27]	$Nd/(1-d)$	$V_{in}/(1-d)$	$(N-1)V_{in}/(1-d)$	N+1	2	N+3	N+1	$2N$−1	$4N$+3
Cuk hybrid topology [27]	$Nd(1+d)/(1-d)$	$(1+d)V_{in}/(1-d)$	$(N-1)(1+d)V_{in}/(1-d)$	N+1	3	N+4	N+1	$2N$+2	$4N$+7
Topology of [28]	$(1+(N-1)d)d/(1-d)$	$dV_{in}/(1-d)$	$(N-1)dV_{in}/(1-d)$	N+1	2	N+3	$3N$−2	1	$4N$+2
Proposed converter	$(N+1)/(1-d)$	V_{in}	$(1+Nd)V_{in}/(1-d)$	***N*+2**	**1**	***N*+3**	**2*N*+1**	***N*+2**	**4*N*+6**

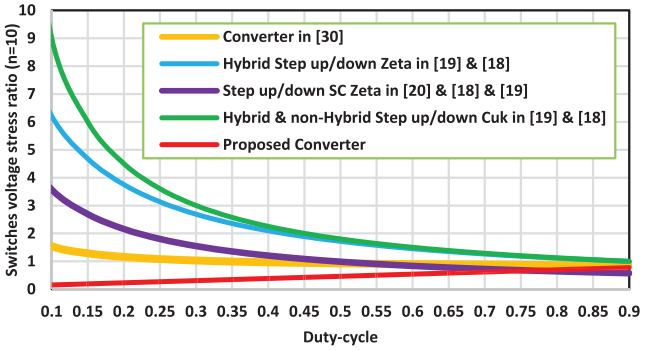

FIGURE 5 Comparing voltage stress on switches of proposed converters and other structures ($N = 5$)

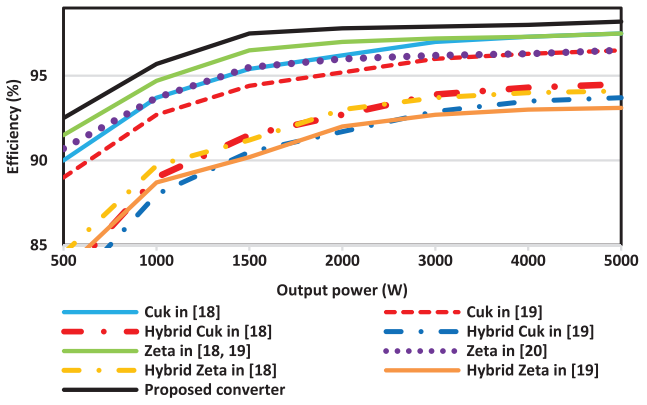

FIGURE 6 Comparing efficiencies of different converter in terms of output power

3.2 | Comparison summary

In Table 3, all of the aforementioned comparison results are briefly listed. As clearly seen, the proposed converter is the best structure or among the best converters in all of the comparisons. In summary, the proposed converter is the best option for modern applications requiring high voltage gain since it can generate very high voltage gains with lower duty-cycle and reduced voltage stress on the power switches and SCs. Generally, this converter does not need a very fast and expensive control circuit. These merits make the proposed converter a cost, size and weight-effective option for modern industrial applications.

4 | EXPERIMENTAL RESULTS

The performance of the proposed topology is validated in this section by presenting comprehensive experimental results. Generally, two experiments have been performed for the converter. In the experiments, switching frequency and number of SC cells are considered to be 25 kHz and 2. Also, the maximum ripple of inductor currents and capacitor voltages are 30% and 10%, respectively. In Figure 7, the proposed converter for $N = 2$ is presented. In Figure 8, the experimental circuit of the proposed converter is presented. In this set-up, 47N60C

TABLE 3 The qualitative results of the comparison

Comparison parameters	Qualitative	Best converters
Total number of passive components	Proposed converter = [28] = Cuk/Zeta up/down of [26, 27] < Hybrid up/down of [26, 27] = [30] < [22] < [23] < [8] < [24]	Proposed converter, [28], non-hybrid Cuk/Zeta up/down of [26, 27]
Voltage gain	Proposed converter > [30] > Cuk up/down of [26,27] > Zeta up/down of [26–28] > Hybrid Cuk up2 = [9] > Hybrid Zeta up2 > Hybrid Cuk/Zeta up3 > [5] = [10] > Cuk = Zeta = Sepic	Proposed converter
Maximum voltage stress on switches	For $D \leq 0.5$: Proposed converter < [30] < Zeta up/down of [26–28] < Hybrid Zeta up/down of [26, 27] < Hybrid and non-hybrid Cuk up/down of [27, 26	Proposed converter
	For $0.5 \leq D \leq 0.7$: Proposed converter < Zeta up/down of [26–28] < [30] < Hybrid Zeta up/down of [26, 27] < Hybrid and non-hybrid Cuk up/down of [27, 26]	Proposed converter
	For $D \geq 0.7$: Zeta up/down of [18–20]≃ Proposed converter < [30] < Hybrid Zeta up/down of [27, 26] = Hybrid and non-hybrid Cuk up/down of [27, 26]	Zeta up/down of [26–28], Proposed converter
Maximum voltage stress on capacitors	For $0.25 \leq D \leq 0.5$: Proposed converter < Converters of [22–24] < [30] < Zeta up/down of [26–28] < Hybrid Zeta up/down of [26, 27] < Cuk up/down of [27, 26] < [11]	Proposed converter
	For $D \geq 0.5$: Proposed converter < [30] < Converters of [22–24] < Zeta up/down of [26–28] < Hybrid Zeta up/down of [26, 27] < Cuk up/down of [27, 26] < [11]	Proposed converter
Efficiency	Proposed converters > Zeta up/down of [26, 27] > [28]≃ Cuk up/down of [27] > hybrid Cuk and Zeta of [26, 27]	Proposed converter

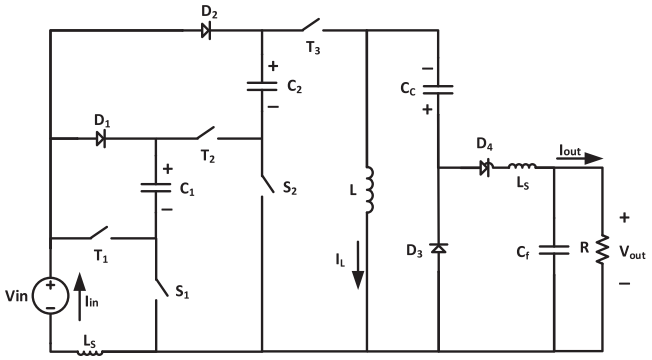

FIGURE 7 Proposed converter when $N = 2$

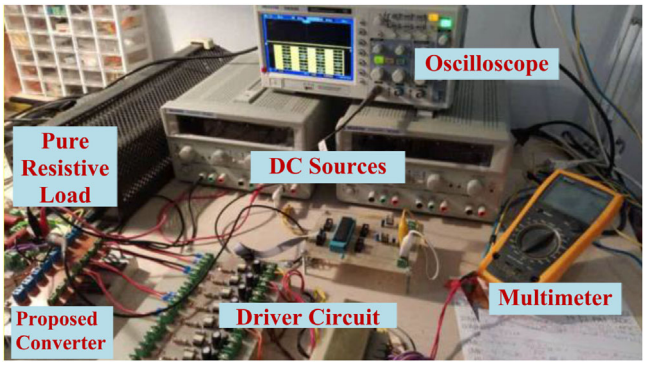

FIGURE 8 Experimental set-up of the proposed converter

MOSFETs, TLP250, and UG12 are used as the switches, drivers, and ultra-fast diodes.

In the first experiment, the output and input voltages are considered to be 210 and 35 V which gives the voltage a gain of 6. By using Equation (5), the duty-cycle is calculated as $D = 50\%$. Since the size of the inductor L should be greater than 2.3 mH based on Equation (8), its size is considered 2.5 mH. According to Equations (10)–(12), the sizes of the SCs, charging capacitor, and output capacitor must be more than 45, 2.5, and 1.25 μF. In Table 4, the specifications used for this experiment are given. Note that the inductors L_S are very small inductors, less than 1 μH, used for limiting the current peak.

Figures 9 and 10 show the results of the first experiment of the proposed converter. As seen in Figure 9, two switching pulses with a duty cycle of 50% are used for controlling the switching devices. Based on the results, the converter successfully generated the expected output voltage (208 V) with acceptable ripples when the input voltage of 35 V has been applied. Besides, all of the capacitors C_1, C_2, and C_C are charged to desirable values of 34.4, 34.4, and 110 V with permissible ripples.

As seen in Figure 10, the current of the inductor L is totally acceptable in all terms of ripple, continuity, and value. The average value and ripple of this current are about 3 and 0.83 A (less than 30%) respectively. Besides, the voltage waveforms of some of the switching devices are presented in this figure. The

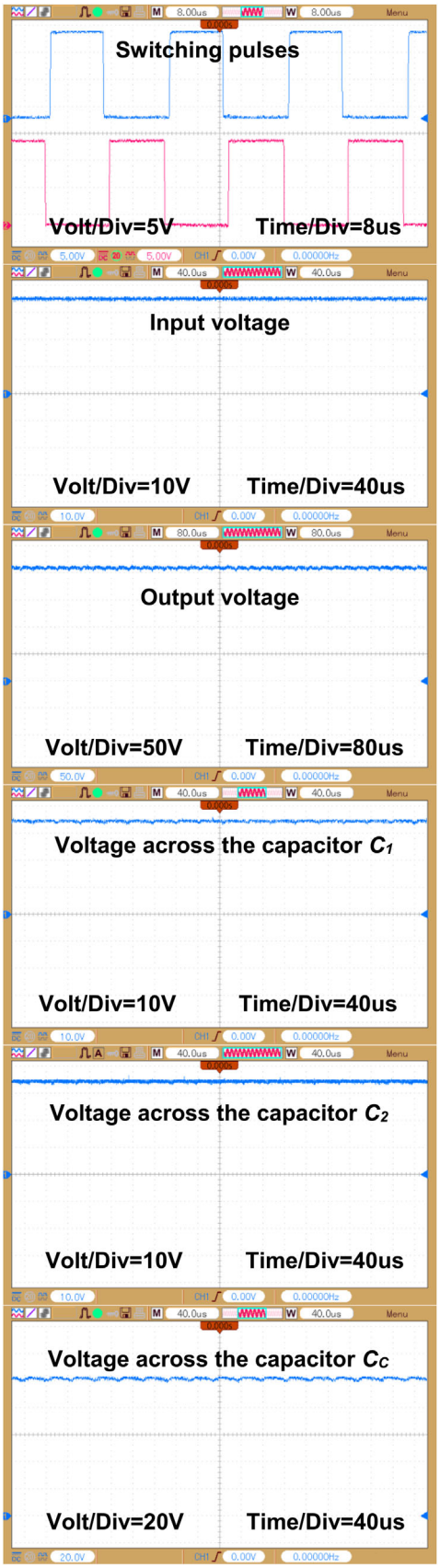

FIGURE 9 First set of the experimental results of the proposed converter for $D = 0.5$

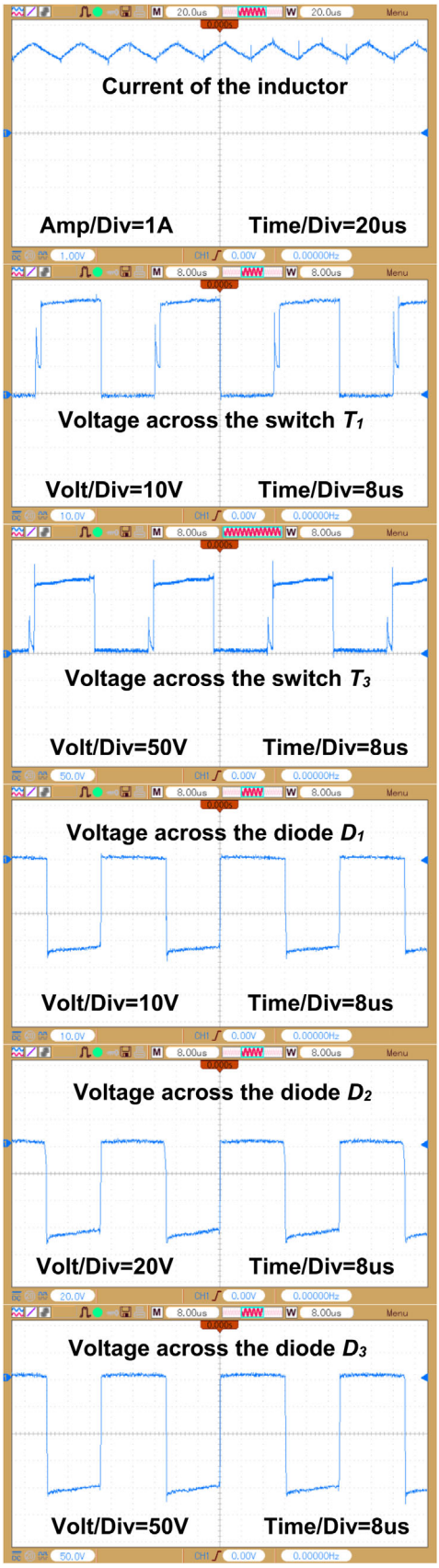

FIGURE 10 Second set of the experimental results of the proposed converter for $D = 0.5$

TABLE 4 Specifications used in the first experiment

Parameters	Symbol	Values
Input voltage	V_{in}	35 V
Output voltage	V_{Out}	210 V
Maximum current ripple of inductor (%)	Δi_L	30%
Maximum voltage ripple of capacitors (%)	ΔV_C	10%
Number of SC cells	N	2
Switched capacitors (SCs)	C_1 and C_2	50 μF
Charging capacitor	C_C	2.5 μF
Output capacitor	C_f	1.25 μF
Input Inductor	L	2.5 mH
Pure Resistive Load	R	160 Ω
Switching Frequency	F	25 kHz
Duty cycle (%)	D	50%

voltages across the switches T_1 and T_3 are shown with maximum values of 36 and 148 V. It should be noted that, according to Figure 7, the voltage stresses of the switches T_1 and T_2 are similar. In addition, as shown, the voltage stress on the diode D_2 ($|-71$ V$|$) is approximately two times greater than the voltage stress on the diode D_1 ($|-35.4$ V$|$). Moreover, the voltage waveform of the diode D_3 is shown in Figure 9 that is totally desirable with a maximum value of $|-212$ V$|$. It is clear that all switching devices successfully follow the designed switching pattern.

In the second experiment, the input and output voltages are considered as 50 and 375 V. Thus, the voltage gain is obtained as $G = 7.5$. According to Equation (5), the duty-cycle is obtained equal to 60%. Similar to the procedure done previously, based on Equation (8) and Equations (10)–(12), the minimum sizes of the inductor L, SCs, charging capacitor, and output capacitor are calculated as 3.2 mH, 48 μF, 1.4 μF, and 0.9 μF. In Table 5, the parameters used for the second experiment are listed.

Figures 11 and 12 present the results of the second experiment of the proposed topology. As seen in Figure 11, two switching pulses are employed. The DC input voltage is equal to 50 V. As seen, the converter can provide the output voltage of 374 V with an acceptable ripple. Moreover, all capacitors C_1, C_2, and C_C are successfully charged to their desired values with permissible ripples ($V_{C1} = 49$ V, $V_{C2} = 49$ V, and $V_{Cc} = 213$ V).

As seen in Figure 12, the current of the inductor L is a continuous waveform with acceptable average value (about 4.13 A) and ripple (1.1 A, i.e., less than 30%). In this figure, the voltages of the switches and diodes are also shown. As seen, the maximum voltage stress on the switches T_1 and T_3 are equal to 51 V and 290 V respectively. Note that the voltages of the switches T_1 and T_2 are similar. Besides, as expected, the maximum voltage stress of the diode D_2 ($|-101$ V$|$) is approximately two times greater than that of the diode D_1 ($|-50.4$ V$|$). Finally, the voltage waveform of the diode D_3 is also presented that is

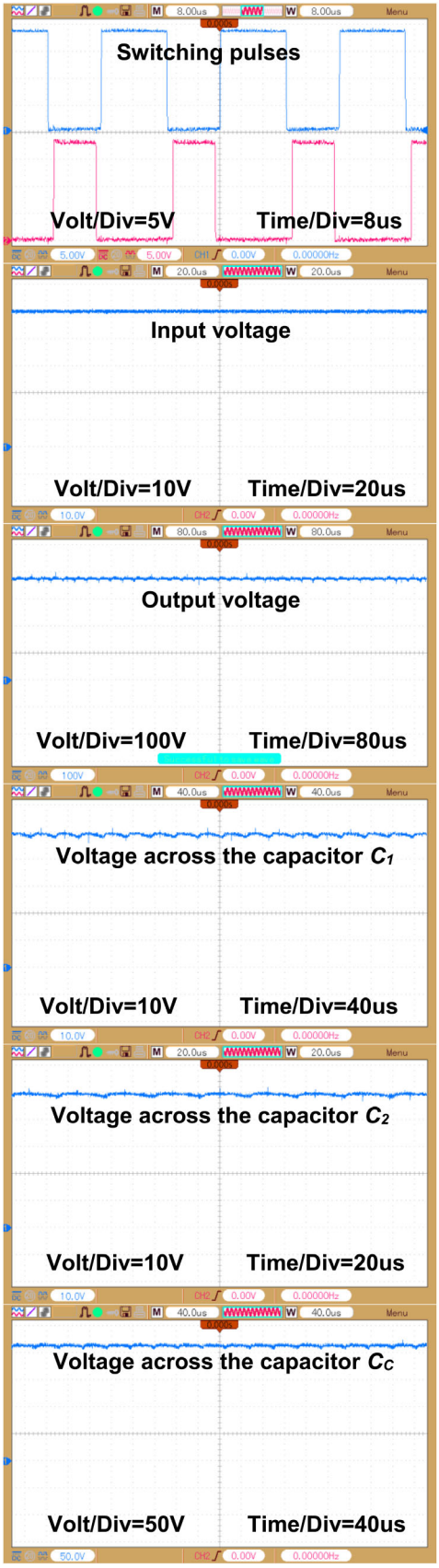

FIGURE 11 First set of the experimental results of the proposed converter for $D = 0.6$

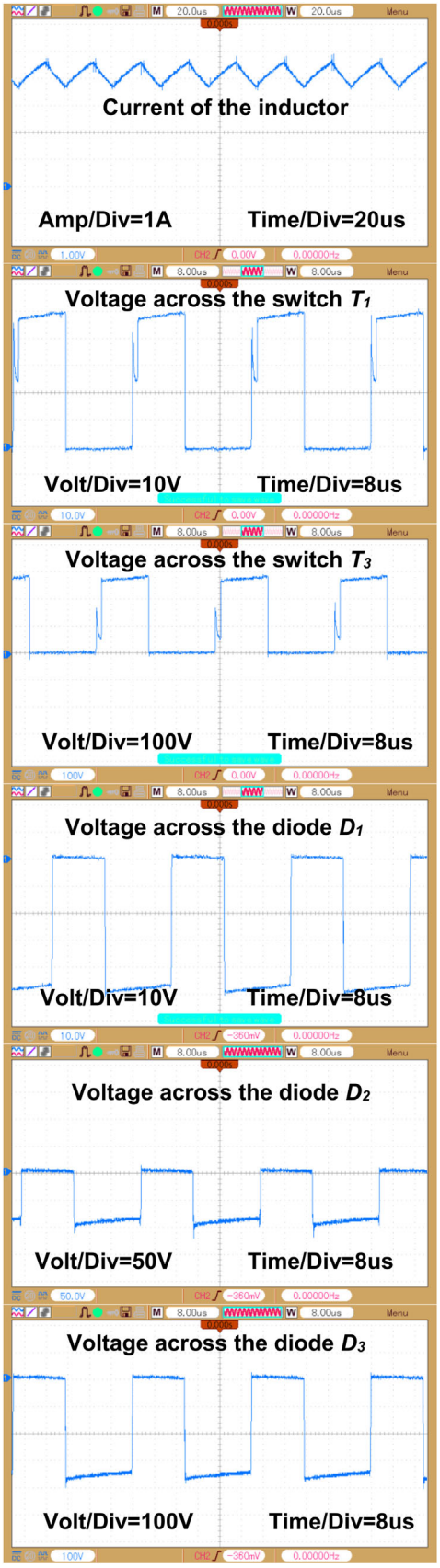

FIGURE 12 Second set of the experimental results of the proposed converter for $D = 0.6$

TABLE 5 Specifications used in the second experiment

Parameters	Symbol	Values
Input voltage	V_{in}	50 V
Output voltage	V_{Out}	375 V
Maximum current ripple of inductor (%)	Δi_L	30%
Maximum voltage ripple of capacitors (%)	ΔV_C	10%
Number of SC cells	N	2
Switched capacitors (SCs)	C_1 and C_2	50 μF
Charging capacitor	C_C	2 μF
Output capacitor	C_f	1 μF
Input inductor	L	3.2 mH
Pure resistive load	R	280 Ω
Switching frequency	F	25 kHz
Duty cycle (%)	D	60%

completely desirable. Obviously, all of the switching devices follow the designed switching pattern properly.

In conclusion, the experimental results are in great agreement with the analysis, which in turn validates the proposed converter performance.

5 | CONCLUSION

In this paper, a new transformerless step-up DC–DC converter is proposed which has several advantages like higher voltage gain and less voltage stress on components in comparison to other structures. Based on the comparison results, the converter can provide higher voltage gains with lower voltage stress on the components by employing lower duty-cycles. The continuous input current is guaranteed by the proposed topology, making it possible to extract the maximum power from RESs such as solar panels. The performance of the converter is validated by two sets of experimental results performed for two different operating conditions. As shown, the proposed converter is able to provide the desired output voltage with permissible ripple. The proposed structure shows a completely desirable performance and is suitable for industrial applications that need high voltage gains.

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