UTS UNIVERSITY OF TECHNOLOGY SYDNEY

Analysis and Modeling of Thermal Coupling Effect Between Power Semiconductor Devices

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Thesis submitted in fulfilment of the requirements for the degree of

Doctor of Philosophy

under the supervision of Dylan Dah-Chuan Lu

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July 2020

Certificate of original authorship

I, Kaixin Wei declare that this thesis, is submitted in fulfilment of the requirements for the award of Doctor of Philosophy, in the Faculty of Engineering and IT at the University of Technology Sydney.

This thesis is wholly my own work unless otherwise referenced or acknowledged. In addition, I certify that all information sources and literature used are indicated in the thesis. This document has not been submitted for qualifications at any other academic institution.

This research is supported by the Australian Government Research Training Program.

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Date: 09/07/2020

Acknowledgment

I would like to express my gratitude to all those who helped me during the journey of my Ph. D study. I gratefully acknowledge the help of my supervisor Prof. Dr. Dylan Lu, for all the support and encouragement he provided to me during my entire Ph. D program. My first journal paper almost took one year from submission to acceptance, and it is him to help me revise more than ten drafts. His constant guidance has walked me through all the stages of my Ph. D study. Under his unselfish guidance, I am growing up to not only an eligible Ph. D student but a person of courage and honesty in life.

I would also like to extend my sincere gratitude to my co-supervisor, Dr. Yam P. Siwakoti, for his instructive advice and useful suggestions on my research progress. He is knowledgeable and always keeps patient for my sudden visit to his office. His timely feedbacks really have helped me a lot.

I also owe a special debt of gratitude to all my good friends and colleagues in my team. They shared happiness with me in daily life and enlightening brainstorming in study which I have benefited a lot.

I really appreciate the love and care of my family. Thanks to my parents for their support and help in my study and life over the years. Thanks to my wife for her tolerant and understanding which make me study abroad at ease. Thanks to my baby for his coming to make me full of energy.

I would like to express my sincere thanks to all the people who have been supporting me, understanding me, and encouraging me. To express my inner gratitude, I borrow a few sentences from a song called "raise me up":

You raise me up, so I can stand on mountains.
You raise me up, to walk on stormy seas.
I am strong, when I am on your shoulders.
You raise me up, to more than I can be.

Finally, I would like to express my heartfelt thanks to all the experts and scholars who have worked hard for the paper review.

Kaixin Wei

September 2019 in Sydney

List of Publications

Journal papers

J-1. **K. Wei**, D.D.C Lu, C. Zhang, Yam P. Siwakoti, et al. Modeling and Analysis of Thermal Resistances and Thermal Coupling Between Power Devices[J]. IEEE Transactions on Electron Devices,2019,66(10):4302-4308. (**SCI, IF 2.704**)

J-2. **K. Wei**, C. Zhang, Yam P. Siwakoti, et al. Multi-Variable Thermal Modeling of Power Devices Considering Mutual Coupling[J]. Applied Sciences,2019,9(16): 3240-3243. (**SCI, IF 2.217**)

J-3. **K. Wei**, D.D.C Lu, Yam P. Siwakoti, et al. Electro-thermal Modeling Considering Ambient Temperature and Convection Coupling[J]. Applied Sciences.(**Under review，SCI, IF 2.704**）

J-4. **K. Wei**, C. Zhang, et al. Thermal Coupling Modeling for Multi-Chip Paralleled IGBT Modules Based on the Thermal Resistance Network Method[J]. Journal of Beijing Institute of Technology, 2017,26(1):147-152.

J-5. **K. Wei**, C. Zhang, et al. The IGBT Losses Analysis and Calculation of Inverter for Two-seat Electric Aircraft Application[J]. Energy Procedia,2017,105:2623-2628

Conference papers

C-1. **K. Wei**, C. Zhang, et al. A Thermal Coupling Model Based on the Thermal Resistance Network Method for Paralleled IGBT Modules[C]. ISEV, 2017.

C-2. **K. Wei**, C. Zhang, et al. An Electric-thermal Model Calculating Losses and Junction Temperature for Paralleled IGBT Modules in an Inverter Application[C]. ICMEE, 2017.

Contents

Abstract

Power semiconductor devices, which are mainly used in power converters such as buck and boost converters and inverters, are the core part of energy transformation and transmission and they are widely used in electric vehicle applications. The recent trend in the design of the high-power density power converters generally reduces the rate of the devices cooling process. As a result, an increased thermal coupling among devices increases the overall power supply temperature, and the uneven temperature distribution of the devices, which negatively affects the performance and lifespan of semiconductor devices and power converters. Traditional thermal models do not consider the changes of self-thermal resistances and also ignore the effect of thermal coupling among the adjacent devices. Compared with these models, the proposed thermal resistances modeling approaches provide better understanding of the thermal behavior of power devices.

The uneven case temperature distribution of the devices in the converter system increases the thermal coupling effect between adjacent devices and thermal stress concentration. In the design stage, considering the demand of power converter system for the case temperature control of the devices, a calculation method of thermal coupling effect is proposed based on the thermal coupling experiment platform for power devices. The thermal coupling effect between adjacent devices under different working conditions can be obtained by building a thermal coupling resistances network (TCRN) model and analyzing the relationships between the self-resistance and the thermal coupling resistances between adjacent devices. Finally, a new thermal coupling testing platform is established with a different device spacing, and the results are compared with the derived TCRN model. The comparisons show that the calculation method of the thermal coupling effect proposed is feasible and effective.

In order to analyze the convection thermal coupling effect between adjacent power devices, a convection thermal coupling testing platform for devices is established, and a multi-variable thermal resistances network model is proposed. Thermal coupling resistances

under different working conditions can be calculated by the proposed network. In addition, the relationships between the thermal coupling resistances and their influence factors are also analyzed. Finally, the model is validated by establishing a new coupling testing platform with a new device spacing.

In order to analyze the conduction thermal coupling effect between the neighboring modules/devices, FEM and PLECS simulations are established for power converter systems. Based on the above analysis, the calculation model of conduction thermal coupling of adjacent power modules is established, and the junction temperature of the power module is calculated. Finally, the model is validated by an online simulation software provided by Infineon Technologies.

Key Words: power converter; semiconductor devices; thermal coupling effect; thermal network; thermal coupling resistances

Chapter 1 Introductions

1.1 Background and significance

The power semiconductor devices used for voltage conversion, rectification and inversionis the core part of energy conversion and transmission in power electronic equipment, which is widely used in electrical appliaances and electric vehicles [1, 2]. In recent years, power electronic applications are growing continuously, and their performance has strong correlation to national economy, such as transportation, aerospace, and renewable energy (wind power generation, solar photovoltaic, etc.), as shown in Fig. 1.1 [3, 4].

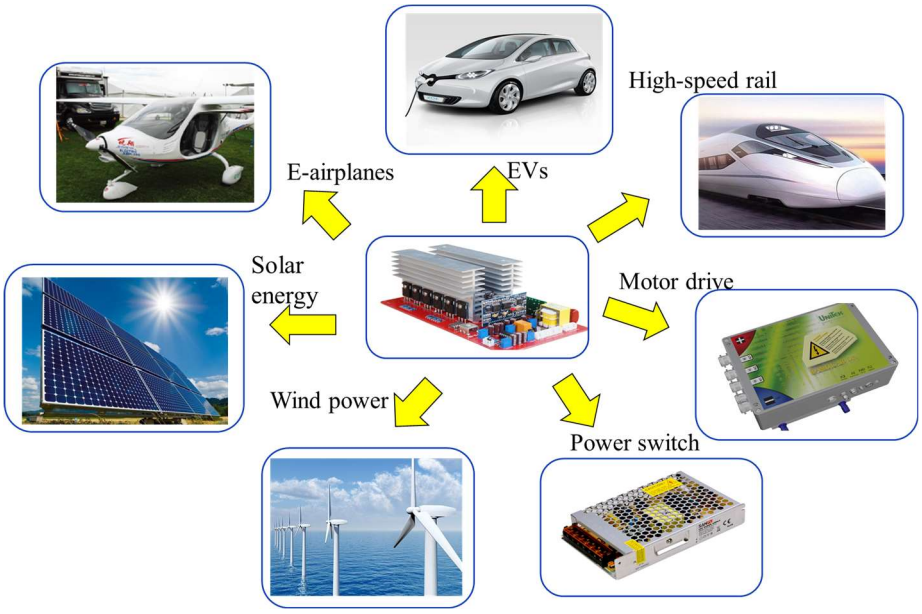


Fig. 1.1. Applications of power semiconductor devices.

According to the report on the current situation of power electronics industry in 2016-2019 [5], the power converter in the vehicles market, including electric vehicles (EV) and hybrid electric vehicles (HEV) and other new energy vehicles, increased by more than 20% in 2016. In 2017, the scale of semiconductor devices in the electric vehicle market is US $4.41 billion, which is expected to reach US $5.49 billion by 2022. According to statistics, the compound annual growth rate from 2017 to 2022 is 4.48%. In 2018, the share of power converters in the power electronics market is US $53.4 billion, and that of power

semiconductor devices is US $17.5 billion. According to the latest EV/HEV power converters market analysis in 2019, the growth rateis expected to be as high as 20.7% from 2018 to 2024 [6].

The power electronic equipments play important roles in motor drive and power control of general transportation industry such as power converter. The power electronics industry occupies an important position in the world. In the 2023 world semiconductor market forecast analysis, as shown in Fig. 1.2, the Asia Pacific region dominates the power electronics market, followed by Europe and North America [5]. Due to the increasingly serious energy and environmental problems, the energy-saving and new energy automobile industry will be vigorously promoted, so as to promote the development of power electronic equipment industry.

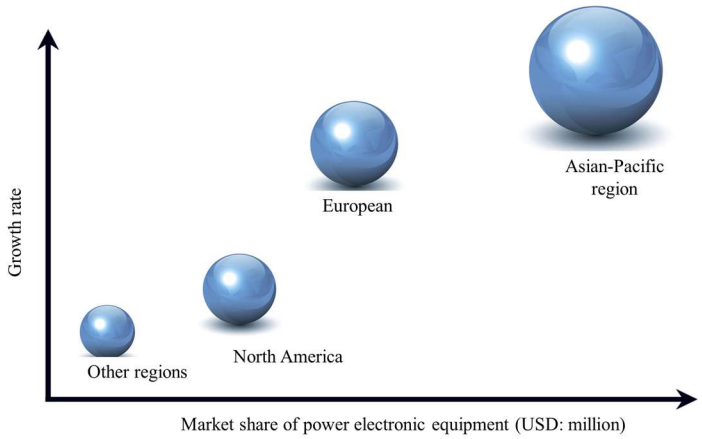


Fig. 1.2: Market share prediction of power electronic equipment in 2023 .

According to the materials of semiconductors, the power semiconductor devices can be divided into traditional silicon-based semiconductor devices, such as IGBT (insulated gate bipolar transistor) power module, MOSFET (metal oxide semiconductor field effect transistor), diodes and new wide band gap semiconducting devices, such as silicon carbide (SiC) and gallium nitride (GaN) based devices [7, 8]. In power converters for electric vehicles, IGBT modules and MOSFETs, as shown in Fig. 1.3, are mainly used. IGBT power modules are generally used in the field of medium and high voltage (high-power applications), and MOSFET are generally used in the field of medium and low-voltage (medium and small

power). The market share distribution of different power electronic devices is shown in Fig. 1.4 [9]. By comparison, in the market share of semiconductor devices in 2018 and 2024, power devices dominated by traditional silicon based MOSFETs and IGBT modules are still in the dominant positions and are developing rapidly and the share of the new wide band gap semiconductor devices has increased. As higher power density and integration are the main demands and goals pursued by power products, it is estimated that in 2022, semiconductor devices will boost the market share of power electronics to 35 billion US dollars [5].

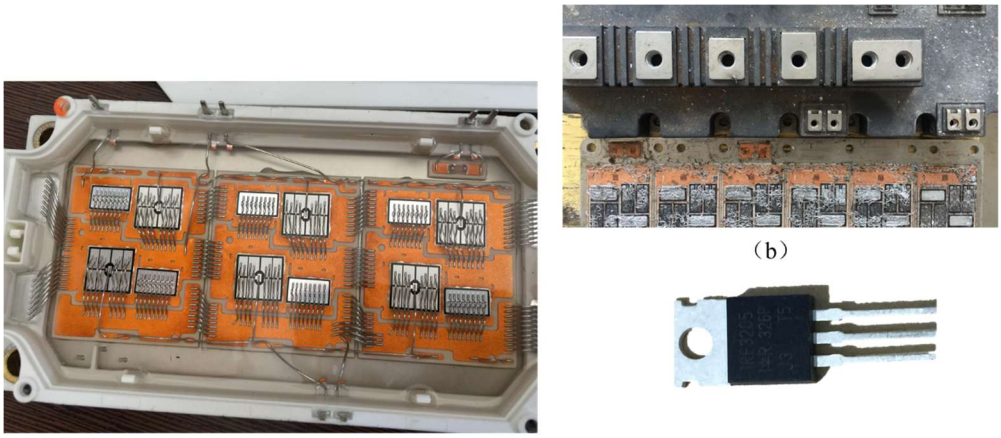
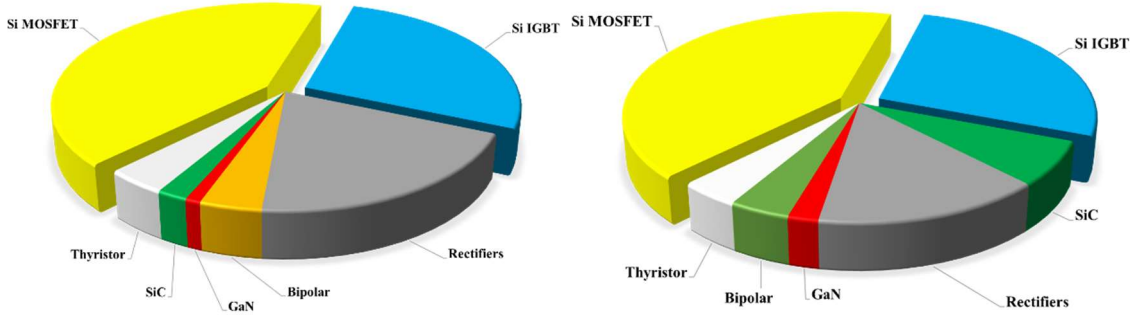


Fig. 1.3: Power devices/modules: (a) 600A FF600R06ME3 IGBT module; (b) 1400A-FF1400R17IP4 IGBTmodule; (c) 33A-IRF540N MOSFET.



(a) (b)

Fig. 1.4: Power devices market share (a) in the year of 2018; (b) prediction in the year of 2024

With the increasing power density of semiconductor devices and the increasing design requirements of compact power converters, the reliability of semiconductor devices and power converter systems has been widely concerned. In the application of power converters, semiconductor devices are an important factor affecting the reliability of power electronic equipments such as power converters [10]. The main causes of electrical failure of power electronic equipment such as semiconductor devices and power converters are temperature, humidity, mechanical vibration, dust, overvoltage, over-current, etc. [11, 12]. According to the statistics of avionics equipment, 20% of the on-site faults are caused by thermal. When the working junction temperature of power electronic devices exceeds the maximum allowable junction temperature, thermal failure of devices will occur , as shown in Fig. 1.5.

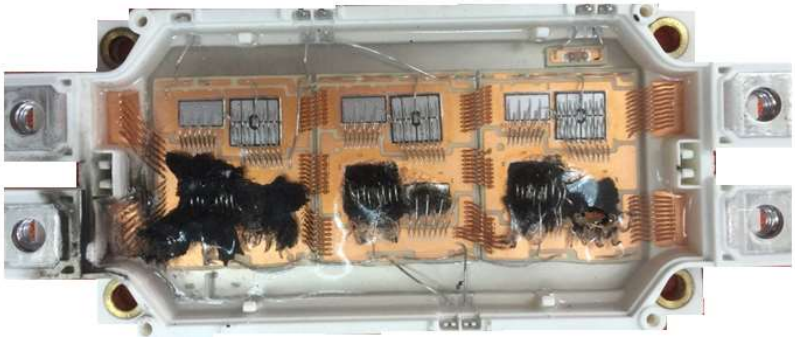


Fig. 1.5: Burned IGBT module [13, 14].

The thermal analysis calculation models [15] can be used to describe the transient or steady-state thermal distribution to ensure that the device temperature is lower than the maximum junction temperature and at the same time to make it working in a good temperature operating range [16]. The temperature of the transient thermal analysis model changes with time, which is mainly used to calculate the temperature of the model in a specific time range. The steady-state thermal analysis model mainly analyzes the influence of stable thermal on the system or components, which can be used to analyze the temperature distribution under different working conditions. Both transient and steady-state thermal analysis have their applications and research significance [17]. By establishing the corresponding thermal analysis models, not only can help the thermal distribution of the system be better analyzed, but also assist the structure optimization of the converter system.

In the application of power converters, with the improvement of power density, higher current density leads to thermal concentration of power devices, and the non-uniformity of case temperature distribution of multiple power devices in power converter which is easy to cause thermal stress concentration [18]. At the same time, the demand of high power density of the power converters, its package volume gradually decreases, which makes the space between multiple power devices compact, thus causing thermal coupling effect between multiple power modules or devices, which greatly reduces the operation reliability of the module/device itself and the converter system.

In order to solve the above problems, based on the devices and system testing platforms and the traditional thermal analysis models of power devices, this paper studies the conduction and convection thermal coupling effect between adjacent devices, and establishes the thermal coupling resistance network models, to analyze the relationships between self-thermal resistance and thermal coupling resistances, which have signaficange for power converter design, structure optimization, and system reliability.

1.2 Outline

An overview of the power devices and power converters and their required thermal models are stated in the previous sections. According to the literature survey, there is a space to improve the proposed thermal models. The organization of this thesis is listed as follows, as shonw in Fig. 1.6:

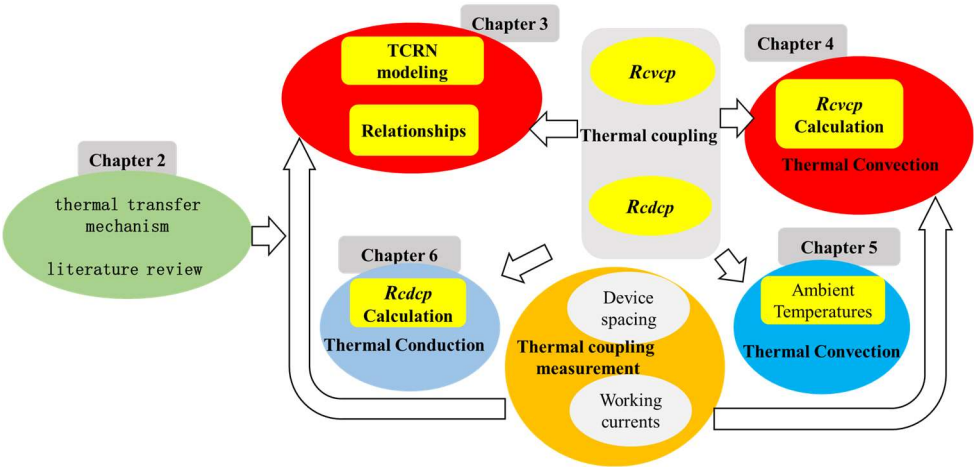


Fig. 1.6: The organization of the thesis.

In Chapter 2, thermal transfer mechanism and literature review are present which includes the thermal analysis modeling for power devices and the existing gap.

In Chapter 3, the TCRN model which considers the conduction and convection thermal coupling has been proposed for the adjacent power devices and the relationships between the thermal resistances are given.

In Chapter 4, in order to further analyze the convection thermal coupling effect, thermal analysis and testing platform of power device is established in this chapter. By changing the working conditions, the influencing factors of convective thermal dissipation under different device spacing are analyzed. In addition, in order to better analyze the convective thermal coupling effect between devices, a single test platform for semiconductor devices (MOSFET and diode) and a convective thermal coupling test platform are established. By changing the device spacing and load current, the device case temperature under different working conditions is obtained. Based on the analysis of the thermal coupling effect in Chapter 3, a multi-variable thermal resistance network model is established considering the convection thermal coupling between power devices.The thermal coupling resistance between devices is calculated, and the relationships between the coupling thermal resistance and the influencing factors (device spacing and load current) are analyzed. Finally, a new convection thermal coupling testing platform under new device spacing is established to verify the proposed thermal model by the comparison results of the thermal coupling resistance values.

The convection thermal coupling between adjacent power devices is dependent on the ambient temperature, while the existing thermal analysis models are often based on a fixed ambient temperature. When the ambient temperature changes, convection thermal coupling also changes. This results in an inaccurate model that causes errors in the prediction of the thermal distribution and junction temperature for power devices. To solve this variable ambient temperate related issue, in Chapter 5, FEM (Finite Element Method) [19, 20] models for semiconductor power devices (MOSFET and diode) considering convection thermal coupling are established. Through these simulations, the junction temperatures of devices

under different ambient temperatures are obtained, and the relationships between junction temperature and ambient temperatures are established. Moreover, the junction temperatures of power devices under different ambient temperatures are calculated and temperature distribution is analyzed in this paper. This method shows the strong significance and has potential applications for high-efficient and high-power density converter design.

In Chapter 6, conduction thermal coupling model has been proposed based on the IGBT modules application.

Finally, a conclusion summary and suggestions for future works are presented in Chapter 7.

Chapter 2 Thermal Transfer Mechanism and Literature Review

2.1 Thermal Transfer Mechanism for Power Devices

The main forms of thermal transfer are thermal conduction, thermal convection, and thermal radiation [3, 21], and the mechanism diagram is shown in Fig. 2.1. In power applications, such as the power converters/inverters, there are many forms of thermal transfer at the same time [10, 22]. The semiconductor devices are important factors affecting the reliability of the power converter system and one of the main failure factors for power converters is the thermal failure caused by the process of thermal generation and transfer, as discussed in Section 1.1. Therefore, it is important to fully understand the thermal transfer theory, and establish corresponding thermal models for the reliability and structural optimization of the devices and systems.

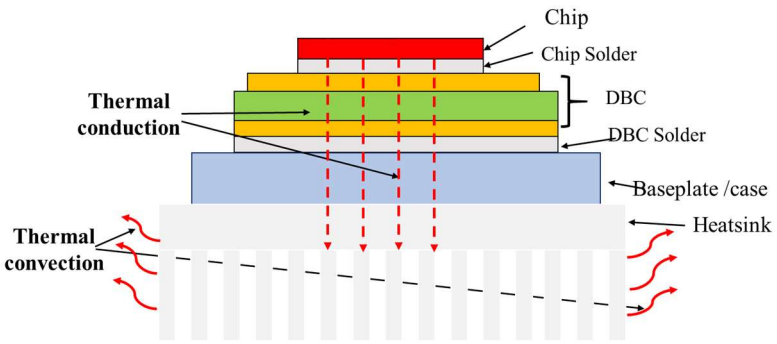


Fig. 2.1: Thermal Transfer.

2.1.1 Thermal Transfer Modes

Thermal conduction is a phenomenon of thermal transfer caused by the thermal movement of micro particles (there is no macroscopic motion in the medium) [3]. The thermal transfers from the chip to the DBC layer, the copper substrate, and then the heatsink and finally to the ambient surroundings. Thermal convection refers to the relative displacement of fluids (liquid, gas, etc.) at different temperatures due to macroscopic motion

[3]. Thermal convection is caused by the density difference between the cold and hot fluids. When the thermal is transferred from the case/ baseplate of the semiconductor devices or through the heatsink to the surrounding air, and the form of thermal transfer is becoming into the thermal convection. Thermal radiation refers to the phenomenon that an object radiates electromagnetic waves due to its temperature [23].

2.1.2 Thermal transfer process

The thermal transfer process refers to the process that the thermal is transferred from the interior of the solid to the other side of the fluid through the solid wall, that is, the thermal transfers from the heating solid (chip) to the surrounding air, as shown in Fig. 2.2. In the figure, t_{w1}, t_{w2}, t_f are the temperatures and h is the convection coefficient. It is assumed that t_{w1}、t_{w2}、t_f and h do not change with time and λ is a constant [3].

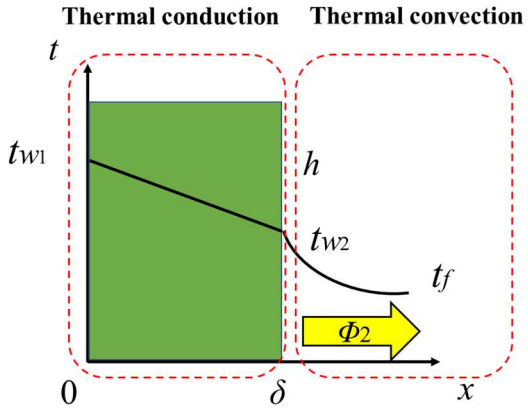


Fig. 2.2: Thermal transfer.

The thermal conduction equation of flat wall can be obtained based on the steady state thermal transfer

$$\emptyset_1 = A\lambda \frac{t_{w1} - t_{w2}}{\delta} = \frac{t_{w1} - t_{w2}}{\frac{\delta}{A\lambda}} = \frac{t_{w1} - t_{w2}}{R_\lambda} \tag{2.1}$$

And the thermal convection equation can be expressed as

$$\emptyset_2 = A\, h_2 \frac{t_{w2} - t_f}{\delta} = \frac{t_{w2} - t_f}{\frac{1}{Ah}} = \frac{t_{w2} - t_f}{R_h} \tag{2.2}$$

When the thermal transfer reaches a steady state, it can be obtained by energy conservation

$$\emptyset = \emptyset_1 = \emptyset_2 \tag{2.3}$$

that is

$$\begin{cases} \emptyset = \dfrac{t_{w1} - t_f}{\dfrac{\delta}{A\lambda} + \dfrac{1}{Ah}} = \dfrac{t_{w1} - t_f}{R_\lambda + R_h} = \dfrac{t_{w1} - t_f}{R_k} \\ R_k = R_\lambda + R_h \end{cases} \tag{2.4}$$

where R_k is the total thermal transfer resistance, R_λ is conduction thermal resistance and R_h is convection thermal resistance.

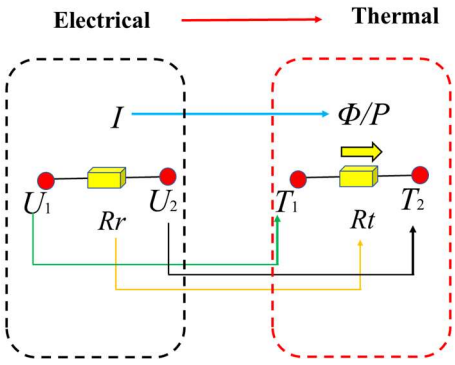


Fig. 2.3: The theory of electrical to thermal.

Based on the theory of electrical to thermal, as shown in Fig. 2.3: the resistance corresponds to the thermal resistance; the voltage difference corresponds to the temperature difference and the current corresponds to the power loss. The corresponding thermal resistance network in the thermal transfer process is shown in Fig. 2.4.

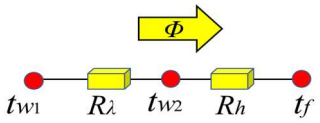


Fig. 2.4: Thermal resistance network.

2.2 Research status of thermal analysis modeling for power devices

For industrial applications, reliability, cost and power density are important considerations in the design of power converters. The increase of power density requires

efficient and intelligent thermal design and thermal management [24, 25] to ensure the reliability of the converter system [26, 27]. Based on the analysis in Section 1.1, a large proportion of the main failure in semiconductor devices and their power converters are temperature related, and the change of temperature may lead to bond wire shedding, welding fatigue crack, power chip breakdown, etc. [28]. For high power density [29] and compact power converters [30], the thermal dissipation of power devices slows down with the decrease of device spacing, thus making the overall temperature of devices and systems higher.

2.2.1 Finite Element Method (FEM) models

As shown in Fig. 2.5, different colors represent different temperature distributions. Thermal dissipation has a negative impact on the performance and lifetime of semiconductor devices and power converters.

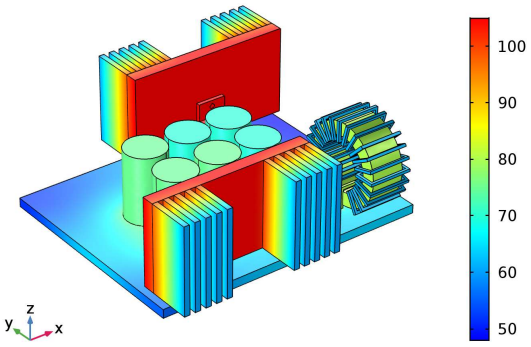


Fig. 2.5: Temperature distributions of a power converter.

Therefore, thermal analysis modeling under different load conditions is essential, and it is necessary to seek the temperature calculation methods of power converters and the optimal distribution schemes of thermal distribution. As the size of a single traditional silicon-based device approaches its basic limit [31], a better understanding of the thermal distribution of adjacent devices under different operating conditions can help the system carry out reasonable thermal management, thus improving the performance of the converter system, and optimizing the overall structure of the converter [32]. The accuracy of the thermal

analysis model has a significant impact on the thermal management and reliability of devices and systems.

For semiconductor devices and power converter systems, the commonly used thermal modeling methods mainly include physical model calculation method, numerical calculation method, finite element method (FEM), thermal resistance network method, etc. [33, 34]. FEM can be used for thermal calculation of devices or power converter systems, and the simulated structures can be simplified within the range of accuracy allowed. The FEM results can be used to analyze the temperature distribution directly by different colors, and the junction/case temperature can be extracted by adding virtual thermal probes to the corresponding components. Unlike the real probes or temperature sensors, the virtual probes are considered to have absolutely ideal thermal conductivity and insulation properties, which can be attached to the device surface or injected inside the devices, or anywhere in the air region [35].

However, it has difficulties when using FEM to establish thermal models for the semiconductor devices, because you should be familiar with the specific parameters of internal structures for power devices or modules. The FEM analysis needs 3D modeling of the devices or systems. Although the structures can be simplified, the structures of the devices and systems need to be better understood. In addition, in order to build a more accurate FEM analysis model, in addition to being familiar with the geometric structure of devices/modules and the relative positions of multiple devices in the system, reasonable meshing and boundary conditions setting are also essential [36], then the speed of FEM simulation will be generally slow [37].In this paper, the FEM method is used to analyze the convection thermal coupling of adjacent semiconductor devices.

2.2.2 Thermal resistance network models

The thermal resistance network method, also known as thermal path method, is fast and effective [38]. It can not only calculate the temperature of junction temperature and case

temperature, but also can describe the thermal distribution of the devices or power converter system and the thermal coupling effect between adjacent devices through the values and distribution of thermal resistances. The thermal resistance network method is generally based on the Foster model [39, 40] and Cauer model [41, 42], as shown in Fig.2.6, and then it can be improved according to the practical application of semiconductor devices or power converters.

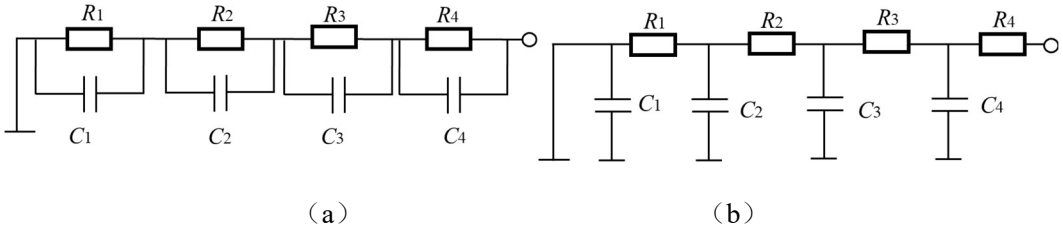


Fig. 2.6: Foster and Cauer network models [43]. (a) is Foster model; (b) is Cauer model.

Forster model is to obtain the thermal characteristic parameters of thermal resistance value (R) and thermal capacity (C), and the parameters R and C is by multi-order exponential fitting of dynamic thermal impedance curve which is measured by simulation or testing. Although the Foster model can not reflect the temperature distribution of different layers in the device, it is simple and effective. The Cauer model reflects the real thermal resistance and thermal capacity of the actual physical layer or each level of packaging structure material [44], which can be used to predict the temperature distribution of each layer or level of structure. However, for semiconductor devices, the packaging structure is complex, and it is difficult to obtain accurate thermal parameters among different levels of structure in the device. The thermal resistance network models established in this paper are all based on Foster model.

Based on the two kinds of thermal resistance network, the thermal resistance of heatsink can be expanded to establish one-dimensional thermal model. Z. Luo and H. Ahn et al. [44] used lumped parameter method to establish a seven-order electrio-thermal coupling model for a single IGBT power module. The thermal model is improved based on the Cauer model and solved by the fourth order Runge Kutta method. The equivalent thermal resistance and

equivalent thermal capacity are calculated and extracted through the combination of power module structure and FEM simulation. In the FEM simulation, a fixed temperature value is set for the substrate temperature (case temperature) to simulate the dynamic thermal dissipation of the heatsink to obtain the temperature of each layer in the module, which can avoid to calculate different kings of the heatsinks [45]. The one-dimensional thermal resistance network proposed by Graovac. Dusan and Purschel. Marcoet et al. is based on the datasheet given in the device manufacturer to obtain the junction-to-case thermal resistance curve of MOSFET. The device temperature is extracted from the thermal analysis testing, and the case-to-ambient thermal resistance is calculated. Finally, the thermal resistance network model of the device is established [46].

The one-dimensional thermal resistance network can well reflect the junction-to-case thermal resistance and can also quickly calculate the junction temperature of the device, while this kind of model often only focuses on the device self-thermal resistance. Although the extended model based on the self-thermal resistance network considers the thermal resistance of the heatsink, the model is relatively simple. The thermal dissipation of the heatsink is generally in three-dimensional way, and the dissipation way includes thermal conduction and convection. The one-dimensional model can not calculate the thermal coupling between adjacent devices (or modules), and the thermal coupling is usually ignored, which affects the accuracy of the model and the calculation results [44].

As the analysis in Section 1.1, with the development of design requirements for power converters at present and in the future, the shape factor is reduced, while the power density is constantly increasing [47, 48], as a result, the thermal dissipation of power devices slows down with the decrease of device spacing, and then the overall temperature of power converter increases. This trend usually reduces the cooling (thermal dissipation) rate of power converter system and semiconductor devices, thus increasing the mutual thermal coupling between adjacent power devices and increasing the junction temperature of devices. Most of the traditional models usually ignore the thermal coupling between devices or only focus on conduction and the conduction coupling. However, in practical power converter applications,

the conduction thermal coupling formed by metal contact surface or copper wire connection and the convection thermal coupling formed by air convection will have a certain impact on the junction temperature (or case temperature) of the device, and then affect the temperature distribution and junction temperature prediction of the device, and the reliability of the device and system will also be affected.

The conduction thermal coupling thermal resistance (R_{cdcp}) can be formed in the following ways: one is that multiple thermaling sources, such as power chips or semiconductor devices/modules, are placed on the same metal substrate, such as copper substrate or heatsink, on which the adjacent thermaling sources will affect each other in the process of thermal transfer, and in different disances the thermal coupling is different, as shown in Fig. 2.7; the other way is that a part of the thermal is conducted along the copper line in the PCB, and the thermal between adjacent devices will affect each other through the circuit.

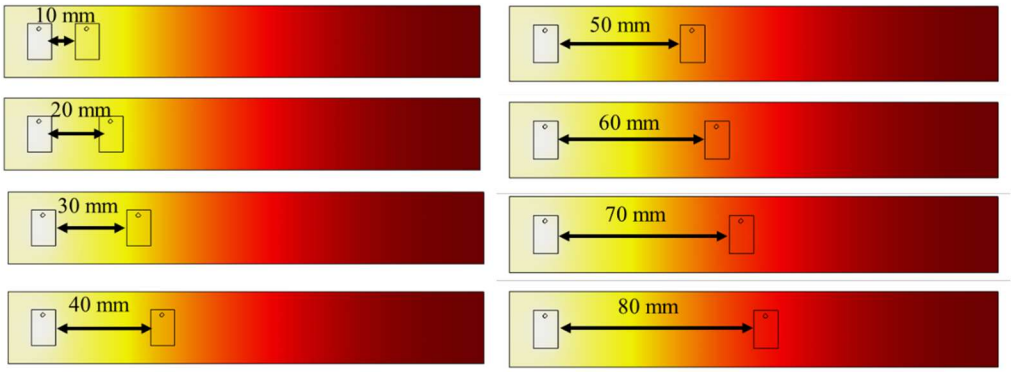


Fig. 2.7: Thermal couping between IGBT chips.

For a single IGBT power module, several IGBT chips and diode chips are generally packaged in an IGBT module. K. Subramanya, J. Pandit et al. and M. Shahjalal et al. analyzed the thermal effect of multiple chips on the same copper substrate in a single IGBT module and gave the calculation method of conduction thermal coupling resistance generated by the adjacent chips, as shown in Fig. 2.8. Compared with the one-dimensional thermal network model, the junction temperature of the device calculated by this model is more accurate.

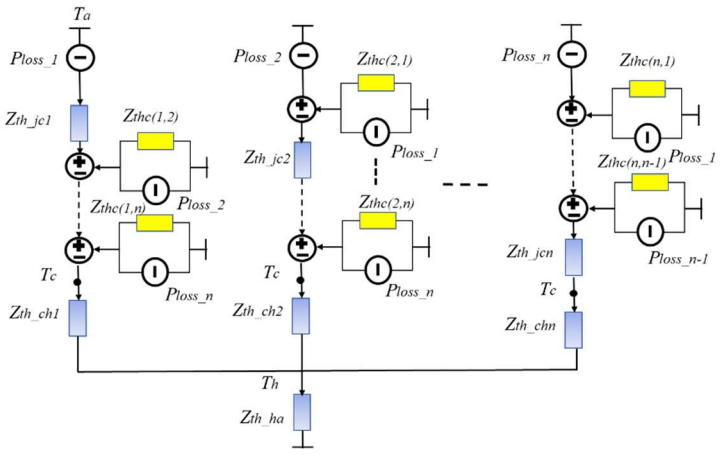


Fig. 2.8: The conduction thermal coupling thermal resistance (R_{cdcp}) in a single IGBT module.

Tang Yunyu and Lin Liaoyuan proposed the influence of installation distance on the thermal coupling of multiple parallel power modules in the power converter, and calculated the average junction temperature of adjacent power modules, while they did not give the specific relationship between different module distances and thermal coupling effect. Moreover, Tang Yunyu and Lin Liaoyuan et al. [49] established a thermal resistance network model of multiple IGBT and diode chips in the power module. The thermal coupling matrix established in the model adopts a given power loss and applies it to the chip and extracts the chip temperature through a series of FEM simulation. The simulation results show that the temperature difference (between the highest point and the lowest point) is 0.52 ℃ (3.8 cm) and 0.96 ℃ (6.8 cm) at two different distances, which indicates that the thermal coupling between chips depends on the geometric position of the chips and the chip spacing [50-52]. Similarly, the conduction thermal coupling model established by Li Hui et al. is also generated by adjacent chips on the same substrate in a single power module [53].

The thermal model established by M. Bernardoni and P. Cova et al. calculates the junction temperature of chips through ANSYS simulation, and the conduction coupling thermal resistance under different working conditions by changing the number of chips and chip spacing are studied [54]. The thermal model established by A. S. Bahman and K. Ma compares the temperatures at the same position of different structural layers in the vertical direction of the power module, calculates the conduction coupling thermal resistance when

the thermal flow passes through the vertical structure layer, and analyzes the influence of different working conditions on the conduction thermal coupling resistance [55].

In [53], Li Hui and Liu Shengquan et al. collected the chip junction temperature through FEM analysis, and then extracted the R and C by curve fitting, and then to derive the calculation formula of transient thermal resistance under multi-chip thermaling source. The calculated thermal resistance includes self-thermal resistance and conduction thermal coupling resistance and the junction temperature of edge position chip and non-edge position junction in the improved model and conventional model are compared. In power module applications, as the limited thermal dissipation conditions and the thermal coupling between adjacent chips at the non-edge position, the junction temperature at the non-edge position is often higher than that at the edge position. Compared with the traditional thermal models, the conduction thermal coupling is considered in this paper, and the junction temperature at different positions can be calculated. C. Batard and N. Ginot et al. [56] established a dynamic electric thermal model of a single IGBT module with multi-chips, which is based on the Cauer thermal model. The model adds a first-order R and C into the three-dimensional network. As the thickness of the chip is far less than the length and width, it can be regarded as a thin flat wall structure. Therefore, the thermal transfer mode considered in the model is one-dimensional thermal conduction in each physical layer of the module; when the thermal of the chip is transferred to the copper substrate, the thermal transfer form changed into three-dimensional thermal conduction.

A.S. Bahman and K. Ma et al. analyzed the several existing thermal models of devices. The analysis shows that the one-dimensional thermal model is limited to the thermal distribution inside the module and some variables, such as cooling and thermaling conditions. The three-dimensional thermal model based on FEM needs a lot of calculation, which is quite difficult for long-term thermal dynamic simulation. Based on the above analysis, a new concentrated three-dimensional thermal model considering the thermal coupling between different layers is proposed in this study. The critical temperature distribution can be obtained relatively easily from the FEM simulation and the boundary conditions of the thermal model

are analyzed. Finally, FEM simulation and an infrared camera (IR) are used to monitor an opened IGBT module's temperature. Tang Yunyu and Ma Hao et al. established an improved loss calculation model based on the analysis of the thermal impedance of power modules, considering the conduction coupling between multiple power modules. The model can be used to describe the interaction between the current distribution and thermal dissipation of several modules. The main work of the study is as follows: 1) The parameters of stray inductance in adjacent parallel modules are analyzed by FEM. 2) An improved power loss model is established based on impedance analysis, considering the couping between adjacent modules. 3) The RC data extracted from the 3D structural model are used to establish the thermal resistance network model and to obtain the transient thermal impedance of the module and the cooling system. The method presented in this paper is a fast electro-thermal co-simulation method for converter systems with multiple parallel power modules, while they do not consider the convection coupling.

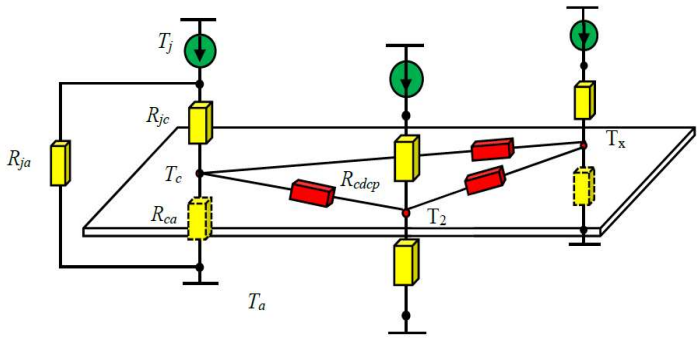


Fig. 2.9: R_{cdcp} in a power converter.

Another way for generating the R_{cdcp} is the thermal coupling effect between the power components (MOSFET, diode, capacitance, and inductance, etc.) in a converter through the copper wire connection. Erik C. W. de Jong et al. established a thermal resistance network model based on the device's surface/case temperature (T_c), as shown in Fig. 2.9. They considered the conduction thermal coupling effect between adjacent devices and the coupling is generated through the interaction of copper wires connected in the PCB. The R_{cdcp} changes when the distance or position of the devices are changed. Therefore, the thermal coupling

resistance depends on the locations of the devices, the length of the copper circuit (spacing between adjacent devices), etc [18].

Erik et al. firstly optimized the two-dimensional temperature distribution map by device case temperature and then based on the thermal map to optimize the device positions and device spacing and finally the structural optimization of the power converter is realized [57]. The conduction thermal coupling effect between adjacent devices is considered, while it ignores the convection thermal coupling between adjacent devices when the device dissipates thermal to the surrounding air. As the small thickness of copper wire for multiple devices connected by copper wire in the PCB, a considerable part of the thermal is transferred to the air domain in the power converter by convection. Due to the limited space and small device spacing, the thermal will be coupled to each other in the surrounding air, forming convection thermal coupling effect. Convection coupling is dependent on environmental factors and is not constant under different loads and the convection thermal coupling between adjacent devices will be formed in the process of convection thermal dissipation. However, there is no method or standard to extract the convection thermal coupling effect/resistance in the device datasheet, and there are relatively few literatures to study the convection thermal coupling effect [58].

The calculation method of thermal coupling effect is complicated, and the means for calculation of the conduction thermal coupling in literatures is to use the linear superposition principle [59]. For two adjacent thermaling devices, only a certain loss P is applied to one device (device I), and the temperature rise of the non-power device (device II) is caused by conduction thermal coupling. Therefore, the conduction thermal coupling effect of device I to device II can be obtained, that is, the values of the conduction thermal coupling thermal resistance. Siliarly, the conduction thermal coupling effect of device II to device I can be obtained through the same method. Based on the principle of linear superposition, this method has certain limitations and is only applicable to linear relations [55, 59]. However, the actual thermal coupling effect contains non-linear convection terms [60]. If the superposition principle is still applied, some errors or wrong results will occur to a certain

extent [3].

2.2.3 R_{ca} and Ambient Temperatures

With regard to the analysis on the self-thermal resistance (case-to-ambient thermal resistance, R_{ca}) of the power devices, the measured values of R_{ca} in datasheet [61] show that the value will vary from the range of 190 ℃/W to 310 ℃/W [52] when the devices packaged with SO-8 with different forms of substrate（P-DSO-14-4 and P-TO252-3-1）insulate. Meanwhile, the manufacturer Infineon, has provided the variation curves for the junction-to-ambient thermal resistance (R_{ja}) packaged under the two conditions of natural convection and forced air cooling, which indicates that the R_{ca} is variable and the values depends on the package, working conditions and the boundary conditions. The existing literatures generally calculate the R_{ca} under one working condition and barely analyze the variation under different working conditions.

Furthermore, the existing thermal analysis models are always established based on a fixed ambient temperature, such as 25 ℃ [62], while as a matter of fact the environmental profile could be diversified. The temperature is different at the different time in one day and different seasons [63, 64]. The convection thermal coupling effect between the adjacent semiconductor devices are reliable to the environment temperature so that the junction temperature will be changed as well. On the contrary, the convection thermal coupling will influence the temperature distribution and the junction temperature. The traditional thermal analysis model does not consider the variable ambient temperature [59].

The calculation formula of junction temperature is derived in [62] which considering the conduction thermal coupling effect, while the calculation formula is based on a fixed ambient temperature and the analysis is based on the ideal air region where the parameters are independent to the temperature while the ambient temperatures are not constant and the parameters are ambient temperatures dependent.

The short-term and long-term electro-thermal models are analyzed in [64], and the long-

term one is considered to be affected by the ambient temperature. The junction and case temperatures of power devices are estimated by the models. The device model estimates the voltage-drop and switching energy of the device by considering the current, the blocking voltage of the off-state and the junction temperature change. The thermal models consider the conduction thermal coupling between MOSFETs and diodes integrated in the same package, and the effect of the junction temperature of devices at the ambient temperatures of 25 ℃ and 30 ℃. In this paper, it is pointed out that different ambient temperature has an influence on the thermal coupling and the junction temperature, while only two ambient temperature points are considered, and the thermal model is only for one power device.

In [28], a dynamic ambient profile is analyzed, and a thermal analysis model based on the profile is established. As the power devices are located in the outdoor environment and the ambient temperature is not constant as discussed in [65], the thermal coupling effect among power devices in the system is not considered [66].

2.3 Research Gap/Problems

Through the thermal analyses of the literature on power devices at home and abroad, the challenges and problems are:

Self-thermal resistance (case-to-ambient) is dependent on environmental factors, when the convection coefficient changes, the thermal resistance will also change. The existing models only calculate the self-thermal resistance under a single working condition, without considering the change of self-thermal resistance under different working conditions or boundary conditions.

When the distance/spacing between adjacent devices changes, the thermal coupling resistance will change, no matter the multiple devices connected in a PCB through copper wires or multiple power modules/devices on the same heatsink. Therefore, the coupling thermal resistance/thermal coupling effect is dependent on the device spacing, while the existing models rarely analyze the relationship between device spacing and thermal coupling.

The non-uniform distribution of the device case temperature is easy to cause the

influence of thermal coupling between adjacent devices and the concentration of thermal stress in the converter system [67]. And the device spacing and working currents will affect the thermal coupling between adjacent devices, and then affect the case temperature or junction temperature of the devices. Through the relationship between the self-thermal resistance and the coupling thermal resistance between adjacent devices, the thermal distribution uniformity can be satisfied, that is, the case temperature/junction temperature of the devices can work at a certain temperature value or a value range through better understanding of the thermal coupling effect between devices under different working conditions. While this is rarely studied in the literatures.

The existing thermal analysis models of semiconductor devices are usually based on a fixed ambient temperature, while there are few kinds of literatures on different environmental ambient profiles. The convection thermal coupling effect between adjacent semiconductor devices depends on the ambient temperature, which leads to the change of thermal coupling effect and device junction temperature. In addition, the convection thermal coupling which caused by air convection will also have a certain impact on the device temperature rise. However, the existing thermal analysis models rarely analyze the effect of convection thermal coupling.

At present, the studies on the thermal model of power devices are largely device level and mostly on thermal conduction that based on a single device or a module. Moreover, the established thermal coupling mostly just considers the multiple chips inside of a single module, which ignores the conduction coupling between power devices or modules in a power converter system.

Chapter 3 Modeling and Analysis of Thermal Resistances and Thermal Coupling Between Power Devices

Reliability, cost, and power density are some of the major factors in the design of a power converter [68], where thermal management and design play important roles [27]. According to the analysis in Section 1.1, one of the major faults in power converters is temperature related. The recent trend in the design of the high-power density [29] and compact [69] power converter generally reduces the rate of the device cooling process. As a result, an increased thermal coupling among devices exists. The thermal dissipation, as shown in Figure 1.8 in Section 1.2, thermal dissipation has a negative impact on the performance and life of semiconductor devices and power converters. Hence for high-power density and compact converters, an optimum solution is sought for the thermal management of power devices under different loading conditions [32]. However, the dimensions of traditional Si-based devices approach their fundamental limits, it is difficult to increase the power by improving the structures of the power devices [31]. Although the research and development of the new materials such as silicon carbide (SiC), gallium nitride (GaN) and other semiconductor devices are developing rapidly, the current cost is relatively high . For the traditional silicon devices, the devices themselves and their application are very mature which will still have strong markets and application advantages. Therefore, a better understanding of thermal resistances and good thermal management of silicon-based power devices at different locations and currents facilitate better optimization [32].

To better analyze the thermal coupling effect between power devices, this chapter establishes the thermal coupling experiments of the power converter system, and the case temperature and temperature difference of devices under different spacing types and load current is analyzed. In addition, in order to meet the requirements of the uniformity of the device case temperature or junction temperature distribution for the power converter system, a thermal coupling testing platform for adjacent semiconductor devices is built.

Traditional thermal models do not consider the changes of R_{ca} and also ignore the effect

of thermal coupling among the adjacent devices. Compared with these models, the proposed thermal resistances modeling approach provides a better understanding of the thermal behavior of power devices. It is helpful for the scheme design of thermal dissipation system (the heatsink selection), the optimization of printed circuit board (PCB) and the design of better power converters [27, 57, 70]. In addition, this chapter is based on the research of establishing the calculation method of thermal coupling effect by the experiments and the measured data. Experiments based analysis method also was adopted by L. mucchi et al [71].

3.1 Single testing analysis of power devices

3.1.1 Relationships between T_c and T_j

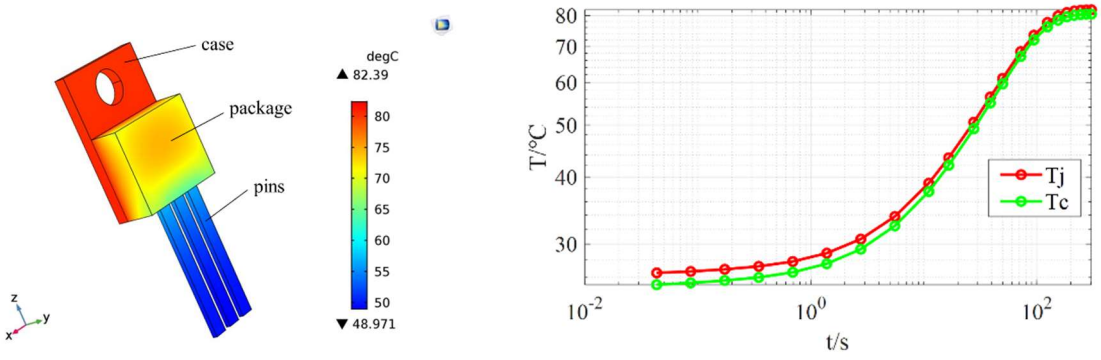
For MOSFET, diode and other semiconductor devices the structure is small and complex, so it is relatively difficult to measure the junction temperature [72]. It is easy to destroy the structure of the device when it is unpacked testing [73], and the actual themal transfering mode will be changed to make errors of the measurement results. The case temperature (T_c) of the devices is one of the important parameters reflecting the semiconductor performance, and it is also an important technical parameter for heatsinks selection. It can reflect the trend of the temperature change and realize the prediction of the T_j of the device through the corresponding thermal calculation method [74]. The themal calculation equation of the T_j and T_c can be expressed as

$$T_j = P_{loss} \cdot R_{jc} + T_c \qquad (3.1)$$

where P_{loss} is the power loss of the power device, T_c is the case temperature of device, R_{jc} is the junction-to-case thermal resistance which is generally given in the datasheet provided by the manufacturer.

Fig. 3.1 shows the FEM themal model of MOSFET. As shown in Fig. 3.1 (a), different colours constitute the thermal map and this simulation can be used to obtain the junction temperature (T_j) and case temperature (T_c), and the temperature at the chip and copper substrate layer is the highest. Fig. 3.1 (b) is extracted by the simulation results to compare

the T_j and T_c.



(a) (b)

Fig. 3.1: FEM thermal analysis model of MOSFET: (a) three-dimensional thermal calculation model; (b) T_j (red solid line) and T_c (green solid line), where time coordinate is marked in the form of exponential.

COMSOL simulation software can be used to establish the three-dimensional model of devices and system. Based on the three-dimensional model, the corresponding thermal analysis and calculation of thermal conduction and convection can be carried out. In addition, some professional modeling softwares also have thermal analysis modules such as UG NX, etc., which can realize the three-dimensional modeling and carry out some columns of FEM analysis on the established model. In this section, the power device model is established by UG NX and imported into COMSOL through the corresponding interface, and then a series of initial conditions and boundary conditions will be set: the initial T_a is 25 °C, and a certain power loss will be applied into the thermal source (1.2 W is set in the proposed thermal model). The boundary conditions are as follows: 1) the packed side is considered to be insulated; 2) all thermal will flow from the copper substrate (case) and pins into the surrounding air; 3) the thermal transfering mode is thermal conduction and natural convection. Probes are added at the key points to extract and compare the device temperature. The simulation runs for 1000 seconds until the device temperature reaches a stable state for a certain time.

The thermal transfering mode of the chip and the substrate is metal thermal conduction.

The temperature distribution and the comparison between the T_j and T_c of the device in Fig. 4.8 show that as the high thermal conduction coefficient and the fast temperature transfering speed of the metal, the temperature of the two structural layers is the highest. The T_j and T_c have the same rising trend from transient state to steady-state, and the temperature difference is only about 1.4 ℃ under the power loss of 1.2 W. This shows that the temperature characteristics of the packaged semiconductor devices can be characterized by collecting and analyzing the T_c. Therefore, in the device temperature testing, the temperature characteristics can be reflected by measuring the T_c, and then the T_j of the device can be estimated by the T_c. The thermal model can also be used in other TO-220 packaging devices, such as diodes.

3.1.2 Single testing of power devices

The single test of semiconductor is to supply power to a single device directly through a controllable current source, and the temperature rise of the device is realized by changing the size of the current source. In order to avoid the interference of other devices, the single testing only has a single semiconductor device, which is connected to the circuit in on-state mode without other components. For the MOSFET used in the testing, it should be noted that the initial condition is that the MOSFET can be turned on only after the PN junction of the gate-source electrode is activated by a certain voltage driving signal. Generally, a voltage of 5 ~ 15 V can be selected for the driving, but the smaller the driving voltage, the greater the on internal resistance (R_{DS}) corresponding to MOSFET [75]. In this section, a 15 V DC voltage source is selected as the driving signal. The voltage drop at both ends of the diode is collected by a digital multimeter. The working current of MOSFET and diode is monitored by the current sensor. The single testing circuit is shown in Fig. 3.2.

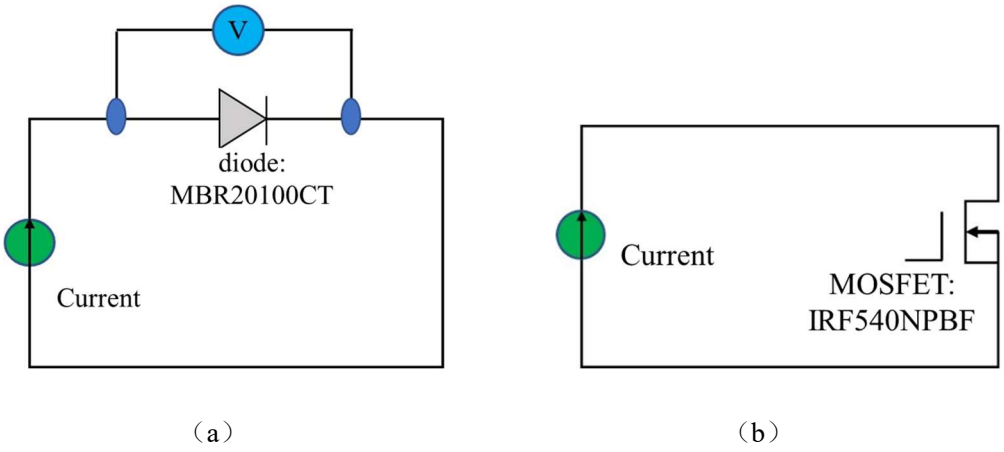


Fig. 3.2: Single testing circuit diagram of power devicse: (a) for diode; (b) for MOSFET.

There are two methods to realize the temperature rise of the power devices. The first one is based on different driving forms and switching frequencies to collect the switching loss, on-state loss, and other power losses of each device when the converter system is working. All power losses will be transferred in the form of thermal and then transferred in the device and the surrounding air, causing the temperature of the case/junction temperature to rise from ambient temperature (T_a) and finally reach a stable state . The second method is to make the device working under the on-state mode. When the device switches on, a certain loss can be generated, which will increase the case temperature. In this case, the loss of the device is only the on-state loss. As discussed in [76] and [77], a controlled current source or a given power loss can increase the temperature of the device [76, 78], regardless of the types of the power loss. Based on the above analysis, the second method is employed in this study to establish the thermal coupling testing platform for the single measurement and the thermal coupling measurement.

3.1.3 Losses calculation

Power loss is considered to be the main cause of thermal generation in semiconductor devices [79, 80]. In the single device testing in Section 3.1.2, the power device is in the on the state, and the temperature-rise of the device mainly comes from the on state loss [33], and its power loss can be calculated by (3.2) [33].

$$P_M = I^2 \cdot R_{DS} \quad (3.2)$$

where P_M is the power loss and I is the working current. R_{DS} is the on-state resistance of MOSFET, which is dependent on the T_j [127]. The relationship between R_{DS} and T_j is always given by manufacturers, as shown in Fig. 3.3. According to the relationship, the values of R_{DS} at different temperatures (as shown in Table 3.1) can be obtained, and then the losses of MOSFET devices can be calculated.

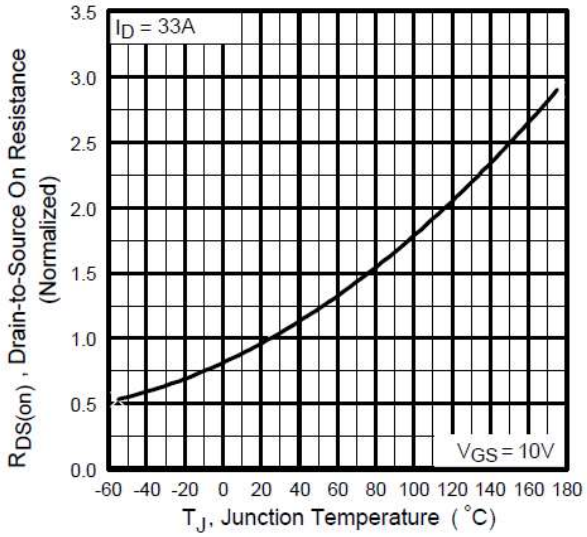


Fig. 3.3: The relationship between R_{DS} and T_j.

There is no reverse recovery loss for the diode in the on-state, and the power loss of the diode is mainly the on-state loss. Therefore, the loss can be expressed by

$$P_D = V_{fd} \cdot I \quad (3.3)$$

where V_{fd} is the forward voltage drop at both ends of the diode, and I is the current flowing through the diode pin.

By bring the T_c of MOSFET and diode collected from the single device testing of semiconductor devices into (3.2) and (3.3), the power losses under different operating currents can be obtained, as shown in Tables 3.1 and 3.2 respectively.

Table 3.1: The values of T_c, R_{DS} and P_M for MOSFET.

I / A	T_{c_M} / ℃	R_{DS} / mΩ	P_M / W
1	25.75	44	0.044
2	34.43	46.64	0.187
3	53.27	55	0.495
4	80.01	66	1.056
5	146.85	110	2.750

Table 3.2: The values of T_c, V_{fd} and P_D for diode.

I/A	T_{c_D}/℃	V_{fd}/V	P_D/W
1	50.66	0.46	0.46
2	79.59	0.50	1.00
3	105.85	0.51	1.53
4	129.26	0.51	2.04
5	149.19	0.51	2.55

3.2 Thermal Coupling Experiments and Requirements of Temperature Control for Power Converter Systems

3.2.1 Thermal Coupling Experiments

In this section, thermal coupling testing platform for the power converter is established as shown in Fig. 3.4, and its circuit diagram is shown in Fig. 3.5.

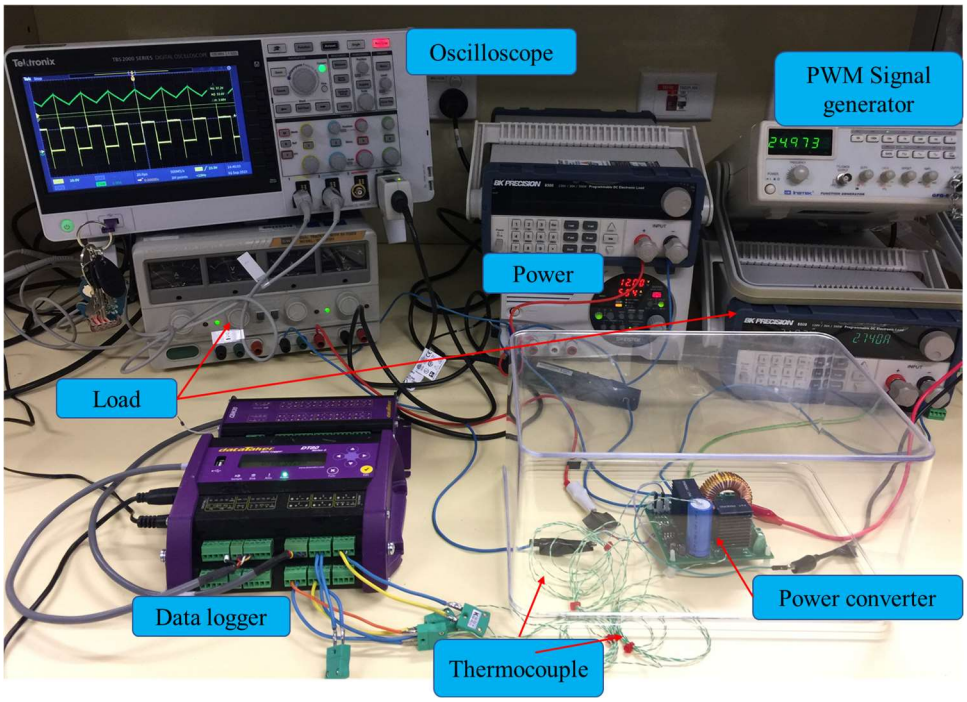


Fig. 3.4: Thermal coupling testing platform of power converter.

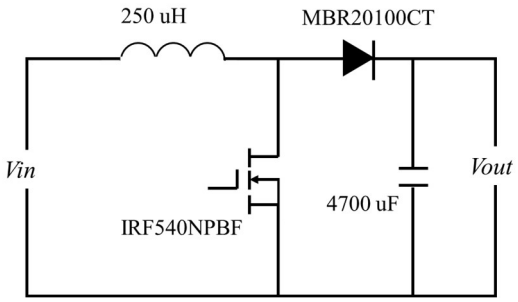
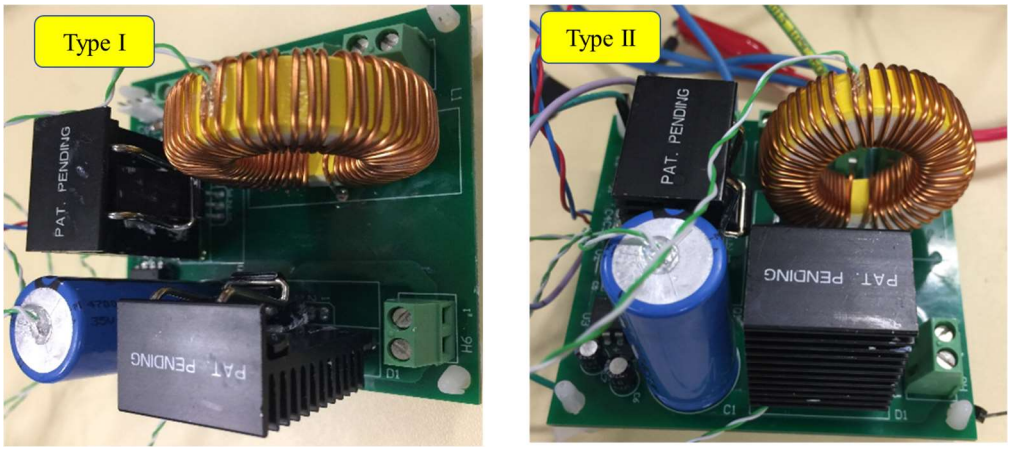


Fig. 3.5: The circuit diagram of power converter.

In this platform, the selected switching frequency of power converter is commonly used, which is 10 kHz, 25 kHz and 50 kHz, respectively. The duty cycle is set to 0.5, and the load resistance is 8 Ω, 6 Ω and 5 Ω, respectively. The type of MOSFET is IRF540 NPBF, the diode model is MBR20100CT, and the semiconductor devices are in TO-220 package. The capacitor is MAL215050472E3-35 V and the value of its capacitance is 4700 UF. The inductance is MCAP115018047A and the value of its inductance is 250 uH. In order to study the influence of device spacing and thermal coupling effect of adjacent devices on the

junction temperatures under different working conditions, two different types of power converters are tested and compared: type I with large device spacing and type II with small device spacing, as shown in Fig. 3.6.



（a） （b）

Fig. 3.6: Two types of power converters: (a) Type I with large device spacing; (b) Type II with small device spacing.

The power converter system is tested in this section. The MOSFET is controlled by PWM wave and its on-state and off-state are controlled by the given duty cycle and switching frequency. During the testing of the converter system, the input voltage and output voltage of the circuit are 12 V and 24 V, respectively. The case temperature of the power devices of the converter system are collected by changing the load resistances.

Fig. 3.7 shows the measurement results of case temperature and the calculation results of the temperature difference of the devices with different types of spacing. In this figure, the case temperature of MOSFET and diodes with two types of spacing (type I: large spacing, dot mark on the blue and cyan solid line; type II: small spacing, six-star mark on red and green solid line) are compared at the switching frequency of 25 kHz and the load resistance are 8 Ω, 6 Ω and 5 Ω, respectively.

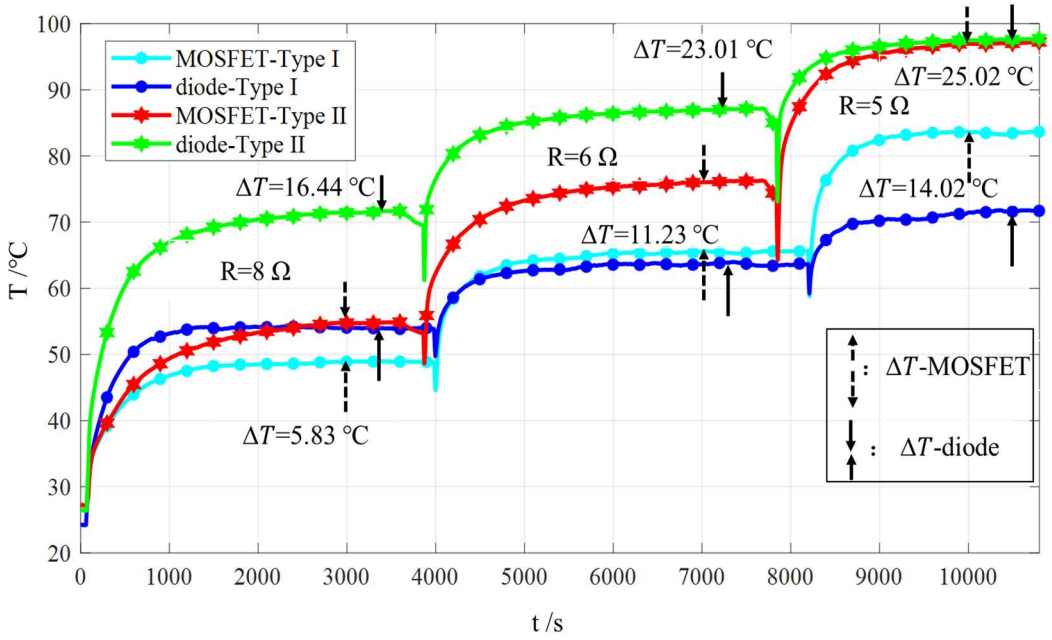


Fig. 3.7: Comparison of case temperature and the temperature difference of power devices with different spacing types.

It can be seen from the comparison results that, for both MOSFET and diode, with the decrease of device spacing the case temperature of the device increases under a same working condition. This shows that the thermal coupling effect between adjacent devices is affected by the device spacing, and with the decrease of the spacing the thermal coupling effect increases. In addition, according to the comparison results of case temperature difference in Table 3.3, we know that when the load resistance decreases, the current flowing through the semiconductor device increases. At this time, the case temperature difference of the two devices changes with the change of current, which shows that the thermal coupling effect between adjacent devices is affected by the working current, and with the increase of the current the thermal coupling effect increases. It is verified that the thermal coupling effect obtained from the thermal coupling testing platform (only the MOSFET and diode are tested) of devices can also be applied to the case where multiple devices exist in the power converter system.

Table 3.3: Temperature difference of case temperature under different load resistances.

$R/\ \Omega$	8	6	5
ΔT_{c_M} / ℃	5.83	11.23	14.02
ΔT_{c_D} / ℃	16.44	23.01	25.02

3.2.2 Temperature Controling Requirements of Power Converter System

There are two important considerations in the converter design phase to ensure the reliable operation of the converter [81, 82]: (1) Maximum junction temperature T_j of the devices, e.g., Si-based devices, cannot exceed the maximum T_j (T_{jmax}) 175 °C [24, 83]. We usually make the devices working around the temperature of 150 ℃ to ensure the devices working in safe operation; and (2) the ability to share thermal among the components with a more uniform temperature distribution [18, 70]. As discussed in [57] the optimal temperature range of the silicon semiconductor devices are about 110 ℃.

As discussed, the thermal dissipation between power devices slows down with the decrease of devices spacing, which result in the temperature increasing of the power converter. Fig. 3.8 describes six cases of thermal maps in UTS Tech lab, where Fig. 3.8 (f) shows the best thermal profile for converter design and operation. Followed by Fig. 3.8 (c), while in the operation of other systems, the temperature distribution peaks locally, and the high-temperature devices have serious impact on the thermal coupling of the low-temperature devices, which will affect the thermal distribution of the overall performance of the system [84]. This means it is desirable to control the temperatures at junctions to operate the power devices at good temperature ranges within the safety operation region even in the worst-case scenario. The methods for controling the case temperature or junction temperature can be by controlling the circuit, then the temperatures can be changed under different power losses, or by adjusting parameters of the drive circuit [85].

In this chapter, based on the fact that in the desigh stage when the heatsinks of the

devices are not selected, the self-thermal resistances are variable; and when the position of the devices and the device spacing are not determined, the coupling thermal resistances are also variable. Thermal coupling resistances analysis among the components can help with the thermal distribution, and by establishing the corresponding thermal resistances network model to analyze the relationships between the variable thermal resistances, the junction pr case temperatures can be controlled.

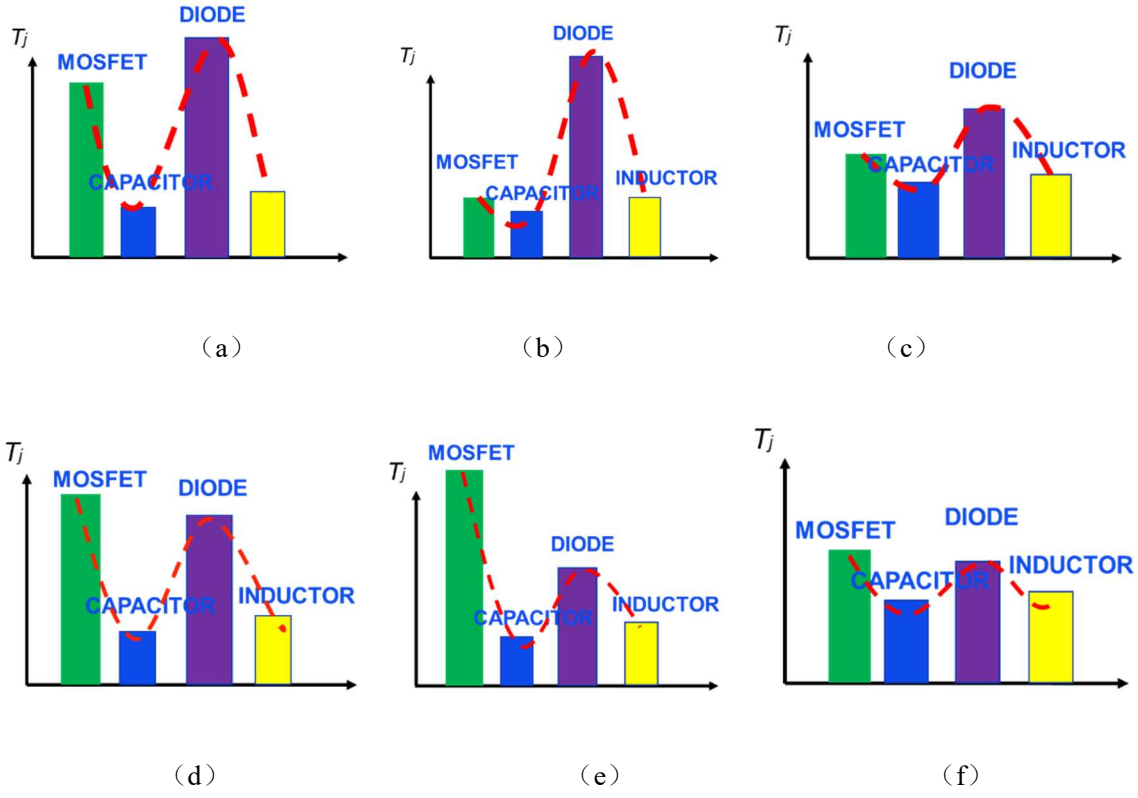


Fig. 3.8: Thermal maps of a basic boost DC-DC converter in six cases:(a) MOSFET and diode are with higher case temperature, and the diode is with the highest case temperature; (b) the diode is with the highest case temperature; (c) the temperature distribution is relatively smooth, and the diode is with the higher case temperature; (d) MOSFET and diode are with higher case temperature, and MOSFET is with the highest case temperature; (E) MOSFET is with the highest case temperature; (f) the temperature distribution is relatively smooth, and MOSFET is with the higher case temperature.

3.3 Thermal Coupling Testing Analysis of Power Devices

In the design stage, the thermal coupling effect between adjacent power devices, including the conduction thermal coupling effect and the convection thermal coupling effect, is further analyzed and calculated at fixed values of case temperature (T_c) of the devices. It is divided into two steps:

1) the thermal coupling network (TCRN) model between adjacent devices is established, and the the case-to-ambient thermal resistance (R_{ca}) and coupling thermal resistance (R_{cp}) are analyzed under different working conditions.

2) the relationships between individual Rca and their R_{cp} to the adjacent device have been obtained for different spacing and load currents during the design phase consideration.

Based on the two steps above, the themal coupling effect can be obtained. New T_c data from the calculation and measurement, which employs different spacing verifies the proposed thermal model and the relationships. The error analysis verifies the correctness and validity of the calculation method of thermal coupling effect between power devices under the fixed case temperature.

3.3.1 Thermal Coupling Testing of Adjacent Devices

The temperatures of the devices are affected by the thermal coupling, which includes conduction and convection coupling. As discussesd in Section 3.2.2, temperatues should be controlled in some fixed values to make the converter work in a good performance. In order to better analyze the thermal coupling effect and its influencing factors, a thermal coupling measurement platform for power devices is established, as shown in Fig. 3.9.

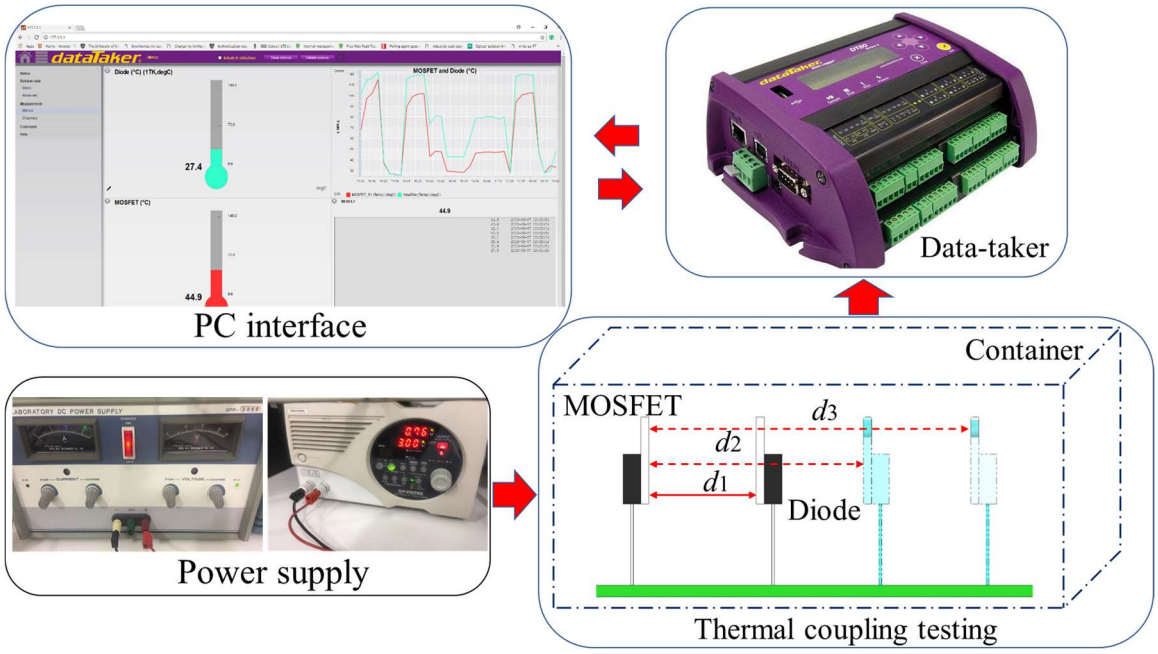


Fig. 3.9: Thermal coupling measurement platform.

Fig. 3.9 shows the thermal coupling measurement platform to test two identical types of MOSFET (IRF540N) and diode (MBR20100CT) which are the same ones as shown in the single measurements. The energy source is a current-controlled power supply and the two devices are connected in series. The devices are in the fully on-state and a digital multimeter is used to measure the voltage drop of the diode.

In the application of the power converters, heatsinks are employed for thermaling devices to transfer thermal effectively and the thermal dissipation capability, size, and installation location need to be considered. Hence in a converter, spacing should be given between the components to avoid installation interference. In the design of the platform, the spacing between two devices started from d = 12 mm, and was followed by d = 18 mm and d = 22 mm.

In this platform, T_c starts from the ambient temperature (T_a) and collects every 2 seconds until the temperature reaches a relatively steady level before the next load current values. In the steady state, it takes a longer time to obtain Tc when the magnitude of the current becomes larger. Therefore, to get a relatively stable Tc, the duration of testing should be

increased by increasing the operating current. For all measurements at different spacings, the total testing time is 3500 s. All the collected Tc data are recorded through a thermal datalogger (DT 80) and the values are verified by an infrared camera. Under the working condition of d = 18 mm and I = 3 A, the steady-state case temperatures for the diode ($T_{c\text{-}D}$) are 108.42℃ (collected by the datalogger) and 108.0 ℃ (taken by the infrared camera, as shown in Fig. 3.10), respectively. The error between the two methods is 0.39% which shows good accuracy.

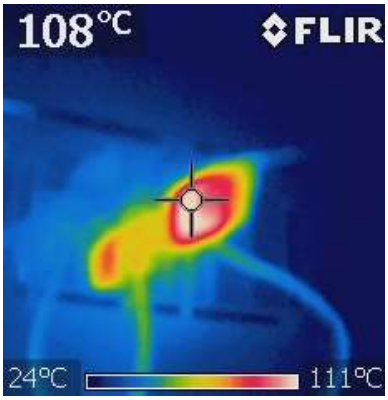
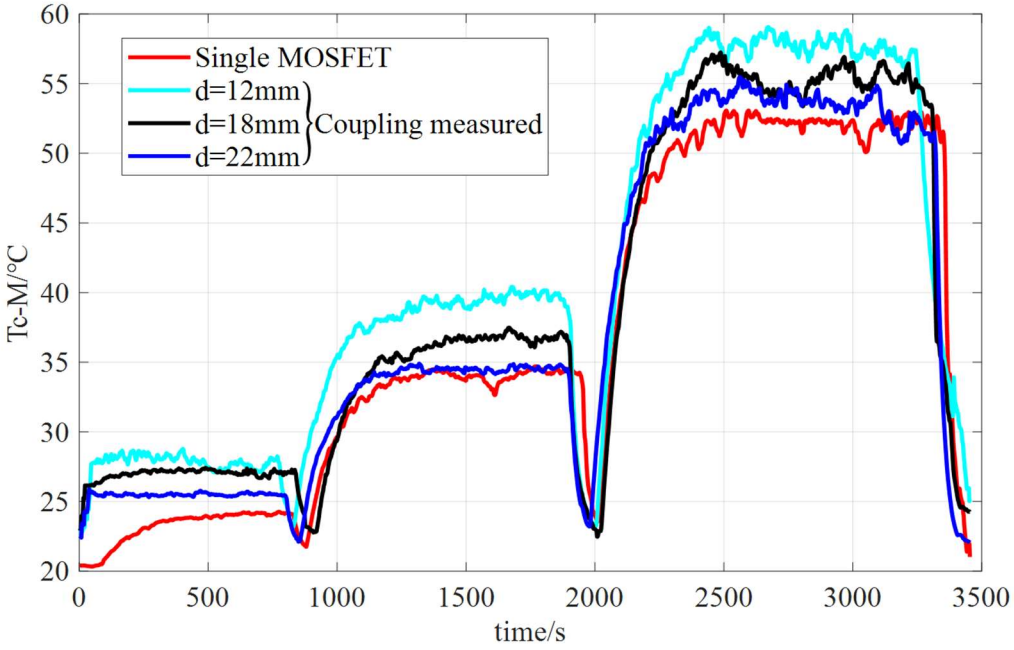


Fig. 3.10: T_c taken by the infrared camera.

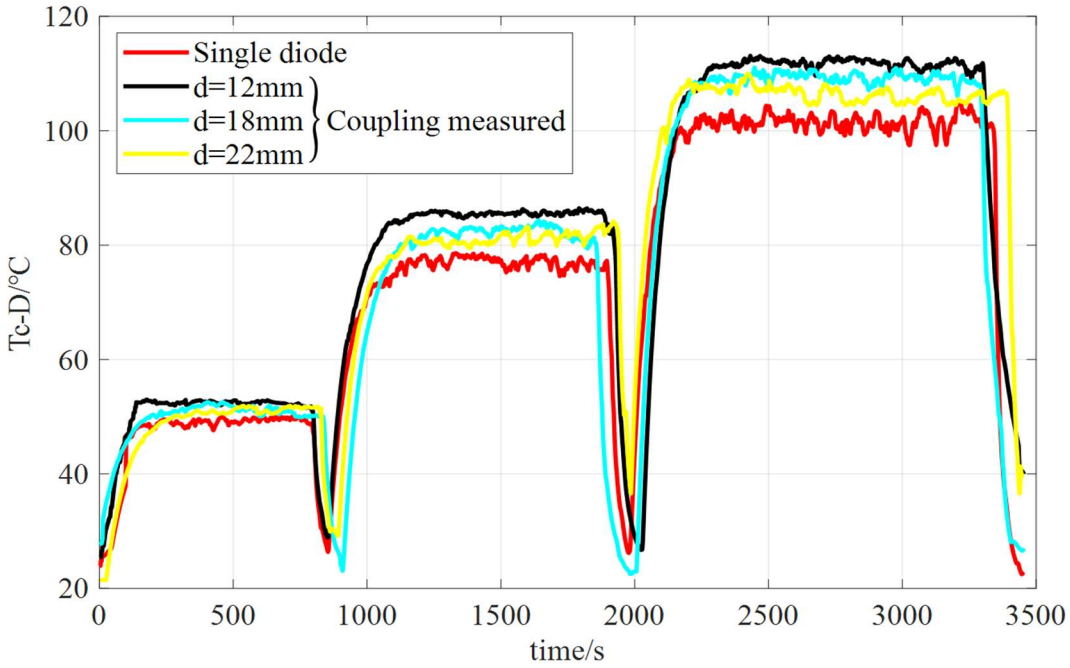
Under different working currents, the comparisons of T_c obtained by the testing of individual devices and thermal coupling at different spacings are given in Fig. 3.11, in which the red solid line is the case temperature of the devices collected in the single testing platform in Section 3.1.2 and other color solid lines are the temperatures collected from the thermal coupling measurement platform. It is observed from the measurement results that:

I) T_c rises rapidly from T_a for the MOSFET and diode and the rate of temperature-rise decreases near the steady-state.

II) T_c shows the lowest value when a single device is tested. T_c is higher when the spacing between two devices decreases.



(a)



(b)

Fig. 3.11: The comparison of T_c. (a) is for MOSFET; (b) is for diode.

3.3.2 Calculation of Self-thermal Resistance

In self-thermal resistance, R_{jc} depends on metal thermal conduction, and the values are generally given in the datasheet provided by the manufacturers. The maximum R_{jc} of MOSFET (IRF540NPBF) is 1.15 ℃ / W, and that of diode (MBR20100CT) is 2.0 ℃ / W.

Convection thermal transfer is the thermal transfer between fluid and solid wall, which depends on the movement of fluid to transfer the thermal [3]. Therefore, convection thermal transfer is closely related to the flow conditions and density of the fluid. As shown in Fig. 3.12, the convection thermal transfer of the same device is different when it is located at different hot surfaces.

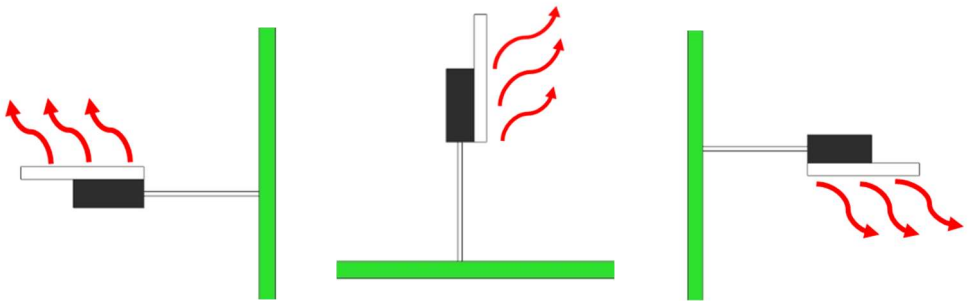


Fig. 3.12: Different positions of hot surface. (a) the hot surface is upward; (b) the hot surface is vertical; (c) the hot surface is downward.

The convection thermal dissipation is affected by the power losses and device thermal dissipation conditions. Its corresponding case-to-air thermal resistance (R_{ca}) is usually not provided in the device datasheet and the values of R_{ca} mainly depends on factors such as environment and package structure [86], which can be defined as:

$$R_{ca} = \frac{1}{hA} \tag{3.3}$$

where A is the convection thermal transfer area and h is the convection thermal transfer coefficient [87].

The value of h is related to many factors in the process of convection thermal transfer. It not only depends on the physical properties of the fluid, but also depends on the shape, size, and arrangement of the thermal exchange contact surface, and also has a close relationship with the flow velocity of the fluid. The values of some commonly used coefficients are shown in Table 4.8.

Table 3.4: Value range of convection thermal transfer coefficient h.

Types of convection thermal transfer	Convection thermal transfer coefficient h / [W/(m^2·K)]
Natural convection thermal transfer of air	1~10
Natural convection thermal transfer of water	100~1000
Forced convection thermal transfer of air	10~100
Forced convection thermal transfer of water	100~15000

Based on the analysis of [88] and [89], the convection thermal transfer coefficient can be expressed as follows

$$h \propto (\frac{\Delta T}{L})^{0.25} \tag{3.4}$$

where ΔT is the temperature difference between T_c and T_a, L is the vertical height of the contact surface.

When the type of the power device is selected, the thermal contact area A and the vertical height L of the contact surface are known constants, and it can be seen from (3.3) and (3.4) that the R_{ca} is a dependent on the temperature difference ΔT. In addition, when the power loss changes, the T_c of the device will also be changed, and the corresponding convection thermal resistance is also changed. Therefore, the R_{ca} is a function of temperature difference and power loss, that is

$$R_{ca} = f(\Delta T,\ P) \tag{3.5}$$

Based on the above analysis, the expression of the transient thermal impedance Z_{ca} (t) and transient thermal capacity C_{ca} (t) can be obtained as follows:

$$\begin{cases} Z_{ca}(t) = \dfrac{\Delta T(t)}{P} \\ C_{ca}(t) = \rho c_p(t) l A \end{cases} \tag{3.6}$$

In addition, according to [86] and [90], the calculation formula of steady-state R_{ca} in convection thermal transfer is obtained as

$$R_{ca} = \frac{\Delta T}{P} \tag{3.7}$$

In this study, the steady-state thermal resistance of devices under different working conditions is analyzed. By bring the measured steady-state T_c into (3.7), the R_{ca} of MOSFET and diode can be obtained. The calculation results are shown in Tables 3.5 and 3.6 respectively.

According to the two tables above, when the power loss (working current) increases and the T_c rises, and the values of R_{ca} decreases. This shows that the R_{ca} is not constant, and its value depends on the power loss and environmental factors.

Table 3.5: Rca for MOSFET.

T_{c_M} [℃]	R_{ca_M} [℃/W]
25.75	69.32
34.43	62.73
53.27	61.76
80.01	54.27
146.85	45.15

Table 3.6: *R*ca for diode.

T_{c_D} [°C]	R_{ca_D} [°C/W]
50.66	60.39
79.59	58.89
105.85	54.35
129.26	52.24
149.19	49.60

3.3.3 Analysis of Variable Thermal Resistances

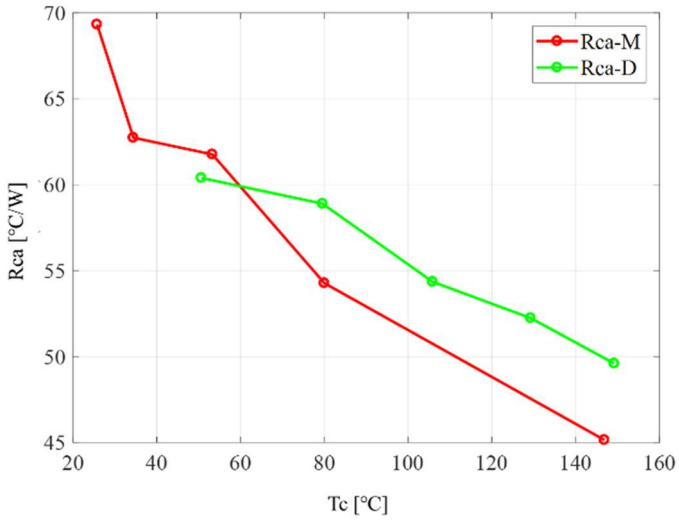
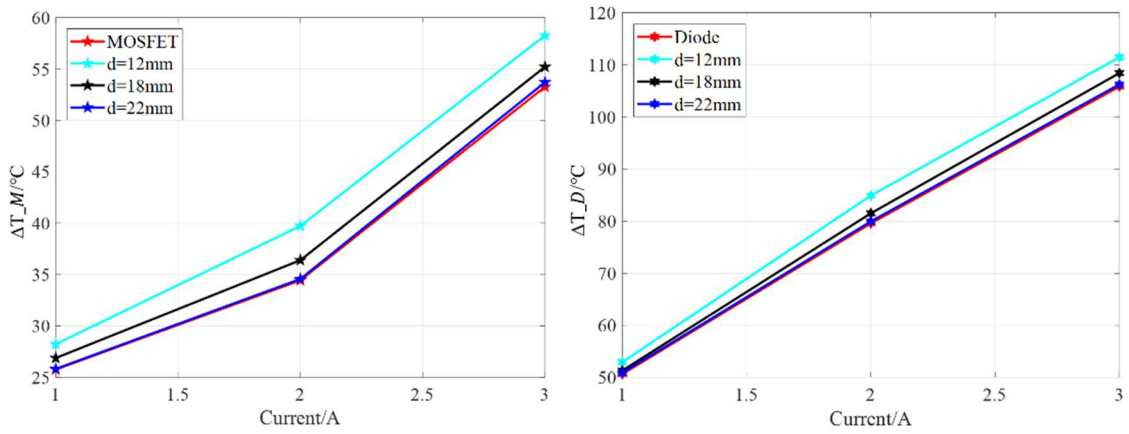


Fig. 3.13: Relationships between the resistances of case-to-ambient and case temperature (red solid line: MOSFET, green solid line: the diode).

From Section 3.3.2, the relationships between the resistances of case-to-ambient and case temperature can be obtained, as shown in Fig. 3.13. It can be seen from the figure that the convection thermal resistance (case-to-air thermal resistance) of the device is not constant under different working conditions [24]. When the loss changes, the case temperature of the

devices' changes, and the corresponding case-to-ambient thermal resistance also changes. That is, when the case temperature of the device increases, the case-to-ambient thermal resistance of MOSFET and diode decreases, and vice versa. This shows that the case-to-ambient thermal resistance depends on the power losses and the surrounding environment. In [24], Eduardo L et al. showed that case-to-ambient thermal resistance can be used to analyze the effects of different cooling technologies. Based on this, in the design stage of the power converters, it is necessary to have identification and analysis when considering widely available thermal dissipation solutions, and the selection of heatsinks can be assisted by the values of case-to-ambient thermal resistance.



（a） （b）

Fig. 3.14: T_c in steady state (red lines are from individual testing; other lines are from thermal mutual testing): (a) is for the MOSFET; (b) is for the diode.

In addition, Fig. 3.14 gives the comparisons of T_c between single devices testing and thermal coupling measurement at different separation distances between the power devices and different working currents. When the devices are individually tested, T_c in the steady state is lowest and when the devices are mutually tested, Tc for the MOSFET and the diode display increasing trends and the T_c increases in size with the reduction of the separation distances. The power losses of the devices are affected by the working currents, and all the losses will be converted into thermal. Under the same working current, the case temperature

of the devices changes obviously in the single testing and the thermal coupling measurement. Moreover, in the thermal coupling measurement, the temperature difference increases with the decrease of the device spacing. Therefore, there is a certain coupling effect between the power devices, and the values of the coupling thermal resistances are related to the device spacing and the working currents.

3.4 Thermal Coupling Resistances Network (TCRN) Modeling for Power Devices

In the design stage of a power converter system, the distances between the semiconductor devices and the type of heatsinks have not been determined yet. The distribution and the resistance values of the self resistances[91] and the thermal couping resistances of power devices can help the design.

The case temperature of the devices is an important parameter for heatsinks selection, and the case-to-ambient thermal resistances of the devices will be affected by the packaging, convection thermaling transfer coefficient, etc. which will have influence on the case temperature[18, 92]. The traditional models build the thermal resistance networks always based on the existing power converters. Contrary to the traditional models, the coupling thermal resistance network model built in this section based on the variable thermal resistances in the design stage of the power converters and the requirement of the uniform case temperature distribution of the devices. Based on these analyses, the case-to-ambient thermal resistances of power devices are variable, and the values of thermal case-to-ambient resistance for the heatsinks can be determined according to the values of the case-to-ambient resistances which can help the selection of the heatsinks [38]. In addition, the devices spacing and positions can be improved by changing the thermal coupling resistances. Although the semiconductor devices in this section are not equipped with heatsinks, the junction temperature of the devices under the maximum power losses are still lower than the maximum junction temperature by about 30 ℃, the devices used to establish the themal

model are safe enough.

3.4.1 TCRN Modeling

Based on the thermal resistance network proposed by Erik C. W. de Jong et al. in [18] and Yunyu Tang et al. in [52], a thermal coupling resistance network (TCRN) model of power devices is established, considering the case-to-ambiente thermal resistances and the thermal coupling effect between the multiple semiconductor devices under different working conditions, as shown in Fig. 3.15. The model established in this section is in the design stage, and in order to meet the requirements of uniform temperature distribution in the power converter, the case temperature of the devices is fixed.

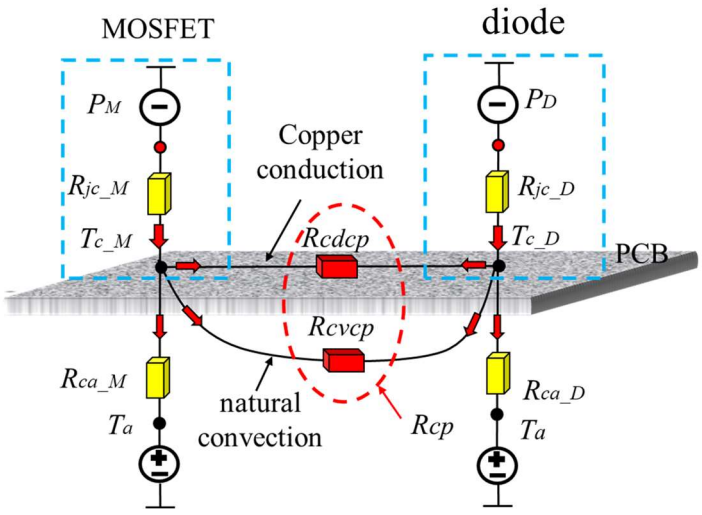


Fig. 3.15: TCRN model.

In the thermal resistance network, individual thermal resistances are in the vertical direction and thermal coupling resistances are in the horizontal direction. The self-thermal resistances (marked in yellow) mainly include junction-to-case thermal resistance (R_{jc}) and case-to-ambient thermal resistance (R_{ca}). The thermal coupling resistances R_{cp} between thermaling devices are mainly composed of: 1) the conduction thermal coupling resistance (R_{cdcp}), generated by the connected copper circuit in PCB between MOSFET and diode; 2)

the convection coupling thermal resistance (R_{cvcp}), generated by the surrounding air domain after the natural convection and thermal dissipation of the devices. P_M and P_D are the total power losses of MOSFET and the diode, respectively.

The temperature-rise of the devices can be obtained by (3.8), in which the total power loss of the diode is used to calculate the temperature-rise caused by adjacent devices. The calculation result by this method is higher than the actual situation, which can be used for the simplified thermal models.

In the actual process of thermal transfer, part of the power losses is used for its own temperature-rise, and part of the losses is used for the thermal coupling to make the adjacent device temperature-rise. Therefore, this section is based on Kirchhoff's current law (KCL) to calculate the case temperature and variable thermal resistances, as shown in (3.10).

$$D_{T\text{-}M} = (R_{jc\text{-}M} + R_{ca\text{-}M}) \cdot P_M + R_{cp} \cdot P_D \qquad (3.8)$$

where D_{T_M} is the temperature-rise of MOSFET, R_{jc_M}、R_{ca_M} is the junction-to-case thermal resistance and case-to-ambient thermal resistance of MOSFET, respectively. R_{CP} is the thermal coupling resistance between MOSFET and adjacent devices (for example the diode), P_M and P_D are the losses of MOSFET and diodes, respectively.

R_{cdcp} can be defined according to the method proposed in [18] and calculated by (3.9) .

$$R_{cdcp} = \frac{l}{\lambda A} \qquad (3.9)$$

where l is the length of copper traces, and the effective values of l with different connection modes of adjacent devices in PCB can also be calculated according to the method proposed in [18]. λ is the thermal conductivity, and A is the cross-sectional area.

In addition, in the TCRN model, the conduction and convection thermal coupling resistances are connected in parallel. Based on (3.10), the total thermal coupling resistance (R_{cp}) between adjacent semiconductor devices can be obtained, that is

$$\frac{1}{R_{cp}} = \frac{1}{R_{cdcp}} + \frac{1}{R_{cvcp}} \qquad (3.10)$$

where R_{cp} is the total coupling thermal resistances between adjacent devices, R_{cdcp} is the conduction thermal coupling resistance, R_{cvcp} is the convection thermal coupling resistance.

According to the TCRN model and KCL[93, 94], the relationships (as shown in Fig. 3.15) between P_{loss}, T_c and thermal resistances can be expressed as

$$\begin{cases} P_M = \dfrac{T_{c\text{-}M} - T_a}{R_{ca\text{-}M}} + \dfrac{T_{c\text{-}M} - T_{c\text{-}D}}{R_{cp}} \\ P_D = \dfrac{T_{c\text{-}D} - T_a}{R_{ca\text{-}M}} + \dfrac{T_{c\text{-}D} - T_{c\text{-}M}}{R_{cp}} \end{cases} \tag{3.11}$$

where, P_M is the power losses of MOSFET and P_D is the power losses of the diode. T_{c_M} is case temperature of MOSFET, T_{c_D} is case temperature of the diode. R_{ca_M} is the case-to-ambient thermal resistance for MOSFET, R_{ca_D} is the case-to-ambient thermal resistance for the diode.

The relationships between the thermal coupling resistances and the self-thermal resistances between the adjacent semiconductor devices can be obtained by (5.3), that is

$$R_{cp} = \frac{2\cdot(T_{c\text{-}D} - T_{c\text{-}M})}{(P_D - P_M) - \left(\dfrac{T_{c\text{-}D} - T_a}{R_{ca\text{-}D}} - \dfrac{T_{c\text{-}M} - T_a}{R_{ca\text{-}M}}\right)} = \frac{2\cdot\Delta T_c}{\Delta P_{loss} - \Delta\dfrac{T_c}{R_{ca}}} \tag{3.12}$$

The self-thermal resistance of the diode can be expressed as

$$R_{ca\text{-}D} = \frac{T_{c\text{-}D} - T_a}{(P_D + P_M) - \dfrac{T_{c\text{-}M} - T_a}{R_{ca\text{-}M}}} \tag{3.13}$$

where, ΔP_{loss} refers to the power losses difference of the power devices, $\Delta\frac{T_c}{R_{ca}}$ is the difference between the ratio of temperature and self-thermal resistance which can be expressed as

$$\Delta\frac{T_c}{R_{ca}} = \frac{T_{c\text{-}D} - T_a}{R_{ca\text{-}D}} - \frac{T_{c\text{-}M} - T_a}{R_{ca\text{-}M}} \tag{3.14}$$

3.4.2 Analysis of Key Influencing Factors

（1）Analysis of the self-thermal resistances

In the application of the converters, the heatsinks can effectively help the semiconductor devices to transfer thermal and play a role in reducing the junction temperature to protect the devices. For the structure of the heatsinks and the whole power converters, in addition to the thermal dissipation capacity or coefficient, the size of the structure and installation position of the heatsinks should also be considered. The designer needs to make a reasonable selection of the heatsinks in the design stage to help the devices with good thermal dissipation. The value of the case-to-ambient thermal resistance is different in different heatsink applications. The designer can select the type of the heatsinks for the devices according to some standards or results [24]. Therefore, before the cooling scheme is given the corresponding case-to-ambient thermal resistances are variable. In addition, in some applications, such as air-cooled or water-cooled cooling system, when the speed of the fan or the flow rate of cooling water changes, the corresponding case-to-ambient thermal resistance will also change. According to the relationships between the variable thermal resistances proposed in this paper, we can get the recommended valuse of case-to-ambient thermal resistances, and then we can choose the appropriate cooling schemes of power devices through the recommended values.

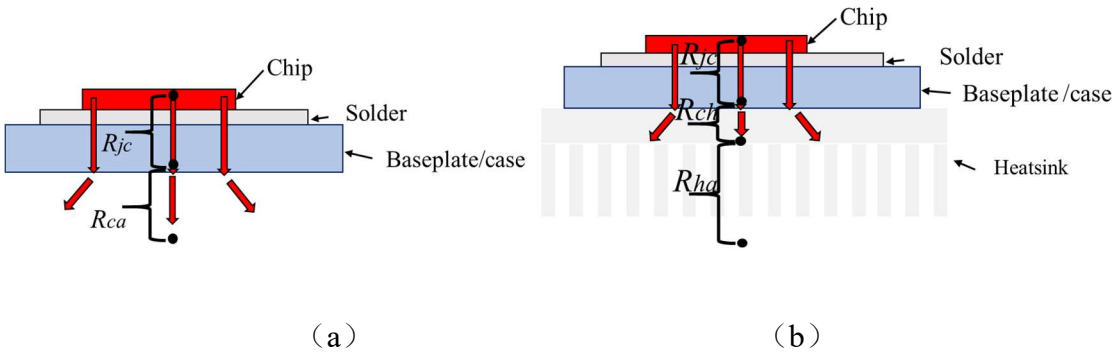


Fig. 3.16: The structure of power devices and the self-thermal resistance distribution.

(a) without a heatsink; (b) with a heatsink.

Fig. 3.16 shows the simplified structure of the power devices. The device shown in Fig. 3.16 (a) is not equipped with a heatsink, and its convection thermal resistance is the case-to-ambient thermal resistance. Ignore the thermal resistances generated by the structural layers such as solder layer and the silicone grease layer. If a heatsink is installed on the power device, the thermal resistance of the heatsink will be generated between the junction-to-case thermal resistance (R_{jc}) and the case-to-ambient thermal resistance (R_{ca}), as shown in Fig. 3.16 (b), that is, the case-to-heatsink resistance (R_{ch}). At this point, the case-to-ambient thermal resistance will change into the heatsink-to-air thermal resistance (R_{ha}). Both case-to-ambient thermal resistance and heatsink-to-air thermal resistance belong to the convection thermal resistances. The R_{ca} or R_{ha} can help the analysis of convection thermal coupling. Better understanding of thermal coupling resistances on different working conditions can help the selection of heatsinks or establish the corresponding controling method of cooling system.

(2) Analysis of the ambient temperature (T_a)

Based on a certain ambient temperature (T_a), the junction temperature or case temperature of the power devices increases due to the power losses in the process of working operation. For the choosing of the ambient temperature used in the testing or measurement, there are two main methods which are

1) to collect the initial ambient temperature before the device is working, and the value is T_a.

2) to collect the ambient temperature of the devices when the temperature (junction temperature or case temperature) reaches the steady-state after the device is working, and the value is T_a'.

The ambient temperature collected by the two methods is different. As the junction temperature and case temperature of the device will increase after operation, the generated thermal diffuses into the surrounding air domain, and the surrounding ambient temperature increases during the thermal dissipation process. Therefore, the ambient temperature collected by the second method is higher than that of the first one. For power devices, the same power losses will make the devices have the same temperature rise, no matter which

method is selected, the junction temperature or case temperature of the devices after steady-state is stable in the same value. According to the steady-state R_{ca} calculation formula (3.7) in Section 3.3.2, in the first method, the temperature difference between the case and the ambient temperature is large, and the value of the corresponding thermal resistance is also large; in the second method, the temperature difference between the case and the ambient temperature is relatively small, and the value of the corresponding R_{ca} is also small. The thermal resistances network established by the two ambient temperature collection methods will get the same results of case temperature or junction temperature. The initial value of the Ta around the device is selected as the ambient temperature in this paper.

(3) Analysis of the electro-thermal [95] coupling of the power devices

In power converter applications, the electrical parameters of the device are depending on the temperature. As analyzed in Section 3.1.2, the R_{DS} will change with the change of temperature, which will influence the on-state loss and finally the junction temperature of the device will be affected. A real-time feedback model between the junction temperature or case temperature and the electrical parameters can help to make the analysis and calculation model more accurate. This paper focuses on the analysis of the thermal coupling effect between adjacent devices including the conduction and convection thermal coupling. And based on the network model proposed in this paper, an electro-thermal coupling feedback model can be added to make the model better for the converter real-time simulation.

（4）Case temperature of the power devices（T_c）

The case temperature of the devices is one important parameter which can reflect the performance of the devices. Based on the analysis of the self-thermal resistance in this section, the case-to-ambient thermal resistance of the device can be used to analyze the effect of different cooling technologies. In addition, according to the guidelines for the selection of heatsinks for power semiconductor devices (JB/T 9684-2000), the case temperature and case-to-ambient thermal resistance of the devices are helpful for the selection of heatsinks.

For a single power device, the case temperature can be calculated by (3.15); for multiple adjacent devices, due to the thermal coupling effect, the case temperature can be obtained by

(3.11) as shown in the thermal coupling resistance network model in Section 3.4.1.

$$T_c = T_a + P_{loss} \cdot R_{ca} \quad (3.15)$$

In the design stage of the converter, the cooling scheme and the distance between the devices are not given. That is, all the thermal resistances are variable. Based on the requirement of a more uniform thermal distribution of the multiple devices in the power converter system in Fig. 3.8, the relationships between the variable thermal resistances under different working conditions can be obtained by controlling the case temperature at a fixed value or narrow temperature range. The values of the thermal resistancex can be selected bythe relationships between the variable thermal resistances, and based on the proposed TCRN model the relationships can be used to assist designers to select the cooling schemes, devices location, and the device spacing. Based on the above analysis, it will be beneficial to the optimization of the power converter.

3.4.3 Losses of Power Devices

In a power converter, when MOSFET or the diode works, the device will generate power losses, and all the power losses will be transferred into the form of thermal. After that the device will be thermaled up. Based on this, any kind of power losses can make the junction temperature of the devices increase [76, 77]. This chapter analyzes the thermal transfer of devices in the on-state. Based on the losses calculation in Section 3.1.3, the losses of MOSFET and the diode under different working conditions can be obtained, as shown in Table 3.7.

Table 3.7: Parameters and losses of MOSFET and the diode.

I [A]	$T_{c\text{-}M}$ [°C]	R_{DS} [mΩ]	P_M [W]	$T_{c\text{-}D}$ [°C]	V_{fd} [V]	P_D [W]
1	25.75	44	0.044	50.66	0.46	0.46

2	34.43	46.64	0.187	79.59	0.50	1.00
3	53.27	55	0.495	105.85	0.51	1.53
4	80.01	66	1.056	129.26	0.51	2.04
5	146.85	110	2.750	149.19	0.51	2.55

3.5 Relationships Between Thermal Resistances and Analysis of the Thermal Coupling Effect

Based on the analysis in Section 3.4, there are multi-devices in a power converter, such as MOSFET, diode, capacitor, inductor, etc. For a power converter, the relatively stable or uniform temperature distribution and working in an area with the best performance is conducive to improving the reliability of the system [18, 70] for the whole converter. In order to make the temperature distribution of the system relatively smooth and avoid severe thermal coupling effect [18] or local thermal stress concentration on other devices, it is necessary to control the case temperature of the devices. The thermal distribution of six power converter systems are as shown in Fig. 3.8 in Section 3.2.

In the proposed TCRN model, the fixed case temperature can be understood as: controlling the case temperature of the devices fixing in a value or floating in a range of temperature range. In this section, the case temperature or junction temperature changes with the change of the ambient and working conditions, the fixed or relatively stable small range case temperature can be achieved by analyzing the relationships between the thermal resistances.

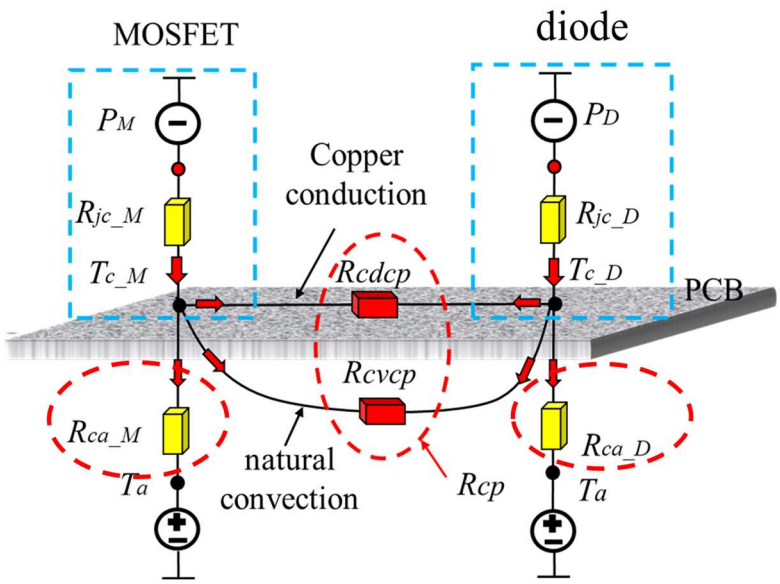


Fig. 3.17: Variable thermal resistances in the TCRN model.

As shown in Fig. 3.17, especially in the design stage, the distance between the cooling scheme and the power devices has not been given, that is the values of the thermal resistances are variable. When the case temperature of the devices is limited to a fixed value or a small range, there are many possible combinations of the variable thermal resistances (case-to-ambient thermal resistance and thermal coupling resistances) in the TCRN model of the adjacent devices. It can be seen from the analysis that:

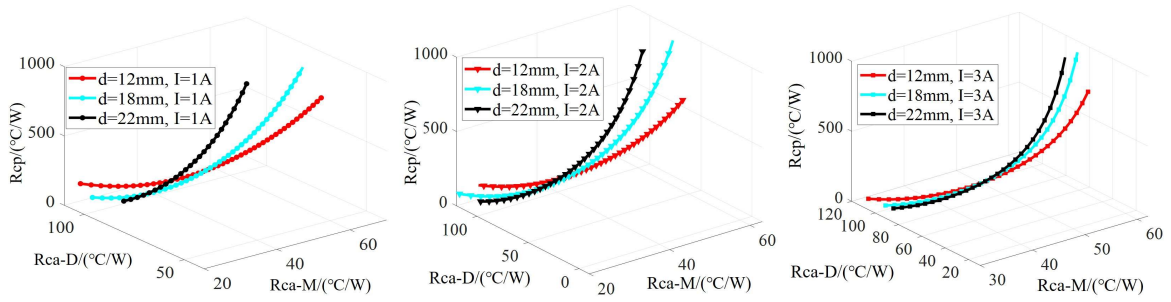
1) the change of self-thermal resistance can be realized by the change of thermal dissipation systems (heatsinks), such as the selection of different thermal dissipation types and different thermal dissipation coefficients.

2) the change of thermal coupling resistance can be realized by improving the device spacing and thermal dissipation environment (surrounding air domain). Therefore, this section is based on a fixed or a small range of the case temperature. In the proposed TCRN model, the relationships between the variable thermal resistances are established and finally, the thermal coupling effect between the devices under different working conditions is obtained.

3.5.1 Analysis of Thermal Coupling Effect Under Different Working Conditions

According to the TCRN model proposed in Section 3.4, bring the data of the case temperature (as shown in Fig. 3.11) obtained from the thermal coupling measuremnet into (3.11) - (3.14), then fix the case temperature and simulate with MATLAB to obtain the relationships between the variable thermal resistances, as shown in Fig. 3.18 and Fig. 3.19.

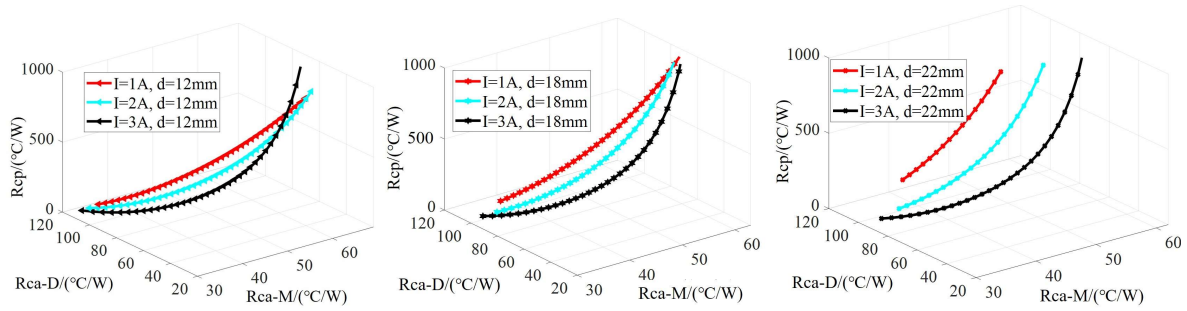
It is desirable to know the temperatures at the junctions (cases) in order to operate the power devices at a fixed value or narrow temperature range within the safety operation region even in the worst-case scenario. Especially, during the design phase consideration where the cooling schemes and the spacing between power devices have not been given. Therefore, the values of thermal resistances are variable. The relationships between thermal resistances at a fixed value of Tc can be given based on the TCRN model. The relationships are shown in Figs. 3.18 and 3.19, and the details are given in Table. IV, where “↑” represents increment, “↓” represents decrement and “-” represents constant/no change.



（a） （b） （c）

Fig. 3.18: Relationships between R_{cp} and R_{ca} at different spacing.

(a) working current is 1 A; (b) working current is 2 A; (c) working current is 3 A.



（a） （b） （c）

Fig. 3.19: Relationships between R_{cp} and R_{ca} with different operating currents. (a) device spacing is 12 mm; (b) device spacing is 18 mm; (c) device spacing is 22 mm.

The thermal coupling effect between devices can reflected by the coupling resistances. In order to analyze the variable thermal resistances and the thermal coupling effect between devices more clearly, the details of the relationships based on Figs. 3.18 and 3.19 are given in Table 3.8, where “↑” represents increment, “↓” represents decrement and “-” represents constant/no change.

Table 3.8: The Changes in Thermal Resistances and Thermal coupling effect.

d	I	$R_{ca\text{-}D}$	$R_{ca\text{-}M}$	R_{cp}	Thermal coupling effect
-	-	↑	↓	↓	↑
-	-	↓	↑	↑	↓
↑	-	-	↓	↑	↓
↓	-	-	↑	↓	↑
↑	-	↓	-	↑	↓
↓	-	↑	-	↓	↑

-	↑	-	↓	↓	↑
-	↓	-	↑	↑	↓
-	↑	↓	-	↓	↑
-	↓	↑	-	↑	↓

The relationships at the same spacing and current:

From the 3D views of Figs. 3.18 and 3.19 and Table. 3.8, the relationships between thermal resistances at the same spacing and under the same current can be given:

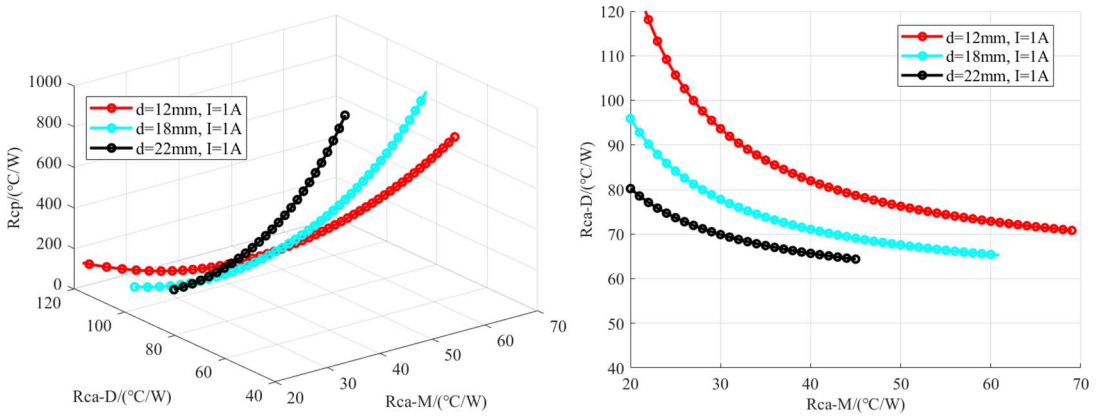
(I) $R_{ca\text{-}D}$ increases, $R_{ca\text{-}M}$ will decrease. That is the values of self-resistances $R_{ca\text{-}D}$ and $R_{ca\text{-}M}$ change in opposite direction.

(II) $R_{ca\text{-}D}$ increases, R_{cp} and $R_{ca\text{-}M}$ will decrease. It means the effect of thermal coupling will increase when the self-resistance of the diode (the device with the relatively higher temperature) increases and at the moment the self-resistance of MOSFET (the device with the relatively lower temperature) decreases; and vice versa.

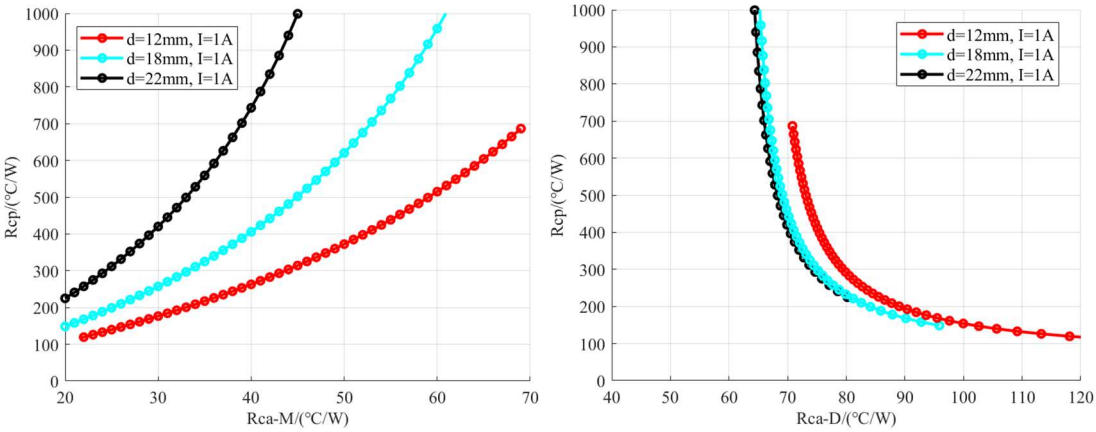
The values (domain) of resistances can be recommended by the relationships between thermal resistances which can help designers to choose the cooling schemes and spacing between components during the design phase consideration.

3.5.2 The Relationships at Different Spacing

In order to analyze the thermal coupling effect between devices under different device spacing more clearly, the relationships of variable thermal resistances can be obtained according to Fig. 3.18, as shown in Figs. 3.20-3.22, in which Figs. 3.20-3.22 (a) are the three-dimensional views, Figs. 3.20-3.22 (b), (c) and (d) are the projection views.

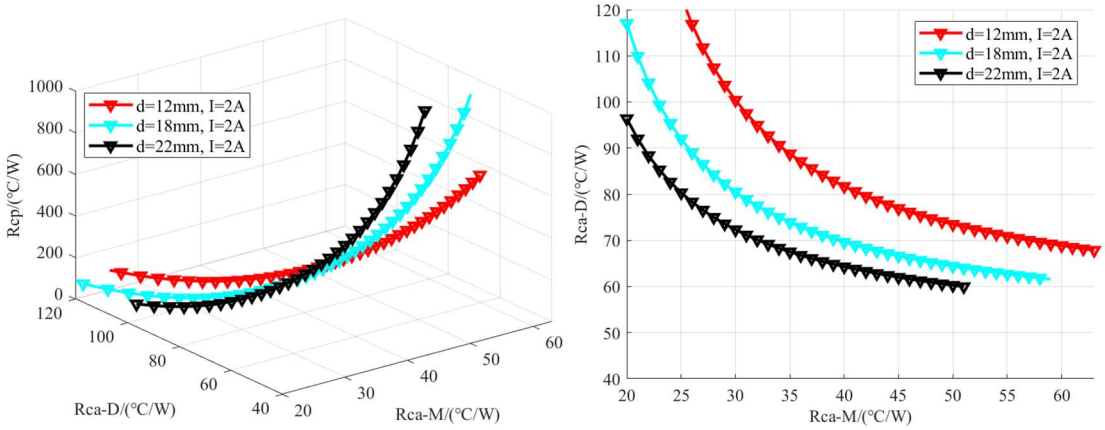


（a）　　（b）

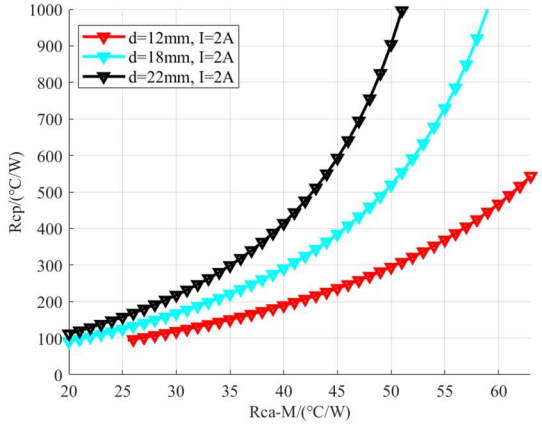


（c）　　（d）

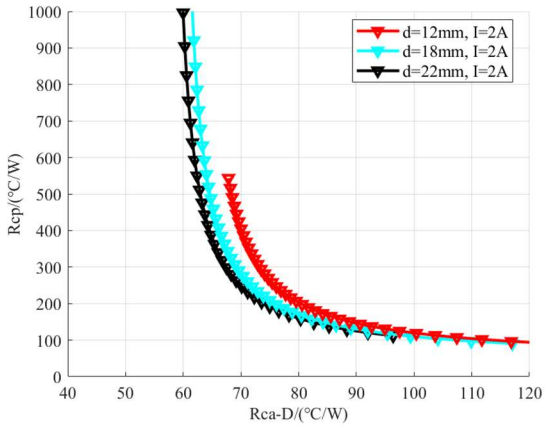
Fig. 3.20: Relashipns with different device spacing at I = 1 A.



（a）　　（b）

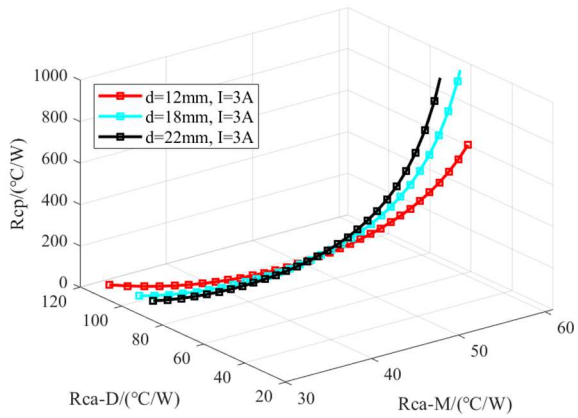


（c）

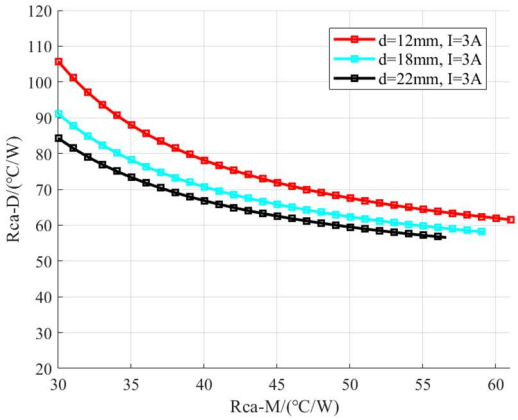


（d）

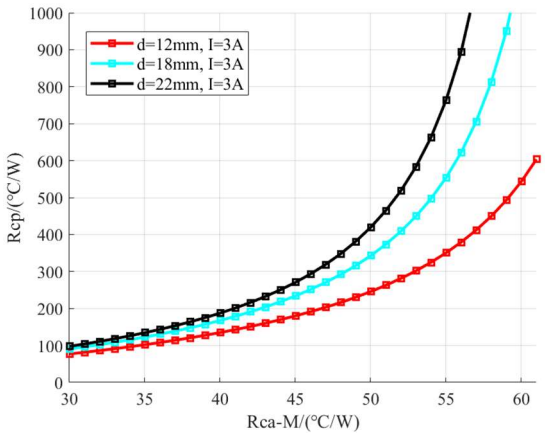
Fig.3.21: Relashipns with different device spacing at I = 2 A.



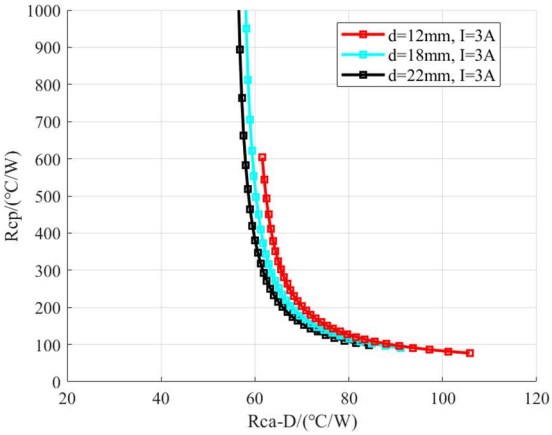
（a）



（b）



（c）



（d）

Fig. 3.22: Relashipns with different device spacing at I = 3 A.

When the devices work under the same current at a fixed value of T_c, the relationships between thermal resistances in the measurement spacing shown in Figs. 3.20-3.22 and Table 3.8 are:

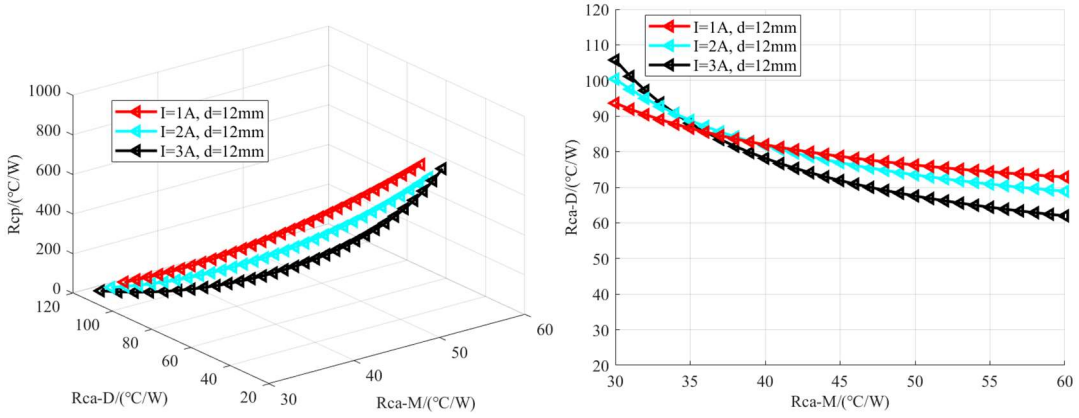
(I) the change of the curve reduces when the spacing between two devices is closer, which reflects a greater coupling effect.

(II) For a given current and $R_{ca\text{-}D}$ value, R_{cp} reduces (larger coupling effect) and $R_{ca\text{-}M}$ increases when the spacing between devices is shorter while the same $R_{ca\text{-}M}$ corresponds to bigger R_{cp} (smaller coupling effect), and vice versa.

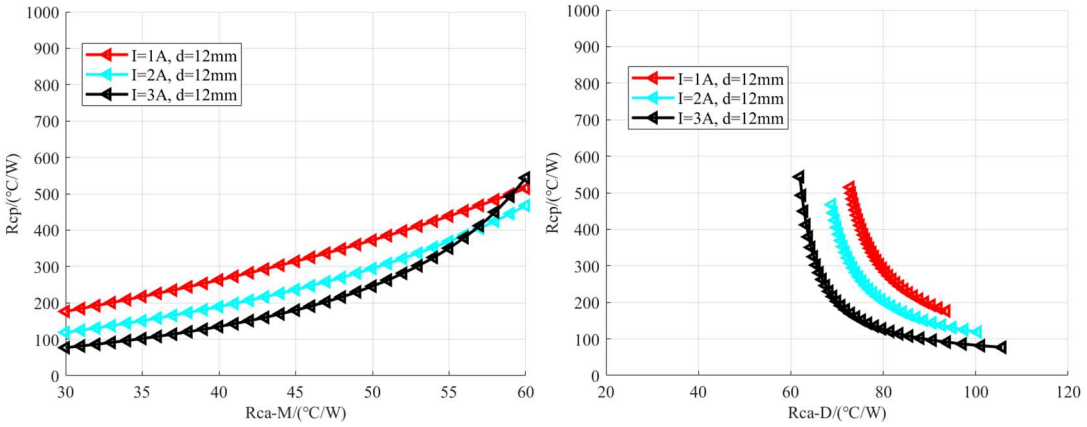
(III) For a given current and $R_{ca\text{-}M}$ value, R_{cp} reduces (larger coupling effect) and $R_{ca\text{-}D}$ increases when the spacing is shorter while the same $R_{ca\text{-}D}$ corresponds to smaller R_{cp} (larger coupling effect), and vice versa.

3.5.3 The Relationships with Different Operating Currents

Similarly, in order to analyze the thermal coupling effect between devices under different operating currents more clearly, the relationships of variable thermal resistances can be obtained according to Fig. 3.19, as shown in Figs. 3.23-3.25, in which Figs. 3.23-3.25 (a) are the three-dimensional views, Figs. 3.23-3.25 (b), (c) and (d) are the projection views.

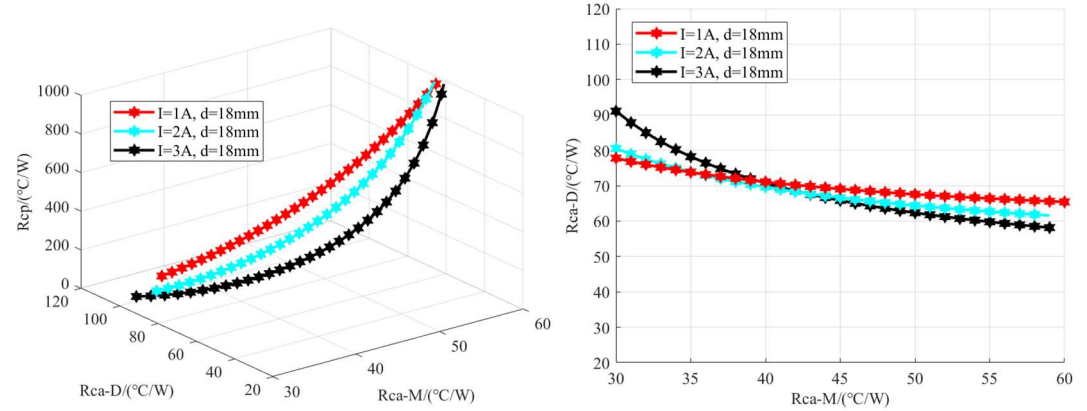


（a） （b）

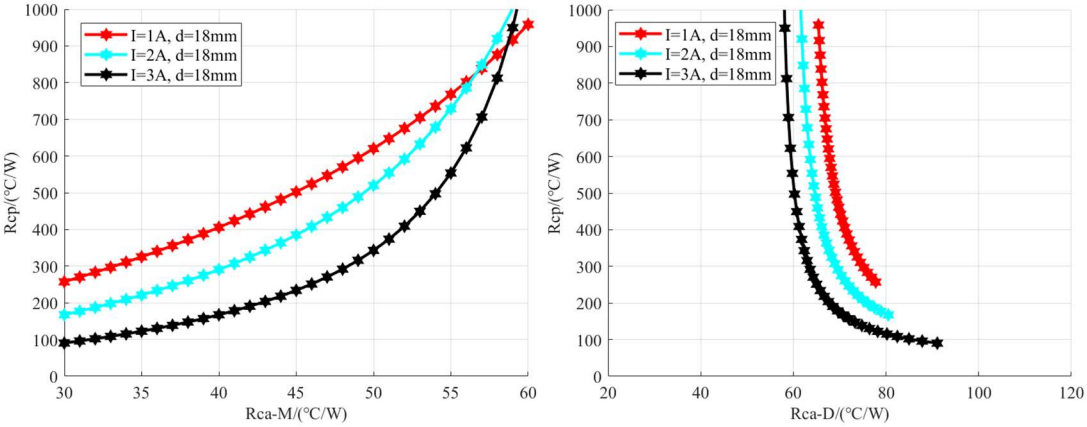


（c） （d）

Fig. 3.23: Relationships with different operating current at d = 12 mm.



（a） （b）



（c） （d）

Fig. 3.24: Relationships with different operating current at d = 18 mm.

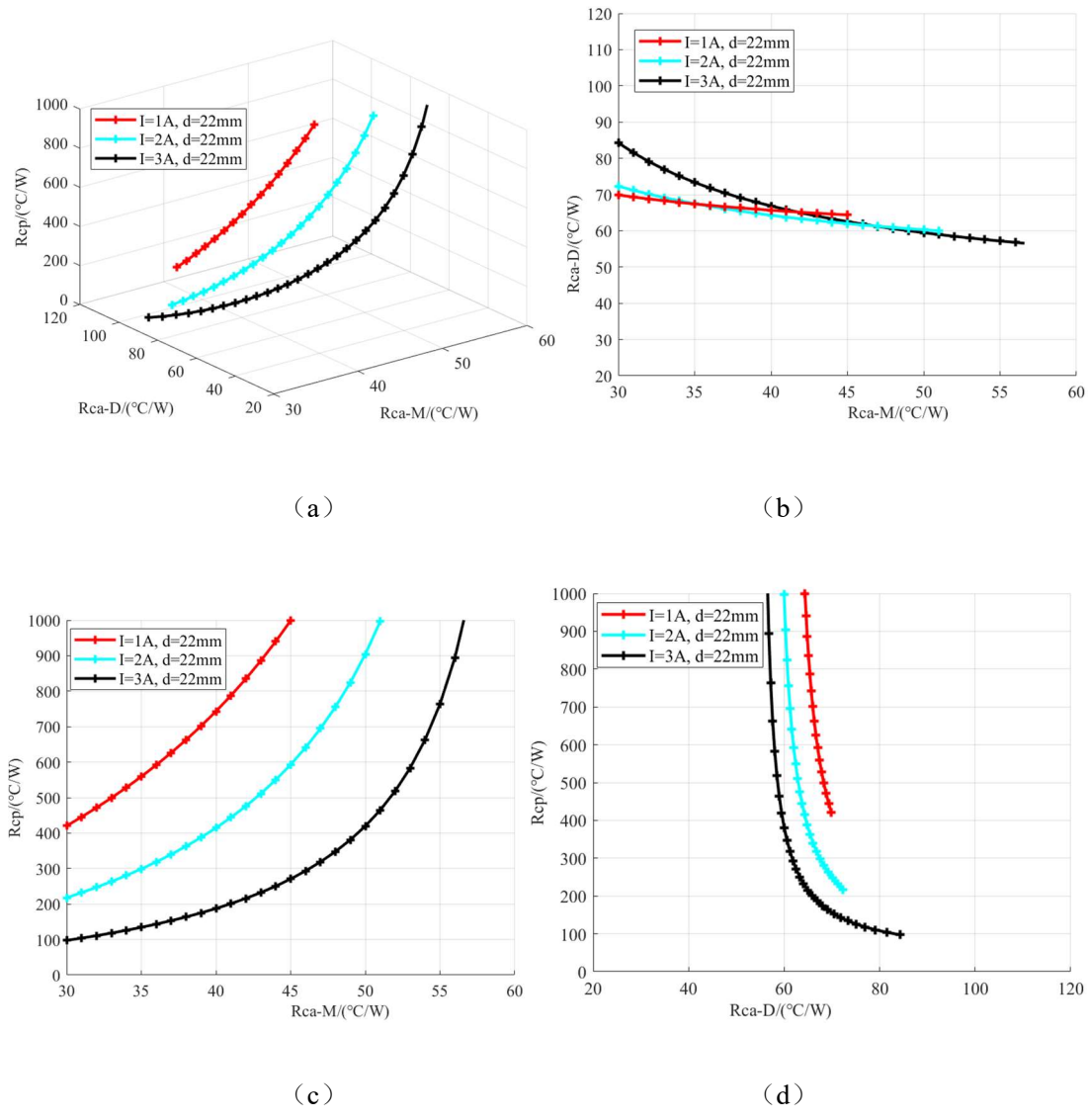


Fig. 3.25: Relationships with different operating current at d = 22 mm.

Figs. 3.23-3.25 and Table 3.8 illustrate the relationships between thermal resistances with different operating current conditions at a fixed T_c.

(I) The values of R_{cp} decrease while the operating currents increase. This indicates the thermal coupling effect can be induced by larger current passing through MOSFET and the diode.

(II) For a given spacing and $R_{ca\text{-}D}$ value, the values of R_{cp} increase (smaller thermal effect) and $R_{ca\text{-}M}$ increase when the operating currents become smaller; and vice versa.

(III) For a given spacing and $R_{ca\text{-}M}$ value, the values of R_{cp} increases (smaller thermal effect) and $R_{ca\text{-}D}$ increase when the operating currents become smaller; and vice versa.

3.5.4 The Steady-state T_c Calculation

The polynomial curve fitting of T_c for MOSFET and the diode based on various component spacing from (12 mm to 22 mm) is experimentally investigated and can be derived as

$$\begin{cases} T_{ca\text{-}M} = a_M \cdot d^2 + b_M \cdot d + c_M \\ T_{ca\text{-}D} = a_D \cdot d^2 + b_D \cdot d + c_D \end{cases} \quad (3.16)$$

where a_M, a_D, b_M, b_D, c_M, c_D are the fitting coefficients of the case temperature of the power devices, and d is the device spacing.

when I = 1 A, 2 A, 3 A, the parameters are

$$\begin{cases} a_M = -0.004 \\ b_M = -0.105 \\ c_M = 30.060 \\ a_D = 0.016 \\ b_D = -0.760 \\ c_D = 59.690 \end{cases}; \quad \begin{cases} a_M = 0.01 \\ b_M = -0.85 \\ c_M = 48.49 \\ a_D = 0.02 \\ b_D = -1.10 \\ c_D = 95.53 \end{cases}; \quad \begin{cases} a_M = 0.014 \\ b_M = -0.92 \\ c_M = 67.31 \\ a_D = -0.004 \\ b_D = -0.40 \\ c_D = 116.70 \end{cases} \quad (3.17)$$

Based on (3.16) and (3.17), the values of T_c at other spacings which are larger than 12 mm (d > 12 mm) can be obtained by calculation.

3.6 Experimental Verification

3.6.1 The Steady-state T_c Calculation

To validate the proposed TCRN model and the relationships between thermal resistances, the values of T_c: 1) from calculation in (3.16) and (3.17); 2) from more measurements at new spacing (e.g. d = 15 mm), have been given considering different operating currents. The comparisons of T_c between calculation results and the experimental data are shown in Tables 3.9 and 3.10. The error of the steady-state case temperature for MOSFET is less than 1%,

and the maximum error is 0.99%; the error of the steady-state case temperature for diode is controlled at about 1%, and the maximum error is 1.33%.

Table 3.9: Comparisons of Modeling and Experimental Data for MOSFET.

Current/A	T_{ca_M}/℃ (Calculation)	T_{ca_M}/℃ (Experimental Data)	Error
1	27.59	27.32	0.99%
2	37.99	37.66	0.88%
3	56.66	56.85	0.33%

Table 3.10: Comparisons of Modeling and Experimental Data for diode

Current /A	T_{ca_D}/℃ (Calculation)	T_{ca_D}/℃ (Experimental Data)	Error
1	51.89	51.21	1.33%
2	83.08	82.82	0.31%
3	109.80	110.08	0.25%

3.6.2 TCRN Model and Relationships Verification

By putting the calculation results and measurement data into (3.11) - (3.14), the relationships between R_{cp} and R_{ca} and the comparisons between calculation and experimental data are given in Fig.3.26. The working currents are 1 A, 2 A and 3 A and this is obtained for

the other spacing (d = 15 mm) as follows:

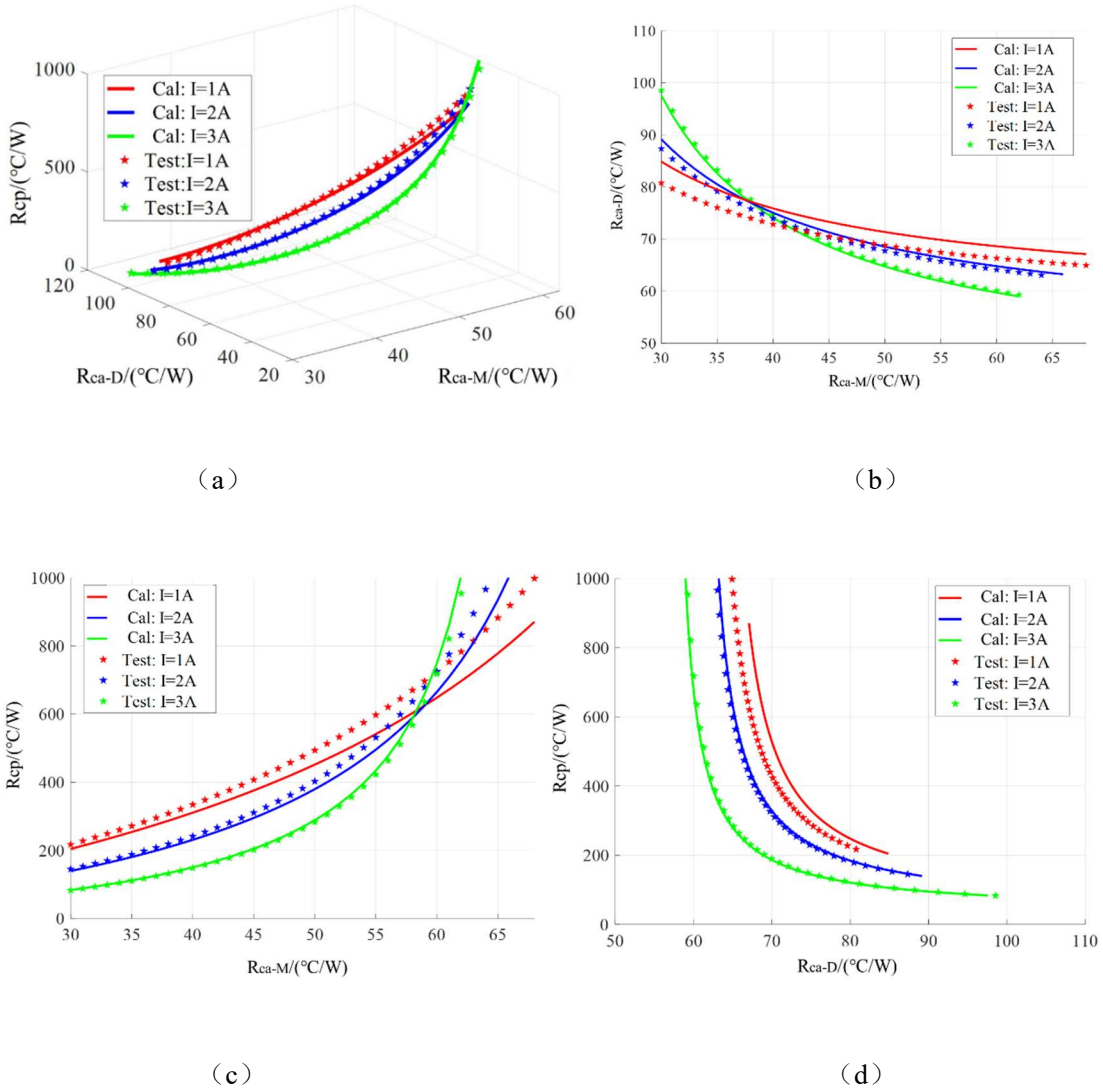


Fig. 3.26: Comparisons of calculation (solid lines) and experimental data (five-star lines). (a) is 3D view. (b), (c) and (d) are the projection views.

(I) The calculated and measured T_c data prove that it has the same relationships between the thermal resistances at the other spacing in the operating currents, as shown in Section 3.5.

(II) The errors between the calculation results and experimental data are calculated under the current of 3 A in Table 3.11. The results show that the error between the calculated

and the experimental value is less than 1%. For the thermal coupling resistance between adjacent devices, the minimum error is 1.15%, and the maximum error is less than 5%. The comparisons show good agreements between them.

(III) One of the reasons for this error is that the electro-thermal coupling effect between the loss and case temperature is not considered in the model establishment.

Table 3.11: Errors Between Calculation and Experimental Data.

$R_{ca\text{-}M}$ [°C/W]	$R_{ca\text{-}D}$[°C/W] (Calcula -tion)	$R_{ca\text{-}D}$[°C/W] (Experimental Data)	Error	R_{cp} [°C/W] (Calcula -tion)	R_{cp} [°C/W] (Experimental Data)	Errors
40	74.1	74.6	0.67 %	150.1	148.4	1.15%
50	64.7	65.1	0.61 %	288.5	283.1	1.91%
60	59.7	60.0	0.50 %	748.5	717.7	4.29%

3.7 Conclusions

In compact power converters, thermal coupling will be formed between surrounding devices with multiple thermaling components under different working conditions. Considering this, this paper focuses on modeling and analysis of thermal resistances of the power semiconductor devices. Based on the modeling and measurement results, a TCRN model has been established. Moreover, the relationships between individual R_{ca} and their R_{cp} to the adjacent device have been obtained for different spacing and load currents during the design phase consideration. New T_c data from the calculation and measurement which

employs different spacing verifies the proposed thermal model and the relationships. The smallest and worst errors between the calculation and testing were less than 1% and 5% respectively at the current of 3 A, which shows the efficacy of the proposed model and its relationships. Better understanding of the environmental dependent resistances will help in terms of the selection and size of appropriate thermal cooling schemes based on the proposed TCRN model and the relationships. Furthermore, this understanding will assist in terms of establishing proper spacing between power devices. The result will be the optimization of PCB circuits and the design of better power converters with high-power density.

Based on the above the purposes of the chapter are: 1) to give a good thermal model which enhances the current thermal models for the power devices; 2) to obtain the relationships between thermal resistances when fixing the case temperature.These outcomes can serve to enhance power converter optimization.

Chapter 4 Research on Convection Thermal Coupling Between Power Devices

Based on the analysis of the conduction thermal coupling effect in Section 1.1 and Chapter 3, it can be seen that when multiple power modules share a heatsink or multiple devices are connected by copper wires through a PCB, the coupling effect will be formed between the modules/devices. In the application of medium and low voltage power converters, the main power devices are MOSFET and diode. After the thermal of the devices transferred to the air through convection, the thermal will be coupled with each other in the surrounding air.

This kind of thermal coupling effects will also have a certain impact on the junction/ case temperature of the devices, which will affect the junction temperature prediction and the reliability of the devices and systems [96]. Therefore, it is of great significance to establish an analysis model of the convection thermal coupling effect between adjacent power devices.

The thermal is mainly transferred in three ways: thermal conduction, thermal convection, and thermal radiation [22]. In the thermal analysis of power devices studied in this chapter, the effect of thermal radiation is relatively small, so it will not be discussed [23]. Based on the analysis in Chapter 3, many thermal models do not consider the convection thermal coupling, and the datasheet does not have the standard for calculating the convection coupling resistances. In this part, convection thermal coupling is discussed.

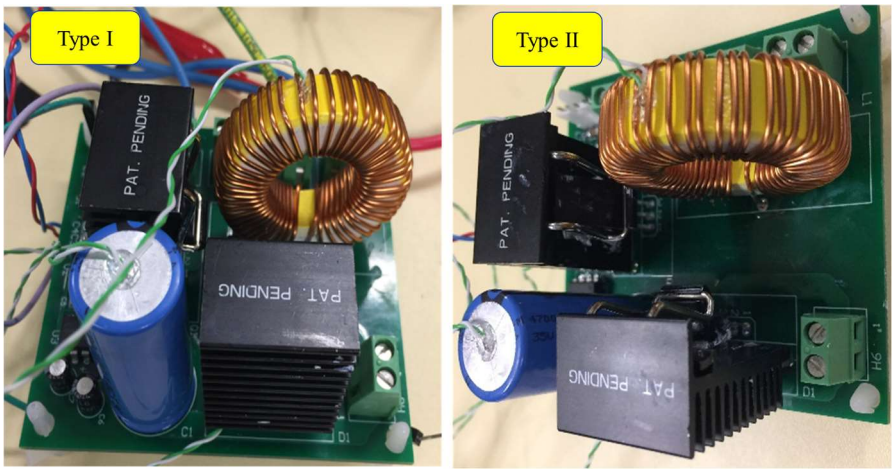
4.1 Thermal Convection Testing Analysis of Power Devices

4.1.1 Thermal Convection Testing of Devices

In order to explore the influence of thermal convection on the devices in the power converter system, a convection thermal analysis testing platform for the testing device is established. The main circuit of the platform is to connect a single semiconductor device

(MOSFET or diode) into the circuit and analyze the change of the case temperature by changing the device spacing. The testing devices include MOSFET, diode, capacitor, inductor and other devices. The devices are not connected with each other, so the devices will not be affected by thermal conduction, and the location of the device and the distance/spacing between the devices will affect the convection thermal dissipation, that is, the thermal convection will have a certain impact on the T_j of the devices.

The type of MOSFET, diode, capacitor, inductor and other devices used in the power converter system tested in this section are identical with those used in Section 3.2. The main difference between the two testing platforms is that the former (the power testing devices) separately energizes the two semiconductor devices, MOSFET and diode. The on-state losses of the devices are changed by changing the working current and then the case temperature of the device will be changed, at the same time, the other devices are in the open circuit state. That is: 1) power on MOSFET, when the testing device is working MOSFET is on-state and other devices are in the open-circuit; 2) power on the diode, when the test device is working the diode is on-state and other devices are in the open-circuit.



（a） （b）

Fig. 4.1: Convection thermal analysis testing devices: (a) Type I, the small device spacing; (b) Type II, the large device spacing.

For better analysis the convection thermal coupling, in the testing all the devices are not connected as a power converter in the circuit. As shown in Fig. 4.1, two key devices

(MOSFET and diode) with different device spacing are tested in the convection thermal analysis platform:

1) a PCB with small spacing (marked as Type I) between MOSFETs, diodes, capacitors, inductors, and other devices, so the convection thermal dissipation of devices will be limited and the couping impact is relatively big.

2) a PCB with large spacing (marked as type II) between MOSFETs, diodes and other devices. The testing devices have good convectiong thermal dissipation space, so the couping impact is relatively small.

The testing platform of the semiconductor devices is shown in Fig. 4.2. The load current used in the testing is 3 A and 6.5 A respectively, the type of MOSFET used in the testing is IRF540NPBF, the type of diode is MBR2010CT, and the packaging type of the two devices are TO-220. In the convection thermal analysis testing, the working condition/working current of the device is changed, and the T_c of MOSFET and diode collected by Type I and Type II under different working current is compared, which is used to analyze the influencing factors of thermal convection and the effect of thermal convection on the device temperature.

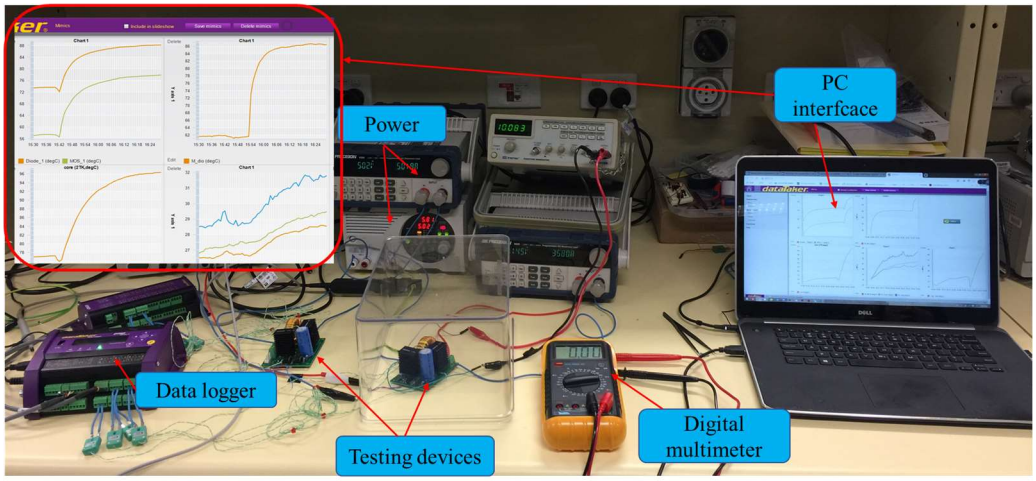
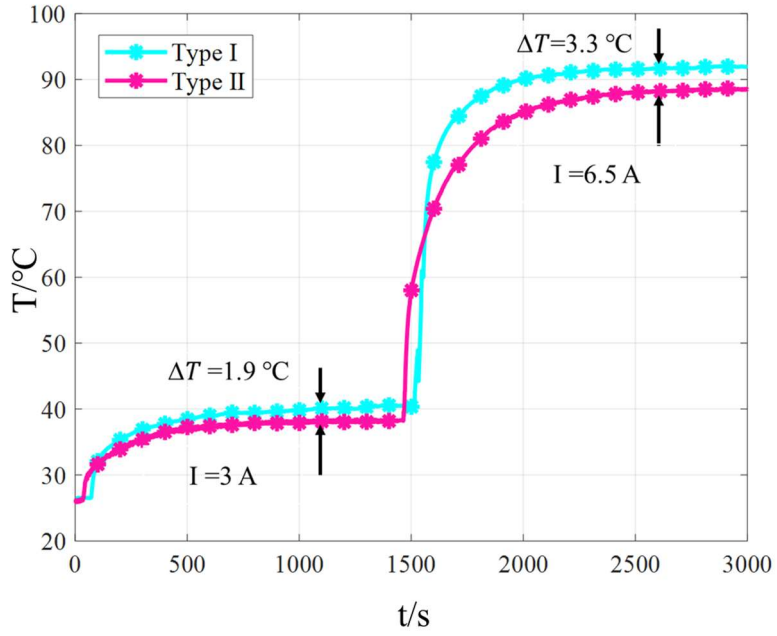


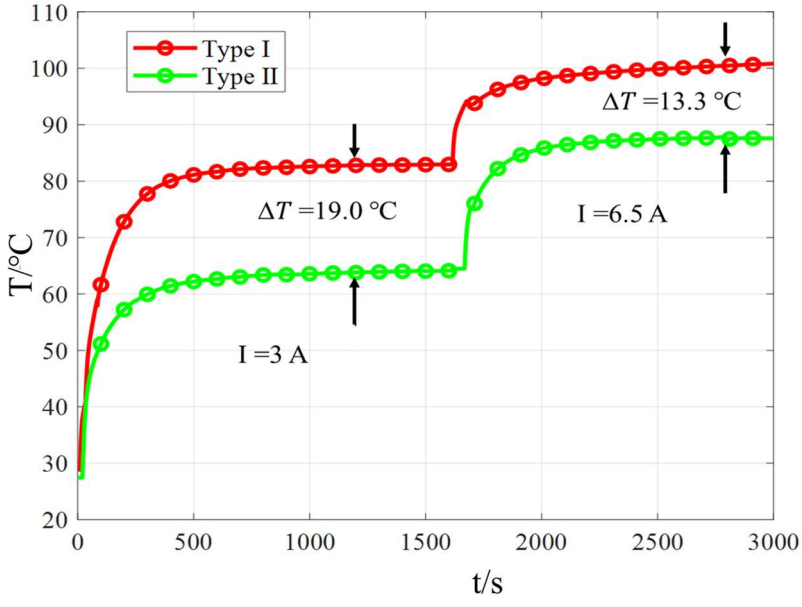
Fig. 4.2: Convection thermal analysis testing platform of semiconductor devices.

In this testing platform, the T_c of the device under different working conditions are collected by the data logger, and the testing results of MOSFET and diode under two different spacing types are compared as shown in Fig. 4.3, where Fig. 4.3 (a) shows the comparison of T_c for MOSFET and the temperature difference under different working currents; Fig. 4.3

(b) shows the comparison of T_c for diode and the temperature difference under different working currents. For MOSFET and diode, the T_c is higher when it is tested under type I (the small sapcing) than that of the T_c tested under type II (the large sapcing). In addition, for MOSFET, the T_c difference under the two types of spacing is 1.9 ℃ and 3.3 ℃ under the working current of 3 A and 6.5 A, respectively; for diode, the T_c difference is as high as 19.0 ℃ at 3 A and 13.3 ℃ at 6.5 A.



(a)



(b)

Fig. 4.3: T_c of the semiconductor devices and temperature difference under different working currents. (a) T_c of MOSFET: type I in blue, type II in pink; (b) T_c of diode: type I in red, type II in green.

The main reason for this phenomenon is that the distance between devices is different, and the convection cooling environment changes, which has an impact on the T_c of the devices. Based on the above analysis, the convection cooling is affected by the power loss /working current, device spacing, and the surrounding cooling environment.

4.1.2 Analysis of the Convection Thermal Coupling

The convection coupling effect is not easily calculated under different working conditions because of the environmental dependency. In this section, the thermal coupling platform is established to analyze the mutual coupling which includes the conduction and convection thermal coupling.

According to the analysis of the thermal convection testing results of the devices in Section 4.1, the convection thermal dissipation is affected by many factors. In the power converter system, when multiple devices conduct thermal dissipation in the form of thermal convection (natural convection), they will be coupled with each other in the process of thermal dissipation, forming convection thermal coupling.

In addition, MOSFET and diode are the two core devices in the power converter system and are the main thermaling devices. Many scientific research institutions and colleges spend a lot of time and energy on the temperature calculation and reliability research of power devices, whose performance directly affects the reliability of the whole system. In order not to be interfered with by adjacent devices (inductance, capacitance, etc.), this section establishes an independent test circuit to carry out a single test and thermal coupling test analysis on MOSFET and diode. The semiconductor devices used in the testing platform are the same as those used in Section 4.1, that is, the MOSFET is IRF540NPBF, the diode is MBR2010CT, and the package is TO-220.

4.1.3 The Experimental Platform for MOSFET and Diode

The thermal coupling platform is illustrated in Fig.4.4. This experimental platform includes: one 30 V DC power supply for the MOSFET gate driving, a controlled DC current supply for the testing circuit (5 A), two power components (MOSFET: IRF540NPBF, Infineon, Munich, Bavaria, Germany, and diode: MBR20100CT, ON Semiconductor, Phoenix, Arizona, USA) packaged with TO-220, a digital multimeter which is used for observing the voltage-drop of the diode, a current sensor which is used to measure the current levels, a data Taker Data Logger (DT80 with eight bi-directional channels, Thermo Fisher Scientific, Waltham, MA, USA) which is employed for collecting the measurement data, K-type thermocouples attached to the case of the devices for T_c testing [97, 98], and real-time data monitoring by a computer and a FR4 PCB board.

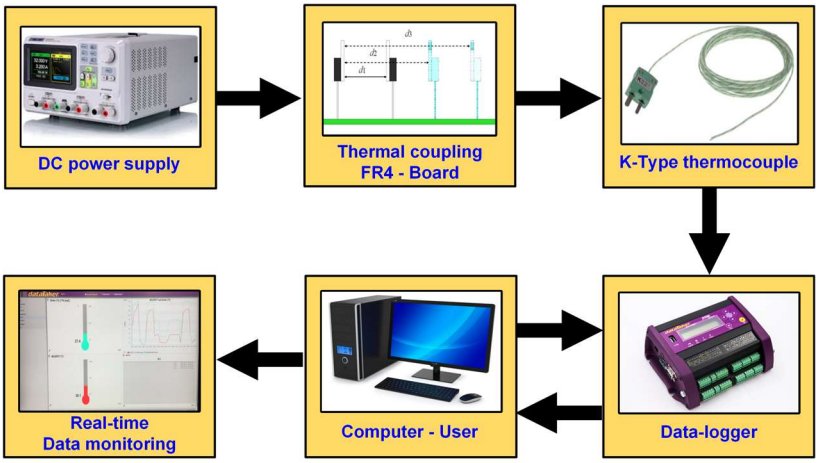


Fig. 4.4: Thermal coupling testing platform.

In power converter applications when the MOSFET and the diode are working, power losses (the conduction loss and switching loss, etc.) will be generated and all the power losses will become factors of component thermaling. Therefore, a given power loss [76] or controlled currents [78] can thermal up the devices. In this study, as shown in Fig.4.5, we focus on the on-state mode.

The two power devices (MOSFET： IRF540NPBF, diode： MBR20100CT) are measured in the thermal coupling experimental platform with the distances of 12 mm, 18 mm, and 22 mm and under three different working currents, respectively. In one minute, 30 T_c values (a maximum of 600 data can be collected) for the MOSFET and the diode are collected

by a Data-Taker and for every testing current it takes 20 min at the separation distances. When the devices are powered on, T_c increases at a fast rate and then reaches its steady state. Since the diode has a higher power loss than the MOSFET, it has a faster rate of increase and a higher steady temperature. When the devices are powered off, T_c decreases at a considerable rate and then reaches T_a and the diode also decreases at a faster rate than the MOSFET. All measured T_c data in steady state, $T_{c\text{-}M}$ for the MOSFET and $T_{c\text{-}D}$ for the diode, are shown in Fig.4.6 and Table 4.1.

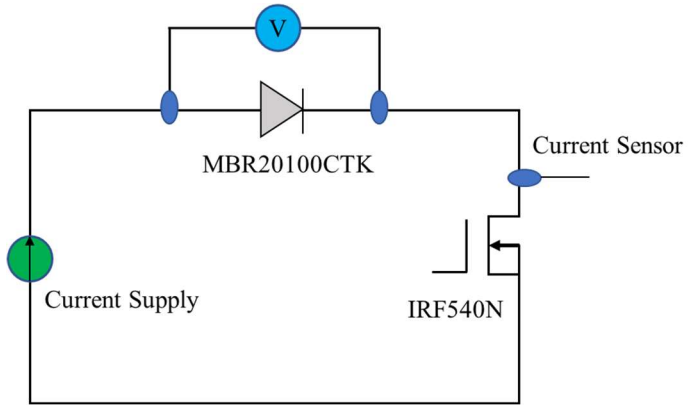


Fig. 4.5: The testing circuit.

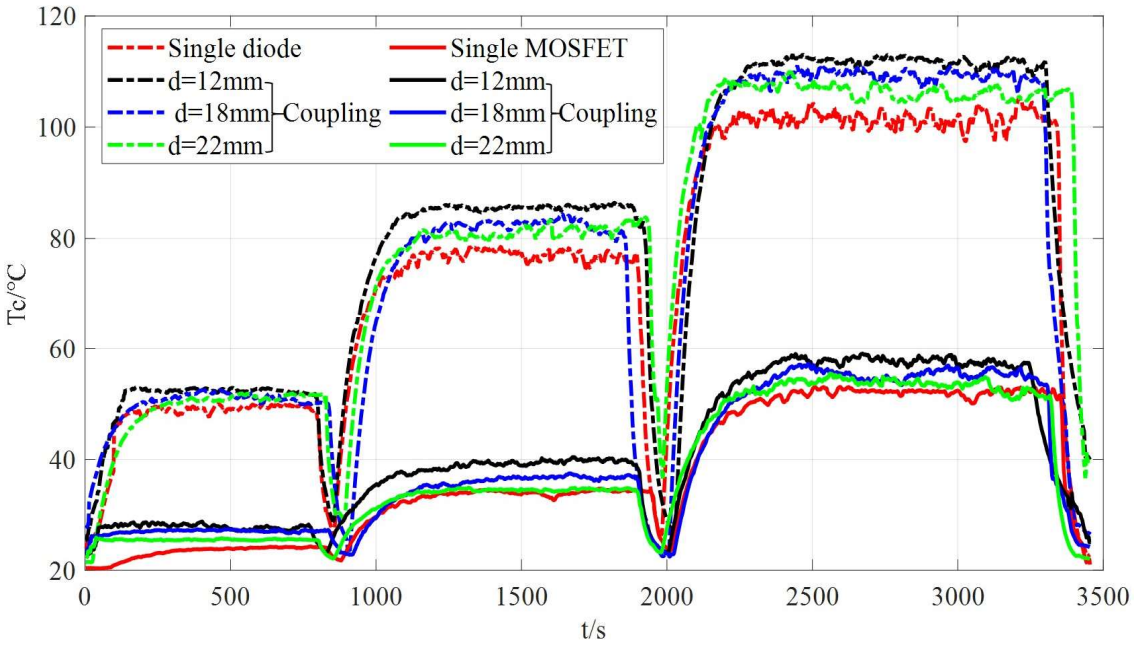


Fig. 4.6: T_c for power devices.

Table 4.1: Steady-state T_c under different working conditions.

d [mm]	I [A]	$T_{c\text{-}M}$ [°C]	$T_{c\text{-}D}$ [°C]
12	1	28.22	52.94
	2	39.72	84.91
	3	58.27	111.45
18	1	26.87	51.85
	2	36.39	82.57
	3	55.21	108.42
22	1	25.81	50.89
	2	34.56	81.45
	3	53.71	106.95

4.2 Multi-Variable Thermal Resistances Network Modeling

4.2.1 Thermal Resistances Network

For thermal analysis of these power components, which are realized in the experimental results, it should be noted that the values of T_j, T_c, and all the thermal resistances are variable when the separation distances and the working currents change. Then a multi-variable thermal resistances model is established considering the self-resistances [91] and coupling resistances between the power components. Based on the analysis of the traditional thermal models in the literature section, the models always ignore the mutual thermal effects or only focus on the R_{cdcp}. In this paper, the R_{cvcp} has been added into the multi-variable thermal network and in this new network the variable thermal resistances are as follows: (1) the self-resistances: junction-to-case resistance (R_{jc}); case-to-ambient resistance (R_{ca}); and (2) the thermal coupling resistances (R_{cp}), R_{cdcp}, which is given through the device pins connected via copper traces; and R_{cvcp}, which is given through the air between the two power components. The power losses for the MOSFET and the diode (P_M and P_D) are the thermal

sources in the network. The packages for the devices are supposed to be insulated and all the thermal is released from case and fins and the air domain is considered as an incompressible fluid [77, 90, 99]. During the process of thermal distribution, mutual thermal coupling will affect the T_j and T_c for the power devices. The thermal analysis model can be given as shown in Fig. 4.7.

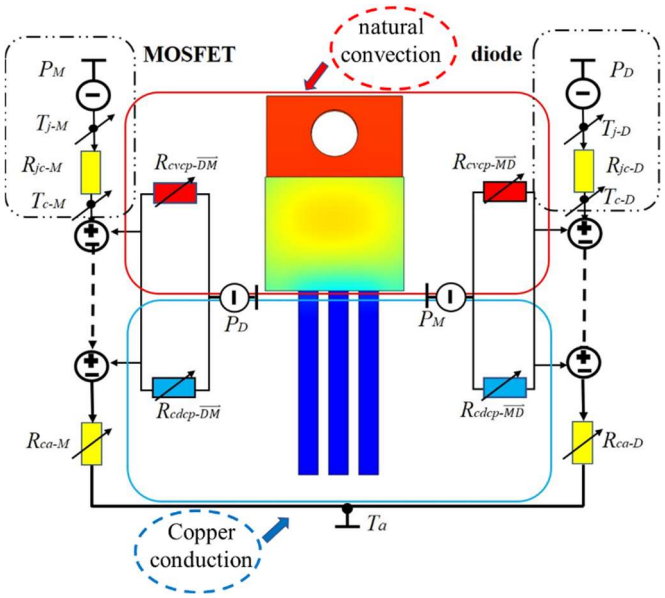


Fig.4.7. Multi-variable thermal resistances model of the power devices.

4.2.2 Self-Resistances Calculation

R_{jc} is in the process of thermal conduction which can be obtained from the datasheet. The method to calculate R_{ca} in the steady state is given as:

$$R_{ca} = \frac{T_c - T_a}{P} \tag{4.1}$$

Therefore, R_{ca} for the MOSFET and the diode can be obtained by:

$$\begin{cases} R_{ca\text{-}M} = \dfrac{T_{c\text{-}M} - T_a}{P_M} \\ R_{ca\text{-}D} = \dfrac{T_{c\text{-}D} - T_a}{P_D} \end{cases} \tag{4.2}$$

Putting the experimental data into (4.2), the values of $R_{ca\text{-}M}$ and $R_{ca\text{-}D}$ in different working conditions can be calculated, as shown in Table 4.2.

Table 4.2. The values of $R_{ca\text{-}M}$ and $R_{ca\text{-}D}$.

d [mm]	I [A]	$R_{ca\text{-}M}$ [°C/W]	$R_{ca\text{-}D}$ [°C/W]
12	1	69.32	60.39
	2	62.73	58.89
	3	61.76	54.35
18	1	69.32	60.39
	2	62.73	58.89
	3	61.76	54.35
22	1	69.32	60.39
	2	62.73	58.89
	3	61.76	54.35

4.2.3 Thermal Coupling Resistances Calculation

R_{cdcp} can be calculated based on the method in Section 3.4.1 [18]. According to the proposed thermal coupling resistances network, R_{cp} is the result of R_{cdcp} and R_{cvcp} in parallel and can be given as

$$\begin{cases} R_{cp\text{-}\overrightarrow{MD}} = \dfrac{1}{\dfrac{1}{R_{cdcp\text{-}\overrightarrow{MD}}} + \dfrac{1}{R_{cvcp\text{-}\overrightarrow{MD}}}} \\ R_{cp\text{-}\overrightarrow{DM}} = \dfrac{1}{\dfrac{1}{R_{cdcp\text{-}\overrightarrow{DM}}} + \dfrac{1}{R_{cvcp\text{-}\overrightarrow{DM}}}} \end{cases} \tag{4.3}$$

where $R_{cp\text{-}\overrightarrow{MD}}$ is the thermal coupling resistance of MOSFET to the diode and $R_{cp\text{-}\overrightarrow{DM}}$ is the coupling resistance of the diode to the MOSFET.

Based on , R_{cp} in the steady state can be calculated by:

$$\begin{cases} R_{cp\text{-}\overrightarrow{MD}} = \dfrac{|T_{c\text{-}M} - T_{c\text{-}D}|}{P_M} \\ R_{cp\text{-}\overrightarrow{DM}} = \dfrac{|T_{c\text{-}D} - T_{c\text{-}M}|}{P_D} \end{cases} \tag{4.4}$$

Bring all the measured T_c data from Table 4.1 into (4.4), the values of $R_{cp\text{-}\overrightarrow{MD}}$ and $R_{cp\text{-}\overrightarrow{DM}}$ at different separation distances and different currents can be calculated and given in Table 4.3.

Table 4.3. The values of $R_{cp\text{-}\overrightarrow{MD}}$ and $R_{cp\text{-}\overrightarrow{DM}}$.

d [mm]	I [A]	$R_{cp\text{-}\overrightarrow{DM}}$ [°C/W]	$R_{cp\text{-}\overrightarrow{MD}}$ [°C/W]
12	1	53.39	561.82
	2	45.19	241.66
	3	33.66	107.43
18	1	53.95	567.73
	2	46.18	246.95
	3	33.68	107.50
22	1	54.17	570.00
	2	46.89	250.75
	3	33.25	107.56

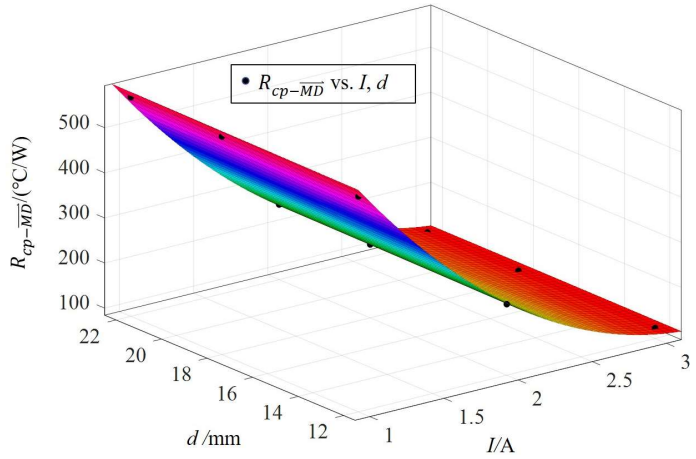
4.2.4 Relationships between R_{cp} and the impact factors

Table 4.3 shows that the separation distances between power components and working currents are the two key impact factors for thermal coupling resistances $R_{cp\text{-}\overrightarrow{MD}}$ and $R_{cp\text{-}\overrightarrow{DM}}$. The relationships between them can be described as (4.5) and Fig.4.8 gives the relationships based on data curve fitting.

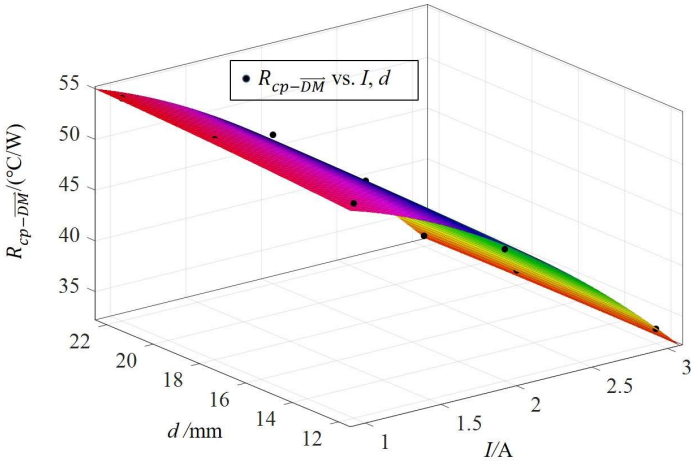
$$\begin{cases} R_{cp\text{-}\overrightarrow{MD}} = f(d, I) \\ R_{cp\text{-}\overrightarrow{DM}} = g(d, I) \end{cases} \tag{4.5}$$

The relationships between thermal coupling resistances and their impact factors, *d* and *I*, are detailed in Table 4.4 and summarized as follows.

$$\begin{cases} R_{cp\text{-}\overrightarrow{MD}} = f(d, I) \\ R_{cp\text{-}\overrightarrow{DM}} = g(d, I) \end{cases} \tag{4.6}$$



（a）



（b）

Fig.4.8: The relationships between thermal resistances and their impact factors.

(a) $R_{cp\text{-}\overrightarrow{MD}}$; (b) $R_{cp\text{-}\overrightarrow{DM}}$.

(1) The values of $R_{cp\text{-}\overrightarrow{MD}}$ and $R_{cp\text{-}\overrightarrow{DM}}$ increase when the distance between power components increases, which means the coupling effect decreases when the separation distances increase, and vice versa.

(2) The values of $R_{cp\text{-}\overrightarrow{MD}}$ and $R_{cp\text{-}\overrightarrow{DM}}$ decrease when the working currents increase, which means the coupling effect increases when the currents increase, and vice versa.

(3) $R_{cp\text{-}\overrightarrow{MD}}$ and $R_{cp\text{-}\overrightarrow{DM}}$ have decreasing trends when the currents increase and the distances decrease, which means the coupling effect increases when the devices are brought closer with higher current magnitude, and vice versa.

Table 4.4: The variations of thermal coupling resistances.

d	I	$R_{cp\text{-}\overrightarrow{MD}}$	$R_{cp\text{-}\overrightarrow{DM}}$	Thermal coupling effect
↑	-	↑	↑	↓
↓	-	↓	↓	↑
-	↑	↓	↓	↑
-	↓	↑	↑	↓
↓	↑	↓	↓	↑
↑	↓	↑	↑	↓

4.2.5 R_{cp} Calculation

Based on Fig.4.8, the formula for calculating R_{cp} considering different distances and currents can be given in (4.7) and the R_{cp} in other separation distances (12 mm ≤ d ≤ 22 mm) or working currents (1 A ≤ I ≤ 3 A) can be estimated by this method:

$$\begin{cases} R_{cp\text{-}\overrightarrow{MD}} = \mathrm{A_{\text{-}M}} + \mathrm{B_{\text{-}M}}I + \mathrm{C_{\text{-}M}}d + \mathrm{E_{\text{-}M}}I^2 + \mathrm{F_{\text{-}M}}Id + \mathrm{G_{\text{-}M}}d^2 \\ R_{cp\text{-}\overrightarrow{DM}} = \mathrm{A_{\text{-}D}} + \mathrm{B_{\text{-}D}}I + \mathrm{C_{\text{-}D}}d + \mathrm{E_{\text{-}D}}I^2 + \mathrm{F_{\text{-}D}}Id + \mathrm{G_{\text{-}D}}d^2 \end{cases} \quad (4.7)$$

where

$$\begin{cases} A_{-M} = 1040 \\ B_{-M} = -584.6 \\ C_{-M} = 1.79 \\ E_{-M} = 90.55 \\ F_{-M} = -0.409 \\ G_{-M} = -0.012 \end{cases} ; \begin{cases} A_{-D} = 52.32 \\ B_{-D} = 0.47 \\ C_{-D} = 0.34 \\ E_{-D} = -2.40 \\ F_{-D} = -0.058 \\ G_{-D} = -0.005 \end{cases} \quad (4.8)$$

4.3 Verifications

To verify the proposed multi-variable thermal resistances model, the coupling resistances have been calculated by (4.7) and (4.8) and more measurements with d = 15 mm, I = 1 A, 2 A, and 3 A have been taken. The comparisons of calculation and measurements are shown in Table 5 for $R_{cp\text{-}\overrightarrow{MD}}$ and Table 6 for $R_{cp\text{-}\overrightarrow{DM}}$, respectively. The values of $R_{cp\text{-}\overrightarrow{MD}}$ and $R_{cp\text{-}\overrightarrow{DM}}$ have decreasing trends when the working currents increase, and all the errors are less than 4%.

Table 4.5: Errors of the calculation results and the testing for $R_{cp\text{-}\overrightarrow{MD}}$.

I [A]	$T_{c\text{-}M}$ [°C]	$R_{cp\text{-}\overrightarrow{MD}}$ [°C/W] （calculation results）	$R_{cp\text{-}\overrightarrow{MD}}$ [°C/W] （testing）	error [%]
1	27.32	563.97	542.95	3.87
2	37.66	244.88	241.50	1.40
3	56.85	106.90	107.54	0.60

Table 4.6: Errors of the calculation results and the testing for $R_{cp\text{-}\overrightarrow{DM}}$.

I [A]	$T_{c\text{-}D}$ [°C]	$R_{cp\text{-}\overrightarrow{DM}}$ [°C/W] （calculation results）	$R_{cp\text{-}\overrightarrow{DM}}$ [°C/W]（testing）	error [%]
1	51.21	53.50	51.60	3.68
2	82.82	45.90	45.16	1.64

3	110.08	33.50	34.79	3.71

4.4 Conclusions

In this study, comparisons of junction temperatures and the increments in a boost converter system have been given to show the conduction thermal coupling effect under different working conditions. Conduction and convection coupling have been added into the mutual thermal effects and a multi-variable thermal resistances model has been built, which includes the variable thermal resistances, $R_{cp\text{-}\overline{MD}}$ and $R_{cp\text{-}\overline{DM}}$. In addition, the relationships between the thermal coupling resistances and their impact factors (d and I) have been discussed. The calculation and the measurements have been done to verify the concept. The errors between the calculations and measurements are less than 4% for both the MOSFET and the diode, which prove the efficacy of the proposed method. Based on the proposed thermal model, T_j can be estimated. Moreover, heatsinks can be included by adding the thermal resistances of heatsinks to discuss the cooling schemes. Additionally, extension thermal models can be given for the overall converters by adding thermal resistances of other components (e.g., capacitors, inductors) to assist the components layouts and the separation distances between them in order to optimize the power converters.

As the thermal analysis model established in this paper does not consider the electrical thermal coupling of semiconductor devices, the junction temperature obtained has a certain error compared with the actual application of power converter.

Chapter 5 Thermal Analysis and Junction Temperature Calculation under Different Ambient Temperatures Considering Convection Thermal Coupling

The existing thermal analysis models are often based on fixed ambient temperatures such as 25 ℃ [62], However, the ambient temperatures is variable [63, 64]. Different ambient temperatures will have different effects on the convection thermal coupling between power devices, on the other hand, the convection thermal coupling will also change the temperature distribution and junction temperature of devices. When the ambient changes, the traditional thermal analysis models will have big errors to calculate the temperature distribution and junction temperature prediction [59].

Therefore, in different ambient temperatures, the thermal coupling between power devices is not well-analyzed which leads to the junction temperature calculation methods are not accurate and cannot be used as design guidelines [100].

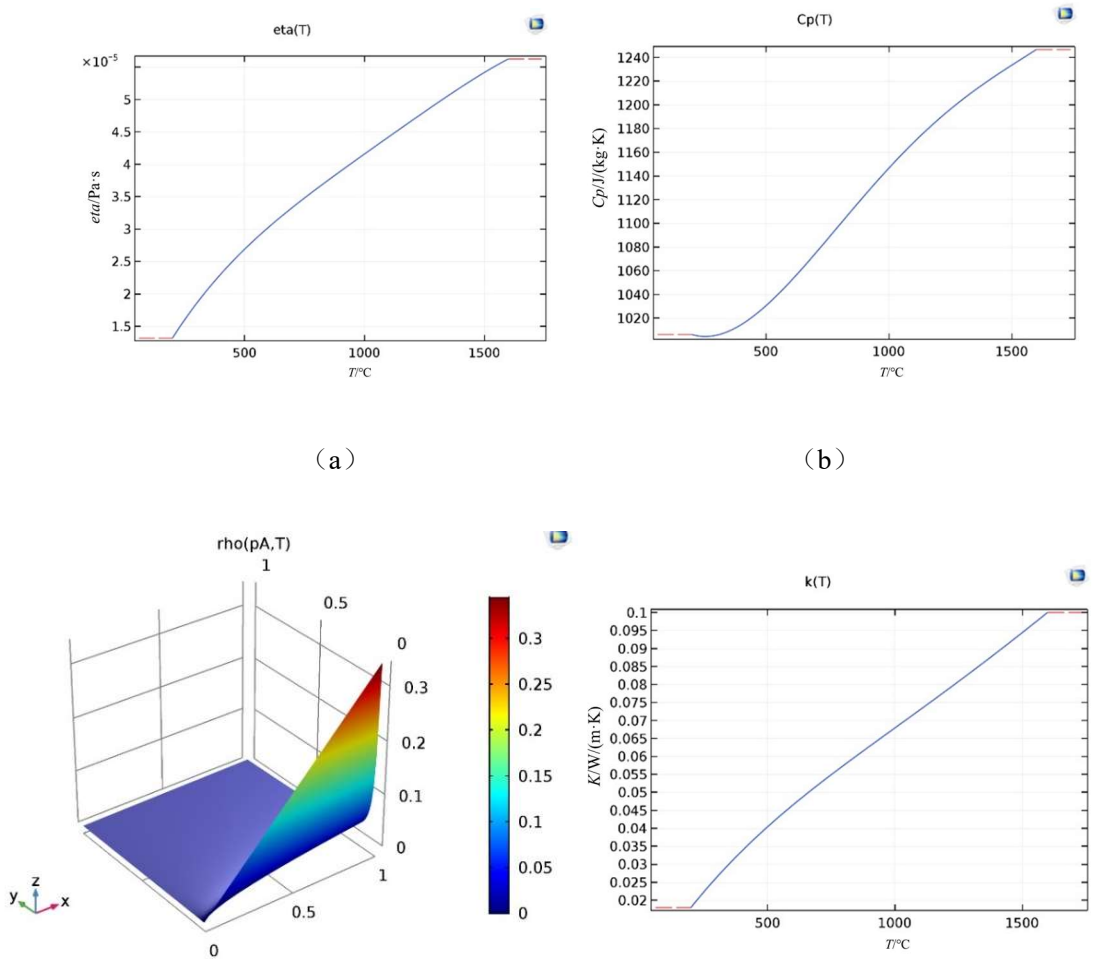
5.1 Ambient Temperatures

5.1.1 Ambient Temperatures Domain

In addition to the power losses factor, the junction temperature of power devices is also affected by environmental factors. The parameters of the outside surrounding ambient domain of power devices, such as the kinetic viscosity, constant pressure thermal capacity, density, thermal conductivity, etc., are all functions of ambient temperatures and will be changed with the change of temperature [28, 101] and the parameters are shown in Table 5.1 and Fig. 5.1.

Table 5.1: Ambient domain parameters.

Name	Symbol	Unit
kinetic viscosity	eta (T)	Pa·s
constant pressure thermal capacity	Cp (T)	J/(kg·K)
density	ρ (pA,T)	kg/m³
thermal conductivity	k (T)	W/(m·K)



（a） （b）

（c） （d）

Fig. 5.1. Ambient domain parameters. (a) kinetic viscosity; (b) constant pressure thermal capacity; (c) density; (d) thermal conductivity.

5.1.2 Analysis and Selection of the Ambient Temperatures

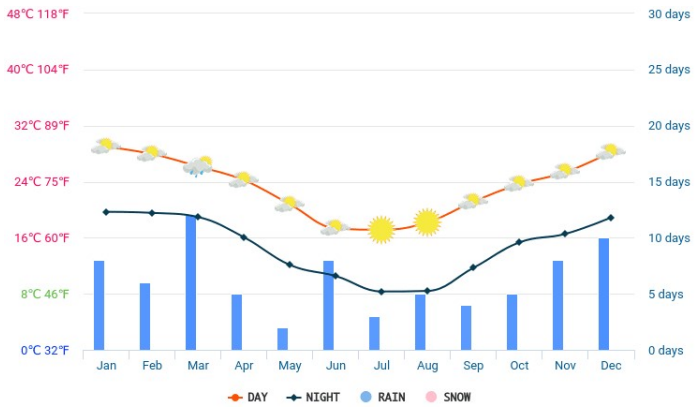


Fig. 5.2: The average temperature change of Sydney in one year.

Fig. 5.2 shows the average temperature change of Sydney in one year. In this year, the temperatures in December and January are the highest of the year, with an average temperature of about 30 ℃ in the daytime and 22 ℃ in the evening; the temperatures from June to August are the lowest, with an average temperature of about 17 ℃ in the daytime and 8 ℃ in the evening; and in February and March, the temperatures are 28 ℃ and 20 ℃ in the daytime and evening, respectively. The average temperatures in the day and night in April are 24 ℃ and 16 ℃, respectively. The average temperature in the day and night in May is 20 ℃ and 12 ℃ respectively. Figure 3 shows the temperature change in Sydney from June 1 to July 17 and Figure 4 shows the temperature change from 20:00 to 17:00 in a day in July in Beijing.

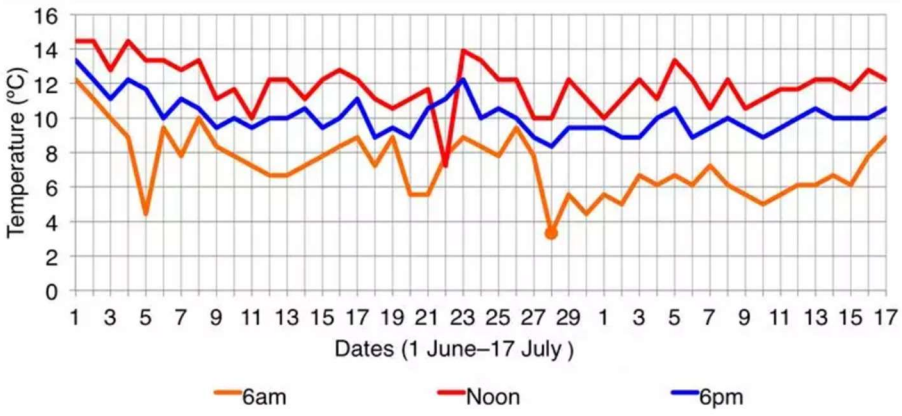


Fig. 5.3: temperature change of Sydney from June 1 to July 17.

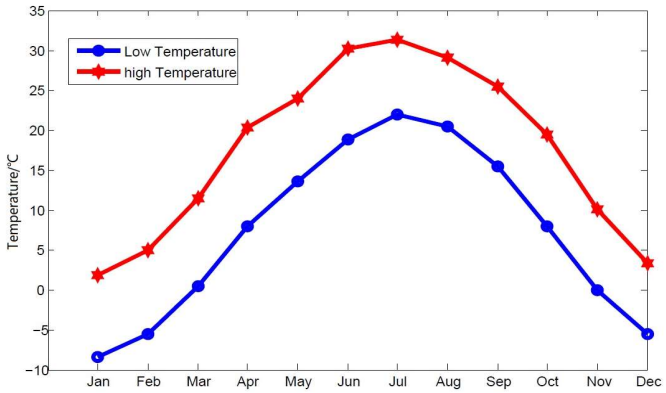


Fig. 5.4: The temperature change in 2019 in Beijing.

Based on the above temperatures, a series of ambient temperatures can be selected, which are - 10 ℃, 0 ℃, 10 ℃, 20 ℃ and 30 ℃. In addition, the high temperature weather from 38 ℃ to 42 ℃ often occurs in summer in Sydney. Therefore, 40 ℃ is also selected in this paper and a special temperature of 50 ℃ is added as the upper limit of the maximum ambient temperature.

5.2 Convection Thermal Coupling Modeling of Adjacent Devices

5.2.1 FEM Modeling

The calculation method of thermal coupling effect is complex. The calculation method of thermal conduction coupling in [59] is based on the principle of linear superposition: a power loss P is applied to one device (device I) and the temperature rise of the adjacent device (device II) is supposed to be caused by the thermal conduction coupling from device I. Then change into give device II a power loss P to affect device I. The conduction thermal coupling between device I and device II can be obtained by this method. However, it has limitations which is only applicable to linear relations [55, 59]. The thermal coupling between power devices contains non-linear convection term. Therefore, there will be errors if the superposition principle is still adopted [3].

Based on the above, FEM modeling is establish in this paper to simulate the convection thermal coupling between adjacent power devices and to calculate the jucntion temperature in different ambient temperatures.

This paper simplifies the structures of the power devices (MOSFET and diode) to better analyze the convective thermal coupling effect between adjacent devices. In addition, in order to get more accurate results and save the simulation time, multi-level grid meshing method is adopted where in the the key layer (chip layer) finer mesh is given and in other layers such as substrate and PCB coarse mesh is used.

5.2.2 Convection Thermal Coupling Simulation and Junction Temperature Calculation

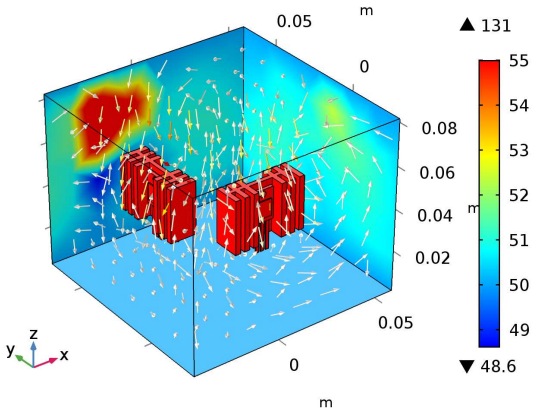
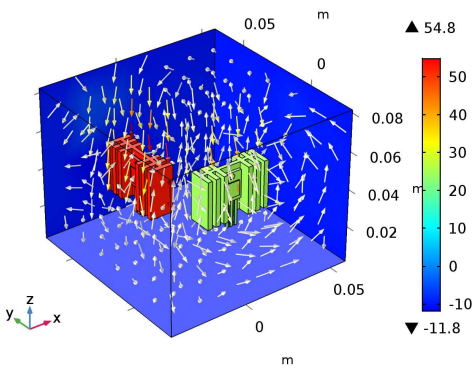
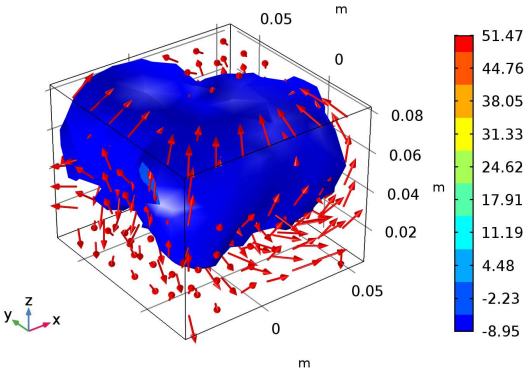


Fig. 5.5: The temperature distribution of convective thermal coupling.

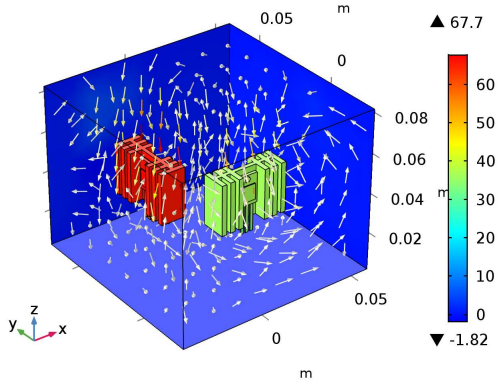
The power loss of the MOSFET is set to 5 W and the diode to 2 W. As the value of power loss for MOSFET is higher than that for diode, the surrounding ambient temperature for MOSFET is also higher than that for diode, as shown in Fig. 5.5. Through the FEM analysis, the temperature distribution and isosurface distribution of power devices under different ambient temperatures are obtained, as shown in Fig. 5.6.



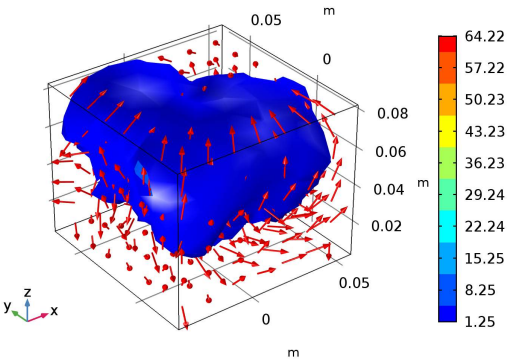
（a_1）



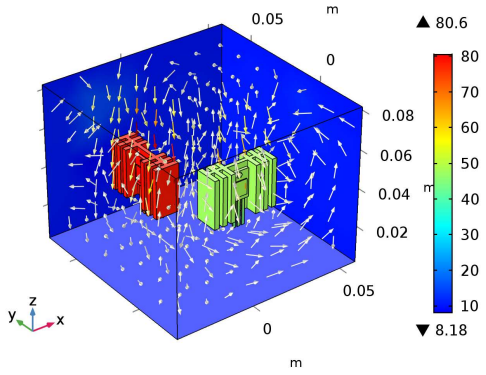
（a_2）



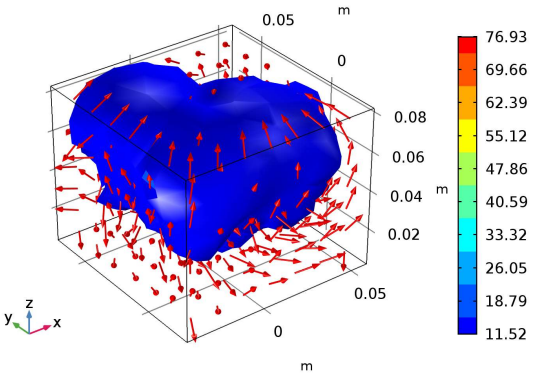
（b_1）



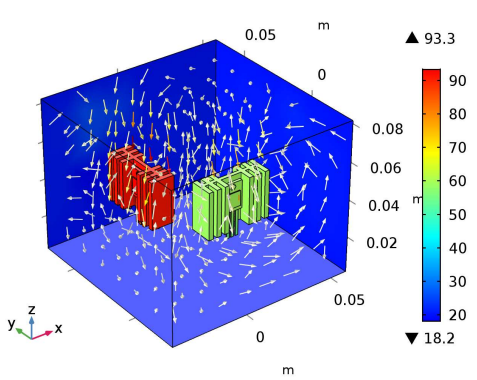
（b_2）



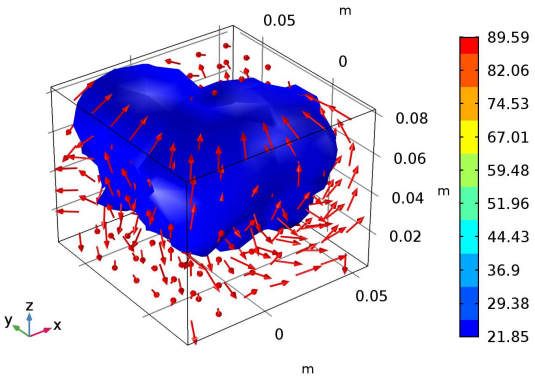
（c_1）



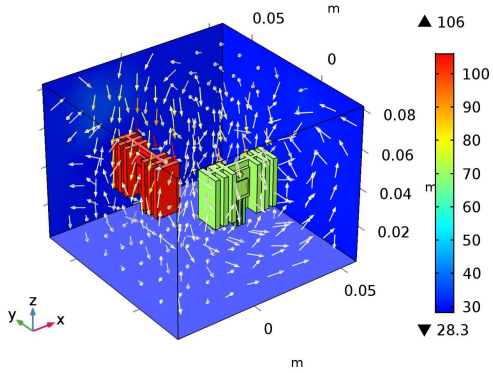
（c_2）



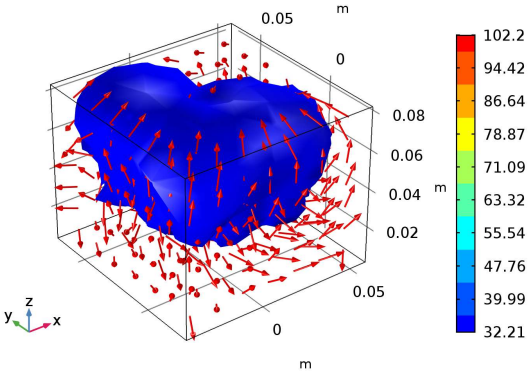
（d_1）



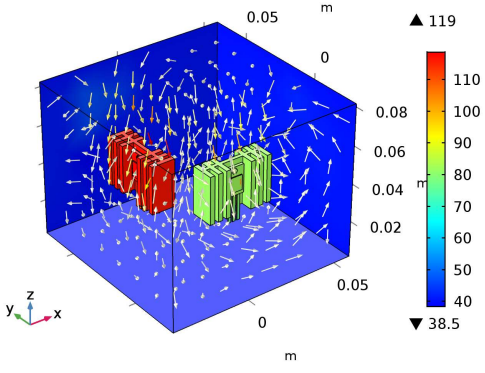
（d_2）



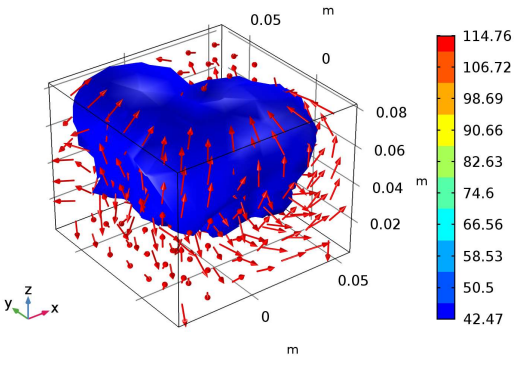
（e_1）



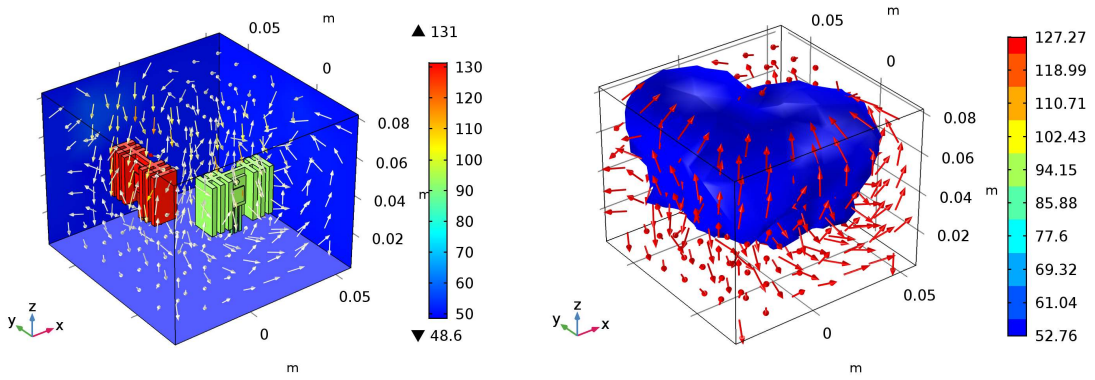
（e_2）



（f_1）



（f_2）



（g_1）　　（g_2）

Fig. 5.6: Simulation analysis of convective thermal coupling. (a_1) and (a_2) are temperature distribution and isosurface distribution when T_a = - 10 ℃; (b_1) and (b_2) are temperature distribution and isosurface distribution when T_a = 0 ℃; (c_1) and (c_2) are temperature distribution and isosurface distribution when T_a = 10 ℃; (d_1) and (d_2) are T_a = 20 Temperature distribution and isosurface distribution at ℃; (e_1) and (e_2) are temperature distribution and isosurface distribution at T_a = 30 ℃; (f_1) and (f_2) are temperature distribution and isosurface distribution at T_a = 40 ℃; (g_1) and (g_2) are temperature distribution and isosurface distribution at T_a = 50 ℃.

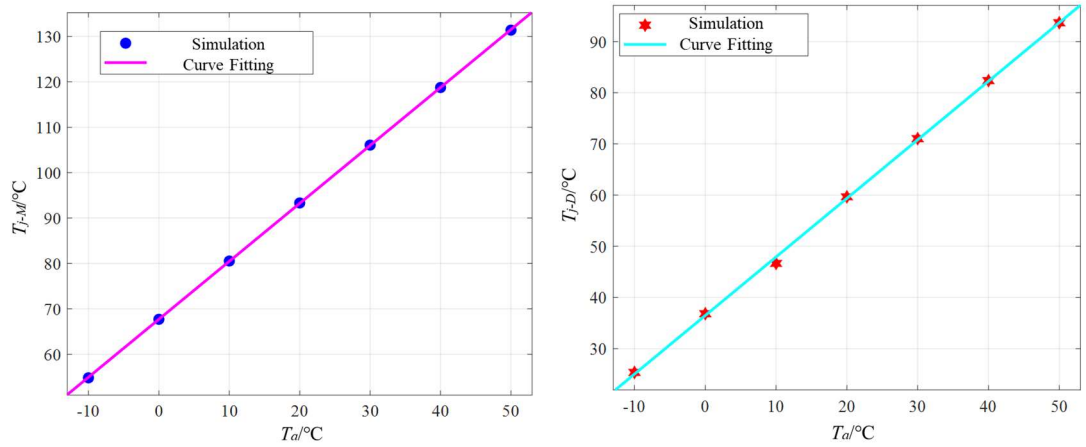
In the simulation, the junction temperature of the device can be directly detected by adding a virtual probe. The junction temperatures of the device under different ambient temperatures can be obtained considering the convective thermal coupling between power devices, as shown in Table 5.2.

Table 5.2: The junction temperatures under different ambient temperatures.

T_a/℃	-10	0	10	20	30	40	50
T_{j_M}/℃	54.81	67.70	80.54	93.33	106.07	118.76	131.40
T_{j_D}/℃	25.35	36.82	46.65	59.66	71.03	82.37	93.67

5.2.3 The Relationships Between Junction Temperature and Ambient Temperatures

The steady-state junction temperatures of power devices in Table 5.2 are used to fit the relationships between junction temperatures and ambient temperatures, and the relationships for MOSFET and diode are shown in Fig. 5.6 and (5.1).



（a） （b）

Fig. 5.6: The relationships between junction and ambient temperatures.

a) for MOSFET; b) for diode.

$$\begin{cases} f\left(T_{j\text{-}M}\right) = p_1 T_a + p_2 \\ f\left(T_{j\text{-}D}\right) = p_3 T_a + p_4 \end{cases} \tag{5.1}$$

The fitting coefficients of the relationships for MOSFET and diode are

$$\begin{cases} p_1 = 1.28 \\ p_2 = 67.73 \\ p_3 = 1.14 \\ p_4 = 36.48 \end{cases} \tag{5.2}$$

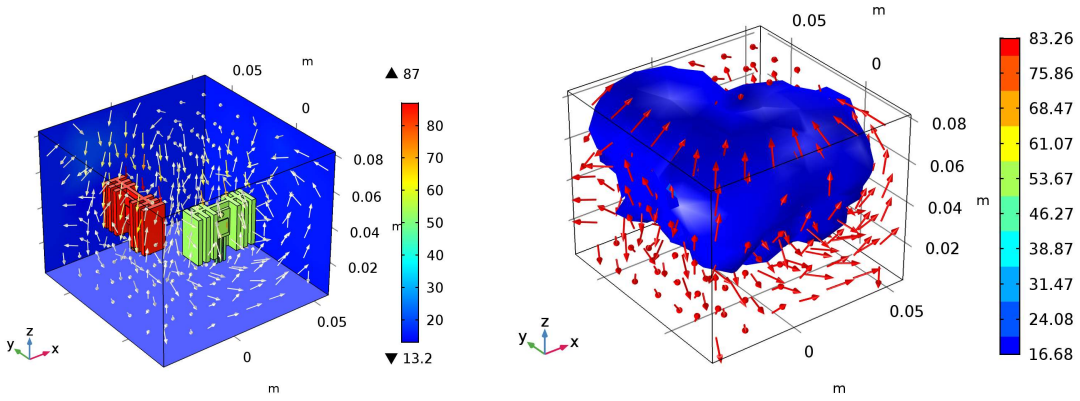
When the ambient changes as a function of time [28], the relationships between the junction and ambient temperature can be expressed as

$$\begin{cases} f\left(T_{j\text{-}M}\left(t\right)\right) = p_1 T_a\left(t\right) + p_2 \\ f\left(T_{j\text{-}D}\left(t\right)\right) = p_3 T_a(\mathrm{t}) + p_4 \end{cases} \tag{5.3}$$

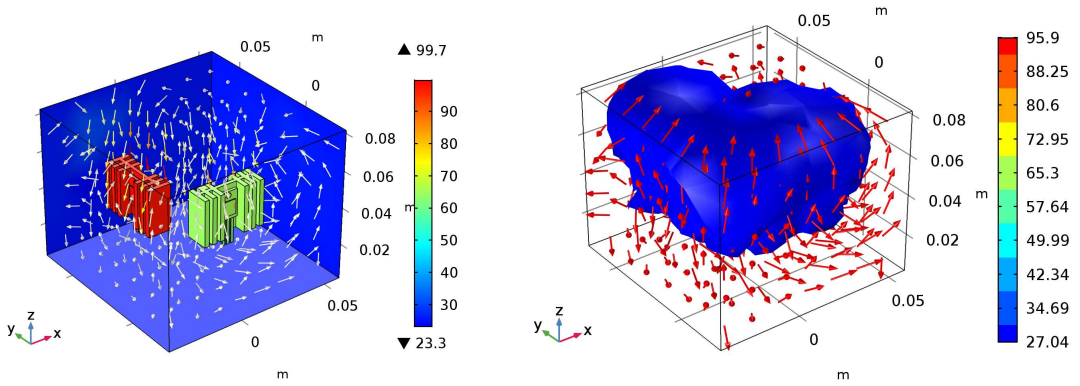
5.3 Modeling Verification

5.3.1 The Simulation Analysis Under New Temperature Profile

In order to verify the correctness of the model and the relationship between device junction temperature and ambient temperature, a new finite element simulation model under the ambient temperature profile is established. The ambient temperature is 15 ℃, 25 ℃, 35 ℃, 45 ℃, respectively. The simulated temperature distribution and isosurface distribution are shown in Fig.5.7.



（a_1）　　（a_2）



（b_1）　　（b_2）

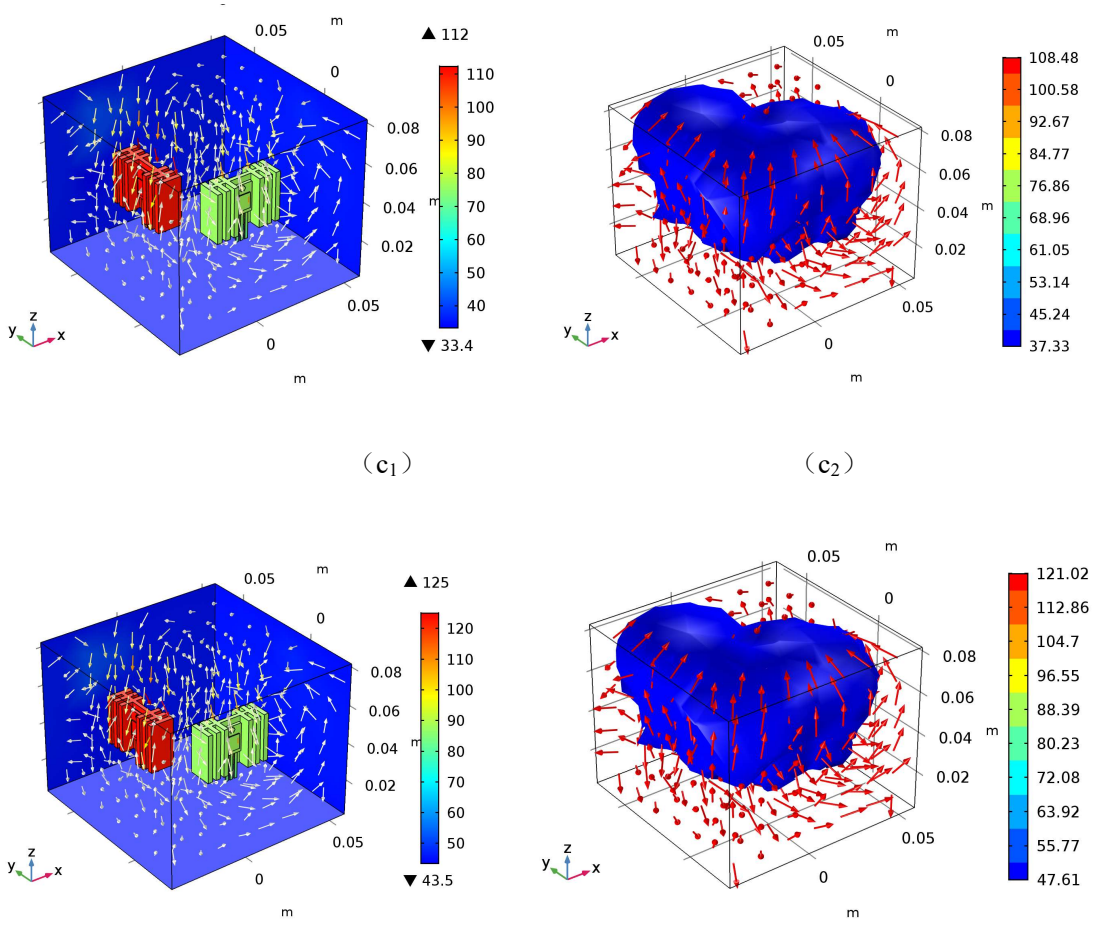


Fig. 5.7. The simulation analysis of convective thermal coupling (a_1) and (a_2) are the temperature distribution and isosurface distribution at T_a = 15 ℃, (b_1) and (b_2) are the temperature distribution and isosurface distribution at T_a = 25 ℃, (c_1) and (c_2) are the temperature distribution and isosurface distribution at T_a = 35 ℃, (d_1) and (d_2) are the temperature distribution and isosurface distribution at T_a = 45 ℃.

5.3.2 Junction Temperature Calculation and Comparisons

The new junction temperatures can be obtained from FEM simulations in Fig.5.7 and the junctions at new ambient temperatures can be obtained through (5.1) and (5.2). The comparisons of the junction temperatures by simulation and calculation for MOSFET and

diode are given in Tables 5.3 and 5.4, respectively. By comparisons, the maximum error of MOSFET is 0.08% and the maximum error of diode is 0.70%, which show the feasibility and effectiveness of the proposed method.

Table 5.3: The junction temperature comparisons of calculation and simulation for MOSFET.

T_a/℃	15	25	35	45
T_{c_M}/℃(Calculation)	86.87	99.63	112.39	125.15
T_{c_M}/℃ (FEM)	86.94	99.71	112.42	125.08
Error /%	0.08%	0.08%	0.03%	0.06%

Table 5.4: The junction temperature comparisons of calculation and simulation for diode.

T_a/℃	15	25	35	45
T_{c_D}/℃ (Calculation)	53.58	64.98	76.38	87.78
T_{c_D}/℃ (FEM)	53.96	65.35	76.70	88.02
Error /%	0.70	0.57	0.42	0.27

5.4 Conclusions

The convection thermal coupling effect between adjacent devices and the junction temperature of the power devices are affected by the ambient temperatures. Based on the FEM analysis, the temperature distribution and isosurface distribution of the adjacent semiconductor devices are obtained. The relationships between the junction temperature and the ambient temperature under different environmental temperatures are analyzed by collecting the junction temperatures of the devices. Finally, the relationships under different ambient temperatures are verified by new FEM models.

Chapter 6 Modeling Analysis of Conduction Thermal Coupling Between IGBT Modules

According to the analysis in Section 1.1, IGBT power modules are generally used in medium and high-power fields, and MOSFET devices are generally used in small and medium power fields. The IGBT modules are always used in the three-phase inverter for controlling the motor. In a motor inverter, multiple IGBT modules are placed on an air-cooled/water-cooled heatsink in parallel, and the thermal transfer way is mainly the thermal conduction [102].

This chapter takes the IGBT modules in a three-phase motor inverter and MOSFET power converter as the research objects to discuss the conduction thermal coupling effect between the adjacent power modules/devices, the electric thermal model for power converters and the FEM models for IGBT modules are established. Based on the simulation analysis, the conduction thermal coupling resistance network for the paralleled adjacent IGBT modules is established, and the self-thermal resistance and the conduction thermal coupling resistance are calculated, and the junction temperature of the modules is calculated.

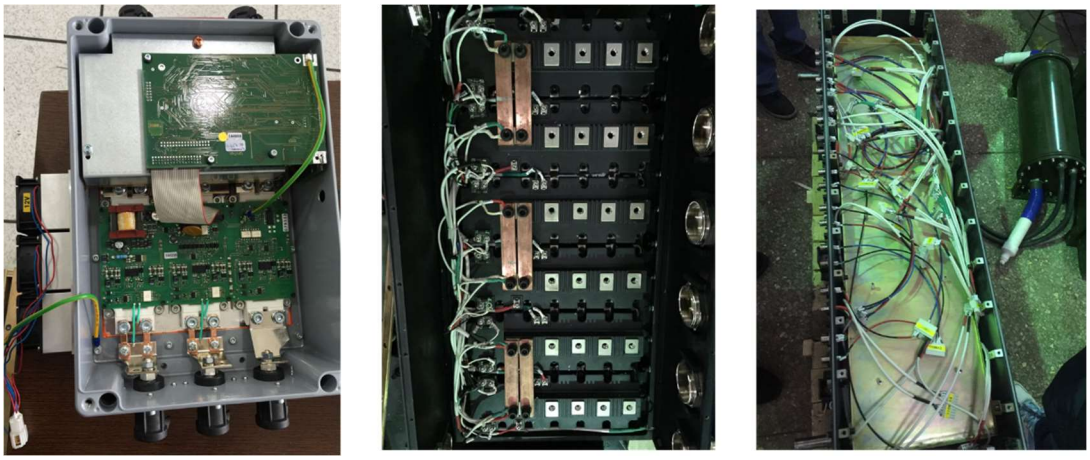
6.1 Analysis of Conduction Thermal Coupling Effect

In this section, the conduction thermal coupling effect between modules/devices is analyzed by the FEM and PLECS simulations.

6.1.1 Analysis of Conduction Thermal Coupling Between IGBT Modules

According to the losses calculation of the IGBT power module in Section 3.1, when the IGBT module works, the power losses will be transferred in the form of thermal. In the process of thermal transfer, the T_j of the chip will rise, and the power module will be cooled by certain thermal dissipation conditions (such as a water-cooled or air-cooled heatsinks, etc.), and the chip will finally reach a steady-state [103, 104]. In order to ensure the safety and

reliability of the IGBT modules, the T_j of the chips should be less than the maximum T_j, T_{jmax}, for example, the T_{jmax} of the silicon chip is 175 ℃. With the high-power demand of power systems, IGBT modules develop towards high-frequency, high-power, and highly integrated direction, and the thermal output of modules increases greatly. At the same time, as shown in Fig. 6.1, multiple IGBT modules are paralleled on the same heatsink in a close distance, which greatly reduces the effective thermal dissipation area.



（a） （b） （c）

Fig. 6.1: power inverter with multiple IGBT modules in parallel. (a) three IGBT modules (for the three-phase bridge); (b) six IGBT modules (every two in parallel); (c) eleven IGBT modules (three in parallel, the other two are used to control the fan and brake resistor respectively).

Under the limited thermal dissipation conditions, the thermal coupling effect between adjacent modules become more serious, which will affect the working performance of the modules, and then affect the working reliability of the whole inverter system. As shown in Fig. 1.5 in Section 1.1, the IGBT module has thermal failure due to long-term high T_j.

6.1.2 FEM Analysis of IGBT Modules

In this section, in order to analyze the conduction thermal coupling effect between multiple IGBT modules on the same heatsink, the FEM analysis model of adjacent modules in a three-phase inverter is established. The structure diagram of a single IGBT module and

the relevant parameters of each key structural layer are given in Fig.6.2 and the calculation results are shown in Fig. 6.3.

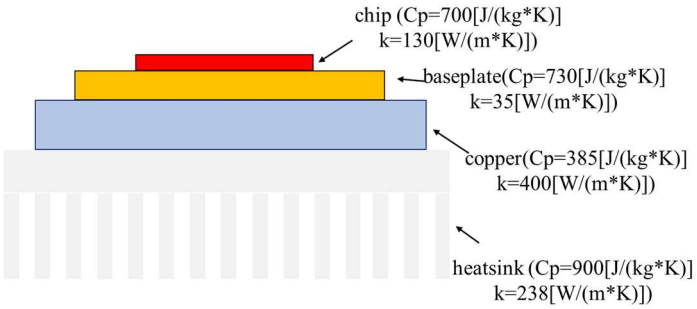
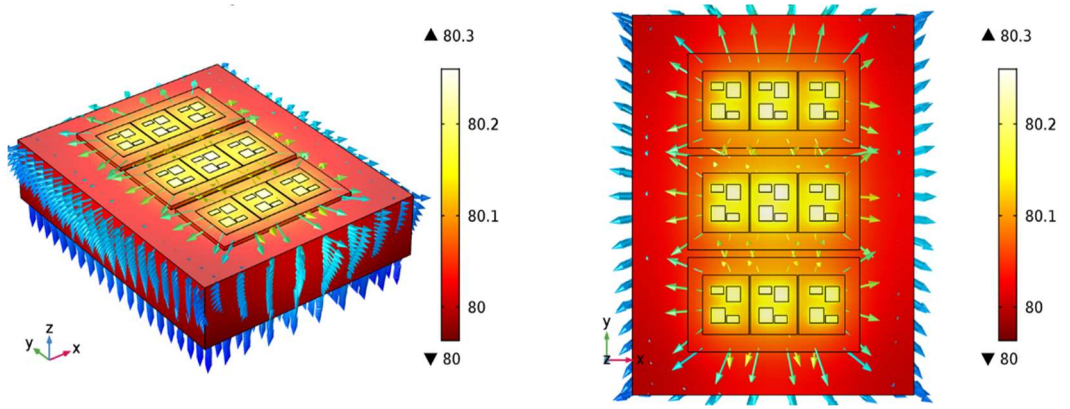
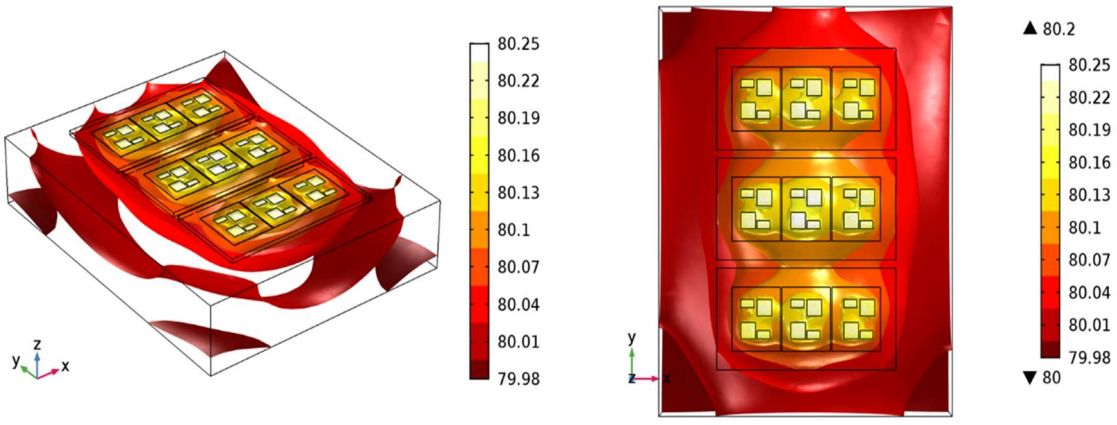


Fig. 6.2: IGBT module and parameters of the structure layers.



（a）



（b）

Fig. 6.3: FEM analysis: (a) temperature distribution; (b) temperature isosurface distribution.

From the FEM analysis, the temperature distribution and isosurface distribution of the power module can be obtained. Different colors represent different temperatures, and the

direction of the body arrows indicate the direction of thermal transfer. According to the simulation results, the temperature at the chip is the highest (marked in bright white), and the thermal is transferred from the chip to the substrate vertically in the module, and the temperature decreases in turn, as shown in Fig. 6.3 (a). When the thermal is transferred to the heatsink, the thermal is transferred vertically and horizontally at the same time. As shown in Fig. 6.3 (b), the temperature between adjacent modules is also relatively high. This is because multiple modules are placed close to each other on the same heatsink, and the thermal is affected by each other in the process of transverse transmission, forming the conduction thermal coupling.

6.1.3 Electro-thermal Coupling Simulation Analysis of Power Converter System

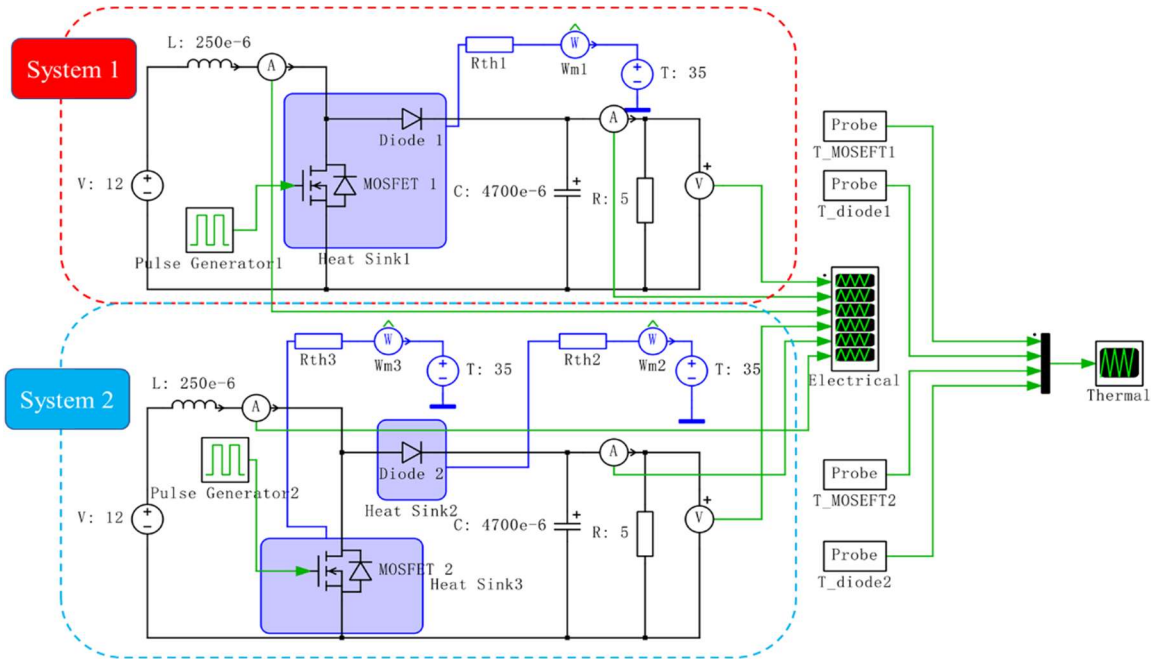
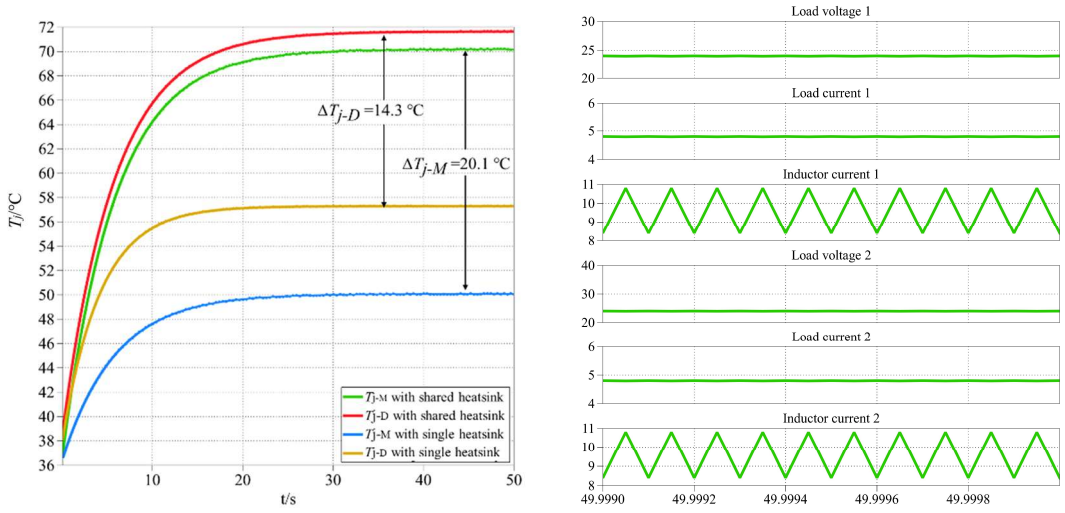


Fig. 6.4: PLECS thermal models. System 1 is with a shared heatsink; System 2 is with two separate heatsinks.

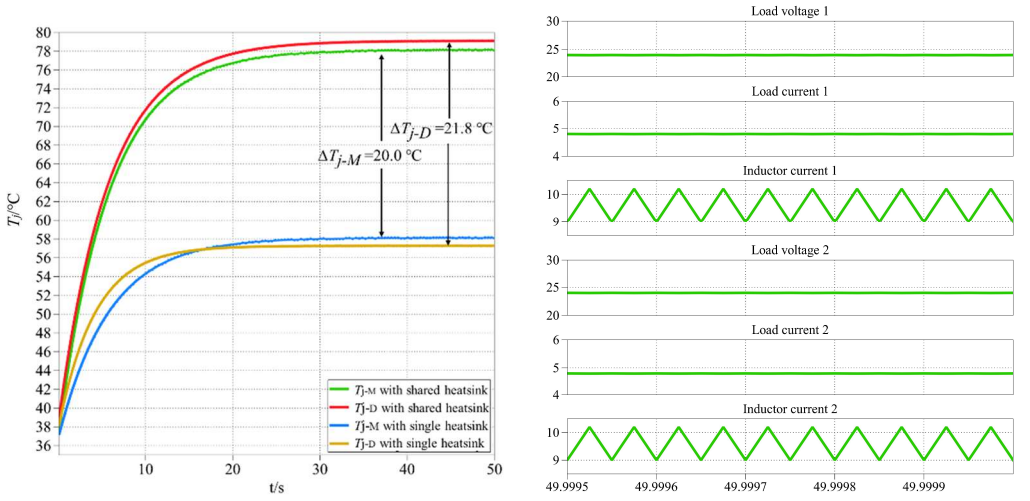
In a DC-DC boost converter, the MOSFET and the diode are two key thermaling components which can affect the performance of the overall converter systems [105]. PLECS has its advantages to simulate the dynamic systems for power converters [106]. The simulation schematics are shown in Fig. 6.4. These figures give basic thermal models which are used for thermal descriptions and the T_j increments' (ΔT_j) comparisons.

The thermal model simulates the boost converter at different frequencies (10 kHz, 20 kHz, and 50 kHz) and different loading resistances (5 Ω, 8 Ω, and 10 Ω). Fig. 6.5 gives the ΔT_j at different frequencies (load: 5 Ω) for the MOSFET (duty cycle: 0.5) and the diode with a shared heatsink (System 1) and two separate heatsinks (System 2), respectively. Fig. 6.6 gives the ΔT_j at different loads (frequency: 20 kHz). The load voltage, load current, and inductor current under different working conditions are also given in Figs. 6.5 and 6.6.

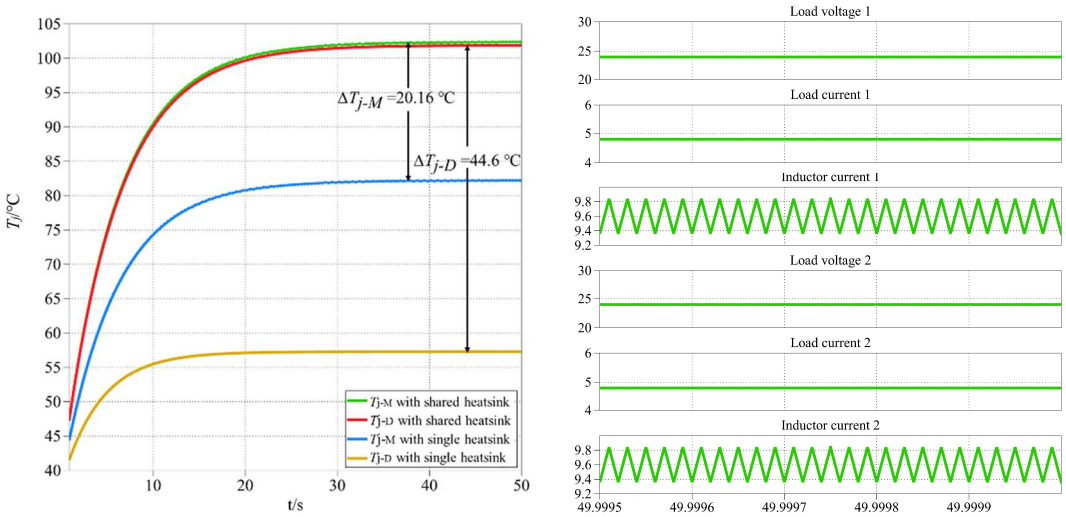
Based on the simulation results, the value of ΔT_j increases while the frequency increases which indicates a greater thermal coupling effect at a higher frequency. The value of ΔT_j decreases with the smaller operating current (by increasing loading resistance). In other words, the greater thermal coupling effect will be induced by a larger current passing through the MOSFET and the diode, and vice versa. Moreover, the T_j of the MOSFET and the diode with a shared heatsink are relatively higher than the ones with separate single heatsinks. The major reason for causing these is the conduction thermal coupling between the two devices, since they share the same heatsink. However, these kinds of models cannot calculate the convection coupling.



（a）

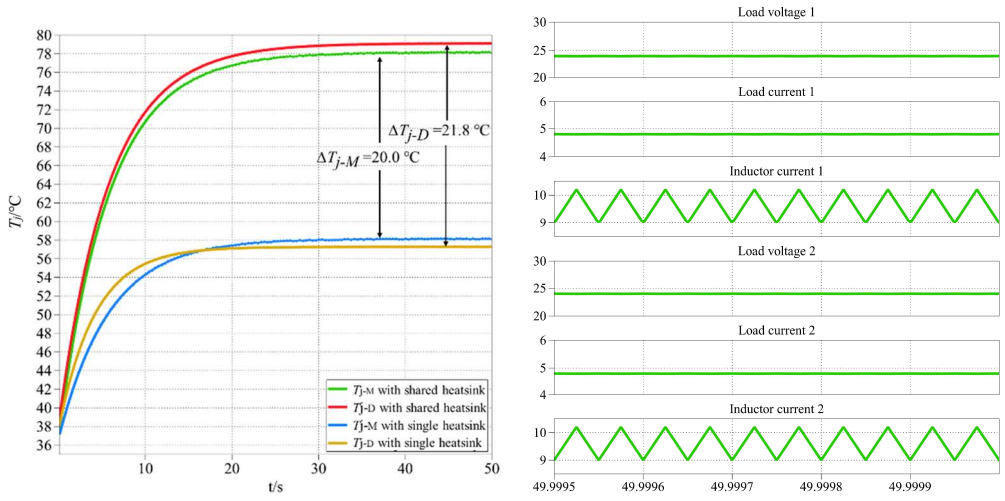


（b）

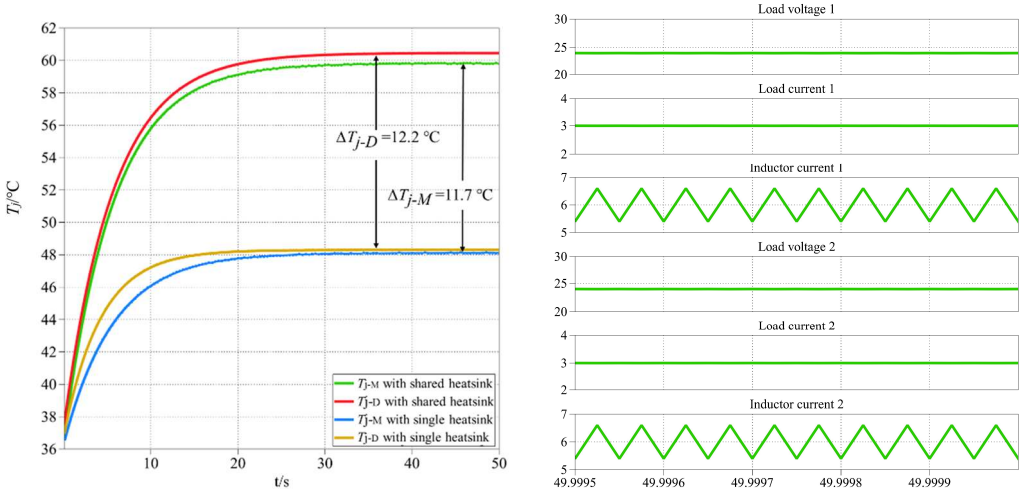


（c）

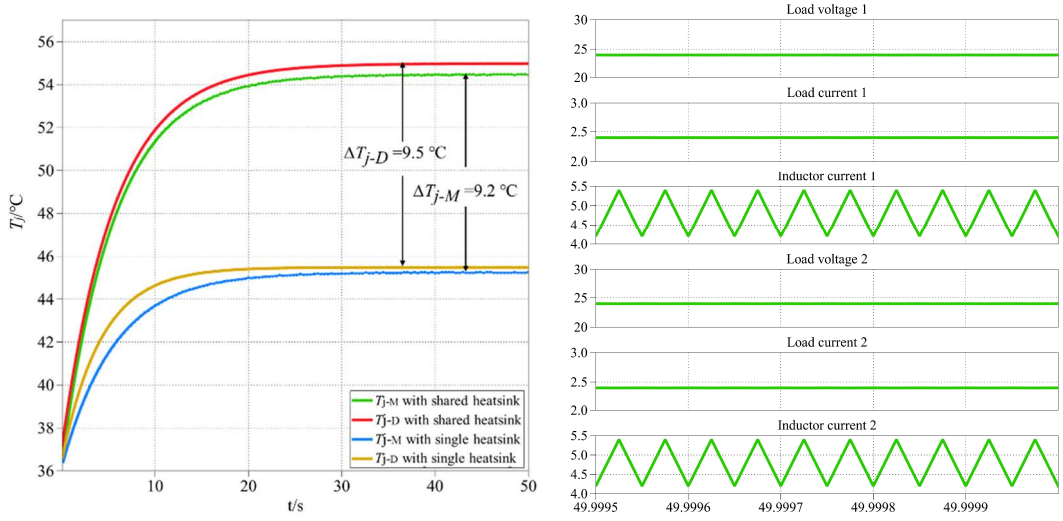
Fig. 6.5: ΔT_j at different frequencies (duty cycle: 0.5; load: 5 Ω): (a) at a frequency of 10 kHz; (b) at a frequency of 20 kHz; and (c) at a frequency of 50 kHz.


Tj/℃
t/s
ΔTj-D =21.8 ℃
ΔTj-M =20.0 ℃
Tj-M with shared heatsink
Tj-D with shared heatsink
Tj-M with single heatsink
Tj-D with single heatsink
Load voltage 1
Load current 1
Inductor current 1
Load voltage 2
Load current 2
Inductor current 2

（a）


Tj/℃
t/s
ΔTj-D =12.2 ℃
ΔTj-M =11.7 ℃
Tj-M with shared heatsink
Tj-D with shared heatsink
Tj-M with single heatsink
Tj-D with single heatsink
Load voltage 1
Load current 1
Inductor current 1
Load voltage 2
Load current 2
Inductor current 2

（b）


Tj/℃
t/s
ΔTj-D =9.5 ℃
ΔTj-M =9.2 ℃
Tj-M with shared heatsink
Tj-D with shared heatsink
Tj-M with single heatsink
Tj-D with single heatsink
Load voltage 1
Load current 1
Inductor current 1
Load voltage 2
Load current 2
Inductor current 2

（c）

Fig. 6.6. ΔT_j at different loading resistances (f: 20 kHz): (a) at a load of 5 Ω; (b) at a load of 8 Ω; and (c) at a load of 10 Ω.

In addition, the T_j of MOSFET and diode in System 1 is generally higher (with shared heatsink) than that in system 2 (with separate heatsinks). One of the important reasons for the temperature differences is that the two devices share a heatsink, which is affected by the conduction thermal coupling between the devices.

As the thermal conductivity of aluminum heatsink is high, when the power devices share the heatsink, the distance between the devices is close, and the device temperature affects each other through the shared heatsink. When the devices use independent heatsinks, the distance between the devices is relatively far and the devices are not in contact, and then the temperature will be lower than the ones with shared heatsinks. Therefore, the conduction thermal coupling is one of the important reasons for the difference of T_j/T_c under different working conditions.

6.2 Modeling of Thermal Conduction Coupling Between Power Modules

6.2.1 Conduction Thermal Coupling Effect Between Power Modules

For motor power inverter, more than three IGBT modules are required to realize the three-phase application, as shown in Fig. 6.1 (a); for the higher power inverters, more devices or power modules are required to meet the requirements, as shown in Fig. 6.1(b) and (c). Based on the analysis of the thermal coupling effect of adjacent modules/devices in Chapter 3, the thermal coupling analysis model of several power modules in a three-phase motor inverter is established in this section. The type of the IGBT module adopted is FF1400R17IP4 and the thermal flow diagram of the paralleled IGBT modules is given in Fig. 6.7.

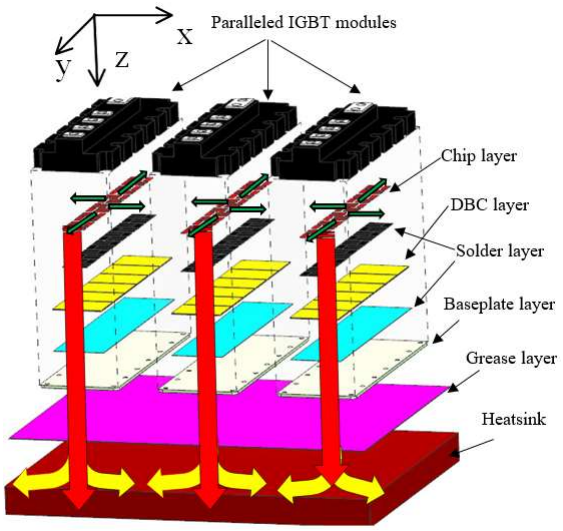


Fig. 6.7: The thermal flow diagram of the paralleled IGBT modules.

As shown in Fig. 6.7, different colors represent different layers. In the chips layer, thermal coupling exists among the IGBT and diode chips. In the inverter system, two parts of thermal flow in the paralleled IGBT modules are as follows: the most losses flow in the vertical direction, another part flows in the horizontal direction.

6.2.2 Conduction Thermal Coupling Modeling Between Adjacent IGBT Modules

In a power inverter system, thermal coupling exists between the chips and modules. As the length and width of the silicon chips and other layers are far greater than the thickness in an IGBT module, the layers can be treated as thin-walled structures. Thermal generated by power loss will transfer from chips to heatsink through copper substrate quickly and the thermal coupling time between chips in the IGBT module is quite short. The single module is treated as a whole object, and the thermal coupling between modules is taken into consideration. Based on existed thermal resistance networks, a thermal coupling model forparalleled IGBT modules can be given as Fig. 6.8.

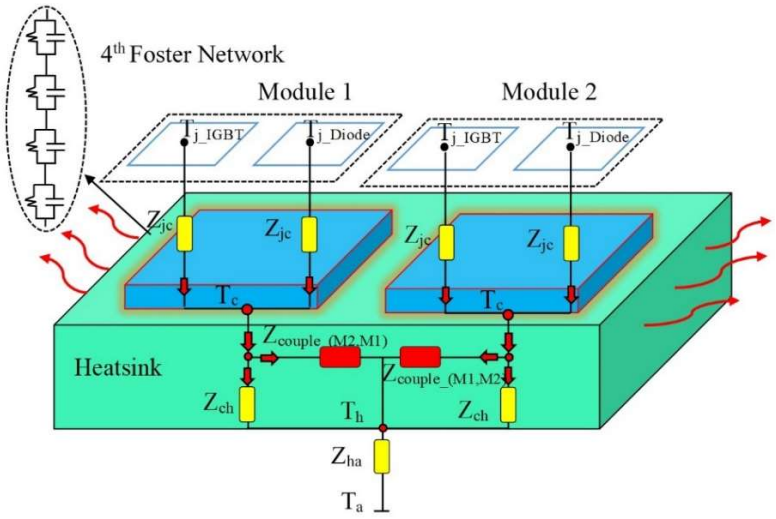


Fig. 6.8: Thermal coupling model for paralleled IGBT modules.

In the established thermal model, the formed thermal impedance is mainly the junction-to-case thermal impedance (Z_{thjc}), and the case-to-heatsink impedance (Z_{thch}) and the horizontal conduction coupling thermal impedance ($Z_{thcouple}$) and the heatsink-to-ambient thermal impedance (Z_{thha}). The model established in this section ignores the thermal coupling between the chips and takes a single IGBT module as a whole.

6.2.3 Calculation of Conduction Thermal Coupling Resistances and Junction Temperature

The fourth-order Foster network is used in [107] and [108] to fit the thermal impedance Z_{thjc} of the power module and the fourth-order Foster network was proved to meet the accuracy requirements of the Z_{thjc}. According to the datasheet provided by the power module manufacturer, the fitting formula is as follows:

$$Z_{thjc} = \sum_{i=1}^{n} r_i \cdot \left(1 - e^{-t/\tau_i}\right) \qquad (6.1)$$

where $n = 4$, the parameters r_i and τ_i can be obtained from Table 6.1.

Table 6.1: IGBT module parameters.

	r_{1} / (K/KW)	r_{2} / (K/KW)	r_{3} / (K/KW)	r_{4} / (K/KW)	τ_1/s	τ_2/s	τ_3/s	τ_4/s
IGBT	1	11.3	2.2	1	0.001	0.03	0.1	1
Diode	2.168	2.763	25.89	1.774	0.000661	0.00685	0.0417	2.07

Bring the parameters from Table 6.1 into (6.1) and the Z_{thjc} of the power module can be obtained as shown in Fig. 6.9. The solid line in the figure is Z_{thjc} for diode, and the circle dotted line is Z_{thjc} for IGBT, and the coordinates are all marked in the form of exponential.

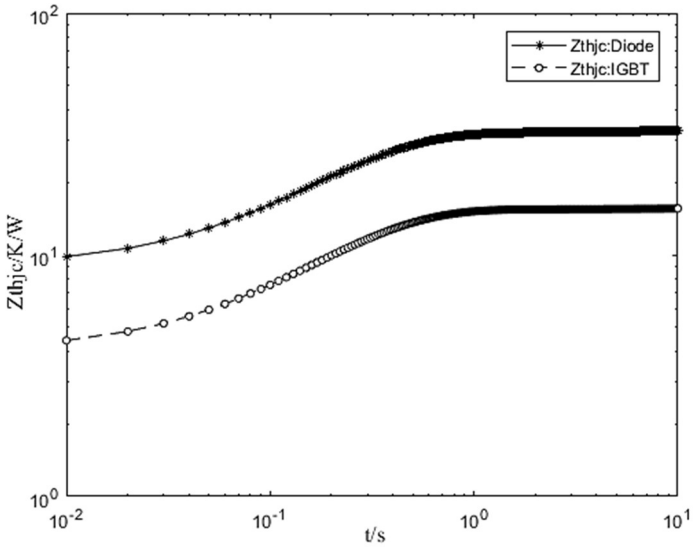


Fig. 6.9: Transient thermal impedance Z_{thjc}.

According to the classification of the thermal impedance, it can be divided into self-thermal impedance and thermal coupling impedance [55]. Based on [109], the self-thermal impedance matrix of the power module can be expressed as:

$$Z_{self}=\begin{bmatrix} Z_{self\_M1} & & 0 \\ & \ddots & \\ 0 & & Z_{self\_Mn} \end{bmatrix} \tag{6.2}$$

where Z_{self_Mi} is the sigle IGBT module self-thermal impedance.

According to the proposed model established in section 6.2.2, the conduction coupling resistance module 1 to module 2 $Z_{couple\_(M1,M2)}$ can be expressed as:

$$Z_{couple\_}(M1,M2) = \frac{T_{M2} - T_a}{P_{loss\_M1}} \tag{6.3}$$

Similarly, the conduction thermal coupling impedance of power module 2 to module 1 $Z_{couple\_(M2,M1)}$ can be expressed as:

$$Z_{couple\_}(M2,M1) = \frac{T_{M1} - T_a}{P_{loss\_M2}} \tag{6.4}$$

Therefore, for any two adjacent power modules i and j, the conduction thermal coupling impedance of module j to module i $Z_{couple\_(Mj,Mi)}$ can be expressed as:：

$$Z_{couple\_}(Mj,Mi) = \frac{T_{M\,i} - T_a}{P_{loss\_Mj}} \tag{6.5}$$

Base on (6.5), the thermal coupling impedance matrix Z_{couple} is adopted as follows.

$$Z_{couple} = \begin{bmatrix} 0 & \cdots & Z_{couple\_(Mn,\ M1)} \\ Z_{couple\_(M1,\ M2)} & \vdots & Z_{couple\_(Mn,\ M2)} \\ Z_{couple\_(M1,\ Mn)} & \cdots & 0 \end{bmatrix} \tag{6.6}$$

In the thermal coupling model, Z_{ha} is the impedance from heatsink to air. Z_{ch} is the impedance from case-to-heatsink and the equivalent thermal impedance Z_{hp} of Z_{couple} and Z_{ch} can be defined as：

$$Z_{hpi} = \frac{Z_{ch(Mi,\ Mj)} + Z_{couple(Mi,\ Mj)}}{Z_{ch(Mi,\ Mj)} Z_{couple(Mi,\ Mj)}} \tag{6.7}$$

The junction temperature matrix T_{ji} for the IGBT module can be expressed as

$$\begin{bmatrix} T_{j1} \\ T_{j2} \\ \vdots \\ T_{jn} \end{bmatrix} = \begin{bmatrix} P_{loss\_j1} & & \\ & \ddots & \\ & & P_{loss\_jn} \end{bmatrix} \cdot \begin{bmatrix} Z_{thjc1} \\ \vdots \\ Z_{thjcn} \end{bmatrix} + \begin{bmatrix} P_{loss\_M1} & & \\ & \ddots & \\ & & P_{loss\_Mn} \end{bmatrix} \cdot \begin{bmatrix} Z_{hp_1} \\ \vdots \\ Z_{hpn} \end{bmatrix}$$

$$+\sum_{i=1}^{n} P_{loss\_M_i} \cdot Z_{ha} + T_a \qquad (6.8)$$

6.3 Model Validation

In order to verify the accuracy of the conduction thermal coupling resistance network model of adjacent power modules, the simulation model of a three-phase motor inverter under different output currents is established on IPOSIM [110], which is an online simulation software provided by Infineon company. The output current, output frequency, power factor, and other relevant parameters used in the simulation are shown in Table 3.3. Through the simulation, the power losses of the IGBT power module (IGBT chip, diode chip) under different working currents can be calculated and the results are shown in Table 6.2.

Table 6.2: Parameters of power inverter.

Output current	Output frequency	Modulation index	Power factor cos(∅)
10A/20A/30A	50 Hz	1	1

Table 6.3: Calculation of IGBT module loss.

	I = 10 A	I = 20 A	I = 30 A
IGBT	17.50 W	21.37 W	25.38 W
Diode	1.85 W	3.01 W	4.06 W

By bring the losses of the power module into (6.8), the T_j of the IGBT module under different output currents can be obtained, as shown in Fig. 6.10. In the figure, the T_j of the

IGBT chip is marked as solid lines, and that of the diode chip are hollow solid lines. With the increament of the output currents, the T_j of IGBT and diode increases, and finally reaches a steady state. The higher the power loss of the chip is, the higher the steady-state T_j is. When the output current is the highest (30 A), the T_j of IGBT and diode chip is the highest and under the same working current, the T_j of the IGBT chip is higher than that of the diode.

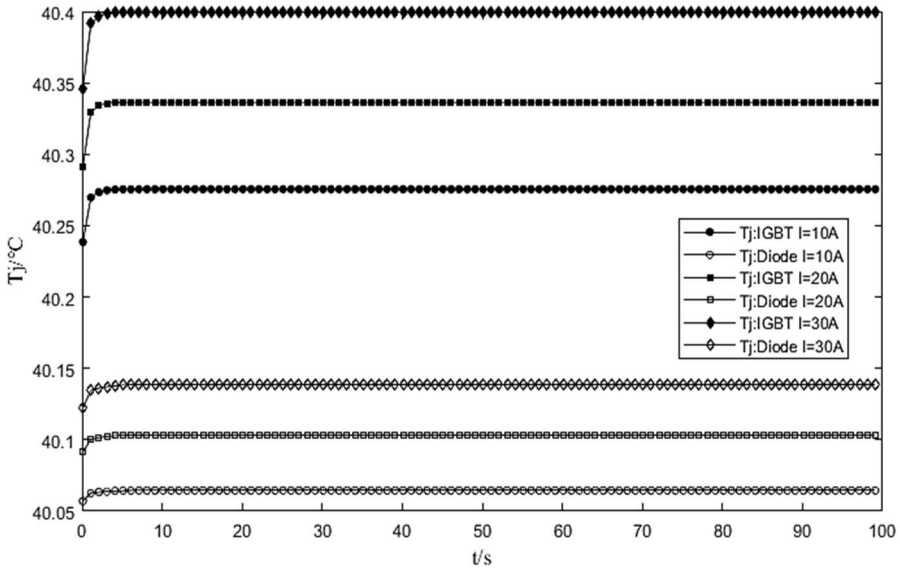


Fig. 6.10: Junction temperatures of the IGBT module.

The IPOSIM simulation software provided by Infineon can be used for power converter system loss and thermal calculation [111, 112]. Comparing the conduction thermal coupling resistance network model and junction temperature calculation method of adjacent modules established in Section 3.4 with the simulation results of IPOSIM, the errors of IGBT and diode chips under different output currents can be obtained, as shown in Table 3.5, in which the maximum error is 6.05% and 4.50%, respectively.

Table 6.4: Comparison of the errors for IGBT modules under different current.

	I = 10 A	I = 20 A	I = 30 A
IGBT	4.12%	3.95%	6.05%
Diode	2.27%	4.50%	4.43%

6.4 Conclusions

(1) The FEM analysis model of a three-phase motor inverter is established, and the conduction thermal coupling effect of the adjacent power modules is analyzed.

(2) The conduction thermal coupling simulation model of different power converter systems is established, and the junction temperature difference of different systems and working conditions is compared.

(3) The conduction thermal coupling resistance network model of adjacent IGBT modules is established, and the calculation method of junction temperature is proposed based on the model. In order to verify the proposed thermal model, the simulation model of three-phase power inverter is established in the professional simulation software IPOSIM provided by Infineon company, and the junction temperatures of IGBT module chips (including IGBT chip and diode chip) under different output currents are compared. The comparison results show that the established model and the proposed junction temperature calculation method have certain accuracy and effectiveness.

The disadvantage of the model proposed in this chapter are that: 1) it does not consider the effect of thermal coupling between chips in the module; 2) the temperature-rise will affect the electrical parameters of the power module, and the change of electrical parameters will also affect the power loss of module, which is one of the reasons for the errors of junction temperature calculation.

However, this paper focuses on the conduction thermal coupling effect between adjacent modules, and the comparisons between the calculated results of the model and the simulation results of IPOSIM can also show that the proposed model has a certain degree of reliability.

Chapter 7 Conclusions and Future Work

7.1 Conclusions

When multiple power modules or semiconductor devices in a power converter system are in the process of thermal transfer, there is a thermal coupling effect between adjacent devices. In this project, semiconductor devices/modules in power converters are the main research objects, and the thermal coupling effect and variable thermal resistances are analyzed and studied.

(1) The thermal transfer mechanism of power devices is summarized. Based on the traditional thermal resistance network models, the reasons for thermal transfer and thermal conduction coupling effect are analyzed and summarized. The calculation methods of the junction temperature of semiconductor devices with different models are given.

(2) Based on the analysis of the influence of conduction thermal coupling and convection thermal coupling on the case/junction temperature of adjacent devices, the thermal coupling effect is studied. The thermal coupling testing platform of adjacent semiconductor devices is established. Based on the requirements of case temperature controlling of power converter system, a TCRN model is proposed from the point of view of power converter design stage and under the premise of fixed case temperature/value range. Moreover, the relationships between the case-to-ambient thermal resistance and thermal coupling resistances under different working conditions are analyzed, and the thermal coupling effect between adjacent devices under different working conditions is obtained. Finally, a new thermal coupling measurement platform is established, and the results of the fitting calculation are compared with the measured device case temperature. The comparison results verify the feasibility and effectiveness of the proposed calculation method.

(3) Based on the existing models, the electrical thermal simulation model of the power converter system is established by PLECS software to analyze the junction temperature rise of the power devices under different working conditions. The comparison of junction

temperature rise shows the influence of the conduction thermal coupling effect on the junction temperature of semiconductor devices.

(4) In view of the fact that the traditional thermal analysis model often ignores the convection thermal coupling effect, the convection thermal coupling testing platform of semiconductor devices is established, and the device case temperature under different working conditions is obtained. Based on the experimental data, a multivariable thermal resistance network model considering the convection thermal coupling effect of adjacent devices is proposed, and the relationships between thermal coupling resistance and its influencing factors is analyzed. Finally, the case temperature of the devices measured under the new device spacing is compared with that obtained by fitting calculation to verify the correctness of the model and the proposed relationships.

(5) In view of the dependence of the convection thermal dissipation of the device itself and the convection thermal coupling effect between adjacent devices on the surrounding air region, a FEM simulation model of convection thermal coupling of adjacent devices at different ambient temperatures is established. By changing the environmental temperature profiles, the temperature distribution, isosurface distribution, and junction temperature of the devices under different ambient temperatures are obtained, and the relationships between junction temperature and ambient temperature are deduced. The relationships are verified by the junction temperature of the device at the new ambient temperatures. The junction temperatures of the device at other ambient temperatures can be calculated by the proposed relationship.

(6) IGBT module and motor power converter (three-phase inverter) are taken as the research object, and based on the traditional IGBT thermal model, the conduction thermal coupling analysis model of adjacent IGBT modules is established, and the calculation formulas of self- thermal resistance and conduction coupling thermal resistance are obtained, and the junction temperature calculation formula is deduced. In order to verify the correctness of the model, the online simulation software provided by Infineon company is applied to calculate the junction temperature of three-phase motor inverter. The comparison results

show that the model established has good accuracy.

7.2 Contributions

(1) According to the requirement of a power converter for the uniformity of thermal distribution, a calculation method of thermal coupling effect (including conduction and convection thermal coupling effect) between power devices is proposed based on the premise of considering the fixed device case temperature. The TCRN model is established and relationships between the variable thermal resistances (including self-resistance and thermal coupling resistances) between adjacent devices under different conditions is analyzed.

(2) In view of the fact that convection thermal coupling effect is ignored in the existing thermal analysis calculation models of semiconductor devices, a multivariable thermal resistance network model considering convection thermal coupling effect between adjacent semiconductor devices is established.

(3) A FEM simulation model of convection thermal coupling of adjacent devices considering different ambient temperatures is established.

(4) The conduction thermal coupling resistance network model of the power modules is established, and the junction temperature calculation formula of the module is deduced. Compared with the traditional module thermal analysis and junction temperature calculation model, the model realizes the conduction thermal coupling of multiple modules in the converter system.

7.3 Future Work

In this paper, the thermal coupling effect of semiconductor devices/modules is studied, while the following aspects need to be further studied.

(1) Compared with the traditional models, the proposed thermal coupling resistance network model of adjacent semiconductor devices adds the convection thermal coupling effect between devices. While the model established in this paper is based on the ideal device loss model. In practical application, the electrical parameters of semiconductor devices will

change with the change of junction temperature, and when the electrical parameters change, the device loss will also have a change. Therefore, the next step is to consider the real-time feedback between the device loss and the device junction temperature/case temperature and establish the electrical thermal coupling model between the device loss and the device case temperature.

(2) The case-to-ambient thermal resistance and convection thermal coupling resistance are dependent on the ambient temperature, while the simulation model established in Chapter 5 is focus on a series of ambient temperatures and does not consider a dynamic ambient temperature variation condition. The next step is to analyze the influence of dynamic ambient temperature on the thermal coupling effect between adjacent power devices.

(3) In chapter 6, the conduction thermal coupling resistance network model, which takes the IGBT module as a whole, which does not calculate the thermal coupling between the chips in the module. In order to get a more accurate junction temperature calculation model, the thermal coupling effect between chips should be considered in the next step.

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