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Analysis and Design of Single-Phase Transformerless Inverter for Photovoltaic Applications

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Certificate of Original Authorship

I, Md Noman Habib Khan declare that this thesis is submitted in fulfilment of the requirements for the award of Doctor of Philosophy in the School of Electrical and Data Engineering at the University of Technology Sydney.

This thesis is wholly my own work unless otherwise reference or acknowledged. In addition, I certify that all information sources and literature used are indicated in the thesis.

This document has not been submitted for qualifications at any other academic institution.

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[6] **Md Noman H. Khan,** M. Forouzesh, Yam P. Siwakoti, L. Li, T. Kerekes, and F. Blaabjerg, " A Classification of Single-Phase Transformerless Inverter Topologies for Photovoltaic Applications." *in proc. IEEE Region 10 Symposium (TENSYMP),* Sydney, Apr. 2018, pp. 174-179. doi: 10.1109/TENCONSpring.2018.8692013.

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[11] S. A. Khan, **N. H. Khan,** Y. Guo, Yam P. Siwakoti, J. Zhu, and F. Blaabjerg "A Step up Three-Phase Seven-Level Switched Capacitor Inverter for grid-tied Photovoltaic Application." *in proc. IEEE Energy Conversion Congress and Exposition (ECCE)-Asia,* 2020. (Accepted)

Abtract

This thesis provides a comprehensive analysis of different transformerless inverter topologies (TLIs) and their control and modulation techniques. Considering the challenges and merits of the transformerless inverter, four different types of transformerless inverter topologies for PV applications have been investigated, analysed and designed in this thesis.

The first topology is H-bridge Zero Voltage Switch Controlled Rectifier (HB-ZVSCR) transformerless mid-point-clamped inverter. The operating principle and CM effect of the proposed topology are analysed and compared with the conventional topologies. This is followed by the thermal analysis and loss calculation which shows better efficiency over the conventional topologies. Validation is carried out using MATLAB-Simulink using the PLECS toolbox followed by a scale-down prototype of 1.5 kW.

The second topology is a single-phase switched-capacitor (SC) based (2n+1)-level inverter with reduced number of components and input DC voltage supply magnitude. The total number of output voltage levels can reach up to (2n+ 1) levels, where $n \geq 2$ is the number of switching cells consisting of three power switches and two switched-capacitors. The operating principle is presented in detail followed by comparative analysis, thermal modelling and design guidelines. Finally, measurement results are carried out for a 5-level inverter with two SC cells as an example to verify the performance of the proposed (2n+1)-level inverter over different operating conditions.

The third topology is a novel dual-mode five-level common grounded type (5L-DM-CGT) transformerless inverter topology for a medium-power application with a wide input voltage range (200 V – 400 V). The theoretical analysis shows the advantages of the dual-mode inverter for various industrial applications. Finally, the laboratory test results are presented to verify the theoretical analysis.

The final topology is a novel configuration of switched capacitor multilevel inverters (SCMLIs) with a lower number of power components with inherent voltage boost. The

proposed topology is compared with other existing five-level inverter topologies to show its superior capabilities/advantages. The performance of the proposed topology is validated by OPAL-RT.

Overall, this thesis provides a comprehensive analysis of all transformerless inverter topologies and their control and modulation techniques and come up with the concept of new single-phase transformerless inverter topologies. The new topologies utilizes minimal components with low voltage stress and offers high power quality output with low total harmonic distortion (THD), high efficiency and power density, low cost and size, and simple modulation techniques.

Keywords: Solar Photovoltaic (PV); Thermal Modelling; Switched Capacitor Converter, Common Mode Voltage; Leakage Current; Multilevel Converter; Quasi Resonant Charging.

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Abbreviations

AC	=	Alternative Current
ANPC	=	Active Neutral Point Clamped
B-ANPC	=	Boost-Active Neutral Point Clamped
CEC	=	California Energy Commission
CGT	=	Common Ground Type
CHB	=	Cascaded H-Bridge
CM	=	Common Mode
CMV	=	Common Mode Voltage
CL	=	Conduction Loss
CSI	=	Current source Inverter
DBFBI	=	Dual Buck Full bridge Inverter
DC	=	Direct Current
DMV	=	Differential Mode Voltage
DSP	=	Digital Signal Controller
EMI	=	Electro Magnetic Interference
EVA	=	Ethylene-Vinyl Acetate
EU	=	European
ESR	=	Equivalent Series Resistances
EVs	=	Electric Vehicles
F-B	=	Full-Bridge
FC	=	Flying Capacitor
FPGA	=	Field Programmable Gate Array
GW	=	Giga Watt
HB-ZVR	=	H-Bridge Zero Voltage Rectifier
HB-ZVR-D	=	H-Bridge Zero Voltage Rectifier-Diode
HB-ZVSCR	=	H-Bridge Zero Voltage Switch controlled Rectifier
HERIC	=	Highly Efficient and Reliable Inverter Concept
HF	=	High Frequency
IEA-PVPS	=	International Energy Agency Photovoltaic Power Systems Program
IGBT	=	Insulated Gate Bipolar Transistor
LF	=	Low Frequency
LS-SPWM	=	Level-Shifted Sinusoidal Pulse Width Modulation
MMC	=	Modular Multilevel Converter
MOSFET	=	Metal Oxide Field Effect Transistor
MPC	=	Model Predictive Controller
MPP	=	Maximum Power Point
MPPT	=	Maximum Power Point Tracker
MW	=	Mega Watt
NI	=	National Instrument

NPC	=	Neutral Point Clamped
PCB	=	Printed Circuit Board
PF	=	Power Factor
PN-NPC	=	Positive Negative- Neutral Point Clamped
PWM	=	Pulse Width Modulation
PV	=	Photovoltaic
QSC	=	Quasi Resonant Charging
RES	=	Renewable Energy System
RMS	=	Root Mean Square
RTP	=	Reactive Power Capability
SC	=	Switched-Capacitor
SD-DBFBI	=	Series-Diode-Dual Buck Full bridge Inverter
SL	=	Switching Loss
SPWM	=	Sinusoidal Pulse Width Modulation
SS-DBFBI	=	Series-Switch-Dual Buck Full bridge Inverter
T-type	=	Transistor-type
TSV	=	Total Standing Voltage
THD	=	Total Harmonic Distortion
U-SPWM	=	Unipolar- Sinusoidal Pulse Width Modulation
VA	=	Volt-Ampere
VSI	=	Voltage Source Inverter
WTs	=	Wind Turbines

Nomenclature

η	=	Efficiency
η_{EU}	=	European Efficiency, weighted
η_{CEC}	=	California Energy Commission Efficiency, weighted
V_{in}	=	Input Voltage
V_{dc}/V_{PN}	=	DC Link Voltage
V_{AB}	=	Inverter Voltage
$(C = 2\times C_1)$ & $(C_1 = C_2)$	=	DC Link Capacitor
i_{cm}	=	Leakage Current
S_B	=	Boost Switch
D_B	=	Boost Diode
D_{DB}	=	Boost Duty Cycle
L_B	=	Boost Inductor
V_{ECM}	=	Equivalent Common Mode Voltage
I_F	=	Forward Current
V_F	=	Forward Voltage
I_{PRR}	=	Peak Reverse Recovery Current
I_{ce}	=	Instantaneous Current
C_{in}	=	Input Capacitor
C_F	=	Flying Capacitor
L_m	=	Flying Inductor
CS	=	Switched Capacitor
v_g or v_{out}	=	Output Voltage
f_g or f_m	=	Line Frequency
f_{sw}	=	Switching Frequency
i_o or i_{out}	=	Output Current
M	=	Modulation Index
P_o	=	Rated Power
L_r	=	Resonant Inductor
ω_s	=	Angular Frequency
ω_r	=	Voltage Factor Coefficient of Switched Capacitor
T_S	=	Sampling Period
C_o or C_f	=	Filter Capacitor
N_S	=	Number of Switches
N_D	=	Number of Diodes
N_L	=	Number of Voltage Levels
PT_S	=	Prototype Size
C_T	=	Total Cost

FC_{Loss}	=	Flying Capacitor Losses
F_{Loss}	=	Filter Losses
L_1, L_2, L_f	=	Filter Inductor
L_r	=	Quasi-Resonant Inductor
τ	=	Time Constant
R	=	Resistive Load
R-L	=	Resistive-Inductive Load
C_{pv1}, C_{pv2}	=	Parasitic Capacitor
R_{sig} or - R_{sig}	=	Reference Signal
C_{sig} or - C_{sig}	=	Carrier Signal
A	=	Reference Amplitude
N	=	Carrier Amplitude
Q_N or Q_{SC}	=	Capacitor Discharging Value
ω_g	=	Angular Frequency
φ_{pf}	=	Power Factor
ΔI_{Factor}	=	Current Ripple Factor
ΔI_{in}	=	Input Current Ripple
T_J	=	Junction Temperature
ΔT_j	=	Avarage Junction Temperature
T_C	=	Case Temperature
T_A	=	Ambient Temperature
T_H	=	Heat Sink Temperature
Z_{C2}	=	Impedance of DC-link Capacitor (C_2)
Z_{CPV}	=	Impedance of Parasitic Capacitor
Z_{L1} or Z_{L2}	=	Impedance of Filter Inductor
R_G	=	Ground Resistor
$Z_{(J-C)}$	=	Thermal Impedance (Junction to Ambient)
$Z_{(C-H)}$	=	Thermal Impedance (Case to Ambient)
$Z_{(H-A)}$	=	Thermal Impedance (Heat Sink to Ambient)
P_{L_D}	=	Diode Power Loss
P_{L_M}	=	MOSFET Power Loss
P_{L_PD}	=	Anti-Parallel Diode of the MOSFET Power Loss
R_{Mb}	=	Magnetic Resistance for Winding W_1
R_{Mf}	=	Magnetic Resistance for Winding W_2
R_{Cb}	=	Magnetic Core Elements for Winding W_1
R_{Cf}	=	Magnetic Core Elements for Winding W_2
R_{C1}	=	Core Loss Resistance for Winding W_1
R_{C2}	=	Core Loss Resistance for Winding W_2
M_{Cb}	=	Magnetic Core Elements for Winding W_1
M_{Cf}	=	Magnetic Core Elements for Winding W_2

Chapter 1

Introduction

1.1. Background

The renewable energy sources (RESs) demand to produce electricity over the past few decades are dramatically escalated as it has eliminated the use of fossil fuel. Electricity penetrates its tentacles deep into every sector, especially in the academic and industrial sectors. Among different RESs, wind turbines (WTs), and photovoltaic (PV) systems fulfil the maximum demand in electricity production. Hence, these two types of RESs are forecasted to have important impacts on the supply side of the distribution networks for the future [1] - [3].

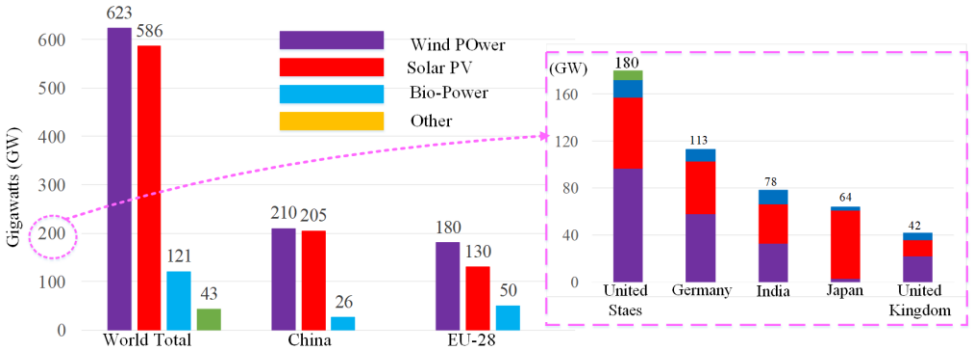


Fig. 1.1. Renewable power capacities in world, EU-28, and top six countries, 2019 [2] and [3].

According to the global energy status report - REN21 and global energy review 2020, the total worldwide renewable power capabilities have reached 1,373 gigawatts (GW) by 2019, where China produces one-third of the total production (see Fig. 1.1). Fig. 1.2 shows the production of electricity through wind and solar PV by 2019 [2] in EU-28 countries. Both methods can reduce pollution and have minimal operational costs. Due to easy availability and operation handling, solar PV is getting more attacractive worldwide [1] - [3].

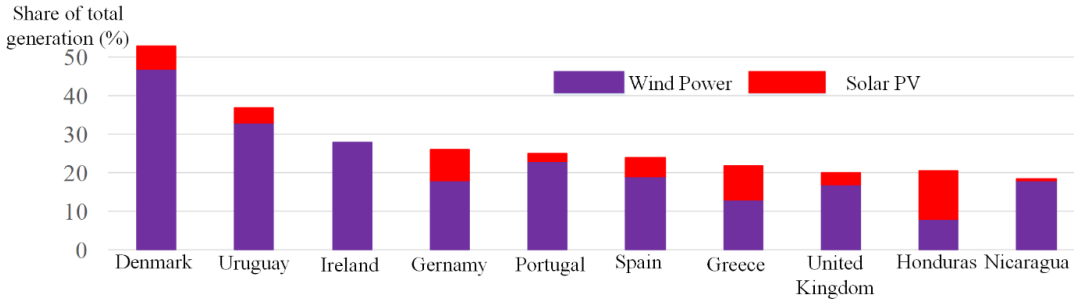


Fig. 1.2. Wind and PV power capacities in different countries by 2019 [2] and [3].

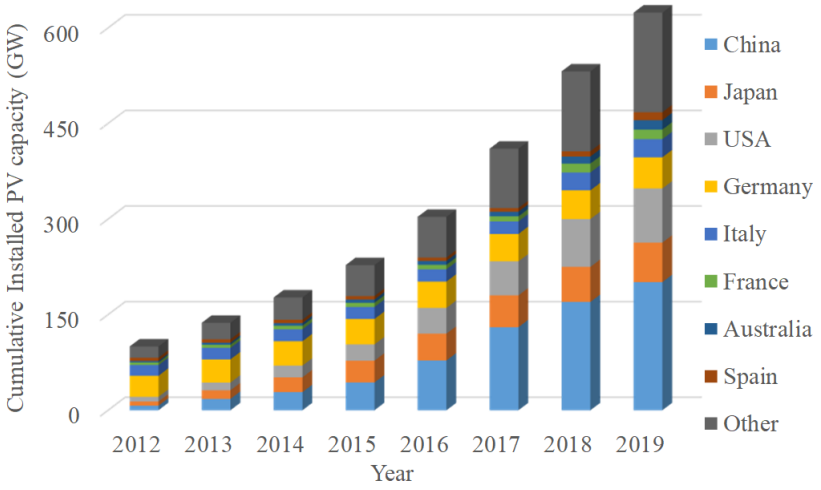


Fig. 1.3. Cumulative PV installations for the top IEA-PVPS countries from 2012 to 2019 [2].

With technological advancements in material and manufacturing techniques, the cost of the PV system is continuously reduced, making it the cheapest energy source for massive deployment in the future. Many countries (USA, Germany, China, Japan, Australia, France, Italy, Spain, etc.) have already begun to reap the benefits through their increased adoption and integration of this system in the utility grid. According to the 2017 annual report of the International Energy Agency-Photovoltaic Power Systems Program (IEA-PVPS) [2], the

global installed PV capacity reached a 100 GW milestone in 2012, and a 200 GW level in 2015. By the end of 2019, the total installed PV capacity was estimated to be roughly 627 GW, while 24 IEA-PVPS countries reached 300 GW [2]. Fig. 1.3 shows the cumulative installed PV capacity of the top IEA-PVPS countries from 2012 to 2019. From this figure, it is evident that the PV industry is facing rapid growth with five leading countries representing 93% of all PV installations in 2019. Among them, China, USA, and Japan experienced the largest installed PV installation capacity increment in recent years.

Among all PV installations, the percentage of off-grid PV systems is very low [3]. The grid-connected PV systems need power inverters as interfaces between the PV panel and the grid, and these are generally categorised as galvanic isolated inverters and non-isolated inverters. In the isolated type, usually a high-frequency DC side transformer or a low-frequency AC side transformer is used to achieve galvanic isolation and this serves to enhance the overall system safety. Due to their lower cost, size/weight, and higher efficiency, transformerless inverters have generated a high degree of interest in terms of residential market with low to medium power capacity [4]-[8].

1.2. Transformerless PV Inverter Topology

Fig. 1.4 illustrates a general layout for a single-phase transformerless inverter for small-scale PV systems. As can be seen, without a galvanic isolation, a direct ground-current path may form between the PV panel and the grid. Due to the presence of large stray capacitance (C_{PV}) between the PV and grid grounds, the varying voltage (also known as common-mode (CM) voltage) can excite the resonant circuit formed by the parasitic capacitor and inverter filter inductor and this produces a high CM ground current i_{cm}. This capacitive i_{cm} comprises line low-frequency and switching high-frequency components which inject harmonics into the grid current, increase the system losses, impair the electromagnetic compatibility, and can cause safety problems such as electric shock [9]-[15].

In order to understand the grid-connected PV systems to satisfy various grid codes and their safety standards, numerous inverter related issues have been thoroughly investigated [16]-[28]. So far, many transformerless inverter topologies have been presented with the aim

of eliminating the leakage current. To achieve this, various decoupling techniques have been adopted, such as, decoupling the DC from the AC side [29]-[36] and/or clamping the common mode voltage (CMV) during the freewheeling period [9], [10], and [37]-[41], or using common ground configurations [5], [12], [16], and [42]-[45].

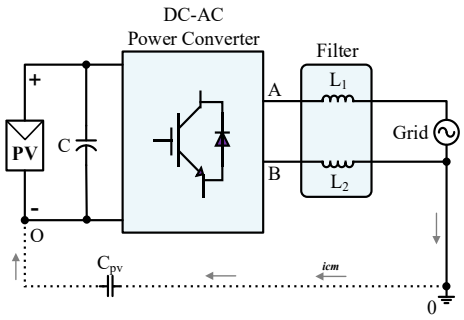


Fig. 1.4. The general layout of a single-phase transformerless inverter using an L-filter.

1.3. Requirements and Issues in Relation to Transformerless PV Inverters

Grid-connected PV systems need special attention in order to satisfy grid codes and standards. Hence, international agencies have regulated some broadly accepted standards for PV systems, which are required in order to avoid safety issues.

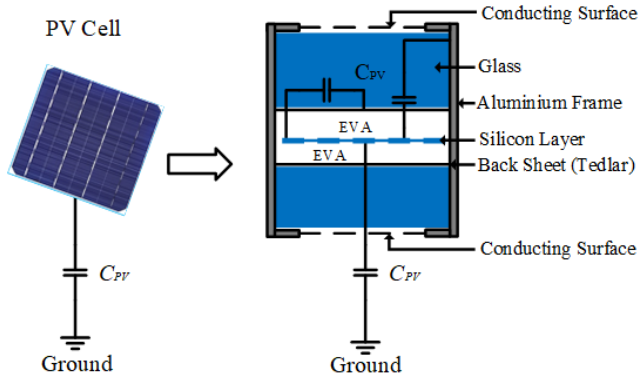


Fig. 1.5. Parasitic capacitance in PV panels [28].

The major cause of these safety issues and concerns is the presence of the ground capacitance C_{PV} between the PV cells/panel and the ground, as illustrated in Fig. 1.5. PV panels are comprised of the combination of glass, Ethylene-Vinyl Acetate (EVA), a back

sheet (Tedlar), and an aluminium frame, in which C_{PV} is created from the PV cell to the frame, the rack, and the ground.

Moreover, in the transformerless PV inverter, a CM resonant circuit can be created between the parasitic capacitor of the PV module and the output filter inductors at the grid side, which can cause severe issues such as high ground current i_{cm} and its subsequent problems [7], [46]. Furthermore, the output filter, which forms a resonant circuit with the power switching circuit plays a major role in ground leakage current. This is very important to understand the CM behaviour of the transformerless system. The following sub-sections provide a brief explanation on the CM behaviour of the circuit and its ground leakage current, followed by different grid codes as well as safety requirements.

1.3.1. Common-Mode Resonant Circuit and Leakage Current Issues

The amplitude and spectrum of leakage current depends mainly on the converter circuit topology, modulation strategy and the resonant circuit formed by the ground capacitor, the converter, the output AC filter and the grid. Fig. 1.6(a) shows the CM equivalent circuit of the inverter which is comprised of the converter, filter inductors (L_1, L_2), and parasitic capacitor (C_{pv}). The power circuit in Fig. 1.6(a) can be replaced with phase voltages of the inverter V_{AO} and V_{BO} which are equal to the potential of A and B points relative to the neural point O (see Fig. 1.6(b)) [29], and [47]-[48]. The CMV and differential-mode voltage (DMV) can be written based on the phase voltages as follows:

$$V_{cm} = \frac{V_{AO} + V_{BO}}{2} \tag{1}$$

$$V_{DM} = V_{AO} - V_{BO} \tag{2}$$

Moreover, the phase voltages can be expressed based on V_{cm} and V_{DM} as mentioned in (3) and (4).

$$V_{AO} = V_{cm} + \frac{V_{DM}}{2} \tag{3}$$

$$V_{BO} = V_{cm} - \frac{V_{DM}}{2} \tag{4}$$

To better understand the CM behaviour, the equivalent circuit can be simplified into a single loop circuit as shown in Fig. 1.7(a). The equivalent CMV (V_{ECM}) shown in this figure can be obtained as

$$V_{ECM} = V_{cm} + \frac{V_{DM}}{2}\frac{L_2 - L_1}{L_1 + L_2} \tag{5}$$

The magnitude of i_{cm} depends mainly on the amount of parasitic capacitance and the amplitude and frequency of the CMV, whose fluctuation can produce a large i_{cm}. To avoid the leakage current i_{cm}, (5) should be equal to zero, which is dependent on the circuit topology. Moreover, the equivalent CMV has to remain constant in each switching period in order to reduce i_{cm}.

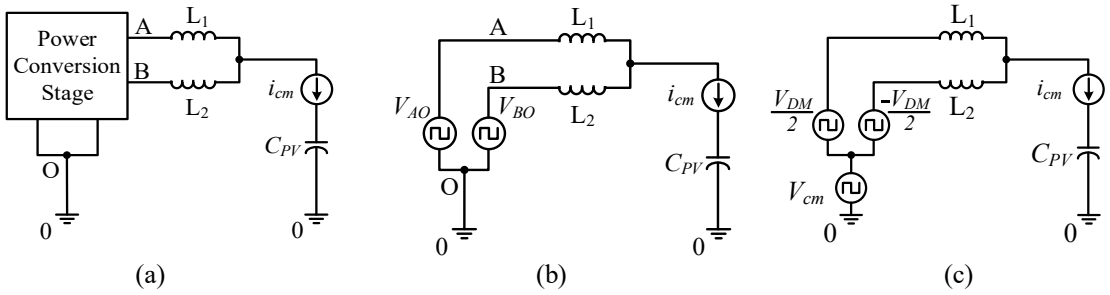


Fig. 1.6. CM model showing (a) the resonant circuit, and (b) the resonant circuit including V_{AO} and $V_{BO,}$ (c) the resonant circuit including CMV.

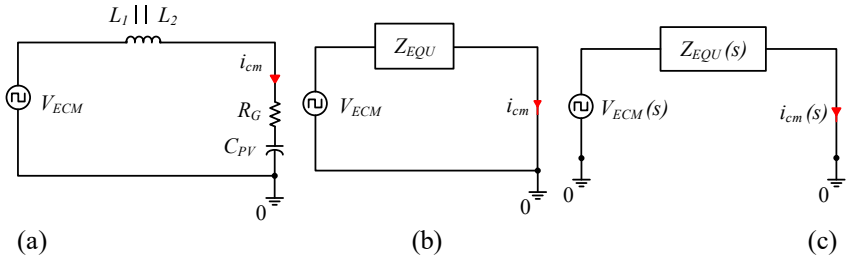


Fig. 1.7. Simplified single loop CM model, (a) considering the series connection of components, (b) the equivalent impedance circuit, and (c) the *s*-domain equivalent circuit.

The effect of DMV can be eliminated in symmetrical topologies like H-bridge inverter by using two identical inductor filters at the output (i.e., $L_1 = L_2$) [29], and [47]-[49]. The

simplified equivalent CM circuit including the equivalent impedance (Z_{EQU}) is shown in Fig. 1.7(b).

This circuit can be demonstrated in the s-domain to analyse the frequency and magnitude of the created resonant circuit (see Fig. 1.7(c)) [10]. Letting $L_1 = L_2$ in (5) for the topologies with a symmetrical structure (e.g. H-bridge), the equivalent CMV can be replaced with V_{cm}. The transfer function from i_{cm} to CMV created by the converter through the resonant circuit can be expressed as (7).

In (6) and (7), $L = (L_1 L_2)/(L_1 + L_2)$. Fig. 1.8 illustrates the Bode plot of (7) considering $L_1 = L_2$ =3 mH and C_{PV} =75 nF.

$$V_{ECM}(s) - \left(Ls + \frac{1}{sC_{PV}}\right) i_{cm}(s) = 0 \tag{6}$$

$$H(s) = \frac{i_{cm}(s)}{V_{ECM}(s)} = \frac{s}{Ls^2 + \frac{1}{C_{PV}}} \tag{7}$$

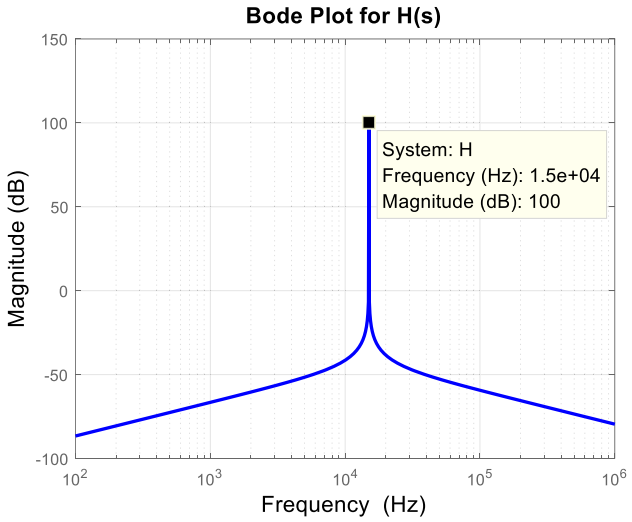


Fig. 1.8. Bode plot of the resonant circuit model in Fig. 1.7.

It is evident that the resonant frequency equals 15 kHz. Moreover, as the filter inductor and parasitic capacitor forms a typical LC resonant circuit, its resonant frequency can be calculated theoretically from (8). Both the simulation and analytical results show the same resonant frequency whereby a large CM current i_{cm} flows into the system.

$$f_r = \frac{1}{2\pi\sqrt{LC_{PV}}} = 15005 \text{ Hz} \quad (8)$$

Without a galvanic isolation, the potential between the PV array and the ground (V_{ECM}) fluctuates which charges and discharges the parasitic capacitor (C_{pv}). This fluctuating CMV activates the resonant circuit, as discussed above, and may lead to a higher ground leakage current. However, the resonant frequency is not fixed, as it depends on the parasitic capacitance together with the DC lines that connect the PV array to the inverter. It also depends on the size of the PV array and the environmental conditions. All these conditions make the elimination of leakage current more difficult in practice [50].

1.3.2. Grid Requirements and Standards

The grid-connected PV systems should comply with some standards that are regulated internationally as well as by each country. In this subsection, a brief overview of different grid codes is demonstrated for grid-connected PV systems, while a more detailed investigation can be found in [51]. Table 1.1 illustrates important required grid codes regulated by major countries and associations. When a PV panel is connected to the grid, different parameters need to be taken care of in order to achieve an acceptable performance level. The major ones are as follows: total harmonic distortion (THD), injected DC current, grid frequency (f_g) range, power factor and i_{cm} range. In most PV standards, the maximum allowable THD of the output current is limited to 5% which is the reason for improved power quality at the distribution feeders. On the other hand, the amounts of injected DC current to the PV system are invariably limited to within 0.22% - 1% of the rated output current. This current is difficult to measure precisely through the means of the existing inverter circuits. The range of grid frequency is provided in Table 1.1 for the different standards. However, the standard frequency range may fluctuate more for varying abnormal conditions [17]-[25], [27].

VDE 0126-1-1 specifies the acceptable range of i_{cm} that should not be more than 100 mA when the fault discontinuity time is not more than 40 ms [55]-[56], as shown in Table 1.2.

Table 1.1. Grid connected PV system standards and grid codes [15]-[23], [26], and [35]-[37]

Standard No.	Publication Origin	THD	DC Current Injected	Grid Frequency (f_g) Range (Hz)	Power Factor
IEEE 1547 [17]	USA (IEEE)	Less than 5%	<0.5% of rated output current	57 ~ 60.5	0.9 to 0.97
IEEE 929-2000 [20]	USA (IEEE)	Less than 5%	<0.5% of rated output current	59.3 ~ 60.5	> 0.85
IEC 61727 [28]	Swiss (IEC)	Less than 5%	< 1% of rated output current	49 ~ 51	> 0.90
AS4777 [52]-[54]	Australia	Less than 5%	0.5% of rated output current per phase	48 ~ 52	0.8 to 0.95
EN 61000-3-2 [22]	England	Less than 5%	< 0.22A corresponding to a 50 W half-wave rectifier	47.5 ~ 50.2	NA
EREC G83 [21]	England	Less than 5%	0.25 % of AC current rating per phase	49 ~ 51	0.95
VDE 4105 [18]	Germany	Less than 5%	< 1 A; max. trip time 0.2 s	47.5 ~ 51.5	0.89 to 0.95
BDEW [23]	Germany	Less than 5%	NA	47.5 ~ 51.5 (-5% ~ +3%)	0.95
GB/T 19964-2012 [24]	China	Less than 5%	< 1% of rated output current	48-50.5	0.95
JEAC 9701-2012 [25]	Japan	Less than 5%	NA	47.5 ~ 51.5 (Eastern Japan) 57 ~ 61.8 (Western Japan)	0.9 to 0.95

Table 1.2. Leakage current with discontinuity time in VDE 0126-1-1

Leakage Current (mA)	Fault Discontinuity time (ms)
30	300
60	150
100	40

Table 1.3. Voltage deviation in IEC 61727 and IEEE 1547-2008 [15], [17]

	10 kW (IEC 61727)		30 kW (IEEE 1547-2008)	
	Range (%)	Time (s)	Range (%)	Time (ms)
Voltage deviations	V < 50	0.1	V < 50	0.16
	50 ≤ V ≤ 88	2	50 ≤ V ≤ 88	2
	110 ≤ V ≤ 120	2	110 ≤ V ≤ 120	1
	V ≥ 120	0.05	V ≥ 120	0.16

Grid-connected systems must follow active and passive anti-islanding requirements due to the fluctuating voltage and frequency range according to IEEE 929-2000, IEEE-1547, VDE-AR-N 4105, and IEC 61727 standards [17]- [19], and [27] and most of the standards follow a limit in terms of voltage variations between 3% and 5% [19]- [21], and [25]. On the

other hand, voltage fluctuation must be kept within ±5% for standard IEEE 1547 [17]. Table 1.3 specifies the voltage deviation range.

1.4. Aims of the Project

1.4.1. Problem Formulation

The efficiency of commercial PV panels is around 23% which is increased to only 3% in last one decade. Therefore, it is very important that the power produced by these panels need to be used properly, by using efficient power converter systems. The efficiency and reliability of both single-phase and three phase PV inverter systems can be improved using transformerless topologies. However, additional care must be taken to avoid safety hazards such as ground fault currents and leakage currents, e.g. via the parasitic capacitor between the PV panel and ground. Therefore, the grid-connected transformerless PV inverters must comply with strict safety standards such as IEEE 1547.1, VDE0126-1-1, EN 50106, IEC61727, and AS/NZS 5033. Additionally power density, efficiency and reliability must be improved, whilst improving the termal management, semiconductor stress and power quality.

1.4.2. Objectives

The main goal of this project is to analyse and model the transformerless PV inverter systems. In particular, I have following objectives:

1. To explore the leakage current issue in the PV panel and investigate mitigation strategy that can follow the IEEE safety standard.
2. To develop an efficient mid-point clamped transformerless inverter topology with constant the Common Mode Voltage (CMV) during the whole (positive, negative and zero) period, whilst achieving relatively low THD at the output.
3. To investigate multilevel single phase transformerless inverter with reduced semiconductor devices and the magnitude of dc-link voltage.

4. To design a dual mode common grounded five-level transformerless invertir with wide input voltage range.
5. To design a soft-start and quasi-resonant charging capability based five-level transformerless inverter.
6. To investigate the model with reactive power capability and better dynamic response.

1.4.3. Limitations

The majority of PV inverters on the market include a boost stage in order to raise the low voltage of the PV array to the needed DC-link voltage of around 400V to achieve required 230 V AC output for single-phase system. During this research only single stage DC to AC topologies for single-phase grid connection has been studied with a power rating of maximum 1.5 kW. The PV array has been simplified by using a DC power source to rule out the need for a Maximum Power Point Tracker (MPPT), both in simulation and experimental tests. For simulation, the MATLAB/Simulink environment has been used together with the PLECS toolbox, to simulate power electronic circuits. All the active and passive components within the modelled electrical circuit were taken to be ideal.

1.5. Main Contributions

- ✓ Various single-phase transformerless inverter topologies are comprehensively reviewed and presented a critical analysis highlighting their pros and cons. Each topologies are simulated in details to analysis their CM effects and output power quality. A summary is presented to identify the best topology.
- ✓ Thermal modelling of major transformerless topologies for single-phase PV inverter topologies are studied in details to better understand the loss distribution.
- ✓ Proposed a high efficient single phase H-bridge zero-voltage switch controlled rectifier (HB-ZVSCR) to reduce the leakage current. Using a voltage clamping circuit, the AC terminal voltage is clamped to the DC midpoint (consisting of two DC-link capacitors) during the freewheeling period. As a result, the common mode voltage (CMV) is held constant which makes it suitable for the grid-connected PV system. Presented analysis,

simulation and measurement result shows a promising result to implement for low power single phase PV applications.

- ✓ Proposed a multilevel inverter with reduced number of semiconductor devices. The total number of output voltage level is up to (2n+ 1) levels, where $n \geq 2$ is the number of switching cell. Compared to conventional SC-based multilevel inverter topologies, the proposed topology features many advantages such as: (1) low number of semiconductor devices, (2) quasi-resonant charging of capacitors that reduce the inrush current and current stress on the devices, (3) self-balancing of capacitor, as they are charges in parallel and (4) reduced voltage stress on the switches.
- ✓ Proposed a dual mode common grounded five-level inverter topology with reduced number of semiconductor devices. It consists only eight power switches, a diode, and two switched-capacitors to develop five voltage levels. The proposed topology features many advantages when compared with various suggested single-phase five-level inverter topologies, namely scalability, utilization of a low number of semiconductors, low voltage stress, high efficiency and power density, low cost and size, and simple modulation control. Furthermore, the experimental waveforms of a 1 kVA prototype are presented to show the validity of the proposed inverter in both buck and boost modes. The measurement results show that the proposed inverter has the 97 ± 1 % efficiency over a wide range of loads with a peak efficiency of 98.96% at 130 W in buck mode and 99% at 122 W in boost mode.
- ✓ Proposed a soft-start and quasi-resonant charging for switched capacitor based five-level inverter topology. The new circuit consists of a single capacitor, an inductor, a diode, and seven active switching elements. Meanwhile, it offers a soft start and quasi-resonant charging capability, which can further improve the transient response and the inrush current profile of the system. To do so, proposed a pre-charge modulation process during the generation of output voltage levels in the zero and middle states of the positive half cycle. On the other hand, quasi-resonant charging for switched capacitor has done by making a charging operation of the switched capacitor at zero level of the output voltage through the resonant inductor. As a result, a RLC circuit is generated and the maximum steady-state charging current of switched capacitor can be limited to a

permissible range tolerable by the involved semiconductor devices. The theoretical analysis shows the advantages of the proposed inverter for both standalone and grid-tied applications. Finally, validated the proposed concept via OPAL-RT.

1.6. Outline of the Thesis

Chapter 1 ***(Introduction):*** This chapter focuses on the background and details explanation of transformerless PV inverter. A brief introduction of the parasitic capacitances with mathematical analysis of a common-mode circuit and leakage current is presented. This is followed by grid requirements and safety standards of major utility companies from around the world. Further, it details the aims, scope and research contributions of the thesis. The chapter conclude with the outline of the thesis.

Chapter 2 ***(Study of Various Transformerless Inverter Topologies):*** This chapter explores and classifies various transformerless inverter topologies based on various significant criteria and systematically reviewed different topologies. The operating principle and critical analysis based on the effect of CM for each topology are also presented. In this chapter, simulation has carried out to show the CMV and leakage current. Finally, the review work is summarized based on their CM effect, number of required components, power density, cost, and efficiency.

Chapter 3 ***(H-Bridge Zero-Voltage Switch Controlled Rectifier (HB-ZVSCR)):*** This chapter presents the HB-ZVSR topology with its operating principles, modulation strategies, CM effect, and component selection guidelines. Further, the thermal analysis showed for loss calculation and compared the proposed topology with selected topologies. This is followed by simulation and experimental results together for 1.5 kVA. Finally, a conclusion is made to summarize the findings and results.

Chapter 4 ***((2n+1)-Level Inverter):*** This chapter presents a (2n+1)-level inverter topology with its modulation strategy, and capacitor charging/discharging balance. The thermal analysis and the loss calculation has been done for electrical and magnetics components when n = 2. A comparison of the proposed inverter and other single input SC-based (2*n*+1)-level inverters is presented. Both simulation and experimental results of an

example five-level inverter are provided in parallel to verify the performance and show the accuracy of the design.

Chapter 5 ***(Dual Mode Common Grounded 5-Level Inverter):*** This chapter presents a dual mode common grounded five-level inverter topology with reduced number of semiconductor devices. The proposed structure analyses and developed a prototype for 1 kVA. The measurement results show that the proposed inverter has the 97 ± 1 % efficiency over a wide range of loads with a peak efficiency of 98.96% at 130 W in buck mode and 99% at 122 W in boost mode.

Chapter 6 ***(Soft Start and Quasi Resonant Charging Capability Based 5-Level Inverter):*** This chapter presents a soft-start and quasi-resonant charging capability based five-level inverter topology where it consists of a single capacitor, an inductor, a diode, and seven active switching elements. It consists of two parts, switched- capacitor (SC) network based on quasi

soft charging (QSC) at the front end to reduce the capacitor inrush current, and a 3-level full-bridge (FB) cell at the end to invert the DC to AC waveform. Soft-start is another advantage of the proposed 5L SC-based topology, which can be inherently provided by the start-up modulation process. Finally, the performance of the proposed topology and the validation of the concept will be validated through OPAL-RT.

Chapter 7 ***(Conclusion and Future Works):*** Some conclusions are shown in this chapter. It also highlights the major contribution of the thesis. Moreover, the end of this chapter identify some future direction and task.

Chapter 2

Study and Analysis of Various Transformerless PV Inverter Topologies

Voltage source inverters (VSIs) are favourable for PV applications due to cost, efficiency, and size over current source inverters (CSIs), and numerous voltage source single-phase transformerless topologies have been proposed and developed for grid-connected PV systems to improve the performance and compatibility to the grid codes [5], [7], [9], [12], [14], [15], [29], and [31]-[77].

Fig. 2.1 illustrates a classification of some of the important topologies in three major sub-groups based on the requirement for the DC-link voltage requirement, i.e., DC-link voltage ($2\times V_{PV}$), DC-link voltage (V_{PV}) and DC-link voltage ($\leq V_{PV}$) based single-phase transformerless inverters. Moreover, the single-input group can be categorised into four subgroups, based on i_{cm} suppression, decoupling and voltage clamping, i.e., common ground, H-bridge, H6, and buck-boost type topologies.

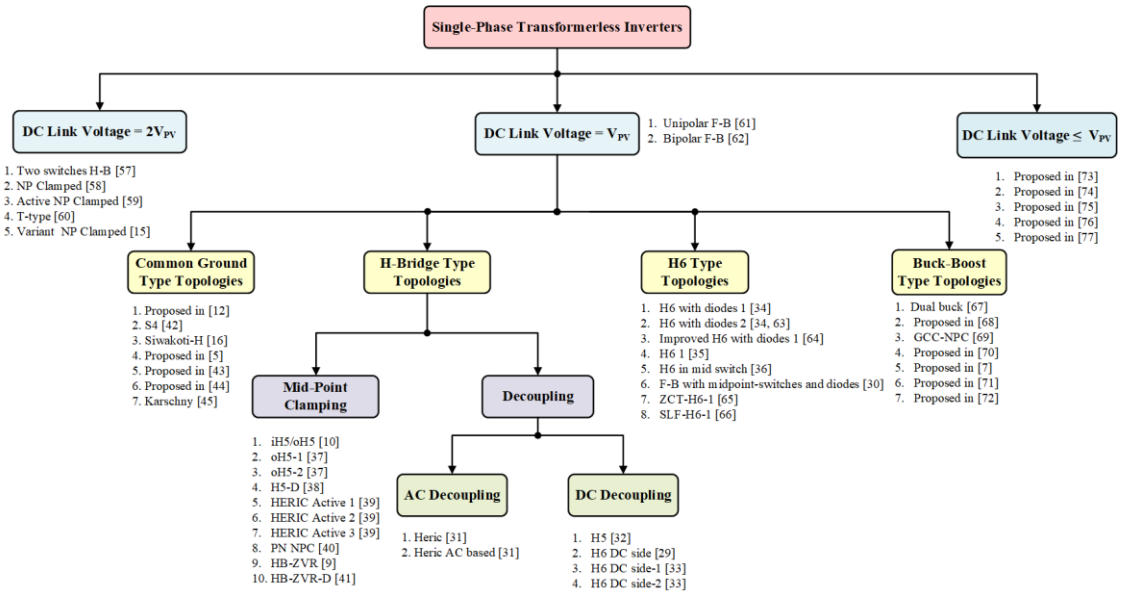


Fig. 2.1. Classification of single-phase transformerless inverter topologies used in PV systems according to DC-link voltage.

To shed more light on each topology considering the leakage current and CMV, the following sections provide analysis and simulation of some of the major topologies illustrating the key waveforms and CMV behaviour. Table 2.1 shows the parameters and values used for the simulations performed in this section and to benchmark the topologies. The voltage and current levels for the selected switches and diodes are 600 V and ~30 A, respectively. Moreover, all the components are chosen such that the best performance can be achieved. The inverters are operated for 1.8 kVA where the input voltage is selected as 400 V_{DC} to obtain 230 V_{ac} and the output current is achieved as ~ 7.35 A (RMS) [9], [35], [39], and [41].

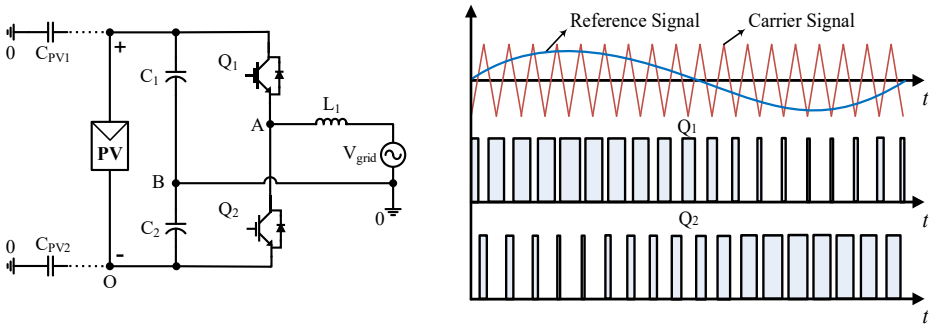
Table 2.1. Parameters Used for Simulations and comparisons

Parameter	**Value**
Input Voltage (V_{pv})	400 V_{DC}
Output Load	32 Ω
Output Voltage (V_g)	240 V_{ac}
Line Frequency (f_g)	50 Hz
Output Current (i_o)	7.35 A
Modulation Index (M)	0.82
Rated Power	1800 kVA
Switching Frequency (f_{sw})	20 kHz
DC Bus Capacitor ($C = 2\times C_1$) & ($C_1 = C_2$)	1600 µF

Flying Capacitor (C_F)	470 µF
Flying Inductor (L_m)	0.3 mH
Filter Capacitor (C_o)	2.2 µF
Filter Inductor (L_1, L_2)	3 mH
Parasitic Capacitor (C_{pv1}, C_{pv2})	75 nF
Switches (IKW30N60DTP)	V_{CE} = 600 V, I_C = 30 A
Diodes (APT15D60B)	V_F = 600 V, I_F = 32 A

2.1. Double Input Voltage ($2V_{PV}$) Type Single-Phase Transformerless Inverter Topologies

In this section, five single-inductor based transformerless inverters are introduced, where either $L_1 = 0$ or $L_2 = 0$ and the parasitic capacitance is 75 nF. The operational modes of each topology is discussed, as well as switching pulses and the output current describing the CM effect.



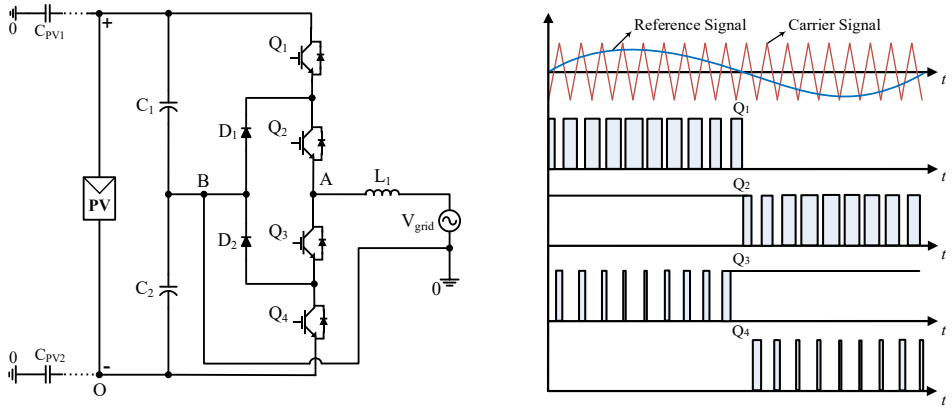
(a) (b)

Fig. 2.2. Illustration of (a) two switches H-B inverter, and (b) its switching pulses.

The two-switch based half-bridge (H-B) inverter works by alternatively switching pulses as shown in Fig. 2.2 (b), and the input voltage operates by charging and discharging the DC link capacitors (C_1 and C_2) (see Fig. 2.2 (a)) [78], which are shown to be more difficult in relation to achieving the maximum power point of the PV panel. Hence, the output current ripple is increased. To simplify the control system and improve the efficiency and current ripple, compared to two-switch based H-B [79], and [80], a new topology was introduced by A. Nabae, et al in 1981 [58] called the neutral point clamped (NPC). This topology which is well known for minimising the cost and size of the filter operates with three voltage levels

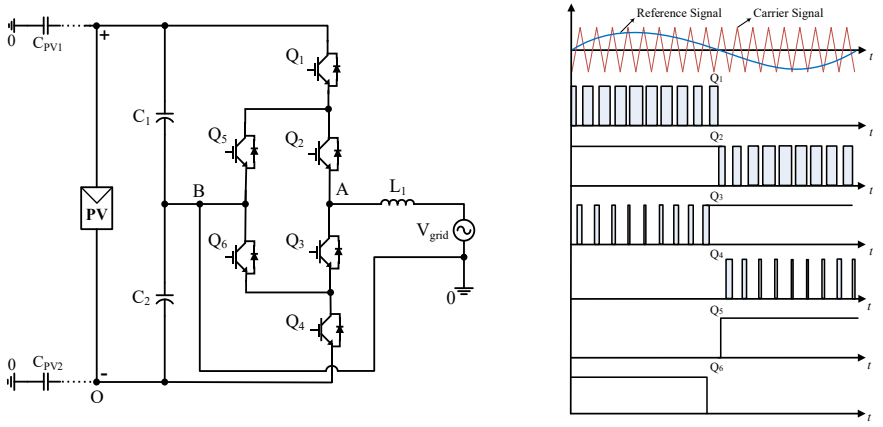
[81], and [82]. The zero voltage stage can be achieved by the clamping technique through the clamp diodes of the midpoint, as shown in the schematic diagram (see Fig. 2.3 (a)), and the modulation pulses are illustrated in Fig. 2.3 (b). However, the negative side of this topology is unbalanced conduction losses and a restricted DC link balance [83] which affects the whole system.

The active NPC (ANPC) is illustrated in Fig. 2.4 (a). This is a modification of the conventional NPC topologies [44], [84], and [85] and it mitigates the limitations of the NPC topology. In this topology, two switches Q_5 and Q_6 are used to replace the D_1 and D_2 diodes of the NPC.



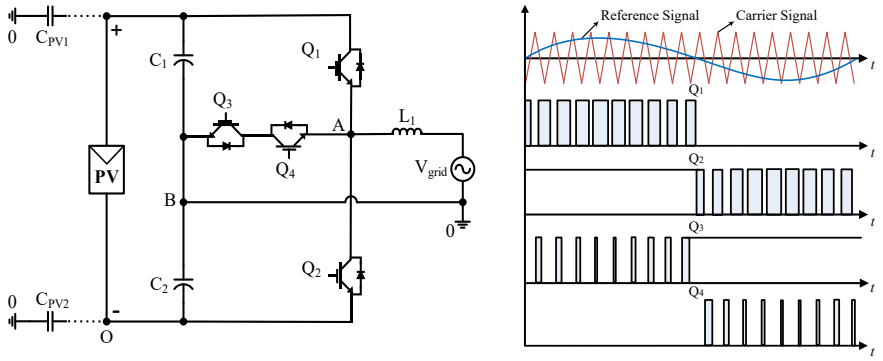
(a) (b)

Fig. 2.3. Illustration of (a) NPC H-B inverter, and (b) its switching pulses.



(a) (b)

Fig. 2.4. Illustration of (a) ANPC H-B, and (b) its switching pulses.

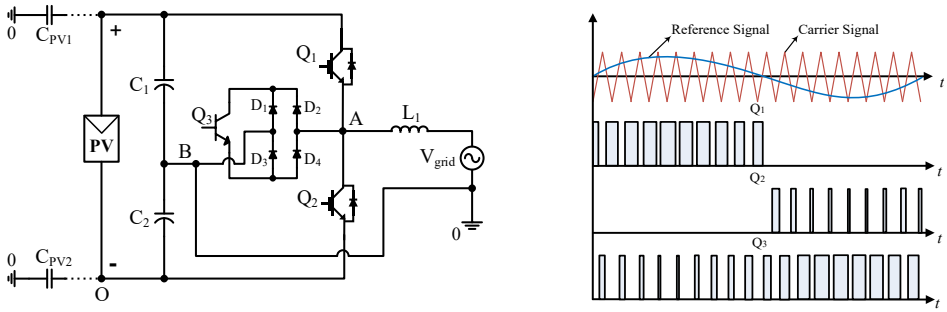


(a) (b)

Fig. 2.5. Illustration of (a) T-type H-B inverter, and (b) its switching pulses.

The upper clamping occurs when tuning on the switches Q_2 and Q_5, whereas the lower clamping works when Q_3 and Q_6 are operated [82]. After replacing the diodes with switches, the conduction losses can be controlled [54]. Fig. 2.4 (b) demonstrates the six switching pulses.

To reduce more conduction losses, the transistor (T)-type shown in Fig.2.5 (a) is a good solution with bidirectional switches which are inserted between the middle points of the DC-link capacitors and the Q_1-Q_2 branch [83], [86], and [87]. The switching pulses are presented in Fig. 2.5 (b) showing that the switches Q_1 and Q_3 work in a complementary fashion with switches Q_2 and Q_4 [88]. Moreover, the switching combination of the four switches is different when the midpoint clamping switches (Q_3 and Q_4) are selected for low switching losses and low forward voltage drops [83]. The T-type, NPC and ANPC topologies are also well known in five-level inverters for improving power quality and reducing complexity in high power applications [89]-[92]. They can also help to obtain a high conversion efficiency with low switching losses [92]-[94].



(a) (b)

Fig. 2.6. Illustration of (a) three-switch H-B inverter, and (b) its switching pulses.

Table 2.2. Summary of the Double Input Voltage Type Transformerless Inverters

Topology name	Semiconductor Devices				i_{cm} (mA)	Passive Filter Component		Voltage Level
	IGBTs		Diodes					
	No.	Voltage	No.	Voltage		No. of Inductor (L)	No. of Capacitor (C)	
Two-Switches based	2	$1.5\times V_{pv}$	0	---	≤ 2	1	0	2
NPC	4	$1.5\times V_{pv}$	2	$1.5\times V_{pv}$	≤ 3.5	1	0	3
ANPC	6	$1.5\times V_{pv}$	0	---	≤ 2.5	1	0	3
T-type	4	$1.5\times V_{pv}$	0	---	≤ 4	1	0	3
Variant NPC	3	$1.5\times V_{pv}$	4	$1.5\times V_{pv}$	≤ 4.2	1	0	3

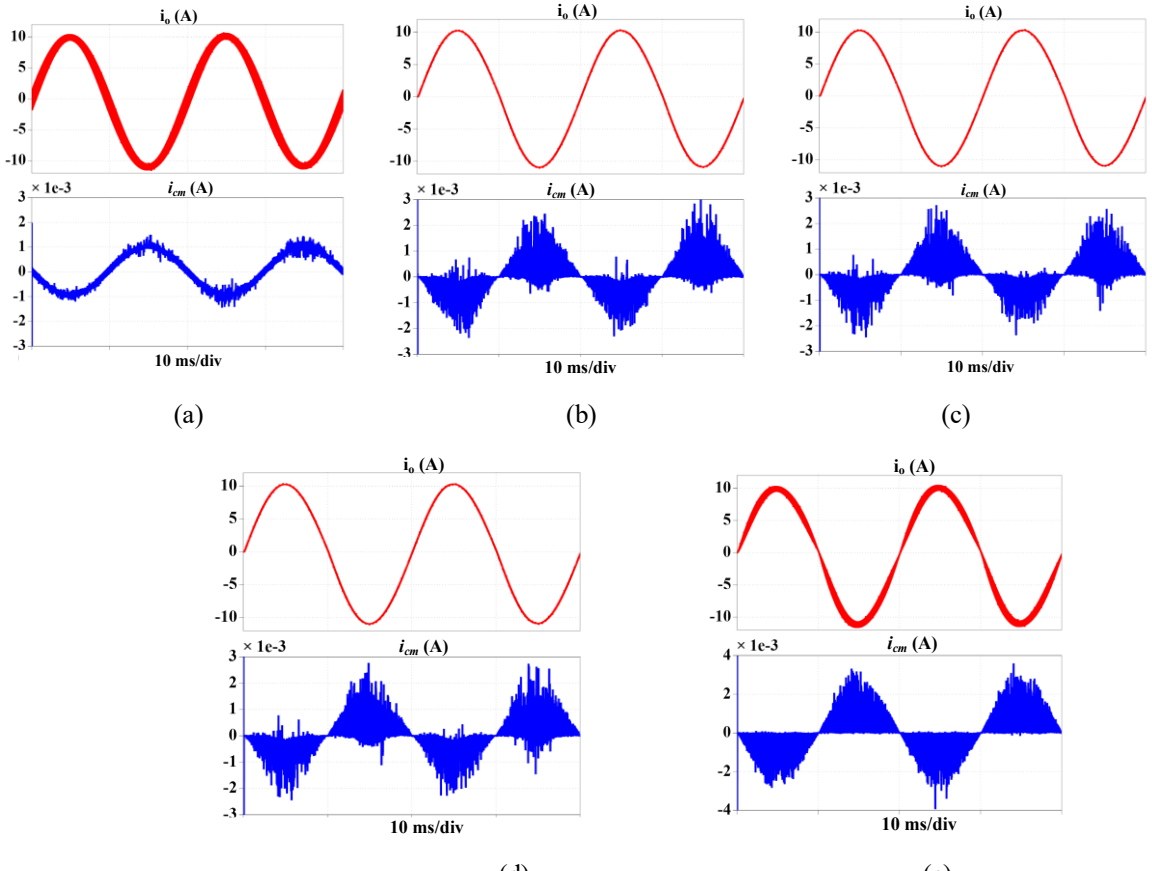


Fig. 2.7. Simulation results of (a) two-switch H-B inverter, (b) NPC inverter, (c) ANPC inverter, (d) T-type inverter and (e) variant NPC inverter.

A variant of the NPC is introduced in Fig. 2.6 (a) [15] to reduce the number of switches of the NPC/ANPC topologies. This topology uses a diode bridge with a bidirectional switch Q_3. The diodes are used for providing a current path during the null states, and the concept of

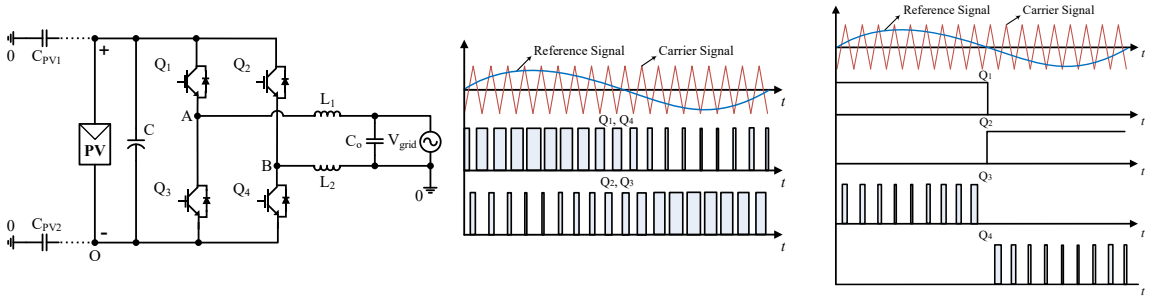
a bidirectional switch is taken from Conergy topology [88] by combining two bidirectional switches with one.

The variant NPC topology operates in four operational modes. In the positive half cycle, only Q_1 is in the ON condition, whereas in the negative half cycle, Q_2 is ON. In the freewheeling time of the positive half cycle, D_1 and D_4 are in forward bias mode with the switch Q_3; and in the negative cycle, the other two switches D_2 and D_3 are ON with the switch Q_3 [50]. Fig. 2.6 (b) shows the different switching pulses of the variant NPC.

The simulation results of the above topologies are shown in Fig. 2.7 (a) to Fig. 2.7 (e) where the input voltage is selected as $2\times V_{PV}$, and L_1 = 3 mH. Table 2.2 indicates the overall summary of the double-input voltage transformerless inverter topologies.

2.2. Single-Input Voltage (V_{PV}) Type Single-Phase Transformerless Inverter Topologies

Full-bridge (FB) single-phase transformerless inverter topologies with both bipolar and unipolar switching pattern [61] are explained in this section. A conventional FB inverter with a bipolar configuration has been used for achieving constant CMV, and low i_{cm}. However, the loss increases which leads to a reduced system efficiency [95].



(a) (b) (c)

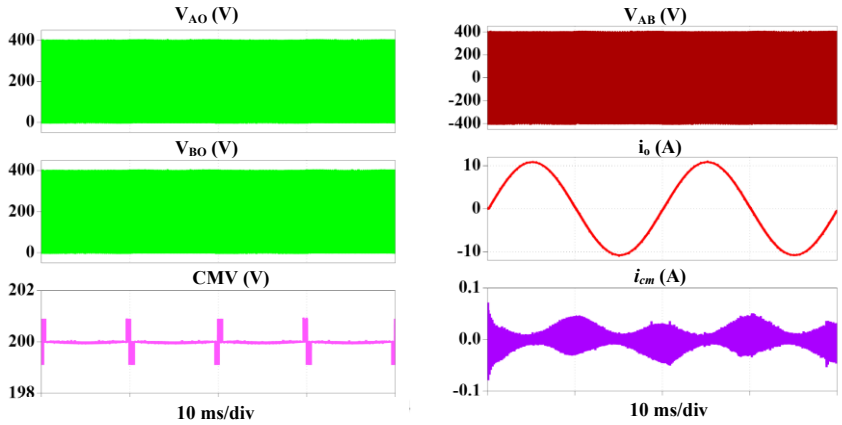
Fig. 2.8. Illustration of (a) Full Bridge inverter, (b) its bipolar switching pulses, and (c) its unipolar switching pulses.

Hence, unipolar has been introduced for overcoming the efficiency issue [62]. In this section, bipolar and unipolar based FB inverters are shown in detail and with the appropriate wave forms. Furthermore, the other single-input transformerless inverters are categorised in Fig. 2.1 and discussed with the simulated waveforms of i_{cm}, output voltage/current, CMV

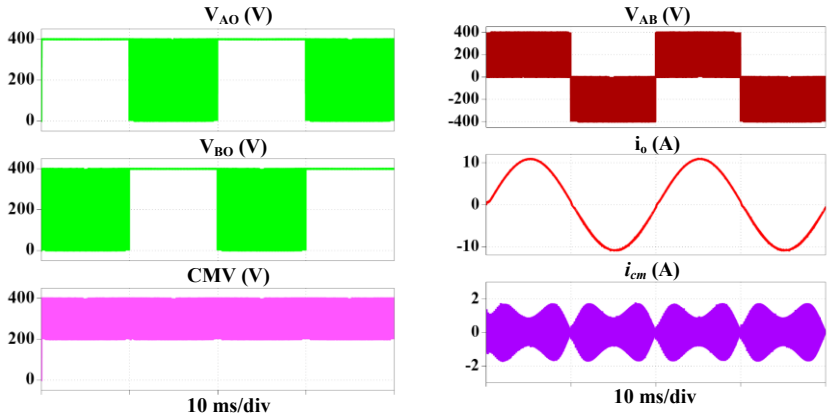
and the voltage of neutral (O) to points A and B. Table 2.1 tabulates the parameter values used for the simulations.

Fig. 2.8 (a) illustrates the circuit configuration of the F-B transformerless inverter topology with the parasitic capacitors on both sides of the PV panel. A bipolar switching pattern is shown in Fig. 2.8 (b). Switches Q_1 and Q_4 are turned ON for the positive half cycle, and the output current flows through the antiparallel diode of Q_2 and Q_4 to the load. On the other hand, Fig. 2.8 (c) shows the switching modulation for unipolar operation. In this modulation scheme, Q_2 is complementary to Q_1, and Q_3 complementary to Q_4. For the positive half cycle, Q_1 and Q_4 are ON, and hence, the output voltage is equal to the input voltage. During the freewheeling period, the output current flows through Q_1 and the antiparallel diode of Q_2 for the positive half cycle; and for the negative half cycle, the output current flows through Q_3 and the antiparallel diode of Q_4.

The output voltage and current of the bipolar FB inverter are shown in Fig. 2.9 (a). The CM current is low and the CMV is constant. However, the output current ripple is high, which increases the size of the output filter. Moreover, the energy conversion efficiency is decreased significantly. On the other hand, the leakage current is very high when an FB inverter is operated for the unipolar switching pattern due to the occurrence of an active and zero state within every pulse width modulation (PWM) cycle. Hence, the CMV varies from 200 V to 400 V with the switching frequency (see Fig. 2.9 (b)). However, the energy conversion efficiency is increased compared to the bipolar modulation due to the reduced output ripple and optimised freewheeling path of the unipolar PWM strategy.



(a)



(b)

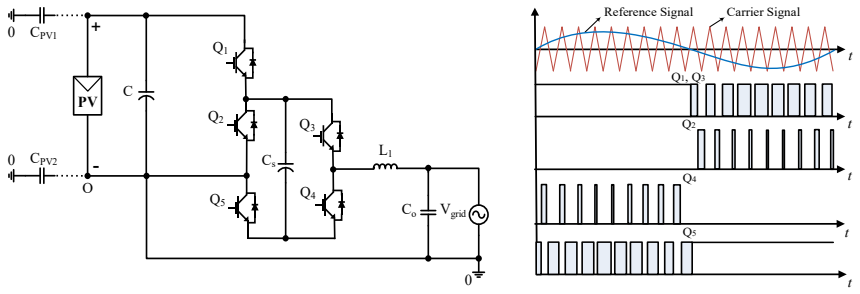
Fig. 2.9. Simulation results of FB inverter with (a) bipolar switching pulses, and (b) unipolar switching pulses.

2.2.1. Common Ground Type Topologies

The topology where the negative polarity of the PV panel is directly connected with the grid is called common ground type topology, such as, S4 [42], Siwakoti-H [16], and those in [12], [5], [44]. The significant advantage of such kinds of topologies is the constant CMV and the elimination of i_{cm}.

A. Inverter Topology in [12]

The topology presented in [12] is the concept of a virtual DC bus. The purpose of this technique is to generate the negative output voltage which is necessary for the operation as an inverter. Hence, the grid neutral line (O) is directly connected with the negative pole of the PV panel, and therefore the parasitic capacitors (C_{pv1} and C_{pv2}) are clamped to the zero potential of the neutral, theoretically resulting in zero i_{cm}. The circuit structure is given in Fig. 2.10 (a) with the modulating switching pulses in Fig. 2.10 (b). During the positive half cycle, the switches Q_1 and Q_3 are always ON, and Q_2 is always OFF. In the negative half cycle, Q_5 is always ON, and Q_4 is always OFF. The most challenging part of this topology is to control the virtual DC bus capacitor (C_s) along with the real bus in every switching frequency (f_{sw}).

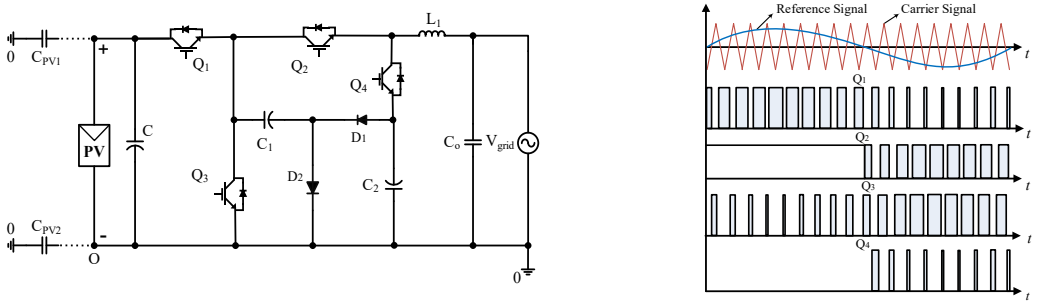


(a) (b)

Fig. 2.10. Illustration of (a) inverter topology in [12], and (b) its switching pulses.

B. S4 Topology

The S4 topology is demonstrated in [42], [96] as shown in Fig. 2.11 (a). To operate the inverter, sinusoidal PWM (SPWM) is used to minimise the switching losses and to reduce the filter requirement, as shown in Fig. 2.11 (b). During the positive half cycle, the switches Q_1 and Q_3 are ON with the switching frequency to produce positive and zero voltage, while Q_2 is OFF throughout the whole period. Hence, the output voltage of $+V_{DC}$ is achieved. In this period, the diode D_1 is OFF while the capacitor C_1 is charged with D_2. On the other hand, the voltage across the capacitor C_2 is constant just as it is in the case of the switched capacitor.



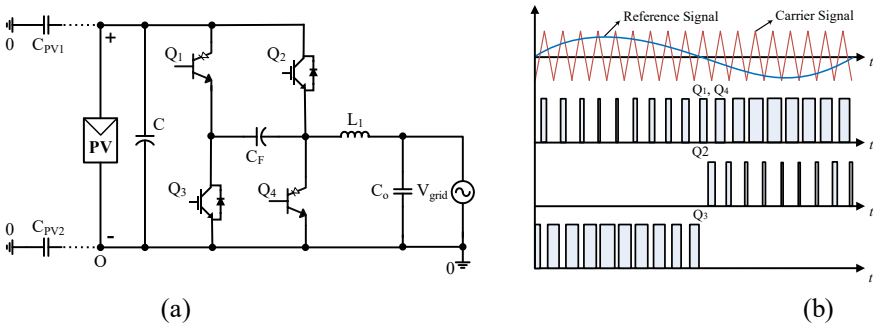
(a) (b)

Fig. 2.11. Illustration of (a) S4 inverter, and (b) its switching pulses [42].

To generate the negative voltage for the utility grid, the capacitor C_2 is charged by the capacitor C_1 with negative polarities up to $-V_{DC}$. However, the two-stage charge transfer process (V_{in} to C_1 and C_1 to C_2) increases the number of power components and also the losses in the system.

C. Siwakoti-H

The number of semiconductor components is significantly reduced in the topology proposed in [16], where only four switches are used. Constructed like an H-bridge shown in Fig. 2.12 (a), the inverter uses a flying capacitor to create a negative bus voltage for the inverter during the negative cycle. Fig. 2.12 (b) illustrates the switching pulses. The switches (Q_1 and Q_4) experience bipolar voltage stress, which is equal to $\pm V_{DC}$. Thus, bipolar voltage blocking capability switches such as the Reverse Blocking (RB) switches are needed (e.g. RB-IGBT). On the other hand, the other two switches (Q_2 and Q_3) are capable of producing the voltage stress of $2V_{DC}$. During the positive half cycle, only Q_2 is connected to produce the positive voltage, and Q_3 is ON for the negative half cycle to produce the negative voltage. The other two switches are used for zero states.



(a) (b)

Fig. 2.12. Illustration of (a) Siwakoti-H inverter, and (b) its switching pulses [16].

D. Flying Capacitor Topologies in [5], and [43]

The flying capacitor concept can be used in common ground transformerless inverter topologies as it is presented in [5], and [43]. The first one of these two new topologies is proposed by Siwakoti in [5], the second one is proposed by Chen in [43], and these are shown in Fig. 2.13 (a) and Fig. 2.13 (b), respectively. Both topologies operate with the same modulation pulses (see Fig. 2.13 (c)). The same concept (negative polarity of the PV panel is directly connected to the grid) is used to get zero i_{cm}. For instance, the switch Q_1 and diode charge the flying capacitor, and the discharging path is through switches Q_2 and Q_4, which creates the negative polarity. The flying capacitor (C_F) is charged from the input voltage, and the constant output voltage which is equal to the input voltage. This is like the voltage converter integrated circuit, e.g., Maxim-ICL7660 and Texas Instrument-LMC7660. The

circuit schematic in Fig. 2.13 (b) is quite similar to the one shown in [43], with the only change being the device position.

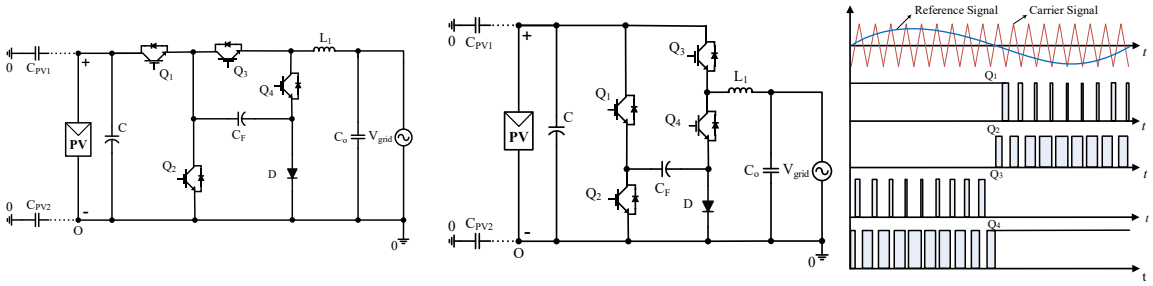


Fig. 2.13. Illustration of (a) inverter topology in [46], (b) inverter topology in [5], and (c) their switching pulses.

The switch Q_3 carries the load current during the positive active cycle and the negative half cycle; Q_2 and Q_4 carry the load current where Q_2 creates a negative power cycle by discharging the flying capacitor (C_F) through Q_4. All the switches work under the switching frequency (f_{sw}) with the standard unipolar SPWM.

E. Flying-inductor inverter

The topology proposed in [44] is a five-switch based diode-less topology. Using a flying inductor (L_m) with low inductance helps to boost the input DC voltage with power injection from the PV panel to the grid [44]-[45].

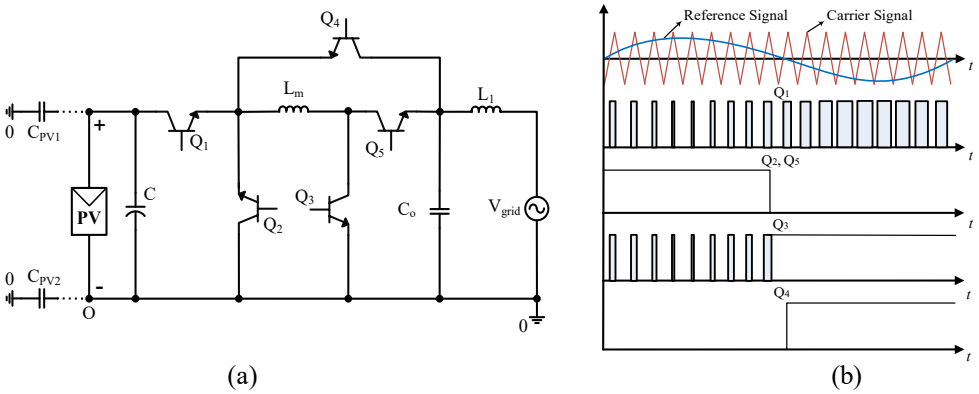


Fig. 2.14. Illustration of (a) inverter topology in [44], (b) its switching pulses.

L_m is charged by the simultaneous conducting of switches Q_1 and Q_3. However, the other three switches are used for discharging the flying inductor. The circuit structure of this

topology is illustrated in Fig. 2.14 (a), and the gate pulses during operation are seen in Fig. 2.14 (b).

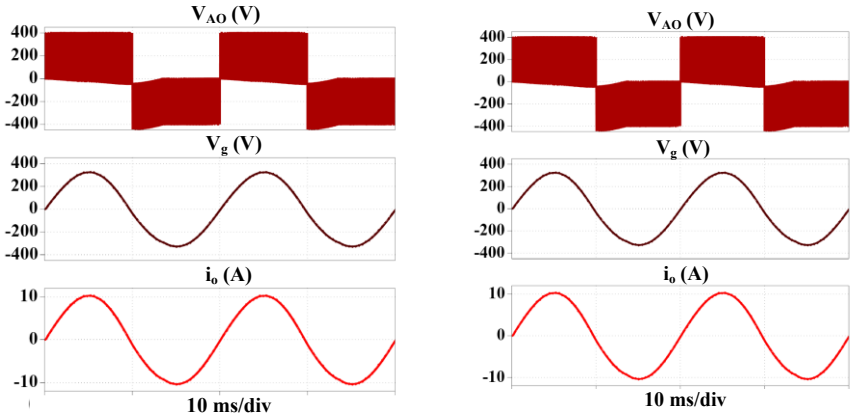


Fig. 2.15. Simulation results of common ground topologies, (a) inverter topology in [12], and (b) inverter topology in [5].

Fig. 2.15 displays the results of common ground topologies proposed in [5] and [12], where the flying capacitance (C_F) is chosen as 470 µF. Both figures (see Fig. 2.15 (a) and Fig. 2.15 (b)) show the inverter output, point A to the ground (O) as well as the PV negative directly connected to the ground through neutral and the output voltage (V_g) and current (i_o).

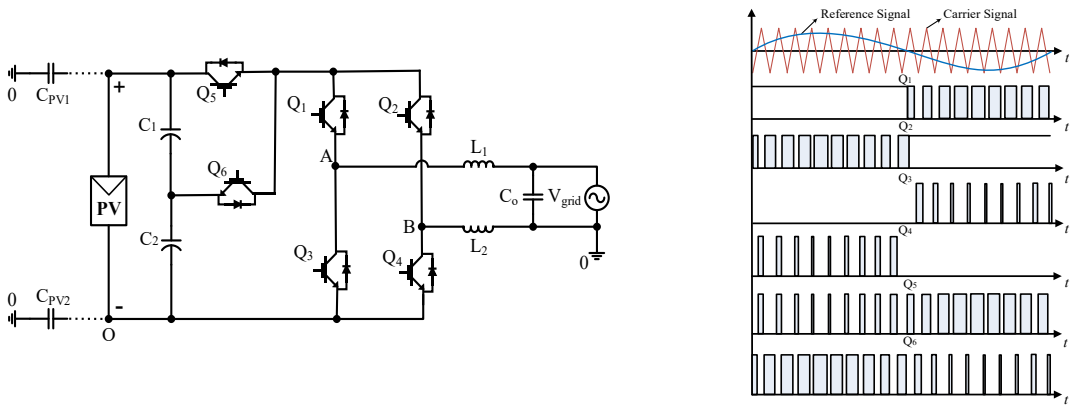
2.2.2. H-Bridge Type Topologies

A. Mid-Point Clamped Type Topologies

The FB inverter can be extended through the semiconductor devices at either the AC or DC side for clamping the voltage. Such kinds of topologies are known as midpoint clamping transformerless inverter topologies. The main advantages of midpoint clamping techniques are the reduced i_{cm} with lower ripple than other topologies where the CMV remains constant. The mid-point clamping topologies, such as iH5/oH5 [97], and [98], oH5-1 [37], oH5-2 [99], and [100], H5-D [38], HERIC Active 1 [39], HERIC Active 2 [39], and [101], HERIC Active 3 [39], PN-NPC [40], and [102], HB-ZVR [7], and HB-ZVR-D [41], are explained through focusing on the operational and working principles. Further, simulated waveforms are presented.

i. iH5/oH5

This topology is presented in [9], and [37] where two switches (Q_5 and Q_6) are added at the DC side, as revealed in Fig. 2.16 (a). The switching pulses are presented in Fig. 2.16 (b).



(a) (b)

Fig. 2.16. Illustration of (a) oH5 inverter, and (b) its switching pulses.

The voltage clamping part of this topology is achieved in two ways. At potential up, the body diode of switch Q_6 is in the forwarding mode with the junction capacitor of switch Q_5 and the DC link capacitor C_1 where the current flow path is Q_1 and the body diode of Q_2 is through the grid.

On the other hand, at potential down, switch Q_6 is in the active mode with the junction capacitors of switch Q_3, Q_4 and the DC link capacitor C_2 where the current flow path is switched to Q_3 and the body diode of Q_4 is through the grid. The main advantage of this topology is the achievement of a good differential mode characteristic, which is the same as the unipolar SPWM FB grid-connected inverter but with more efficiency. Moreover, extra switches on the DC side blocks the input voltage to half; hence a constant CMV can be achieved.

ii. oH5-1 and oH5-2

The oH5 topology (both 1 and 2), as shown in Fig. 2.17, is introduced in [37] to guarantee the clamping to half the input voltage in the freewheeling period, thereby avoiding the high-frequency common-mode voltage.

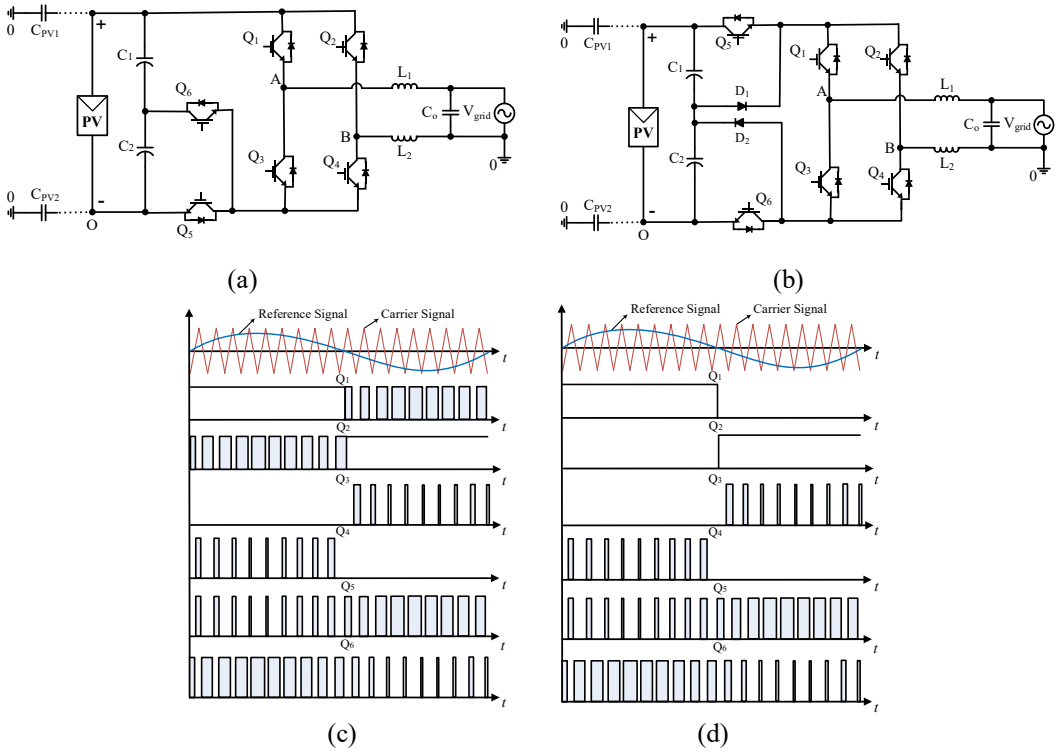


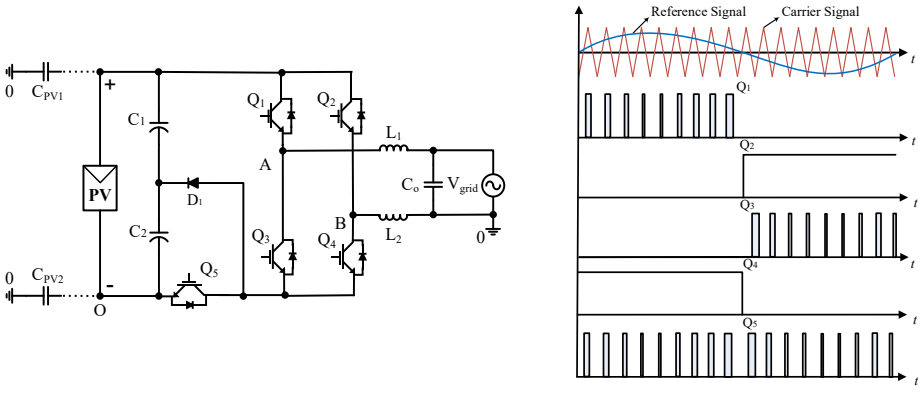
Fig. 2.17. Illustration of (a) oH5-1 inverter, (b) oH5-2 inverter, (c) switching pulses for oH5-1 inverter, and (d) switching pulses for oH5-2 inverter.

The two switches (Q_5 and Q_6) and diodes (D_1 and D_2) are used to clamp the voltage for constant CMV which reduces the ground current. Switches Q_1 to Q_4 work like an FB inverter. Switches Q_5 and Q_6 are alternatives to each other. Switches Q_1 and Q_2 work with the grid frequency (f_g), and the other four work at the switching frequency (f_{sw}).

iii.H5-D

The topology named as H5-D is presented in [38] where five switches are used together with a diode. This topology is an improved H5 topology, in which the diode (D_1) and switch (Q_5) are used to clamp the input voltage in order to achieve a constant CMV. Moreover, the improved modulation technique is set to keep the CMV constant. The CM current is only

about one-third of that in the H5 topology using the same electrical parameters and power switches. On the other hand, the THD is quite high as the H5 topology. The circuit diagram and the modulation strategy, as shown in Fig. 2.18, reveals that the two switches operate at the grid frequency (f_g), and the remaining three switches operate at the switching frequency (f_{sw}).

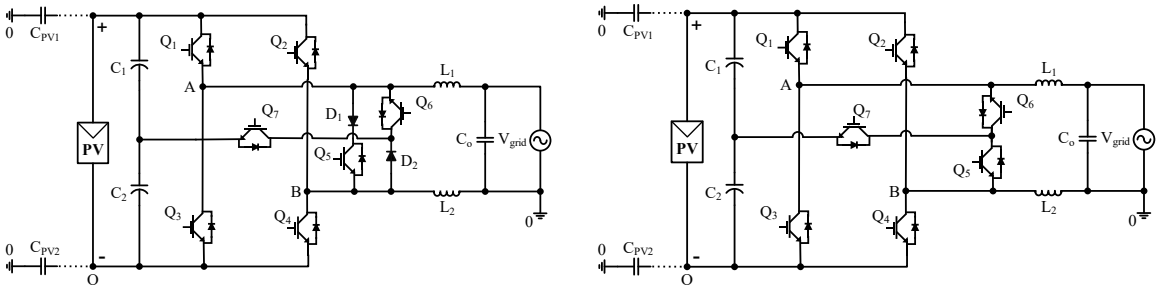


(a) (b)

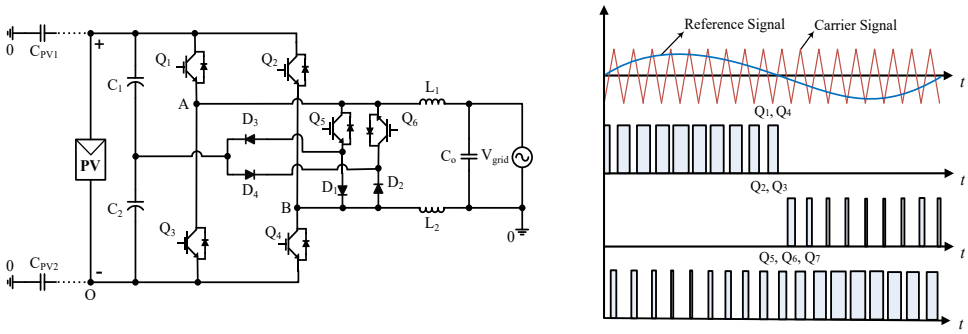
Fig. 2.18. Illustration of (a) H5-D inverter, and (b) its switching pulses.

iv.HERIC Active 1, HERIC Active 2 and HERIC Active 3

As discussed in the AC decoupling subsection, the HERIC topology reveals that the leakage current is in the medium range and the CMV is not fully constant. Three major topologies are proposed by changing and adding the placement of semiconductor devices; see Fig. 2.19 (a) to Fig. 2.19 (c). Fig. 2.19 (d) shows the switching pulses keep i_{cm} constant with low i_{cm} [37], [99]. The main disadvantage of these topologies is the shoot-through issue in the unidirectional controllable clamping path. Hence, a dead time should be introduced to avoid the short circuit issue [103].



(a) (b)

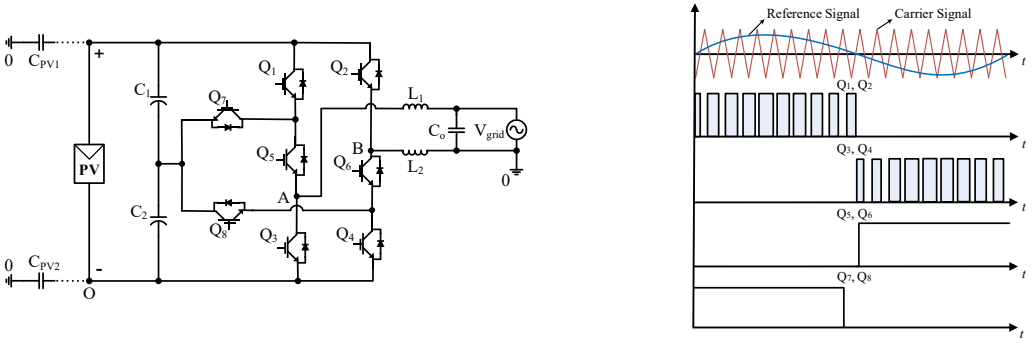


(c) (d)

Fig. 2.19. Modifications of HERIC inverter, (a) HERIC Active-1 inverter, (b) HERIC Active-2 inverter, (c) HERIC Active-3 inverter, and (d) their switching pulses.

v.PN-NPC

Positive negative NPC (PN-NPC) is proposed in [40] which combines the positive NPC (P-NPC) and negative NPC (N-NPC) switching cells. The circuit diagram of PN-NPC is illustrated in Fig. 2.20 (a) with the switching modulation in Fig. 2.20 (b). In this topology, four switches work at the grid frequency (f_g) while the other four work with the switching frequency (f_{sw}). This topology can operate in four operational modes for each period of the utility grid. In the freewheeling period, four switches are ON so that the inductor current flows through all of these switches and this can lead to high conduction losses.



(a) (b)

Fig. 2.20. Illustration of (a) PN-NPC inverter, and (b) its switching pulses.

vi.HB-ZVR, and HB-ZVR-D

The H-Bridge Zero Voltage Rectifier (HB-ZVR) (see Fig. 2.21 (a)) topology is presented in [9] where four switches work like the FB inverter and the short-circuit voltage

clamped to the midpoint of the DC bus is done through four rectified diodes and a bidirectional switch.

In the positive half cycle, Q_1 and Q_4 work to generate the active vector as shown in Fig. 2.21 (c). Similarly, in the negative half cycle, Q_2 and Q_3 are ON and work to generate the active vector. When Q_5 is ON, the other switches are OFF. Thus, zero voltage states can be achieved. The circuit structure of the H-Bridge Zero Voltage Rectifier-Diode (HB-ZVR-D) is revealed in Fig. 2.21 (b) with gate drive signals in Fig. 2.21 (c) [41], which is very similar to HB-ZVR. The difference between these two topologies is a fast-recovery diode which is used to achieve zero i_{cm} and constant CMV. The two diodes (D_5 and D_6) are used for clamping branches of the freewheeling path. Fig. 2.22 (a) shows the voltage of the terminal A to neutral and terminal B to neutral and this neutral state allows it to achieve a constant CMV. A low value of i_{cm} can be seen in Fig. 2.22 (b) with a low ripple on the output current.

Fig. 2.23 shows the result for oH5-1 topology. It can be seen that the output current shows less ripple, the CMV is not sufficiently constant, and the common mode current is in the medium range.

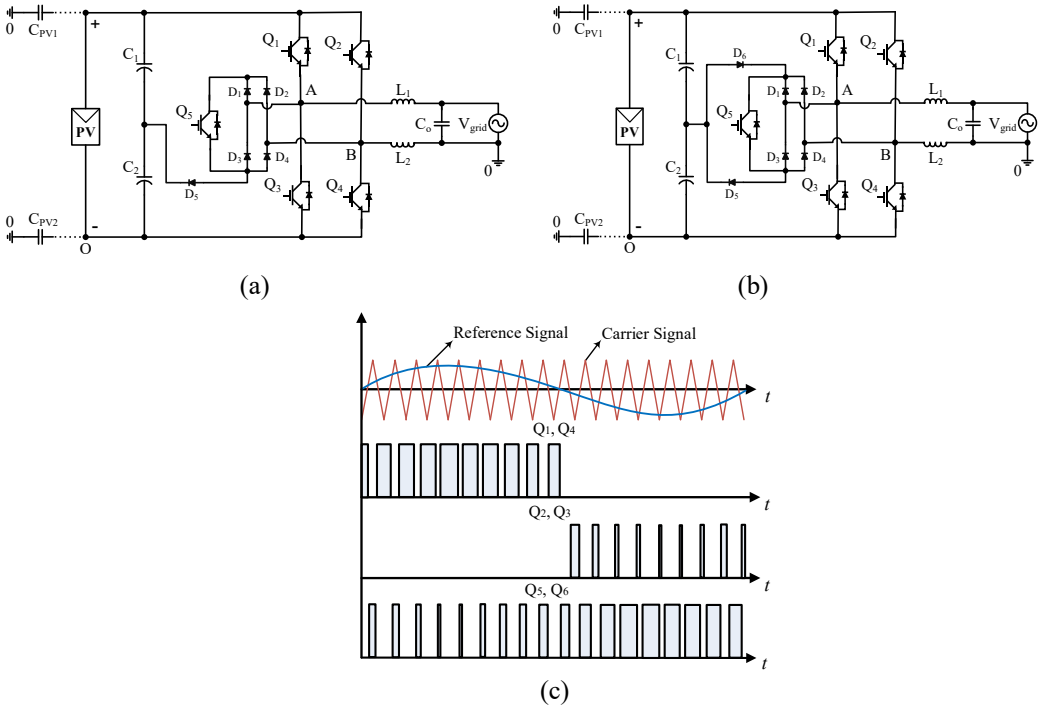


Fig. 2.21. HB-ZVR family inverters, (a) HB-ZVR inverter, (b) HB-ZVR-D inverter, and (c) their switching pulses.

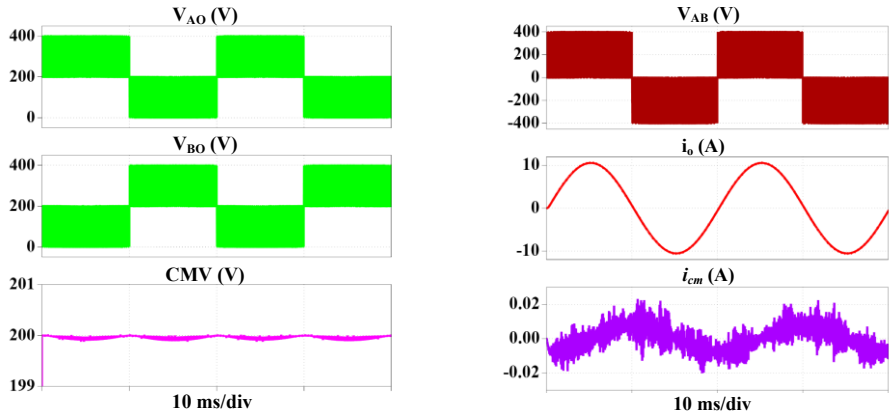


Fig. 2.22. Simulation results of iH5/oH5 inverter.

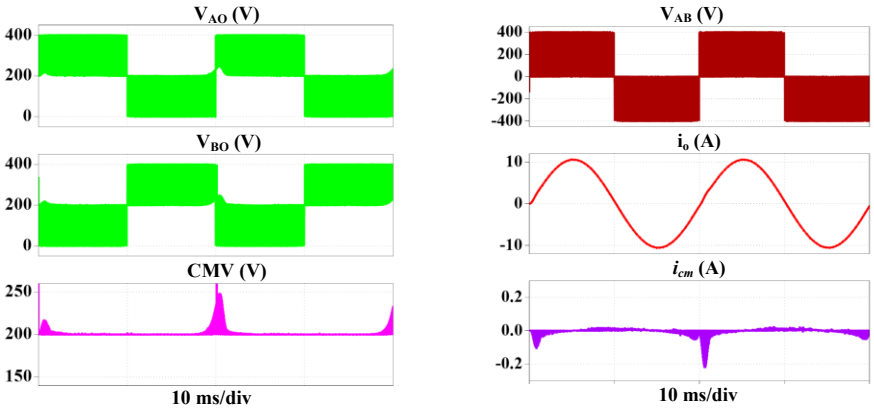


Fig. 2.23. Simulation results of oH5-1 inverter.

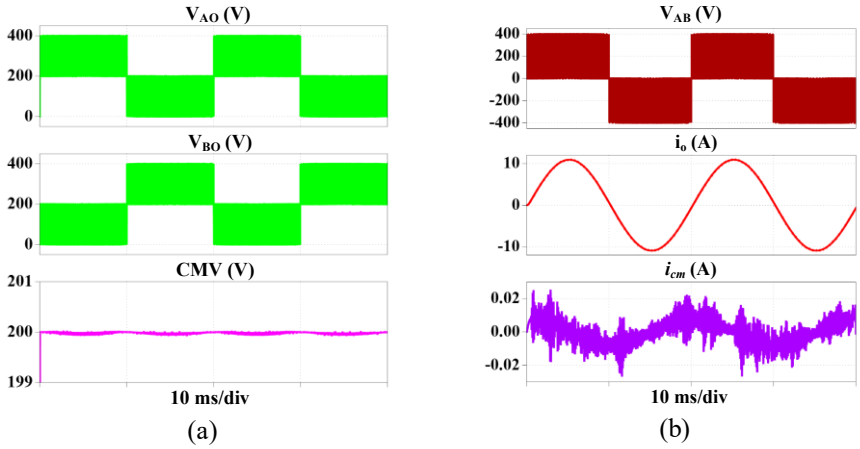
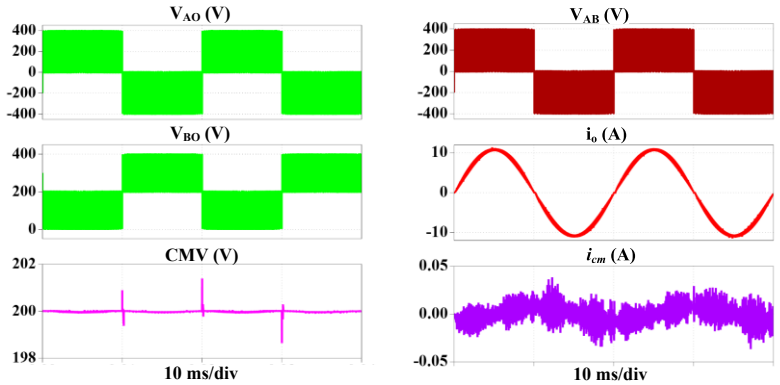


Fig. 2.24. Simulation results of HERIC Active-1 inverter.



(a) (b)

Fig. 2.25. Simulation results of PN-NPC inverter.

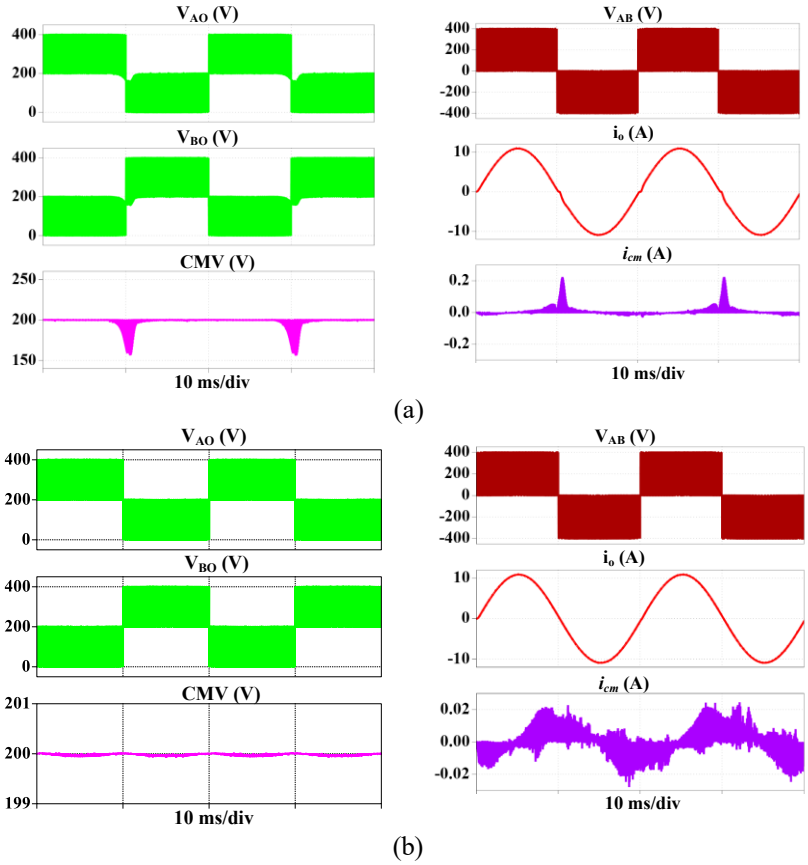


Fig. 2.26. Simulation results of HB-ZVR family inverters, (a) HB-ZVR inverter, (b) HB-ZVR-D inverter.

With the additional placement of switches and diodes on the HERIC topology, as shown in Fig. 2.24, i_{cm} can be reduced to a more constant CMV. The PN-NPC result is shown in Fig. 2.25 (a) and Fig. 2.25 (b) where a low i_{cm} with a constant CMV is achieved.

The resulting wave forms for HB-ZVR are shown in Fig. 2.26 (a), which achieves an almost constant CMV and a medium range of i_{cm}. However, the HB-ZVR-D achieves low i_{cm} with an almost constant CMV as shown in Fig. 2.26 (b).

B. Decoupling Techniques

B.1. AC Decoupling Type Topology

AC decoupling based transformerless inverter topologies are extended by adding switches and diodes at the AC side. These kinds of topologies are presented to achieve a low THD based output voltage and current. Moreover, the leakage current is reduced with a balanced system and constant CMV. The AC decoupling topologies are HERIC and HERIC AC based topologies [9], [31], and [104].

The HERIC topology, well known in string inverters for achieving high efficiency, was first invented in 2003 [85]. In addition, in the case of the German manufactured Sunways NT solar inverter, the use of this topology is highly recommended. Moreover, 5 kW string inverters are investigated, which achieve 98% efficiency [105]. This topology employs Unipolar-SPWM to achieve a low current ripple and high efficiency because the load current is short-circuited through the switches Q_5 and Q_6 during the freewheeling period. However, the CM issue is present there as the PV module is decoupled from the grid and the voltage is not clamped to the half of the supply voltage [106]. The HERIC AC based topology is similar to the HERIC topology which uses two diodes with the switches Q_5 and Q_6 in series as proposed in [104], and [107]. These two diodes are used to conduct the output current at the freewheeling time. The operational mode of these topologies is the same as the FB inverter; the only difference is the output current flow path through the addition of the used diodes and switches in the freewheeling period. The circuit diagrams of both topologies are given in Fig. 2.27 (a) and Fig. 2.27 (b) respectively and the gate drive signals in Fig. 2.27 (c).

The simulation results for the HERIC topology are illustrated in Fig. 2.28. The obtained CMV is almost constant and the i_{cm} is 160 mA. The main advantage of this topology is that less ripple is obtained on the output. Hence the THD is very low.

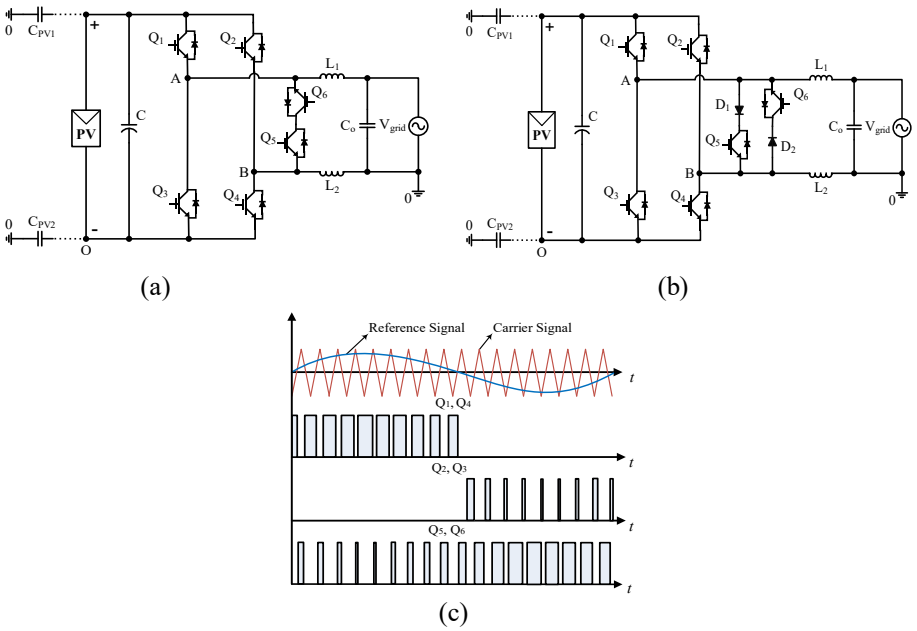


Fig. 2.27. Illustration of (a) HERIC (b) HERIC ac based (c) switching pulses.

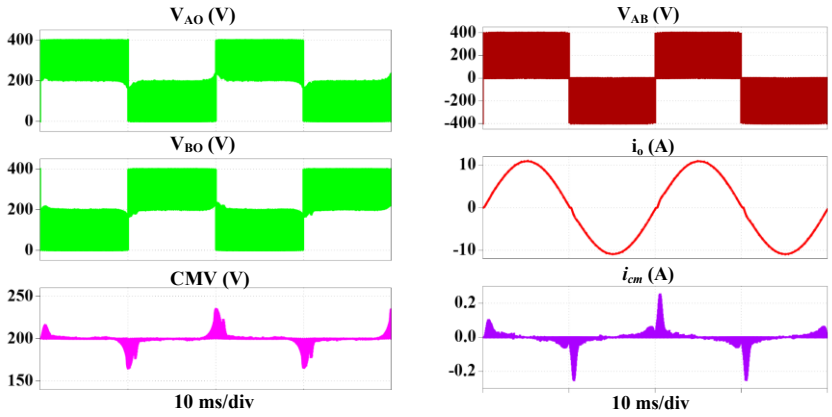


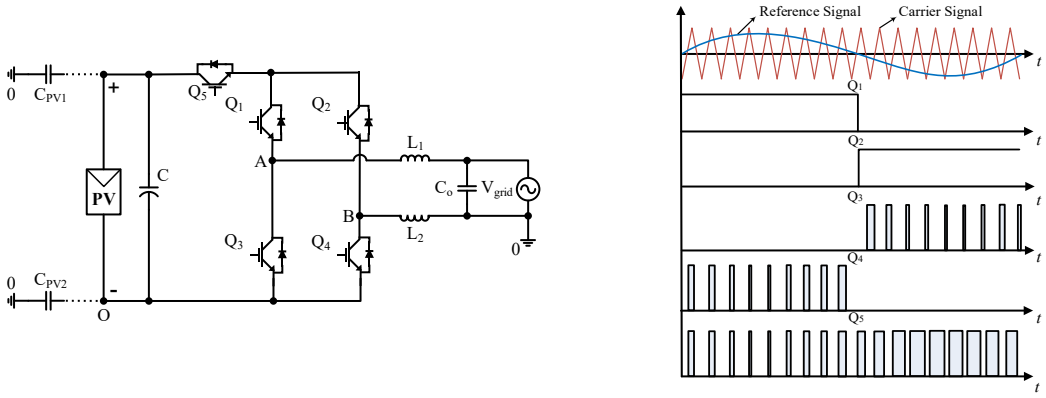
Fig. 2.28. Simulation results of HERIC inverter.

B.2. DC Decoupling Type Topologies

The extra switches and diodes on the DC side are added for inventing new topologies and such kinds of topologies are known as DC decoupling based transformerless inverter topologies. These topologies are introduced for mitigating the common mode current for balancing the system. A few topologies are explained below such as H5 [97], H6 DC side [54], H6 DC side -1 [33] and H6 DC side -2 [33] topologies.

i.H5

The H5 topology is a high efficiency based transformerless inverter topology and it was first proposed in [32] which was patented by one of the best PV inverter producers, SMA solar technology. Its operational principle is almost the same as the FB. However, one switch is used on the DC side, which is called the DC decoupling switch. This switch is operated at the switching frequency (f_{sw}). The upper switches are operated with grid frequency (f_g), and the lower switches are operated with the switching frequency (f_{sw}).



(a) (b)

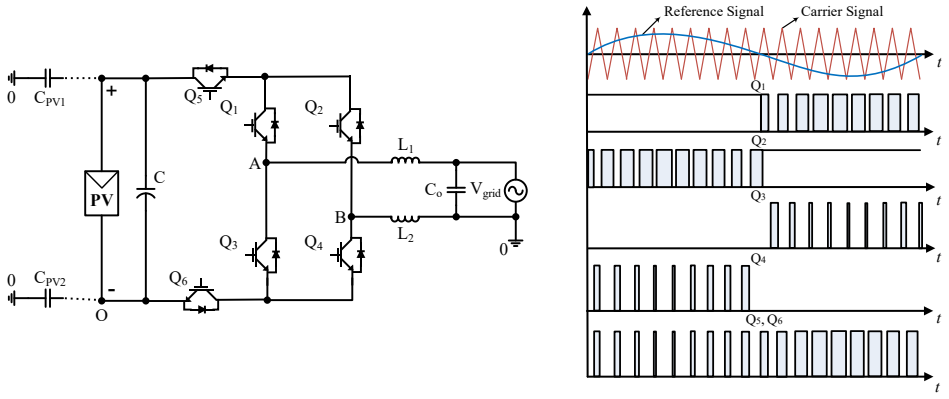
Fig. 2.29. Illustration of (a) H5 inverter, and (b) its switching pulses [8].

The PV panel is disconnected from the grid side during zero voltage states when the switch Q_5 is OFF; as a result, during the current freewheeling period, there is no way to flow the output current at the DC side which is an effective solution to reduce the i_{cm} [39], [108], and [109]. In the positive half cycle, switches Q_5 and Q_4 turn ON at the switching frequency (f_{sw}), and Q_1 at the grid frequency (f_g) whereas the other two switches are OFF.

By contrast, Q_5 and Q_2 turn ON at the switching frequency (f_{sw}) and Q_3 at grid frequency (f_g) whereas the other two switches are OFF in the negative half cycle. At the freewheeling period, the output current flows through Q_1 and the body diode of Q_3 for the positive period, and through Q_3 and the body diode of Q_1 for the negative period. The main disadvantage of this topology is the higher conduction losses through the three associated series switches in the active phase [110]. The circuit structure and switching modulation of the H5 are shown in Fig. 2.29 (a) and Fig. 2.29 (b) respectively.

ii.H6 DC Side

The H6 DC side topology is displayed in Fig. 2.30 (a) with the gate drive signals in Fig. 2.30 (b). This topology is introduced in [48], and it is operated in four stages. Moreover, the presence of the junction capacitor in the H6 DC side topology, like the H5 topology, is explained in [49] and [111], as well as the effect of the resonant circuit through the junction capacitor and its leakage current issue. The switches Q_5, Q_1 and Q_6 conduct in the positive half cycle, while Q_3 and Q_2 are OFF. On the freewheeling period of the positive and negative half cycle, the body diode of Q_3 is in the forward bias with conducting switch Q_1, and the body diode of Q_4 is in the forward bias with conducting switch Q_2, respectively. In this topology, extra low value capacitors are used to remove the CM effect which is the reason for increasing the losses [112].



(a) (b)

Fig. 2.30. Illustration of (a) H6 DC side inverter, and (b) its switching pulses [29].

iii.H6 DC Side -1 and H6 DC Side -2

These two topologies are presented in [33], and the concept is taken from the aforementioned topologies H5 [32] and H6 [48]. The positive terminal of the PV array and the terminal (A) are connected through a switch Q_6 to make a current path as seen in Fig. 2.31 (a). Further the terminal (A) is changed to terminal (B), which is shown in Fig. 2.31 (b). In both topologies, the gate drive signals are the same (see Fig. 2.31 (c)). These topologies work in four operational modes. The switches Q_1 and Q_3 work at the grid frequency (f_g), and the other four switches work at the carrier frequency (f_{sw}). In the freewheeling period, switch Q_1 conducts with the body diode of Q_3 for the positive half cycle; the switch Q_3 and the body

diode of Q_1 are ON for the negative half cycle. Both topologies have less power losses compared to H5. Fig. 2.32 illustrates the output waveforms of H5 where the inverter output voltage and the output current are shown. The i_{cm} is around 200 mA with an almost constant CMV.

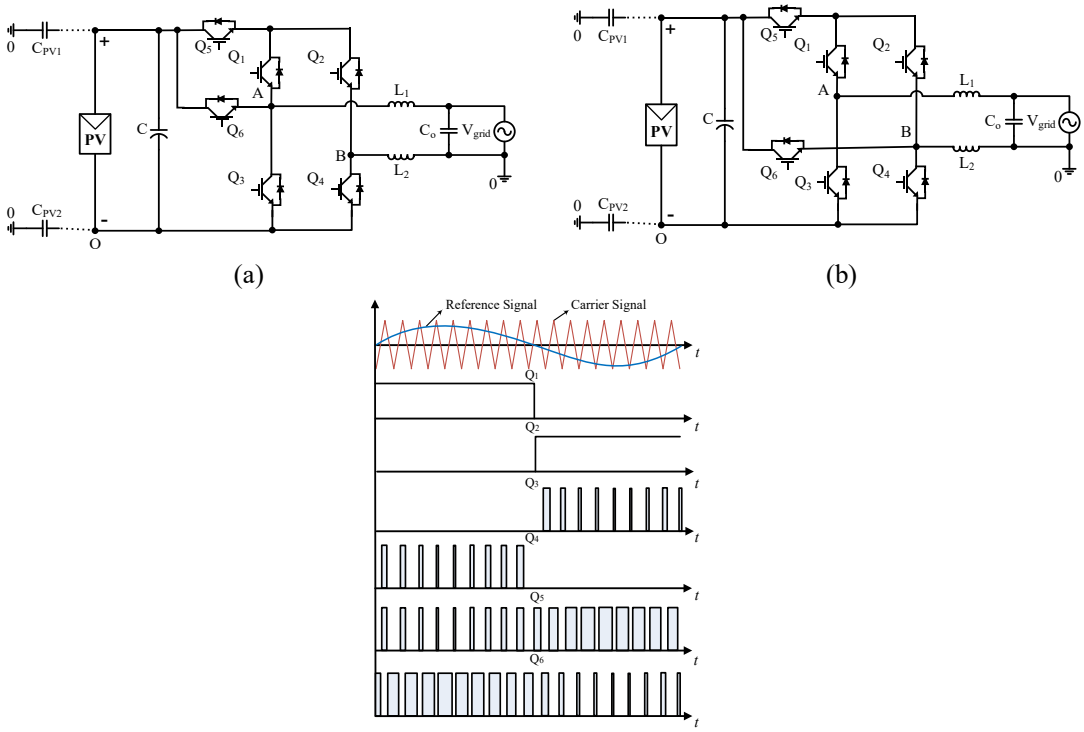


Fig. 2.31. Illustration of (a) H6 DC side-1 inverter, (b) H6 DC side-2 inverter, and (c) their switching pulses.

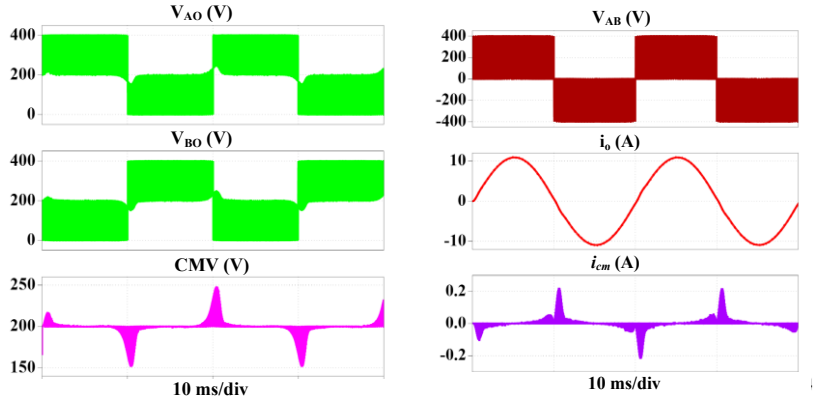


Fig. 2.32. Simulation results of H5 inverter.

2.2.3. H6 Type Topologies

F-B topologies are extended with switches and diodes to reduce the leakage current with smoother output waveforms. In this sub-section, those kinds of topologies are presented like H6 with diodes-1 [34], H6 with diodes-2 [63], H6-1 [35], H6 in mid-switch [36], and midpoint switches with diodes [39], and [49]. Further, the circuits are simulated to see the output waveforms, i_{cm} and CMV.

A. H6 with Diodes-1 and H6 with Diodes-2

H6 with diodes-1 is presented in [34], which is structured by Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) switches. Four MOSFETs work as an F-B inverter as well as two extra switches and the diodes are used for freewheeling purposes.

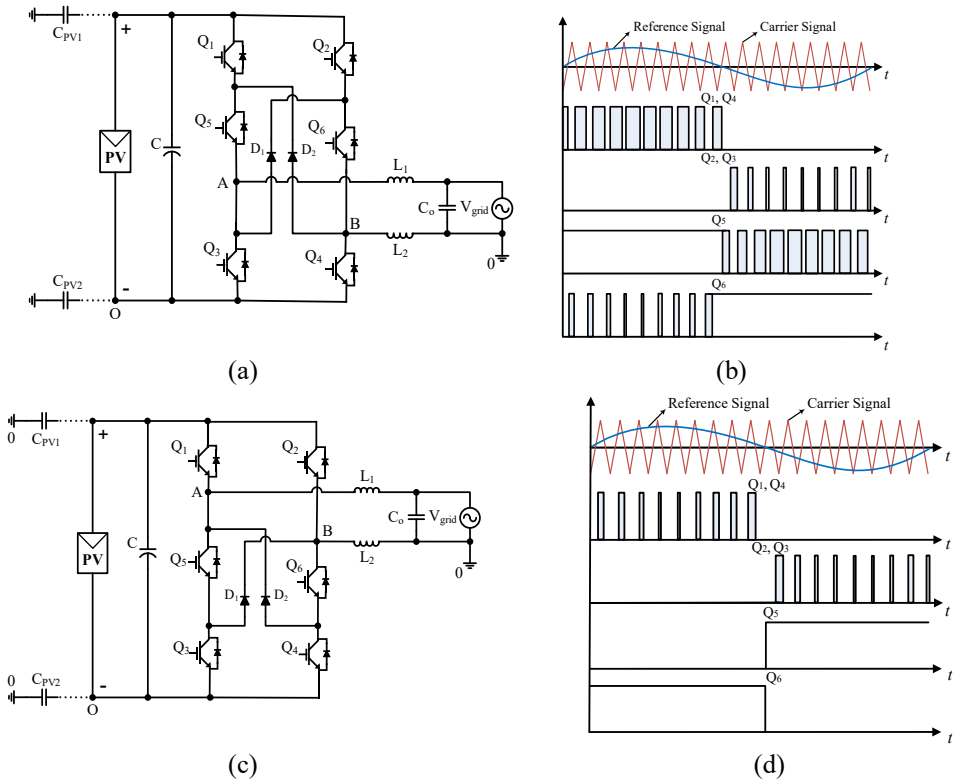


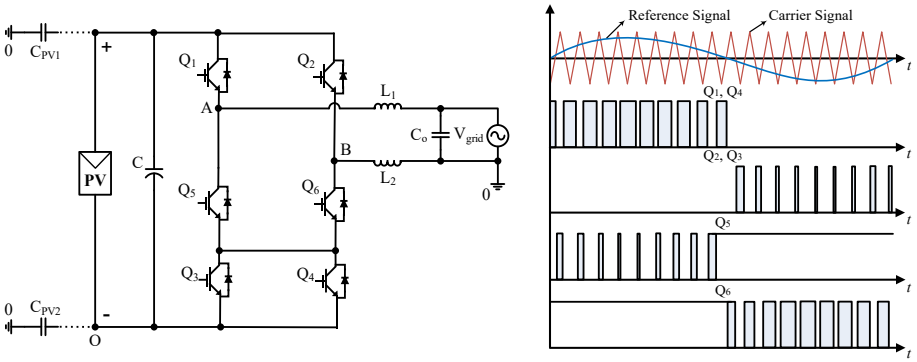
Fig. 2.33. Illustration of (a) H6 with diodes-1 inverter, (b) its switching pulses, (c) H6 with diodes-2 inverter, and (d) its switching pulses [57].

The same basic concept is used for H6 with diodes-2 topology. Fig. 2.33 (a) shows the circuit structure of H6 with diodes-1 and in Fig. 2.33 (c) is the circuit diagram of H6 with

diodes -2. Meanwhile, Fig. 2.33 (b) and Fig. 2.33 (d) show the switching pulses for these two topologies. After simulating these two topologies, i_{cm} is obtained as around 200 mA for H6 with diodes-1 and 250 mA for H6 with diodes-2 topology. However, in both cases, the CMV is quite constant. To reduce the i_{cm} correctly, an accurate modulation technique is needed. Hence, in [113] a topology is proposed, which replaces the switches Q_5 and Q_6 by two IGBTs and uses a new modulation controller based on the reactive power injection space vector PWM (SVPWM) technique as well as using proportion-integral-resonance (PIR) current controllers. The main deficiency of these topologies is the higher conduction losses in the active mode as the output current flows through the three switches [112].

B. H6-1 Topology

H6-1 topology is proposed in [35], and the idea is taken from the topologies including six switches with two diodes as discussed in [34], and [36]. However, the extra cross connected diodes are removed and MOSFET switches are replaced with IGBTs, as demonstrated in Fig. 2.34 (a) with the switching pulses in Fig. 2.34 (b). Hence, it is possible to handle the reactive power flow, which is not possible by MOSFET based topologies [114]. It works in six operational modes and makes a connection internally through creating a freewheeling path. Therefore, the circuit operates smoothly when it is connected to the grid. In the positive half cycle, Q_1, Q_6 and Q_4 are ON, and the current flows through the inductors, completing the cycle. Moreover, zero voltage state switch Q_6 and the antiparallel connected body diode of switch Q_5 both conduct and are not connected with the input; hence the current flows through the load. On the other hand, the remaining three switches Q_2, Q_5 and Q_3 conduct in the negative half cycle. A zero voltage state occurs in the negative half cycle, and the current flows between the switch Q_5 and the antiparallel connected body diode of switch Q_6.



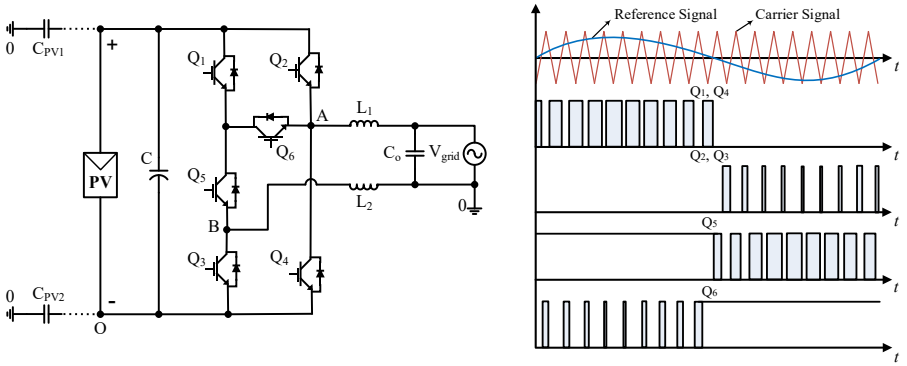
(a) (b)

Fig. 2.34. Illustration of (a) H6-1 inverter, and (b) its switching pulses [58].

The topology H6-1 [35] can be modified after changing the position of point A to B and B to A, and this topology also works in six operating modes like H6-1 [35]. The modified one can be simulated after changing the switching pulse Q_5 of the H6-1 to Q_6, and the other pulses remain the same. Indeed, the THD is reduced somewhat.

C. H6 in Mid Switch

H6 in mid-switch topology is presented in [36] which has four operational modes. Fig. 2.35 (a) displays the schematic diagram of the midpoint switch based H6 topology, and the switching pulse is shown in Fig. 2.35 (b). Moreover, the mid switch Q_6 is used to complete the circuit for the freewheeling period. In the positive half cycle, the freewheeling path works through the switch Q_6 and the body diode of Q_5. On the other hand, for the negative half cycle, the body diode of Q_6 is in active mode with the Q_5 switch. The main disadvantages of this topology are the high volume of the filter capacitor, and high ripple based output waveforms.

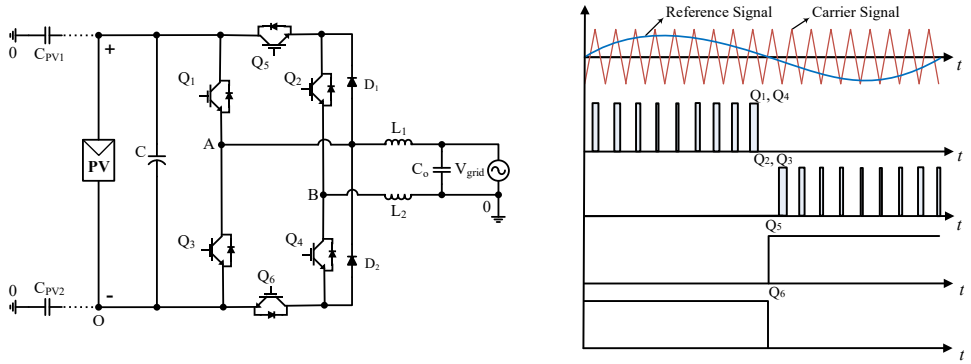


(a) (b)

Fig. 2.35. Illustration of (a) H6 with mid switch inverter, and (b) its switching pulses [60].

D. F-B with Midpoint-Switches and Diodes

In [39], [49] and [115], a topology is discussed where the idea is taken from the H5 topology. Two extra switches are added at the top and bottom of the middle of the F-B topology, and the two diodes are used for creating a freewheeling path. This topology is also known as hybrid bridge topology [116]. Moreover, the topology consists of two modules such as the H-B and NPC bridge. The circuit diagram is displayed in Fig. 2.36 (a). Switches Q_1 and Q_6 conduct together when Q_4 conducts. On the other hand, Q_5 works with the same switching pulses as Q_2 while Q_3 is continuously ON.



(a) (b)

Fig. 2.36. Illustration of (a) F-B inverter with midpoint-switches and diodes, and (b) its switching pulses [107].

The switching strategy is shown in Fig. 2.36 (b). In the freewheeling period, during the positive half cycle, D_2 works in forwarding bias with the conducting switch Q_4, and the output current flows through the load. Alternatively, during the negative half cycle, D_1 is in forward bias with Q_2. In this topology, the most important factor is that the dead time is fixed because switches Q_1, Q_2, Q_4, Q_6, and diode D_1 might be turned ON once in the positive half cycle.

E. ZCT-H6-1 and SLF-H6-1

Using the zero-current-transition (ZCT) technique, a new transformerless inverter is discussed in [65] as shown in Fig. 2.37 (a). In this topology, two auxiliary switches (Q_7, and Q_8) and two H6 switches (Q_5, and Q_6) operate at high frequency, whereas the full-bridge inverter switches $Q_1 - Q_4$ operate at line-frequency.

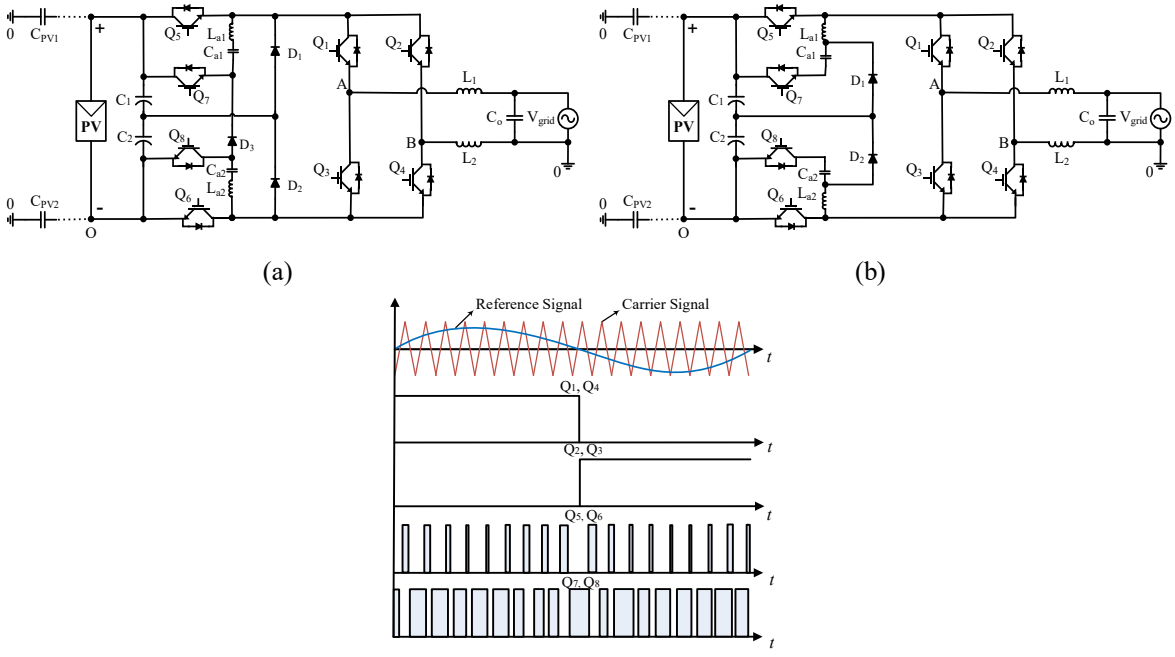


Fig. 2.37. Illustration of (a) ZCT-H6-1 [65], (b) SLF-H6-1 [66], and (b) switching pulses.

In addition, few resonant components are used in this topology to realise ZCT operation. As a result of using many additional components, the overall efficiency is comparatively low.

Another improved soft-switching circuit called the switching loss-free (SLF) inverter is introduced in [66], where it is possible to reduce the number of auxiliary components (see Fig. 2.37 (b)). Compared to the ZCT-H6-I topology, the connection points of two resonant tanks are moved from the midpoints of the auxiliary switch and resonant capacitor to the midpoints of the resonant capacitor and resonant inductor, respectively. With this arrangement, this new topology is able to obtain over 95% efficiency over a wide load range, which is roughly 1.5% higher than the ZCT-H6-1 topology. Moreover, SLF-H6-1 topology mitigates more leakage current than ZCT-H6-1 topology. Fig. 2.37 (c) shows the required gate signals for both topologies.

Fig. 2.38 (a) displays the output voltage and current of the H6-1 topology with the i_{cm}. The RMS value of i_{cm} is around 180 mA, and the CMV remains almost constant. Fig. 2.38 (b) shows the output voltage and the current of hybrid bridge topology.

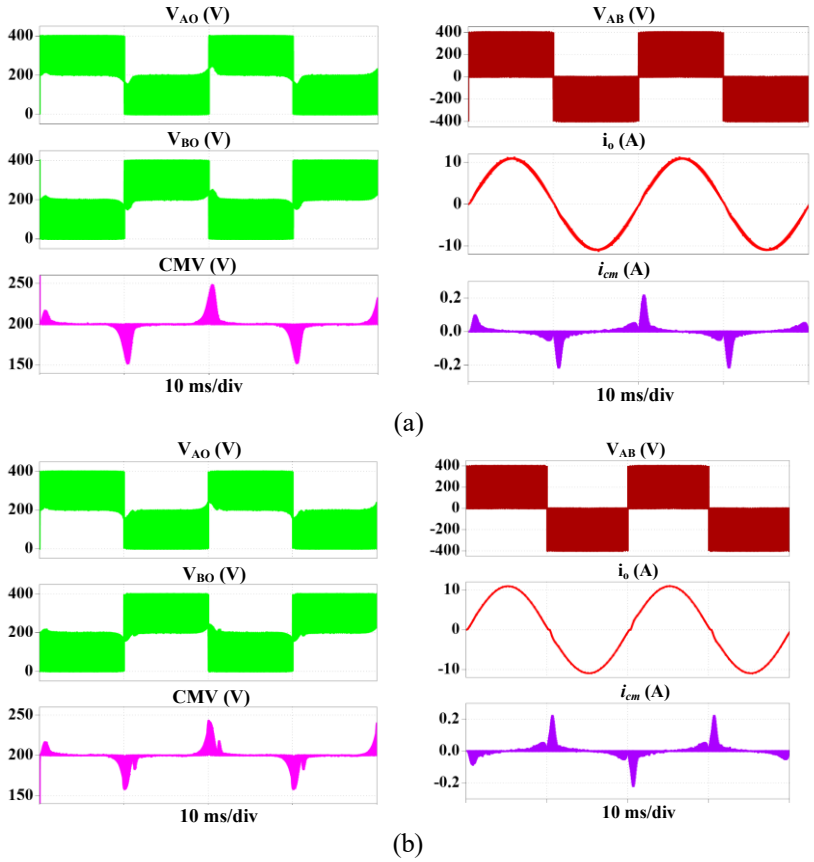


Fig. 2.38. Simulation results (a) H6-1, (b) F-B inverter with midpoint-switches and diodes.

The CMV is almost constant like H6-1 topology. The extra switches based on the F-B transformerless inverter topologies are used with almost the same techniques, that is, just changing the location of the diodes and bidirectional switches. Hence, the obtained CMV and i_{cm} are practically identical.

2.2.4. Buck-Boost Type Topologies

Buck-boost topologies are created by employing buck/boost and buck-boost topologies in the circuit to avoid the complexity of single-phase transformerless inverters. As a result, the i_{cm} can be reduced dramatically for some buck-boost topologies [69-70]. In some topologies like [117], there is a direct connection between the ground of the PV panel and load, and hence no leakage current will flow through the parasitic capacitor. However, their THD values might be high.

In [70], a boost converter is used at the front of the circuit that helps in reducing the minimum required input voltage level. In this topology, extra switches are used to clamp the mid-point voltage, and hence the CMV remains constant with a low level of i_{cm}.

On the other hand, when the output voltage falls below the peak grid voltage, the DC-DC converter is energised in a way to charge the second DC-link capacitor such that the total DC-link voltage becomes more than the peak grid voltage. Thus, the topology is also used to increase the voltage level into five levels through the DC-link capacitors. Further, a high gain DC-DC converter based topology that is connected with a doubly grounded voltage swing inverter is introduced in [72], which is able to reduce the components' voltage requirement. However, such a kind of topology utilises multiple stages and operates in high switching frequency which results in a low conversion efficiency. Moreover, the double PV panel is used with NPC and the generation control circuit (GCC) to increase the DC-link voltage in [69]. This circuit construction allows the operation of each PV string at a different current-voltage point which helps to avoid the partial shadowing problem. As a result, the maximum current of the most shaded PV module limits the current of the string. On the other hand, the output ground is directly connected to the mid-point of the DC-link capacitors, which is the main reason for getting low i_{cm}. The topology is implemented for 5 kW where the achieved efficiency is 96%. Moreover, the same technique is used in [68] and [7], and this obtains a low i_{cm} [72]. Table 2.3 summarises the major single input type transformerless inverter topologies in terms of CMV, leakage current, voltage stress and the number of components required which have all been analysed previously. Finally Table 2.4 presents the qualitative summary of the major single input type transformerless inverter topologies for selecting the best topology.

2.3. Single/low Input voltage ($\leq \mathbf{V_{PV}}$) Type single-phase Transformerless Inverter Topologies

The requirements of higher power quality with a minimal distortion factor is also essential especially in the industrial field which cannot be mitigated by a simple three-level inverter. Up to now, different converters are introduced for electricity network to connect

with PV panels, where the most suitable and applicable solution for both academic and industrial fields are multilevel inverter (DC power to AC power) due to its high power quality, accurate output waveform, low total harmonic distortion (THD) and reduced dv/dt stress [122], [123].

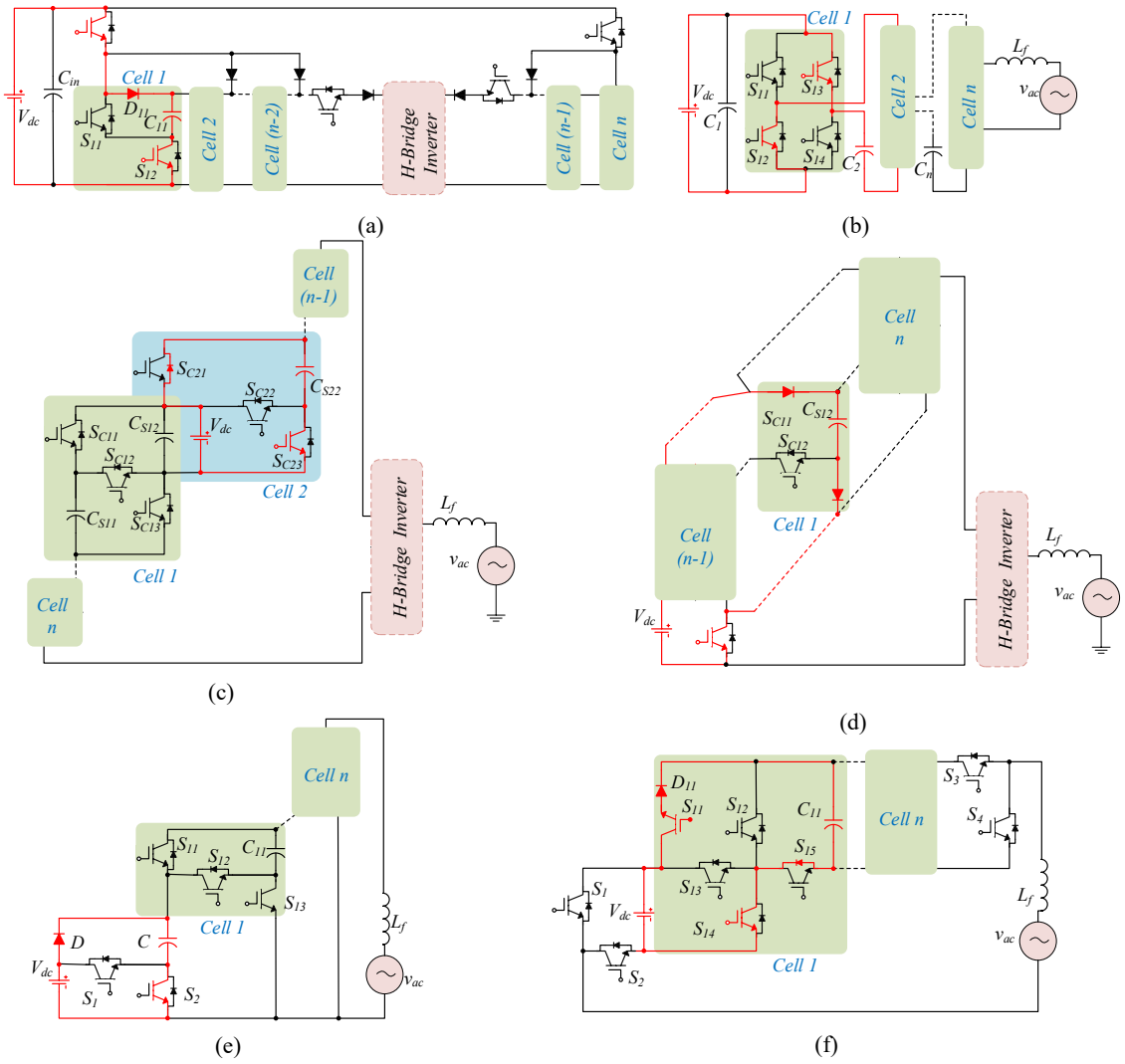


Fig. 2.39. Different SC-based multilevel inverter topologies, (a) topology in [73], (b) topology in [74], (c) topology in [75], (d) topology in [76], (e) topology in [77], and (f) topology in [127].

The most common types of multilevel inverters are diode clamped, cascaded H-bridge (CHB), and capacitor clamped. Among them, diode clamped and capacitor clamped types require high number of semiconductor devices and the dc-link series capacitor voltage is

unbalanced [124], [125]. On the other hand, above-mentioned topologies cannot be used in electric vehicles (EVs) and uninterruptible power supplies (UPS) due to incapability of providing boost feature. As a result, the recent trend in multilevel inverter focus in adding boosting feature to the inverter topologies. In [126], a five-level inverter topology presented that use a flying capacitor where the required input voltage is half of the dc link voltage. However, this topology is not capable of extending the voltage level. In [73], a new topology with boosting feature has been presented using SC, but one main drawback related to this circuit is that it is not capable of extending the voltage level due to the variation in input voltage. The first generation of the SC-based multilevel inverters are proposed in early 90's and up to now they are well developed, and many new topologies have been presented [73]-[77].

Fig. 2.39 shows six boost inverter topologies with reactive power capability based on SC structure leading to (2n+1)-levels inverters. Fig. 2.39 (a) is a topology that had proposed in 1998 [73], where each cell is required a large number of semiconductor devices (i.e. two MOSFETs, and two diodes) with one SC. Single-direction-balance mode or the bi-direction-balance mode based multilevel inverter has presented in Fig 2.39 (b) [74], where each cell require four power switches with one SC and the structure of this topology is based on H-bridge configuration. On the other hand, a smaller number of semiconductor devices are required in Fig. 2.39 (c) [75] and Fig. 2.39 (d) [76] topologies, respectively. The topology in Fig. 47 (d) suffers from high total voltage ratings on its components, called hereafter total standing voltage (TSV), compared to the topology in Fig. 2.39 (c). Moreover, huge number of power devices are required for topology in Fig. 2.39 (f) [127]. Fig. 2.39 (e) shows a multilevel inverter that require three power switches and a diode for each cell [77] where Fig. 2.39 (e) suffers from less amount of TSV compared with above presented topologies.

In this section a comparative analysis is carried out with the well-known SC-based inverters [73]-77], and [128]-[130] for multilevel. Table 2.5 shows the required number of SC, and semiconductor devices for mentioned topologies where proposed topology required 3(n-1) number of switches per cell and peak output voltage is depended on duty ratio for proposed topology. Moreover, the voltage stress of the each device is showed for n cells.

2.4. Thermal Analysis of single-phase Transformerless Inverter Topologies

2.4.1. Thermal Parameter

Inverters are operated in a wide range of temperatures and their operating temperature affects the overall system cost and efficiency. Therefore, thermal analysis is an important aspect for the technical analysis of a power electronics system as this affects the required heat sink size, cooling system and thermal protection of the switches [131]-[139]. The temperature needs to be considered for each semiconductor device from junction temperature (T_j) to case temperature (T_c). Fig. 2.40 shows the thermal impedance model which is related to the temperature and Fig. 2.41 shows the thermal equilibrium model of semiconductor devices.

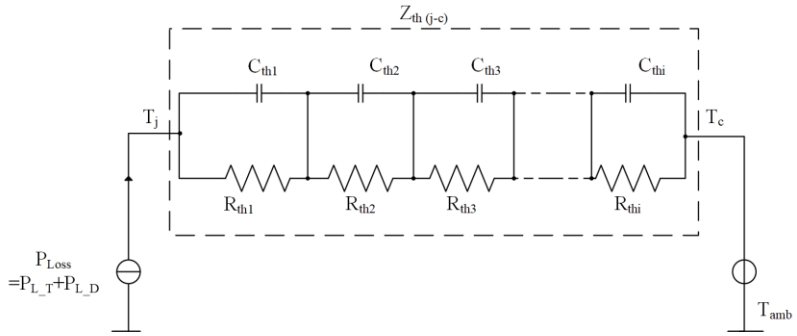


Fig. 2.40. Thermal impedance Foster- model used in circuit design.

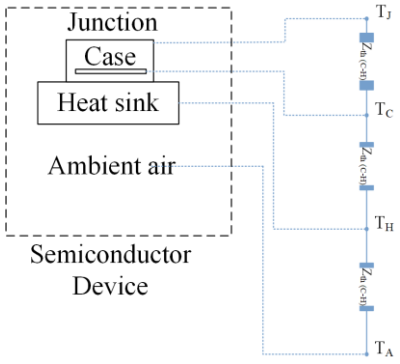


Fig. 2.41. The equilibrium of thermal model.

The junction temperature depends on thermal capacities C_{th} and thermal resistances R_{th} through the following equations.

$$R_{th} = \frac{T_j}{\rho} = \frac{T_j}{Q/t} \tag{9}$$

where ρ is the heat flow, Q is the flowing heat, and t is the time,

$$\frac{1}{C_{th}} = \frac{T_j}{Q} \tag{10}$$

The total impedance is

$$Z_{thi}(t) = \frac{\Delta T}{P} = \sum_{i=1}^{n} R_{thi}(1 - e^{-\frac{t}{\tau_{thi}}}) \tag{11}$$

where ΔT is the temperature between different nodes in the system, n is the number of exponential terms to fit $Z_{th}(t)$ to the transient thermal impedance curve, P is the power dissipation, and

$$\tau_{thi} = R_{thi}.C_{thi} \tag{12}$$

On the other hand, the power losses (IGBT (P_{L_T}) + diode (P_{L_D})) are dependent on the junction temperature and case temperature as shown in (13).

The junction temperature can be expressed as follows

$$T_j = \mathrm{P_{Loss}}.Z_{th(j-c)} + T_c \tag{13}$$

The junction temperature of the IGBT can be calculated by the following equation

$$T_{j-IGBT} = T_H + \mathrm{P_{avg.IGBT\ Loss}}(\mathrm{R_{th-IGBT}} + \mathrm{R_{th(ch-IGBT)}}) \tag{14}$$

The junction temperature of the diode can be calculated by the following equation

$$T_{j-diode} = T_H + \mathrm{P_{avg.Diode\ Loss}}(\mathrm{R_{th-diode}} + \mathrm{R_{th(ch-diode)}}) \tag{15}$$

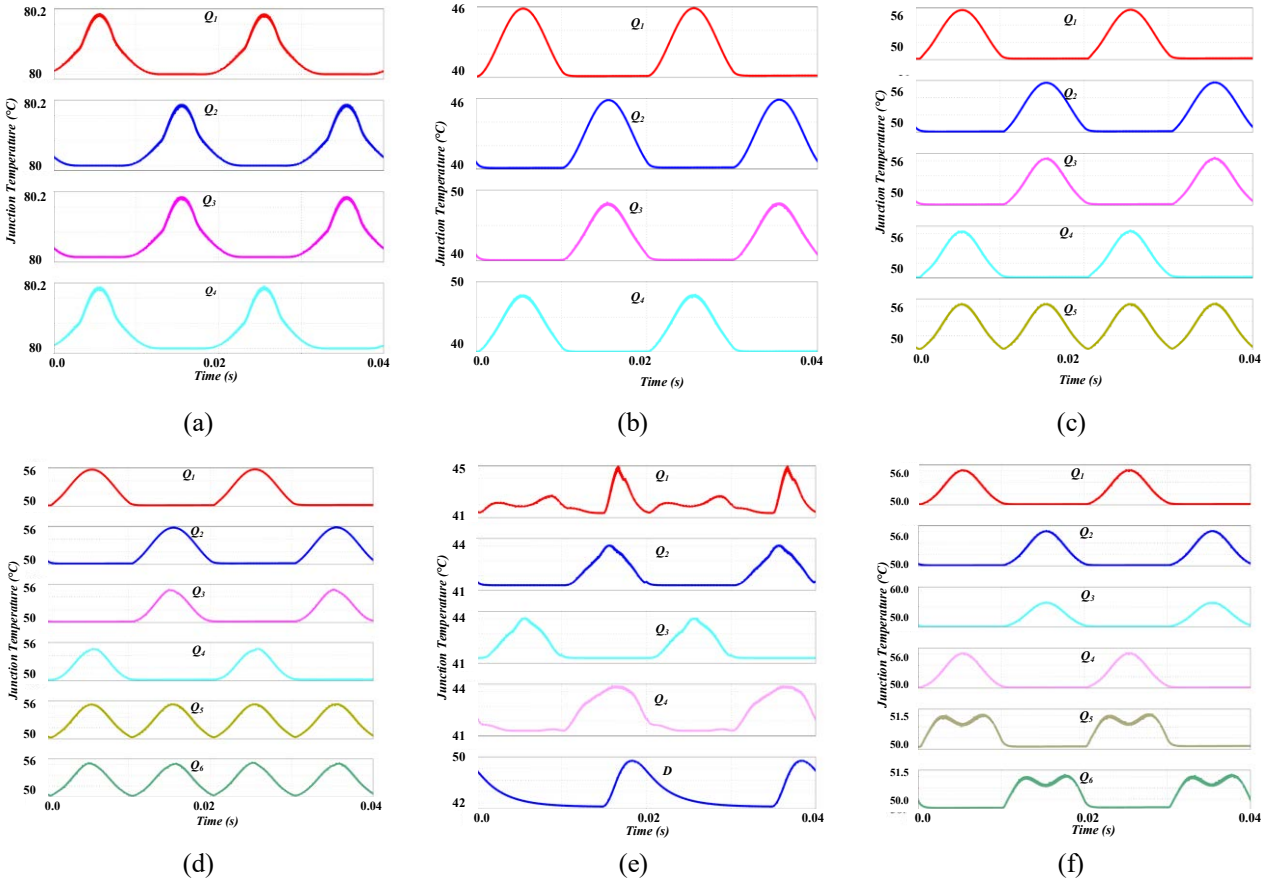
The heatsink temperature can be found as given in (16).

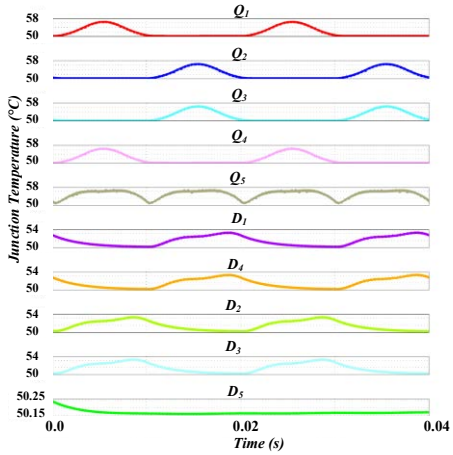
$$T_H = T_{amb} + \mathrm{R_{th-H}}(\mathrm{P_{avg.IGBT\ Loss}} + \mathrm{P_{avg.Diode\ Loss}}) \tag{16}$$

where T_{amb} represents the ambient temperature, and $\mathrm{R_{th-H}}$ stands for the thermal resistance between the heat sink and the environment.

2.4.2. Relation Between Junction Temperature with Semiconductor Devices

Fig. 2.42 illustrates the junction temperature curves of the semiconductors in turn-ON and turn-OFF conditions. The maximum junction temperature is related to the bipolar F-B inverter [62], and hence the maximum losses occur through the switches, which are almost identical for all switches (see Fig. 2.42 (a)). The junction temperature is dramatically reduced for all switches in the unipolar F-B inverter, where two switches (Q_1 and Q_2) are operated at a slightly lower temperature than the other two switches (Q_3 and Q_4); see Fig. 2.42 (b). Fig. 2.42 (c) and Fig. 2.42 (d) illustrate the junction temperature curves for H5 and H6 DC side semiconductor devices. In these topologies, the additional switches (Q_5 and Q_6) represent an increase in the junction temperature in both turn-ON and turn-OFF conditions according to the switching pulses.





(g)

Fig. 2.42. Semiconductor devices junction temperature curves in switching intervals, (a) Bipolar F-B topology, (b). Unipolar F-B topology, (c) H5 topology, (d) H6 DC side topology, (e) Topology in [5], (f). HERIC topology, and (g) HB-ZVR topology.

The topology presented in [5] demonstrates the lowest junction temperature and loss among the evaluated topologies (see Fig. 2.42 (e)). Moreover, the junction temperature curves for semiconductor switches in HERIC and HB-ZVR topologies are illustrated in Fig. 2.42 (f) and Fig. 2.42 (g), respectively.

2.4.3. Loss Calculation

The loss analysis is verified through simulations for seven major topologies using the parameters listed in Table 2.1. The values of the individual devices are taken from the datasheets [134]-[135]. The power losses of the semiconductor switches are comprised of conduction losses and switching losses. Similarly, for diodes, the power losses comprise conduction and reverse recovery. The mathematical expressions of the losses of IGBT (conduction loss and switch turn-ON/OFF loss) and the diode (conduction loss and reverse recovery loss) are adopted from [115-121]. As discussed, the conduction losses of the semiconductor devices depend on the ON-state voltage $V_{ON}(t)$, and the instantaneous current *i(t)* [140]-[144].

The conduction losses or the ON-state losses are disclosed in (17) where the inverter fundamental period is T, and ON-state voltage is V_{ON} with the instantaneous current I_{ce} which is the IGBT collector emitter-current.

$$P_{\text{conduction loss}} = \frac{1}{T}\int_0^T (V_{ON}(t) \times I_{ce}(t))dt \quad (17)$$

The ON-state voltage (18) is the voltage across the collector and emitter; this voltage depends on the internal series resistance (r_T). In the time of conduction losses through the antiparallel diode of the switches, the diode current (I_D) flows through the internal diode resistance as shown in (19).

$$V_{ON}(t) = V_T(t) + r_T\, I_{ce}(t) \quad (18)$$

$$V_{ON}(t) = V_D(t) + r_D\, I_D(t) \quad (19)$$

On the other hand, the conduction losses of the diode occur at the active state through the forward voltage V_F and freewheeling current I_F as shown in (20) [35].

$$P_{\text{conduction loss}} = \frac{1}{T}\int_0^T \big(V_F(t) \times I_F(t)\big)dt \quad (20)$$

The turn-ON energy losses can be calculated by (21),

$$E_{ON} = E_{ON.T} + E_{ON.FD} \quad (21)$$

where $E_{ON.T}$ is the switch turn-ON energy without reverse recovery process, and $E_{ON.FD}$ is the switch turn-ON energy by considering the reverse recovery process. The peak reverse recovery current (I_{PRR}) is given in (22),

$$I_{PRR} = \frac{2 * Q_{RR}}{T_{RR}} \quad (22)$$

where T_{RR} is the reverse recovery time. Now, the diode reverse recovery losses are dependent on the reverse recovery energy $E_{ON.D}$ and diode voltage at the time of reverse recovery $V_{RR.D}$.

$$E_{ON.D} = \frac{1}{4} \times Q_{RR} \times V_{RR.D} \quad (23)$$

For the turn-OFF energy, the reverse recovery effect is negligible. From (18) and (21), the total turn-ON and OFF losses of the switches are obtained by (24).

$$E_T = E_{ON} + E_{ON.FD} + E_{OFF} \quad (24)$$

The total switching losses for the IGBT ($P_{IGBT.T}$) are

$$P_{IGBT.T} = \frac{I}{T}\sum_{n=1}^{\frac{f_{sw}}{f}}(E_{ON}(n)) + E_{ON.FD}(n) + E_{OFF}(n)) \quad (25)$$

where f_{sw} is the switching frequency. The reverse recovery losses for diode is

$$P_{D.T} = \frac{I}{T}\sum_{n=1}^{\frac{f_{sw}}{f}}(E_{ON}.D(n)) \quad (26)$$

The total IGBT losses are expressed in (27) for IGBT and (28) for the diode from (20), (23), (25), and (26)

$$P_{avg.IGBT\ Loss} = P_{turn\ ON\ loss} + P_{turn\ OFF\ loss} + P_{conduction\ loss}$$
$$= \frac{I}{T}\sum_{n=1}^{\frac{f_{sw}}{f}}(E_{ON}(n)) + E_{ON.FD}(n) + E_{OFF}(n)) + \frac{1}{T}\int_0^T (V_{ON}(t) \times I_{ce}(t))dt \quad (27)$$

$$P_{avg.Diode\ Loss} = P_{reverse\ recovery} + P_{conduction\ loss}$$
$$= P_{D.T} = \frac{I}{T}\sum_{n=1}^{\frac{f_{sw}}{f}}(E_{ON}.D(n)) + \frac{1}{T}\int_0^T \big(V_F(t) \times I_F(t)\big)dt \quad (28)$$

From (14) and (27), the total temperature for IGBT losses can be expressed as given in (29), and from (15) and (28), the total temperature for diode losses can be expressed in (30).

$$T_{j-IGBT} = T_H + (\frac{I}{T}\sum_{n=1}^{\frac{f_{sw}}{f}}(E_{ON}(n)) + E_{ON.FD}(n) + E_{OFF}(n)) + \frac{1}{T}\int_0^T (V_{ON}(t) \times I_{ce}(t))dt)(R_{th-IGBT} + R_{th(ch-IGBT)}) \quad (29)$$

$$T_{j-diode} = T_H + P_{D.T}$$
$$= \frac{I}{T}\sum_{n=1}^{\frac{f_{sw}}{f}}(E_{ON}.D(n)) + \frac{1}{T}\int_0^T (V_F(t) \times I_F(t))dt)(R_{th-diode} + R_{th(ch-diode)}) \quad (30)$$

The power losses of each semiconductor device of the major transformerless topologies ([5], H5, H6 DC side, HERIC, and HB-ZVR) are shown graphically in Fig. 2.43. It is clear that the maximum power losses are associated with the FB bipolar topology. On the other hand, the lowest power losses in the semiconductor devices are achieved by the topology in [5] and the HERIC topology.

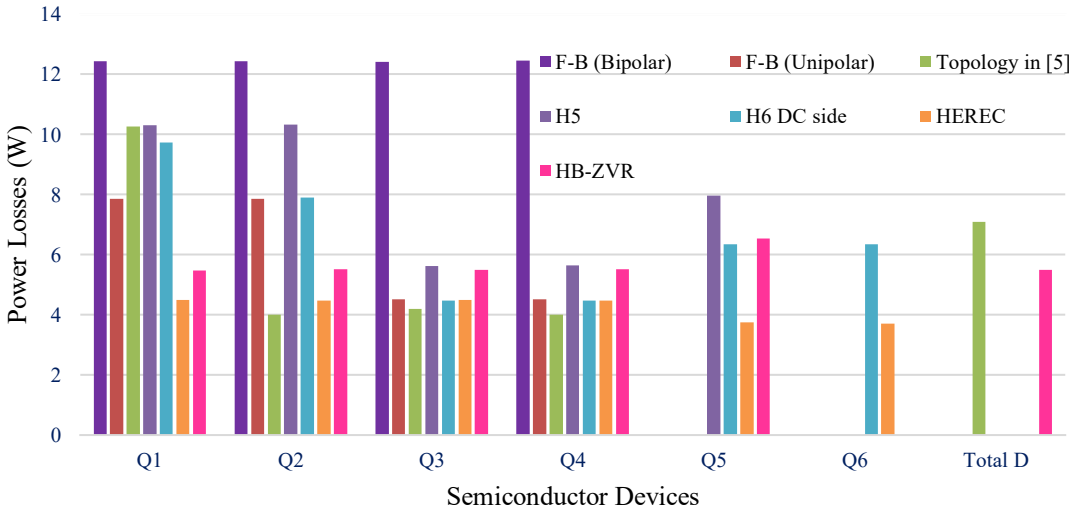


Fig. 2.43. Comparison of power losses for some of the transformerless inverter topologies for 1.8 kW rated power.

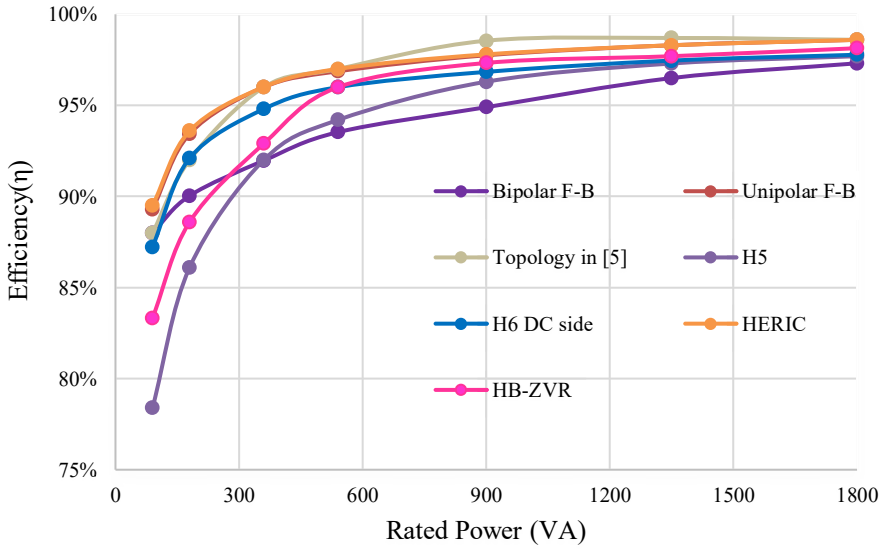
2.4.4. Efficiency Evaluation

The maximum efficiency is achieved by the topology in [5] (see Fig. 2.13 (b)) which is 98.06 % when selecting California Energy Commission (CEC) weighted efficiencies for calculation formula, and 97.36 % when selecting the European (EU) weighted efficiencies. The formula for calculating the overall efficiencies are given in (31) and (32) for EU and CEC

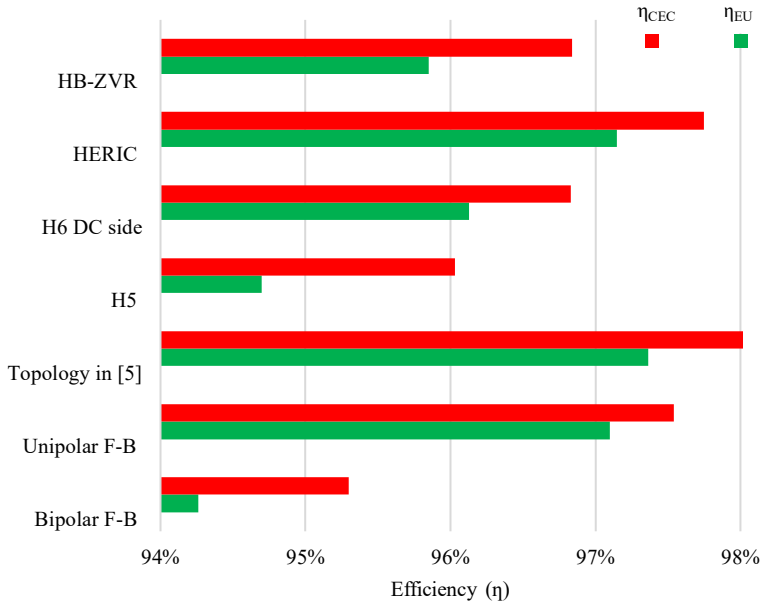
weighted efficiencies respectively. Fig. 3.44 illustrates the efficiency curve for different ranges of the output power as well as the overall efficiency.

$$\eta_{EU} = 0.03.\ \eta_{5\%} + 0.06.\ \eta_{10\%} + 0.13.\ \eta_{20\%} + 0.10.\ \eta_{30\%} + 0.48.\ \eta_{50\%} + 0.20.\ \eta_{100\%} \quad (31)$$

$$\eta_{CEC} = 0.04.\ \eta_{10\%} + 0.05.\ \eta_{20\%} + 0.12.\ \eta_{30\%} + 0.21.\ \eta_{50\%} + 0.53.\ \eta_{75\%} + 0.05.\ \eta_{100\%} \quad (32)$$



(a)



(b)

Fig. 2.44. Efficiency evaluations for major transformerless inverter topologies, (a) efficiency curves vs. output power, and (b) CEC and EU efficiencies.

2.5. Summary

Various transformerless inverter topologies are presented with operating principle. Each topology simulated to analyse the CM effect and output wave form. Indeed, the topologies are summarized in Table 2.3, Table 2.4, and Table 2.5. On the other hand, thermal analysis has done for major single-phase transformerless inverter topologies. It shows the relationship between the junction temperature and time for each semiconductor devices. Further simulated the system through the PLECE software and design the thermal model through the semiconductor device data sheet for getting accuracy. Moreover, presents the equations for loss calculation of each devices for 1.8 kW rated power. Finally evaluated the efficiency for different output power and presented the maximum efficiencies for both California Energy Commission (CEC) and the European (EU) calculation formula.

Table 2.3. Summary of Single Input Voltage Type Transformerless Inverters

pology Name	Semiconductor Devices		No. of C*	No. of L	Common Mode Current i_{cm} (mA)	Common Mode Voltage CMV (V)	Passive Filter		Output Voltage Level	Reported PF	Reported THD, (%)	Cost#	Reported Efficiency, η (%)
	No. of IGBTs	No. of Diodes					No. of C	No. of L					
Bipolar F-B [62]	4	0	1	0	≤ 55	199 to 201	1	2	2	Unity	N/A	+	95.2 @ 5 kVA
Unipolar F-B [61, 108]	4	0	1	0	≤ 1800	200 to 400	1	2	3	Unity	N/A	+	98.0@3 kVA
Inverter topology in [12]	5	0	2	0	≈ 0	constant	1	1	3	0.94	2.1	++	95.20 @ 0.5 kVA
S4 Topology [42]	4	2	3	0	≈ 0	constant	1	1	3	0.8	2.1	++	97.2 @ 0.5 kVA
Siwakoti-H [16]	4	1	2	0	≈ 0	constant	1	1	3	0.85	< 2.3	++	97.8 @ 1 kVA
Inverter topology in [5]	4	1	2	0	≈ 0	constant	1	1	3	0.85	< 2	++	99.25 @ 1 kVA
Inverter topology in [43]	4	1	2	0	≈ 0	constant	1	1	3	0.9	< 2.2	++	99.2 @ 1 kVA
Inverter topology in [44]	5	0	2	1	≈ 0	constant	1	1	3	Unity	N/A	++	95 @ 200 VA
Karschny [45]	5	2	2	1	≈ 0	constant	1	1	3	Unity	N/A	+++	N/A
iH5/oH5 [10]	6	0	2	0	≤ 20	199.89 to 200	1	2	3	Unity	N/A	++	96.9 @ 1 kVA
oH5-1 [37]	6	2	2	0	≤ 200	200 to 248	1	2	3	Unity	N/A	+++	N/A
oH5-2 [37]	6	0	2	0	≤ 200	198to 249	1	2	3	Unity	N/A	++	97.16 @ 5

													kVA
H5-D [38]	5	1	2	0	≤ 50	185to 195	1	2	3	Unity	4.888	++	95@650 VA
HERIC Active 1 [39]	7	2	2	0	≤ 25	199.93 to 200	1	2	3	N/A	N/A	++++	N/A
HERIC Active 2 [39]	7	0	2	0	≤ 25	199.96 to 200	1	2	3	N/A	1.7	++++	97 @ 2 kVA
HERIC Active 3 [39]	6	4	2	0	≤ 25	199.91 to 200	1	2	3	Unity	N/A	++++	N/A
PN-NPC [40]	8	0	2	0	≤ 35	199.3 to 201.1	1	2	3	Unity	N/A	++++	97.2 @ 1 kVA
HB-ZVR [9]	5	5	2	0	≤ 200	163 to 200	1	2	3	Unity	N/A	+++	94.88 @ 2.8 kVA
HB-ZVR-D [41]	5	6	2	0	≤ 40	199.89 to 200	1	2	3	Unity	1.9	+++	95.03 @ 1 kVA
HERIC [31]	6	0	1	0	≤ 200	165 to 235	1	2	3	Unity	N/A	++	97.1 @ 2 kVA
HERIC AC based [31]	6	2	1	0	≤ 200	165 to 236	1	2	3	Unity	N/A	+++	N/A
H5 [32]	5	0	1	0	≤ 200	159 to 235	1	2	3	Unity	N/A	++	98.50 @ 0.5 kVA
CH5 [113]	5	5	1	2	≤ 50	N/A	1	2	3	Unity	2.69		N/A
H6 DC side [29]	6	0	2	0	≤ 200	151 to 249	1	2	3	Unity	1.585	++	95.9 @ 1kVA
H6 DC side improved-1 [33]	6	0	1	0	≤ 1000	200 to 400	1	2	3	Unity	N/A	++	N/A
H6 DC side improved-2 [33]	6	0	1	0	≤ 1000	200 to 400	1	2	3	Unity	N/A	++	N/A
H6 in mid diodes-1 [34]	6	2	1	0	≤ 200	159 to 240	1	2	3	0.9937	1.86	++	97.33 @ 1 kVA
H6 with diodes-2 [34]	6	2	1	0	≤ 200	150 to 249	1	2	3	Unity	N/A	+++	97.31 @ 1 kVA
Improved H6 in mid diodes-1 [64]	6	2	1	0	≤ 20	190 to 200	1	2	3	0.9	N/A	+++	96.5 @ 4 KVA
H6 -1 [35]	6	0	1	0	≤ 200	151 to 258	1	2	3	Unity	1.7	++	97.22 @ 1 kVA
H6 in mid switch [36]	6	0	1	0	≤ 200	159 to 240	1	2	3	Unity	N/A	++	N/A
Hybrid bridge [30]	6	2	1	0	≤ 250	158 to 241	1	2	3	Unity	N/A	+++	94.75 @ 1 kVA
ZCT-H6-1 [65]	8	3	4	2	≤ 250	N/A	1	2	3	Unity	N/A	++++	95.6 @ 1 kVA
SLF-H6-1 [66]	8	2	4	2	≤ 150	N/A	1	2	3	Unity	N/A	++++	96.25@ 1 kVA
Inverter topology in [67]	4	2	1	0	≤ 150	N/A	1	6	3	0.9	3.6	++++	98.2 @ 2 kVA
Inverter topology in [68]	6	0	2	0	≤ 250	N/A	1	3	3	Unity	< 4.5	+++	94.8 @ 1.5 kVA

GCC-NPC [69]	6	2	2	1	≤ 20	N/A	1	1	3	Unity	4.08	++++	95.7 @ 2 kVA
Inverter topology in [70]	8	1	2	1	≤ 20	N/A	1	2	3	Unity	4.2	++++	96.11@ 220 VA
Inverter topology in [7]	8	0	2	0	≤ 20	N/A	2	2	3	Unity	4.35	++++	96@ 1 kVA
Inverter topology in [71]	6	2	1	1	≤ 150	N/A	1	2	3	Unity	N/A	+++	97.5@ 2 kVA
Inverter topology in [119]	8	4	4	2	≤ 100	N/A	1	3	3	Unity	< 4.61	++++	97.02@ 1.5 kVA
Inverter topology in [72]	7	3	4	4	≤ 100	N/A	1	1	3	0.7	N/A	++++	94.09@ 300 VA
Inverter topology in [120]	4	0	2	1	≤ 200	N/A	1	1	3	0.7	2.1	+++	95.8@ 100 VA
Inverter topology in [50]	6	0	3	0	≤ 20	N/A	1	3	3	0.95	N/A	+++	N/A
Inverter topology in [121]	5	2	4	2	≤ 40	N/A	0	1	3	Unity	N/A	++++	N/A

* including the input capacitor

The more "+" represents the higher cost, + ≡ low, ++ ≡ medium, +++ ≡ high, and ++++ ≡ extremely high.

In the above table, "C" represents capacitor, "L" represents inductor, "PF" power factor, "THD" total harmonic distortion`

Table 2.4. Qualitative Summary of the Major Single-Phase Transformerless Inverter Topologies

Transformerless Inverter Topologies	**Advantages**	**Disadvantages**	**Reactive Power Capability**	**Size of the Inverter**	**Efficiency**	**Recommended Topology**
Common Ground Type Topologies	▪ No CM effect. ▪ Less semiconductor devices are used. ▪ Small filter required.	▪ Flying capacitor or switched capacitor or flying inductor controlling is difficult.	Yes	Small	Very high	Inverter topology in [5]
Mid-Point Clampling	▪ Constant CMV and low i_{cm}.	▪ Increased complexity. ▪ More semiconductor devices.	Yes	Large	Medium	HERIC Active 2 [39]

AC-Decoupling	▪ Low Conduction losses. ▪ Output current does not flow through the antiparallel diodes of F-B. ▪ Lower THD.	▪ Additional switches required. ▪ Residual line frequency leakage current.	Yes	Medium	High	HERIC [31]
DC-Decoupling	▪ DC bypass switch helps to disconnect PV from the grid during leakage current.	▪ High conduction losses. ▪ Additional devices required. ▪ Unbalanced switching.	Yes	Medium	Medium	H5 [32]
H6 Type Topologies	▪ Low output current ripple.	▪ Complex control. ▪ More semiconductor devices. ▪ CMV fluctuates.	Yes (except H6 with diodes-1 and H6 with diodes-2)	Large	Medium	H6-1 [35]
Buck-Boost Type Topologies	▪ Low i_{cm}	▪ High THD	Yes	Large	Medium	Inverter topology in [71]

Table 2.5.Comparison of Basic Parameters in Various Switched-Capacitor Type Multilevel Inverter

Topologies	**No. of components**				**Output voltage levels**	**Peak of ac output voltage ($\hat{v}_{ac}$)**	**Voltage stress on**				**Inrush/ spike current**
							Switched capacitor n/w			**H-bridge switch**	
	C	**D**	**S**	**L**			**C**	**S**	**D**		
Topology in [73]	$n-1$	$2n$	$2(n-1)$	0	$2n+1$	$\mp(n-1)V_{dc}$	$(n-1)V_{dc}/n$	$(n-1)V_{dc}/n$	$(n-1)V_{dc}/n$	$(n-1)V_{dc}$	Yes
Topology in [74]	$n-1$	0	$4(n-1)$	0	2^n+1	$\mp 2^{n-1}V_{dc}$	$2^{n-1}V_{dc}/n$	$2^{n-1}V_{dc}/n$	NA	$2^{n-1}V_{dc}$	Yes
Topology in [127]	$n-1$	$n-1$	$5(n-1)$	0	$2n+1$	$\mp(n+1)V_{dc}$	$(n+1)V_{dc}/n$	$(n+1)V_{dc}/n$	$(n+1)V_{dc}/n$	NA	Yes
Topology in [75]	$n-1$	0	$3(n-1)$	0	$4n-1$	$\mp(n+1)V_{dc}$	$(n+1)V_{dc}/n$	$(n+1)V_{dc}/n$	NA	$(n+1)V_{dc}$	Yes
Topology in [76]	$n-1$	$2n-2$	$n-1$	0	$2n+1$	$\mp(n+1)V_{dc}$	$(n+1)V_{dc}/n$	$(n+1)V_{dc}/n$	$(n+1)V_{dc}/n$	$(n+1)V_{dc}$	Yes
Topology in [77]	$n-1$	$n-1$	$3(n-1)$	0	2^n	$\mp 2^n V_{dc}$	$2^n V_{dc}/n$	$2^n V_{dc}/n$	$2^n V_{dc}/n$	$2^n V_{dc}$	Yes
Topology in [128]	n	$n+1$	$2(n+1)$	1	$2n+1$	$\mp V_{dc}$	V_{dc}/n	V_{dc}/n	V_{dc}/n	V_{dc}	No
Topology in [129]	$n-1$	$n-1$	$2(n-1)$	0	$2n+1$	$\mp(n+1)V_{dc}$	$(n+1)V_{dc}/n$	$(n+1)V_{dc}/n$	$(n+1)V_{dc}/n$	$(n+1)V_{dc}$	Yes
Topology in [130]	$n-1$	0	$3(n-1)$	0	2^n	$\mp 2^n V_{dc}$	$2^n V_{dc}/n$	$2^n V_{dc}/n$	NA	$2^n V_{dc}$	Yes

Chapter 3

H-Bridge Zero-Voltage Switch Controlled Rectifier (HB-ZVSCR) Transformerless Mid-Point-Clamped Inverter (Proposed Topology I)

3.1. Circuit Structure

A new topology called H-Bridge Zero Voltage switch controlled Rectifier (HB-ZVSCR) is proposed as shown in Fig. 3.1. The circuit consists of two switches and a full bridge rectifier which clamp the AC terminal to the DC midpoint (consisting of two DC-link capacitors (C_1 and C_2)) during the freewheeling period. This topology is modified topology of both HB-ZVR [9] and HB-ZVR-D [41].

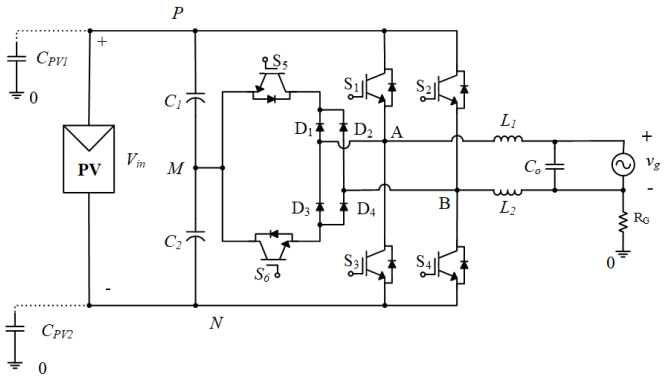


Fig. 3.1. The proposed transformerless inverter circuit.

The proposed topology replace two diodes of the HB-ZVR-D with two extra switches and eliminates the bidirectional switches which alleviate the loss. The freewheeling path is created by the bridge rectifier and extra switches (S_5 and S_6), during the zero voltage vector the mid-point of the DC-link is clamped to the ac terminals which bypass the flow of leakage current to the grid.

3.2. Operating Principles

According to the operating principle of the proposed HB-ZVSCR topology, there are four operating modes. Mode 1, and Mode 3 operates in the positive half-period of grid voltage, and Mode 2, and Mode 4 operates in the negative half-period. Fig. 3.2 (a) shows the mode 1. S_1 and S_4 are ON while S_2 and S_3 are OFF. Current increases and flows through S_1, S_4, and load where positive DC-link voltage ($+V_{PN}$) appears across the filter capacitor.

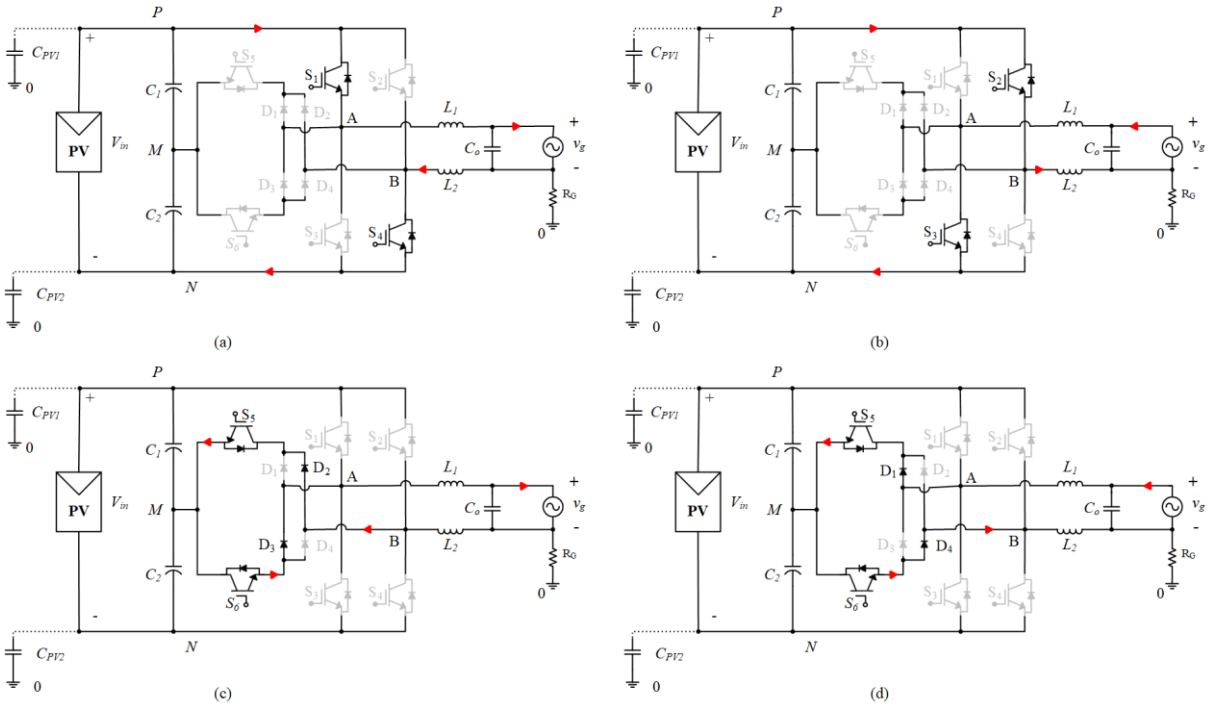


Fig. 3.2. Operating modes of HB-ZVSCR inverter, (a) mode 1, (b) mode 2, (c) mode 3, and (d) mode 4.

In mode 2, S_2 and S_3 are an active while S_1 and S_4 are OFF (see Fig. 3.2 (b)). The output voltage is equal to the negative DC-link voltage ($-V_{PN}$). In mode 3, and mode 4 are the freewheeling path for positive half-period and negative half-period demonstration in Fig. 3.2

(c) and Fig. 3.2 (d) respectively where the bridge diodes are working in alternatively. In positive freewheeling time (see Fig. 3.2 (c)), switches S_5 and S_6 are conducted with diodes D_2, D_3. Fig. 3.2 (d) shows the negative half cycle freewheeling path, where the output current goes through D_1, D_4 and the switches S_5 and S_6.

3.3. Modulation Strategies

A unipolar sinusoidal pulse width modulation (SPWM) technique is employed in the proposed HB-ZVSCR topology which is shown in Fig. 3.3.

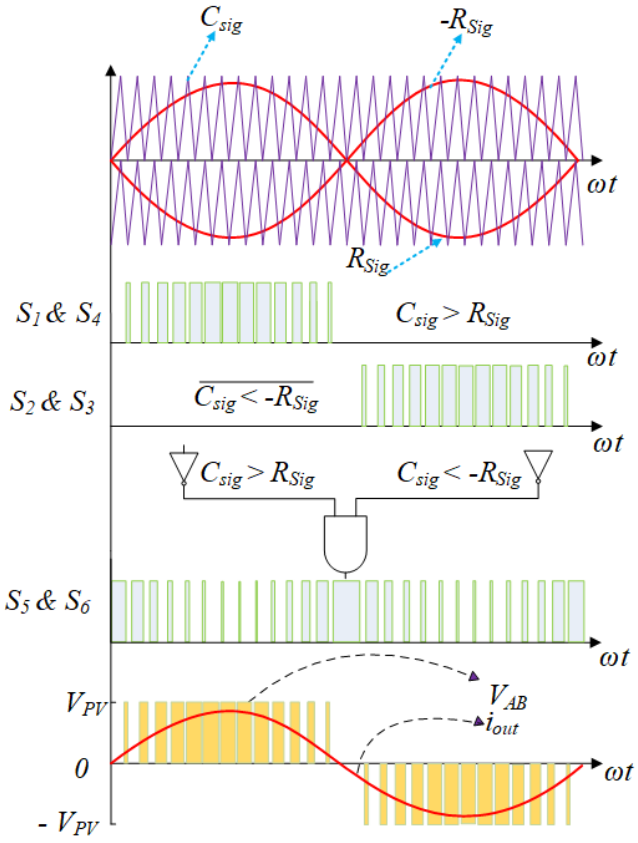


Fig. 3.3. PWM modulation for proposed topology.

The modulation signal can be written as follows,

$$R_{Sig} = A \sin\omega_s t \tag{33}$$

where A is the maximum amplitude value of the reference waveform, ω_s is the angular frequency.

$$M = \frac{A}{N} < 1 \tag{34}$$

The maximum amplitude of a carrier signal (N) is 1 and the modulation index as (34);

The reference signal is compared with the triangular carrier signal. In the positive half-period, S_1 and S_4 have the same driving signals, and S_5 and S_6 have the opposite driving signals. In the negative half-period, S_2 and S_3 have the same driving signals, and S_5 and S_6 have the opposite driving signals.

3.4. Common Mode effect

In order to investigate the ground leakage current (i_{cm}), the equivalent CM circuit is presented in Fig. 3.4 where M is the mid-point clamping point which comprises the converter, filter inductors (L_1, L_2), and parasitic capacitor (C_{pv}). The power circuit can be replaced with phase voltages of the inverter V_{AN} and V_{BN} which are equal to the potential of A and B points relative to the neural point N[14], and [15]-[18].

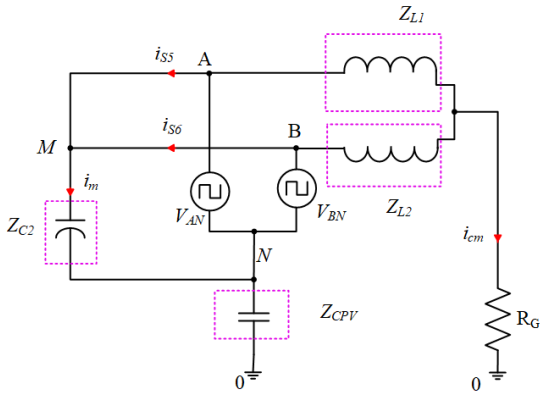


Fig. 3.4. CM equivalent circuit of the proposed PV inverter.

The CMV and differential-mode voltage (DMV) can be written based on the phase voltages as follows:

$$V_{CMV} = \frac{V_{AN} + V_{BN}}{2} \tag{35}$$

$$V_{DMV} = V_{AN} - V_{BN} \tag{36}$$

Moreover, the phase voltages can be expressed based on V_{CMV} and V_{DMV} as mentioned in (37) and (38).

$$V_{AN} = V_{CMV} + \frac{V_{DMV}}{2} \tag{37}$$

$$V_{BN} = V_{CMV} - \frac{V_{DMV}}{2} \tag{38}$$

Voltage at point "B" to "N" and "A" to "N" is zero for the proposed topology at positive and negative half cycle respectively, so the common mode voltage (CMV) is achieved half of the DC-link voltage (see equation (39)-(41)).

$$V_{CMV}(\text{positive half cycle}) = \frac{V_{PN} + 0}{2} = \frac{V_{PN}}{2} \tag{39}$$

$$V_{CMV}(\text{negative half cycle}) = \frac{0 + V_{PN}}{2} = \frac{V_{PN}}{2} \tag{40}$$

$$V_{CMV}(\text{zero Vector states}) = \frac{\frac{V_{PN}}{2} + \frac{V_{PN}}{2}}{2} = \frac{V_{PN}}{2} \tag{41}$$

The equivalent CMV (V_{ECMV}), and leakage current (i_{cm}) show in Fig. 54, and Fig.5,

$$V_{ECMV} = V_{CMV} + \frac{V_{DMV}}{2} \times \frac{L_2 - L_1}{L_1 + L_2} \tag{42}$$

$$i_{cm} = \frac{V_{ECMV}}{Z_{EQU}} = \frac{V_{ECMV}}{Z_{C2} + (Z_{CPV}) + (Z_{L1} // Z_{L2}) + R_G} \sim i_m \tag{43}$$

$$i_m = i_{S5} - i_{S6} \tag{44}$$

where, $Z_{CPV} = (Z_{CPV1} // Z_{CPV2})$.

The maximum leakage current flows during the freewheeling time due to non-separation between PV panel, and grid at freewheeling time. Hence, the mid-point clamping connection is helping to get the path (see Fig. 1.6, and Fig. 1.7). This circuit can be demonstrated in the

s-domain to analyse the frequency and magnitude of the created resonant circuit (see Fig. 3.4 (c)). Letting $L_1 = L_2$ in (42) for the topologies with symmetrical structure (e.g. H-bridge), the equivalent CMV can be replaced with V_{CMV}. The transfer function from i_{cm} to CMV created by the converter through the resonant circuit can be expressed as (45-46).

$$V_{ECMV}(s) - \left(L_f s + \frac{1}{sC_{PV}}\right) i_{cm}(s) = 0 \tag{45}$$

$$H(s) = \frac{i_{cm}(s)}{V_{ECMV}(s)} = \frac{s}{L_f s^2 + \frac{1}{C_{PV}}} \tag{46}$$

In (45) and (46), $L_f = (L_1 L_2)/(L_1 + L_2)$. Fig. 3.5 illustrates the Bode plot of the transfer function in (46) considering $L_1 = L_2$ =2.6 mH and C_{PV} =68 to 330 nF. It shows the changing resonant frequency values based on C_{PV} but the magnitude remain almost same.

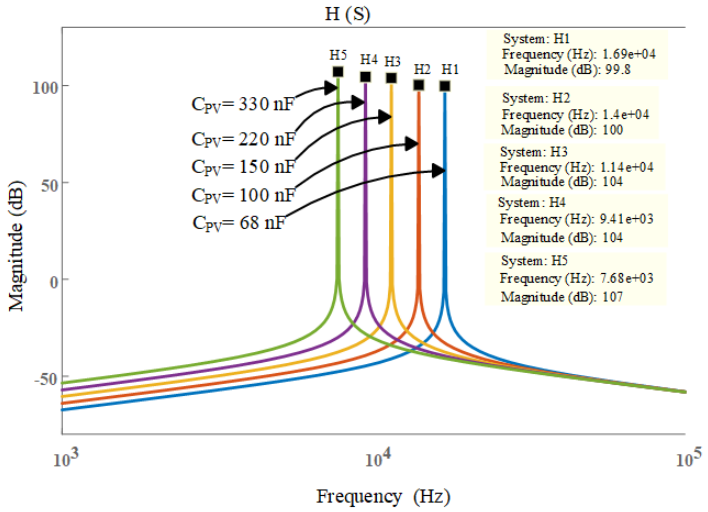


Fig. 3.5. Bode plot of the resonant circuit model in Fig. 3.4.

It is evident that the resonant frequency is varying from 7.68×10^3 to 16.9×10^3 Hz for different parasitic capacitor from 68 to 330 nF. Moreover, as the filter inductor and parasitic capacitor forms a typical LC resonant circuit, its resonant frequency can be calculated theoretically from (47). Both the simulation and analytical results show the equal resonant frequency, with which a large CM current i_{cm} flows into the system.

$$f_r = \frac{1}{2\pi\sqrt{L_f C_{PV}}} \tag{47}$$

Without a galvanic isolation, the potential between the PV array and the ground (V_{ECMV}) fluctuates which charges and discharge the parasitic capacitor (C_{pv}). This fluctuating CMV activates the resonant circuit as discussed above and may lead to higher ground leakage current. However, the resonant frequency is not fixed, as it depends on the parasitic capacitance together with the DC-link that connects the PV array to the inverter. It also depends on the size of the PV array and the environmental conditions. All these conditions make the elimination of leakage current more difficult in practice.

3.5. Design Guidelines

A design guideline is helpful in estimation and selection of the parameters for the practical design. First of all, the voltage and current rating of the active switches and diodes must be selected just above than the safety margin. Even though input DC-link capacitor helps to maintain a constant voltage at the DC-link, there are some small spikes in practice across the semiconductor devices. As a result, the voltage and current rating of the selected semiconductor devices are 650 V, and ≥ 50 A accordingly.

To select the components of the proposed inverter, few more things need to be calculated such as boost inductor (L_B), DC-link capacitors (C_1 or C_2), and the output filter (L_1 or L_2, and C_o).

Following parameters are considered for practical design: the switching frequency (f_{sw}) of the incverter was 25 kHz, input voltage (V_{in}) was 173.5 V, forward voltage of the diode (C5D50065D) (V_D) is 1.8 V, modulation index (M) is 0.90, and the DC-link voltage (V_{PN}) was 364 V.

The boost inductor can be calculated by (48) which depends on input current ripple (ΔI_{in}), input voltage (V_{in}) and output voltage of the boost converter. Using (48), the calculated value of the inductor is 0.4 mH.

$$L_{Bmin} = \frac{V_{in} \times (V_{boost} + V_D - V_{in})}{\Delta I_{in} \times f_{sw} \times (V_{boost} + V_D)} \quad (48)$$

The DC-link capacitors C_1 and C_2 can be calculated by (49) which is depended on maximum output load current ($i_{O,max}$) and the permissible voltage ripple across the applying input voltage (ΔV_{in}) of the system. More specific selection can be done by duty ratio (D_b) as at the front side has used boost converter which is selected 0.5. As a result, the calculating minimum capacitor value is around 650 μF.

$$C_{1min}\ or\ C_{2min} \geq \frac{i_{O,max} \times D_b \times (1 - D_b) \times 1000}{\Delta V_{in} \times f_{sw}} \tag{49}$$

The selection criteria mentioned here is for voltage source type inverters that only need filters inductor at the output to provide filtering for the output waveform. However, to reduce the inductor size usually a capacitor is used in parallel with the load, and hence, the solution here would be similar to the use of a low pass LC filter. The required inductance should be computed for the instant that the value of current ripple is maximum at inductor output which is recommended to choose a value between 20% and 40 % of rated output inductor current (i_{L_f}). Moreover, the filter inductor value depends on the modulation type, and switching conditions [19], [20]. Thus, the maximum ripple factor ($\Delta \mathrm{I}_{factor}$) (51), and Fig. 3.6 shows the waveform of $\Delta \mathrm{I}_{factor}$ for selected modulation index (M) to obtain the maximum ripple factor which helps to calculate the filter inductor value by (51). The highlighted maximum ripple factor is approximately 0.25 which applies in (50) together with a ripple across the inductor of 40%, resulting in a minimum inductance value of approximately 2.5 mH.

$$\Delta I_{Factor} = M\ sin\ (2\pi f_m t) - M^2\ sin^2\ (2\pi f_m t) \tag{50}$$

where, f_m is the fundamental frequency.

$$L_{1min} \text{or } L_{2min} = \frac{V_{out} \times \Delta I_{Factor}}{f_{sw} \times \Delta I_{Lf}} \tag{51}$$

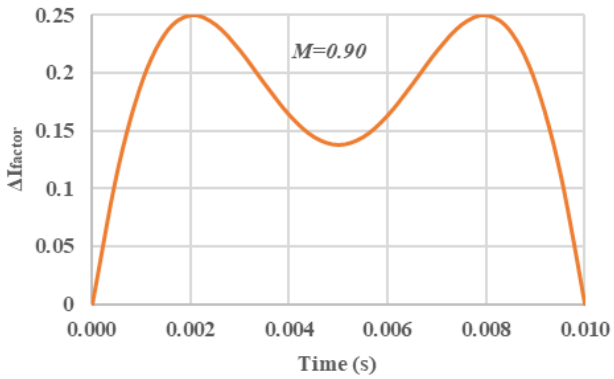


Fig. 3.6. Graph of ΔI_{factor} vs M for highlighting the maximum ripple factor.

On the other hand, the filter capacitor (C_o) can be calculated by (52) where cut-off frequency (f_c) is set to be 10% of the f_{sw}[19] and the calculated value is approximately 2.2 µF.

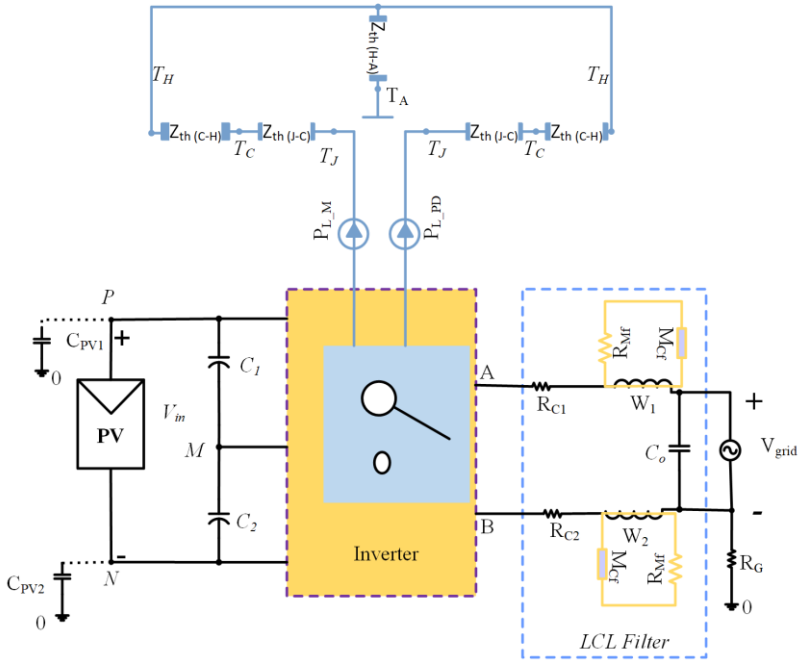
$$C_o = \frac{1}{4 \times \pi^2 \times {f_c}^2 \times L_1} \tag{52}$$

3.6. Comparison with Existing Topologies

3.6.1. Thermal Analysis and Comparison the Loss Calculation with Selected Topologies

To have a feeling of the loss distribution in different components of the mid-point clamping inverter topologies simulations have been carried out using PLECS models. Similar parameters and switches (SCT3022ALGC11 for active switches and C5D50065D for diodes) covered by the heat sink was considered for the thermal modelling.

The thermal impedance with conduction and switching (turn-ON/OFF) loss characteristics have been imported from the datasheet of the devices. Passive components losses in the filter and capacitor are also modelled appropriately considering the magnetic property of the inductor core and ESR of the filter capacitor (see Fig. 3.7).



T_J = junction temp. , T_C = case temp., T_H = heat sink temp. , T_A = ambient temp. , $Z_{(J-C)}$ = thermal impedance (junction to case) , $Z_{(C-H)}$ = thermal impedance (case to heat sink) , $Z_{(H-A)}$ = thermal impedance (heat sink to ambient) , thermal impedance (heat sink to ambient) , P_{L_D} = diode power loss, P_{L_M} = MOSFET power loss, and P_{L_PD} = Anti-parallel diode of the MOSFET power loss, R_{Mf1} = Magnetic resistance for winding W_1, R_{Mf2} = Magnetic resistance for winding W_1, M_{Cf1} = Magnetic core elements for winding W_1, M_{Cf2} = Magnetic core elements for winding W_2, R_{C1} = Core loss resistance for winding W_1, and R_{C2} = Core loss resistance for winding W_2.

Fig. 3.7. Thermal equilibrium circuit of mid-point clamping transformerless inverter.

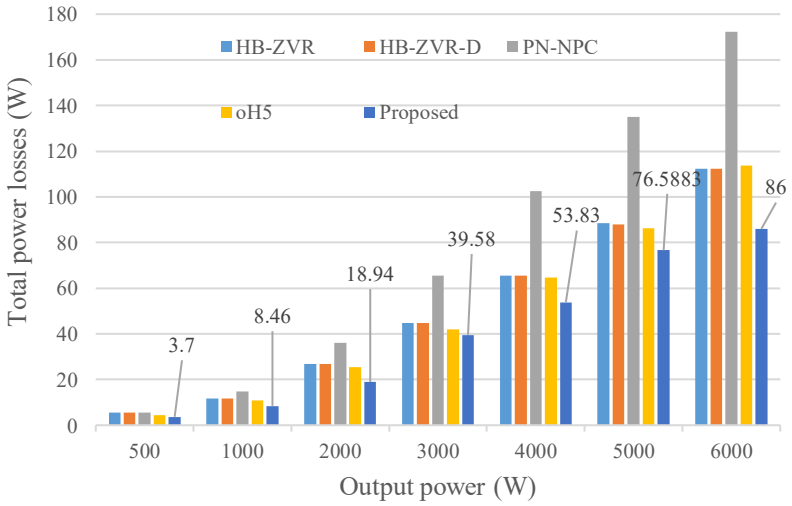


Fig. 3.8. Total power losses comparison.

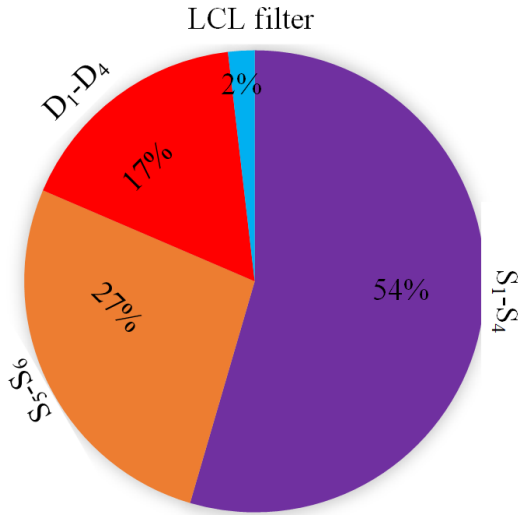


Fig. 3.9. Losses in full load condition of proposed topology for 6 kW.

Table 3.1 illustrates the loss breakdown (conduction, and switching) of the mid-point clamping topologies and Fig. 3.8 shows the total losses for selected topologies. It is evident that the proposed topology exhibit minimal losses.

Table 3.1 Comparison of the calculated power losses of existing mid-point clamping single phase transformerless inverter topologies with proposed topology

Topologies	**Output Power (W)**							**Losses**
	500	1000	2000	3000	4000	5000	6000	
HB-ZVR	2.86	7.25	19.2	33.8	51.7	69.5	91	C_{Loss}
	2.63	4.63	7.7	11	14.6	19	22.7	S_{Loss}
HB-ZVR-D	2.86	7.05	19	33.7	50.88	69.46	89.64	C_{Loss}
	2.633	4.64	7.7	11	14.5	18.44	22.7	S_{Loss}
PN-NPC	4.11	11.48	30.4	57.1	90.8	120	154	C_{Loss}
	1.43	3.2	5.6	8.3	11.65	14.9	18.3	S_{Loss}
oH5	3.1	7.86	20.46	34.93	55.14	74.4	98.6	C_{Loss}
	1.42	3	5.01	6.96	9.44	11.87	15	S_{Loss}
Proposed	2.68	6.66	15.96	31.9	45.83	66.48	74	C_{Loss}
	1.02	1.8	2.98	7.68	8	10.11	12	S_{Loss}

Note: C_{Loss} = Conduction loss, S_{Loss} = Conduction loss.

Moreover, Fig. 3.9 shows losses in different part of the proposed inverter, where semiconductor losses on the top. In addition, the loss related to the forward voltage drop in

the bridge diodes are considerable. In contrast, the losses in the passive components are considerably low.

3.6.2. Voltage and Current Stress Comparison with Selected Topologies

Table 3.2 lists the voltage stress, current parts and no. of required high-frequency switches. The voltage stress of the proposed topology is equal to the DC-link voltage for four switches (S_1-S_4), and other two switches (S_5 and S_6) are half of the DC-link voltage which is later verified by simulation and experiment. However, topology PN-NPC requires four grid frequency. As a result, the total switching losses is low, but as the required number of semiconductor switches are more. Hence, overall loss is comparatively higher than the mentioned topologies which are explained briefly in below.

Table 3.2. Voltage and Current Stress Comparison of Selected Mid-Point Clamping Topologies

Topologies	**Voltage stress**	**No. of semiconductors in the current path**		**No. of high-frequency switches**
		positive	**negative**	
HB-ZVR [9]	$V_{S1} = V_{S2} = V_{S3} = V_{S4} = V_{S5} = V_{PN}$	2	2	4 (f_{sw} for half cycle only) 2(f_{sw} for full cycle)
HB-ZVR-D [41]	$V_{S1} = V_{S2} = V_{S3} = V_{S4} = V_{S5} = V_{PN}$	2	2	4 (f_{sw} for half cycle only) 2(f_{sw} for full cycle)
PN-NPC [40]	$V_{S2} = V_{S3} = V_{PN}, V_{S1} = V_{S4} = V_{S5} = V_{S6} = V_{S7} = V_{S8} = \frac{V_{PN}}{2}$	4	2	4 (f_{sw} for half cycle only) 4 (f_m for half cycle only)
oH5 [37]	$V_{S1} = V_{S2} = V_{S3} = V_{S4} = V_{DC}, V_{S5} = V_{S6} = \frac{V_{PN}}{2}$	3	3	4 (f_{sw} for half cycle only) 2(f_{sw} for full cycle)
Proposed	$V_{S1} = V_{S2} = V_{S3} = V_{S4} = V_{DC}, V_{S5} = V_{S6} = \frac{V_{PN}}{2}$	2	2	4 (f_{sw} for half cycle only) 2(f_{sw} for full cycle)

3.6.3. Leakage Current Comparison Curve with Selected Topologies

On the other hand, the main limitation of the transformerless inverter topology is leakage current that flows through the parasitic capacitor. Hence, at the end of this section has analysed the leakage current (i_{cm}) and compared with nominated topologies (HB-ZVR, HB-ZVR-D, PN-NPC and oH5) in different condition (see Fig. 3.10). In between all topologies, proposed topology shows an excellent performance. Fig. 3.10 considers different

filter inductors (1 mH-5 mH), and different parasitic capacitances (68 μF-330 μF). Leakage current (i_{cm}) is increased inversely proportional with increasing the filter inductor values. Maximum i_{cm} flows for HB-ZVR topology (indicates by pink color) whereas proposed (red color) and PN-NPC (green color) flow the low amount of leakage current. Moreover, analysing the leakage current for the proposed topology is verified through the simulation and experiment in the next section for 2.6 mH filter inductors. The leakage current (i_{cm}) of the proposed topology reaches maximum 22.02 mA for 330 nF ($C_{PV1} = C_{PV2}$), and minimum 13.08 mA for 68 nF ($C_{PV1} = C_{PV2}$) for 2.6 mH filter inductors. However, for the same filter inductor values i_{cm} reaches maximum 34 mA, and 31 mA for HB-ZVR, and oH5 topologies respectively whereas PN-NPC, and HB-ZVR-D topologies i_{cm} remain low comparatively.

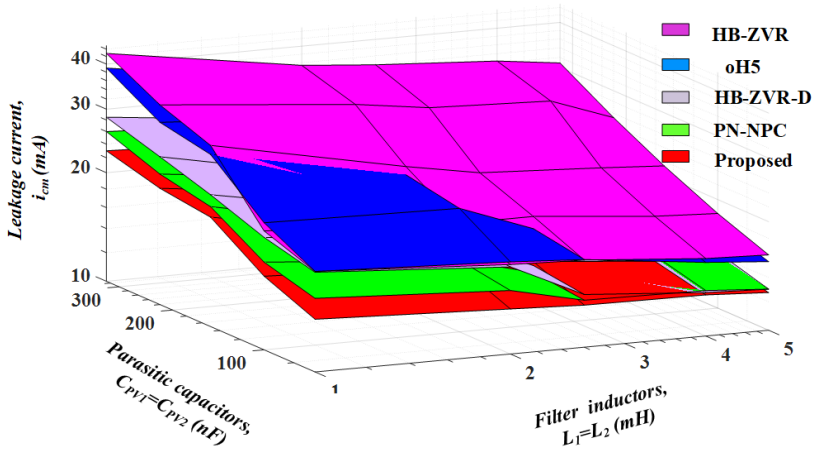


Fig. 3.10. Leakage current comparison curve with existing mid-point clamping topologies for varying the parasitic capacitors and the filter inductors.

3.7. Comparative Summary of Proposed Topology with Conventional Mid-Point Clamped Transformerless Inverter Topologies

The following section systematically compares the proposed topology with conventional mid-point clamped transformerless inverter topologies. Table 3.3 presents a detailed comparison list of the proposed topology with selected mid-point clamped topologies considering the required input voltage, output voltage, the number of active and passive

components to design the inverter, output filter type and its value, CM effect, reactive power capabilities, power factor, THD, cost, and efficiency.

It can be seen that the proposed topology is required the least semiconductor devices with low CM effect. Moreover, the proposed topology has reactive power capability and low THD. The prototype cost and size depend on how many components are required in the system. As a result, analysed the mentioned topologies cost accordingly and compared with a proposed topology where the cost and size show reasonable for proposed topology, but oH5 [14], and H5-D [25] require small in size with lower cost comparatively. Nonetheless, both topologies are not capable to achieve high efficiency. On the other hand, the efficiency is of the proposed topology reaches 98.15% at a full load condition (1.5 kW) which is comparatively higher than the other topologies.

3.8. Results and Discussions

3.8.1. Components Selection for Simulation and Experiment of Proposed Topology I

Simulation of the proposed topology has been carried out in Matlab-Simulink using the PLECS toolboxes and then verified experimentally with a 1500 W laboratory test. Both simulation and experiment use same parameters and are listed in Table 3.4.

Table 3.4. Parameters for simulation and Measurements

Description	Values/Parameters
Input Voltage, V_{in}	173.5 V
DC-link voltage, V_{PN}	364 V
Output Voltage, V_{grid}	230 V
Rated Power P_o	1.5 kW
Switching Frequency(f_{SW})	25 kHz
Line Frequency, (f_m)	50 Hz
Modulation Index, M	0.90
Boost Diode, (D_B)	C5D50065D (650 V, 50A)
DC-link-Capacitors, $(C_1$ and $C_2)$	0.68 mF (LLS2E681MELA)
Switches, $(S_B, S_1 - S_6)$	SCT3022ALGC11 (650 V, 93 A, 22 m Ω)
Filter Inductor, $(L_1 = L_2)$	2.6 mH
Filter Capacitor, (C_O)	2.2 μF
Parasitic Capacitors, ($C_{PV1,}$and C_{PV2})	220 nF
Ground Resistor, R_G	10 Ω
Resistive Load	51.8 Ω
Resistive-Inductive Load	46.8 Ω, 70 mH

Power Factor	0.86
Controller	sb-RIO GPIC
Gate Drive Circuit ($GDC_{SB}, GDC_{S1} - GDC_{S6}$)	
Optocoupler IC	ACPL-P343
DC/DC Converter	RP1212D
Resistor	10 Ω, 47 kΩ
Capacitor	1 μF, 100 μF

A simple boost converter is interfaced at the front stage of the proposed inverter for boosting the PV voltage (173.5 V) to the required DC-link voltage (364 V) which is the required DC-link voltage of the inverter for 230 V AC output.

3.8.2. Hardware Setup

Fig. 3.11 (a) shows the test bench of the experiment work showing the layout of the loads and equipments used. Zoomed in view of the top and bottom part of the circuit board are shown in Fig. 3.11 (b), and 3.11 (c) respectively.

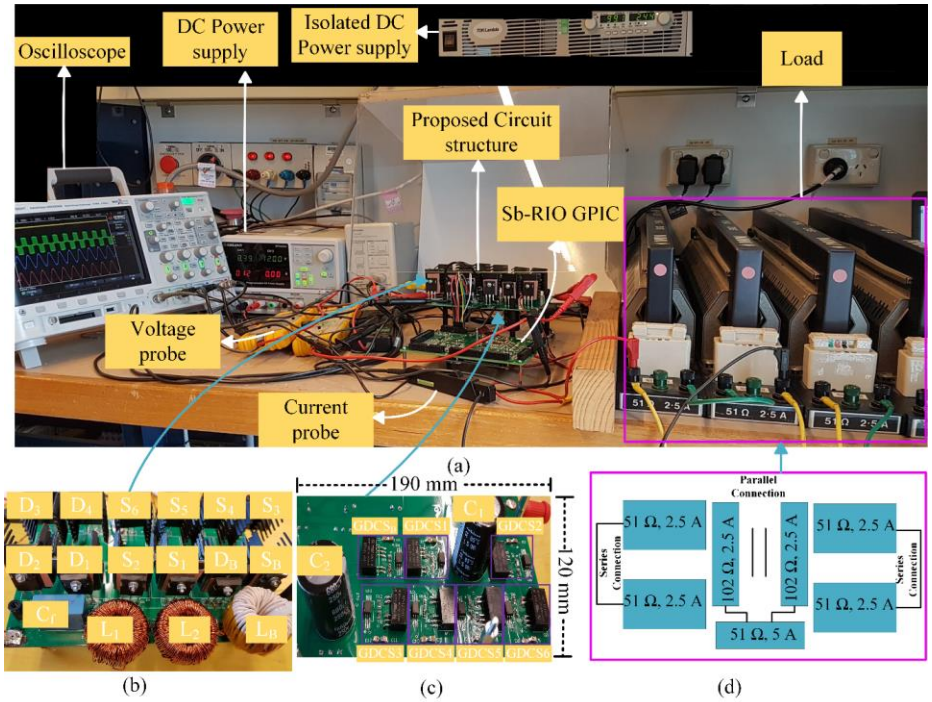


Fig. 3.11. Experimental setup of the HB-ZVSCR transformerless inverter topology (a) test bench, (b) top view of the proposed circuit structue, and (c) bottom view of the proposed circuit structue, (d) Load connection for 1.5 kVA prototype test.

Table 3.3. Comparative summary of proposed topology with conventional mid-point clamped transformerless inverter topologies

Topologies	No. of Semiconductor devices		Extra Passive Component		Output Filter Type			Common mode effect		RPC	Reported Ø	Reported THD	Cost / size *	Reported η (%)
	S	D	L	C	L_1 (mH)	L_2 (mH)	C_f (μF)	i_{cm} (mA)	CMV (V)					
PN-NPC [40]	8	0	0	2	3	3	0.47	< 20	constant	Yes	Unity	N/A	+++ +	97.2 @ 1 kW
oH5 [37]	6	0	0	2	4	4	6.6	< 20	constant	Yes	Unity	N/A	++	N/A
[39]	7	0	0	2	0.85	0.85	--	< 20	constant	Yes	Unity	1.7%	+++ +	97 @ 2 kW
HB-ZVR [9]	5	5	0	2	1.8	1.8	2	> 20	constant	Yes	Unity	N/A	+++	94.88 @ 2.8 kW
HB-ZVR-D [41]	5	6	0	2	3	3	6	> 20	constant	Yes	Unity	N/A	+++	95.03 @ 1kW
H5-D [38]	5	1	0	2	1	1	10	>20	constant	Yes	Unity	N/A	++	95.8 @ 630 W
[145]	9	1	1	2	0.9	0.9	--	< 20	constant	Yes	Unity	4.2%	+++ +	96.13 @ 220 W
[66]	8	2	2	4	N/A	N/A	N/A	N/A	constant	NR	Unity	N/A	+++ +	97 @ 1 kW
[7]	8	0	0	2	5	5	5	< 20	N/A	Yes	Unity	4.35%	+++ +	96.02 @ 1 kW
[102]	7	4	0	2	3	3	4	< 20	constant	Yes	Unity	1.6%	+++ +	97.65 @ 1 kW
Proposed topology	6	4	0	2	2.6	2.6	2.2	< 20	constant	Yes	0.86	1.8%	+++	98.1 @ 1.5 kW

* The more "+" represents the higher cost/size, + ≡ low, ++ ≡ medium, +++ ≡ high, and ++++ ≡ extremely high. In the above table, "S" represents switch, "D" represents diode, "C" represents capacitor, "L" represents inductor, "η" represents efficiency, "RPC" reactive power capability, "Ø" power factor, "THD "total harmonic distortion, "NR" not recommended, "N/A" not available.

To turn ON the MOSFET with a proper voltage level, the gate drive circuit generates 18 V from an isolated DC/DC converter and the voltage isolation between the control board and the power circuit is achieved by the optocoupler.

The gate driver circuit for the MOSFETs of the proposed inverter prototype can be found on the bottom side of the PCB (see Fig. 3.11 (c)). Fig. 3.11 (d) shows the load connection for 1.5 kW. The block diagram view of the gate drive circuit is shown in Fig. 3.12.

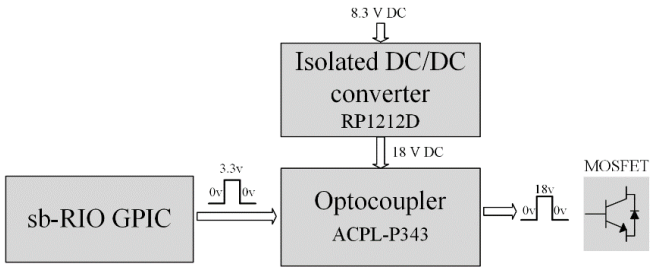


Fig. 3.12. The implemented way of gate pulse generation for the MOSFETs.

3.8.3. Simulation and Experimental Results

The controller sb-RIO GPIC is interfacing with LabVIEW software and operating the switching pulses through the LabVIEW software. The PWM gate pulses for all active switching devices that are generated by the sb-RIO GPIC are illustrated in Fig. 3.13. Simulations and experiment were also carried out together for proposed topology, as shown in Fig. 3.14 - Fig. 3.22 using the parameters listed in Table 3.4. Fig. 3.14 (a), and Fig. 3.14 (b) shows the voltage stress of the power switches ($S_1 - S_6$) in both simulation and experimental waveforms respectively where it is possible to observe the similarity. On the other hand, the voltage stress of H-bridge diode rectifiers are shown in Fig. 3.15.

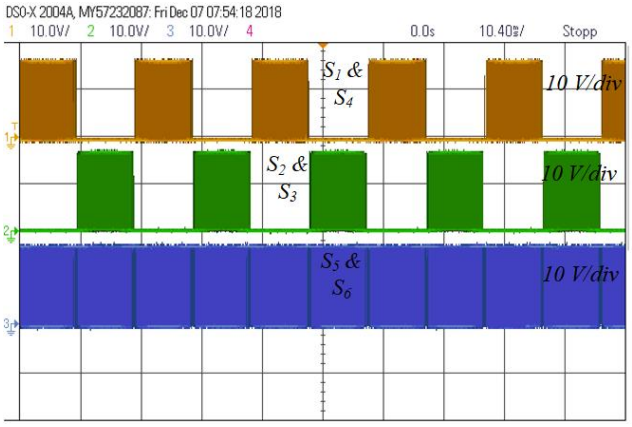
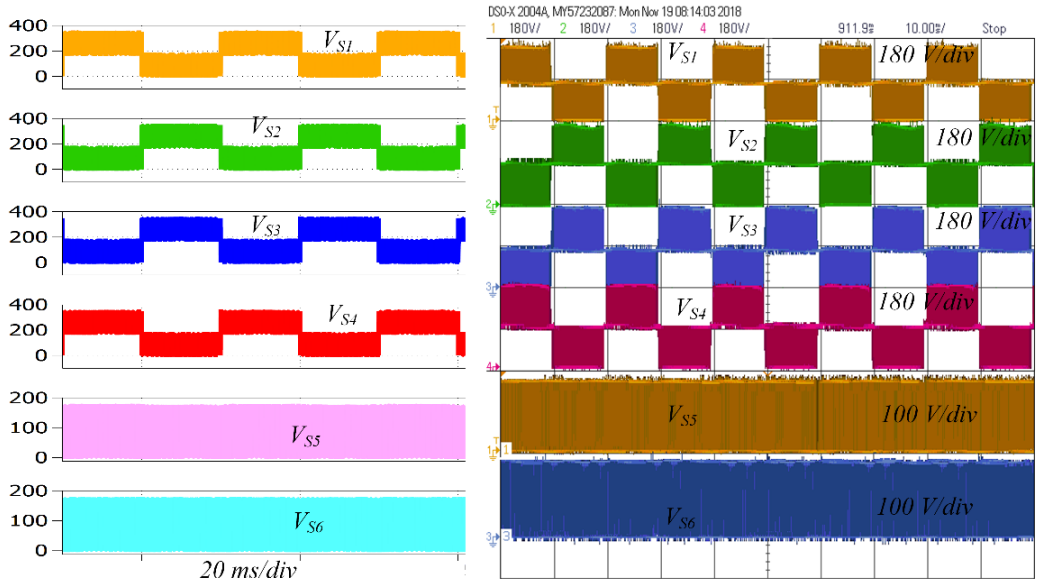


Fig. 3.13. Switching pulses.

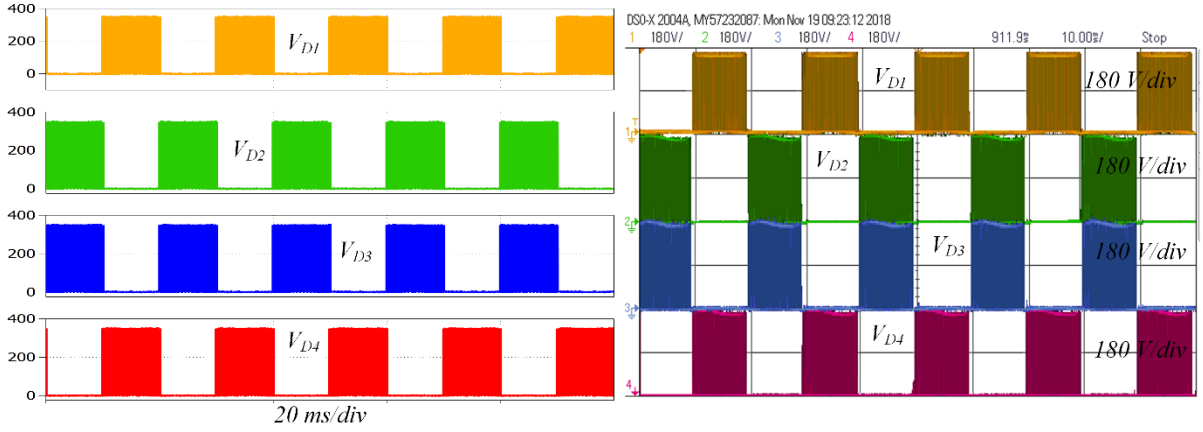
The input voltage (V_{in}), DMV (V_{AB}), output voltage (V_{grid}), and output current (i_{grid}) displayed in Fig. 3.16, and Fig. 3.17. The input voltage is 173.5 V, the DC-link voltage is boosted to 364 V.

The RMS value of the output voltage is 228.4 V which is in phase with the corresponding load current of 4.45 A for a 51.8-Ω resistive load. Moreover, the THD of the output voltage and current waveforms are measured which is 1.6%, and 1.8% respectively.



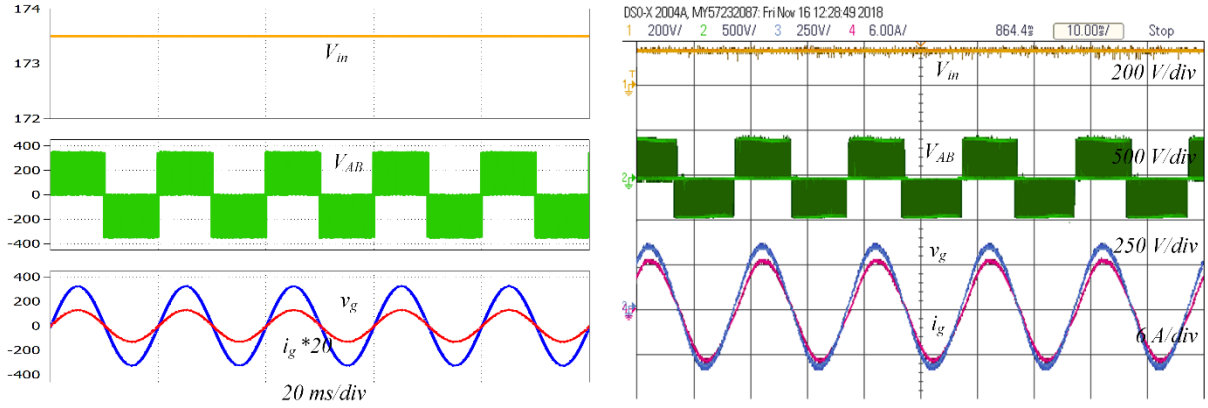
(a) (b)

Fig. 3.14. Voltage stress of the power switches; (a) simulation waveforms, (b) experimental waveforms.



(a) (b)

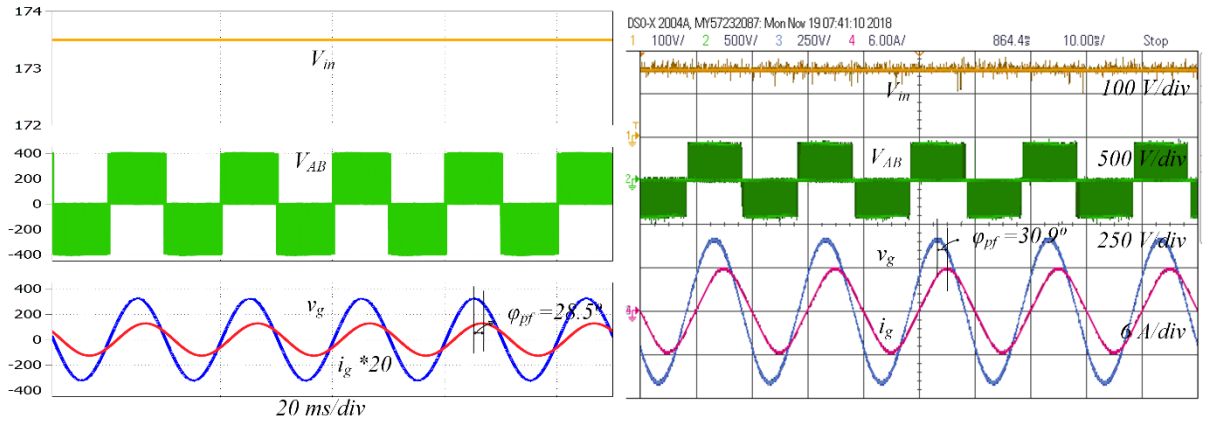
Fig. 3.15. Voltage stress of the bridge diodes; a) simulation waveforms, (b) experimental waveforms.



(a) (b)

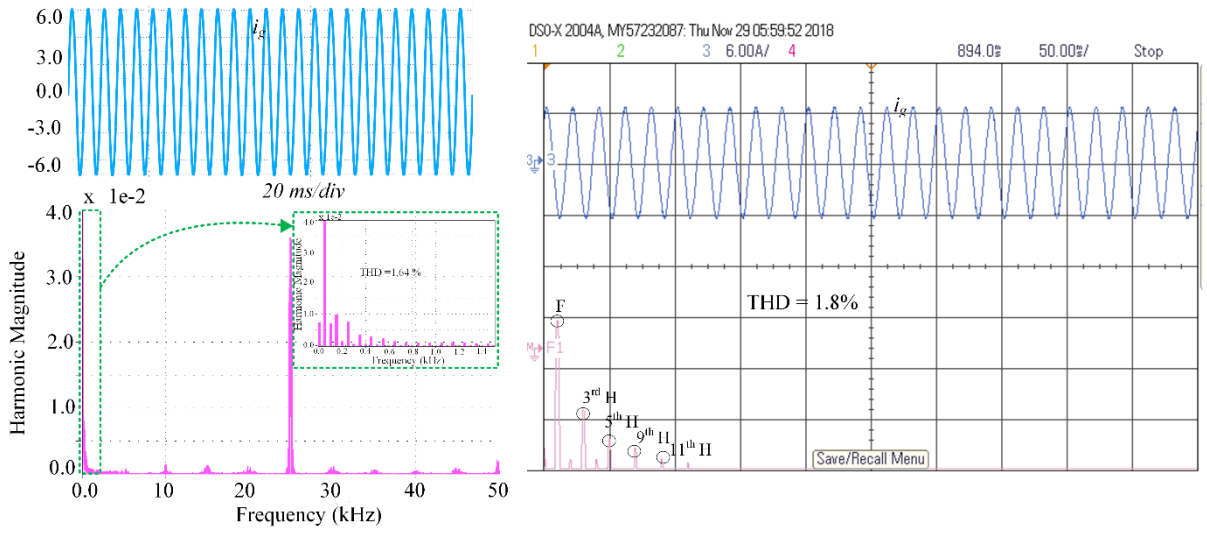
Fig. 3.16. Input voltage, inverter output, Output voltage and current for resistive (R) load(a) simulation waveforms, (b) experimental waveforms.

The capacity of delivering reactive power to the grid has also been successfully demonstrated in simulation (see Fig. 3.17 (a)) and experimental (see Fig. 3.17 (b)) with cos φ = 0.87 (φ = 28.5° lagging current), and cos φ = 0.86 (φ = 30.8° lagging current) respectively. Fig. 3.18 displays the harmonic spectrum of the output current to show the THD in simulation (see Fig. 3.18 (a)), and experimental (see Fig. 3.18 (b)). Hence, it is an evidence that the THD of the output current is less than1.8%.



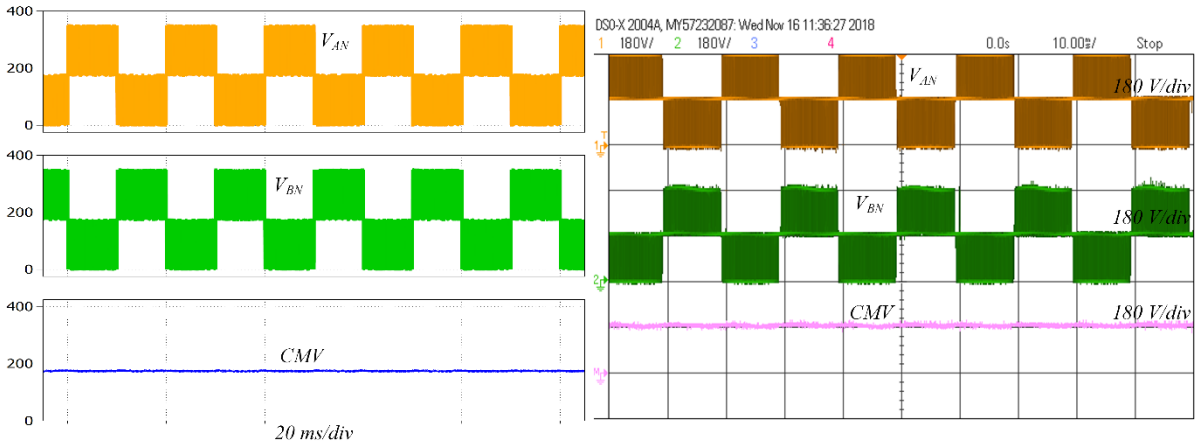
(a) (b)

Fig. 3.17. Input voltage, inverter output, Output voltage and current for resistive-inductive (R-L) load(a) simulation waveforms, (b) experimental waveforms.



(a) (b)

Fig. 3.18. Harmonic spectrum of the output current(a) simulation waveforms, (b) experimental waveforms.

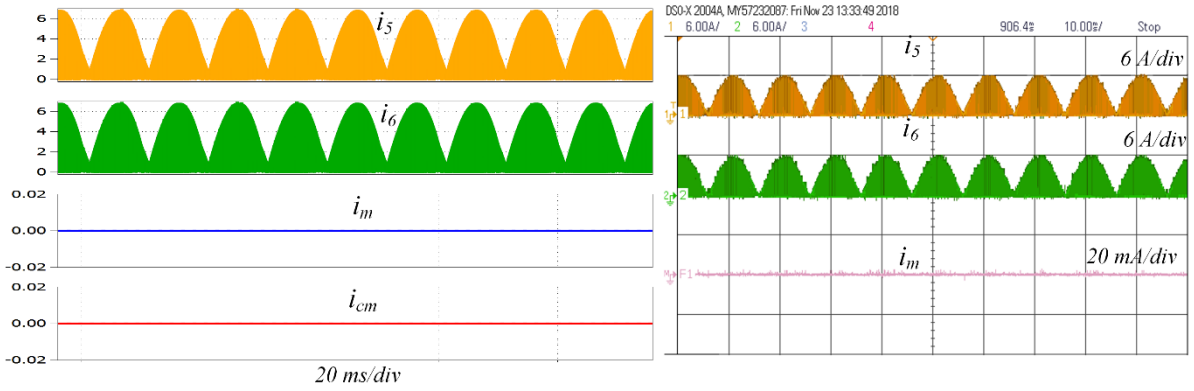


(a) (b)

Fig. 3.19. Voltage across the point A to neutral, Voltage across the point B to neutral, and CMV(a) simulation waveform, (b) experimental waveform.

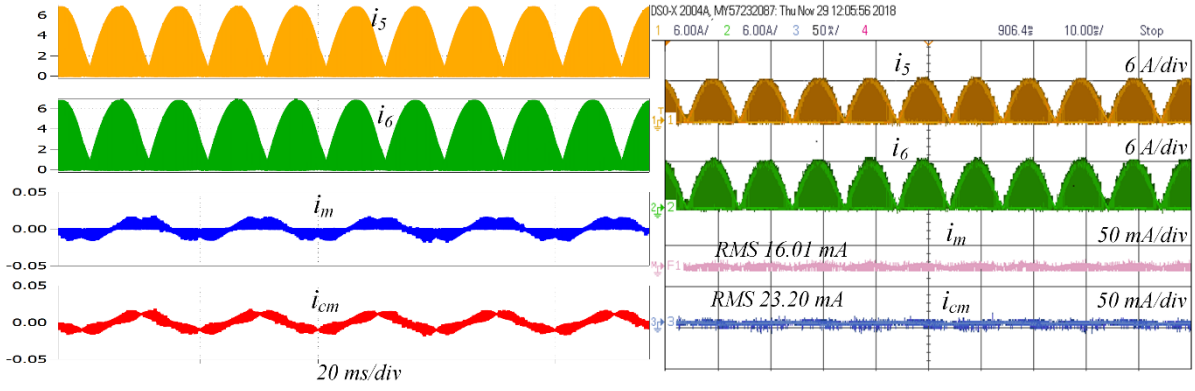
The waveforms of the voltage V_{AN}, V_{BN} and CMV ($\frac{V_{AN}+V_{BN}}{2}$) (using the math function of the oscilloscope) show in Fig. 3.19 where in both simulation (see Fig. 3.19 (a)), and experimental (see Fig. 3.19 (b)), the CMV is kept constant. The mathematical explanation of the resonant circuit, and the current different between switch S_5, and S_6 has shown in previous sub-section called "common mode effect" that the current different between switch

S_5, and S_6 is almost equal to the leakage current which is, $i_m = (i_5 - i_6) \sim i_{cm}$. In consequence, Fig. 3.20 and Fig. 3.21 show the effect of parasitic capacitor, and the theoretical verification through simulation and experimental. Fig. 3.21 shows the current through the switches S_5, and S_6, difference between these switches (i_m), and i_{cm}.



(a) (b)

Fig. 3.20. Effect of parasitic capacitor when $C_{PV1} = C_{PV2} = 0$; (a) simulation waveform, (b) experimental waveform.



(a) (b)

Fig. 3.21. Effect of parasitic capacitor when $C_{PV1} = C_{PV2} = 220\ nF$; (a) simulation waveform, (b) experimental waveform.

As parasitic capacitors ($C_{PV1} = C_{PV2}$) is zero, there is no change to flow any ground current ad there is equal current ($i_5 = i_6$). On the other hand, after applying parasitic effect ($C_{PV1} = C_{PV2} = 220\ nF$), current between the switches (S_5, and S_6) are different ($i_5 \neq i_6$)

and i_{cm} reaches to 16.01 mA (RMS) which is approximately equal to i_m by 23.20 mA (RMS). Fig. 3.22 shows the leakage current for different values of parasitic capacitances for 25 kHz switching frequency.

It can be seen that leakage current gradually increased by increasing the value of $C_{PV1} = C_{PV2}$. For example, when $C_{PV1} = C_{PV2} = 68\ nF$, i_{cm} reaches to 12.55 mA (see Fig. 3.22 (a)). Moreover, few more examples are shown in Fig. 3.22 (b) – Fig. 3.22 (e) where maximum leakage current flows by 16.65 mA for 330 nF parasitic capacitances.

Table 3.5 demonstrates the measured value of both $i_{cm}, and\ i_m$ to change the switching frequency from 20 kHz to 30 kHz for different values of parasitic capacitance. It is clear evidence that, leakage current is proportionally increased with the switching frequency. In between these switching frequency and parasitic capacitance, leakage current flowing range is (12.70 mA-18.32 mA), and i_m range is (14.10 mA-22.70 mA).

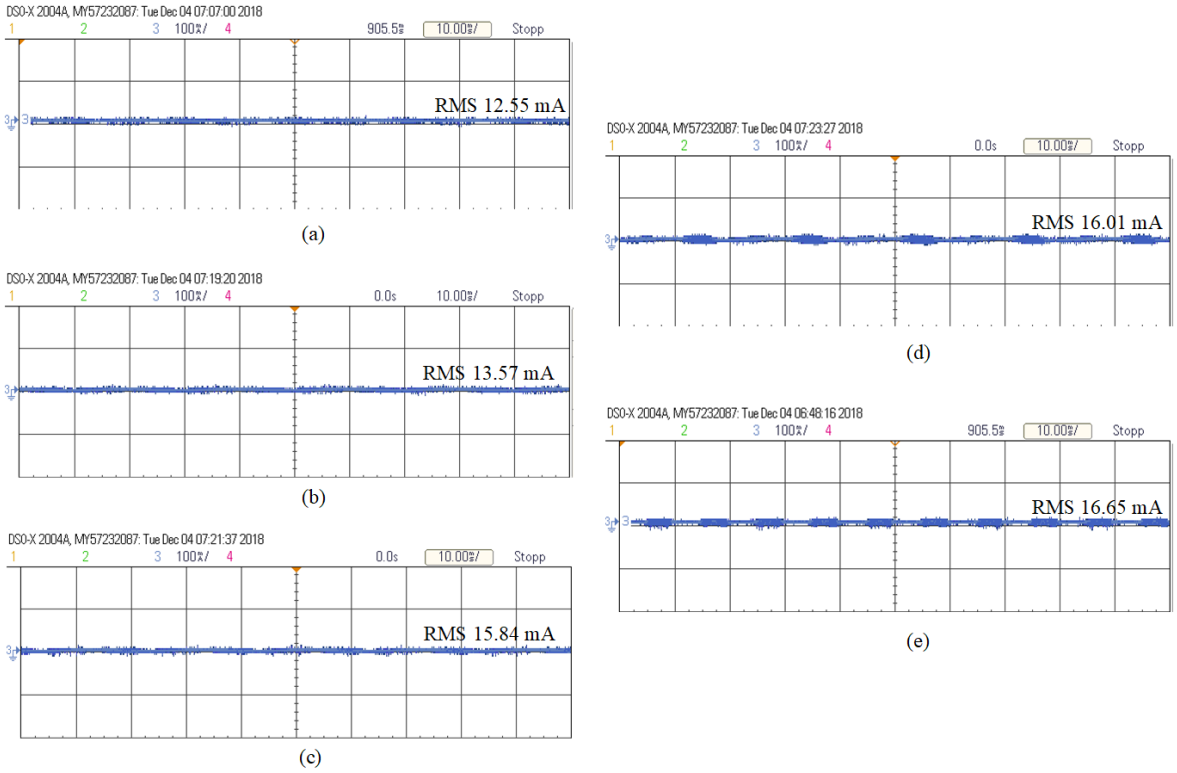


Fig. 3.22. Experimental waveforms of the Leakage Current when; (a) $C_{PV1} = C_{PV2} = 68\ nF$, (b) $C_{PV1} = C_{PV2} = 100\ nF$, (c) $C_{PV1} = C_{PV2} = 150\ nF$, (d) $C_{PV1} = C_{PV2} = 220\ nF$, and (e) $C_{PV1} = C_{PV2} = 330\ nF$.

Table 3.5. Measured RMS value of the leakage current at different f_{sw}

$C_{PV1} = C_{PV2}$ (nF)	f_{sw} (kHz)	i_{cm} (mA)	i_m (mA)
68	20	18.32	22.70
	25	12.55	19
	30	9.40	15.40
100	20	20.13	25.10
	25	13.57	20.50
	30	10.70	16.20
150	20	21.90	28.80
	25	15.84	22.20
	30	11.02	19
220	20	27.70	30.80
	25	16.01	23.20
	30	12	15
330	20	27.50	31.30
	25	16.65	24.20
	30	12.70	14.10

The overall efficiency curve in both simulation and experimental of the proposed inverter is illustrated in Fig. 3.23, and measured by a FLUKE 345 power quality clamp meter where the peak efficiency reaches 98.96% at the full load condition, and 98±1% over a wide range of load. In (31) and (32) are given the formula for calculating the overall efficiencies which stand for European (EU) and California Energy Commission (CEC) weighted efficiencies respectively.

Table 3.6.Efficiency Comparison for 1kw Rated Power of Different Mid-Point Clamping Existing Topologies

Topologies	**Output power (W)**						
	~100	**~200**	**~300**	**~500**	**~750**	**~1000**	**~1500**
HB-ZVR [9]			89 %	90.4 %	91.6%	92.8%	93.8 %
HB-ZVR-D [41]	89 %	90.8 %	93.2%	95.2 %	96.1 %	96.1 %	
PN-NPC[40]	96%	97.7 %	97.7 %	97.5 %	97.3 %	97.1%	
oH5 [37]	95.6 %	97 %	97.4 %	97.2 %	97 %	96.8 %	
Proposed	94.1 %	96.76 %	97.22 %	97.74 %	98 .32%	98.8 %	98.1 %

Table 3.6 displays the efficiency for different load conditions and compared with selected topologies. In proposed topology, the voltage stress of the freewheeling switches are half of the DC-link voltage and the inductor current flows through two switches during the whole grid period.

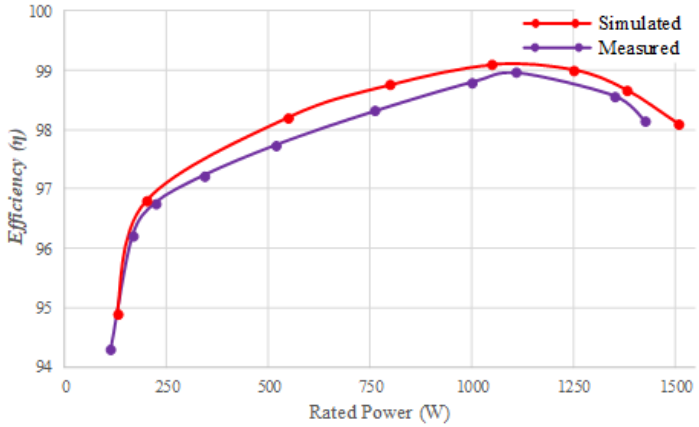


Fig. 3.23. Plot of power vs. efficiency.

As a result, the switching losses and conduction losses are reduced considerably. Thus, the proposed topology shows the maximum efficiency. According to the given formulas, calculated efficiencies are 98.1%, and 97.84% when selecting CEC, and EU respectively. Note that, the efficiency is measured without the front stage boost DC-DC converter and it covers the total power device losses and the output filter losses, but it does not include the losses for the control circuit.

3.9. Summary

In this Chapter, a new single-phase transformerless mid-point claimed PV inverter has been presented. The proposed topology exhibits constant CMV during the whole time period (positive, negative, and zero states). As a result, the leakage current is well mitigated. This is demonstrated by measuring the leakage current at different parasitic capacitance values and switching frequencies, where the maximum leakage current is 16.65 mA with 330 nF capacitor at 25 kHz switching frequency. The proposed topology reduces the output current ripples, and as a result, THD is relatively low (≤1.8 %). Moreover, only two switches are in series during the active state, which helps in reducing the conduction loss in the system. Finally, the measured efficiency is 98±1% over a wide range of loads for a 1.5 kW prototype with the peak efficiency of 98.96% which is higher than the conventional mid-point clamped topologies. With all these advantages, the proposed topology provides a good choice for single-phase transformerless PV inverters.

Chapter 4

Switched Capacitor Integrated (2n+1)-Level Step-Up Inverter (Proposed Topology II)

4.1. Circuit Structure Explanation

The proposed variable dc-link multilevel inverter is a modular multicell structure similar to flying capacitor (FCC) or cascaded H-Bridge (CHB), where it is possible to increase/decrease the number of levels by connecting/disconnecting the basic switching cell units following the multicell arrangement. The generic circuit of the proposed converter to generate (2n+1)-level in the output voltage is shown in Fig. 4.1.

Each cell consists of three active switches and two capacitors and represents two extra voltage levels ($V_{C1} = V_C$ or $V_{C2} = V_C$ and $V_{C1} + V_{C2} = 2\ V_C$). However, the number of capacitor in the succeeding cell has one less than the antecedent cells, as one of the capacitor is shared between the cells. Hence, the total number of switches and capacitor for n-level inverter is 3(n-1) and n respectively.

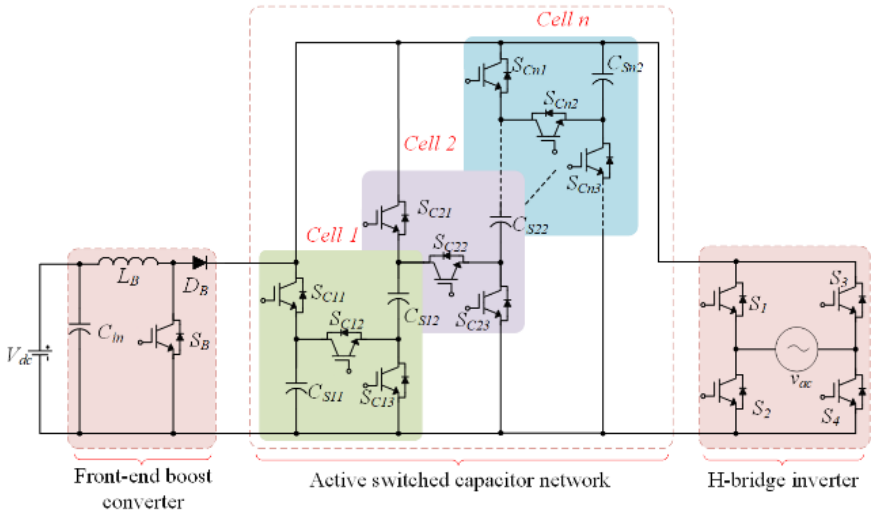


Fig. 4.1. The proposed (2n+1)-level inverter structure.

Their allowed switching states provide a path to connect the capacitor of each cells in such a way that it adds or bypasses the capacitor voltage, which is pre-charged through a boost dc-dc converter at the front side. This create a variable dc-link voltage across P and N, which is fed to the 2-level VSI at the output side. Combinations of several switched capacitor-cells at the dc-link can increase/decrease the number of voltage levels generated at the ac side, without increasing the number of active devices proportionally to the three phases. In addition, the output voltage can be regulated to suitable ac voltage regardless of the drop in the input voltage from the source such as from renewable energy (PV panel, small wind turbine or fuel cells).

The equivalent circuit of the proposed multilevel inverter is shown in Fig. 4.2. The inductor L_B in the front boost converter also serve as a quasi-resonant inductor to charge the capacitor C_{S11}~ C_{SN2} in different mode of operation. Here, R_{eq} is the equivalent resistance of the circuit consisting of ON resistance of switches ($R_{DS,on}$), forward voltage drop of diodes and Equivalent Series Resistance (ESR) of capacitors, and S_{eq} is the equivalent of switch(es) in series with the capacitor(s). All capacitors are considered to be identical and with equal value and ESR. Similarly, all switches are identical with same voltage and current rating with same $R_{DS,on}$. Hence, unlike conventional topologies, where rating of devices in successive cells are higher than the antecedent cells; the rating of all devices are same in the proposed topology.

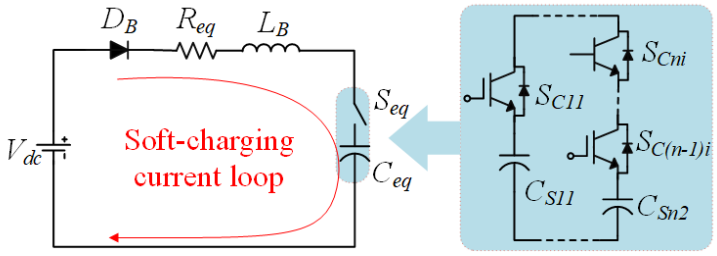


Fig. 4.2. Equivalent circuit of the proposed multilevel inverter with soft-charging current loop.

To simplify the circuit analysis, the following conditions are assumed:

1) Capacitors C_1, C_2 … C_n are large enough to keep V_{C1}, V_{C2} … V_{Cn} constant in one switching period.
2) The power MOSFET and diodes are treated as ideal. ON-state resistance $R_{DS\text{-}on}$ and parasitic capacitances of the switches are neglected. In addition, the forward voltage drops of the diode is ignored.
3) Equivalent Series Resistances (ESRs) of all capacitors are neglected.

4.2. Operating Principle and State Analysis

The operating principle of the proposed (2n+1)-level inverter is illustrated in Fig. 4.3. The operating principle is based on the generation of a variable dc-link voltage using the switched capacitor cells. Here, each capacitor in each switch switching cells are charges up to V_C, where

$$V_{CS11} = V_{CS12} \ldots V_{SCn1} = V_{SCn2} = V_C = \frac{V_{dc}}{1-D_b}. \tag{53}$$

Since there are two capacitors in each cell and every cell has two allowed switching states. So the voltage across each cell is

$$\hat{V}_{cell} = \begin{cases} V_C = \frac{V_{dc}}{1-\mathrm{D}}, \; S_{Cn1} = S_{Cn3} = 1 \; and \; S_{Cn2} = 0 \\ 2V_C = \frac{2V_{dc}}{1-\mathrm{D}}, \; S_{Cn1} = S_{Cn3} = 0 \; and \; S_{Cn2} = 1 \end{cases} \tag{54}$$

where, $S_{ni} = 1$ means that the i^{th} switch on n cell is ON and $S_{ni} = 0$ means that it is OFF.

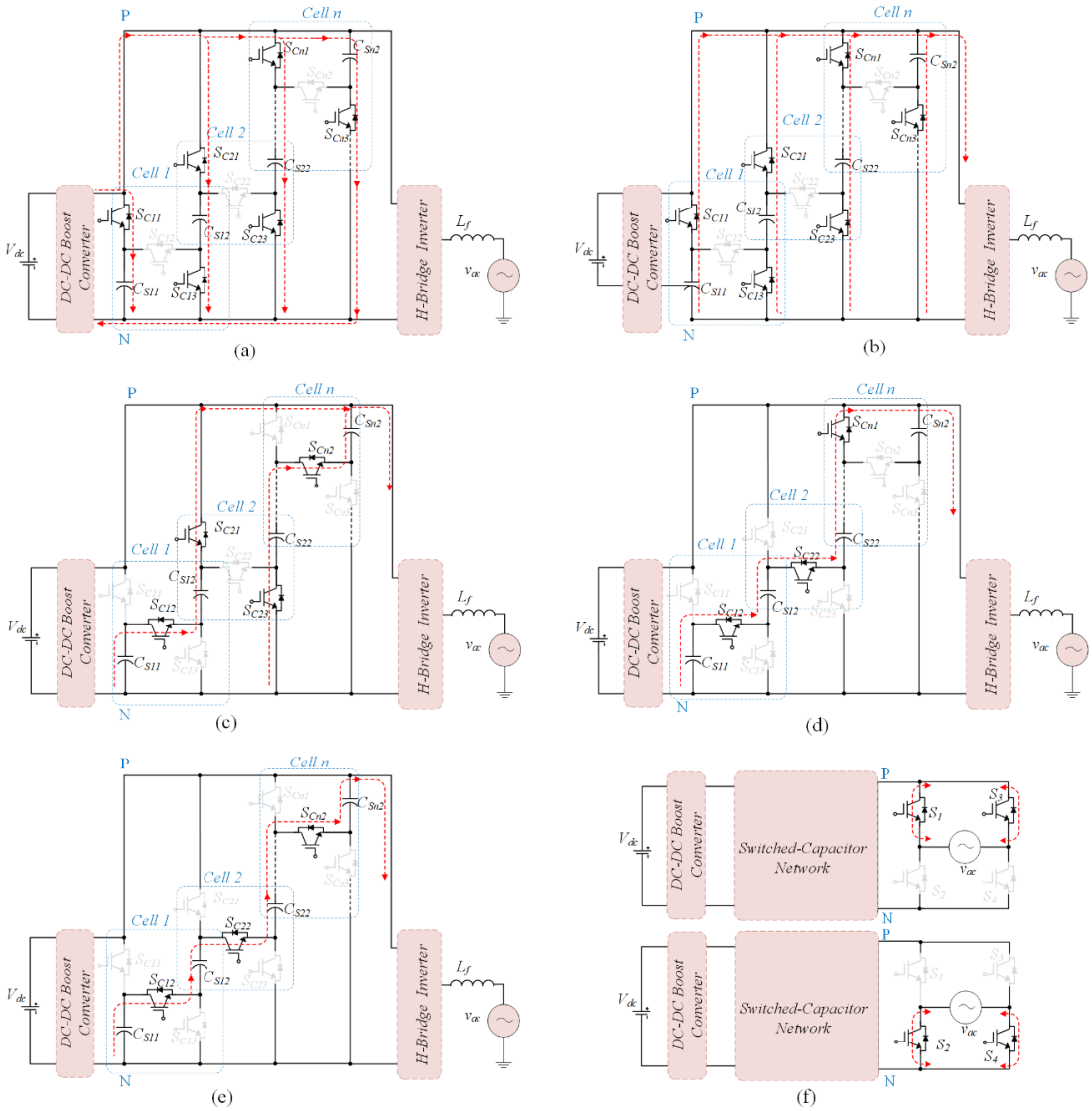


Fig. 4.3. Illustration of principle of operation: (a) capacitor charging in parallel $\hat{V}_{PN} = V_C$ and $\hat{v}_{ac} = \mp V_C$, (b) level 1 to create $\hat{V}_{PN} = V_C$ and $\hat{v}_{ac} = \mp V_C$, (c) level 2 to create $\hat{V}_{PN} = 2V_C$ and $\hat{v}_{ac} = \mp 2V_C$, (d) level 3 to create $\hat{V}_{PN} = 3V_C$ and $\hat{v}_{ac} = \mp 3V_C$, (e) level n to create $\hat{V}_{PN} = nV_C$ and $\hat{v}_{ac} = \mp nV_C$, and (f) (a) H-bridge to create $\hat{v}_{ac} = 0\,V$.

Fig. 4.3 shows a selections of the n different dc-link level generation possibilities. In Fig. 4.3 (a) & (b), capacitor are charging and discharging in parallel. In this mode, switches S_{Cn1} and S_{Cn3} are ON, whereas S_{Cn2} are turned OFF to connect all capacitors in parallel, where the equivalent capacitance in this mode is $C_{eq} = \sum_{n=1}^{n} C_{sn} \sum_{n=1}^{n} C_{sn}$. The peak voltage across PN and output ac is $\hat{V}_{PN} = V_C$ and $\hat{v}_{ac} = \mp V_C$ respectively. The next level of voltage is generated by turning ON switch S_{Cn2} sequentially to combine capacitor voltages, where

$\hat{V}_{PN} = V_{CS11} + V_{CS12} = 2V_C$ and $\hat{v}_{ac} = \mp 2V_C$. Similarly, maximum the peak voltage across the dc-link is created by turning ON S_{Cn2} and turning off rest of the switches. In general, the peak of dc-link voltage is given as:

$$\hat{V}_{PN} = \frac{n\,V_{dc}}{1-D_b}. \tag{55}$$

The zero state in the circuit is created by turning ON the upper switches (S_1 and S_3) or lower switches (S_2 and S_4) of the H-bridge. The details of the switching states of the converter is presented in Table 4.1.

Using (55), the peak of the AC output voltage of n-level inverter is

$$\hat{v}_{ac} = MV_{PN} = \frac{nM\,V_{dc}}{1-D_b} \tag{56}$$

where M is the modulation index, and is defined as the ratio of the peak of sinusoidal reference to the total peak-to-peak voltage of the two triangular carriers. Therefore, the maximum voltage gain of the proposed topology is the product of the gain of pre-boost converter and the gain of the switched capacitor network.

$$\frac{\hat{v}_{ac}}{V_{dc}} = G = \frac{nM}{1-D_b} \tag{57}$$

Therefore, the maximum voltage gain of the proposed n-level topology is the product of the gain of pre-boost converter and the gain of the switched capacitor network.

Table 4.1.Switching States and Corresponding Output Voltage Level Showing Capacitor State

Reference/ Switching State	**Voltage level**	**Max. output voltage ($\hat{v}_{ac}$) (For M = 1.0)**	**Switching capacitor network**										**H-Bridge**				**Impact on capacitor voltage**
			Cell 1			**Cell 2**			**…**	**Cell n**							
			S_{C11}	S_{C12}	S_{C13}	S_{C21}	S_{C22}	S_{C23}	…	S_{Cn1}	S_{Cn2}	S_{Cn3}	S_1	S_2	S_3	S_4	
Fig. 76(a) A	∓ 1	$-V_C$	1	0	1	1	0	1	…	1	0	1	1	0	0	1	↑
		$+V_C$											0	1	1	0	↑
Fig. 76(b) B		$-V_C$	1	0	1	1	0	1	…	1	0	1	1	0	0	1	↑
		$+V_C$											0	1	1	0	↑
Fig. 76(c) C	∓ 2	$-2V_C$	0	1	0	1	0	1	…	0	1	0	1	0	0	1	↓
		$+2V_C$											0	1	1	0	

Fig. 76(d) D	∓ 3	$-3V_C$	0	1	0	0	1	0	…	1	0	0	1	0	0	1	↓
		$+3V_C$											0	1	1	0	
Fig. 76(e) N	$\mp n$	$-nV_C$	0	1	0	0	1	0	…	0	1	0	1	0	0	1	↓
		$+nV_C$											0	1	1	0	
Fig. 76(f) Z	∓ 0	$0\ V$	1	0	1	1	0	1	…	1	0	1	1	0	1	0	↑
		$0\ V$	1	0	1	1	0	1	…	1	0	1	0	1	0	1	↑

Note: "↓" means discharging of capacitor; "↑" means charging of capacitors.

4.3. 5-level Inverter Implementation (n = 2)

Fig. 4.4 shows the implemented 5-level inverter with possible switching states. It consist of a front side boost dc-dc converter, one switching cell (n = 2) and a 2L-VSI at the output stage.

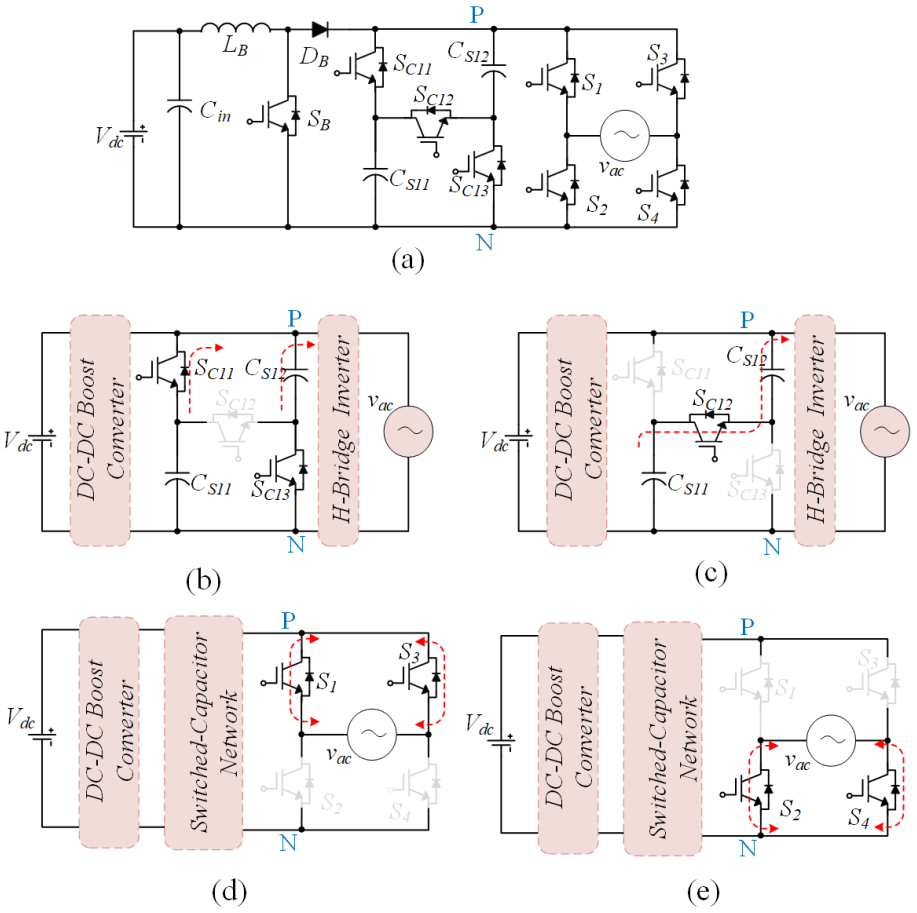


Fig. 4.4. (a) an example of the 5-level (n = 2) inverter implementation with its operating modes (b) State A or B [∓ 1] to create $\hat{V}_{PN} = V_C$ and $\hat{v}_{ac} = \mp V_C$, (c) State C [∓ 2] to create $\hat{V}_{PN} = 2V_C$ and $\hat{v}_{ac} = \mp 2V_C$, (d)&(e) State Z [∓ 0] to create $\hat{v}_{ac} = 0\ V$.

The switched capacitor has two switching states as shown in Fig. 4.4 (b) and Fig. 4.4 (c) to create level ∓ 1 ($\hat{V}_{PN} = V_C$ across PN and $\hat{v}_{ac} = \mp V_C$ at the output of the H-bridge) and level ∓ 2 ($\hat{V}_{PN} = 2V_C$ across PN and $\hat{v}_{ac} = \mp 2V_C$ at the output of the H-bridge). The additional zero states is created by the H-bridge VSI as shown in Fig 4.4 (d) and Fig 4.4 (e). The capacitors C_{S11} and C_{S12} charges through the input voltage in parallel (Fig. 4.4 (b), Fig. 4.4 (d) and Fig. 4.4 (e)) to ensure their voltage balancing and discharges to the load in Fig. 4.4 (b) and Fig. 4.4 (c) to create ∓ 1 and ∓ 2 voltage levels.

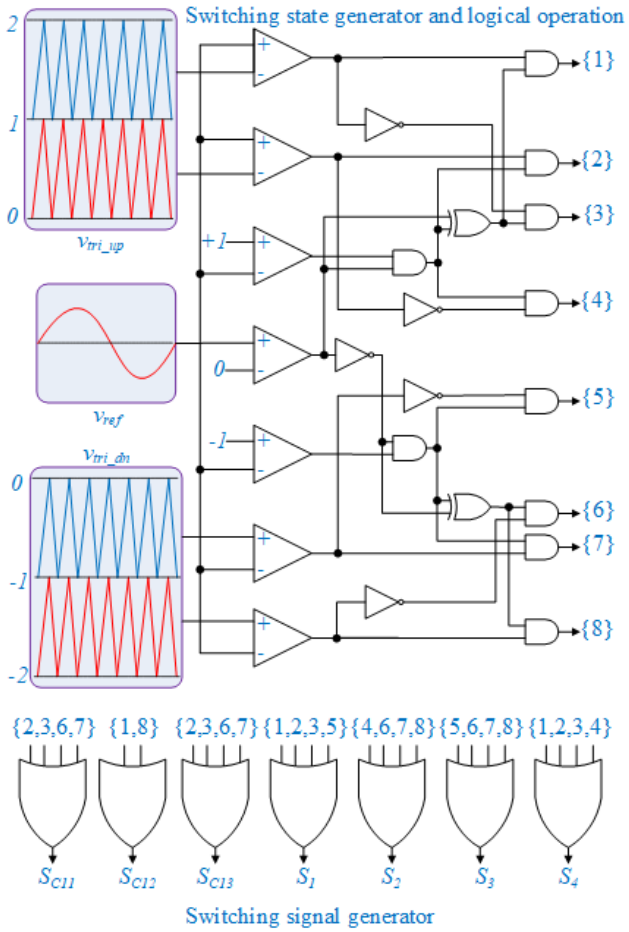


Fig. 4.5. An example of sinusoidal pulse width modulator implementation for 5-level inverter.

The inverter is controlled by a level-shifted sinusoidal PWM (LS-SPWM) as depicted in Fig. 4.5. A sinusoidal reference (v_{ref}) is used to compare with two level-shifted triangular carriers ($\hat{v}_{tri}$) for switching states computation, followed by a combinational logic circuit,

which is used to compute switching signals for each power switch. For 5-level circuit, the peak of fundamental ac output voltage is

$$\hat{v}_{ac} = MV_{PN} = \frac{2M\,V_{dc}}{1-D_b} \tag{58}$$

From this, the maximum peak of fundamental output voltage of 5-level inverter is equal to the dc-link voltage $V_{PN} = 2\,V_{dc}/(1 - D_b)$ at M = 1.0.

4.4. 7-level Inverter Implementation (n = 3)

Combinations of two switched capacitor-cells at the dc-link increase the number of voltage level from 5-level (n = 2) to 7-level (n = 3) generated at the ac side without increasing the number of active devices proportionally. The implemented 7-level inverter is shown in Fig. 4.6 with all possible switching states.

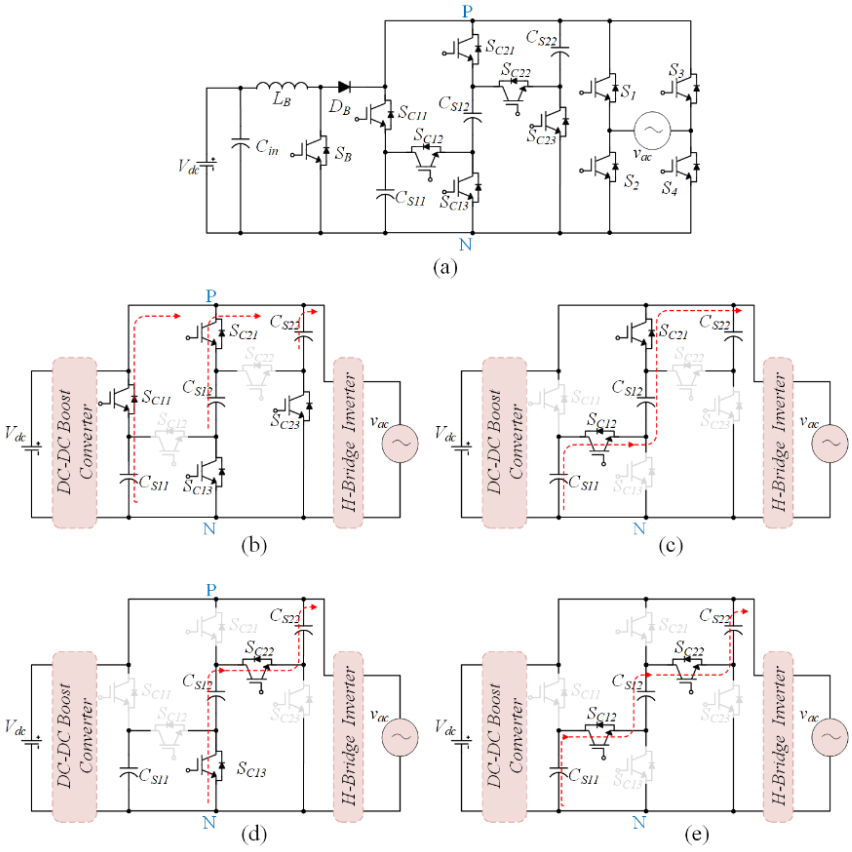


Fig. 4.6. (a) An example of the 7-level (n = 3) inverter implementation with its operating modes (a) level 1 to create $\hat{V}_{PN} = V_C$ and $\hat{v}_{ac} = \mp V_C$, (c) level 2 to create $\hat{V}_{PN} = 2V_C$ and $\hat{v}_{ac} = \mp 2V_C$, (d)&(e) to create $\hat{v}_{ac} = 0\,V$.

The switched capacitor has four switching states as shown in Fig. 4.6 (b) - Fig. 4.6 (e) to create level ∓ 1, ∓ 2 and ∓ 3 at the output voltage levels. Fig. 4.6 (b) shows ∓ 1 level, where all capacitor are connected in parallel to generate $\hat{V}_{PN} = V_C$ across PN and $\hat{v}_{ac} = \mp V_C$ at the output of the H-bridge. There are two redundant switching states to create ∓ 2 as shown in Fig. 4.6 (c) & Fig. 4.6 (d), where two capacitors are connected in series to generate $\hat{V}_{PN} = 2V_C$ across PN and $\hat{v}_{ac} = \mp 2V_C$ at the output of the H-bridge. Level 3 is created by adding voltage of all capacitors in series to generate $\hat{V}_{PN} = 3V_C$ across PN and $\hat{v}_{ac} = \mp 3V_C$ at the output of the H-bridge. The additional zero states is created by the H-bridge VSI as discussed before.

4.5. Components Selection and Design Guidelines

To design the proposed (2*n*+1)-level inverter few components such as input capacitor, boost inductor, SC, and filter need to be selected. The input capacitor C_{in} can be calculated by maximum output load current ($i_{O,max}$) and the permissible voltage ripple across the applying input voltage (ΔV_{in}) of the system. More specific selection can be done by minimum boost duty ratio ($D_{b,min}$) and switching frequency (ω_s) as expressed in (59).

$$L_B = \frac{2\,\pi\,V_{in}}{\Delta I_{in}\omega_s} \times \frac{(V_{out} - V_{in})}{V_{out}} \tag{59}$$

The proposed topology has boosting feature where a DC/DC converter is implemented at the front side. Therefore, the vital issue of this part is the selection of boost inductor (L_B) where this inductor value depends on input current ripple (ΔI_{in}).

$$C_{in} \geq \frac{2\,\pi\,i_{O,max}D_{b,min}}{\Delta V_{in}} \tag{60}$$

The switched-capacitor is related with the input voltage and can be selected by (61) where *k* is the maximum accepted voltage ripple. This value varies for different value of capacitors as the discharging time is different for capacitors.

$$C_{SN} > \frac{Q_N}{kV_{in}} \tag{61}$$

And the peak current of the capacitor can be present as follows,

$$I_{C_{SN}} = \frac{V_{in} - V_{C_{SN}}}{r_{C_{SN}} - 2 \times r_{0N}} \tag{62}$$

where, $r_{C_{SN}}$ is the equivalent series resistance (ESR) of the ($2n$+1)-level SC and turn-ON resistance of internal switching devices is represented by r_{0N}.

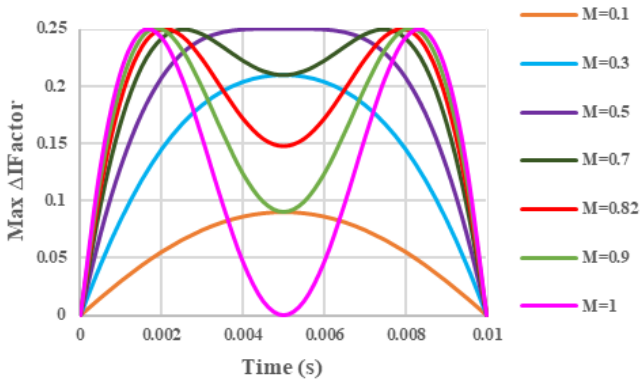


Fig. 4.7. Plot of ΔI_{Factor} vs. time at different modulation indexes.

The selection criteria mentioned here is for voltage source type inverters that only need inductor filters at the output to provide smooth output waveform. However, to reduce the inductor size usually a capacitor is used in parallel with the load, and hence, the solution here would be similar to the use of a low pass LC filter. The required inductance should be computed for the instant that the value of current ripple is maximum at output, which can be calculated from the maximum value of (63) [75, 77].

$$\Delta I_{Factor} = M\ sin\ (\omega_g t) - M^2\ sin^2\ (\omega_g t) \tag{63}$$

In (63), ω_g is the angular frequency of the grid. Fig. 4.7 demonstrates the maximum ripple factor with different modulation indexes, which is obvious that the maximum ripple factor is 0.25.

The required filter inductance can be calculated from (64) by selecting a limit factor for the inductor current ripple. Although, a high ripple value can reduce the filter size, the RMS

current and conduction losses will be increased. Therefore, it is recommended to not choose a value more than 20%.

$$L_f = \frac{2\pi\, V_{in}\Delta I_{Factor}}{\omega_s\, \Delta I_{in}} \tag{64}$$

The cut-off frequency (f_c) of output filter can be tuned and calculated from (65) by selecting a proper value for the filter capacitor C_f.

$$f_c = \frac{1}{2\pi\sqrt{\frac{L_f}{2}C_f}} \tag{65}$$

4.6. Thermal Analysis and Loss Calculation

To have a feeling of the loss contribution of different components of the proposed topology some simulations have been done with the loss model carried here. It should be noted that the losses have been explained theoretically for (2n+1) levels and in simulation it is considered that *n* is equal to 2.

Table 4.2.Semiconductor device losses for different input voltage with junction temperature when *n*=2

Power Devices	V_{in}= 102 V_{dc}			V_{in}=141 V_{dc}		
	Conduction Loss (W)	Switching Loss (W)	T_J (º C)	Conduction Loss (W)	Switching Loss (W)	T_J (º C)
D_B	4.293	0	32.48	4.9222	0	43.6
S_B	10.52	0.76	120.48	5.482	0.6612	100.5
S_{C11}	1.1794	0.2024	71.69	1.524	0.191	78.6
S_{C12}	0.9484	0.3121	78.62	1.28	0.3116	85.8
S_{C13}	1.1794	0.2024	71.69	1.524	0.191	78.6
S_1	0.372	0.0324	41.13	0.38	0.0337	42.33
S_2	0.3682	0.0213	28.55	0.3786	0.022	26.58
S_3	0.3707	0.0019	33.93	0.381	0.002	38.83
S_4	0.3737	0.0018	28.35	0.382	0.0018	26.42

The topology has covered by the heat sink, and the selected power switch parameters is for SCT3022ALGC11 and the diode parameters is for C5D50065D. The thermal impedance with conduction and switching (turn-ON/OFF) characteristics have been implemented from the datasheets. Moreover, the inductor losses are calculated by the designed magnetic core of

both inductors (boost and filter). Finally, the switched-capacitors and filter capacitor are also considered in the analysis.

The power losses and junction temperatures of all semiconductors are gathered in Table 4.2. The boost switch temperature is high for $V_{in} = 102\ V_{dc}$ which is mainly because of high RMS current stress leading to high conduction loss. On the other hand, the boost switch loss reduces for $V_{in} = 141\ V_{dc}$ which is because of the reduced RMS current and hence conduction loss. Moreover, the temperature is quite low for the H-bridge switches for both input voltages, and fewer losses have occurred through these four switches ($S_1 - S_4$).

Fig. 4.8 illustrates the loss breakdown of the proposed inverter. It is evident that most part of the loss is related to semiconductor losses and the large part of the loss with both high and low input voltage levels is for the boost switch and diode. In addition, the loss related to the voltage level increasing switches is considerable. On the opposite, the losses in the passive components are very low.

The losses on power devices have been calculated for 5-level, and 7-level configurations (see Fig. 4.9). A detailed thermal analysis and loss calculation using PLECS software. It can be seen that in 7-level configuration, the power loss in SC network is increased by 4% due to additional SCs used for level extension.

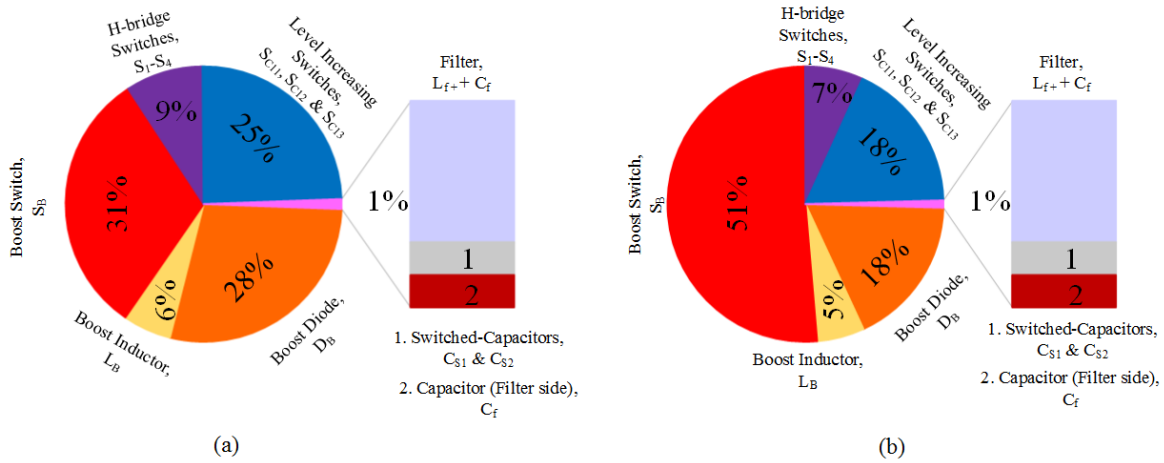


Fig. 4.8. Losses in full load condition for proposed inverter (when n=2) (a) V_{in}= 141V_{dc}, and (b) V_{in}= 102 V_{dc}.

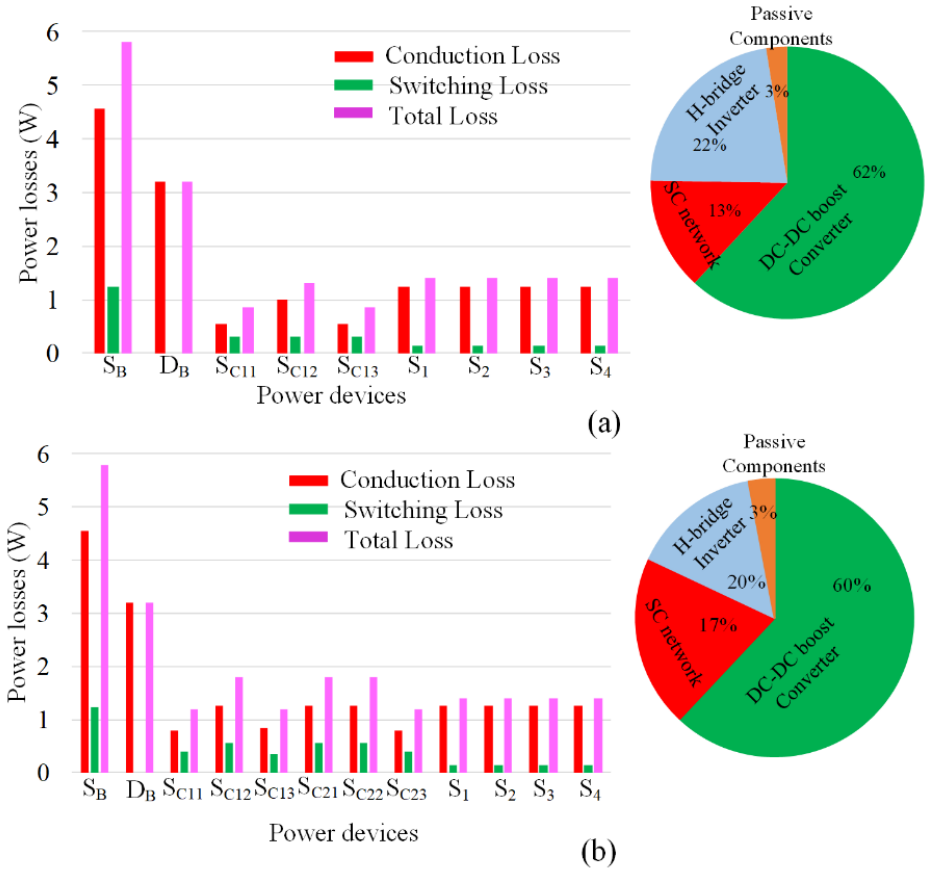


Fig. 4.9. Loss distribution analysis for full load condition (500VA), (a) 5-level configuration, and (b) 7-level configuration.

4.7. Comparison of the Proposed Topology with Various Suggested Topologies

In this section a comparative analysis is carried out with the five well-known SC-based inverters [73]-[77], [127] for (2n+1) levels or n cells. Table 4.3 shows the number of components used in each of the (2n+1)-level inverter. Furthermore, in Fig. 4.10 the number of required SCs in each inverter is compared graphically with the number voltage levels (N_L) in the inverters.

Table 4.3.Comparison of different items for various (2n+1)-levels inverter

Comparison items	Topology [74]	Topology [75]	Topology [76]	Topology [77]	Topology [127]	proposed
No. of Switches (N_S)	4.(n-1)+4	2n+4	n+4	3n+3	5n-1	3n+2
No. of Diodes (N_D)	0	0	2n-2	n	n-1	1
No. of SC (C_S)	n-1	n-1	n-1	n	n-1	n

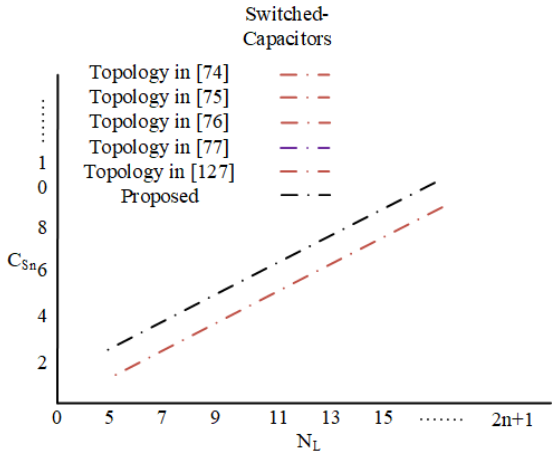


Fig. 4.10. Comparison of used switched-capacitor for various (2n+1)-level inverters.

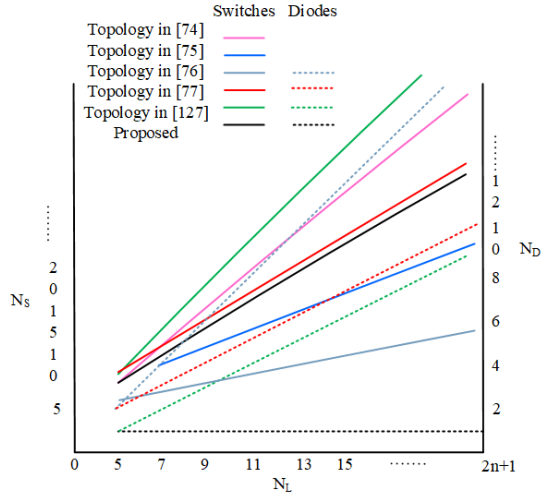


Fig. 4.11. Comparison of semiconductor devices for various (2n+1)-level inverters.

Morover, in Fig. 4.11 the number of required diodes and switches for each inverter are compared graphatically based on N_L. Fig. 4.12 shows the comparison of TSV for different inverters where the TSV formula is written for each inverter. It is clear that the proposed topology has the lowest TSV among other similar topologies. The TSV in the topologies in [76] and [77] is increased nonlinearly whereas it is increased linearly in the topologies in [75] and [127].

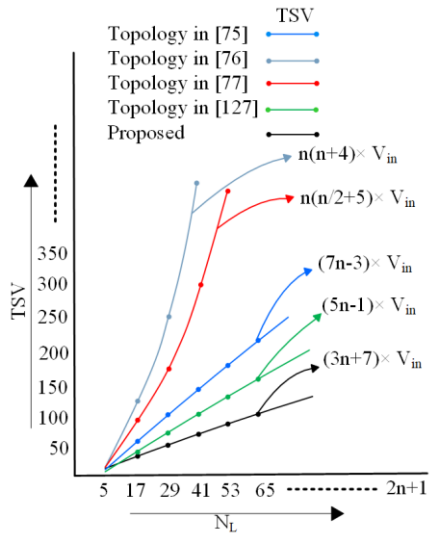


Fig. 4.12. Comparison of TSV for various (2n+1)-level inverters.

Compared to all presented topologies, the proposed topology shows a very low TSV with a linearly increasing slope due to the increase of the voltage level. The voltage stress of all elements is not equal for the proposed topology. The voltage stress of H-bridge and boost switches are equal to $1\times V_{PN}$ and it is reduced to half $\frac{1}{2}\times V_{PN}$ for level increasing switches. Hence, the TSV is equal to $1\times V_{PN}+3n\times 0.5\times V_{PN}+4n\times 1\times V_{PN}=0.5(3n+7)\times V_{PN}$.

Another important aspect of the (2n+1)-level inverter is the prototype implementation size. The size mainly depends on the filter and SC values. In [74], different values of SC have been used as 2.2 mF - 4.7 mF and they did not implement an output filter in the prototype. The topology presented in [75] use 147 µF, and 1 mF SCs, and they used small LC output filter. Hence, the size is quite smaller compared with the topology presented in [74]. In [76] and [127] a very high electrolytic SC (4.7 mF) has been used compared with the one used in the topology presented in [77]. In the proposed topology a 680 µF SC with a small output LC filter has been used. As a result, the proposed topology has a smaller porotype size than the mentioned suggested topologies. The required space for the gate drive circuit of the topologies are assumed to be the same.

To understand the cost of the proposed (2n+1)-level inverter, a cost analysis has been done considering price of the components used in the prototypes based on the data provided in Table 4.4. Fig. 4.13 shows the cost comparison of the different inverter topologies. It should be noted that the SC prices are not fixed as different topologies use different values of SCs. It is also a reason affecting the printed circuit board (PCB) size and cost. Therefore, the total cost (C_T) of a (2n+1)-level inverter can be calculated from (66).

$$C_T = (K_1 + K_3) \times N_S + K_2 \times N_D + C_{Sn} \times K_4 + PCB_C \quad (66)$$

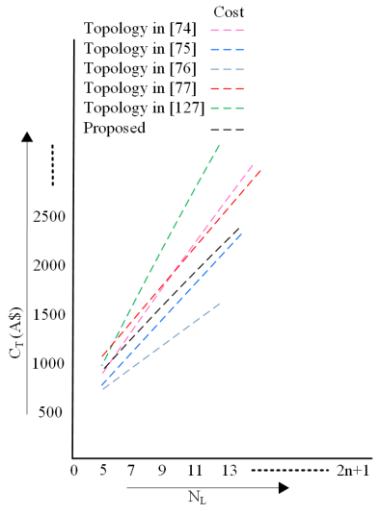


Fig. 4.13. Comparison of total cost for various (2n+1)-level inverters.

where K_1 represents the switch price, K_2 represents the diode price, K_3 represents the gate drive circuit price, K_4 represents the SC price that is not fixed and change by the number of SC cells, and so the PCB cost (PCB_C) alter by the required size for SCs. The price value has taken from au.rs-online.com. The prices may vary based on market growth.

Table 4.4. Price list of different component

Component name	*Price (A$)/component
Switches (SCT3022ALGC11)	68.42
Diode (C5D50065D)	29.209
Gate drive circuit	23.809
Switched-capacitor (150 µF-4700 µF)	3.50-7.76

*A$= Australian Dollar

4.8. Results and Discussions

4.8.1. Components Selection for Simulation and Experiment of Proposed Topology II

The performance of the proposed topology is first simulated by MATLAB-Simulink using the PLECS toolbox and then verified experimentally with a 500 VA laboratory prototype. In order to precisely verify the performance of the proposed inverter and to have fare comparison, same parameters have been used for both the simulation and experiment that are listed in Table 4.5.

Table 4.5.Parameters for Simulation and Experimental

Description	Values/Parameters
Input Voltage (V_{in})	102 V_{dc} and 141 V_{dc}
Output Voltage (V_{out})	230 V_{ac}
Rated Power (P_o)	500 VA
Switching Frequency (f_{SW})	20 kHz
Line frequency, (f_m)	50 Hz
Modulation Index, M	0.82
Boost Diode, (D_B)	C5D50065D (650 V, 50A)
Switched-Capacitors, (C_{S1} and C_{S2})	0.68 mF (LLS2E681MELA)
Switches, (S_B, $S_{C11} - S_{C13}$, $S_1 - S_4$)	SCT3022ALGC11 (650 V, 93 A, 22 m Ω)
Filter inductor, (L_f)	0.68 mH
Filter Capacitor, (C_f)	4.7 µF
Load, R	105 Ω
Load, R-L	92.5 Ω, 70 mH
Dead time	300 ns
Controller	sb-RIO GPIC
Gate Drive Circuit (GDC_{SB}, $GDC_{SC11} - GDC_{S13}$, $GDC_{S1} - GDC_{S4}$)	
Optocoupler IC	ACPL-P343
DC/DC converter	RP1212D
Resistor	10 Ω, 47 kΩ
Capacitor	1 µF, 100 µF

4.8.2. Hardware Setup

The experimental setup is shown in Fig. 4.14 (a) and the top and bottom side views of the prototype are displayed in Fig. 4.14 (b) and Fig. 4.14 (c), respectively. The required pulses are created by the sb-RIO GPIC controller from National Instrument (NI) based on carrier-based PWM modulation technique. To turn ON the MOSFET with a proper voltage level, the

gate drive circuit generates 18 V from an isolated DC/DC converter and the voltage isolation between the control board and the power circuit is achieved by an optocoupler. The gate driver circuit for the MOSFETs of the proposed inverter prototype can be found on the bottom side of the PCB (see Fig. 4.14 (c)).

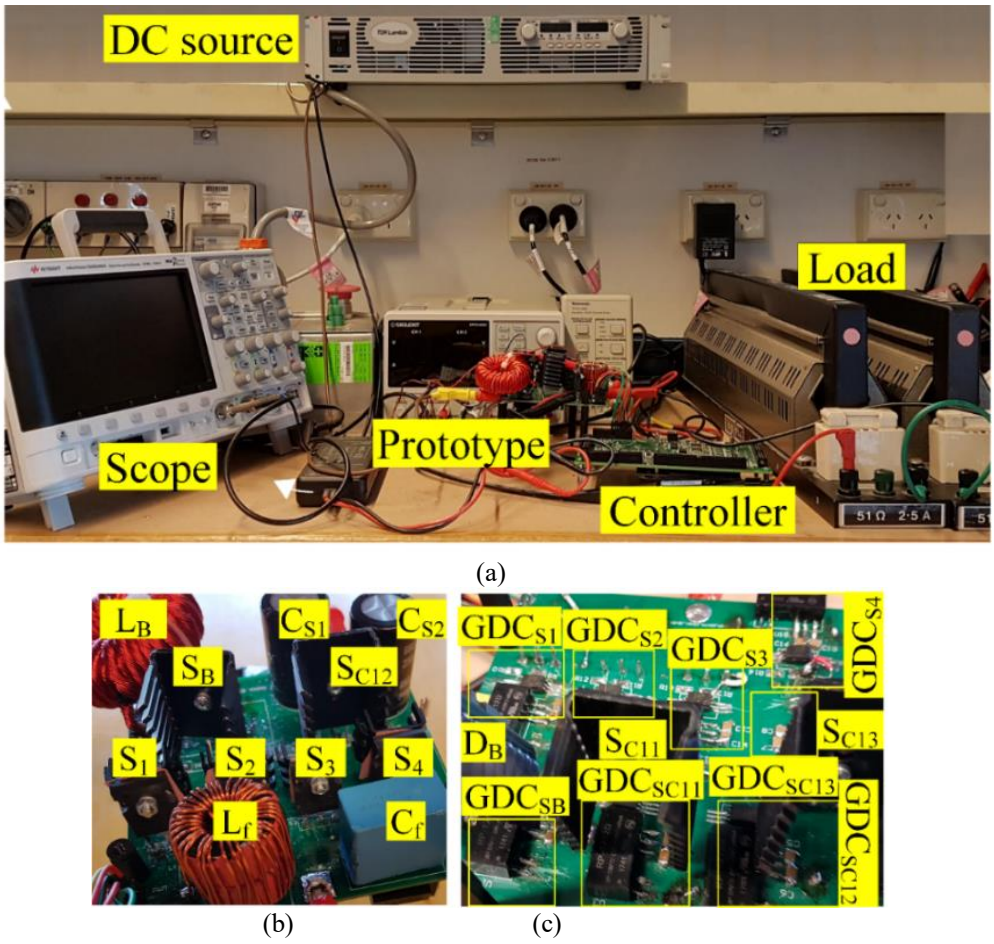


Fig. 4.14. Prototype and measurement platform of 5-level inverter showing: (a) test setup, (b) top view of the inverter and (c) bottom view of the inverter.

4.8.3. Simulation and Experimental Results

The controller sb-RIO GPIC is interfacing with LabVIEW software and operating the switching pulses through the LabVIEW software. The PWM gate pulses for all active switching devices that are generated by the sb-RIO GPIC are illustrated in Fig. 4.15. Fig. 4.15 (a) shows the switching pulses of level increasing switches where switches S_{C11} and S_{C13} are operated with the same switching pulses. On the other hand, the switching pulses of H-bridge

switches are shown in Fig. 4.15 (b). The voltage across the all switches are illustrated in Fig. 4.16 and Fig. 4.17. Simulation and experimental waveforms are shown together where it is possible to observe the similarity. Fig. 4.16 (a) and Fig. 4.16 (b) display the simulated and experimental voltage waveform of switch S_B, S_{C12}, S_{C11}, and S_{C13}, respectively.

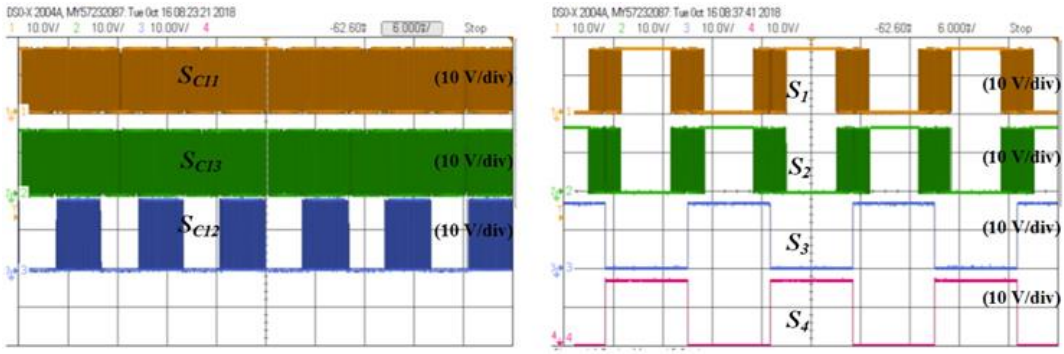


Fig. 4.15. The experimentally generated gate pulses for active switches.

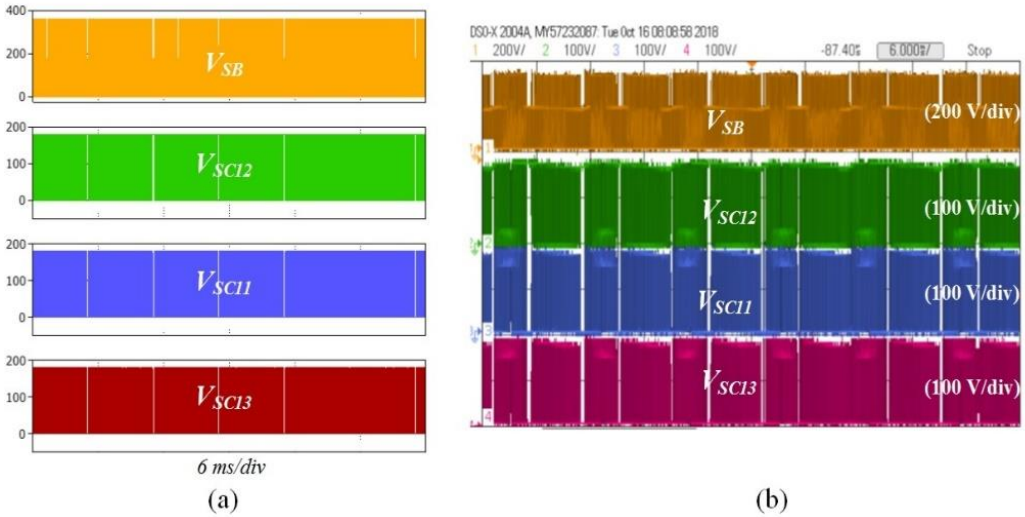


Fig. 4.16. The voltage stress of switch S_B, S_{C12}, S_{C11}, and S_{C13}, (a) simulation waveform, and (b) corresponding experimental waveform.

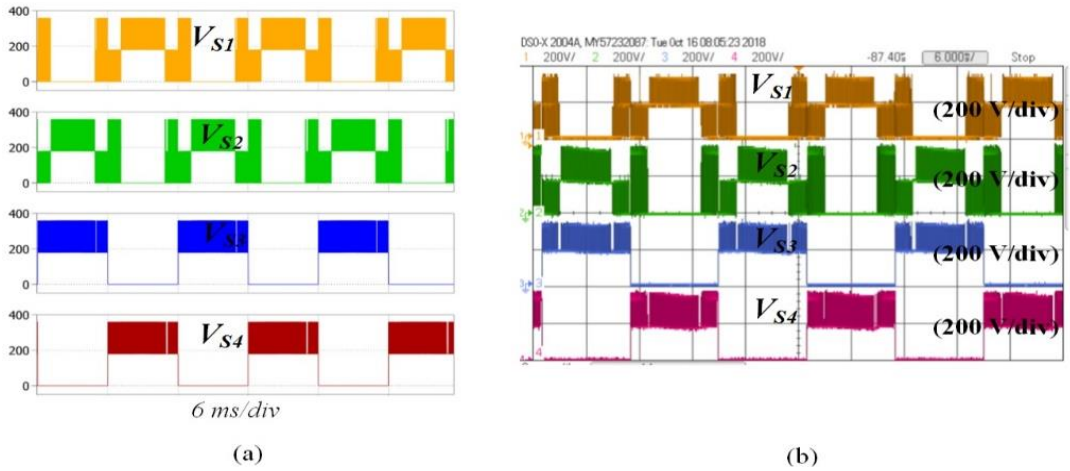


Fig. 4.17. The voltage stress of switch S_1, S_2, S_3, and S_4, (a) simulation waveform, and (b) corresponding experimental waveform.

On the other hand, the voltage stress of H-bridge side switches are shown in Fig. 4.17. Fig. 4.18 shows the waveform of the input voltage and the dc-link voltage. The dc-link voltage level is created by the voltage step-up converter in which the voltage level is dependant to the boost duty cycle (D_{DB}).

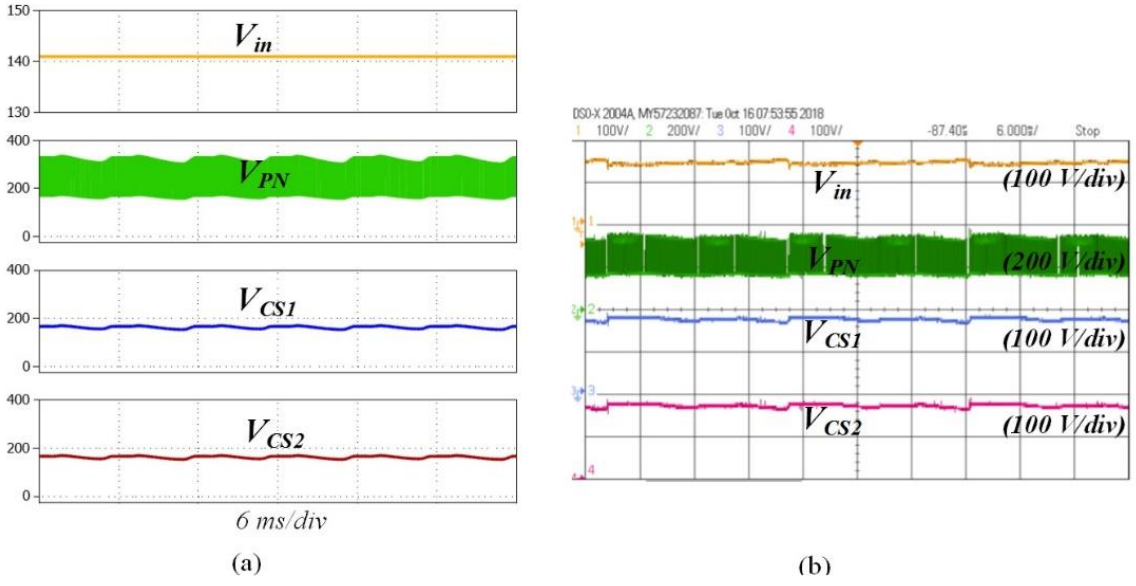


Fig. 4.18. The input voltage, DC-link voltage, voltage across the switched-capacitors, (a) simulation waveform, and (b) corresponding experimental waveform.

By applying 30% boost duty cycle, the required 230 V_{ac} can be achieved by 141 V_{dc} input voltage and then the dc-link voltage is fluctuated between 180 V to 360 V. Moreover, the voltage across the SCs are presented in Fig. 4.18. The output voltage and current are displayed in Fig. 4.19. In simulation, the RMS value of the output voltage is 228 V and the RMS value of the output current is 2.3 A, and the peak values for the output voltage and current are shown in Fig. 4.19 (a). On the other hand, in the experiment the RMS value of the output voltage for same input voltage is 228 V and the RMS value of the output current is 2.2 A.

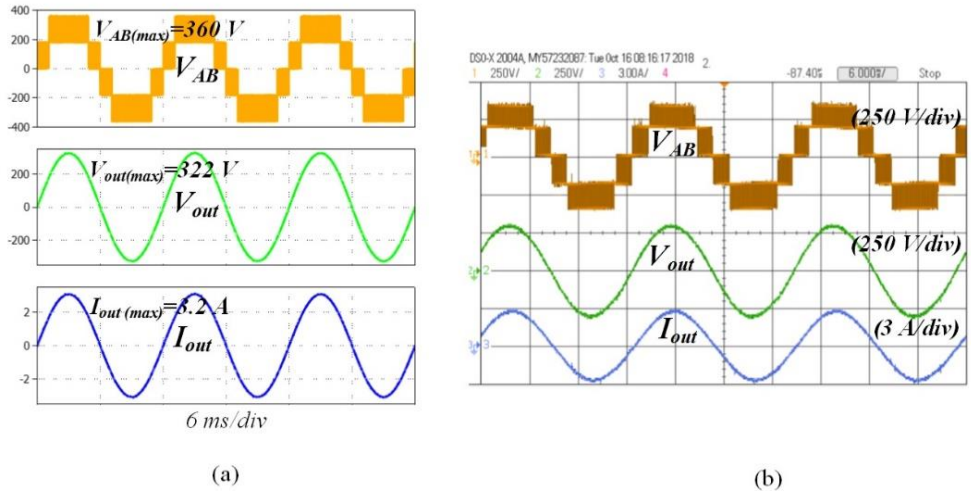


Fig. 4.19. The inverter voltage without filter, output voltage and current after the LC filter for resistive (R) load. (a) Simulation waveform, and (b) corresponding experimental waveform.

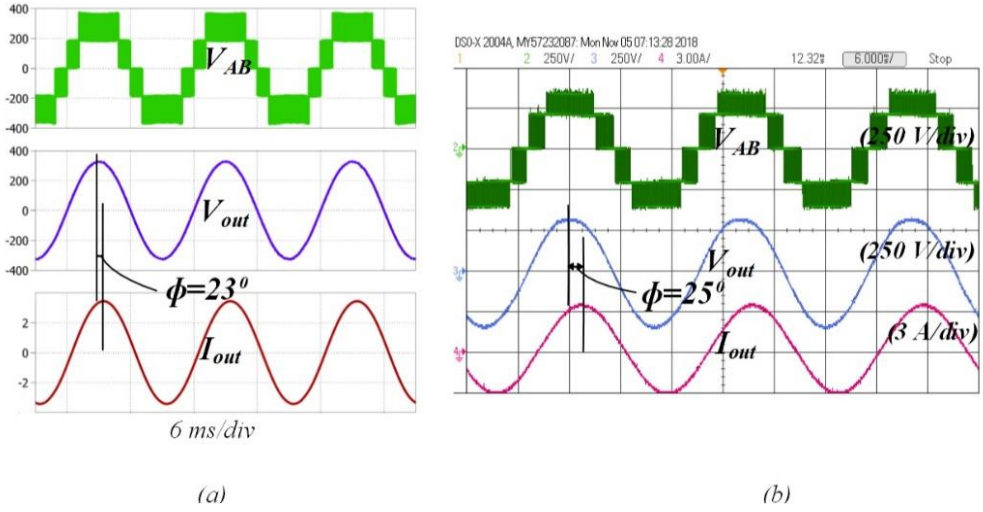


Fig. 4.20. Inverter voltage, output voltage and current after using the LC filter for resistive-inductive (R-L) load, (a) simulation waveform, and (b) corresponding experimental waveform.

Moreover, Fig. 4.20 shows the reactive power capability of the inverter prototype connected to a resistive-inductive (R-L) load and compared with simulated waveform for the same 141 V_{dc} input voltage. In the second case the boost duty cycle is changed to 50%, and as a result 102 V_{dc} is required to achieve 230 V_{ac} output voltage and then the dc-link voltage is fluctuated between 175 V to 356 V (see Fig. 4.21).

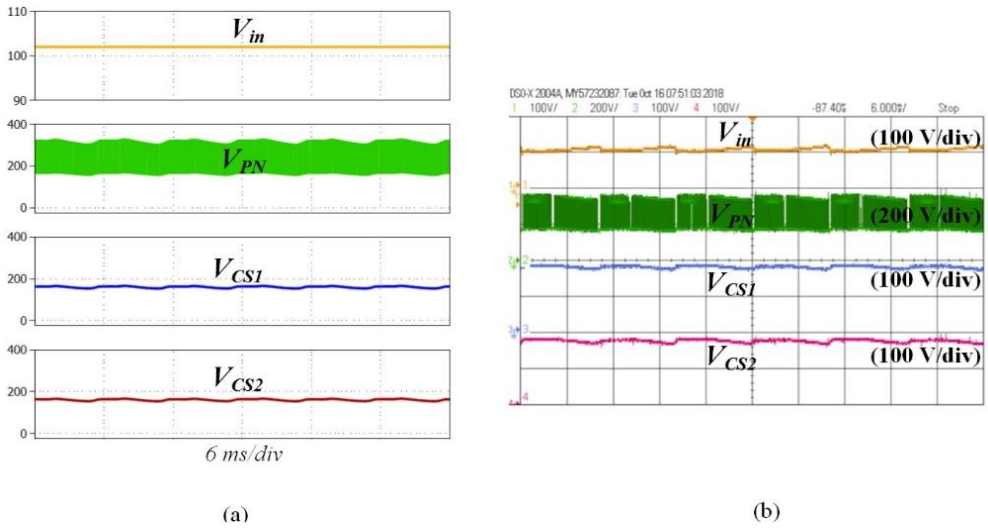


Fig. 4.21. The input voltage, DC-link voltage, voltage across the switched-capacitors, (a) simulation waveform, and (b) corresponding experimental waveform.

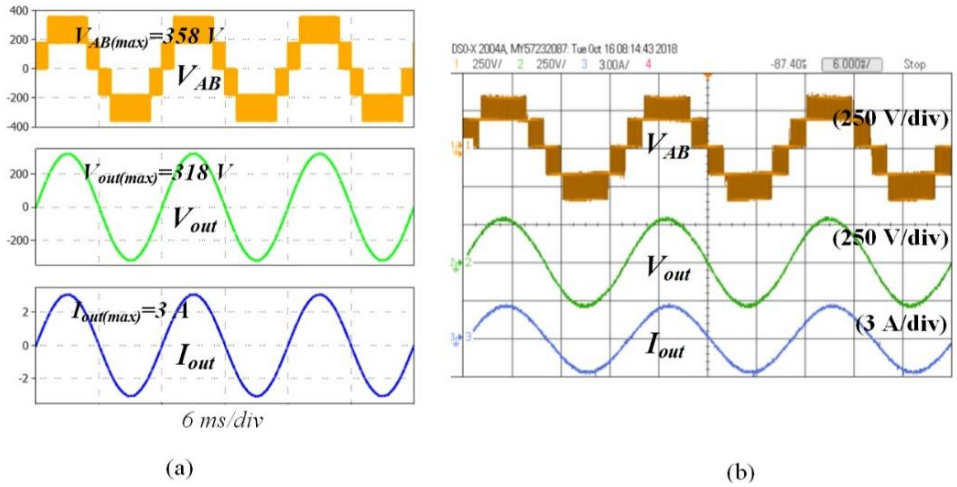


Fig. 4.22. The inverter voltage without filter, output voltage and current after the LC filter for resistive (R) load, (a) simulation waveform, and (b) corresponding experimental waveform.

Fig. 4.21 (b) shows the experimental waveforms of the input voltage, the dc-link voltage, and the voltage across the SCs (C_{S1}, and C_{S2}). Moreover, the output voltage and current waveform for 50% boost duty cycle is shown in Fig. 4.22.

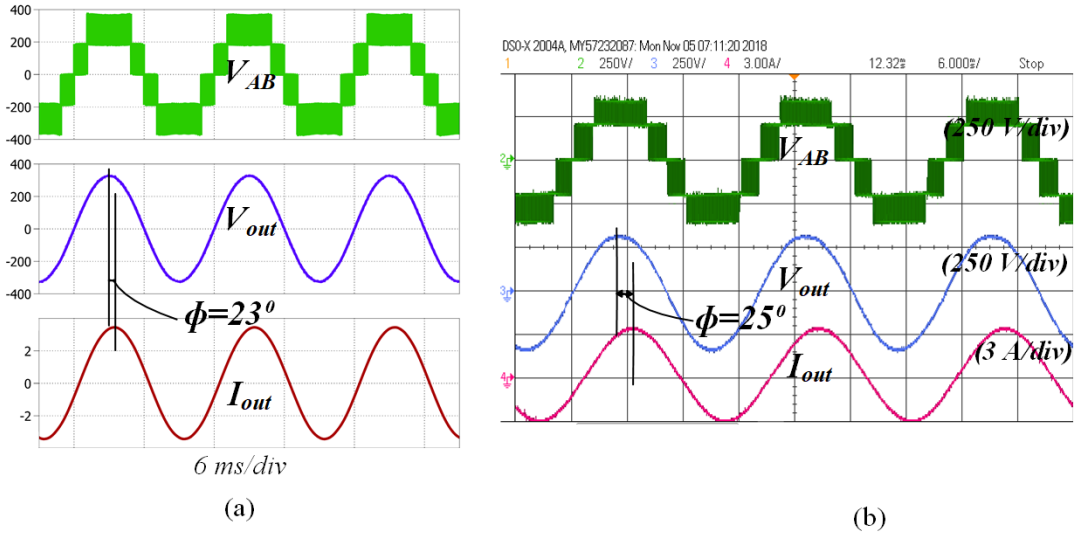


Fig. 4.23. Inverter voltage, output voltage and current after using the LC filter for resistive-inductive (R-L) load. (a) Simulation waveform, and (b) corresponding experimental waveform.

The peak voltage and current level are shown in the simulation waveform and the RMS value of the output voltage is 225 V_{ac}, and the RMS value of the output current is 2.18 A. On the other hand, in the experiment the RMS value of the output voltage is 223 V_{ac} and the RMS value of the output current is 2.1 A. The ability of delivering reactive power to the ac-side is also tested successfully in this operating condition with cos φ = 0.9 (φ = 25º lagging current) as shown in Fig. 4.23 (b) and compared with the simulation result with the power factor of 0.92 (φ = 23º lagging current).

Some measurement results from the 7-level (n=3) inverter are also presented at the end to support the analysis made in Section II. In this case, the Simulink model is implemented in OPAL-RT to get some useful results from the real-time model, such as 7-level output voltage, capacitor voltages and input and output voltages as shown in Fig. 4.24. The presented results show the efficacy of the proposed concept for any level inverter.

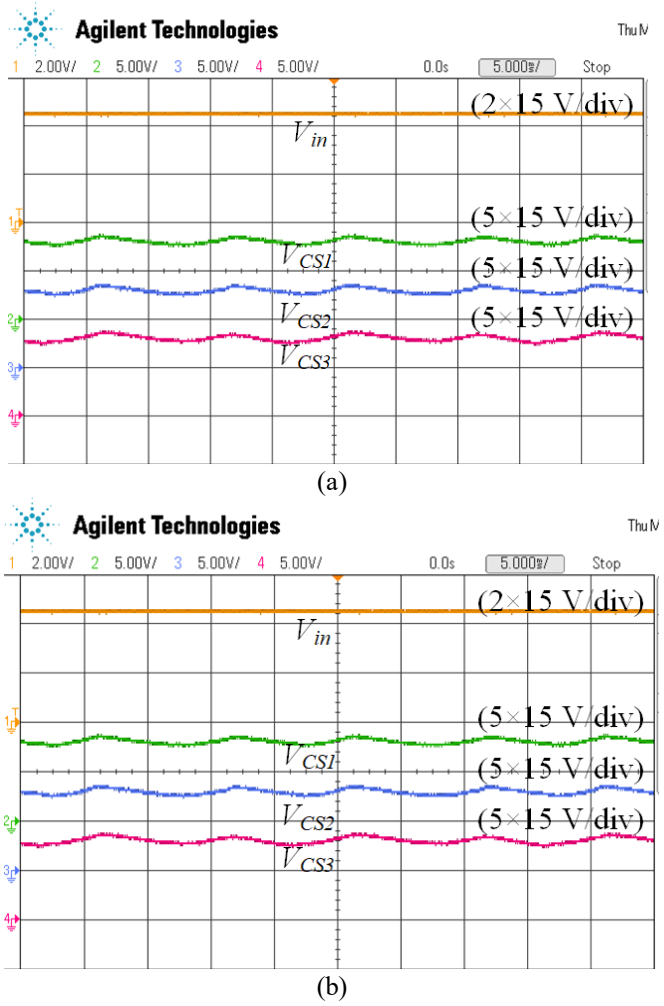


Fig. 4.24. Measured waveform of the 7-level inverter: (a) the input voltage, voltage across the switched-capacitors and (b) inverter voltage, output voltage and current after using the LC filter for resistive (R) load.

The overall efficiency of the proposed converter (when n = 2) is investigated and compared between the calculated and experimental results for different load levels as depicted in Fig. 4.25. A FLUKE 345 power quality clamp meter has been used to measure the efficiency of the prototype. The maximum measured efficiency is equal to 98.40% with the input voltage of 141 V_{dc} and the load level of 25% of the full load. Moreover, the lowest efficiency measurement is for full load condition with the lowest input voltage level of 102 V_{dc} that is equal to 93.90%. In Fig. 4.25, the efficiency curves are illustrated for two different input voltages where the calculated results are quite matched with the experimental results.

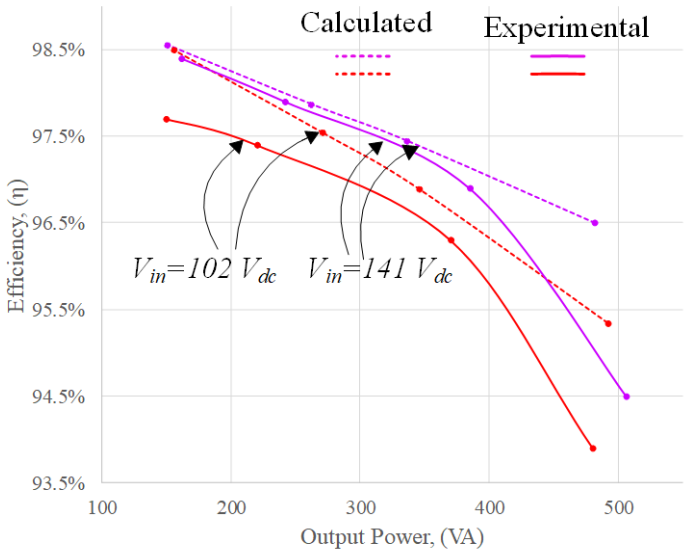


Fig. 4.25. Power conversion efficiency of the 5-levels inverter prototype for two input voltages (V_{in}= 141V_{dc}, and V_{in}= 102V_{dc}).

The calculated efficiency varies from 96.50 % to 98.56% when the input voltage is 141 V_{dc} and the experimental measurement varies from 94.50% to 98.40%. On the other hand, when the input voltage is changed to 102 V_{dc} for 50% boost duty cycle, the calculated efficiency varies from 95.35% to 98.50% and the measured efficiency varies from 93.90% to 97.70%.

4.9. Summary

The proposed inverter has the ability to increase the voltage level with a single low input voltage source and benefits from low voltage stress on the semiconductors. The mathematical and theoretical analysis of the proposed topology derived and presented. Moreover, a thermal analysis explained in detail to show the relationship between the power losses occur in each semiconductor devices and the junction temperature of the devices. In addition, a detailed loss analysis conducted for different input voltage levels. Moreover, the comparison with existing single-phase five-level inverters verified that the proposed inverter is a viable and efficient solution when it is required to supply form a low voltage dc source. Furthermore, the simulation and experimental waveforms of an example 500 VA prototype displayed in parallel to demonstrate the validity of the proposed inverter.

Chapter 5

Dual Mode Common Grounded Type 5-Level Inverter (Proposed Topology III)

5.1. Circuit Structure

The topology of the proposed dual-mode five-level common grounded type (5L-DM-CGT) transformerless inverter consists of nine switches, and two switched capacitors as shown in Fig. 5.1. The switched capacitors are used to attain different voltage levels by charging and discharging in predefined switching states. During the inverter's operation, the capacitors are charged in one of two fashions: either charged in parallel and discharged in series or charged in series and discharged in parallel. The choice depends on the input voltage and the desired magnitude of the output voltage.

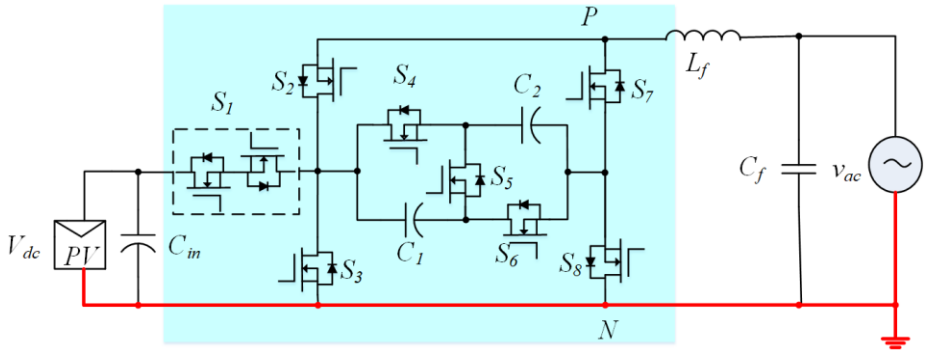


Fig. 5.1. Proposed 5L-DM-CGT transformerless inverter topology.

The voltage across capacitors C_1 and C_2 is half of the DC-link voltage ($V_{C1} = V_{C2} = V_{dc}/2$) in buck mode and equal to the DC-link voltage ($V_{C1} = V_{C2} = V_{dc}$) in boost mode. Five output voltage levels, as shown in (67), can be achieved, which are defined respectively as 0, ±1, and ±2.

$$V_{PN} = \begin{cases} 0V_{dc}, \pm\frac{1}{2}V_{dc}, \pm V_{dc} & \text{Buck mode} \\ 0V_{dc}, \pm V_{dc}, \pm 2V_{dc} & \text{Boost mode} \end{cases} \quad (67)$$

Now the RMS value of the output voltage during different modes of operation are given in (68), where M is the modulation index.

$$v_{RMS} = \begin{cases} \frac{M \times V_{dc}}{2\sqrt{2}} & \text{Buck mode} \\ \frac{2 \times M \times V_{dc}}{\sqrt{2}} & \text{Boost mode} \end{cases} \quad (68)$$

To simplify the circuit analysis, the following conditions are assumed:

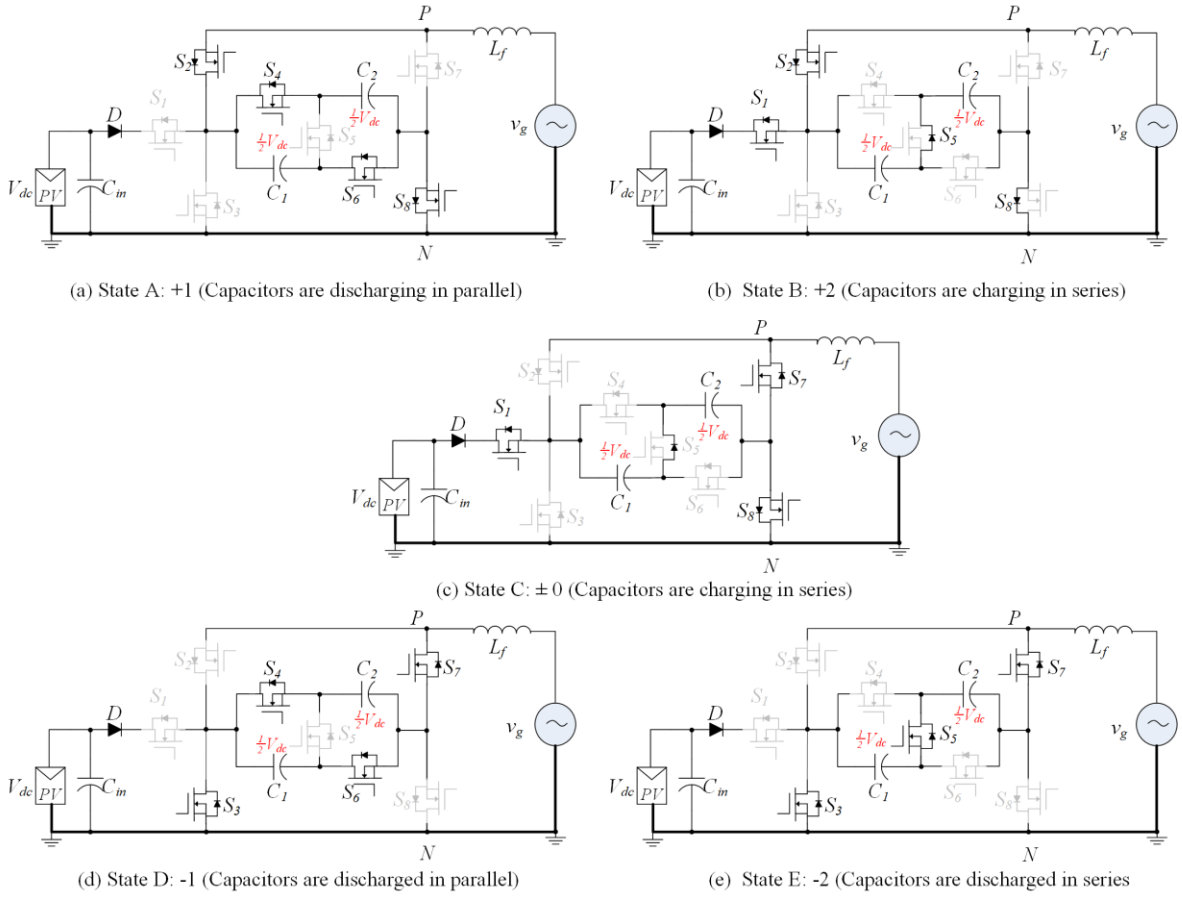
i. PV panel is considered as a fixed DC power supply.
ii. Capacitors are large enough to keep the voltage constant in one switching period.
iii. The power MOSFETs are treated as ideal. The ON-state resistance and parasitic capacitances of the switches are neglected. In addition, the forward voltage drop across the anti-parallel diode of each switch is ignored.
iv. The equivalent series resistance (ESR) of each capacitor is neglected.

5.2. Operating Principle

The inverter operates in two modes, whilst producing the same AC voltage over wide input voltage range. In addition, both modes have 5 levels of output voltage, which simplify and unify the output filter design. The details of each operation mode are discussed below:

5.2.1. Buck Mode

There are five modes of operation in buck-mode and each produces five different output voltages: $0V_{dc}, \pm\frac{1}{2}V_{dc}$, and $\pm V_{dc}$. Fig. 5.2 (a) shows State A where the inverter output before the filter is $+1/2\,V_{dc}$.



(a) State A: +1 (Capacitors are discharging in parallel)

(b) State B: +2 (Capacitors are charging in series)

(c) State C: ± 0 (Capacitors are charging in series)

(d) State D: -1 (Capacitors are discharged in parallel)

(e) State E: -2 (Capacitors are discharged in series

Fig. 5.2. Switching states of the inverter in buck mode.

The capacitors C_1 and C_2 are discharged in parallel through the switches S_2, S_4, S_6, and S_8. Fig. 5.2 (b) shows State B which produces a voltage level $+V_{dc}$ and simultaneously charges the capacitors in series via the switch S_5. To prevent a short circuit in the capacitors, S_4 turns

off. State C is the zero state (see Fig. 5.2 (c)). In this state, the capacitors are charged in series through the switch S_5, and the capacitors are charged up to $+1/2\,V_{dc}$.

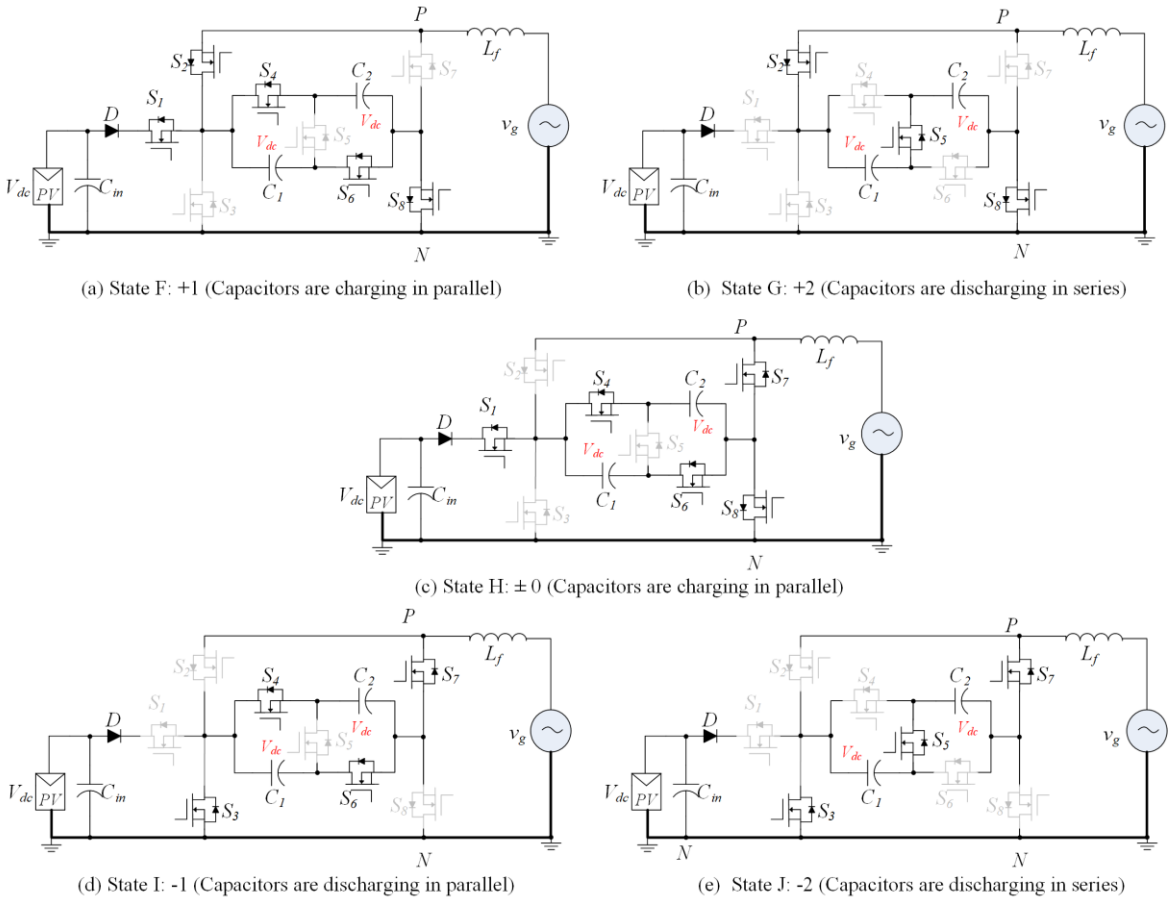
$$V_{PN} = \begin{cases} V_{C1} \parallel V_{C2} = \frac{1}{2} \times V_{dc} \parallel \frac{1}{2} \times V_{dc} = \frac{1}{2} \times V_{dc}, \text{State A} \\ V_{C1} + V_{C2} = \frac{1}{2} \times V_{dc} + \frac{1}{2} \times V_{dc} = V_{dc}, \text{State B} \\ 0\ , State\ C \\ V_{C1} \parallel V_{C2} = \left(-\frac{1}{2} \times V_{dc}\right) \parallel \left(-\frac{1}{2} \times V_{dc}\right) = -\frac{1}{2} \times V_{dc}, \\ \text{State D} \\ V_{C1} + V_{C2} = \left(-\frac{1}{2} \times V_{dc}\right) + \left(-\frac{1}{2} \times V_{dc}\right) = -V_{dc}, \\ State\ E \end{cases} \quad (69)$$

At the same time, switches S_7 and S_8 turn on to form a bidirectional path for the current to flow during the zero state. Fig. 5.2 (d) shows State D where the capacitors are discharged in parallel and the output current flows through the switches S_3, S_4, S_6, and S_7. Hence, the output of the inverter before the filter is $-1/2\,V_{dc}$. Fig. 5.2 (e) shows the continuation of the capacitor discharging in series which creates the voltage level equal to $-V_{dc}$. The variable DC-link voltage is represent by (69) using different combinations of voltages across the capacitors for different output voltage levels.

5.2.2. Boost Mode

In this mode, the inverter produces twice the peak of the AC voltage as compared to the buck mode operation. Hence to keep the same AC voltage output, the DC-link voltage can be reduced by half. There are also five operation modes that produces five levels of output voltage, i.e., $0V_{dc}, \pm V_{dc}$, and $\pm 2V_{dc}$. Fig. 5.3 (a) shows State F, where the inverter output before the filter is + $1V_{dc}$. Capacitors C_1 and C_2 charge in parallel through the switches S_1, S_4, S_6 and S_8. During this state, C_1 and C_2 also serve as an additional DC-link capacitor. Fig. 5.3 (b) shows State G, which produces a voltage level $+2V_{dc}$ by discharging the capacitors in series via S_5. To prevent a short circuit the capacitors, S_4 and S_6 are off. State H is the zero state (see Fig. 5.3 (c)). In this state switch S_2 is off, which allows the capacitors to be charged in parallel. Switches S_7 and S_8 are closed to form a bidirectional path for the current to flow during the zero state. Fig. 5.3 (d) shows State I, where capacitors C_1 and C_2 are connected in

parallel to provide a DC-link voltage of $-V_{dc}$. During this mode, S_3, S_4, S_6 and S_7 are on, and S_5 and S_8 are off. Assuming C_1 and C_2 are equal, the grid current splits equally between the two capacitors. Switch S_1 is off during this state to prevent a short circuit on the DC input. Switch S_2 remains off for the complete negative cycle.



(a) State F: +1 (Capacitors are charging in parallel)

(b) State G: +2 (Capacitors are discharging in series)

(c) State H: ± 0 (Capacitors are charging in parallel)

(d) State I: -1 (Capacitors are discharging in parallel)

(e) State J: -2 (Capacitors are discharging in series)

Fig. 5.3. Switching states of the inverter in boost mode.

Fig. 5.3 (e) shows the State J where the switching state is similar to State G. In this state, the capacitors are connected in series to boost the voltage level. However, S_1, S_2, and S_8 are off, S_3 and S_7 are on, and the capacitors are connected with reverse polarity to the output filter. In State G, the switch S_4 and S_6 are turned off and S_5 is turned on.The capacitors are connected in series rather than in parallel to the output filter, doubling the voltage. During this mode, the current in C_1 and C_2 is equal to the grid current. The resulting voltage $-2V_{dc}$ is applied to the output filter.

On the other hand, the voltage level is generated through the voltages across the

capacitors as shown in (70) for the boost mode.

Table 5.1 shows the switching states in both modes where the charging/discharging condition of the capacitors in the individual states are shown.

$$V_{PN} = \begin{cases} V_{C1} \parallel V_{C2} = V_{dc} \parallel V_{dc} = V_{dc}, \text{State A} \\ V_{C1} + V_{C2} = V_{dc} + V_{dc} = 2V_{dc}, \text{State B} \\ 0\ , \text{State C} \\ V_{C1} \parallel V_{C2} = (-V_{dc}) \parallel (-V_{dc}) = -V_{dc}, \text{State D} \\ V_{C1} + V_{C2} = (-V_{dc}) + (-V_{dc}) = -2V_{dc}, \text{State E} \end{cases} \quad (70)$$

Table 5.1. Switching states of the proposed inverter and the charging/discharging states of capacitors.

Mode	State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	C_1	C_2
Buck	A	0	1	0	1	0	1	0	1	▼	▼
	B	1	1	0	0	0	0	0	0	▼	▼
	C	1	0	0	0	0	0	1	1	▲	▲
	D	0	0	1	1	0	1	1	0	▼	▼
	E	0	0	1	0	1	0	1	0	▲	▲
Boost	F	1	1	0	1	0	1	0	1	▲	▲
	G	0	1	0	0	1	0	0	1	▼	▼
	H	1	0	0	1	0	1	1	1	▲	▲
	I	0	0	1	1	0	1	1	0	▼	▼
	J	0	0	1	0	1	0	1	0	▼	▼

Note: 1=switch ON, 0=switch OFF, ▼ = charging, ▲ = discharging

5.3. Modulation Technique

The inverter is controlled by a level-shifted sinusoidal pulse width modulation (LS-SPWM) technique as depicted in Fig. 5.4.

A sinusoidal reference (v_{ref}) is compared with two level-shifted triangular carriers ($\hat{v}_{tri}$) for switching states computation, followed by a combinational logic circuit, which is used to compute switching signals for each power switch (see Fig. 5.4 (a)). Figs. 5.4 (b) and 5.4 (c) show the switching signal generation for buck mode and boost mode respectively that can be selected from the operating principle of each mode. Through the switching signal of each switch and parallel/series charging and discharging capability of flying-capacitors, a 5-level output voltage can be generated for both modes.

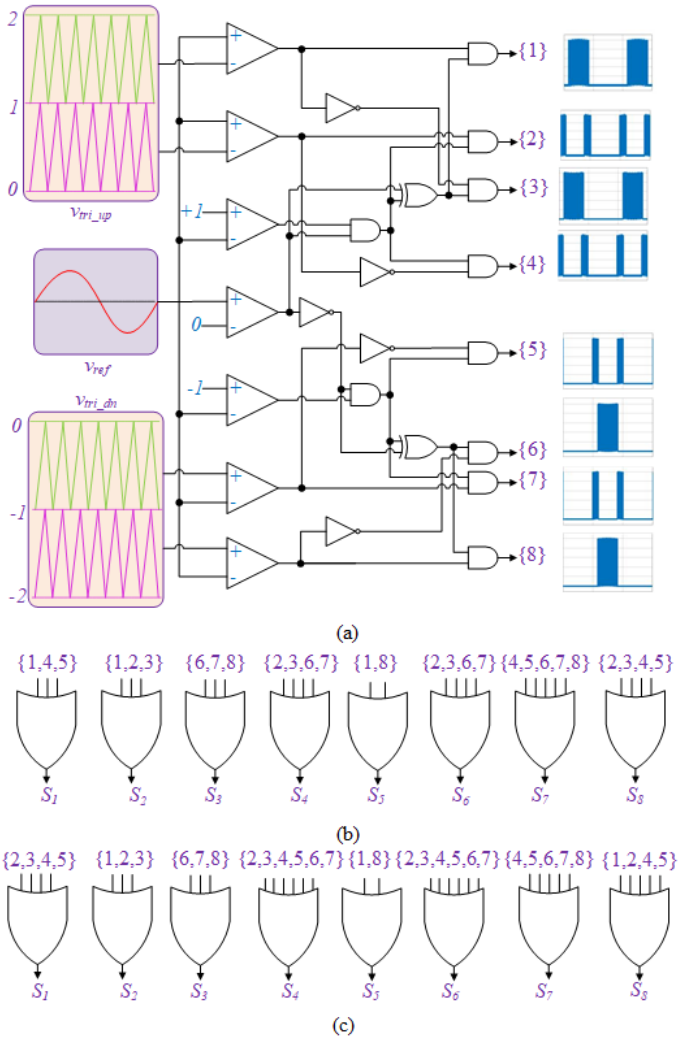


Fig. 5.4. Sinusoidal pulse width modulator implementation for proposed topology: (a) logical operation, (a) switching signal generation for buck mode, and (c) switching signal generation for boost mode.

5.4. Thermal Analysis and Loss Calculation

The simulated average power loss distribution and the operating junction temperature (T_j) of the individual switching elements are presented in Fig. 5.5. A constant ambient temperature of 40°C is assumed and the uniform temperature distribution across the heat sink is shown for buck and boost mode of the proposed topology.

It is expected that switches (S_1 and S_8) in the capacitor-charging path have a higher loss (conduction) and hence relatively higher temperature ($\Delta Tj \approx 7$°C) than the other switches. Fig. 5.6 (a) shows similar findings and the loss distribution across the switching components.

Finally, the total conduction losses, switching losses, flying capacitor losses (FC_{Loss}), and filter losses (F_{Loss}) are shown in Fig. 5.6 (b) for both modes respectively.

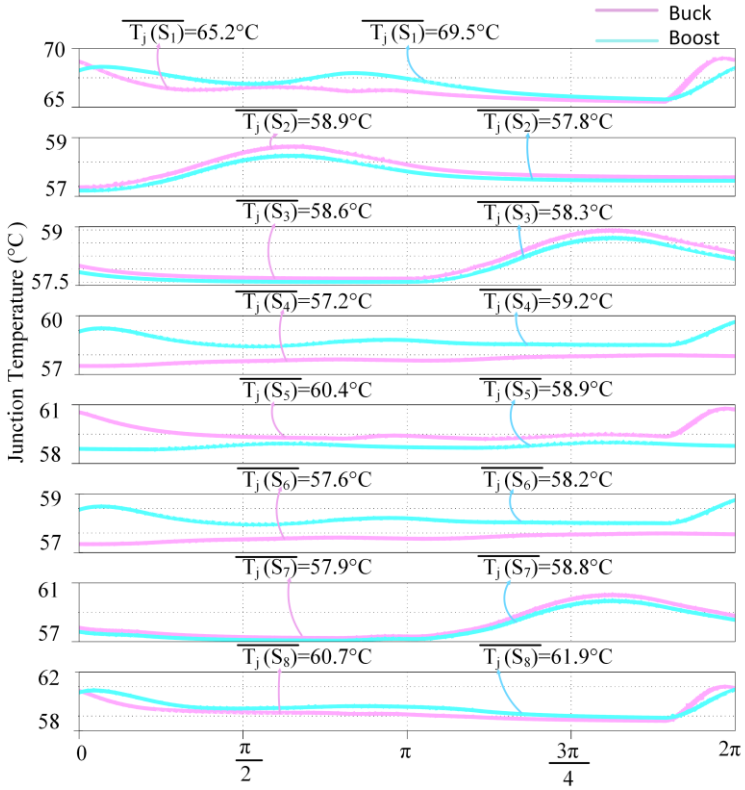
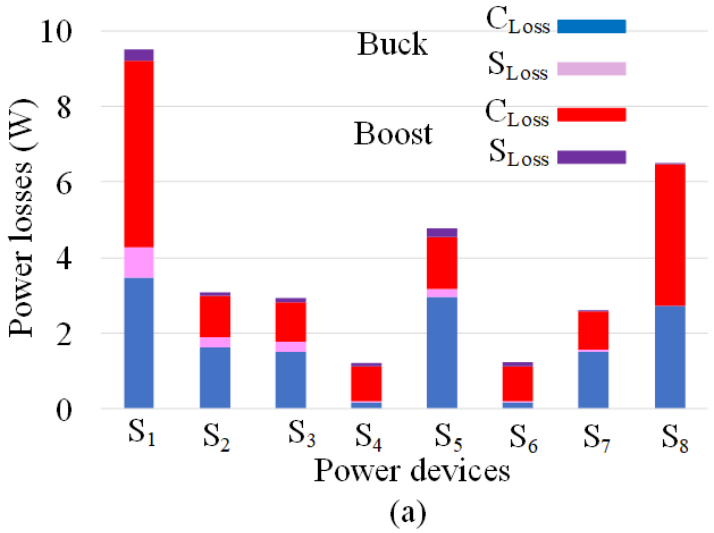
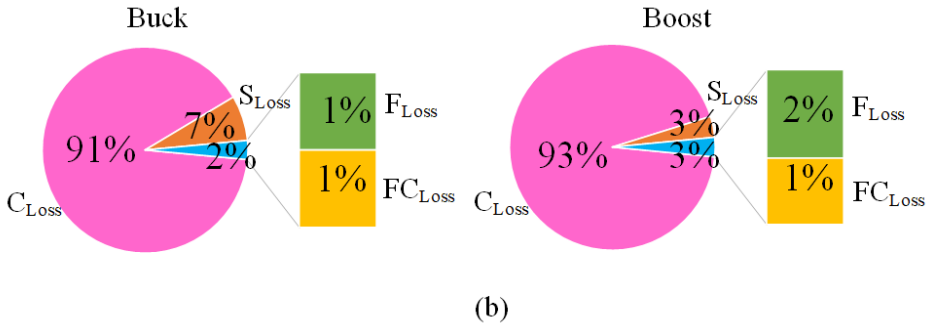


Fig. 5.5. Steady-state operating junction temperature of the semiconductor devices in both modes for one fundamental period.





(b)

Note: C_{Loss}=Conduction losses, S_{Loss}=Switching losses, F_{Loss}=Filter losses, and FC_{Loss}=Flying apacitor losses.

Fig. 5.6. Loss analysis of the proposed topology: (a) switching and conduction losses, and (b) total loss distribution in full load condition.

5.5. Design Parameter and Guidelines

A component selection guideline is helpful to estimate and select the parameters for the practical design. First of all, the voltage and current rating of the active switches and diodes must be selected just above the safety margin. Even though the input DC-link capacitor helps to maintain a constant voltage at the DC-link, there are some small spikes in practice across the semiconductor devices. As a result, the voltage and current rating of the selected semiconductor devices are 650 V and 50 A accordingly.

To select the components of the proposed inverter, a few more things need to be calculated such as DC-link capacitor (C_{in}), flying-capacitors (C_1 and C_2) and the output filter (L_f and C_f).

The DC-link capacitors C_{in} can be calculated by (71) where the input power is greater than the output power by ΔP, α_{max} is the maximum hold-on cycle number ($\alpha_{max} > 1$), t_c is the per cycle time period, and ΔV_{dC} is the permissible voltage ripple across the supply voltage of the system. The voltage ripple across the supply voltage can be selected between 5%− 10% of the rated input voltage. As a result, the selected capacitor value should be greater than 400 μF, which satisfies all working modes.

$$C_{in} \geq \frac{2 \times t_c \times \Delta P \times (\alpha_{max} - 1)}{\Delta V_{dC}{}^2} \tag{71}$$

The flying capacitors (C_1 and C_2) of the proposed topology can be calculated using (72) through the capacitor discharging time (t_{dis}) the average output current (i_{acavg}) and the voltage ripple requirements of the capacitor (Δv_{C1}).

$$C_1 = C_2 \geq \frac{i_{acavg} \times t_{dis}}{\Delta v_{C1}} \tag{72}$$

An LC filter was selected for this design. The required filter inductor depends on the output current ripple (Δi_{acmax}) which is recommended to choose a value between 5-10 % of the rated output current (i_{ac}). Moreover, the filter inductor value depends on the modulation type, and switching conditions. For the system, the switching frequency (f_{sw}) is selected at 20 kHz, and the maximum output current is 5 A for 1 kVA rated output power. As a result, the filter inductor can be calculated by (73) which is less than 0.6 mH.

$$L_f \geq \frac{0.03 \times \sqrt{2} \times v_{ac}}{f_{sw} \times \Delta i_{acmax}} \tag{73}$$

Following this, the filter capacitor (C_f) can be calculated by (74) where the cut-off frequency (f_c) is set to be 10% of f_{sw} and the calculated value is approximately 5 µF.

$$C_f \geq \frac{1}{4 \times \pi^2 \times {f_c}^2 \times L_f} \tag{74}$$

5.6. Comparison with Conventional Topologies

This section systematically compares the proposed dual-mode topology with conventional five-level transformerless inverter topologies. It presents a detailed comparison list (see Table 5.2) of the proposed topology with selected five-level transformerless inverter topologies considering the required number of active and passive components to design the inverter, number of required DC sources, output filter type and its value, common ground-type, reactive power capabilities, total harmonic distortion (THD), cost, boosting ability and efficiency. It can be seen that the proposed topology is operated in both modes with common grounded-type configuration. The THD is comparatively low for the proposed topology (2.1% for boost mode and 2.4% for buck mode). The prototype cost and size depends on the number of components used in the system design. A careful analysis and comparison of the cost of

the mentioned topologies and the proposed topology reveals that the cost and size of the proposed topology are reasonably lower than [146]-[158]. Moreover, the peak efficiency of the proposed topology is 99.01% at 122 VA in boost and 98.96% at 130 VA in buck mode. Table 5.3 presents a comparative summary of the proposed 5L-inverter with the conventional 5L-inverter topologies in terms of voltage stress across the major components and the number of required high-frequency switches. For the proposed topology, the voltage stress of five switches (S_1-S_3, S_7 and S_8) is equal to the required input voltage, and the voltage stress of the other three switches ($S_4 - S_6$) is half of the required input voltage when the proposed topology is operated in buck mode. On the other hand, five switches (S_1-S_3, S_7, and S_8) experience voltage stress which is twice the input voltage and other three switches (S_4-S_6) experience voltage stress equal to the input voltage in boost mode. In boost mode of the proposed topology, all switches experience f_{sw} over a half power cycle. On the other hand, in buck mode, five switches experience f_{sw} over a half power cycle, while other three switches experience f_{sw} in a full power cycle. Furthermore, the voltage stress on the switch is either the same as or less than the conventional topologies.

5.7. Results and Discussion

5.7.1. Components Selection for Simulation and Experiment of Proposed Topology III

The performance of the proposed topology is first simulated by MATLAB-Simulink using the PLECS toolbox and then verified experimentally with a 1000 VA laboratory prototype. In order to precisely verify the performance of the proposed inverter and to have fare comparison, same parameters have been used for both the simulation and experiment that are listed in Table 5.4.

Table 5.4. Parameters and components for simulation and experimental purposes

Parameter/Description	*Value*
Rated power, P_o	1 kVA
Input voltage, V_{dc}	200-400 V
Output voltage, v_{ac}	~230 V (RMS)
Output current, i_{ac}	~4.73 A (RMS)
Modulation index, M	0.82
Switching frequency, f_{SW}	20 kHz
Line frequency (f_L)	50 Hz
Registive load (R)	~52 Ω
LC filter	0.542 µH, 4 µF
Flying capacitors (C_1 & C_2)	1.64 mF Elect.
Power switches	IPP60R125P6
Controller	TMS320F28335

5.7.2. Hardware Setup

A proof-of-concept 1 kVA hardware prototype as shown in Fig. 5.7 was build and tested with the parameters and component values listed in Table 5.4. Experimental results of the proposed topology in buck mode conditions are shown in Figs. 5.8-5.11. Figs 5.12-5.15 demonstrate the behavior of the inverter in boost mode. It can be seen that the inverter is capable of generating a 5-level output voltage with a clean sinusoidal voltage and current after the filter in both modes.

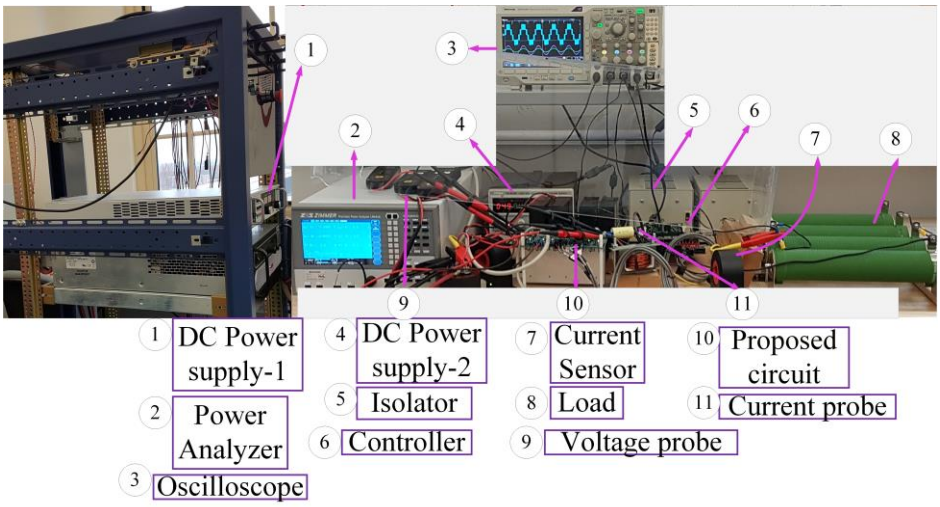


Fig. 5.7. Test bench of the experimental setup.

5.7.3. Experimental Results

Voltage stress on the switches are shown in Fig. 5.8 for buck and Fig. 5.12 for boost

mode of the proposed topology. The maximum voltage stress on the switches is 400 V for $S_1 - S_3, S_7$ and S_8 , and 200 V for the other switches ($S_4 - S_6$). Fig. 5.9 shows the waveform of the input voltage when the inverter is run in buck mode. The inverter clearly has five levels in the output voltage with a clean sinusoidal output voltage and current after the filter. The RMS value of the output voltage and current is 230 V and 4.73 A. The inverter produces good output quality voltage and current waveforms without high distortion (THD < 2.4%). As shown in Fig. 5.10, the load is changed from R = 50 Ω to 75 Ω (see Fig. 5.10 (a)), and from R = 75 Ω to 50 Ω (see Fig. 5.10 (b)).

This result shows that the proposed structure can function in various dynamic conditions and keep the inverter output voltage to five levels. Additionally, the output voltage and current show a clear sinusoidal waveform. Fig. 5.11 and Fig. 5.15 show the waveform of the voltage across the capacitors in buck and boost mode where it is shown that both capacitors are kept constant for both modes. The required input voltage is 400 V and 200 V for the buck mode operation and boost mode respectively to obtain 230 V AC output voltage. The measured voltage across the DC-link capacitors is shown in Ch1 and Ch2 of the measured waveforms. The measured peak-to-peak voltage ripple of the capacitor is 4 V (4 V/196 V = 2%) and they are self-balanced due to the series/parallel operation of the capacitors.

Table 5.2. Comparative summary of the proposed topology with conventional five-level transformer-less inverter topologies

Topologies	**No. of semiconductor devices**		**No. of passive components**		**DC sources**	V_{PN}	**Output filter type**			**CGT**	**RPC**	**THD (%)**	**Cost / size***	**Boosting**	η_{peak}
	S	**D**	**L**	**C**			L_{f1} **(mH)**	L_{f2} **(mH)**	C_f **(µF)**						
5L-CHB [147]	8	0	0	0	2	$\frac{1}{2}V_{dc}$	N/A	N/A	N/A	no	N/A	3	++	no	N/A
5L-T-type [148]	8	0	0	2	1	$\frac{1}{2}V_{dc}$	0.18	N/A	10	no	N/A	N/A	+++ +	no	98.7% @ 5 kVA
5L-FC [149]	8	0	0	3	1	V_{dc}	N/A	N/A	N/A	no	N/A	<5.3	+++ +	no	N/A
5L-NPC [150]	8	4	0	2	1	$\frac{1}{2}V_{dc}$	3	N/A	N/A	no	N/A	N/A	+++ +	no	N/A
5L-ANPC [151]	12	0	0	3	1	$\frac{1}{2}V_{dc}$	N/A	N/A	N/A	no	N/A	N/A	+++ +	no	N/A
5L-S-ANPC [152]	7	2	0	3	1	V_{dc}	1.6	N/A	N/A	no	yes	1.6	+++	no	N/A
5L-B-ANPC [126]	6	0	0	3	1	$2V_{dc}$	0.4	N/A	2.2	no	N/A	N/A	++	yes	99% @ 1 kVA

MMC [153]	8	8	2	0	1	V_{dc}	4.6	4.6	N/A	no	N/A	N/A	+++ +	no	N/A
5L-SS-DBFBI[153]	6	4	0	2	1	V_{dc}	2	2	0.47	no	N/A	<5	+++ +	no	99.2% @ 1 kVA
5L-SD-DBFBI[154]	6	6	0	2	1	V_{dc}	2	2	0.47	no	N/A	<5	+++ +	no	98.7% @ 1 kVA
[155]	8	1	0	2	1	V_{dc}	8	8	0	no	N/A	<5	+++	no	96.8% @ 0.5 kVA
[156]	12	2	0	2	1	$\frac{1}{2}V_{dc}$	N/A	N/A	N/A	no	N/A	N/A	+++ +	no	N/A
[49]	6	0	0	2	1	V_{dc}	8	N/A	N/A	yes	yes	<5	+++	no	N/A
[157]	6	2	0	3	1	$2V_{dc}$	3	N/A	N/A	yes	yes	2.2	++	yes	98.1 % @ 0.5 kVA
[158]	6	1	0	2	1	V_{dc}	2	N/A	N/A	yes	yes	3.5	++	no	98.55% @ 1.2 kVA
[159]	6	3	1	2	1	V_{dc}	1	N/A	3	no	N/A	4.8	+++	yes	N/A
[160]	8	2	0	1	1	V_{dc}	N/A	N/A	N/A	no	N/A	N/A	+++	no	N/A
[161]	6	2	0	2	1	V_{dc}	3.18	N/A	N/A	no	N/A	2.48	+++	no	N/A
Proposed (buck)	9	0	0	2	1	V_{dc}	0.542	N/A	4	yes	yes	2.4	+++	no	98.6 % 1 kVA
Proposed (boost)	9	0	0	2	1	$2V_{dc}$	0.542	N/A	4	yes	yes	2.1	+++	yes	98.5 % 1 kVA

*More "+" represents the higher cost/size: "+" ≡ low, "++" ≡ medium, "+++" ≡ high, and "++++" ≡ extremely high.In the above table, "S" represents switch, "D" represents diode, "C" represents capacitor, "L" represents inductor, "V_{dc}" input voltage, "V_{PN}" DC-link voltage, "η_{peak}" represents peak efficiency, "f_S" switching frequency, "CGT" common ground type, "RPC" reactive power capability, "φ_{pf}" reported power factor, "THD" reported total harmonic distortion, "NR" not recommended, "N/A" not available.

Table 5.3. Voltage stress comparison of selected topologies

Topologies	**Voltage stress on switches and number of required high-frequency switches**		**Voltage stress on diodes and number of required high-frequency diodes**		**Voltage stress on capacitors**
	Voltage stress	**Number of required high-frequency switches (switching frequency - f_{SW})**	**Voltage stress**	**Number of required high-frequency diodes (switching frequency - f_{SW})**	
[157]	V_{S1}=V_{dc}, V_{S2}=V_{dc}, V_{S3}=V_{dc}, V_{S4}=$2V_{dc}$, V_{S5}=$3V_{dc}$, V_{S6}=$2V_{dc}$	5 (f_{SW} for half line cycle) 1 (f_{SW} for full line cycle)	V_{D1}=V_{dc}, V_{D2}=$2V_{dc}$	1 (f_{SW} for half line cycle) 1 (f_{SW} for full line cycle)	V_{C1}=V_{dc}, V_{C2}= $2V_{dc}$
[152]	V_{S1}=$\frac{3}{4}V_{dc}$, V_{S2}=$\frac{1}{4}V_{dc}$, V_{S3}=$\frac{1}{4}V_{dc}$, V_{S4}=$\frac{3}{4}V_{dc}$, V_{S5}=$\frac{1}{2}V_{dc}$, V_{S6}=$\frac{1}{2}V_{dc}$, V_{S7}=$\frac{1}{4}V_{dc}$	2 (f_{SW} for half line cycle) 3 (f_{SW} for full line cycle) 2 (f_{Line})	V_{D1}=$\frac{1}{4}V_{dc}$, V_{D2}=$\frac{1}{4}V_{dc}$	2 (f_{SW} for full line cycle)	V_{C1}=$\frac{1}{2}V_{dc}$, V_{C2}= $\frac{1}{2}V_{dc}$, V_{C1}=$\frac{1}{4}V_{dc}$

[126]	$V_{S1}=\frac{1}{2}V_{dc}$, $V_{S2}=\frac{1}{2}V_{dc}$, $V_{S3}=\pm\frac{1}{4}V_{dc}$, $V_{S4}=\frac{1}{2}V_{dc}$, $V_{S5}=\frac{1}{2}V_{dc}$, $V_{S6}=\pm\frac{1}{4}V_{dc}$	2 (f_{SW} for half line cycle) 2 (f_{SW} for full line cycle) 2 (f_{Line})	N/A	N/A	$V_{C1}=\frac{1}{2}V_{dc}$, $V_{C2}=\frac{1}{2}V_{dc}$, $V_{C3}=\frac{1}{4}V_{dc}$
[155]	$V_{S1}=V_{dc}$, $V_{S2}=V_{dc}$, $V_{S3}=V_{dc}$,$V_{S4}=V_{dc}$, $V_{S5}=\frac{1}{2}V_{dc}$, $V_{S6}=\frac{1}{2}V_{dc}$, $V_{S7}=\frac{1}{2}V_{dc}$, $V_{S8}=\frac{1}{2}V_{dc}$	6 (f_{SW} for half line cycle) 2 (f_{SW} for full line cycle)	$V_D=\frac{1}{2}V_{dc}$	1 (f_{SW} for half line cycle)	$V_{C1}=\frac{1}{2}V_{dc}$, $V_{C2}=\frac{1}{2}V_{dc}$
5L-SS-DBFBI [154]	$V_{S1}==\frac{1}{2}V_{dc}$, $V_{S2}==\frac{1}{2}V_{dc}$, $V_{S3}=\frac{1}{2}V_{dc}$, $V_{S4}=\frac{1}{2}V_{dc}$, $V_{S5}=V_{dc}$, $V_{S6}=V_{dc}$	6 (f_{SW} for half line cycle)	$V_{D1}=V_{dc}$,$V_{D2}=V_{dc}$, $V_{D1}=\frac{1}{2}V_{dc}$,$V_{D2}=\frac{1}{2}V_{dc}$	4 (f_{SW} for full line cycle)	$V_{C1}=\frac{1}{2}V_{dc}$, $V_{C2}=\frac{1}{2}V_{dc}$
5L-SD-DBFBI [154]	$V_{S1}=V_{dc}$, $V_{S2}=V_{dc}$, $V_{S3}=\frac{1}{2}V_{dc}$, $V_{S4}=\frac{1}{2}V_{dc}$, $V_{S5}=V_{dc}$, $V_{S6}=V_{dc}$	6 (f_{SW} for half line cycle)	$V_{D1}=\frac{1}{2}V_{dc}$, $V_{D2}=\frac{1}{2}V_{dc}$, $V_{D1}=V_{dc}$, $V_{D2}=V_{dc}$,	4 (f_{SW} for full line cycle)	$V_{C1}=\frac{1}{2}V_{dc}$, $V_{C2}=\frac{1}{2}V_{dc}$
Proposed (buck)	$V_{S1}=V_{dc}$,$V_{S2}=V_{dc}$,$V_{S3}=V_{dc}$, $V_{S4}=\frac{1}{2}V_{dc}$, $V_{S5}=\frac{1}{2}V_{dc}$, $V_{S6}=\frac{1}{2}V_{dc}$, $V_{S7}=V_{dc}$, $V_{S8}=V_{dc}$	5 (f_{SW} for half line cycle) 3 (f_{SW} for full line cycle)	N/A	N/A	$V_{C1}=\frac{1}{2}V_{dc}$, $V_{C2}=\frac{1}{2}V_{dc}$
Proposed (boost)	$V_{S1}=\pm V_{dc}$, $V_{S2}=2V_{dc}$, $V_{S3}=2V_{dc}$, $V_{S4}=V_{dc}$, $V_{S5}=V_{dc}$, $V_{S6}=V_{dc}$, $V_{S7}=2V_{dc}$, $V_{S8}=2V_{dc}$	8 (f_{SW} for half line cycle)	N/A	N/A	$V_{C1}=V_{dc}$,$V_{C2}=V_{dc}$

This result shows that the proposed structure can function in various dynamic conditions and keep the inverter output voltage to five levels. Additionally, the output voltage and current show a clear sinusoidal waveform. Fig. 5.11 and Fig. 5.15 show the waveform of the voltage across the capacitors in buck and boost mode where it is shown that both capacitors are kept constant for both modes. The required input voltage is 400 V and 200 V for the buck mode operation and boost mode respectively to obtain 230 V AC output voltage. The measured voltage across the DC-link capacitors is shown in Ch1 and Ch2 of the measured waveforms. The measured peak-to-peak voltage ripple of the capacitor is 4 V (4 V/196 V = 2%) and they are self-balanced due to the series/parallel operation of the capacitors. Using this charging/ discharging of the capacitor, the topology can generate five-level inverter voltage.

Fig. 5.13 shows the waveform of the input voltage when the inverter operates in boost mode. In this scenario, the required input voltage is 200 V to obtain 230 V AC output voltage

and 4.65 A output current. The inverter output voltage and current waveforms with clear five levels in the output voltage have a clear sinusoidal output voltage and current after the filter.

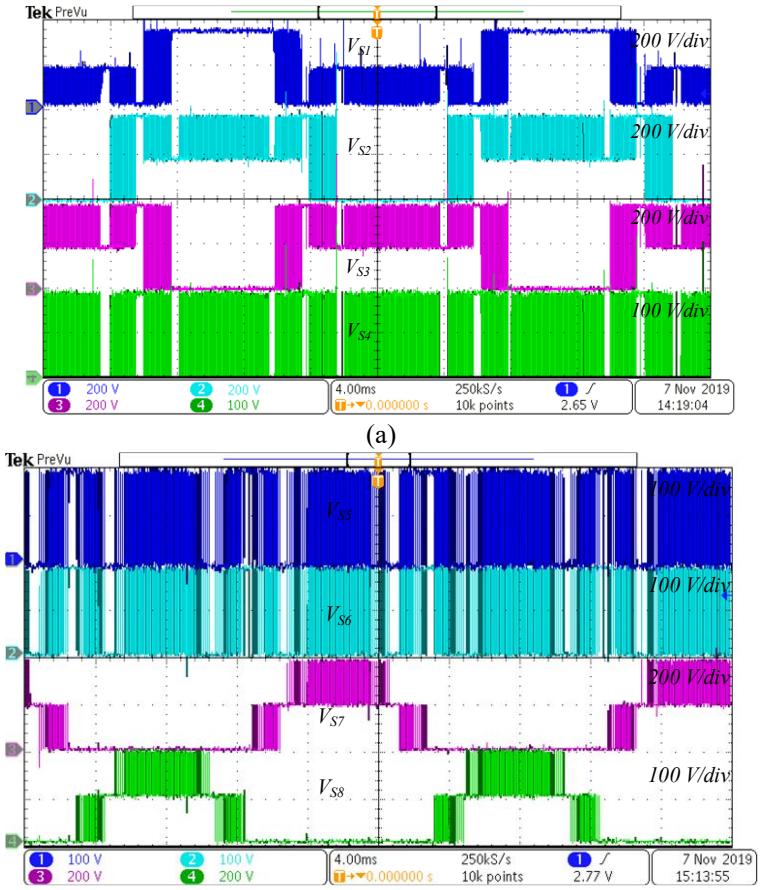
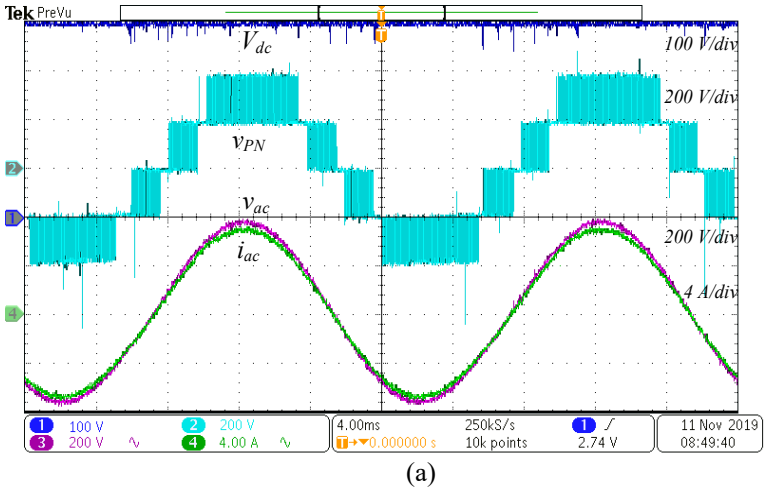
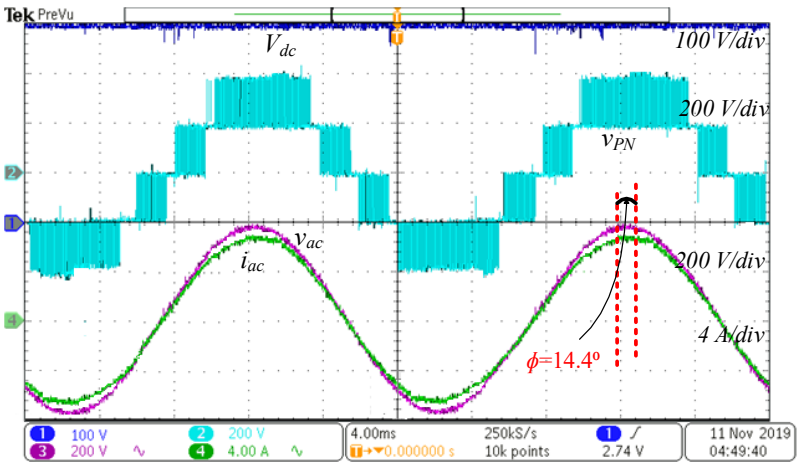


Fig. 5.8. Voltage stress of the switches in buck mode: (a) switch $S_1 - S_4$, and (b) switch $S_5 - S_6$.

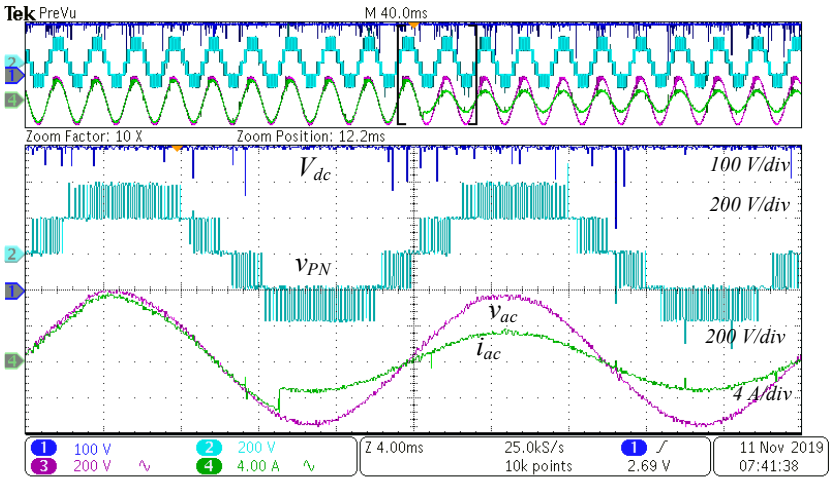




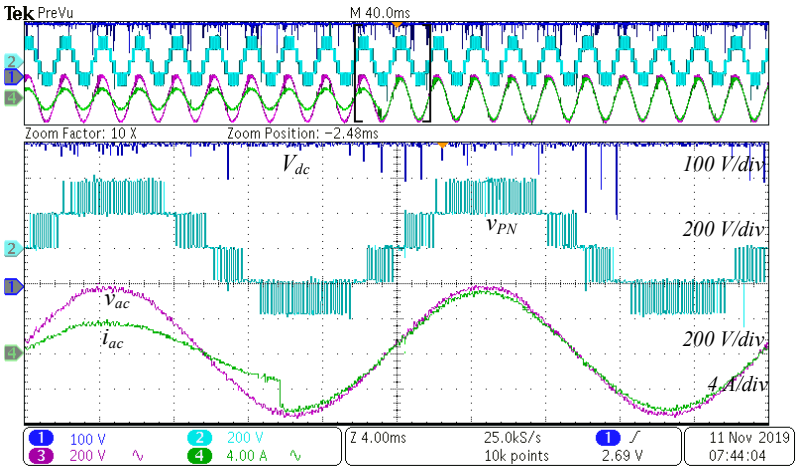
(b)

Fig. 5.9. Input voltage, inverter voltage without filter, output voltage and current after the LC filter in the buck mode (a) resistive load (R) and (b) reactive power condition (cos φ = 0.967).

The RMS value of the output voltage and current is 230 V and 4.65 A respectively. The inverter produces good-quality voltage and current waveforms without high distortion (THD < 2.1 %). As shown in Fig. 5.15, the load changes between from R = 50 Ω to 75 Ω (see Fig. 5.14 (a)), and from R = 75 Ω to 50 Ω (see Fig. 5.14 (b)).



(a)



(b)

Fig. 5.10. Dynamic performance in buck mode under sudden load change: (a) 50 Ω to 75 Ω, and (b) 75 Ω to 50 Ω.

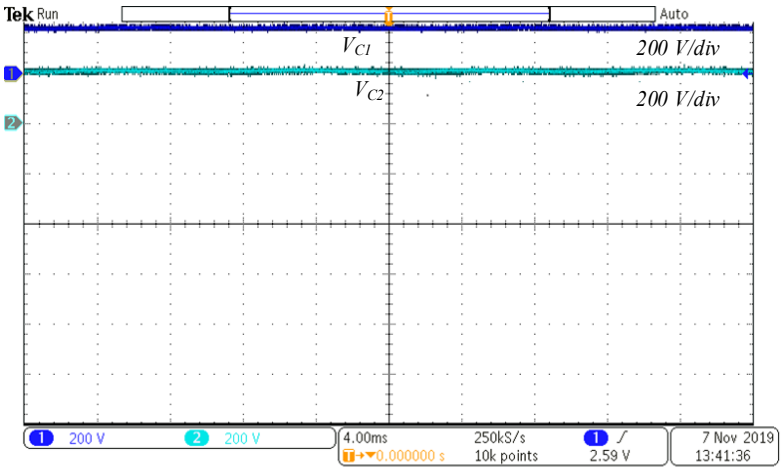
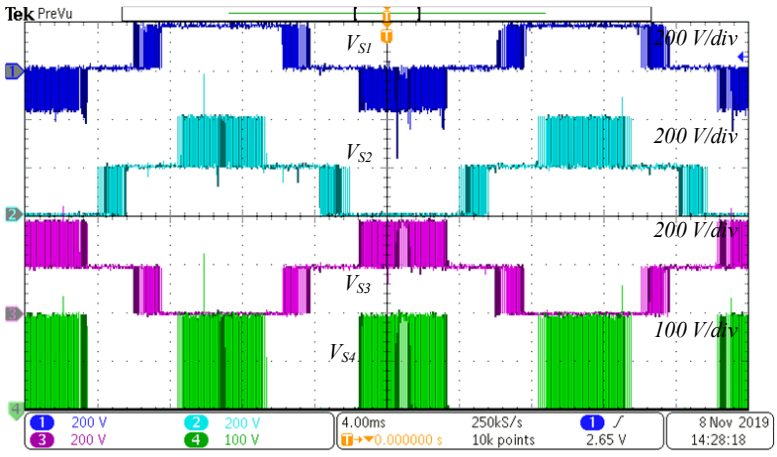
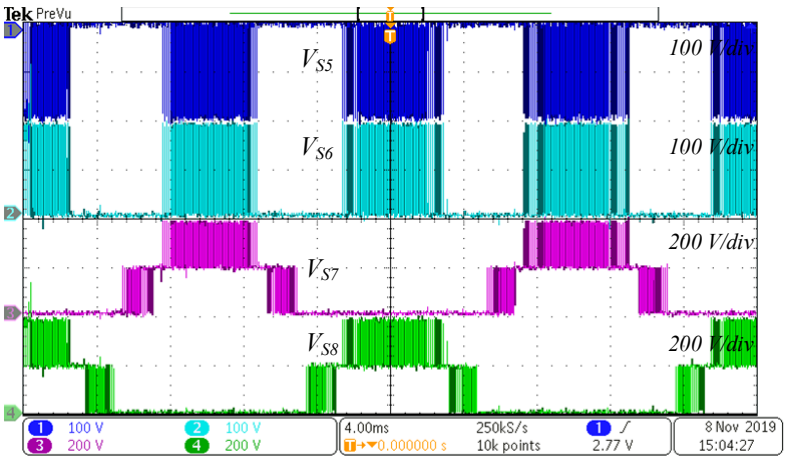


Fig. 5.11. Voltage across the capacitors (C_1, and C_2) in buck mode.

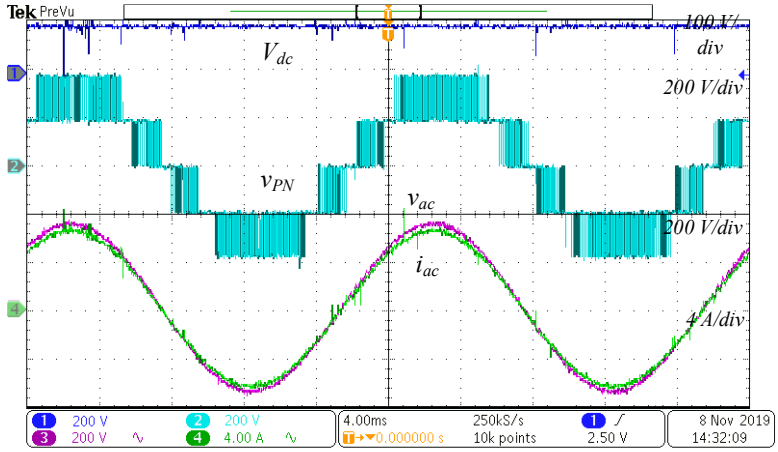


(a)

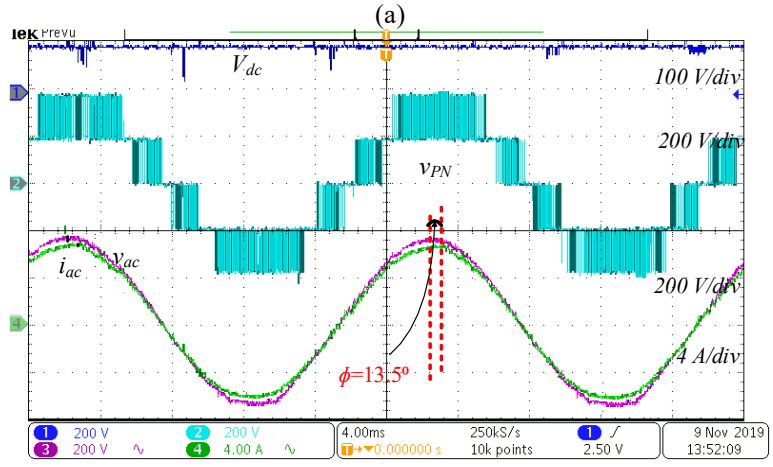


(b)

Fig. 5.12. Voltage stress of the switches in boost mode: (a) switch $S_1 - S_4$, and (b) switch $S_5 - S_6$.

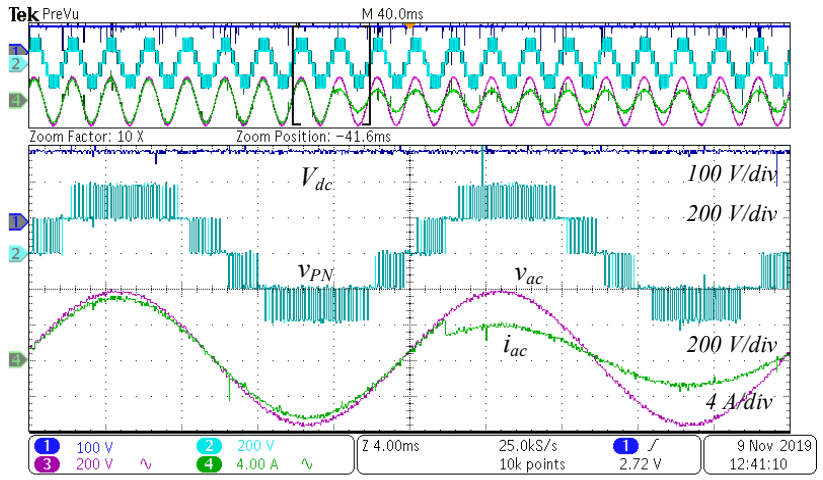


(a)

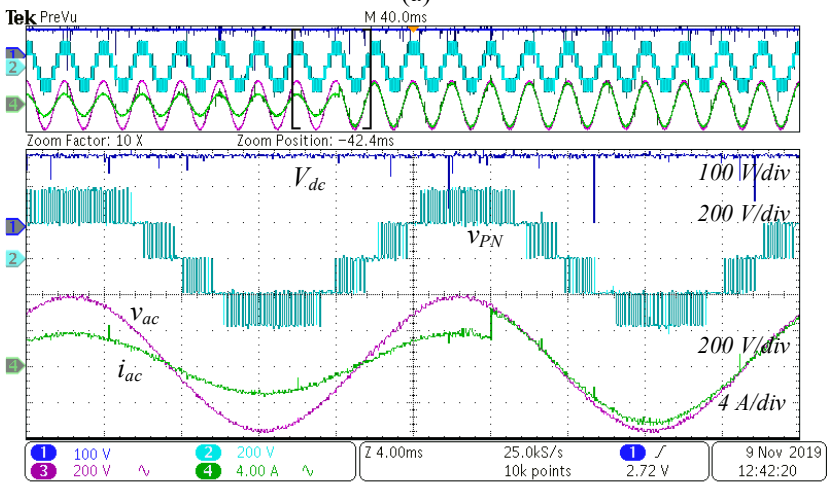


(b)

Fig. 5.13. Input voltage, inverter voltage without filter, output voltage and current after the LC filter in boost mode (a) resistive load (R) and (b) reactive power condition (cos φ = 0.97).



(a)



(b)

Fig. 5.14. Dynamic performance in boost mode under sudden load change: (a) 50 Ω to 75 Ω, and (b) 75 Ω to 50 Ω.

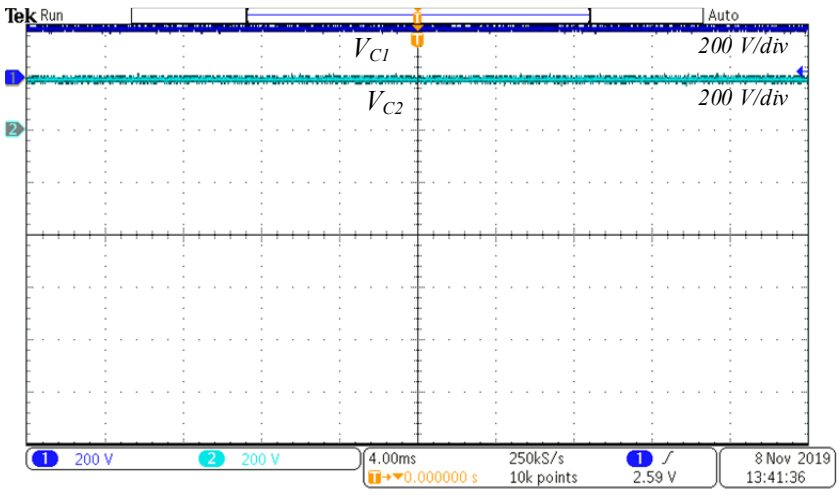


Fig. 5. 15. Voltage across the capacitors (C_1, and C_2).

This result shows that the proposed structure in boost mode can function under various dynamic conditions while maintaining five levels at the inverter's output. Additionally, the output voltage and current are a clean sinusoidal waveform. The curves for the overall efficiency of the proposed converter are shown in Fig. 5.16. Both modes of operation were evaluated using resistive loads. The efficiency was measured using a LMG640 power analyzer. The inverter has an efficiency of 97±1% over a wide operating range. The peak efficiency was 98.96% at 130 VA in buck mode and 99 % at 122 VA in boost mode.

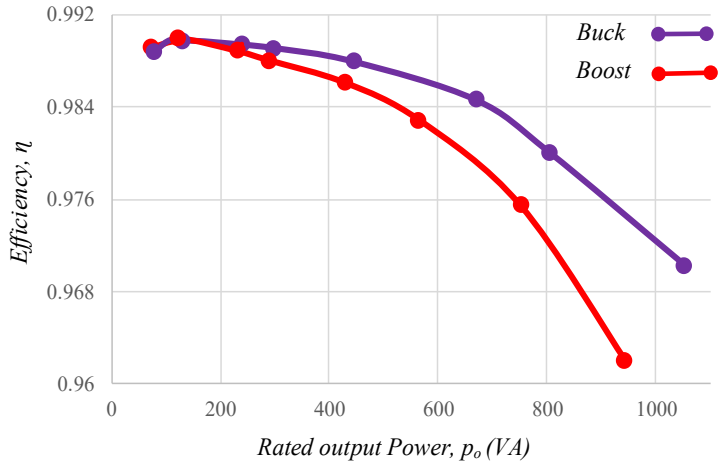


Fig. 5.16. Measured efficiency curve of the proposed inverter in both modes.

5.8. Summary

A new dual mode common ground-type five-level inverter has been presented in this chapter. The theoretical analysis of the proposed topology is derived and presented in detail. The proposed topology features many advantages when compared with various suggested single-phase five-level inverter topologies, namely scalability, utilization of a low number of semiconductors, low voltage stress, high efficiency and power density, low cost and size, and simple modulation control. Furthermore, the experimental waveforms of a 1 kVA prototype are presented to show the validity of the proposed inverter in both buck and boost modes. The measurement results show that the proposed inverter has the 97±1% efficiency over a wide range of loads with a peak efficiency of 98.96% at 130 VA in buck mode and 99% at 122 VA in boost mode.

Chapter 6

Soft Start and Quasi Resonant Charging (QSC) Capability Based 5-Level Inverter (Proposed Topology IV)

6.1. Circuit Structure

The circuit configuration of the proposed 5L SC-based inverter is illustrated in Fig. 6.1. It needs a single dc source, an SC network, and a front-end FB cell to make five-distinctive output voltage levels. Since the grid-connected application is of the target, the proposed 5L-SC-based inverter is connected to the grid via a small LC filter.

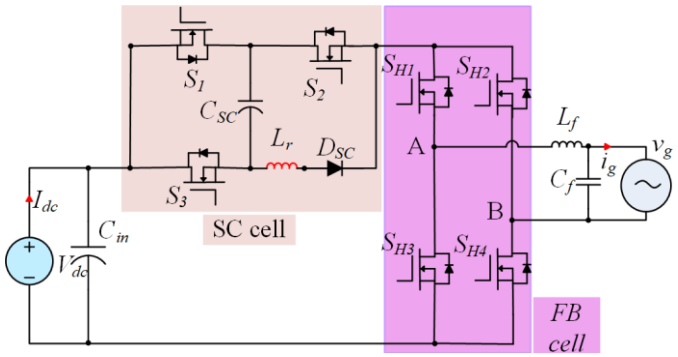


Fig. 6.1. Circuit structure of the proposed single-phase 5L inverter topology.

Herein, unlike the conventional series-parallel SC network, three unidirectional power switches (S_1, S_2, and S_3), a single capacitor (C_{SC}), an additional quasi-resonant inductor (L_r)

series with a single power diode (D_{SC}) are employed. As earlier mentioned, the proposed 5L-SC based topology rather than its double voltage boosting ability, offers two major added benefits corresponding to the start-up moment and QSC operation of the involved capacitor. In the following subsections, the steady-state switching performance of the proposed topology, its soft-start switching states, and its QSC operation capability are discussed. Meanwhile a short description of the generalization to cope up with generating higher number of inverter output voltage levels is also presented.

Some of the prominent features of the proposed topology structure include:

1. Has the capability to boost the voltage, and thus, it requires reduced dc-link supply compared to existing topologies.
2. It requires a minimum number of components compared to the conventional topologies. This topology requires only seven active switches, a diode, a capacitor and an inductor to generate 5L voltage output.
3. It has soft-start and quasi resonant charging capability. Thus, it reduces the charging current through the capacitor and input inrush current.
4. The voltages stress on the switched-capacitor do not exceed the input dc voltage. As a result, it reduces the size of the capacitors.
5. The circuit does not require any additional sensor or control strategy to balance the capacitor voltages.
6. It can operate with both leading and lagging power factors. Thus, it can provide reactive power support to the grid when necessary.

6.2. Steady-State Switching States

In order to generate all the 5L output voltage waveform of the proposed inverter, six different switching modes are available as shown in Fig. 6.2 (a)-(f). Here, C_{SC} can only be charged to the input voltage (V_{dc}) during the freewheeling period (zero states in both half cycle) as it can be realized in Fig. 6.2 (a), and (d). Both switches of a single leg from the FB cell must be turned ON, while the charging loop of C_{SC} is made through the ON state contribution of S_1 from the SC network with the forward bias condition of D_{SC}. Regarding the

incorporated L_r of the capacitive charging loop, a QSC path is provided, which can limit the current stress profile of the involved semiconductors.

Table 6.1. Switching states of the proposed converter

Mode	Switches							Output voltage level	Inverter output voltage (v_{AB})	Capacitor state
	S_1	S_2	S_3	S_{H1}	S_{H2}	S_{H3}	S_{H4}			
A	1	0	0	1	0	1	0	+0	$+0$	C
B	1	1	0	1	0	0	1	+1	$+V_{dc}$	NC
C	0	1	1	1	0	0	1	+2	$+2V_{dc}$	D
D	1	0	0	1	0	1	0	-0	-0	C
E	1	1	0	0	1	1	0	-1	$-V_{dc}$	NC
F	0	1	1	0	1	1	0	-2	$-2V_{dc}$	D

Note: "1" ON, "0" OFF, "C" charging, "NC" non-connecting, and "D" discharging.

Contemporarily, C_{SC} is disconnected from the input dc source and the grid during the generation of middle output voltage levels ($\pm V_{\mathrm{dc}}$), as it can be seen in Fig. 6.2 (b) and (e). Here, S_1 and $\mathrm{S}_2$from the SC network must be ON in both half cycles of the middle output voltage level generations, while the polarity of the output voltage can be turned through the FB cell switches. Also, considering the active power support mode, C_{SC} is discharged during both the top positive ($+2V_{\mathrm{dc}}$) and top negative ($-2V_{\mathrm{dc}}$) output voltage levels generation as realized by Fig. 6.2 (c) and (f). So, in both these cases, $\mathrm{S}_2$and S_3 must be turned ON, whereas the FB cell switches act as the polarity generator unit of the inverter output voltage. The instant C_{sc} condition with the ON switching states of the switches per each output voltage level is summarized in Table 6.1.

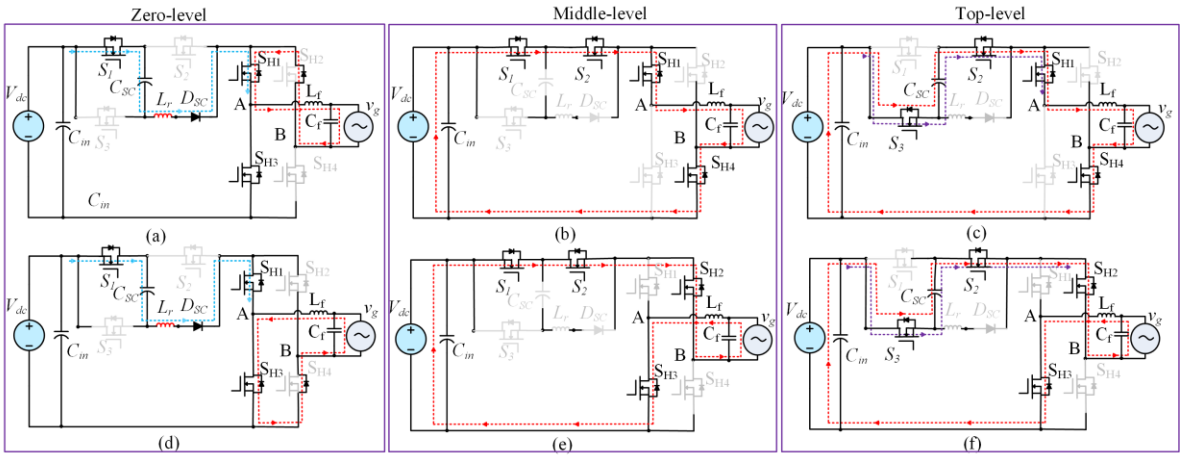


Fig. 6.2. Operating modes of the proposed topology: (a) Mode A [+0] to create $v_{AB} = +0$, (b) Mode B [+1] to create $v_{AB} = +V_{dc}$ (c) Mode C [+2] to create $v_{AB} = 2V_{dc}$ (d) Mode D [-0] to create $v_{AB} = -0$ (e) Mode E [-1] to create $v_{AB} = -V_{dc}$ (f) Mode F [-2] to create $v_{AB} = -2V_{dc}$.

6.3. Soft-Start Operation

Conventional SCMLIs suffer from large input inrush current at the beginning of the operation and whenever the involved capacitors are switched in parallel to the input dc source. Using an additional relay with a damping resistor associated with a voltage sensor to track the pre-charging operation of the involved capacitors has been recommended in [162], and [163] as the pre-charged process. So, this procedure may increase the overall cost per power density, while the ON/OFF switching conversion of the incorporated relay with a huge current stress can also impose additional power losses. The proposed 5L-SC based inverter has an inherent soft-start capability by changing the pre-charge modulation process**.** Fig. 6.3 (a)-(b) shows the start-up modulation of the proposed inverter during the generation of output voltage levels in the zero and middle states of the positive half cycle. Herein, unlike the steady-state condition, C_{SC} is not charged to V_{dc} during the zero state as realized by Fig. 6.3(a). So none of the SC network switches are ON at this stage and C_{sc} is disconnected from the input and the grid.

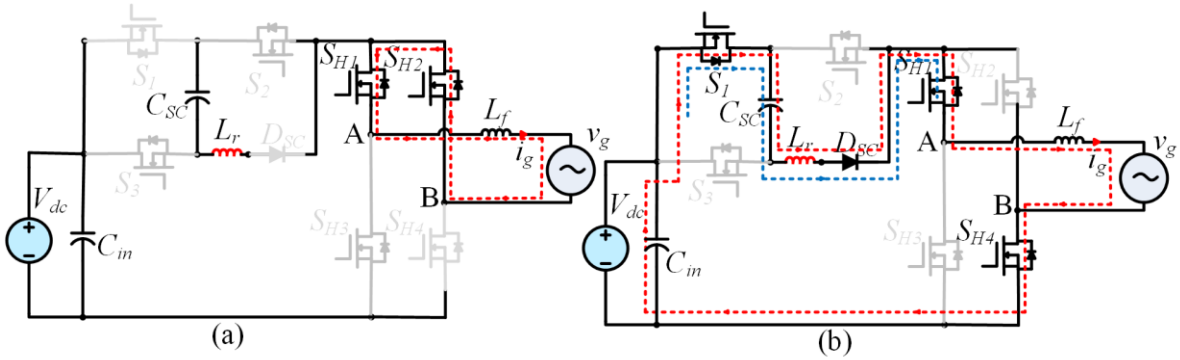


Fig. 6.3. Current flowing path during the soft start mode: (a) Mode G: +0-level, and (b) Mode H: +1-level.

In contrast, considering $V_{C,SC}(0) = 0$ as the initial condition of $v_{C,SC}$, C_{sc} can be charged to V_{dc} once the middle positive output voltage is generated through S_1, and the FB cell switches. Here, apart from the grid voltage ($v_g(t) = V_m sin(\omega t)$), both the resonant and filter inductors with a forward-bias condition of D_{SC} are involved in the charging loop of the C_{SC}. Contemporary, the top positive level of the output voltage is made similar to the steady-state operation. So, considering the active power support mode condition, C_{SC} is discharged at the top positive level. Regarding this technique, the large inrush current of the proposed inverter is alleviated by the provided QSC path and the filter/grid side impedance. It is worth noting that in case of standalone operation, again, the same start-up procedure is applicable since the large inrush current of the input dc source is limited by the filter/load side impedance. The duration of this soft-start operation depends on the time constant of the above-mentioned charging loop.

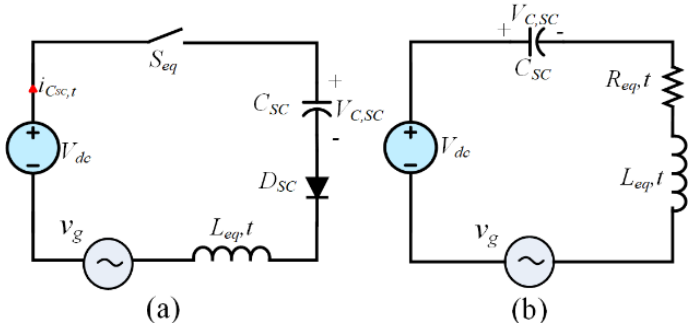


Fig. 6.4. Illustration of equivalent circuit during soft start modulation: (a) main transient charging loop, and (b) equivalent RLC circuit of the main charging loop.

Fig. 6.4 (a) and (b) shows this transient charging loop and its equivalent circuit scheme. Here, $R_{eq,t}$ and L_{eq} are the equivalent transient parasitic resistance and equivalent inductor of such a transient charging loop, respectively. Also, S_{eq} represent the role of S_1, S_{H1} and S_{H4}. Therefore, regarding the equivalent RLC circuit of the transient charging path depicted in Fig. 6.4 (b), the initial charging current relation of C_{SC} ($i_{Csc,t}(t)$) can be written as follows:

$$\frac{d^2 i_{Csc,t}(t)}{d^2 t} + \frac{2}{\tau}\frac{d i_{Csc,t}(t)}{dt} + \omega_{o,t} i_{Csc,t}(t) = \frac{1}{L_{eq}} v_g(t) \tag{75}$$

where, τ is the time constant of the RLC circuit and it is equal to $\frac{2L_{eq}}{R_{eq,t}}$. Also, $\omega_{o,t} = \frac{1}{\sqrt{L_{eq} C_{SC}}}$ is the resonant frequency of the transient charging loop. So, considering a very small value of $R_{eq,t}$ compared to L_{eq}, $i_{Csc,t}(t)$ can be expressed as:

$$i_{Csc,t}(t) = i_{Csc,t}(0) e^{-\frac{t}{\tau}} \cos(\omega_1 t + \varphi) \tag{76}$$

where ω_1 is defined in (77), while $i_{Csc,t}(0)$ and φ depends on the initial condition of the transient charging loop RLC circuit.

$$\omega_1 = \omega_{o,t} \sqrt{(1 - \frac{1}{\omega_{o,t}\tau})} \tag{77}$$

Therefore, considering (77), the duration of such a soft-start process to reach a stable voltage for $v_{C,sc}$ is limited by τ. Regarding such observations, the typical transient waveforms of the inverter output voltage (v_{AB}), $v_{C,sc}$, $i_{Csc,t}$, and the injected grid current (i_g) with and without the described soft start process are shown in Fig. 6.5 (a), and (b), respectively. Here, I_m is supposed to be the peak of the injected current to the grid. As it can be seen, without having the soft-start capability, a huge inrush current caused by the charging operation of the involved capacitor during the zero states output voltage level generation, appears at the beginning, while the peak of $v_{C,sc}$ exceeds the steady-state charged value of the C_{SC}. Also the stable settling time of $v_{C,sc}$ takes around three fundamental cycles of the grid (50 Hz). In contrast, within the proposed soft-start scheme and without any use of additional

sensors/relays, the charging inrush current is limited to only three-times of I_m, while after a quarter of the fundamental grid cycle, $v_{C,sc}$ can reach its stable point.

6.4. QSC Path Analysis

As described earlier, during the charging operation of C_{sc} at the zero level of the output voltage and in the steady-state condition, a QSC path including the power switch S_1 from the SC network, two power switches from one leg of the FB cell, the power diode D_{SC} and the quasi resonant of L_r is provided. Regarding this RLC circuit, the maximum steady-state charging current of C_{SC} can be limited to a permissible range tolerable by the involved semiconductor devices. Herein, such a QSC operation is possible once the under-damped condition of such an RLC circuit is fulfilled. So, considering R_{ch} as the ON state charging parasitic resistance of the involved semiconductors and equivalent series resistance of C_{SC}, the following relation can be written [128]:

$$R_{Ch} < \sqrt{\frac{4L_r}{C_{SC}}} \tag{78}$$

Therefore, considering such a QSC path, the steady-state voltage value across C_{SC} and its required charging current ($i_{Ch,Csc}(t)$) are obtained as the following relations, respectively.

$$v_{C,sc}(t) = V_{dc} - \frac{\beta}{\omega_r}\, e^{-\alpha t}(\alpha \sin \omega_r t + \omega_r \cos \omega_r t) \tag{79}$$

$$i_{Ch,Csc}(t) = \frac{\beta}{L_r \omega_r} e^{-\alpha t} \sin \omega_r t \tag{80}$$

where, β, α, and ω_r are denoted as the voltage factor coefficient of C_{sc}, the neper frequency of the QSC path, and the damped quasi-resonant frequency. The respective relations of such coefficients can also be found as follows:

$$\begin{cases} \beta = V_{dc} - V_{Csc,max} + \Delta V_{Csc} \\ \alpha = \frac{R_{Ch}}{2L_r} \\ \omega_r = \sqrt{\frac{1}{C_{sc}\, L_r} - \alpha^2} \end{cases} \tag{81}$$

Here, ΔV_{Csc} and $V_{Csc,max}$ are the maximum allowable voltage ripple and also the maximum voltage value of C_{SC} during the variation, respectively.

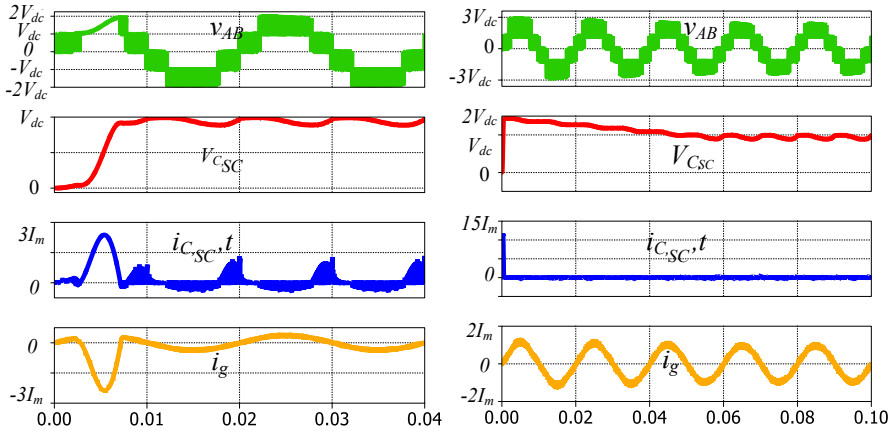


Fig. 6.5. Typical waveforms of v_{AB}, $v_{C,sc}$, $i_{Csc,t}$ and the injected grid current (a) with the proposed soft-start process (b) without soft-start process.

Now having taken the importance of such a described QSC path and considering (81), a standard and feasible value for L_r can be selected. Fig. 6.6 (a) and (b), shows the typical waveforms of the current passing through C_{sc} without and with such a small resonant inductor of the QSC path, whereas the waveforms related to the voltage across C_{sc} along with the injected grid current of the proposed inverter within a fundamental grid cycle are illustrated in Fig. 6.6 (c) and (d), respectively. As is clear from Fig. 6.6, the maximum charging current of C_{SC} $(i_{Ch,Max})$ becomes more than five times of I_m if no QSC path is provided, while it will be close to I_m in the presence of the QSC path. It is obvious that a reduction in the value of $i_{Ch,Max}$ leads to a smooth waveform in the current stresses profile of all the power switches that are involved in the capacitive charging loop. So, the QSC path can increase the operating efficiency of the converter.

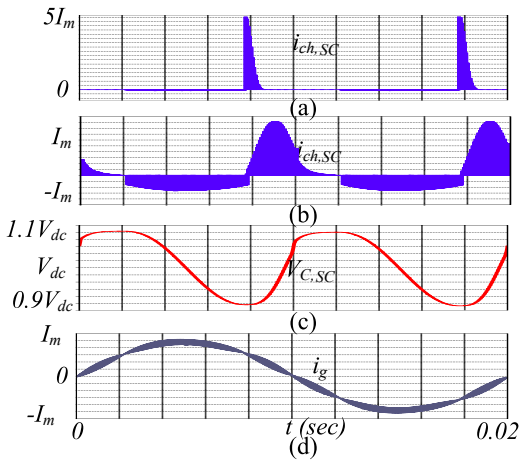
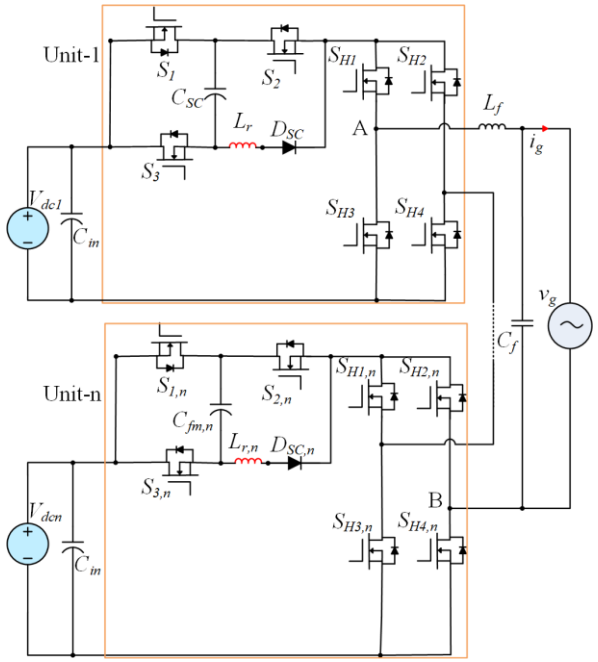


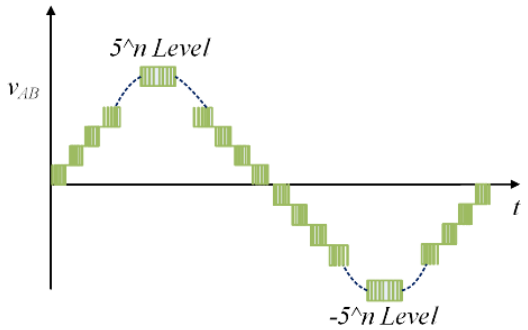
Fig. 6.6. Typical waveforms showing (a) current through C_{SC} without QSC path, (b) current through C_{SC} with QSC path ($L_r = 20\mu H$), (c), the voltage across C_{SC} with QSC path (d) the injected grid current with QSC path.

6.5. Generalized Cascaded Scheme of the Proposed SCMLI

Similar to the other available SCMLIs, the proposed topology can be generalized through its cascaded connection as shown in Fig. 6.7 (a). Herein, by choosing the value of the dc sources as (82), and considering "*n*" number of cascaded modules, the maximum number of output voltage levels can be taken as (83).



(a)



(b)

Fig. 6.7. A 5^n-level cascaded structure showing (a) a general topology and (b) 5^n–level output voltage waveform.

Fig. 6.7 (b) shows the typical waveform of this 5^n-level output voltage waveform.

$$V_{dc} = \left(5^{i-1}\right)V_{dc1} \qquad i = 1, \dots, n \tag{82}$$

$$N_{level} = 5^n \tag{83}$$

6.6. Design Guidelines

A component selection guideline at the end is helpful in estimation and selection of the parameters for the practical design. First of all, the voltage and current rating of the active switches and diodes must be selected just above the safety margin. Even though the input DC-link capacitor helps to maintain a constant voltage at the DC-link, there are some small spikes in practice across the semiconductor devices. As a result, the voltage and current rating of the selected semiconductor devices are 650 V and above 50 A accordingly. To select the components of the proposed inverter, a few more things need to be calculated such as switched-capacitor ($\boldsymbol{C_{SC}}$), filter inductor ($\boldsymbol{L_f}$), and filter capacitor ($\boldsymbol{C_f}$).

The switched-capacitor C_{SC} can be calculated by (88) which is dependent on the switched capacitor discharging amount (Q_{SC}) and the permissible voltage ripple across the applied input voltage (ΔV_{dc}) of the system.

$$C_{SC} \geq \frac{Q_{SC}}{\Delta V_{dc} V_{dc}} \tag{88}$$

On the other hand, the selection criteria mentioned here are for voltage source type inverters that only need small LC filter at the output to provide filtering for the output waveform. However, to reduce the inductor size, usually a capacitor is used in parallel with

the load, and hence, the solution here would be similar to the use of a low pass LC filter. To calculate the filter inductor value can be obtained by (89). The maximum ripple factor is approximately 0.25 which, applied in (89) together with a current ripple across the inductor of 40%.

$$L_f \geq \frac{v_g \times \Delta I_{Factor}}{f_{sw} \times \Delta I_{Lf}} \tag{89}$$

On the other hand, the filter capacitor (C_f) can be calculated by (90) where the cut-off frequency (f_c) is set to be 10% of f_{sw}.

$$C_f \geq \frac{1}{4 \times \pi^2 \times {f_c}^2 \times L_f} \tag{90}$$

6.7. Comparison with Different Topologies

The foremost challenging issue for multilevel inverter topologies is related to the number of active and passive components to improve efficiency and power density. Table 6.2 gives a the comparison of different single-phase 5L inverter topologies in terms of the required input voltage, power semiconductor devices, additional devices, boosting feature, required isolated DC source, output filter type, reactive power capability (RPC), total harmonic distortion (THD), cost, efficiency, and soft charging capability.

The NPC inverter uses twelve power switches and six diodes to achieve five levels, while ANPC and T-type 5L inverter have no requirements of diodes. Instead, they require additional capacitors. Diode clamped (DC), Flying capacitor (FC), and cascaded H-bridge (CHB) use eight power switches; however, the DC requires extra four capacitors and 12 diodes to achieve five levels in the output voltage. Moreover, CHB needs isolated DC sources. The required components for a 5-level inverter are one inductor, one capacitor, one diode and eight power switches. The proposed topology requires fewer components among other mentioned topologies except the topologies in [164], [165], [157], and [158].

Moreover, as seen in Table II, the proposed topology is capable of boosting the input voltage and the required filter size is very small. It has reactive power capability like the reported topology [158], [165], CHB [167], [168] and [169], and FC [182].

Table 6.2. Comparison with existing single-phase 5-L inverter topologies with proposed topology

Topologies	Power devices		Additional devices		Step Up feature	Need isolated DC sources	Input voltage, V_{in}(V)	Output filter type		Reported RPC	Reported THD (%)	Cost/ size*	Inrush current	Reported Efficiency (η)
	D	S	L	C				L_f (mH)	C_f (μF)					
[162]	1	8	1	2	Yes	no	100	0.68	4.7	yes	< 2.1	++	no	96.5%@ 500 W
[154]	4	6	0	2	no	no	400	2	0.47	n/a	< 5	++	yes	99.06 %@ 1kW
[168]	6	8	0	4	no	no	800	2	0.47	yes	2.18	+++	yes	96.3 %@ 1kW
[178]	0	10	0	3	no	no	400	n/a	n/a	n/a	n/a	++++	yes	n/a
[179]	4	10	2	2	yes	yes	200	3	-	n/a	n/a	++++	no	96.0 % @ 500 W
[169]	4	8	2	3	yes	yes	400	3	-	yes	1.8	+++	no	95.5 %@ 1kW
[164]	4	4	2	2	no	no	400	0.9	1.5	n/a	2.2	+++	no	93.5 %@ 500 W
[165]	2	6	0	2	no	no	400	3	3	yes	1.8	+++	yes	94.92 %@ 1kW
[172]	3	8	2	4	yes	yes	200	1.2	25	n/a	3.6	++++	no	91.0 %@ 2kW
[73]	2	8	4	4	yes	yes	200	1.2	-	n/a	4.6	++++	no	90.0 %@ 500 W
[1174]	6	8	4	4	yes	no	200	2.2	0.47	n/a	3.6	++++	no	92.50 %@ 1kW
ANPC [171]	0	12	0	5	no	no	800	5	-	n/a	3.51	++++	yes	n/a
DC [180]	12	8	0	4	no	no	400	8	-	n/a	n/a	++++	yes	n/a
NPC [170]	6	12	1	2	no	no	800	n/a	n/a	n/a	3	++++	yes	n/a
T-Type [181]	0	8	2	2	no	no	800	0.18	10	n/a	n/a	+++	yes	96.5 % @ 5kW
CHB [167]	0	8	0	2	no	yes	400	1	-	yes	n/a	+++	yes	n/a
[175]	0	12	0	4	yes	no	100	1.5	3	n/a	3.87	+++	yes	n/a
FC [182]	0	8	0	10	no	no	400	n/a	n/a	yes	n/a	++++	yes	n/a
[166]	0	8	0	2	no	no	400	1.4	4.7	yes	2.5	+++	yes	97.5 % @ 5kW
[158]	1	6	0	3	no	no	400	2	-	yes	3.5	+++	yes	96.6 %@ 1.4 kW
[176]	1	8	0	2	no	no	400	8	-	n/a	< 5	++	yes	96.8 % @ 1kW
[177]	4	6	0	2	no	no	400	3	n/a	n/a	n/a	++	yes	98.65 %@ 1kW
[157]	2	6	0	2	yes	no	200	2.9	-	yes	2.2	++	yes	98.1 %@ 500 W
[183]	0	6	0	2	yes	no	200	0.4	2.2	n/a	n/a	++	yes	98.5 % @ 1kW
[152]	2	7	0	2	no	no	400	1.6	n/a	yes	1.6	++	yes	n/a
[184]	0	8	0	2	no	no	400	3	n/a	n/a	2.85	++	yes	n/a
[185]	4	7	0	2	yes	no	200	n/a	n/a	yes	n/a	+++	yes	n/a
Proposed Inverter	1	7	1	1	yes	no	200	0.8	2.2	yes	1.4	++	no	98.8 % @ 1kW

Note: *More "+" represents the higher cost/size: "+" ≡ low, "++" ≡ medium, "+++" ≡ high, and "++++" ≡ extremely high.
In the above table, "S" represents switch, "D" represents diode, "C" represents a capacitor, "L" represents inductor, "V_{dc}" input voltage, "RPC" reactive power capability, "THD" reported total harmonic distortion, "n/a" not available.

On the other hand, the THD is reduced to 1.4% for the proposed topology where THD shows more for [154], NPC [170], ANPC [1171], and [172]-[176]. The prototype cost and size depend on the number of components required in the system design. A careful analysis and comparison of the cost of the mentioned topologies and the proposed topology reveal that the cost and size of the proposed topology are reasonably less [176], just a little higher than [164], [166] and [177]. Finally, the proposed topology features the capability of quasi-resonant charging of the capacitors (soft-charging), which results in reducing the current spike on the devices and thus enhances the performance by increasing the reliability and lifetime of the inverter.

6.8. Performance Evaluation

6.8.1. Components Selection for Performance Evaluation of proposed topology IV

The performance of the proposed inverter concept is validated by the laboratory measurement results through the OPAL RT with eHS module. The specification of the converter is shown in Table 6.3.

Table 6.3. Grid Parameters and Components used for Simulation and real Time Implementation

Description	Value/Parameter Used for Measurement
Input voltage (V_{dc})	200 V
DC-link Voltage (V_{PN})	412 V
Output voltage (v_g)	240 V
Power rating (P_O)	1000 VA
Sampling frequency (f_{sp})	30 kHz
Line frequency (f)	50 Hz
Switched capacitor (C_{SC})	470 µF, 250 V
Soft charging inductor (L_r)	58 µH, 0.01 Ω
Filter inductor (L_f)	0.8 mH
Filter capacitor (C_f)	2.2 μF
Switches ($S_1 - S_3$) and ($S_{H1} - S_{H4}$)	C2M0080120D (1200 V, 31 A, 80 mΩ)
Diodes (D_{SC})	C4D20120D (1200 V, 68 A)
Dead time	450 ns

6.8.2. OPAL-RT Implementation

Fig. 6.8 shows the pulse-width modulation signals generated for all switches in quasi resonant active switches (S_1, S_2 and S_3), and H-bridge switches ($S_{H1}-S_{H4}$). The voltage stress on the switch in the quasi resonant active switch is half of the H-bridge circuit switches. Hence, the maximum voltage stress on the switch is 400 V for all switches in the H-bridge and 200 V for the switches in the quasi resonant switches.

The RMS value of the output voltage and current is 236.5 V and 4.38 A. The reactive power operation mode is also demonstrated as shown in Fig. 6.11 with a power factor of 0.834. The inverter still produces good-quality voltage and current waveforms without high distortion (THD < 1.4 %). As shown in Fig. 6.12, the reference current is changed between 4.38 A RMS to 3.8 A RMS.

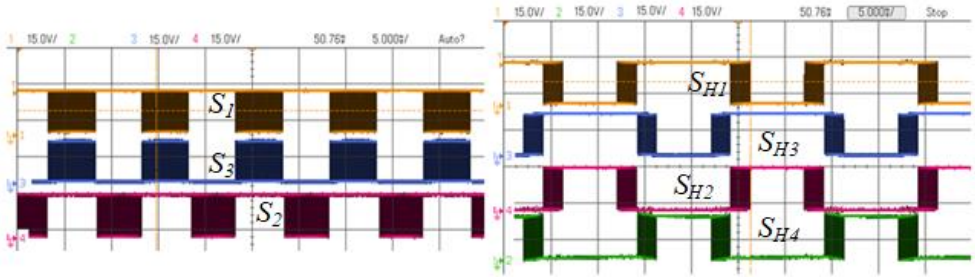


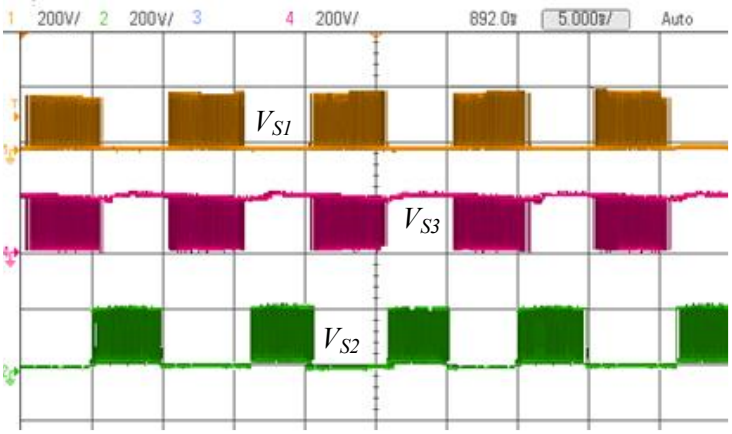
Fig. 6.8. Measured gate signals: (a) active switched capacitor network switches (S_1, S_2 and S_3), and (b) H-bridge network switches ($S_{H1}-S_{H4}$).

Fig. 6.9 shows the waveforms of the voltage stress of all semiconductor devices along with the switched-capacitor. Fig. 6.9 (a) shows the voltage stress of quasi resonant switches and Fig. 6.9 (b) displays the voltage stress of H- bridge switches. The voltage stress of the diode and switched capacitor is shown in Fig. 6.9 (c) and Fig. 6.9 (d) respectively. In both cases, voltage stress is half of the H-bridge circuit switches. Fig. 6.10 shows the input applied voltage, inverter input/output voltage and current waveforms with five clear levels of the output voltage with a clear sinusoidal output voltage and current. This result shows that the proposed structure can function in any dynamic condition and keeps the inverter output voltage to five levels. Additionally, the output voltage and current are sinusoidal. Fig. 6.13

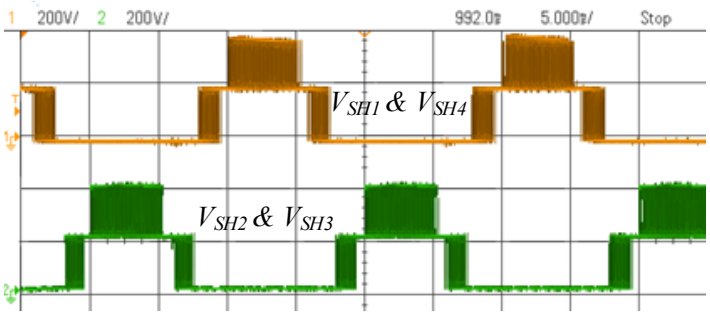
shows sudden change from active to reactive power. However, still the proposed structure keeps the inverter output voltage to five levels. Additionally, the output voltage and current show to be sinusoidal.

The simulated average power loss distribution and the resultant junction temperature (T_j) of the individual switching elements are presented in Fig. 6.14 (a). Fig. 6.14(b) and Fig. 6.14 (c) show similar findings and the loss distribution across the switching components. Finally, the total conduction losses, switching losses, and total losses are shown in Fig. 6.14 (b).

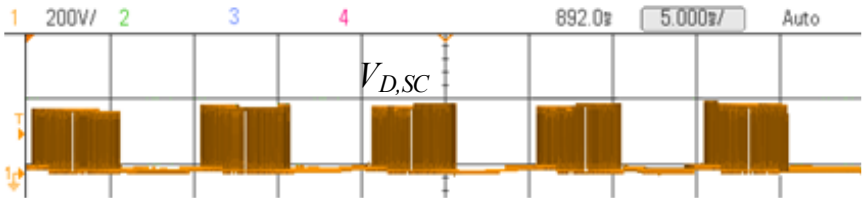
Fig. 6.14 (c) shows total loss distribution where it can be seen that, the power loss in the active switched-capacitor (SC_{Loss}) is increased by 16% from H- bridge (FB_{Loss}) due to the higher conduction losses in the capacitor-charging path. Finally, the overall efficiency curve for different rated power is illustrated in Fig. 6.14 (d).



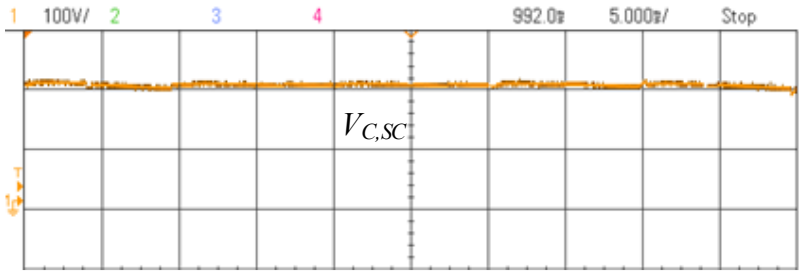
(a)



(b)



(c)



(d)

Fig. 6.9. Measured voltage stress on semiconductor devices and capacitor: (a) voltage stress on active switched capacitor network switches (S_1, S_2 and S_3), (b) voltage stress on H-bridge network switches ($S_{H1}-S_{H4}$), (c) voltage stress on diode (D_{SC}), and (d) voltage stress on switched-capacitor (C_{SC}).

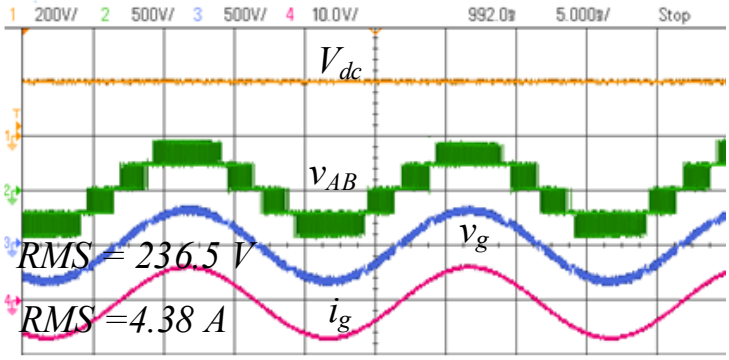


Fig. 6.10. Measured input applied voltage (V_{dc}), inverter voltage (v_{AB}), output voltage (v_g), and current (i_g) in unity power factor.

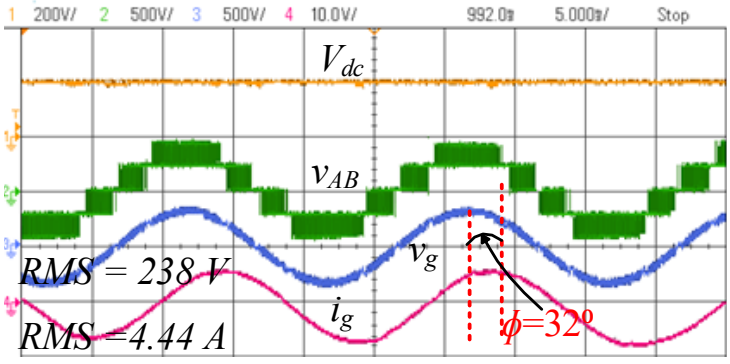


Fig. 6.11. Measured input applied voltage (V_{dc}), inverter voltage (v_{AB}), output voltage (v_g), and current (i_g) in non-unity power factor (φ=32°).

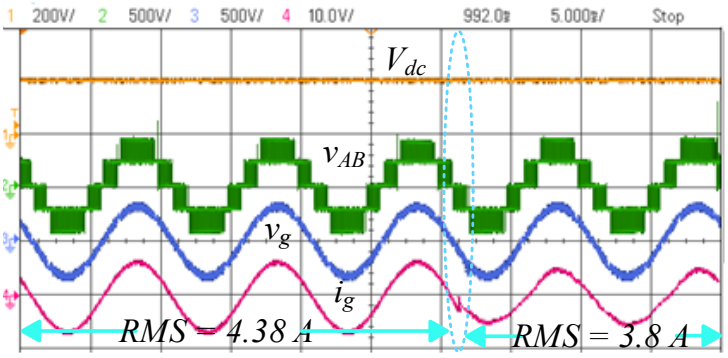


Fig. 6.12. Transient response of the proposed topology after sudden reference current changing from 4.38A to 3.8A.

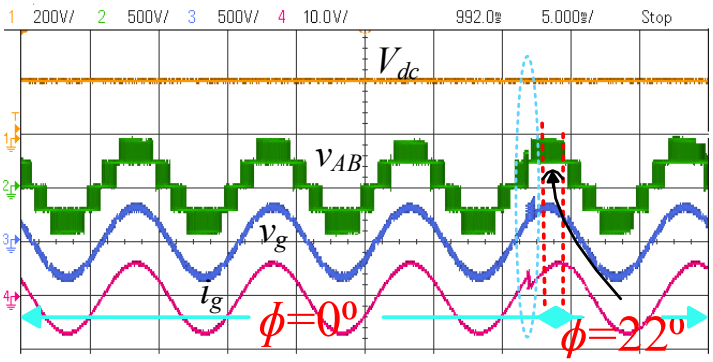


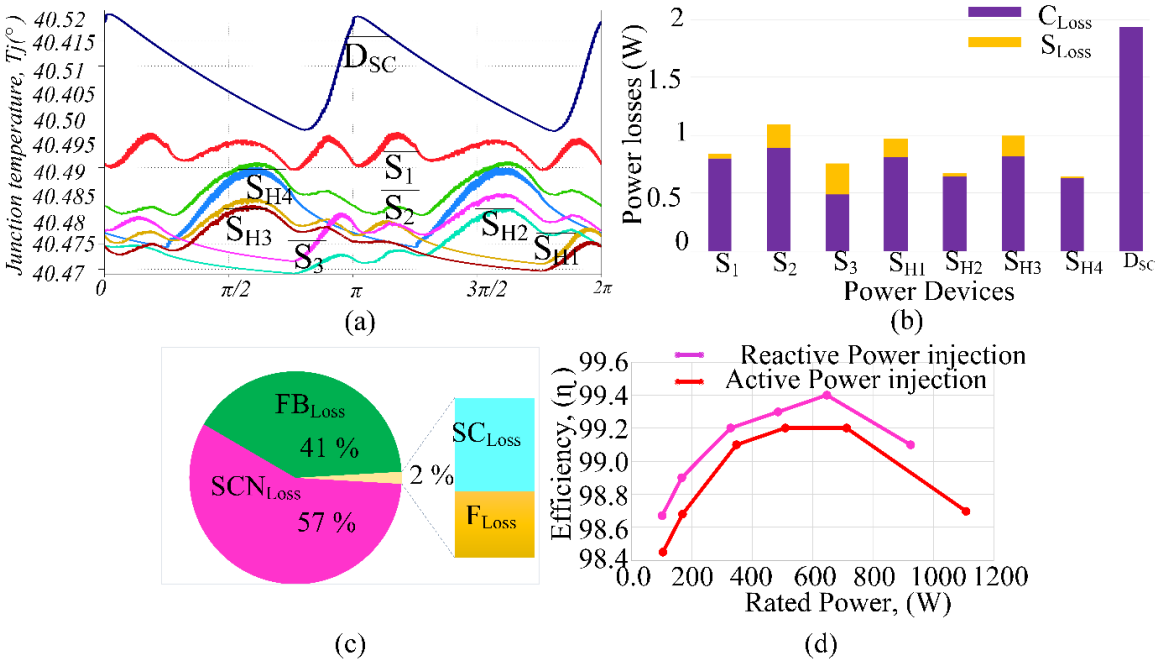
Fig. 6.13. Transient response of the proposed topology from active power to reactive power.

It has 99.4% peak efficiency for injecting the reactive power to the grid and 99.2% peak efficiency for injecting the active power to the grid. In full load condition, the efficiency reaches 99.2% in reactive power injection and 98.7% efficiency after injecting the active power to the grid.

6.9. Summary

A novel voltage boosting capability-based single-phase multilevel inverter topology is proposed in this chapter. This topology requires only seven active switches, a diode, an inductor, and a capacitor for 5L voltage generation, which is the minimum component count compared to the existing topologies. This topology reduces the dc supply voltage requirement by 75% compared to the existing NPC, ANPC, and CHB topologies, and by 50% compared to hybrid topologies. This feature eliminates the multi-stage dc-dc power conversion system of the grid-connected PV system. It has soft-start and quasi-resonant charging capability. The inherent self-balanced capacitor's voltage reduces the control complexity and additional

sensor circuit requirement. To validate the proposed topology and its modulation performance, some laboratory measurement results have been presented.



Note: C_{Loss} = Conduction losses, S_{Loss} = Switching losses, F_{Loss} = Filter losses, SC_{Loss} = Switched capacitor losses, FB_{Loss} = FB Cell losses, and SC_{Loss} = Switched-capacitor network losses.

Fig. 6.14. Converter (a) junction temperature, (b) switching and conduction losses, (c) total loss distribution in full load condition and (d) efficiency curve for different rated power (considering only semiconductor loss).

Chapter 7

Conclusion and Future Works

This chapter concludes the PhD thesis and it consists of a summary as well as some future research directions. The objectives of this chapter is to summarize the works, which have been conducted throughout this PhD project, and proposes some works for the future to investigate more in the area of research.

7.1. Summary of the Ph.D. Thesis

This dissertation mainly focused on the analysis and design of single-phase transformerless PV inverter, which strictly maintains the safety standard such as IEEE 1547.1, VDE0126-1-1, EN 50106, IEC61727, and AS/NZS 5033. Addressing the need of current trend and technological updates on the single-phase transformerless inverter, a comprehensive literature review of single-phase transformerless inverter topologies has been presented in the beginning of the thesis. A complete summary of various circuit structures considering CM effect, semiconductor devices, thermal analysis, power density, and efficiency is presented. This help to comprehend a global picture of the transformerless inverters and helps to identify their pros and cons and the technological roadmap. Upon understanding the concept to overcome the limitations of transformerless inverter topologies, a three-level transformerless

topology has been proposed initially in Chapter 3, which helps to maintain a constant common-mode voltage, which mitigate the leakage current in the transformerless inverter systems. Research from the topological prospective with multilevel output voltage is also equally important and attractive to reduce the size and cost of the system. In Chapter 4, a (2n+1)-level inverter with inherent voltage boosting capability have been presented to achieve a compact and high efficient dc-ac inverter with less number of semiconductor devices. In addition to this an entirely novel topology of multilevel inverter, "dual-mode five-level common grounded type (5L-DM-CGT)" transformerless inverter topology for a medium-power application with a wide input voltage range (200 V – 400 V) has been proposed in Chapter 5. The major advantage of the presented concept is its capability to operate in both buck and boost mode to accommodate wide range of input voltage whilst generating smooth five-level voltage at the output of the inverter. Finally, a soft charging and quasi resonant charging concept have been presented in Chapter 6 for switch capacitor based multilevel converter improve the efficiency, reliability and lifetime of the components and converter systems. The presented concept is general and can be implemented to any switched capacitor based converter without the need of any extra sensor or relay to pre-charging the switching capacitor.

7.2. Contributions

In conclusion, main contributions of this thesis to knowledge and understanding of the field are:

✓ A comprehensive review of single-phase transformerless PV inverters, including circuit structure, modulation technique, thermal modeling, and analyzing the common-mode effect, cost, power density, and converter efficiency to help both academic and industry readers for identifying their best DC-AC inverter selection. (Chapter-2).

✓ Design a three-level transformerless PV inverter called "H-Bridge Zero Voltage Switched Controlled Rectifier (HB-ZVSCR)" with higher efficiency, less complexity, Less CM effect, high power quality, light weight, and affable cost. The topology is hardware-implemented for 1.5 kW. (Chapter-3).

✓ To increase the voltage level with lower number of semiconductor devices are presented which is a single-phase switched-capacitor (SC) boost capability based (2n+1)-level inverter. It has soft charging capability, hence no inrush current in the input and capacitors. It shows very smooth output voltage and current with around 2% THD and it can provide reactive power support to the grid. The topology is hardware-implemented for 500 kVA. (Chapter-4).

✓ To eliminated the ground leakage current a new single-phase common grounded type five-level inverter for a medium- power application with a wide input voltage range (200 V – 400 V) has proposed. The topology is hardware-implemented for 1000 kVA. (Chapter-5).

✓ Design a novel configuration of switched capacitor based five-level inverter to reduce the inrush current profile of the converter, and proposed new modulation process for soft start up, thus a soft start and quasi-resonant charging capability has been explored and implemented. (Chapter-6).

7.3. Possible Future Works

In this thesis, several aspects have been documented for single-phase transformerless inverter topologies. However, there are still many possible works which may improve the system performance. Some important issues which are highly interesting for future studies are listed below:

- Design of more compact size of single-phase and three-phase transformerless DC/AC multilevel inverter through Gallium nitride (GaN) power devices for medium and high power application.
- When the grid is abnormal, the PV inverter needs to disconnect from the grid. A control scheme needs to be developed and further investigated to make the inverter to operate between grid-tied mode and islanding mode.
- Design of more advanced controlled like fixed switching mode model predictive control (MPC) to enhance the PV inverters dynamic performance.
- Investigation of soft-switching, and quasi resonant charging technique, to further push the efficiency of the inverters.

- The use of multiple switched capacitor units in a cascaded manner to realize boosted and multilevel output voltage initiates some critical issues to investigate, e.g., fault-tolerant capability, dynamic response of the inverter, and some power device have to block the higher than the DC supply voltage. Also, the common-mode voltage (CMV), leakage current, low voltage ride through (LVRT) capability, unsymmetrical loading of power devices, and losses distribution across the power devices might be the interesting research directions.

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