Topology, Modeling and Control Scheme for a New seven-level Inverter with Reduced DC-Link Voltage

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***Abstract*—This paper presents a new single-source three-phase seven-level inverter with an inherent three-time voltage boosting capability for medium-voltage applications. The proposed topology is comprised of series connection of two switched-capacitor (SC) networks with an added half-bridge module per phase. Each of such integrated SC networks requires a single capacitor associated with three active power switches. The three-time voltage boosting feature of the proposed topology can reduce the dc-link voltage requirements by 50% in comparison to the traditional neutral point clamped (NPC), flying capacitors, active NPC (ANPC), hybrid and hybrid clamped ANPC and cascaded H-bridge topologies, and 75% to advanced ANPC topologies. It can also reduce the number of required switches and capacitors as well as their voltage stresses compared to those state-of-the-art topologies reported in the literature so far. By integrating "n" number of added SC networks in the proposed seven-level basic topology, the number of output voltage levels can be extended to 2n+3 per phase. A finite control set model predictive control algorithm is also derived to control the converter in both the active and reactive power exchanges modes without distorting the generated grid current quality. The capacitor voltage balancing is inherent in the proposed topology, and thus, there is no need for any additional voltage balancing circuit, which further reduces the control complexity. The performance of the proposed topology and its control algorithm are validated by several measurement results.**

***Index Terms*— Model predictive control, multilevel converter, switched capacitor, voltage boosting, power control.**

I. Introduction

RENEWABLE energy sources (RESs) are the long-term sustainable energy sources. Nowadays, they are becoming more and more popular due to the ever-growing concerns of global environment and energy sustainability. To overcome the energy crisis, more and more systems are being built around the world for energy harvesting from the clean RESs, such as photovoltaic (PV) and wind energy sources, and they are used in conjunction with the centralized electrical power generators to support the utility grid as well as to improve grid stability. The grid-connected power converter plays a crucial enabling role for integrating these RESs into the electricity grid. Such interfacing module can be implemented by either a single-phase or three-phase power converter. These converters are generally cost-driven, which limits the massive deployment of RESs in the grid. Hence, the main challenge is to develop a power converter that can provide high-quality ac power to the grid with a low cost. The dc-ac voltage source inverter (VSI) is the main device currently used as an interface between the PV and the ac power grid. The PV panels can be either directly connected to the VSI or through a boost stage, depending on the inverter topology and the voltage level of PV panel [3, 4]. For grid-connected applications, VSIs are responsible for dealing with increasingly stringent grid connection standards, power quality, reliability, and robustness as well as performing other ancillary services. For residential and commercial applications, the common VSI topologies usually used to interface the RESs to the grid are the two-level ones. In recent years, multilevel inverters (MLIs) are receiving more and more attentions, and have been extensively used in a range of low and high voltage power conversion applications, especially in renewable energy systems [5-7]. A higher number of output voltage levels enables higher quality output waveforms, which leads to reduced filter size, higher electromagnetic compatibility, and lower switching losses. Meanwhile, the MLIs have less *dv/dt* stress on the semiconductor devices, which enables the use of low-cost switching devices, and consequently, increases their efficiency [8-10].

Many MLI topologies have been reported in the literature with some basic concepts [5]. Still more new topologies with various application-oriented approaches are being proposed and investigated. Among them, the cascaded H-bridge (CHB), firstly proposed in the 1990s, is the mostly employed topology to synthesize the multilevel output voltage. This topology is becoming prominent due to its modularity and symmetric converter structure [12-17]. The neutral point clamped (NPC) converter is another extensively used one since its proposal in the 1980s [14, 18, 19]. These two classic topologies are considered as the base structures to derive many other multilevel converters proposed in recent years [5]. Several other popular multilevel converter topologies include the flying-capacitor (FC) converter [8, 11, 20, 22], T-Type converter [7, 15], active NPC (ANPC) converter [24], hybrid multilevel NPC converter [8, 18, 21, 25], modular multilevel converters (MMC) [15, 26], and hybrid topologies based on the combination of CHB, FC and NPC topologies [27-29]. The CHB converter structure can generate a large number of output voltage levels by employing the cascaded H-bridge structure and provide loss equalization by using a simple pulse width modulation (PWM) technique. Due to its high redundancy states and modularity,

this converter structure is suitable for the fault-tolerant applications. Nevertheless, it requires a large number of power devices and independent dc-links in higher voltage level generation, and hence, increases the cost, volume and control complexity remarkably. Moreover, in the CHB converter structure, each dc-link requires a large electrolytic capacitor to absorb the power ripple generated by the H-bridge. Consequently, this reduces the reliability and lifetime of the converter [6, 15, 17, 26, 30, 31].

Similar to the CHB topology, the FC converter can achieve fault-tolerant operation by programming the converter control in redundancy states [33]. This topology, however, requires a large number of capacitors when a large number of voltage levels are synthesized. This topology also suffers from the capacitor voltage unbalancing problem, and consequently, requires a complex control strategy to achieve the balanced capacitor voltages [11, 20, 34, 35]. In contrast, the control of NPC converter is simple and popular in industrial applications. Nevertheless, it suffers from the dc-link capacitor voltage unbalancing as the number of voltage levels increases, and thus, increases the control complexity [5, 15, 32]. The T-type converter requires fewer number of components compared to the NPC converter topologies, and is simple to control. However, a higher voltage stress is observed across the power devices in the T-type converter [5, 7, 15]. Similar to the FC converter, the MMC converter requires a complex control strategy due to the use of a large number of capacitors in its structures [6, 26]. For grid-connected inverters, the dc-link voltage should be higher than the peak of the ac voltage output. The voltage requirements can be up to double the ac output voltage for some topologies like the traditional NPC inverter. Table I presents a comparative study of different topologies in terms of the level of output voltage and its p.u. magnitude for a specific dc-link voltage.

It can be observed that the hybrid clamped topologies require equal or smaller dc-link voltage compared to the mid-point clamped topologies for the same maximum voltage level generation. Therefore, in some applications like grid-connected PV systems, a high boost dc-dc stage is required to provide the required voltage level to feed the mid-point clamped topologies, which can be realized by using an additional dc-dc boost converter, or a large number of series-connected PV panels.

TABLE I. PEAK PHASE-PHASE VOLTAGE ($\hat{V}_{ph}$) OF DIFFERENT SEVEN-LEVEL INVERTERS (FOR $V_{DC} = 400 = 1\ p.u.$)

Mid-point Clamped	Hybrid Active-Clamped			Switched Capacitor	ANPC		Proposed Topology
[1, 2]	[20]	[23]	[21]	[36]	[37]	[6]	
1/2	1	1/2	3/4	3/2	3/2	1	2

The use of multiple converters as the front-end converter not only reduces the overall system efficiency and reliability, but also increases the system cost, converter size and control complexity. For PV applications, alternately, a series of PV panels can be employed to eliminate the extra boost stage to provide the desired dc-link voltage level. However, the series connection of PV panels can cause mismatch among the PV panels, which reduces the amount of energy extracted from the PV panels. Thus, a single-stage dc-ac inverter with voltage boosting capability can be an interesting way compared to a multi-stage power conversion system [20].

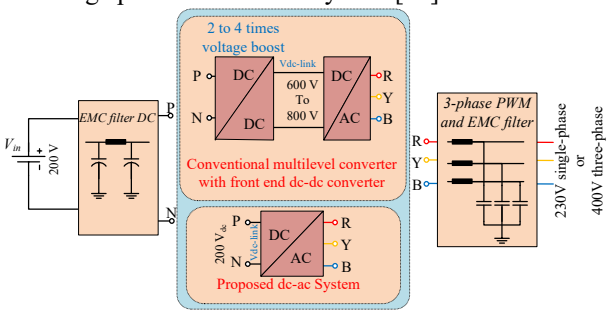


Fig. 1. Illustration of the conventional two-stage converter (dc-dc + dc-ac) system and single-stage (dc-ac) system with proposed multilevel topology.

Recently, the hybrid and ANPC converter topologies have received much attention in medium power applications because these topologies combine the advantages of the classical topologies, such as FC, CHB, and NPC converters [21, 38, 39]. The major drawback of these topologies is that they still require a large number of components and high dc-link voltage. Thus, addressing the shortcomings of the classical topologies has become the main motivation behind developing more attractive converter circuits.

This paper proposes a new switched-capacitor (SC)-based topology of multilevel inverters, which can be suitable for many renewable energy-based applications like grid-connected systems. The proposed three-phase seven-level SC-based inverter offers the highest voltage boosting capability compared to the other existing converter structures. The high voltage boosting capability of the proposed structure reduces the required dc-link voltage requirement significantly to generate the required peak output voltage. In the proposed structure, a reduced voltage stress is also observed across the switching devices and capacitors compared to the existing structures. These advantages significantly reduce the cost of the converter. The self-voltage boosting capability of the proposed structure also reduces the control complexity and the required sensor circuits. Thanks to such an inherent voltage-boosting feature, a single-stage energy conversion system can be possible with a relatively lower value of the input dc voltage. Fig. 1 illustrates the conventional two-stage converter (dc-dc and dc-ac) system and the single-stage (dc-ac) system with the integration of the proposed multilevel inverter topology.

The paper is organized as follows: Section II presents the concept of the proposed multilevel inverter topology emphasizing the working principles of its seven-level derived basic topology. The current stress and capacitance determination principles are discussed in Section III, while the modelling and control are presented in Section IV. Following, a comprehensive comparison is presented in Section V, whereas Section VI presents the experimental validation. The conclusions are finally drawn in Section VII.

II. THE PROPOSED CIRCUIT TOPOLOGY

Fig. 2 illustrates one phase-leg of the proposed three-phase inverter constructed based on SC technique. Considering a seven-level SC-based inverter as an example, the proposed topology requires eight active switches, two capacitors, and a

single dc source. As depicted in Fig. 2(a), S_{X1}, S_{X2}, S_{X3}, …, S_{X8} (X ∈ (R, Y, B) phases) are active switches, where switches S_{X2} and S_{X5} are reverse blocking IGBTs and the other six switches are the standard unipolar devices, e. g. either MOSFETs or IGBTs. Two reverse blocking switches can also be made through the standard IGBT/MOSFET module with a series diode.

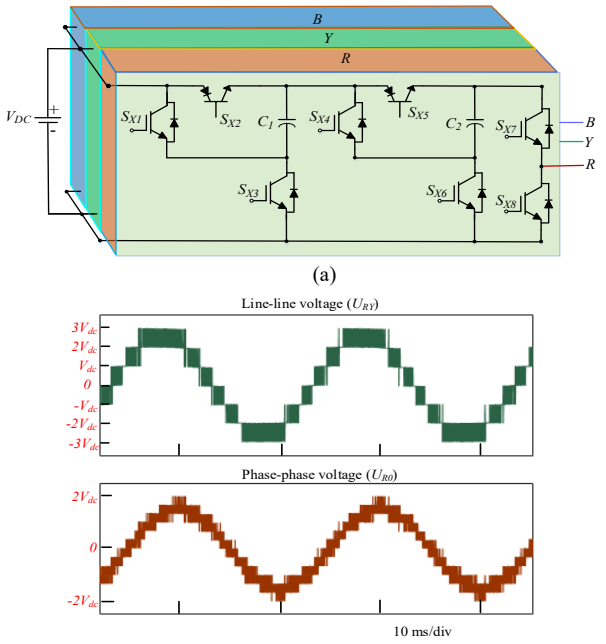


Fig. 2. (a) Proposed seven-level three-phase inverter circuit and its (b) output line voltage (U_{RY}), and phase voltage (U_{R0}).

To achieve a three-time voltage boosting gain, two SC cells including, C_{X1} and C_{X2}, are incorporated with the input dc voltage source, while the proposed topology can generate up to $3V_{DC}$ at the output terminal (before the filter) where V_{DC} is the magnitude of input dc voltage.

The switching states of the converter are designed to charge the capacitors C_{X1} and C_{X2} to V_{DC} from the input supply voltage through the switches S_{X3} and S_{X6}, respectively, and to achieve the balanced voltage around the reference value V_{DC}. For further analysis and providing a base for comparison, the maximum level (line to line) voltage is defined as 1 p.u. The line and phase voltages of the proposed topology are shown in Fig. 2(b). A major advantage of the proposed topology is that its number of output levels can be increased by cascading similar SC units in series, which will be discussed in the following.

The switching states of the proposed seven-level SC-based inverter current flowing paths in different output voltage levels are presented in Table II and Fig. 3, respectively. As is clear, each switching state has a distinct effect on charging/discharging process of the involved capacitors. Regarding Fig. 3, the gate switching pulses of the involved switches to generate seven-output voltage level per phase have also been shown in Fig. 4.

The prominent features of the proposed SC-based MLI are summarized as follows:

(1) The presented three-phase inverter offers a two-time voltage boosting capability, while the maximum voltage boosting capability of the existing topologies is 1.5 times as reported in the literature. Thus, the proposed structure

TABLE II. SWITCHING STATES OF THE PROPOSED CONVERTER

Stage	*Level*	U_{XO}	S_{X1}	S_{X2}	S_{X3}	S_{X4}	S_{X5}	S_{X6}	S_{X7}	S_{X8}	i_{C1}	i_{C2}	V_{C1}	V_{C2}
A	1	*0*	0	1	1	0	1	1	0	1	i_{c1f}	i_{c2f}	↑	↑
B	2	$+V_{DC}$	0	1	1	0	1	1	1	0	i_{c1f}	i_{c2f}	↑	↑
C	3	$+2V_{DC}$	0	1	1	1	0	0	1	0	i_{c1f}	$-i_x$	↑	↓
D	4	$+3V_{DC}$	1	0	0	1	0	0	1	0	$-i_x$	$-i_x$	↓	↓

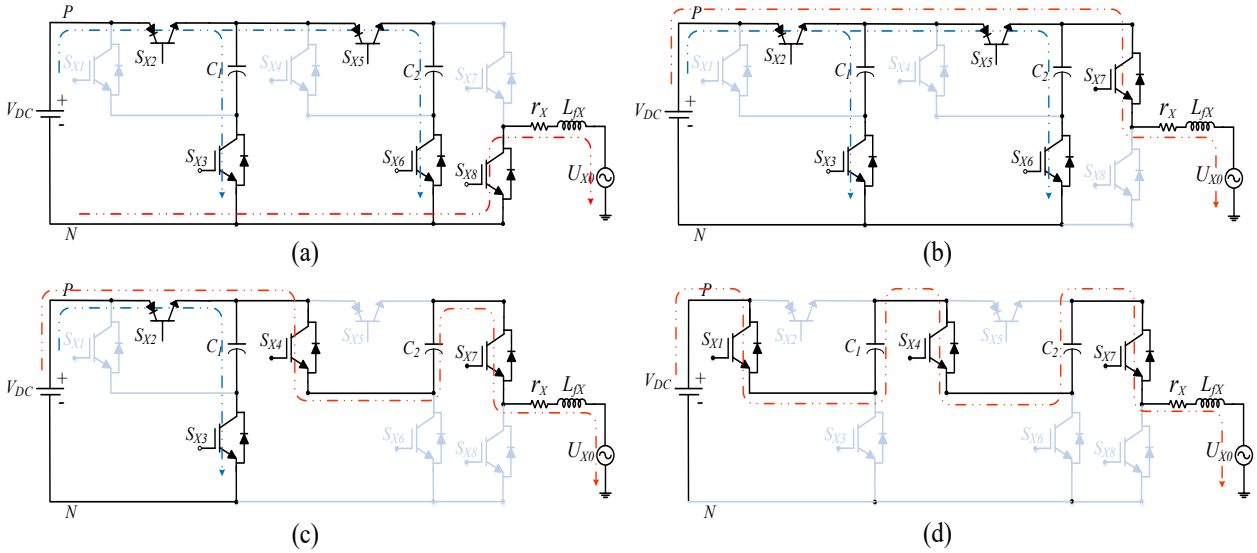


Fig. 3. Four switching states of the proposed inverter: (a) State A: 0, (b) State B: +1, (c) State C: +2, and (d) State D: +3.

requires a minimum dc-link voltage supply compared to the other existing topologies.

TABLE III. MAXIMUM VOLTAGE STRESS ON THE COMPONENTS OF THE PROPOSED CIRCUIT (MAX. PHASE VOLTAGE = 400 V =1 *p. u.*)

Devices	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	C_{x1}	C_{x2}
Voltage Stress (p.u.)	0.5	0.5	0.5	0.5	0.5	1	0.5	1.5	0.5	0.5

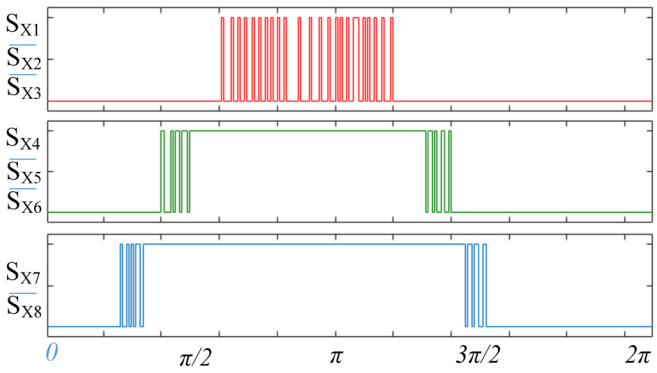


Fig. 4. Gate signals of the switches.

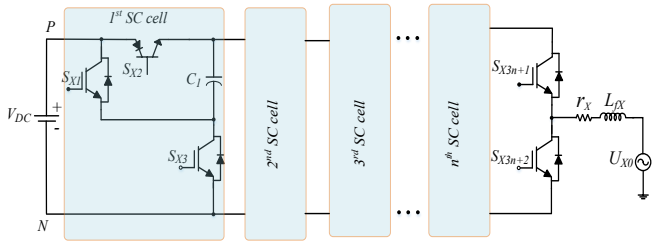


Fig. 5. The generalized version of the proposed SC-based MLI.

(2) The voltage stress across the power switches is less than the conventional topologies. As a result, the cost of the semiconductor devices is reduced. Details of maximum voltage stress across the switches and the capacitors in per unit scale are reported in Table III.

(3) The proposed structure requires minimum dc-link voltage and consists of only two capacitors, where the voltage stress on the capacitors does not exceed the dc-link voltage. This, as a result, reduces the cost and size of capacitors.

(4) The proposed circuit does not require any additional sensor or control strategy to balance the capacitor voltages.

(5) The proposed converter can be operated at either leading or lagging power factor, and thus it can feed reactive power to the grid if required.

(6) It requires less number of components than those of the NPC, ANPC, and FC converter topologies. For example, the seven-level inverter requires only eight active switches and two capacitors in each lag.

(7) By adding several SC-cells in series to each other, the proposed SC-based MLI can be generalized to achieve higher static voltage boosting gain and more number of output voltage levels as shown in Fig. 5. Regarding this

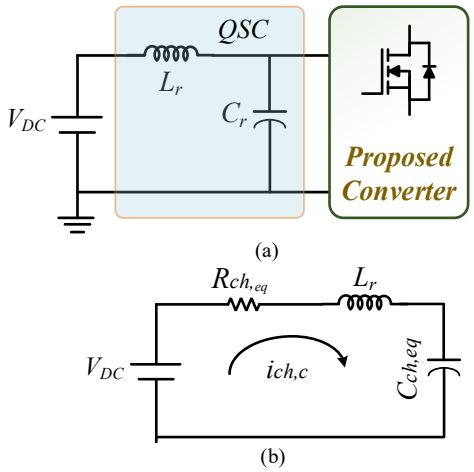


Fig. 6. (a) The QSC-based configuration of the proposed SC-based MLI , (b) The equivalent RLC circuit of the quasi-resonant capacitive charging loop.

and considering "n" as added number of SC-cell, the following equations as for addressing the possible number of inverter output voltage levels per each phase, total number of required power switches per each phase and total number of needed capacitors per each phase can be derived as:

$$N_{level} = 2n + 3 \quad (1a)$$

$$N_{Switch} = 3n + 2 \quad (1b)$$

$$N_{Cap} = n \quad (1c)$$

III. CURRENT STRESS AND SC CELL CAPACITANCE DETERMINATION

Similar to any other SC-based MLIs, the involved power switches of the capacitive charging loop may experience a large current stress caused by parallel connection of the capacitors with the dc source. To alleviate this problem in practice, an LC-based quasi-soft charging (QSC) filter can be configured in the input side of the proposed SC-based MLI as shown in Fig. 6 (a). Regarding such an QSC-input filter, an RLC resonant circuit can appear, which corresponds to the equivalent parasitic resistance of the capacitive charging path ($R_{ch,eq}$) as well as the equivalent capacitance of the path ($C_{ch,eq}$) as shown in Fig. 6 (b). The provided resonant RLC circuit can sluggish the charging current of the involved capacitor. Herein, if an under damp operation of the RLC series circuit is fulfilled, the value of L_r must meet the following relation [40]:

$$L_r = \frac{R_{ch,eq}{}^2 C_{ch,eq}}{4} \quad (2)$$

Through the under-damp operation of the above-mentioned quasi-resonant RLC circuit, the charging current of the involved power switches as well as the SC-cell capacitors conform an exponential trend as the following relation:

$$i_{ch,C}(t) = \frac{V_{dc} - V_{C,\max} + \Delta V_C}{L_r \omega_r} e^{-\alpha t} \sin \omega_r t \quad (3)$$

Table IV. Duty Cycles and Capacitors Status Per Each Switching Time Interval.

Duty Cycles for Switching States of A and B	Duty Cycles for Switching States of B and C	Duty Cycles for Switching States of C and D
$d_A(t)=1-3d(t)$ $d_B(t)=3d(t)$	$d_B(t)=3d(t)$ $d_C(t)=3d(t)-1$	$d_C(t)=3d(t)-1$ $d_D(t)=3d(t)-2$
C_1&C_2: Charged at states A and B	C_1 : Charged at states B and C & C_2: Charged at state B /Discharged at state C	C_1: Charged at state C /Discharged at state D C_2: Discharged at states C and D

where ω_r is the resonant frequency that should cover the operating switching frequency of the proposed SC-based MLI. Also, $V_{C,\max}$, ΔV_C and α represent the maximum value of the capacitor's voltage during the switching variation, the maximum voltage drop across the capacitors and a constant coefficient equal to $\alpha = R_{ch,eq}/2L_r$, respectively.

However, if the value of L_r is to be very low and a large capacitance is to be adopted to cancel out the effect of capacitors ripple voltage drop, the equivalent RLC circuit is then operated in over-damped condition. In this case, the charging current of the capacitors conforms the following expression:

$$i_{ch,C}(t)=\frac{C_{ch,eq}}{2}\left(s_1A_1e^{s_1t}+s_2A_2e^{s_2t}\right) \tag{4a}$$

$$\begin{cases} s_{1,2}=-\dfrac{R_{ch,eq}}{2L_r}\pm\sqrt{\left(\dfrac{R_{ch,eq}}{2L_r}\right)^2-\dfrac{2}{L_rC_{ch,eq}}} \\ A_1=\dfrac{s_2}{s_1+s_2}\Delta V_{C,1} \\ A_2=\dfrac{s_1}{s_1+s_2}\Delta V_{C,2} \end{cases} \tag{4b}$$

Concerning the relation compiled in (3) and (4a), the maximum charging current of the involved capacitors can be alleviated by the QSC cell by operating either in under-damp or in over-damped region. Therefore, instead of having an extremely huge inrush current caused by the parallel connection of the capacitors to the dc-source, the charging current experiences an exponential behavior over each switching frequency, and its maximum value can be limited to a permissible value by the help of QSC cell parameters like L_r or $R_{ch,eq}$. Regarding the working principles of the proposed topology shown in Fig. 3, only four out of eight switches per phase (S_{X2}, S_{X3}, S_{X5}, S_{X6}) are in charging path of the capacitors. Therefore, the current stresses of these switches are affected by the maximum charging current of the capacitors. Also, the current stresses of the rest of power switches are confined within the load/grid current shape since they are out of charging path of the capacitors.

On the other hand, to determine a suitable value for the capacitance of the involved capacitors (C_1 and C_2), their maximum discharging time interval and the voltage difference across them (ΔV_{C1}&ΔV_{C2}) are of importance. Considering the longest discharging time interval of the capacitors (α,β), the following equation can be expressed:

$$\frac{1}{C_i}\int_{\alpha}^{\beta} i_{Ci}(t)\,\mathrm{dt}=\Delta V_{Ci}\quad i=1,2 \tag{5a}$$

where, $i_{Ci}(t)$ is the passing current through the capacitors. To determine the value of $i_{Ci}(t)$ and (α,β) for each of the involved capacitors, the duty cycle and the status of the involved capacitors in each of the switching states must be identified. Considering $d(t)=\mathrm{D}_{\max}Sin(\omega\mathrm{t})$ as the steady-state duty cycle of the output voltage of the proposed inverter, the dwell time for each of the switching states named as A, B, C, and D in Fig. 3 and the capacitors status (charge or discharge in unity power factor condition) are summarized in Table IV. Here, $\mathrm{D}_{\max}$ is referred as the maximum modulation index of the proposed SC-based seven-level inverter. Details of respective duty cycle calculation during different switching states for a multilevel-based inverter can be found in [41-42].

Regarding Table IV, it can be discerned that the longest discharging time interval for C_2 occurs when the top output voltage levels in switching states of C and D are generated, while this longest switching time interval for C_1 is in the switching state of "D" only. Hence, considering $i_g(t)$ as the output current of the inverter per phase, which possess a sinusoidal trend with a function of $i_g(t)=I_mSin(\omega t)$, the value of $i_{Ci}(t)$ for C_2 and C_1 within their longest discharging time interval can be found as follows:

$$i_{C2}(t)=i_g(t)\rightarrow t_x\le\omega t\le\frac{T}{4}+t_x \tag{5b}$$

$$i_{C1}(t)=(3d(t)-2)i_g(t)\rightarrow State\,D \tag{5c}$$

where t_x is the transition time once the output voltage of the proposed inverter is switched from the middle region (switching states of B and C) to the top region (switching states of C and D). Hence, following expression can be written [41]:

$$t_x=\frac{1}{\omega}\sin^{-1}\left(\frac{2}{3D_{\max}}\right) \tag{5d}$$

where, ω is the angular term at the grid fundamental frequency. Concerning (5b), and (5a), the required capacitance for C_2 can be obtained as:

$$C_2=\frac{I_m}{\omega\Delta V_{C2}}\left[\frac{2}{3D_{\max}}+Cos\left(Sin^{-1}\left(\frac{2}{3D_{\max}}\right)\right)\right] \tag{6a}$$

where, I_m is the maximum value of the injected grid current.

On the other hand, C_1 is charged/discharged regularly within the switching states of C/D. Hence its maximum discharging time interval is related to the switching frequency. Considering (5c) and (5a), the capacitance required for C_1 would be

relatively small compare to C_2), and by neglecting the sinusoidal terms of the resultant integral, its relation can be expressed as:

$$C_1 \approx \frac{3I_m D_{\max}}{2 f_{Sw} \Delta V_{C1}} + \frac{2I_m}{\omega} \tag{6b}$$

Regarding (6a) and (6b), it can be discerned that C_1 can possess much smaller value than C_2.

IV. Control Scheme

For the proposed three-phase SC-based seven-level inverter illustrated in Fig. 2, we propose the discrete switching states in the $\alpha\beta$ plane as shown in Fig. 7. Herein, it is assumed that the circuit is supplied by an input dc voltage source set at V_{DC}. Also, it has been considered that the proposed seven-level inverter is connected to the grid via an L-type filter with inductance value of L and an equivalent series resistance of r. Based on different switching combinations, one phase-leg in the proposed topology can offer four switching states: 'A' state, 'B' state, 'C' state, and 'D' state as described earlier.

In the two-phase stationary $\alpha\beta$ orthogonal coordinate system, the voltage and current vectors can be described by (7) and (8), respectively:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \tag{7}$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{8}$$

The switching states of the converter can be described in the $\alpha\beta$ frame as follows:

$$\vec{S}_{\alpha\beta} = \begin{bmatrix} s_\alpha \\ s_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \tag{9}$$

Then, the output voltage space vector of the inverter can be expressed as

$$\vec{v}_{con.} = \frac{2}{3}\left(v_{ao} + \vec{\omega} v_{bo} + \vec{\omega}^2 v_{co}\right) \tag{10}$$

where $\vec{\omega} = e^{j2\pi/3} = -1/2 + j\frac{\sqrt{3}}{2}$ is a unit vector that denotes the 120° phase shift between any two of the three phases.

According to the switching matrix, the dynamic model of the inverter output voltage can be expressed with respect to the dc-link voltage as

$$\vec{V}_{\alpha\beta} = \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \vec{S} V_{DC} \tag{11}$$

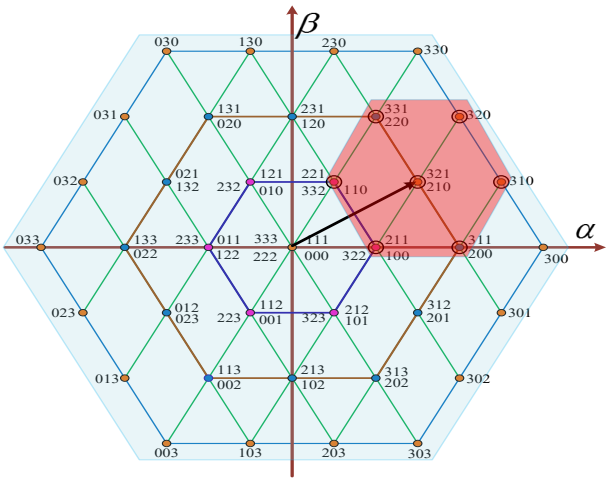


Fig. 7. Voltage vectors and switching states of the proposed three-phase seven-level inverter.

Considering the switching combinations of a seven-level inverter, 4^3=64 voltage vectors can be generated from the 64 consequence switching states. Due to the redundancy of some voltage vectors that generate identical voltage vectors, only 37 space vectors are available for the finite-control set (FCS) control of the proposed three-phase seven-level inverter, as illustrated in Fig. 7.

The mathematical model of the three-phase inverter in the *abc* reference frame can be then written as

$$\frac{d}{dt}\begin{bmatrix} i_{ga}(t) \\ i_{gb}(t) \\ i_{gc}(t) \end{bmatrix} = \begin{bmatrix} \frac{1}{L} & 0 & 0 \\ 0 & \frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} v_{ga}(t) \\ v_{gb}(t) \\ v_{gc}(t) \end{bmatrix} - \begin{bmatrix} \frac{R}{L} & 0 & 0 \\ 0 & \frac{R}{L} & 0 \\ 0 & 0 & \frac{R}{L} \end{bmatrix} \begin{bmatrix} i_{ga}(t) \\ i_{gb}(t) \\ i_{gc}(t) \end{bmatrix} \tag{12}$$

where v_{ga}(t), v_{gb}(t), and v_{gc}(t) are the grid voltages, and i_a(t), i_b(t), and i_c(t) the output currents of phases *a*, *b*, and *c*, respectively.

To apply FCS-MPC to the proposed inverter, the discrete time predictive model of (12) can be obtained using the forward Euler's approximation method as the following:

$$\begin{bmatrix} i_{ga}^{k+1} \\ i_{gb}^{k+1} \\ i_{gc}^{k+1} \end{bmatrix} = \begin{bmatrix} 1-\frac{RT_s}{L} & 0 & 0 \\ 0 & 1-\frac{RT_s}{L} & 0 \\ 0 & 0 & 1-\frac{RT_s}{L} \end{bmatrix} \begin{bmatrix} i_{ga}^{k} \\ i_{gb}^{k} \\ i_{gc}^{k} \end{bmatrix} - \begin{bmatrix} \frac{T_s}{L} & 0 & 0 \\ 0 & \frac{T_s}{L} & 0 \\ 0 & 0 & \frac{T_s}{L} \end{bmatrix} \begin{bmatrix} v_{ga}^{k} \\ v_{gb}^{k} \\ v_{gc}^{k} \end{bmatrix} \tag{13}$$

where, T_s is the sampling time of the controller. Since the main objective of the controller is to track the reference current, the cost function can be defined as the difference between the predicted and reference values of the system variables.

The current dynamics of the inverter can be represented in the α-β orthogonal coordinates as

$$\frac{d\vec{i}_{g,\alpha\beta}}{dt} = -\frac{R_s}{L_f}\vec{i}_{g,\alpha\beta} + \frac{1}{L_f}\vec{v}_{\alpha\beta} - \frac{1}{L_f}\vec{v}_{g,\alpha\beta} \tag{14}$$

where $\boldsymbol{v_{g,\alpha\beta}}$ and $\boldsymbol{i_{g,\alpha\beta}}$ are the grid voltage and current vectors, respectively.

The discrete time model of the grid current at the $(k+1)^{th}$ instant for a sample time T_S can also be expressed as

$$\vec{i}_{g,\alpha\beta}^{\,k+1} = \frac{1}{R_s T_s + L_f}\left[L_f \vec{i}_{g,\alpha\beta}^{\,k} + T_s\left(\vec{V}_{\alpha\beta}^{\,k} - \vec{V}_{g,\alpha\beta}^{\,k}\right)\right] \quad (15)$$

The active and reactive powers of this system can be then calculated as

$$P = \frac{3}{2}\mathrm{Re}\left(v_g i_g^*\right) = \frac{3}{2}\left(v_{g,\alpha} i_{g,\alpha} + v_{g,\beta} i_{g,\beta}\right) \quad (1)$$

$$Q = \frac{3}{2}\mathrm{Im}\left(v_g i_g^*\right) = \frac{3}{2}\left(v_{g,\beta} i_{g,\alpha} - v_{g,\alpha} i_{g,\beta}\right) \quad (17)$$

At the *(k+1)*th instant, the active and reactive power can be expressed as

$$P_g^{k+1} = \frac{3}{2}\left(v_{g,\alpha}^{k+1} i_{g,\alpha}^{k+1} + v_{g,\beta}^{k+1} i_{g,\beta}^{k+1}\right) \quad (18)$$

$$Q_g^{k+1} = \frac{3}{2}\left(v_{g,\beta}^{k+1} i_{g,\alpha}^{k+1} - v_{g,\alpha}^{k+1} i_{g,\beta}^{k+1}\right) \quad (19)$$

In order to reduce the computational burden of the microprocessor for applying FCS-MPC, it is necessary to reduce the number of vectors in each computation. It is also necessary to reduce the switching frequency to increase efficiency of the converter, especially at high power level. To realize these objectives, the following targets are considered in the formulation of the cost function.

Target 1: Tracking active and reactive power

For the active and reactive power control, the cost function *J* can be defined as

$$J = \left[\left(P_g^{k+1} - P_{ref}\right)^2 + \left(Q_g^{k+1} - Q_{ref}\right)^2\right] \quad (20)$$

where P_{ref} and Q_{ref} are the active and reactive power references, respectively.

The voltage across the capacitors used in the structure is self-balanced. As a result, the formulated cost function does not need to consider the capacitor voltage unbalancing constraint, which reduces the control complexity.

Target 2: Reducing the computational burden

A modified control algorithm is derived to reduce the computational burden. In the modified algorithm, like the conventional two-level inverters, only seven voltage vectors out of 64 available set are required to be considered. A reference voltage vector is then calculated instead of calculating the best voltage vector from the available space vectors (64 voltage vectors for seven-level) for realizing the reference power values. The expression of (15) can be rewritten as follows:

$$\vec{V}_{ref,\alpha\beta}^{\,k} = R_S \vec{i}_{g,\alpha\beta}^{\,k} \frac{L_f}{T_s}\left[\vec{i}_{g,\alpha\beta}^{\,k+1} - \vec{i}_{g,\alpha\beta}^{\,k}\right] \quad (21)$$

The reference voltage $\vec{v}_{ref,\alpha\beta}^{\,k}$ is compared with the available voltage states (64 voltage vectors for seven-level) to identify the closest states to the reference (see Fig. 7 in red marked area). These closest states can be determined using the cost function J_v, given as

$$J_v = \left(V_{ref,\alpha} - v_{j,\alpha}\right)^2 + \left(V_{ref,\beta} - v_{j,\beta}\right)^2 \quad (22)$$

The control algorithm then only evaluates the adjacent vectors to determine the best switching action.

It can be concluded from (20) and (22) that the voltage state that minimizes the calculated *J*, also minimizes the calculated J_v. From (20)-(22), we have

$$J_c = \left[\left(P - P_{ref}\right)^2 + \left(Q - Q_{ref}\right)^2\right]\left(\frac{T_s}{L_f}\right)^2 \quad (23)$$

Target 3: Switching frequency reduction

The effective tracking of the reference active and reactive power can be realized by the cost function defined in (23). The generated current quality can be improved by considering higher sampling frequency, which also increases the switching frequency of the converter, and consequently, it increases switching losses. Thus, it is important to reduce the switching frequency particularly at high power level in order to reduce the switching losses. To reduce the switching frequency of the converter while maintaining the power tracking performance, an optimization function is considered as:

$$f_{sw}^{k+1} = \left|S_a^{k+1} - S_a^k\right| + \left|S_b^{k+1} - S_b^k\right| + \left|S_c^{k+1} - S_c^k\right| \quad (24)$$

where S_X^{k+1} and S_X^k are the two adjacent switching states. Therefore, the objective cost function is formulated by combining (23) and (24), given by

$$J = J_c + \lambda\left(\left|S_a^{k+1} - S_a^k\right| + \left|S_b^{k+1} - S_b^k\right| + \left|S_c^{k+1} - S_c^k\right|\right) \quad (25)$$

where λ is the weighting factor calculated as $\lambda = 2\sqrt{P^2 + Q^2}$.

V. Comparative Summary

Tables V, VI, and VII compare the proposed topology with some existing popular topologies with the same number of voltage levels and a single dc voltage source incorporation. The study evaluates the pros and cons of the proposed topology versus the existing topologies in terms of number of semiconductor devices and capacitors used, the required dc-link voltage for the same output voltage generation, the total blocking voltage by the switches in p.u., and the total voltage across the capacitors in p.u. The study is performed for one phase leg. The proposed seven-level SC-based inverter topology uses eight semiconductor switches, which is the minimum among all the topologies studied in this comparison. In terms of reliability of the converters, the capacitors are the most critical component used in the converter topologies. The number of capacitors and their voltage ratings used in each topology should be minimum to reduce the converter volume and space requirement. As shown in Table VI, the proposed topology requires the minimum number of capacitors. Table VII compares the voltage stress across the components of different topologies. As is clear, the proposed seven-level SC-based inverter needs the smallest numbers of active switches and capacitors and the smallest total voltage stress across the capacitors among all topologies studied. The proposed topology presents enhanced structural merits in terms of the voltage boosting capability. It can reduce the dc-link voltage requirement by 75% compared to the conventional NPC and ANPC with mid-point grounding, and 50% to the hybrid topologies. The total blocking voltage by the semiconductor switches in the proposed topology is significantly lower than those are in the NPC, CHB and some hybrid topologies, which

TABLE V. COMPARISON OF THE PROPOSED TOPOLOGY WITH THE TRADITIONAL TOPOLOGIES (MAX. PHASE VOLTAGE = 400V = 1 $p.u.$)

Parameters	[1, 2]	[11]	[18]	[20]	[21]	[23]	[32]	[18]	[6]	[36]	[43]	[44]	Pro.
No. of active switches	18	12	10	12	14	10	10	14	8	10	9	9	8
Total voltage stress across the switches	6	8	6	8	6.66	5.33	8	8	5	8	8	8	5.5
dc- link voltage required for the same phase voltage	2	2	2	1	1.5	2	2	2	1	0.66	0.66	0.66	0.5

TABLE VI. COMPARISON OF NUMBER OF CAPACITORS USED AND TOTAL VOLTAGE STRESS ACROSS THE CAPACITORS (MAX. PHASE VOLTAGE = 400V =1 $p.u.$)

Parameters	[1, 2]	[11]	[18]	[20]	[21]	[23]	[32]	[18]	[6]	[29]	[36]	[43]	[44]	Pro
No. of capacitors	6	7	4	6	5	4	3	7	4	4	4	3	3	2
Total voltage across the capacitors (p.u.)	2	7	3.33	4	2.66	2.33	2.5	3	3.25	2	2	2.5	2.5	1

TABLE VII. MAXIMUM VOLTAGE STRESS ON THE COMPONENTS OF CONVENTIONAL TOPOLOGIES (MAX. PHASE VOLTAGE = 400 V =1 $p.u.$)

Device	[11]	[18]	[20]	[21]	[23]	[32]	[18]	[6]	[29]	Proposed
S_{X1}	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$
S_{X2}	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$
S_{X3}	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\pm\frac{1}{4}V_{DC}$	$\frac{1}{2}V_{DC}$
S_{X4}	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{3}{8}V_{DC}$	$\frac{1}{2}V_{DC}$
S_{X5}	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{8}V_{DC}$	$\frac{1}{2}V_{DC}$
S_{X6}	$\frac{5}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{8}V_{DC}$	V_{DC}
S_{X7}	$\frac{5}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{4}V_{DC}$	$\frac{3}{8}V_{DC}$	$\frac{1}{2}V_{DC}$
S_{X8}	$\frac{1}{6}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{4}V_{DC}$	$\pm\frac{1}{4}V_{DC}$	$\frac{3}{2}V_{DC}$
S_{X9}	$\frac{1}{6}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{4}V_{DC}$	–	–
S_{X10}	$\frac{1}{6}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{4}V_{DC}$	–	–
S_{X11}	$\frac{1}{6}V_{DC}$	–	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	–	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	–	–	–
S_{X12}	$\frac{1}{2}V_{DC}$	–	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	–	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	–	–	–
S_{X13}	–	–	–	$\frac{1}{6}V_{DC}$	–	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	–	–	–
S_{X14}	–	–	–	$\frac{1}{6}V_{DC}$	–	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	–	–	–
C_1	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{4}V_{DC}$	$\frac{1}{2}V_{DC}$
C_2	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{2}V_{DC}$	$\frac{1}{4}V_{DC}$	$\frac{1}{2}V_{DC}$
C_3	–	–	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	–	$\frac{1}{3}V_{DC}$	–	–	–
C_{f1}	$\frac{1}{6}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$	$\frac{1}{4}V_{DC}$	$\frac{1}{2}V_{DC}$	–
C_{f2}	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	–	$\frac{1}{3}V_{DC}$	$\frac{1}{6}V_{DC}$	–	$\frac{1}{8}V_{DC}$	–
C_{f3}	$\frac{1}{2}V_{DC}$	–	$\frac{1}{3}V_{DC}$	–	–	$\frac{1}{2}V_{DC}$	–	–	–	–
C_{f4}	$\frac{2}{3}V_{DC}$	–	–	–	–	$\frac{1}{3}V_{DC}$	–	–	–	–
C_{f5}	$\frac{5}{6}V_{DC}$	–	–	–	–	$\frac{1}{6}V_{DC}$	–	–	–	–

would result in significant cost saving for the overall system design.

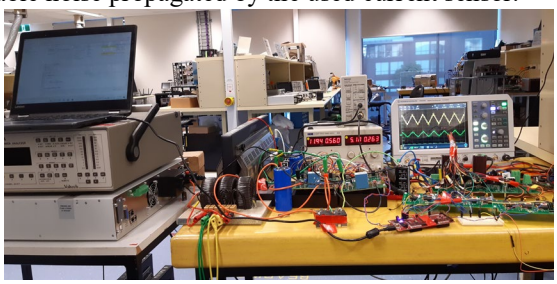
TABLE VIII. CONVERTER SPECIFICATION AND GRID-PARAMETERS

Description	Value/Parameter Used
Input voltage (V_{DC})	200 V
Output voltage (v_{ae})	230 V (RMS)
Max. switching frequency	12.5 kHz
Line frequency (f)	50 Hz
Switched capacitors (C_{X1} & C_{X2})	1.5 mF, 250 V
Filter inductor (L_{fX})	1.5 mH
DSP	TMS320F28379D
Equivalent series resistance (r_X)	0.1 Ω
Switches (Sx_2, Sx_5)	IXRH 40N120
Switches (S_{X1}, S_{X3}, S_{X4}, S_{X6}- S_8)	SCT3022AL

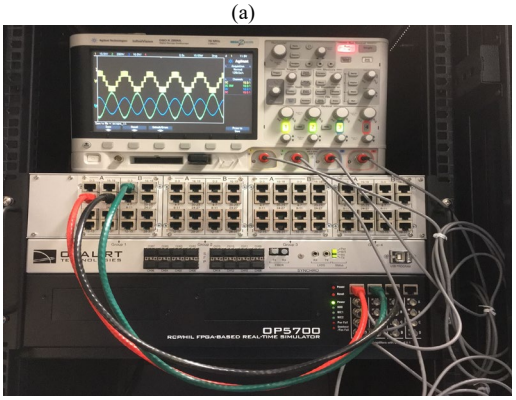
VI. PERFORMANCE EVALUATION

The model of the proposed multilevel inverter concept is validated through both the experimental fabricated setup and the real time OPAL-RT-based environment. TABLE VIII lists the specifications of the converter, while a picture of the built prototype and the implemented OPAL-RT setup have been depicted in Figs. 7 (a) and (b). Herein, a PV emulator with the part number of EA-PSI-9750-12 as an adjustable dc laboratory power supply has also been utilized to feed the proposed SC-based MLI. The input dc source value is set at 110 V, which results in 330 V peak of seven-level output voltage of the proposed inverter per each phase. To generate the required gate signals based on Fig. 4 and the proposed control scheme, a

Texas-Instrument (TI) controller with the part number of F28379D has been utilized. Also, to implement the proposed control scheme, a Hall-effect based linear current sensor (ACS 712) associated with a simple voltage divider sensors are used. The obtained experimental results of the proposed inverter output voltage, load current and the balanced voltage of two involved capacitors per each phase can be seen in Fig. 8 (a). Herein, to sluggish the current stress profile of the involved power switches, a very small inductor with a value of 33µH has been utilized as an input QSC-filter. As can be seen both the involved capacitors are balanced at 110 V which is equal to the input dc supply voltage, while the peak of load current is around 2.5 A. Regarding 330 V as the peak of seven-level output voltage of the proposed inverter per phase, the converter can successfully inject 350 W active power. The visible spikes of the output voltage of the inverter can be attributed to the available noise propagated by the used current sensor.

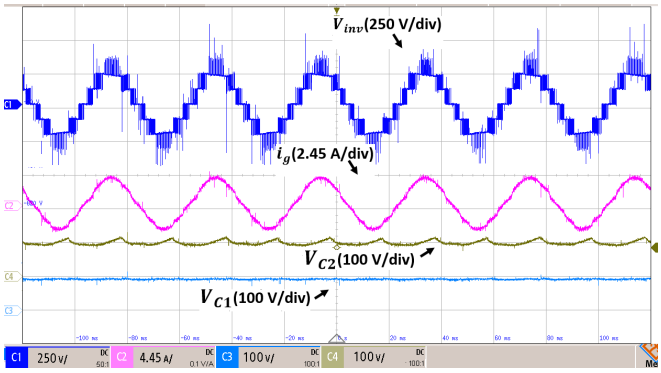


(a)

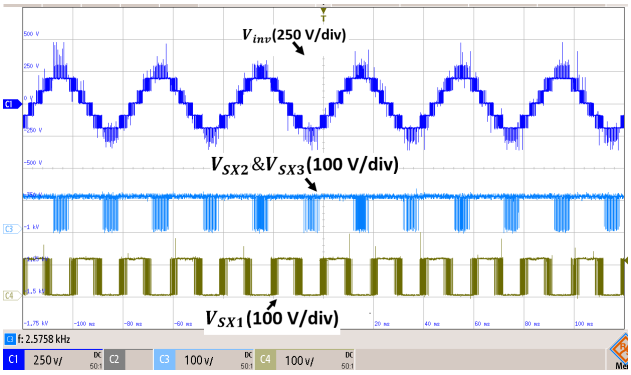


(b)

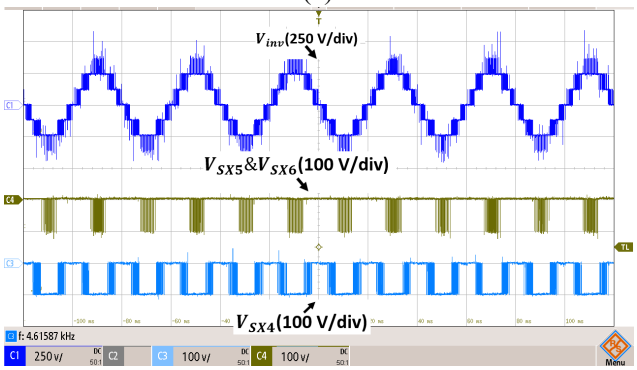
Fig. 7. (a) A picture of built prototype, (b) real time measurement setup of the proposed system by OPAL-RT.



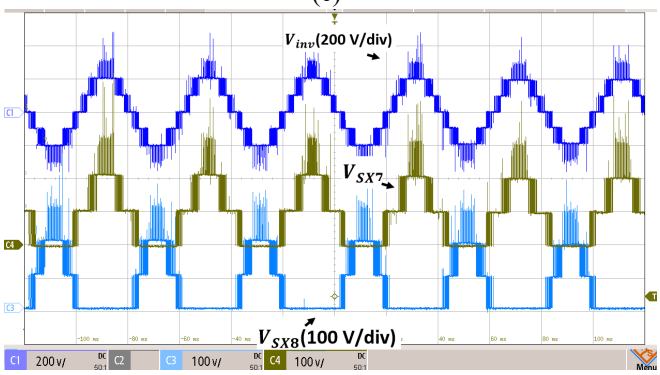
(a)



(b)



(c)



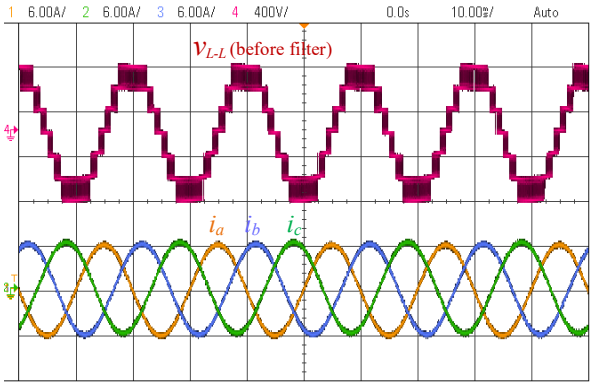
(d)

Fig. 8. Experimental results: (a) the inverter output voltage, the load current and the capacitors voltage (b) the inverter output voltage and the voltage stress across S_{X2}& S_{X3} and S_{X1} (c) the inverter output voltage and the voltage stress across S_{X5}& S_{X6} and S_{X4}, (d) the inverter output voltage and the voltage stress across S_{X7} and S_{X8}.

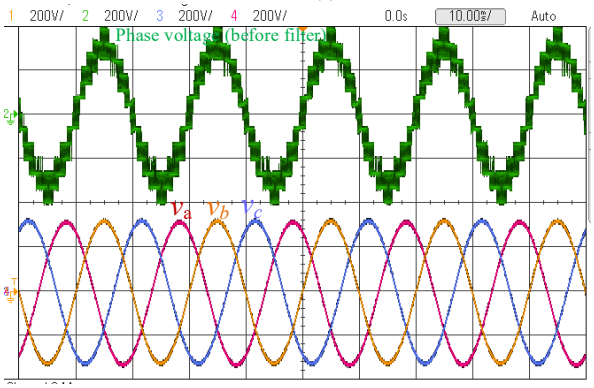
The seven-level inverter output voltage and the drain-source voltage across all the power switches have also been capture by the experiment and shown in Fig. 8 (b)-(d). As can be confirmed from these results, the voltage stresses of the involved power switches conform the mentioned relation compiled in TABLE IV.

In the following, through the help of OPAL RT with the capability of hardware-in-the-loop implementation, the line-to-line voltage (before filter) and the grid current waveforms under the unity power factor operation have been shown in Fig. 9 (a). The phase voltage (before filter) and the grid voltage waveforms of the proposed inverter are also shown in Fig. 9 (b). As can be reconfirmed, the proposed topology can generate sinusoidal output current and clean seven-level (line-line) output voltage.

Fig. 10 also shows the obtained results for operation modes of unity, lagging, and leading power factors. As can be seen, the proposed inverter can generate clean sinusoidal current and seven-level voltage even in the negative power region. Here, the reference power is changed from 1000 W to 1500 W to analyse the transient performance of the predictive controller. The results obtained during this transient operation are shown in Fig. 11. As can be realized, the converter current changes instantly to realize the reference power value, and a distinct seven-level voltage is also observed during this transient.

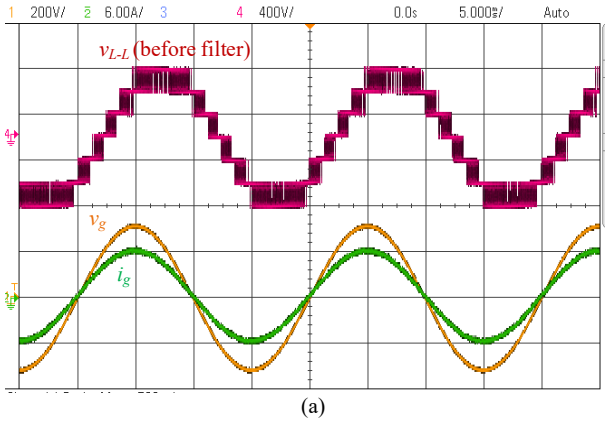


(a)

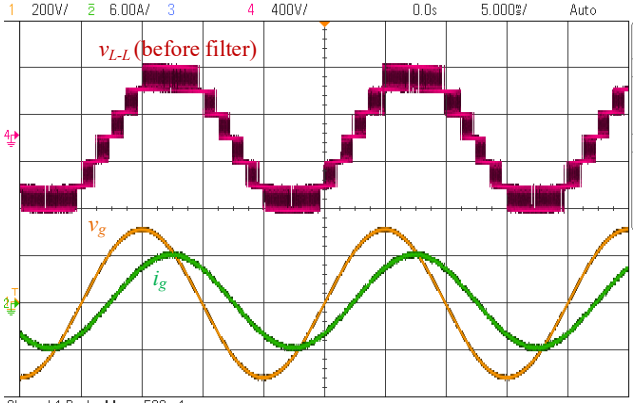


(b)

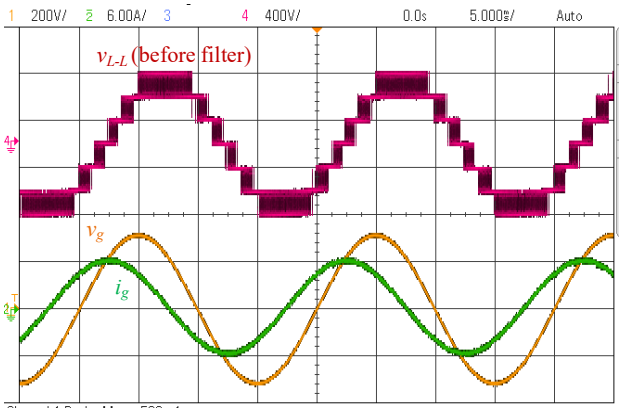
Fig. 9. The measurement results (a) line voltage and grid current waveforms, (b) the phase voltage before filter and the grid voltage waveforms.



(a)



(b)



(c)

Fig. 10. Grid voltage and current waveforms with different power factor, (a) unity power factor, (b) lagging power factor, and (c) leading power factor.

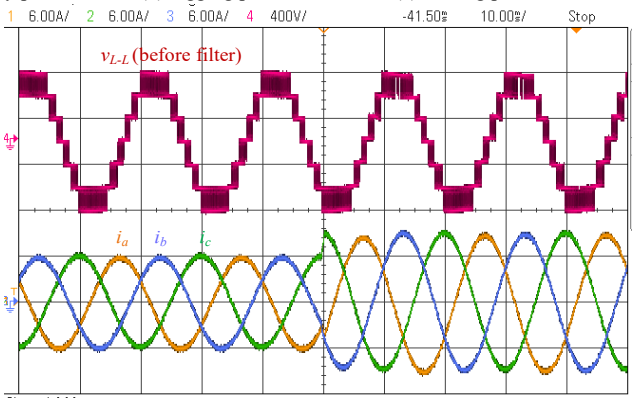


Fig. 11. Line to line voltage and current waveforms under transient condition (step change in load from 1 kW to 1.5 kW).

VII. Conclusion

A new three-phase switched-capacitor based multilevel inverter topology is proposed in this paper. The proposed topology has been comprised of minimal switching devices to realize the three-phase system. Voltage step-up feature, self-voltage balancing of the capacitors without requiring additional sensors and the capability of generalization are three main features of the proposed topology. The voltage stress across the capacitors and switches of the proposed topology is the minimum compared to the traditional topologies. The seven-level variant of the proposed topology can reduce the dc supply voltage requirement by 75% compared to the existing NPC, ANPC, and CHB topologies, and by 50% to the hybrid

topologies. This feature can eliminate the multi-stage dc-dc power conversion system of the grid-connected PV system. To control the converter, a finite control set model predictive control algorithm is derived with a cost function formulated to operate at any specified power factor. The inherent self-balanced capacitor voltage can reduce significantly the control complexity and the requirement of additional sensor circuit. The novel concept of the proposed topology and the associated control scheme have been validated by both the experimental results and the real-time measurement tests in the OPAL-RT based environment.

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