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ORIGINAL RESEARCH PAPER

Generalized diamond-type single DC-source switched-capacitor based multilevel inverter with step-up and natural voltage balancing capabilities

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Abstract

This paper proposes a diamond-shaped high step-up switched-capacitor based basic multilevel inverter topology. The basic switched-capacitor (SC) stage consists of 2 active switches, 2 diodes, and 2 capacitors. Using a single DC source with the unfolding circuit (10 switches, 5 capacitors, and 5 diodes) results in the production of 17 voltage-steps at the output with the gain of up to 8 times of the input voltage. By extending the diamond-shaped switched-capacitor stages, higher voltage levels and voltage gains can be possible. The suggested topology employs two half-bridges (instead of a full-bridge) to produce positive, zero, and negative steps, which reduces the Voltage Stress (VS) on two output switches and consequently reduces Total Voltage Stress (TVS). In addition, the natural voltage balancing of capacitors eliminates the need to an additional control circuitry and consequently reduces the total converter size, complexity, and cost. In addition, modularity, scalability, low voltage ripple on capacitors, low total voltage stress, high power quality, and capability of supplying low/medium power factor (R-L) loads are some of the merits of the proposed topology. The low Cost Function (CF) obtained in the comparison section as well as experimental results verifies the advantages of the proposed topology.

1 | INTRODUCTION

In recent years, multilevel inverters have gained tremendous attention among power electronic converters due to their outstanding features such as: simple structure, suitability for medium/high voltage/power applications, low electromagnetic interference, low total harmonic distortion (THD), and improved power quality [1–3]. The DC supplies as well as switches and diodes are included devices of multilevel inverters. But numerous devices are demanded for reaching increased steps. In literature, many structures have been presented profiting from the reduced number of devices [4–6]. The reduction in semiconductor device count leads to reduced gate-driver circuits and reduced overall size and cost [7]. Usually, the DC sources are bulkier, heavier, and more expensive than other parts in multilevel inverters. So, most of the papers have focused on presenting structures with less number of DC supplies [8]. The capacitors are good candidates for replacing DC sources, which results in the introduction of capacitor-based multilevel inverters (or called "Switched-Capacitor Based Multi-Level Inverters (SCBMLIs)") [9–24]. In SCBMLIs, DC source(s) and pre-charged capacitor(s) are synthesized to produce staircase voltage waveform.

In [9–11], the application of capacitors has only decreased the number of sources (unity gain). But in [12–24], the enhanced gain has also been reported besides reduced source count. The charge balancing of capacitors is the main challenge of SCBMLIs [25]. The topology presented in [26] requires additional auxiliary control circuits for charge balancing of the capacitor, which increases the total cost and size of the converter. But, in [9–24], the charge balancing of capacitors is done naturally (without auxiliary circuits) leading to less complexity and simple control.

The topologies presented in [9, 11, 13–19, 21, 23, 24, 27] are modular and can be extended by increment of switched-capacitor stages, where the non-modular structures presented in

[10, 12, 20, 22] can only be extended by cascading the basic units. This increases the number of sources/devices, weight, cost, and volume of the converter. The extension of [14–19, 23, 24, 27] increases the number of steps and voltage gain, but in [9–13, 20, 22] the voltage gain remains constant.

The SCBMLIs presented in [9, 28–30] employ an H-bridge unit to provide negative steps, which imposes maximum voltage stress ($= V_{o,max}$) and consequently high losses on H-bridge switches. To overcome this shortcoming, two half-bridges [11–15, 22–24, 27] or a developed H-bridge [10, 16–19] can be applied (instead of H-bridge) to create negative steps, where only two switches (instead of 4 switches) are imposed to maximum voltage stress. The creation of AC voltage waveform can be free of H-bridge, developed H-bridge or half-bridges. For example, the bipolar output voltage waveform generation of [21] is accomplished inherently, which reduces the total voltage stress. The SCBMLIs presented in [19–24] have been investigated in detail, in the comparison section.

Another important feature in SCBMLIs is the quality of output voltage waveform. Higher number of steps leads to higher quality and lower THDs. However, this objective can be obtained in expense of increased devices, cost, weight, and volume. So, there should be a trade-off between number of devices (cost) and number of steps. While the cost factor is dominant, a linear relationship is preferred between number of levels and devices [20–24]. But if quality factor is the main objective, an exponential relation between number of steps and devices is aimed [19], where large number of steps and accordingly high quality and low THD can be achieved.

This paper suggests a modular developed diamond-type single-source SCBMLI configuration that benefits from increased levels per device. Application of 2 half-bridges (for creating negative steps) has reduced the total voltage stress. The suggested topology is extended by adding switched-capacitor stages to reach more steps and higher voltage gains. Also, the suggested structure can properly supply the *R-L* loads. In Sections 2 and 3, the proposed basic and generalized topologies have been introduced. Then, the modulation technique as well as losses analysis and design procedure of capacitors have been explained in Sections 4 and 5. The comparative analysis is also presented in Section 6. The experimental results and conclusions have been presented in Sections 7 and 8, respectively.

2 | PROPOSED DEVELOPED 17-LEVEL TOPOLOGY

The proposed 17-level configuration (shown in Figure 1) is consisted of a single DC-source, 10 switches, 5 capacitors, and 5 diodes. All the switches are unidirectional. So, the count of switches (N_{Switch}), MOSFETs (N_{MOSFET}), and gate-driver circuits (N_{Driver}) are the same. Thus,

$$N_{Source} = 1, N_{Switch} = N_{MOSFET} = N_{Driver} = 10$$
$$N_{Capacitor} = 5, N_{Diode} = 5, N_{Device} = 31 \quad (1)$$

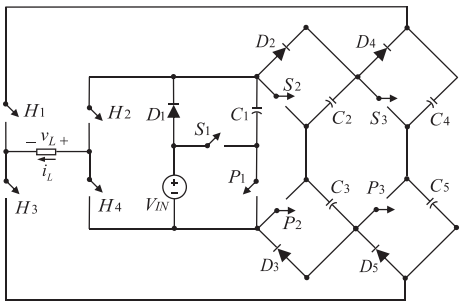

FIGURE 1 Proposed 17-level inverter topology

TABLE 1 Switching pattern and charge/discharge process of capacitors in proposed 17-level topology

V_o	$S_1S_2S_3P_1P_2P_3$ $H_1H_2H_3H_4$	$D_1D_2D_3$ D_4D_5	$C_1C_2C_3$ C_4C_5
$+8V_{IN}$	1000110110	01010	↓↑↓↑↓
$+7V_{IN}$	0001110110	10010	↑↓↓↑↓
$+6V_{IN}$	1100010110	00110	↓↓↑↑↓
$+5V_{IN}$	0101010011	10010	↑↓↓↑↓
$+4V_{IN}$	1010100110	01001	↓↑↓→↑
$+3V_{IN}$	0011100110	10001	↑↓↓→↑
$+2V_{IN}$	1110000110	00101	↓↓↑→↑
$+1V_{IN}$	0111000011	10001	↑↓↓→↑
0 ($I_o > 0$)	1110000011	00101	↓↓↑→↑
0 ($I_o < 0$)	1000111100	01010	↓↑↓↑→
$-1V_{IN}$	0001111100	10010	↑↓↓↑→
$-2V_{IN}$	1000111001	01010	↓↑↓↑→
$-3V_{IN}$	0101011001	10010	↑↓↓↑→
$-4V_{IN}$	1100011001	00110	↓↓↑↑→
$-5V_{IN}$	0011101100	10001	↑↓↓↓↑
$-6V_{IN}$	1010101001	01001	↓↑↓↓↑
$-7V_{IN}$	0111001001	10001	↑↓↓↓↑
$-8V_{IN}$	1110001001	00101	↓↓↑↓↑

Table 1 describes the switching states and charge/discharge process of capacitors in the proposed configuration. Due to the symmetric characteristic of the proposed structure, the H_1, H_2, and S_1-S_3 are switched in complementary manner with H_3, H_4, and P_1-P_3, respectively.

Figure 2 displays the charging path of C_1-C_5 capacitors of proposed topology. As seen in Figure 2, the C_1 is charged by input voltage source, through P_1 and D_1. This process happens in 8 modes of each cycle, during the generation of $\pm V_{IN}$, $\pm 3V_{IN}$, $\pm 5V_{IN}$ and $\pm 7V_{IN}$ voltage levels. This guarantees the voltage balancing of C_1 to V_{IN} ($V_{C1} = V_{IN}$). The C_2 capacitor is paralleled with series connection of V_{IN} and C_1, through S_1, P_2 and D_2. So, the C_2 is charged to $V_{C2} = V_{IN} + V_{C1} = 2V_{IN}$. The charging of C_2 occurs during 5 intervals at each cycle, while generation of zero ($I_o < 0$), $+4V_{IN}$, $+8V_{IN}$, $-2V_{IN}$ and $-6V_{IN}$ voltage levels (Table 1). Similarly, the C_3 is paralleled with series

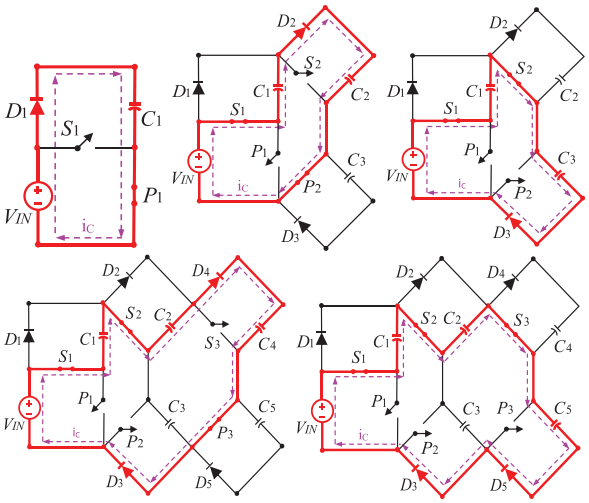

FIGURE 2 The charging path of C_1–C_5 capacitors

connection of V_{IN} and C_1, through S_1, S_2 and D_3. Accordingly, the C_3 is charged to $V_{C3} = V_{IN} + V_{C1} = 2V_{IN}$. The charging of C_3 occurs in 5 intervals at each cycle, while generation of zero ($I_o \geq 0$), $+2V_{IN}$, $+6V_{IN}$, $-4V_{IN}$ and $-8V_{IN}$ output voltage levels (Table 1). Based on Figure 2, the C_4 is paralleled with series connection of V_{IN}, C_1 and C_2, through S_1, S_2, P_3, D_3 and D_4. So, the C_4 is charged to $V_{C4} = V_{IN} + V_{C1} + V_{C2} = 4V_{IN}$. The process takes place during 9 modes (at zero ($I_o < 0$), $+5V_{IN}$, $+6V_{IN}$, $+7V_{IN}$, $+8V_{IN}$, $-1V_{IN}$, $-2V_{IN}$, $-3V_{IN}$ and $-4V_{IN}$ voltage levels) at each switching cycle. Similarly, the C_5 is paralleled with series connection of V_{IN}, C_1 and C_2, through S_1, S_2, S_3, D_3 and D_5. So, it is charged to $V_{C5} = V_{IN} + V_{C1} + V_{C2} = 4V_{IN}$. The charging process of C_5 happens in 9 operational modes (while generation of zero ($I_o \geq 0$), $+1V_{IN}$, $+2V_{IN}$, $+3V_{IN}$, $+4V_{IN}$, $-5V_{IN}$, $-6V_{IN}$, $-7V_{IN}$ and $-8V_{IN}$ voltage levels). Due to numerous charging modes of C_1-C_5 capacitors, the voltage of capacitors is naturally balanced on desired values presented in Equation (2), during initial cycles. Then, the proposed topology reaches to its steady-state operation.

$$V_{C_1} = V_{IN}, V_{C_2} = V_{C_3} = 2V_{IN}, V_{C_4} = V_{C_5} = 4V_{IN} \quad (2)$$

Figure 3 shows equivalent circuits of the proposed converter during the generation of different voltage steps. It is evident from Figure 3 that the proposed topology can simultaneously produce the output voltage level and balance the charge of capacitors at desired values, which is called "natural voltage balancing".

The voltage stress and Normalized Voltage Stress (*NVS*) on semiconductors are shown in Table 2. Note that the *NVS* is defined as voltage stress on semiconductor divided by maximum output voltage: $NVS = (VS/V_{o,max})$. The suggested basic topology applies two half-bridges instead of a full-bridge, which keeps the switch count the same, but decreases the voltage stress on H_2 and H_4 switches to quarter. Accordingly, the losses and expense of H_2, H_4 as well as total voltage stress of the converter are reduced. Only H_1, and H_3 withstand $V_{o,max}$. As seen

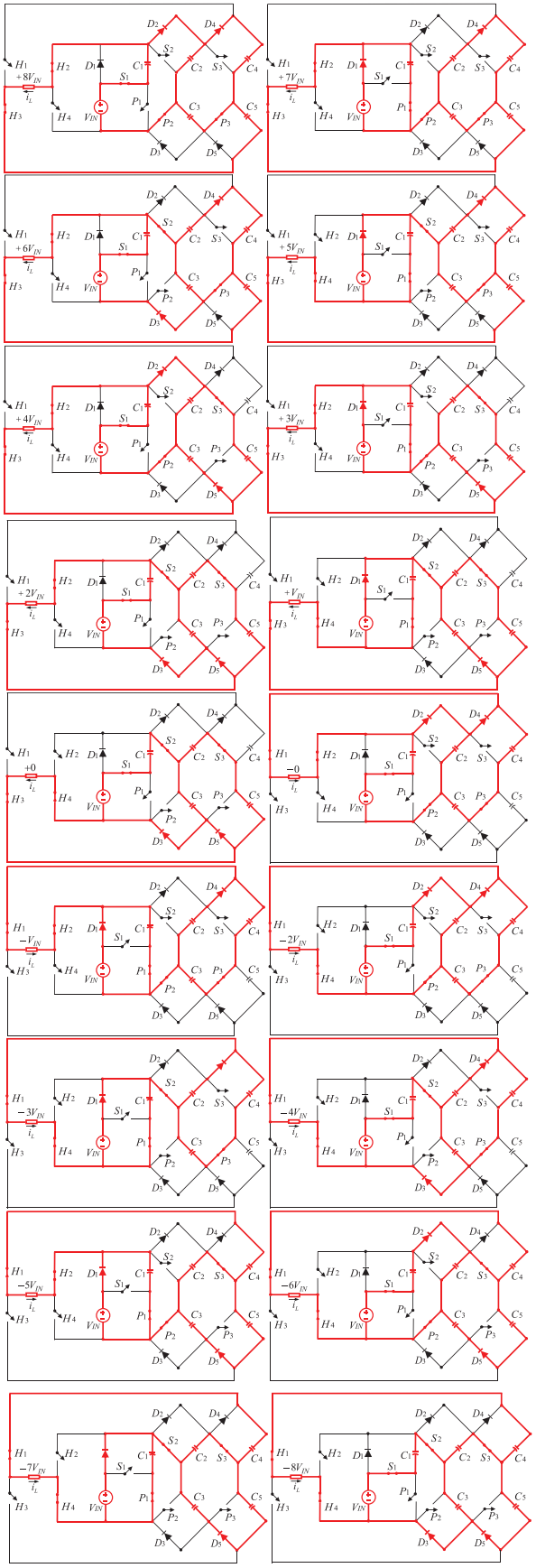

FIGURE 3 Operational modes of proposed 17-level converter

TABLE 2 Voltage stress (VS) on switches/diodes of proposed 17-level topology

Switch	*VS*	*NVS* [%]	Switch	*VS*	*NVS* [%]	Diode	*VS*	*NVS* [%]
S_1	V_{IN}	12.5	P_1	V_{IN}	12.5	D_1	V_{IN}	12.5
S_2	$2V_{IN}$	25	P_2	$2V_{IN}$	25	D_2	$2V_{IN}$	25
S_3	$4V_{IN}$	50	P_3	$4V_{IN}$	50	D_3	$2V_{IN}$	25
H_1	$8V_{IN}$	100	H_3	$8V_{IN}$	100	D_4	$4V_{IN}$	50
H_2	$2V_{IN}$	25	H_4	$2V_{IN}$	25	D_5	$4V_{IN}$	50

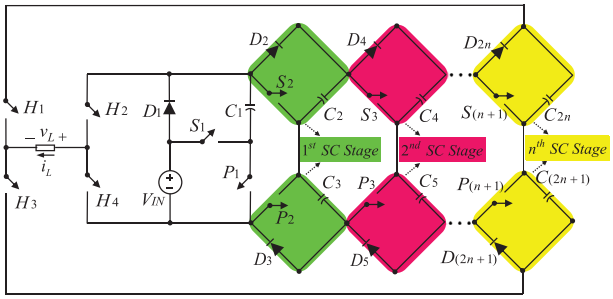

FIGURE 4 Proposed extended topology

from Equation (3), the Normalized Total Voltage Stress (*NTVS*) of proposed topology is an acceptable amount of 5.875. The NTVS is equal to the sum of semiconductors' voltage stress divided by peak output voltage, as in Equation (3).

$$NTVS = \frac{\sum_{i=1}^{3} VS_{S_i} + \sum_{i=1}^{3} VS_{P_i} + \sum_{i=1}^{5} VS_{D_i} + \sum_{i=1}^{4} VS_{H_i}}{V_{o,\max}} = \frac{47\ V_{IN}}{8\ V_{IN}} = 5.875 \quad (3)$$

3 | PROPOSED GENERALIZED TOPOLOGY

The proposed basic topology can be extended by increasing switched-capacitor stages to obtain more voltage gains and output steps, as shown in Figure 4. Each switched-capacitor stage contains 2 unidirectional switches (MOSFETs), 2 capacitors, and 2 diodes. The addition of each switched-capacitor stage doubles positive and negative steps, which improves the output voltage quality and reduces the THD of the suggested topology. Then, the filter can be eliminated or downsized. Also, the voltage gain is doubled by increment of each switched-capacitor stage.

The number of steps and devices, as well as gain of generalized configuration, have been summarized in Table 3, where '*n*' denotes the number of switched-capacitor stages.

TABLE 3 Description of proposed generalized topology

Parameter	Value	Parameter	Value
N_{Level}	$2^{(n+2)}+1$	$N_{Capacitor}$	$2n+1$
$N_{Switch} = N_{MOSFET}$	$2n+6$	N_{Diode}	$2n+1$
N_{Driver}	$2n+6$	N_{Device}	$8n+15$
N_{Source}	1	*Gain*	$2^{(n+1)}$

4 | SWITCHING TECHNIQUE

In this study, the "Nearest Level" (or named as "fundamental frequency") technique has been employed as modulation strategy. In this technique, a sinusoidal waveform with fundamental frequency of 50 Hz is considered as the reference waveform ($V_{Ref} = V_m \sin(\omega t)$). The magnitude of reference waveform can be selected through $0 \le V_m \le N_P = (N_{Level} - 1)/2$, where N_P denotes the total number of positive levels. To guarantee maximum number of levels, the V_m should be selected as close as possible to N_P. In proposed 17-level topology, the N_P is equal to 8. Therefore, the reference waveform is defined as in Equation (4):

$$V_{Ref} = 8\ \sin(2\pi \times 50t) = 8\sin(100\pi t) \quad (4)$$

In nearest level modulation technique, the reference waveform is compared with producible voltage levels (0, $\pm V_{IN}$, $\pm 2V_{IN}$,..., $\pm 8V_{IN}$). At each instant (t), the difference between producible voltage levels and reference waveform (called "*error*") is monitored. The nearest level to the reference waveform is specified by checking relevant error values. The level that has an error less than 0.5 is the nearest one to the reference waveform. So, it is produced at the output port. While the difference between reference waveform and produced level is less than 0.5, the switching pattern remains unchanged. But, when the error reaches its peak value ($error_{max} = 0.5$), the switching pattern is changed to produce the next step, as shown in Figure 5 [20].

The step-changing instant of ith voltage level (t_i) can be calculated from Equation (5). Note that Equation (5) presents the step-changing times of first quarter of switching cycle. The step-changing instants of 2nd, 3rd and 4th quarters can also be calculated based on symmetric nature of output voltage waveform. As seen from Table 4, the employment of nearest level technique reduces the operating frequency of semiconductors, which leads to suppressed switching losses. The simplicity as well as ease of implementation of nearest level technique has increased its popularity.

$$t_i = \frac{1}{\omega} \arcsin\left(\frac{(i - 0.5) \times V_{IN}}{V_m}\right) \qquad i = 1, 2, \ldots, N_P \quad (5)$$

To certify low-frequency operation of switches in nearest level technique, the total ON-OFF transitions of switches during each switching cycle have been presented in Table 4. It is

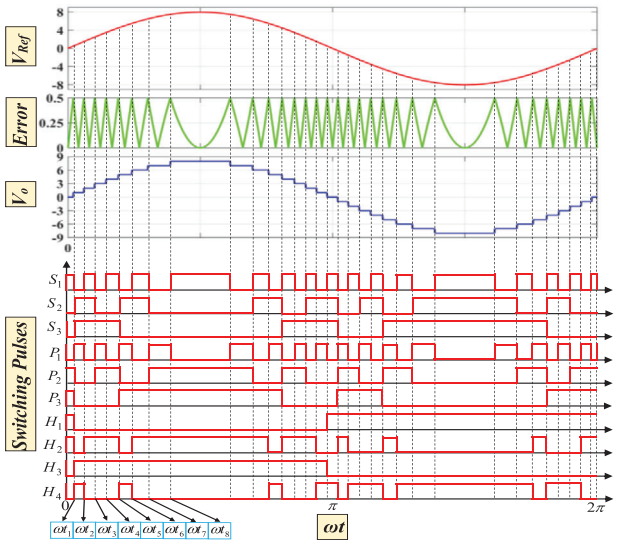

FIGURE 5 Nearest-level based switching pattern of suggested 17-level topology

TABLE 4 ON/OFF transitions of switches at each switching period and estimated operating frequency of switches

Switch	Number of ON/OFF	Frequency [Hz]	Switch	Number of ON/OFF	Frequency [Hz]
S_1	16	800	P_1	16	800
S_2	7	350	P_2	7	350
S_3	3	150	P_3	3	150
H_1	1	50	H_3	1	50
H_2	7	350	H_4	7	350

noted that the H_1 and H_3 switches operate at fundamental frequency, while the other semiconductors operate at quite low switching frequencies. This leads to reduced switching losses.

5 | LOSSES ANALYSIS AND DESIGN OF CAPACITORS

5.1 | Losses analysis

The losses occurred in switched-capacitor multilevel inverters can be classified to three main types, which are elaborated in the following.

5.1.1 | Conduction losses

The conduction losses usually happen at on-state resistance of switches and diodes (R_{on}), forward voltage drop of diodes (V_{FD}) and equivalent series resistance of capacitors (R_{ESR}). Total conduction losses of the structure can be achieved from (6), where the I_{rms} and I_{ave} denotes the Root Mean Square (RMS) and average values of components' current, respectively [24].

$$P_{Loss,\,Cond} = P_{Cond,\,Switches} + P_{Cond,\,Diodes} + P_{Cond,\,Capacitors} = \\ = R_{on}^{Switch} I_{rms,\,Switch}^2 + \left(R_{on}^{Diode} I_{rms,\,Diode}^2 + V_{FD} I_{ave,\,Diode}\right) \\ + R_{ESR} \times I_{rms,\,Capacitor}^2 \tag{6}$$

5.1.2 | Switching losses

The switching losses happen during ON-OFF transitions of semiconductors. The switching losses depends on voltage stress (V_S) and current stress (I_{Stress}), rising time (t_r) and falling time (t_f) and switching frequency (f_s) of semiconductors, as (7). In this study, the employment of nearest level modulation technique has reduced the switching frequency of switches, which suppress the switching losses [24].

$$P_{Loss,\,Switching} = \frac{1}{6} f_s V_S I_{Stress} (t_r + t_f) \tag{7}$$

5.1.3 | Voltage ripple loss of capacitors

Besides the conduction losses that happen at ESR of capacitors, the voltage ripple of capacitors is another source of loss, which is called "voltage ripple loss" of capacitors. This kind of loss can be computed from (8), where f_s: switching frequency, C: capacitance of capacitor, ΔV_{Ripple}: voltage ripple of capacitor [24].

$$P_{Loss,\,Ripple} = \frac{1}{2} f_s C (\Delta V_{Ripple})^2 \tag{8}$$

5.2 | Capacitor design

The voltage ripple of capacitors is an important factor that affects the capacitor losses as well as output voltage quality (and THD). The long discharging intervals of capacitors lead to higher ripples, higher losses and lower output voltage quality. The voltage ripple on capacitors can be limited by suitable design of capacitances.

In this paper, the capacitances have been selected based on (9–10) [24], where I_o: magnitude of the output current, $\cos(\varphi)$: load power factor, $[t_{start} - t_{end}]$: longest discharging interval of capacitors, ΔV_{Ripple}: maximum allowable voltage ripple of capacitors

$$\Delta Q_C = C \times \Delta V_{Ripple} = \int_{t_{start}}^{t_{end}} I_o \sin(\omega t) \times \cos(\varphi) dt \tag{9}$$

$$C \geq \frac{\int_{t_{start}}^{t_{end}} I_o \sin(\omega t) \times \cos(\varphi) dt}{\Delta V_{Ripple}} \tag{10}$$

TABLE 5 Comparison statistics

Topology	[19]	[20]	[21]	[22]	[23]	[24]	Proposed
N_{Level}	$2(3^n)+1$	$12n+1$	$12n+1$	$8n+1$	$8n+1$	$8n+1$	$2^{(n+2)}+1$
$N_{MOSFET/IGBT}$	$5n+4$	$14n$	$18n+5$	$12n$	$8n+2$	$20n$-1	$2n+6$
$N_{Switch} = N_{Driver}$	$5n+4$	$11n$	$15n+4$	$10n$	$6n+2$	$20n$-1	$2n+6$
N_{Source}	1	$2n$	1	n	n	1	1
$N_{Capacitor}$	$2n$	$2n$	$6n$	$2n$	$2n$	$4n$-1	$2n+1$
N_{Diode}	n	$14n$	$4n$	0	n	$3n$	$2n+1$
N_{Device}	$13n+9$	$43n$	$43n+10$	$25n$	$18n+4$	$47n$-2	$8n+15$
Gain	$3n$	2	$6n$	2	2	$4n$	$2^{(n+1)}$
TVS	$5.66(3^n)$	$32n$	$42n$-2	$11n$	$16n+8$	$20n$-1	$12(2^n)-1$
Efficiency (%) Output power	92.1244 W	95.360 W	97.2900 W	80.615.5W	95400 W	88.974 W	94.2235 W
THD (%)	7.6 13-level	2.325-level	6.313-level	N/A	N/A	4 9-level	3.9717-level

6 | COMPARISONS

To verify the claimed properties, the suggested topology is compared with novel configurations presented in [19–24] from aspects of voltage gain, number of output voltage levels (N_{Level}), sources (N_{Source}), capacitors ($N_{Capacitor}$), switches (N_{Switch}), MOSFETs (N_{MOSFET}), gate-driver circuits (N_{Driver}), total devices (N_{Device}), and total voltage stress. Also, some conventional topologies [19–24] and the proposed topology have been compared from economic viewpoint through a *CF*. Various definitions have been presented for *CF* in literature, like [23, 24, 30]. This study considers the definition presented in [23], as (11), where the 'α' denotes the weight coefficient of total voltage stress [23].

$$CF = (N_{MOSFET} + N_{Diode} + N_{Driver} + N_{Cap} + \alpha\ TVS)N_{Source} \tag{11}$$

Table 5 and Figure 6 show the comparison results. Based on Figure 6a, despite using single DC source, the suggested and [19, 21, 24] topologies produce more steps (or gains) than others. This leads to a compact, cheap, and light structure. Also, to achieve equal steps, the proposed configuration requires less switches, MOSFETs and gate driver circuits than others (see Figure 6b,c). This property leads to reduced size and simple structure. As evident from Figure 7a,b, in wide range, the proposed configuration requires less number of capacitors and diodes than [20–24] to obtain equal number of steps. The reduction in diodes count will lead to reduced losses and improved efficiency.

Figure 8a,b confirms that with the same count of devices ($N_{Source} + N_{MOSFET} + N_{Driver} + N_{Capacitor} + N_{Diode}$), the suggested structure can provide more steps and gains than the others. In the other words, to obtain the same gain or steps, the proposed topology requires fewer devices, which causes to have a compact, light, and cheap structure.

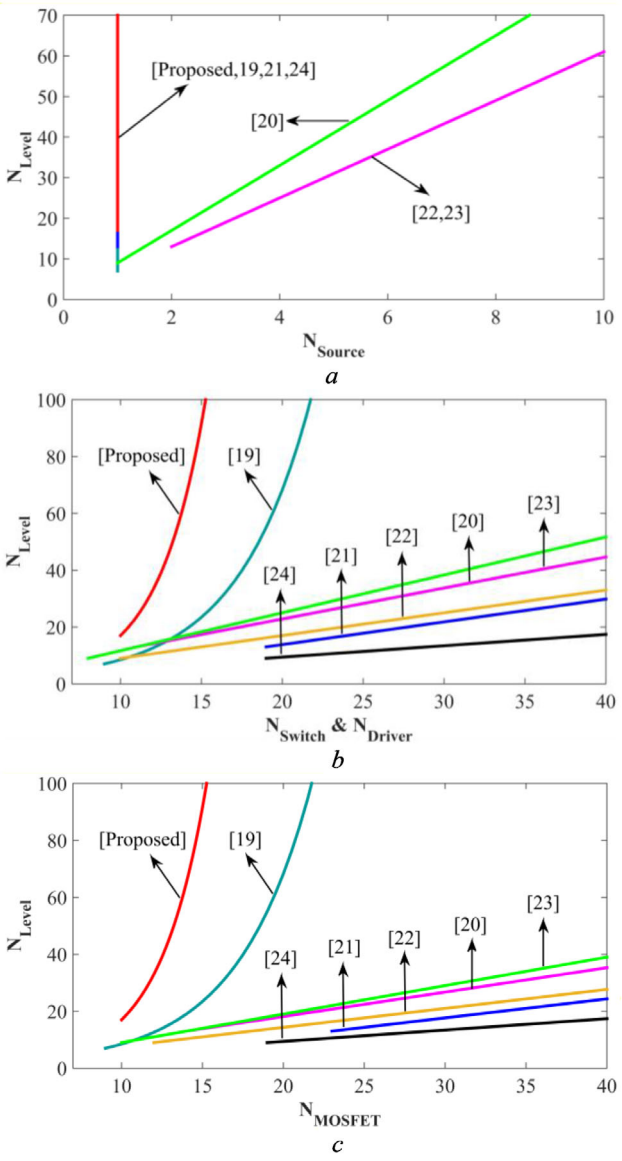

FIGURE 6 Comparison results for number of sources, switches, gate-driver circuits and MOSFETs: (a) N_{Level} vs. N_{Source}; (b) N_{Level} vs. N_{Switch} and N_{Driver}; (c) N_{Level} vs. N_{MOSFET}

Based on Figure 9, while producing the same gains, less total voltage stress is imposed on semiconductors of proposed topology than other structures. This leads to reduced losses and improved efficiencies. Figure 10 displays the CF/N_{Level} of the proposed topology and [19–24] for different weighting coefficient of total voltage stress (α). It is seen that the CF/N_{Level} in the proposed topology is always less than that of other structures, which is a sign of reduced devices, low total voltage stress on semiconductors, and increased number of levels.

Table 5 presents the reported efficiency of topologies presented in [19–24] at their operation point (at a specific output power). It is seen that the proposed topology has better efficiency than other counter parts at equal output power levels. Also, the proposed topology has the second least THD among selected topologies. The low-THD of proposed topology is because of its high number of levels.

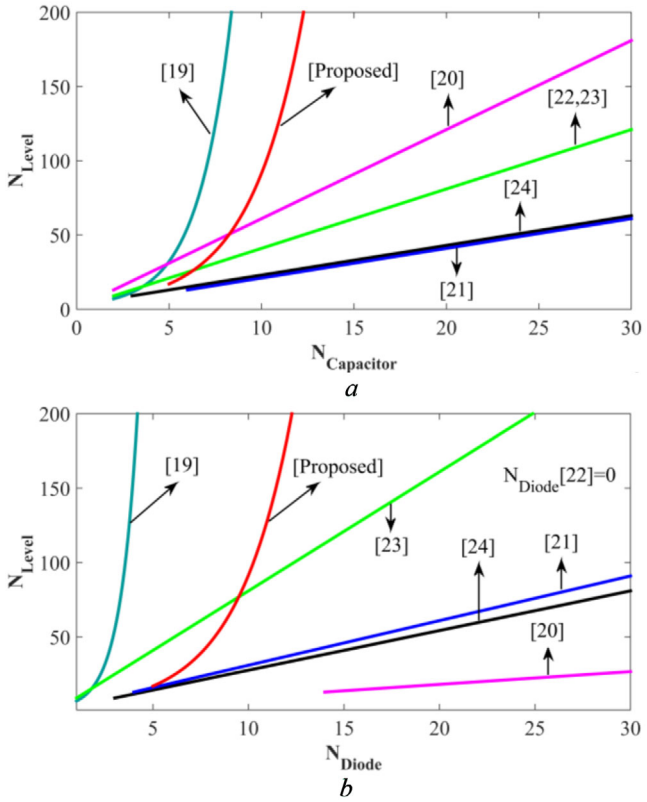

FIGURE 7 Comparative analysis on number of levels, capacitors and diodes: (a) N_{Level} vs. $N_{Capacitor}$; (b) N_{Level} vs. N_{Diode}

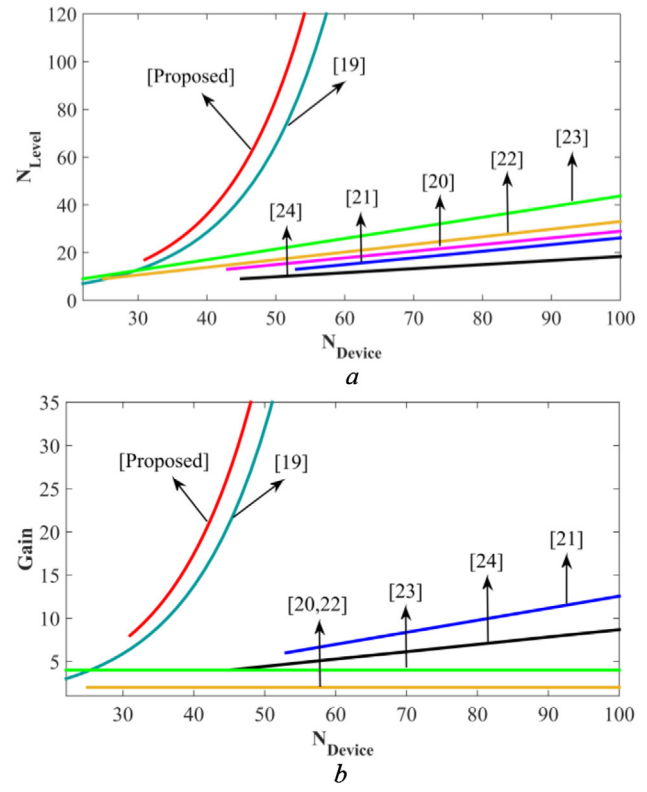

FIGURE 8 Comparisons on number of levels, number of devices and step-up capability: (a) *Gain* vs. N_{Device}; (b) *Gain* vs. *TVS*

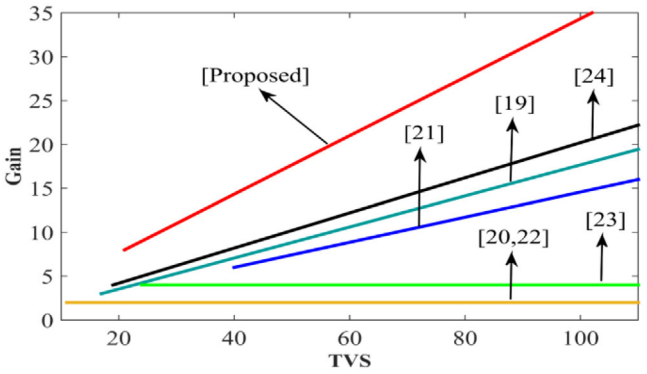

FIGURE 9 Gain comparison vs. TVS

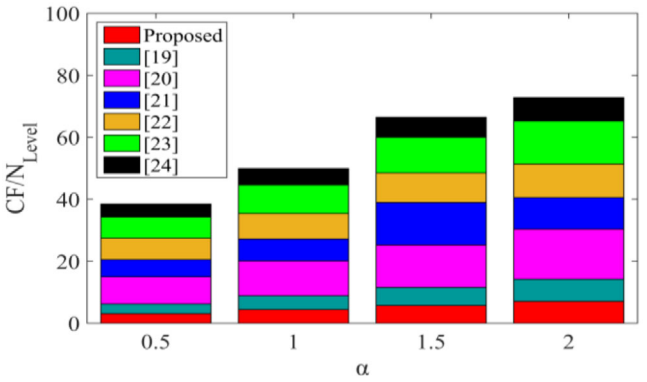

FIGURE 10 CF/N_{Level} of structures in different values of α

7 | EXPERIMENTAL RESULTS

To certify the feasibility of the proposed topology, the laboratory-scale prototype of the basic (17-level) structure has been implemented (Figure 11a). The nearest level technique (Figure 5) and the *Atmega*32 microcontroller have been employed for producing switching pulses. The setup parameters and device specifications have been presented in Table 6. Figure 11b shows the output voltage/current of the proposed basic topology for *R-L* load of $R = 48\ \Omega$ and $L = 120$ mH. It

TABLE 6 Description of the experimental setup

Parameter	Value
Input DC source	$V_{IN} = 20[V]$
Frequency of reference waveform in nearest level	$f_o = 50[Hz]$
MOSFETs	*IRFP260NPbF*
Diodes	*DSEP29-06A*
Optocoupler-driver	*TLP-250*
Capacitances	$C_1 = C_2 = C_3 = C_4 = C_5 = 4700[\mu F]$
Microcontroller	*ATmega32*
Load	$R = 48[\Omega]$, $L = 120[mH]$
Oscilloscope	GPS-1072B+

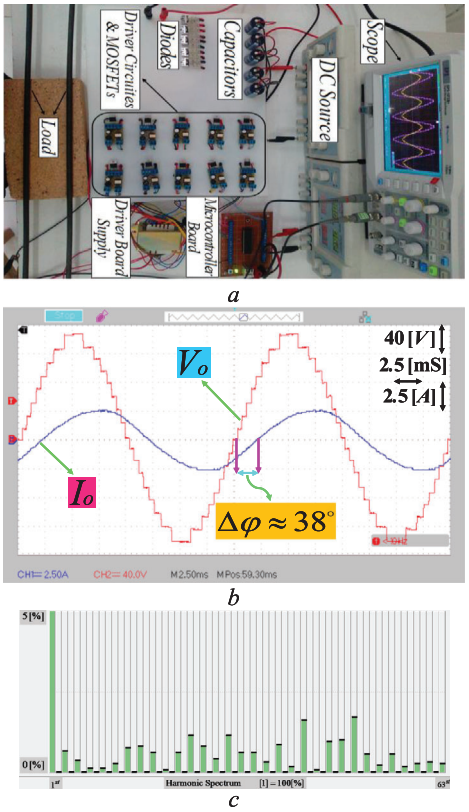

FIGURE 11 Experimental setup and results: (a) laboratory prototype of proposed 17-level topology; (b) output voltage and current waveforms; (c) harmonic spectrum

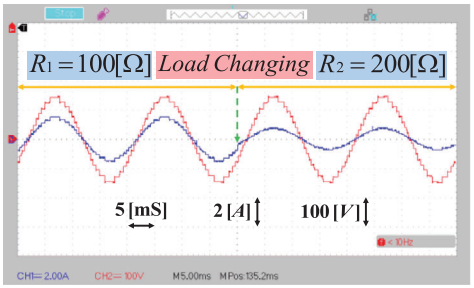

FIGURE 12 Dynamic performance of proposed topology during load step change from 113 to 60 W

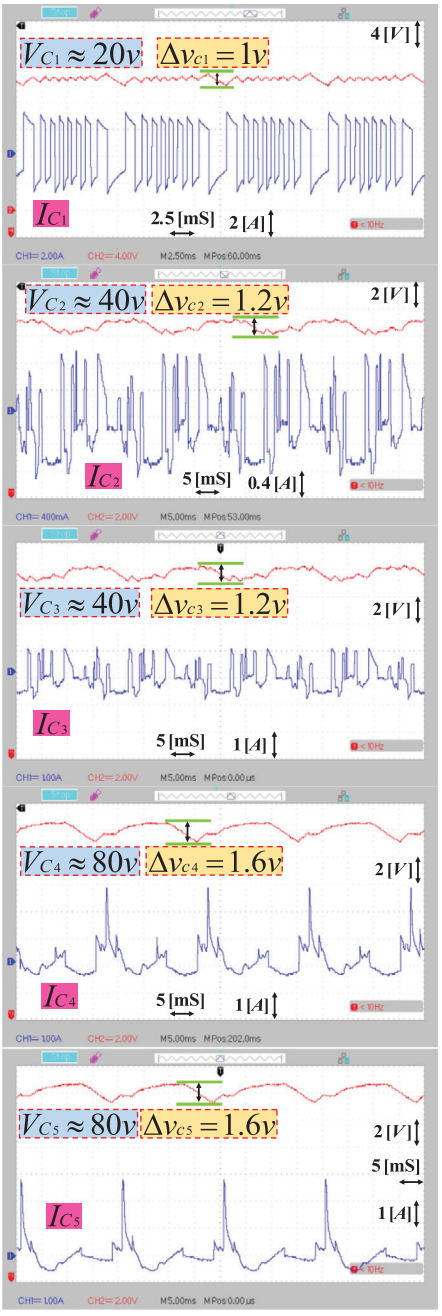

FIGURE 13 Voltage and current waveforms of capacitors

is evident that the proposed basic topology has efficiently produced 8 positive, 8 negative, and zero (totally 17) steps. The peak load voltage and current are respectively about $V_{o,max} \approx$ 150 V, and $I_{o,max} \approx 2.5A$. So, the experimental gain of basic topology is about $(V_{o.max}/V_{IN}) \approx 7.5$. The difference between theoretical and experimental results originate from voltage drop on components (on-state resistance of semiconductors, forward voltage drops of diodes, ESR of capacitors). The phase difference of $\Delta\varphi \approx 38°$ seen between load voltage and current waveforms (validated by $\Delta\varphi = \arctan(L\omega/R)$) proves the capability of the proposed configuration on supplying *R-L* loads. According to Figure 11c, the THD (obtained from simulations done in PSCAD/EMTDC) of the output voltage is about 3.97%, which follows the IEEE519 standard ($THD \leq 8\%$, $H_i \leq 5\%$).

Figure 12 shows the dynamic performance of the proposed topology. It is observed that during load step-change from $R = 100\ \Omega$ to $R = 200\ \Omega$, the load current is decreased to about half, and the output voltage increases just 2% to 2.5%. This certifies the appropriate dynamic performance of the proposed topology.

The voltage/current waveforms of C_1–C_5 have been presented in Figure 13. The results show that the voltage of C_1–C_5 has been naturally regulated on $V_{C1} \approx 20$ V, $V_{C2} = V_{C3} \approx 40$ V, $V_{C4} = V_{C5} \approx 80$ V.

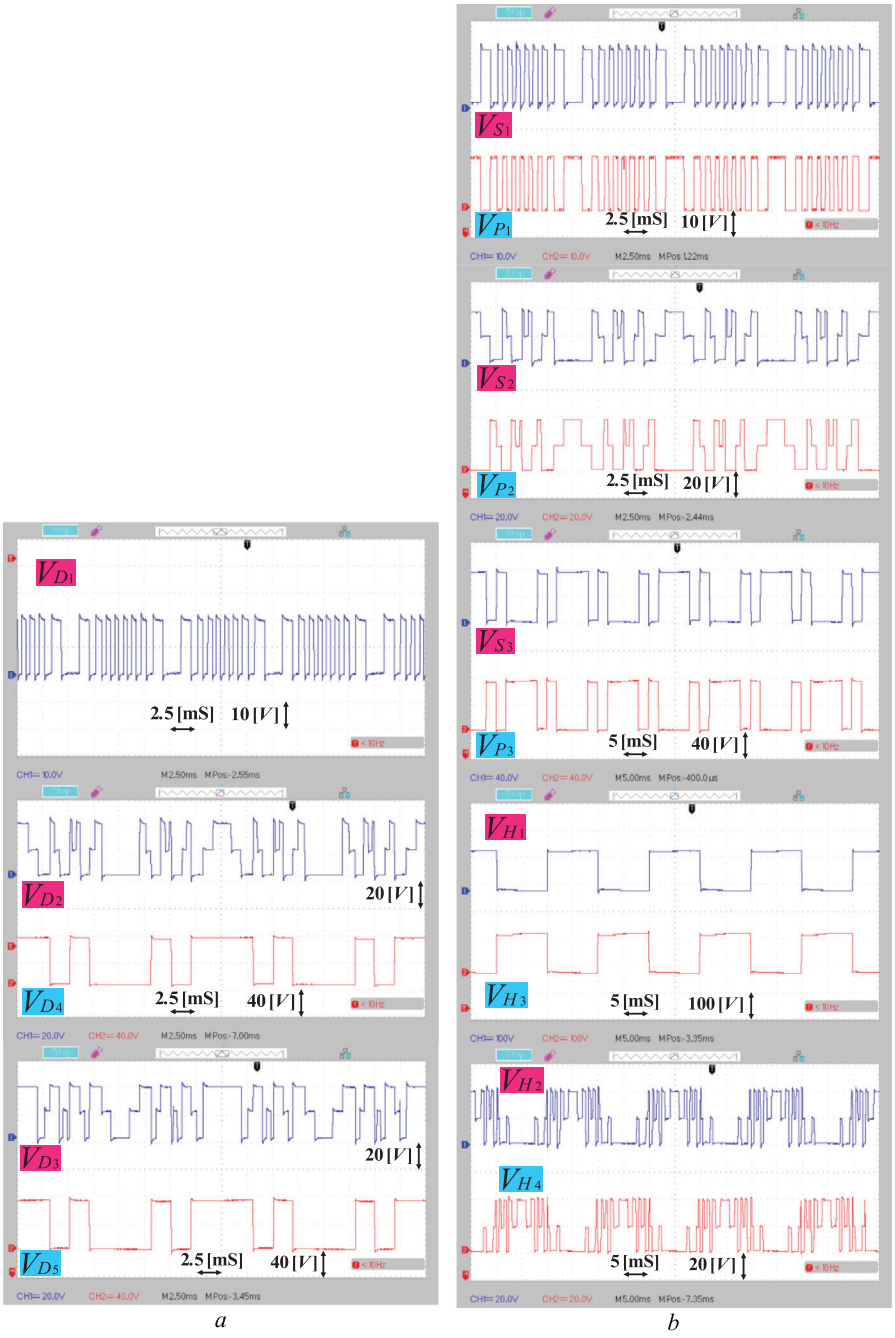

FIGURE 14 Voltage waveforms of (a) diodes and (b) switches

The obtained results for voltage ripple of capacitors are $\Delta v_{C1} \approx 1$ V, $\Delta v_{C2} = \Delta v_{C3} \approx 1.2$ V, and $\Delta v_{C4} = \Delta v_{C5} \approx 1.6$ V. These small values obtained for voltage ripple confirm proper natural voltage balancing of capacitors. Also, the voltage/current waveform of capacitors (Figure 13) indicates that the charge/discharge process of capacitors has been uniformly distributed in the switching period. Based on Table 1, the charge/discharge process of C_2 (or C_4) is exactly the same as C_3 (or C_5). The only difference is that the C_2 (or C_4) is employed in positive voltage levels, but the C_3 (or C_5) is applied at the same negative voltage levels. So, the C_2 (or C_4) can be selected identical to C_3 (or C_5). That is why the voltage waveform, voltage ripple, and charge/discharge current waveform of C_2 (or C_4) is similar to that of C_3 (or C_5).

The voltage waveform and voltage stress on semiconductors are shown in Figure 14 and Table 7. Figure 14 confirms that only H_1 and H_3 switches withstand $V_{o,max}$ and the voltage stress on other semiconductors (especially the H_1 and H_3 as output switches) are much less than $V_{o,max}$.

Figure 15 displays the THD of the proposed structure at different modulation indexes. According to Figure 15, as the modulation index increases, the THD of converter decreases, which

TABLE 7 Experimental results obtained for voltage stress (VS) on switches/diodes

Switch	*VS* [*V*]	Switch	*VS* [*V*]	Diode	*VS* [*V*]
S_1	20	P_1	20	D_1	20
S_2	40	P_2	40	D_2	40
S_3	80	P_3	80	D_3	40
H_1	160	H_3	160	D_4	80
H_2	40	H_4	40	D_5	80

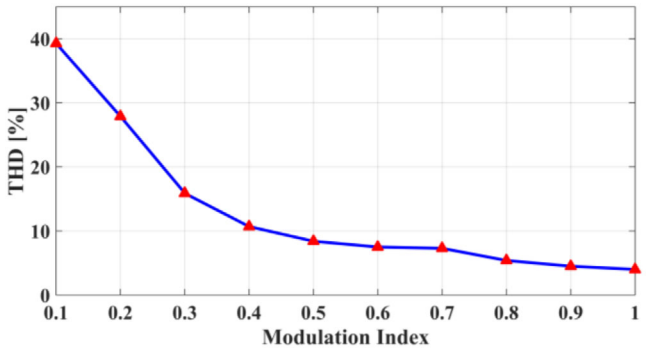

FIGURE 15 THD of the output voltage vs. modulation index

leads to higher qualities. Note that at low modulation indexes, the number of levels of proposed topology decreases, but it still operates as a multilevel inverter.

Figure 16a shows the measured efficiency of suggested 17-level structure for different pure resistive loads of $R = 210[\Omega]$ ($P_o = 59[W]$) to $R = 48[\Omega]$ ($P_o = 217[W]$) (as worst condition). Figure 16a indicates that the efficiency of the converter is reduced by increment of the output power. Please note that much better efficiencies can be obtained by employing gallium nitride (GaN) or silicon carbide (SiC) semiconductors, which benefit from small on-state resistances. The efficiency of the proposed basic topology at operating point ($R = 48[\Omega]$ and $L = 120[mH]$) is about 94.2% (Figure 16b). The switching loss of diodes and MOSFETs are respectively $P_{Sw,Diodes} \approx 3.3[mW]$ and $P_{Sw,MOSFETs} \approx 13.7[mW]$. The conduction loss of diodes and MOSFETs are respectively $P_{Cond,Diodes} \approx 8.5[W]$ and $P_{Cond,MOSFETs} \approx 4.7[W]$. Also, the total power loss of capacitors is about $P_{Loss,Capacitors} \approx 1.5[W]$. It is seen that the employment of nearest level technique has limited the switching loss of semiconductors.

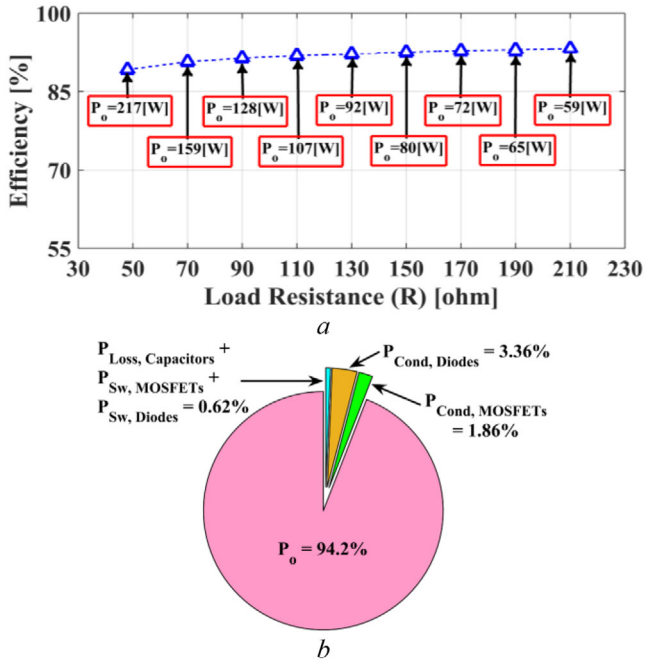

FIGURE 16 Efficiency analysis: (a) efficiency of proposed basic topology at pure resistive loads; (b) power losses at operating point ($R = 48\ \Omega$ and $L = 120$ mH)

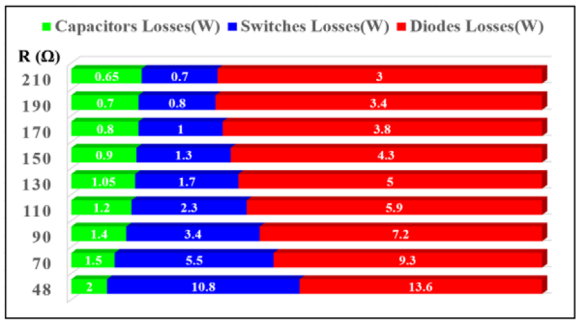

FIGURE 17 Detailed losses and the share of switches, diodes, and capacitors of total power loss at different output powers

Figure 17 shows the loss distribution (in watt and per cent) between switches, diodes, and capacitors at different output powers.

At low powers, the diodes and switches have almost the same losses. But as the output power increases, the loss of diodes becomes larger than that of switches. It is also seen from Figure 17 that the power dissipated in capacitors (due to their voltage ripple) smoothly increases by increment of output power.

8 | CONCLUSIONS

This paper proposes and developed a basic SCBMLI topology that can produce 17 steps and the voltage gain of 8 by means of only 1 DC source, 10 unidirectional switches, 5 capacitors, and 5 diodes. The proposed basic structure can be extended by extending the switched-capacitor stages to achieve higher voltage gains and levels. Due to the single-source nature of the proposed extended topology, it is expected to have less size, weight, and cost than other multi-source counterparts. The proposed generalized topology applies two half-bridges instead of a full-bridge (H-bridge) to create negative steps. Thus, only 2 switches (rather than 4 switches) are imposed to maximum voltage stress. This leads to less total voltage stress. Also, modularity, self-voltage balancing of capacitors, low voltage ripple on capacitors, and suitability for R-L loads are other main advantages of the proposed topology. Due to high quality and low THD

of output voltage, the output filter can be eliminated or downsized. It is also noticed from comparison results that the proposed topology has higher steps per device count, higher gain per device count, lower total voltage stress, and lower cost function than other similar SCBMLIs, which are impressive profits. The laboratory-scale prototype of the proposed 17-level topology has been implemented. The comparative analysis as well as experimental results certify the effective and correct performance of the suggested topology.

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REFERENCES

1. Vijeh, M., et al.: A general review of multilevel inverters based on main submodules: Structural point of view. IEEE Trans. Power Electron. (2019).
2. Perez, M.A., et al.: Circuit topologies, modeling, control schemes, and applications of modular multilevel converters. IEEE Trans. Power Electron. 30(1), 4–17 (2014).
3. Khan, M.N., et al.: Switched capacitor integrated (2n+1)-level step-up single-phase inverter. IEEE Trans. Power Electron. (2019)
4. Sandeep, N., et al.: A self-balancing five-level boosting inverter with reduced components. IEEE Trans. Power Electron. 34(7), 6020–6024 (2018).
5. Babaei, E., Alilu, S., Laali, S.: A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-bridge. IEEE Trans. Ind. Electron. 61(8), 3932–3939 (2014).
6. Lee, S.S., et al.: Hybrid 7-level boost active-neutral-point-clamped (H-7L-BANPC) inverter. IEEE Trans. Circuits Syst. II Express Briefs (2019)
7. Gupta, K.K., et al.: Multilevel inverter topologies with reduced device count: A review. IEEE Trans. Power Electron. 31(1), 135–151 (2015).
8. Lee, S.S., et al.: New family of boost switched-capacitor 7-level inverters (BSC7LI). IEEE Trans. Power Electron. (2019).
9. Raman, S.R., Cheng, K.W.E., Ye, Y.: Multi-input switched-capacitor multilevel inverter for high-frequency AC power distribution. IEEE Trans. Power Electron. 33(7), 5937–5948 (2018).
10. Taheri, A., Rasulkhani, A., Ren, H.P.: An asymmetric switched capacitor multilevel inverter with component reduction. IEEE Access 7, 127166–127176 (2019).
11. Majumdar, S., Mahato, B., Jana, K.C.: Implementation of an optimum reduced components multi-cell multilevel (MC-MLI) inverter for lower standing voltage. IEEE Trans. Ind. Electron. (2019)
12. Saeedian, M., Hosseini, S.M., Adabi, J.: A five-level step-up module for multilevel inverters: Topology, modulation strategy, and implementation. IEEE J. Emerging Sel.Top. Power Electron. 6(4), 2215–2226 (2018).
13. Sandeep, N., et al.: Switched-capacitor-based quadruple-boost nine-level inverter. IEEE Trans. Power Electron. 34(8), 7147–7150 (2019).
14. Liu, J., et al.: A novel nine-level quadruple boost inverter with inductive-load ability. IEEE Trans. Power Electron. (2018)
15. Saeedian, M., et al.: A novel step-up single source multilevel inverter: Topology, operating principle, and modulation. IEEE Trans. Power Electron. 34(4), 3269–3282 (2019).
16. Varesi, K., Karimi, M., Kargar, P.: A new basic step-up cascaded 35-level topology extendable to higher number of levels. In: 2019 10th International Power Electronics, Drive Systems and Technologies Conference (PEDSTC). IEEE, pp. 291–296 (2019)
17. Alishah, R.S., et al.: New high step-up multilevel converter topology with self-voltage balancing ability and its optimization analysis. IEEE Trans. Ind. Electron. 64(9), 7060–7070 (2017).
18. Ghodsi, M., Barakati, S.M.: A generalized cascade switched-capacitor multilevel converter structure and its optimization analysis. IEEE J. Emerging Sel. Top. Power Electron. (2019)
19. Roy, T., Sadhu, P.K., Dasgupta, A.: Cross-switched multilevel inverter using novel switched capacitor converters. IEEE Trans. Ind. Electron. 66(11), 8521–8532 (2019).
20. Samadaei, E., Kaviani, M., Bertilsson, K.: A 13-levels module (K-type) with two DC sources for multilevel inverters. IEEE Trans. Ind. Electron. 66(7), 5186–5196 (2018).
21. Khenar, M., et al.: Multi-level inverter with combined T-type and cross-connected modules. IET Power Electron. 11(8), 1407–1415 (2018).
22. Lee, S.S.: Single-stage switched-capacitor module (S 3 CM) topology for cascaded multilevel inverter. IEEE Trans. Power Electron. 33(10), 8204–8207 (2018).
23. Barzegarkhoo, R., et al.: A new boost switched-capacitor multilevel converter with reduced circuit devices. IEEE Trans. Power Electron. 33(8), 6738–6754 (2018).
24. Taghvaie, A., Adabi, J., Rezanejad, M.: A self-balanced step-up multilevel inverter based on switched-capacitor structure. IEEE Trans. Power Electron. 33(1), 199–209 (2018).
25. Gandomi, A.A., Varesi, K., Hosseini, S.H.: Control strategy applied on double flying capacitor multi-cell inverter for increasing number of generated voltage levels. IET Power Electron. 8(6), 887–897 (2015).
26. Shu, Z., et al.: Voltage balancing approaches for diode-clamped multilevel converters using auxiliary capacitor-based circuits. IEEE Trans. Power Electron. 28(5), 2111–2124 (2012).
27. Deliri Khatoonabad, S., Varesi, K.: An extended high step-up switched-capacitor based multi-level inverter topology. In: *2019 International Power System Conference (PSC)*, Tehran, Iran. IEEE, pp. 459–464 (2019)
28. Babaei, E., Gowgani, S.S.: Hybrid multilevel inverter using switched capacitor units. IEEE Trans. Ind. Electron. 61(9), 4614–4621 (2014).
29. Ye, Y., et al.: A step-up switched-capacitor multilevel inverter with self-voltage balancing. IEEE Trans. Ind. Electron. 61(12), 6672–6680 (2014).
30. Raman, S.R., et al.: Family of multiport switched-capacitor multilevel inverters for high-frequency AC power distribution. IEEE Trans. Power Electron. 34(5), 4407–4422 (2018).

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