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Improved Cascaded H-Bridge Multilevel Inverters with Voltage-Boosting Capability

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Abstract: This paper proposes two improved cascaded H-bridge (ICHB) multilevel inverters that feature voltage-boosting capability. The conventional H-bridge with a front-end dc–dc boost converter was restructured for single-stage operation. The developed three-level topology not only saves one power switch but also exhibits lower voltage stress across its capacitor. Extension to five-level generation was also introduced by merely adding two power switches and one capacitor. The final five-level topology outperforms the classical cascaded H-bridge (CHB) multilevel inverter with a significant reduction in the power switch count, with a 42% and 50% reduction in both the isolated dc source and inductor counts. The power efficiency was also improved without compromising the modularity feature of the classical CHB multilevel inverter. The operation and theoretical analysis of the proposed topologies were validated via simulations and experimental tests.

Keywords: cascaded H-bridge; multilevel inverter; voltage-boosting

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1. Introduction

The establishment of the first multilevel inverter dates to 1971. The cascaded H-bridge (CHB) [1] has revolutionized the dc-to-ac power conversion since its introduction. It has become a highly developed and mature technology for various industrial and renewable energy applications after a few decades of improvement [2–7]. Today, researchers are continuously improving the compactness and efficiency of cascaded multilevel inverters by establishing various topologies with reduced switch counts and fewer conversion stages [8].

One popular approach to lower the switch count is to adopt a hybrid concept that divides the voltage level generation and polarity inversion into two stages [9]. Multiple half-bridges that respectively control an isolated dc source are cascaded to generate multiple levels of a unipolar voltage across the dc-link of an H-bridge. The H-bridge is operated at the line frequency with a duty cycle of 0.5 to generate a multilevel ac voltage. This type of topology is referred to as a multilevel dc-link inverter, and its half-bridges can be replaced by different modules to favorably increase the number of levels with minimal switch count. For example, a switched-diode module in place of a half-bridge is able to reduce the essential power switches from six to three for controlling three isolated dc sources [10].

Compact modules that control multiple isolated dc sources for bipolar ac voltage generation without a rear-end H-bridge have also been explored in recent years. In Ref. [11], an E-type module that integrates a half-bridge and a T-type inverter with four additional switches was presented. It uses four isolated dc sources with asymmetrical magnitudes to generate 13 voltage levels. The E-type module can be extended to generate an ac voltage of 17 levels by adding two additional power switches [12]. An optimized module for the cascaded multilevel inverter in [13] achieves the least switches per level generation.

However, the requirement of multiple isolated dc sources for each module leads to an uneven duration to supply the load, which, in turn, results in a power-balancing issue. Therefore, it does not preserve the modularity feature of the conventional CHB [14].

One common limitation of all the above modules is that their voltage gain is restricted to unity, which is similar to the classical CHB multilevel inverter. They require the same number and magnitude as isolated dc sources as those in the CHB. Considering a PV source that generates low dc voltage in each module, a large number of series-connected PV modules are necessary to achieve a sufficient magnitude of ac voltage. Alternatively, a boost dc–dc converter can be added between PV source and inverter module. This two-stage power conversion, however, uses more components and reduces power efficiency. In light of this, there is a growing trend in developing inverter topologies with integrated voltage-boosting. To achieve single-stage power conversion, the concept of a Z-source inverter was adopted in [15] by integrating a quasi-switched impedance network into each H-bridge. In [16], a five-level boost inverter module was established by using 10 power switches, 2 inductors, and 2 capacitors.

Two improved CHB topologies are proposed in this paper, i.e., a three-level configuration and a 5five-level configuration that provides voltage-boosting without sacrificing the modularity feature of the conventional CHB. Moreover, they also exhibit higher compactness with a reduced number of switches, isolated dc sources, and inductors. The rest of the paper is organized as follows. Section 2 presents the steady-state analysis of the proposed improved CHB topologies and their pulse-width modulation (PWM) technique. Section 3 benchmarks the proposed topologies with the existing cascaded multilevel inverters. The simulation and experimental results are discussed in Section 4. Finally, Section 5 concludes this paper.

2. Proposed ICHB Multilevel Inverters

2.1. ICHB (3L)

The use of a front-end dc–dc boost converter in a classical CHB multilevel inverter is mandatory to boost the voltage. The resultant two-stage structure is depicted in Figure 1a. Some structural modifications of such a configuration enable a concurrent achievement of voltage-boosting and ac voltage generation within a single-stage operation. The established topology is referred to as ICHB (3L), and it uses one switch less than the CHB with a front-end boost converter, as illustrated in Figure 1b. The reorganized structure shows that the capacitor C_1 is connected in series with the dc source, thus alleviating its voltage stress.

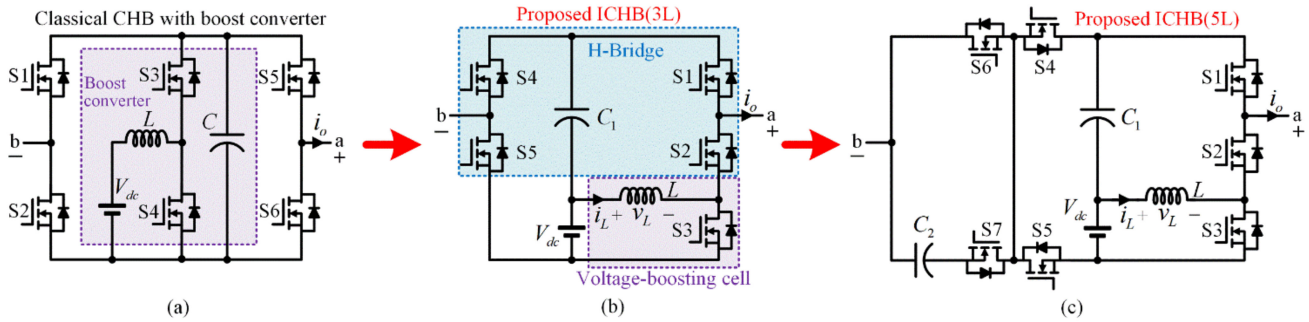


Figure 1. Derivation of the proposed ICHB topologies: (**a**) classical CHB with a front-end boost converter, (**b**) proposed ICHB (3L), and (**c**) proposed ICHB (5L).

Referring to the switching states in Figure 2a, it is known that the proposed ICHB (3L) is able to generate three ac voltage levels, while simultaneously charging the boost inductor with a constant duty cycle D, according to the modulation scheme in Figure 3a. By taking the volt-second balance across the inductor L, the average voltage of the capacitor C_1 is obtained as

$$V_{C_1} = \frac{D}{1-D} V_{dc} \tag{1}$$

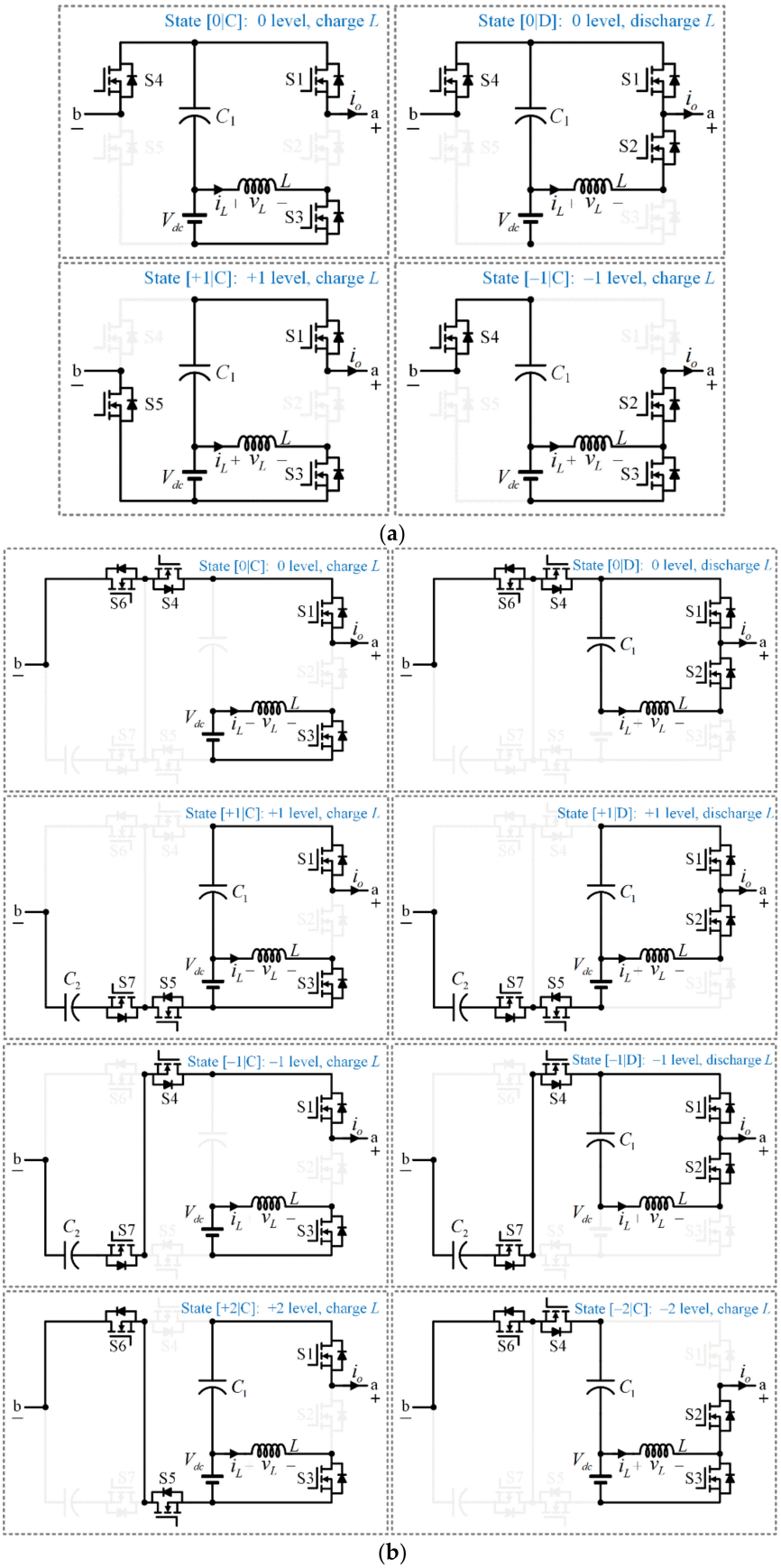


Figure 2. Switching states of the proposed topologies: (**a**) ICHB (3L) and (**b**) ICHB (5L).

The maximum ac voltage level $V_{\max}$ is the sum of the capacitor and dc source voltages. That is,

$$V_{\max} = \frac{1}{1-D} V_{dc} \tag{2}$$

By controlling the modulation index M, the amplitude of the fundamental ac voltage $\hat{V}_{o,1}$ can be written as

$$\hat{V}_{o,1} = \frac{M}{1-D} V_{dc} \tag{3}$$

The voltage ripple of the capacitor C_1 and current ripple of the inductor L consist of low-frequency and high-frequency components due to the single-phase load and the pulse-width modulation (PWM), respectively. The low-frequency voltage ripple of C_1 can be obtained by analyzing the double-line-frequency current flowing through this capacitor. Through Fourier analysis, the double-line-frequency component of the rectified load current depicted in Figure 3a is derived. Considering the impedance of C_1 at double-line-frequency, the low-frequency voltage ripple $\Delta V_{C_1,2f_o}$ of capacitor C_1 can be written as

$$\Delta V_{C_1,2f_o} = \frac{4\hat{I}_{o,1}}{6\pi^2 f_o C_1} \tag{4}$$

where $\hat{I}_{o,1}$ is the amplitude of the load current at the line frequency f_o. Considering the ideal dc source, the voltage across the inductor at double-line frequency can be calculated by multiplying the capacitor C_1 voltage with (1-D). Considering the impedance of inductor L at double-line frequency, the low-frequency current ripple $\Delta I_{L,2f_o}$ of the inductor L is given by the following expression:

$$\Delta I_{L,2f_o} = \frac{(1-D)\hat{I}_{o,1}}{6\pi^3 f_o^2 L C_1} \tag{5}$$

As the inductor is charged with a constant duty cycle D, the high-frequency ripple of the capacitor voltage $\Delta V_{C_1,f_s}$ and inductor current $\Delta I_{L,f_s}$ are similar to the equations of the boost dc–dc converter that can be respectively written as

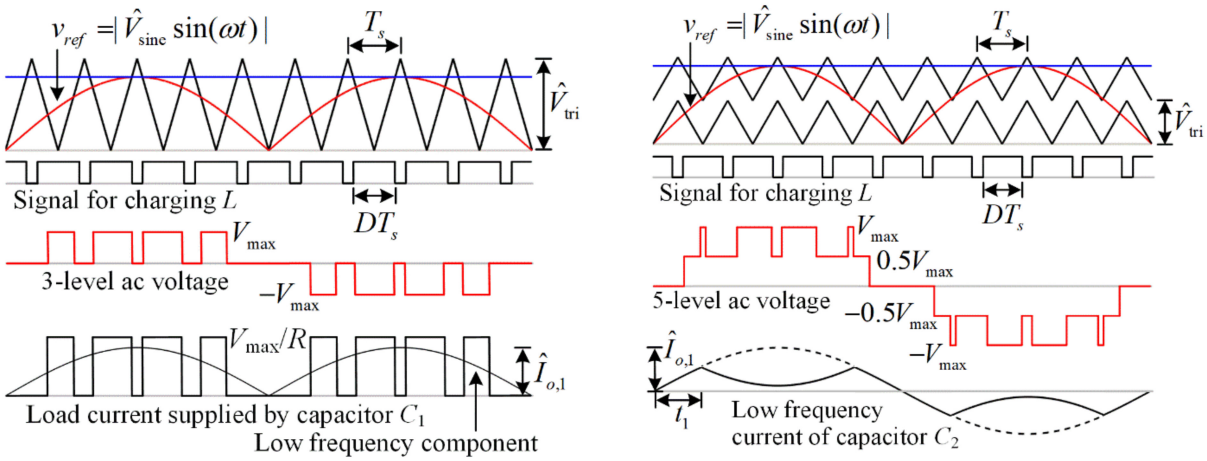
$$\Delta V_{C_1,f_s} = \frac{2D\hat{I}_{o,1}}{\pi f_s C_1} \tag{6}$$

$$\Delta I_{L,f_s} = \frac{DV_{dc}}{f_s L} \tag{7}$$

2.2. ICHB (5L)

The number of voltage levels can be further extended to five by integrating merely two additional power switches and one additional capacitor, as depicted in Figure 1c. The switching states in Figure 2b show that the capacitor C_2 is operated symmetrically over each half-cycle, signifying that the capacitor voltage is balanced naturally at 0.5 $V_{\max}$. Figure 3b shows the extended PWM scheme for the proposed ICHB (5L). Based on the current waveform depicted in Figure 3b, the charge balance of C_2 is clearly seen in each fundamental cycle. The amount of electric charge flowing into the capacitor in each fundamental cycle can be obtained by integrating the current in positive half-cycle. By dividing electric charge by the capacitance, the voltage ripple ΔV_{C_2} of C_2 can be written as

$$\Delta V_{C_2} = \frac{\hat{I}_{o,1}}{\pi f_o C_2}\left[1 + \frac{\pi}{2M} - 2\cos\left(\sin^{-1}\frac{1}{2M}\right) - \frac{1}{M}\sin^{-1}\frac{1}{2M}\right] \tag{8}$$



(**a**) (**b**)

Figure 3. Pulse-width modulation scheme for the proposed topologies: (**a**) ICHB (3L) and (**b**) ICHB (5L).

2.3. Cascaded Extension

Both the proposed ICHB (3L) and ICHB (5L) topologies preserve the modularity of the conventional CHB, and they can be conveniently extended by cascading n modules controlled by the same reference signals. The phase shift of the triangular carrier for the mth module is

$$\theta_{tri,m} = \frac{360^\circ}{n}(m-1) \tag{9}$$

where $m = \{1, 2, \ldots, n\}$. The maximum number of voltage levels for n cascaded ICHB (3L) and ICHB (5L) is, respectively, expressed as

$$N_{level}^{\text{ICHB(3L)}} = 2n + 1 \tag{10}$$

$$N_{level}^{\text{ICHB(5L)}} = 4n + 1 \tag{11}$$

3. Comparison with CHB Multilevel Inverter

Table 1 compares the proposed topologies and the classical CHB. While the voltage gain of a classical CHB was restrained to unity, the comparison was made for the classical CHB with an integrated front-end boost converter, as shown in Figure 1a. Considering the same number of voltage levels, noteworthy advantages of the proposed topologies are listed as follows.

Superiority of the proposed ICHB (3L) over a conventional single CHB module (Figure 1a with $n = 1$):

(1) Reduced switch count from 6 to 5.
(2) Reduced capacitor voltage stress from $V_{\max}$ to $DV_{\max}$.
(3) Reduced total standing voltage (TSV) of the inverter from $6V_{\max}$ to $5V_{\max}$.

Superiority of the proposed ICHB (5L) over two cascaded conventional CHB modules (Figure 1a with $n = 2$):

(1) Reduced switch count by 42%, i.e., from 12 to 7.
(2) Reduced number of isolated dc sources from 2 to 1.
(3) Reduced inductor count from 2 to 1.

Table 1. Comparison between the proposed ICHBs and the classical CHB with a front-end boost converter (Figure 1a).

	3-Level		5-Level	
	CHB (Figure 1a, n = 1)	**Proposed ICHB (3L)**	**CHB (Figure 1a, n = 2)**	**Proposed ICHB (5L)**
Switch	6	5	12	7
DC source	1	1	2	1
Inductor	1	1	2	1
Capacitor	1	1	2	2
Gain	$M/(1-D)$	$M/(1-D)$	$M/(1-D)$	$M/(1-D)$
V_{C_1}/V_{max}	1	D	0.5	D
V_{C_2}/V_{max}	–	–	0.5	0.5
TSV/V_{max}	6	5	6	6

Gain is the ratio between the peak of the fundamental ac voltage and the total voltage of isolated dc sources.

It is worth emphasizing that the advantages of the proposed topologies are more apparent when more levels are generated. Take the nine-level generation as an example, in which the number of cascaded modules required for a classical CHB with a boost converter is four. On the contrary, the proposed ICHB (5L) requires only two cascaded modules to achieve the same number of levels. This implies that it saves 10 power switches, 2 isolated dc sources, and 2 inductors compared to the CHB with a front-end boost converter. In short, the voltage boost function and single-stage power conversion of both the proposed topologies greatly improve the compactness and efficiency of the classical CHB. The proposed topologies are also more compact than the latest boost inverter modules. For a three-level module, each ICHB (3L) saves two diodes compared with [15]. The proposed ICHB (5L) can generate the same number of voltage levels (five-level) as [16] while using significantly lesser components by saving three power switches, one inductor, and one capacitor.

4. Simulation and Experimental Results

For validation, simulations using Matlab Simulink SimPowerSystems toolbox and experimental tests of a prototype depicted in Figure 4 were conducted. The following parameters were considered: V_{dc} = 40 V, C_1 = C_2 = 1000 µF, L = 3 mH, f_o = 50 Hz, f_s = 10 kHz, D = 0.8, load resistance = 100 Ω and load inductance = 100 mH. A power board consisting of silicon carbide power MOSFETs was used to construct the proposed ICHB (3L) and ICHB (5L) according to their schematic, as shown in Figure 1b,1c, respectively. An FPGA was used to implement the PWM scheme presented in Figure 3 and generate switching signals for controlling the inverter.

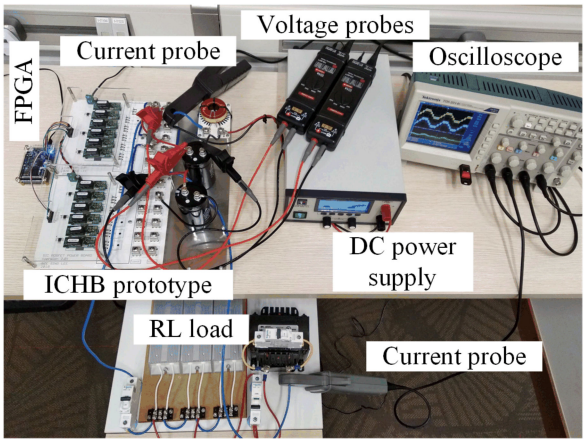


Figure 4. Experimental setup.

The simulation results of the ICHB (3L) depicted in Figure 5a show that the inductor was charged with a constant D of 0.8 that in turn boosted the capacitor voltage of C_1 to 160 V. The maximum voltage level is 200 V. When the capacitor C_2 in the ICHB (5L) achieved natural balancing at 100 V, five symmetrical voltage levels were clearly seen between 200 V and −200 V, as shown in Figure 5b. Figure 5c shows the simulation results of the ICHB (5L) when two modules (n = 2) were considered. The number of voltage levels was extended to nine, and it is obvious that the waveforms in each module were identical, thus confirming the modularity feature of the proposed topology.

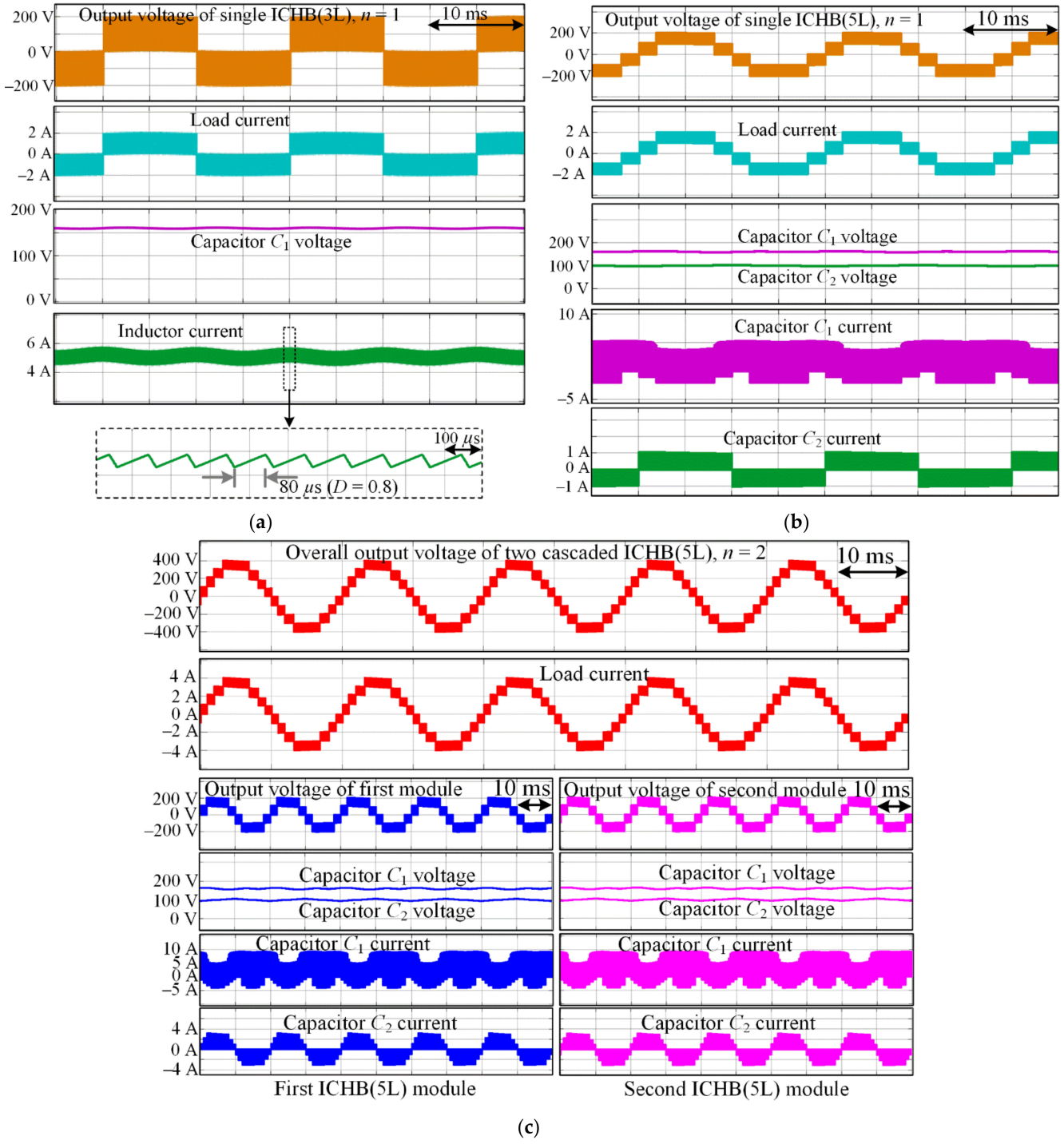


Figure 5. Simulation results of the proposed improved CHB multilevel inverters: (**a**) single module of 3-level topology (ICHB (3L), n = 1), (**b**) single module of 5-level topology (ICHB (5L), n = 1), and (**c**) two cascaded modules of 5-level topology (ICHB (5L), n = 2).

To investigate the advantage of the proposed topology compared to the conventional CHB, an efficiency study was carried out in Figure 6. The efficiency was computed via simulation by modelling the characteristics of power switches and components. For a fair comparison, the same parameters for both the conventional CHB and the proposed ICHB (5L)were considered. As anticipated, the proposed ICHB (5L) exhibited higher efficiency than the conventional CHB. The efficiency improvement increased with power level. This is attributed to a significant reduction in switch and inductor counts by 42% and 50%, respectively, which reduces conduction loss.

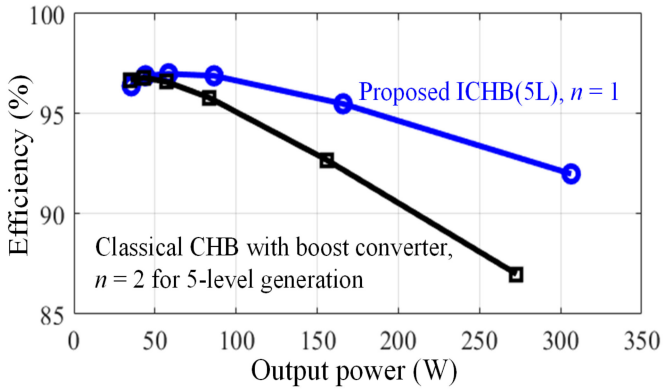


Figure 6. Efficiency of the proposed ICHB (5L) and comparison with the classical CHB for 5-level generation.

For further validation, measurement results from the experimental prototype are presented in Figures 7 and 8. Good agreement is observed between the experimental results and simulations for both ICHB (3L) and (ICHB (5L), thus validating the operation of the proposed topologies. The steady-state response under an *RL* load in Figure 8b and transient response from an *RL* to *R* load in Figure 8c further confirmed the effectiveness of the proposed ICHB (5L).

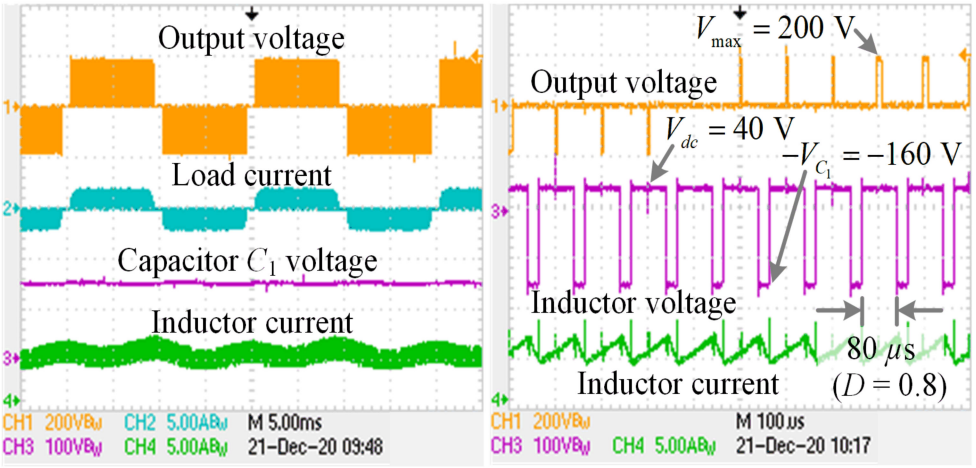


Figure 7. Experimental results of a single ICHB (3L), $n = 1$.

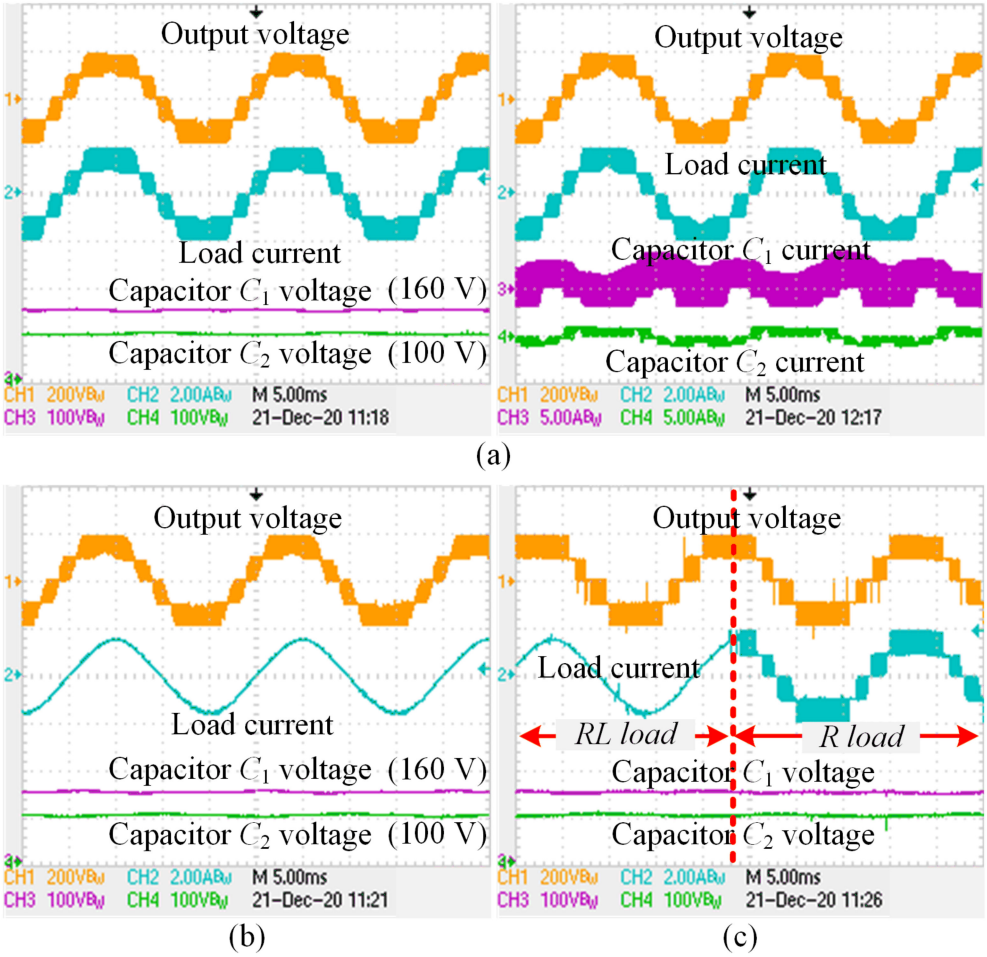


Figure 8. Experimental results of a single ICHB (5L), $n = 1$: (**a**) steady-state response under purely resistive R load, (**b**) steady-state response under series resistive-inductive RL load, and (**c**) transient response.

5. Conclusions

Two improved CHB topologies capable of three-level and five-level generation are proposed in this paper. Without sacrificing the modularity feature of the classical CHB, the superiority of the proposed topologies lies in their compactness and voltage-boosting capability. The three-level topology is developed by reconstruction of the two-stage CHB structure, which encompasses a front-end boost converter and a rear-end H-bridge. The single-stage structure not only saves one switch but also reduces the capacitor voltage stress. When compared to the CHB with the same voltage gain and level generation, the extended five-level topology offers a further reduction in power switch, an isolated dc source, and inductor counts. Moreover, a significant efficiency improvement is guaranteed. Good agreement is found among the theoretical analysis, simulations, and experimental results. The proposed topologies are suitable for renewable energy applications such as micro inverters for PV system.

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