Losses in the Saturated Iron-core Superconducting Fault Current Limiter for VSC-HVDC System

Boyang Shen, Xiaoyuan Chen, Lin Fu, Mingshun Zhang, Shan Jiang, Jie Sheng, Wei Wang, Yujia Zhai, Yupeng Yuan, Shuo Gao, Wafa Ali Soomro, Youguang Guo, Sheng Wang, Chuanyue Li, Xingming Bian, Hongwei Liu, Zhongting Zheng, Chao Li, Runtao Zhang, Yavuz Öztürk, Yi Liu, Jiabin Yang, and Tim Coombs

***Abstract* — This paper presents the loss analysis on the saturated iron-core superconducting fault current limiter (SISFCL) for a VSC-HVDC transmission system. The numerical model of SISFCL as well as its loss calculation on superconducting parts were carried out by the finite-element method (FEM) using the *H*-formulation merged into the commercial package COMSOL. The SISFCL model was established for a practical ±10 kV VSC-HVDC system, and the fault current situation was simulated using the PSCAD with a SISFCL. The capability of fault current limiting was verified using the analysis of electromagnetic characteristics, and the corresponding patterns of magnetic field in the iron-core were studied. During the process of fault current limiting, the instantaneous power losses in the superconducting components were studied with the increasing DC bias current. Even in a DC grid system, results proved there were considerable amounts of losses occurred in the superconducting parts, when the SISFCL encountered the fault currents.**

***Index Terms* — Voltage Source Converter based High Voltage Direct Current (VSC-HVDC), Saturated iron-core superconducting fault current limiter (SISFCL), High-temperature superconducting (HTS) coil, Finite element method (FEM), AC loss.**

(Corresponding author: Xiaoyuan Chen.)

B. Shen, L. Fu, Y. Öztürk, Y. Liu, J. Yang, and T. A. Coombs are with the Electrical Engineering Division, Department of Engineering, University of Cambridge, Cambridge CB3 0FA, U.K. (e-mail: bs506@cam.ac.uk).

X. Chen, M. Zhang, and S. Jiang are with the School of Engineering, Sichuan Normal University, Chengdu 610101, China (e-mail: chenxy44@sina.com).

J. Sheng is with the School of Electronic Information and Electrical Engineering, Shanghai Jiao Tong University, Shanghai 200240, China (e-mail: sjl@sjtu.edu.cn).

W. Wang is with the College of Electrical Engineering, Sichuan University, Chengdu 610065, China (e-mail: weiwangca283@gmail.com).

Y. Zhai is with the College of Electrical and Information Engineering, Hunan University, Changsha, 410082, China (e-mail: yz378@hnu.edu.cn).

Y. Yuan is with the Reliability Engineering Institute, School of Energy and Power Engineering, Wuhan University of Technology, Wuhan 430063, China (e-mail: ypyuan@whut.edu.cn).

S. Gao is with the School of Instrumentation and Optoelectronic Engineering, Beihang University, Beijing, 100191, China (e-mail: shuo_gao@buaa.edu.cn).

W. Soomro and Y. Guo are with School of Electrical and Data Engineering, Faculty of Engineering and IT, University of Technology Sydney, New South Wales 2007, Australia (e-mail: wafa.a.soomro@student.uts.edu.au).

S. Wang and C. Li are with the School of Engineering, Cardiff University, Cardiff CF24 3AA, U.K. (e-mail: WangS9@cf.ac.uk).

X. Bian and H. Liu are with State Key Laboratory of Alternate Electrical Power System with Renewable Energy Sources, North China Electric Power University, Beijing 102206, China (e-mail: bianxingming@ncepu.edu.cn).

Z. Zheng is with Hangzhou Yuhang Company, State Grid Corporation of China, Hangzhou 311100, China (e-mail：448450268@qq.com).

C. Li and R. Zhang are with the Key Laboratory of Smart Grid of Ministry of Education, Tianjin University, Tianjin 300072, China (e-mail: lichao_tju@126.com).

I. Introduction

The VSC-HVDC transmission technology has been playing a key role in the future smart grid and energy system including the renewable energy and energy storage [1, 2]. The VSC-HVDC is capable to deliver bulk power to long-distance networks with minimal power loss, featuring decoupled control of active power and reactive power transmission which overcomes the disadvantages of the traditional Line Commuted Converters based HVDC system (LCC-HVDC). The VSC-HVDC is additionally a suitable solution to the connection of renewable power networks owing to its advantages of coordinating various frequencies and compensating a reasonable amount of reactive power to weak AC systems.

However, if a fault current suddenly occurs in the DC side, the transiting current abruptly increases tenfold within millisecond level, which can easily damage the power electronics devices, and spontaneously, the voltage in DC side sharply decays and thus cause extra faults in the AC side [3]. This could be one of the major factors that resist the VSC-

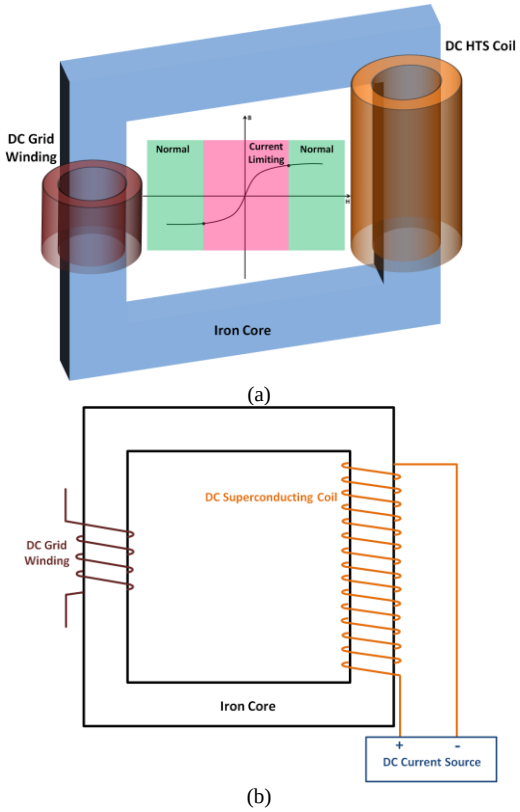

Fig. 1. (a) Configuration of SISFCL for the VSC-HVDC transmission system, (b) Schematic of SISFCL.

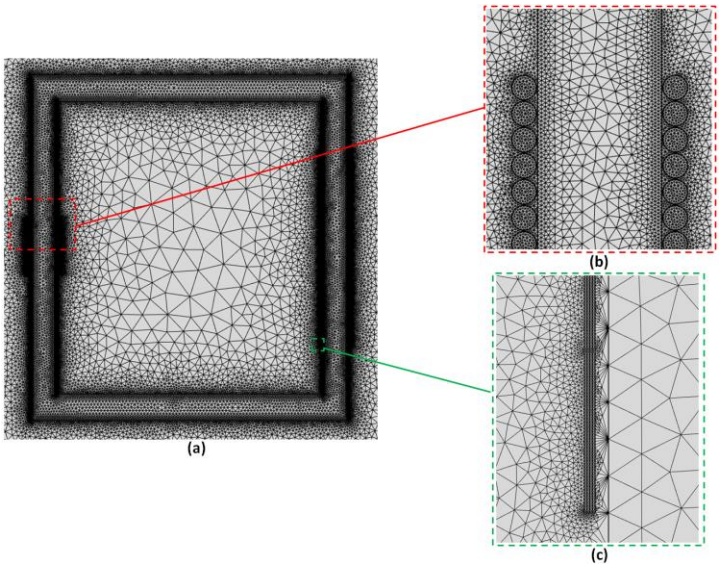

Fig. 2. (a) Mesh of SISFCL designed for the VSC-HVDC system, (b) Zoomed-in domain (red dash area) of (a) to present the details of the DC grid winding, (c) Zoomed-in domain (green dash area) of (a) to present the details of HTS tapes in the DC superconducting coil.

TABLE I. SISFCL MODEL FOR THE VSC-HVDC SYSTEM

Parameters	Value
Inner iron-core width	1000 mm
Outer iron-core width	1200 mm
Inner iron-core height	1100 mm
Outer iron-core height	1300 mm
AC copper winding diameter	122 mm
Copper cable diameter	20 mm
Turns of copper cable	10
Diameter of DC HTS coil	102 mm
HTS tapes turns	300 (60 × 5)
Thickness of superconducting layer	1 μm
Separation of superconducting layer	0.2 mm (between HTS layers)
HTS tape width	12 mm
J_{c0}	4.75×10^{10} A/m^2
E_0	10^{-4} V/m
n (power factor of E-J)	25
μ_0	$4\pi\times10^{-7}$ H/m

HVDC transmission system being intensively used in the modern power system. Therefore, there are several actions have been taken to limit the harm of fault current: positive temperature coefficient resistor, solid state fault current limiter, and superconducting fault current limiter (SFCL). All of them are designed to mitigate the problem that the fault current surge up to an unrecoverable level, and also slow down the voltage drop of DC capacitors. Therefore these devices can protect power electronic devices, and reduce the fault impact on the overall VSC-HVDC system.

The superconducting fault current limiters own the advantages of their fast response facing over-current (usually called quench) and almost zero loss in the normal operation. There have been two typical types of SFCL: the resistive-type SFCL [4], and inductive-type SFCL [5, 6]. The saturated iron-core superconducting fault current limiter (SISFCL) has its unique advantages that the superconducting coil is only to conduct strong DC transport current to saturate the iron-core but on no occasion in quench condition, which overcomes the potential disadvantage of resistive-type SFCL: probable damage of the superconducting coil. Moreover, the SISFCL is accordant to an high voltage transmission systems such as the VSC-HVDC system [7].

In the previous studies, as the resistivity of superconductivity is generally assumed to be zero when carrying a DC current, the power loss in the DC superconducting coil was ignored. However, in these studies of the SISFCL implemented into AC system, authors mentioned that there are losses in the DC superconducting coil, although it only transports DC current, because some of the AC magnetic fields could leak from the iron-cores and penetrate into the DC superconducting coil [8, 9].

However, there is no systematic study to investigate the power losses in the SISFCL designed for the VSC-HVDC system. It is forgettable that the alternating magnetic field will be created when the DC fault current surges to a reasonably high level, namely, in the fault current limiting operation of the SISFCL in the VSC-HVDC system there could be power loss in the DC superconducting coil. That power loss should be analyzed as it could produce the heat on superconducting coil and cause possible early quench, and thus lead to the instability or even the damage of other components in the VSC-HVDC system.

In this paper, a $\pm$10 kV VSC-HVDC system was used as the test environment for the SISFCL model. As shown in Fig. 1, the SISFCL for VSC-HVDC system occupies 3 main parts: the DC grid wilding, the DC bias superconducting coil, and the iron-core. During the normal running, the DC superconducting coil is charged to a reasonably high current level, in order ensure the iron-core is saturated (either left or right green domain in Fig. 1, where the ***B-H*** curve is in the well saturation region and the derivative $d\boldsymbol{B}/d\boldsymbol{H}$ is relatively small). If the fault occurs and the operation point enters the unsaturated region (pink domain in Fig. 1, where the derivative $d\boldsymbol{B}/d\boldsymbol{H}$ is relatively high), there will be a huge inductive impedance generated in the DC grid, which is able to limit the fault current to further increase. By using the FEM method, this article presents the verification of fault current limiting behavior according to the analysis of electromagnetic characteristics, as well as the correlating patterns of magnetic field. The instantaneous power dissipation in the HTS DC coil was studied with the increasing DC current.

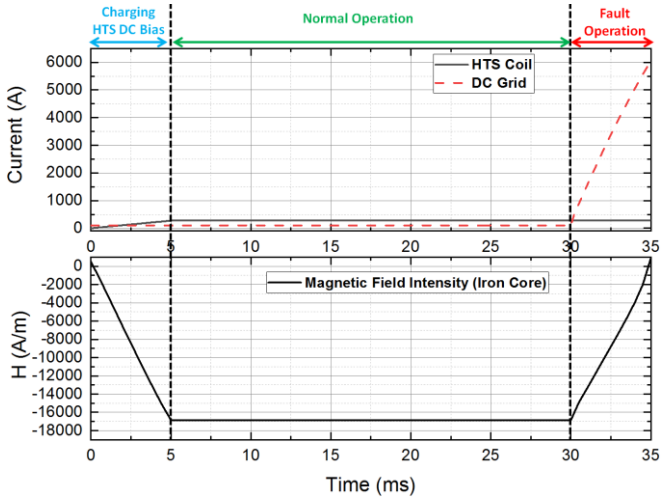

Fig. 3. Operating principle of the fault current limiting behavior of the SISFCL model designed for the VSC-HVDC network. Stage 1 charging the DC bias: A DC bias current charged the DC superconducting coil to maintain a level which can ensure the iron-core entering the deep saturated region, Stage 2 normal operation: the normal running current was in the DC grid and the iron-core was saturated, and there was no impedance in the grid side; Stage 3 fault current limiting: there was a steep fault current surge in the DC grid, a huge opposite magnetic field was produced to repel against the DC bias superconducting coil, and the iron-core returned back to the unsaturated state, and therefore a reasonable inductive impedance was induced in the grid to limit the fault current from further rising.

II. Modeling

A. Modeling of SFCL for the VSC-HVDC system

The real device of the SFCL for VSC-HVDC system is in the presence of 3 dimensions (3D), but the loss calculation in HTS components tends to be a more microscopic analysis. Due to the capability of FEM formulation for HTS, the 3D model has the problems in boundary condition settings, which could cause more errors in the loss calculation. The calculation speed of 3D model should be considered because of the massive numbers of turns in the DC HTS winding and DC grid wind, and the overall large structure.

Therefore, in this study, the 3D model of the SFCL for VSC-HVDC system was simplified into a 2D model of cross-section. It should be noticed the power loss in the actual superconducting coil is different in the cross-sectional model. However, the 2D cross-sectional model shows the worst case and is able to provide an upper limit of the loss in the SISFCL for VSC-HVDC.

The SISFCL model was adapted to a $\pm$10 kV VSC-HVDC system, and the fault condition was modeled by PSCAD. In this article, we used a typical SISFCL size and configuration using 10 turns AC windings. We used the actual dimension of the commercial HTS tapes with the superconducting layer 1 μm thick, and that is good for calculating the loss in the DC superconducting coil with high accuracy. The mesh of the SISFCL is illustrated in Fig. 2. Fig. 2 (b) shows the zoomed-in domain (red dash area) of (a) to present the details of the DC grid winding, Fig. 2 (c) shows the zoomed-in domain (green dash area) of (a) to present the details of HTS tapes in the DC bias superconducting coil. By using the method [10], the electromagnetic characteristic of the material of iron-core was imported to the SISFCL model. TABLE I lists the specific parameters to design the SISFCL model.

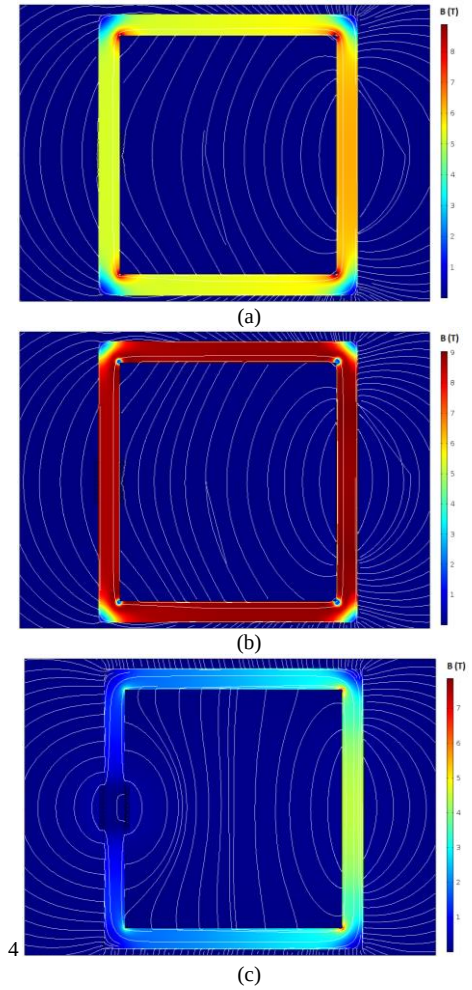

Fig. 4. Magnetic field (corresponding to Fig. 3) in the iron-core in the three stages: (a) Stage 1 charging the DC bias, (b) Stage 2 normal operation (iron-core saturated), and (c) Stage 3 fault current limiting process (iron-core unsaturated).

B. Loss Calculation

The ***H***-formulation on the basis of the Maxwell's equations has been selected as the modeling method: Equation (1) below can be solved by the FEM software COMSOL [11, 12]:

$$\frac{\partial(\mu_0\mu_r \boldsymbol{H})}{\partial t} + \nabla \times (\rho \nabla \times \boldsymbol{H}) = 0 \qquad (1)$$

where the magnetic field intensity is $\boldsymbol{H}$, the resistivity is ρ, the permeability of free space is μ_0, and the relative permeability is μ_r. More details on loss calculation of 2D cross-sectional model for HTS applications can be found in [9].

III. Analysis and Discussion

Fig. 3 presents the operating principle of the fault current limiting behavior of the SISFCL model designed for the VSC-HVDC network. There were 3 stages of the whole procedure. Stage 1 charging the DC bias: A DC bias current charged the DC superconducting coil to maintain a level which generated a strong magnetic field and was able to ensure the iron-core going into the deep saturated region; Stage 2 normal operation: the normal operating current was in the DC grid and the iron-core was saturated, and there was no impedance in the grid; Stage 3 fault current limiting: there was a steep fault current surge in the DC grid, and a tremendous opposite

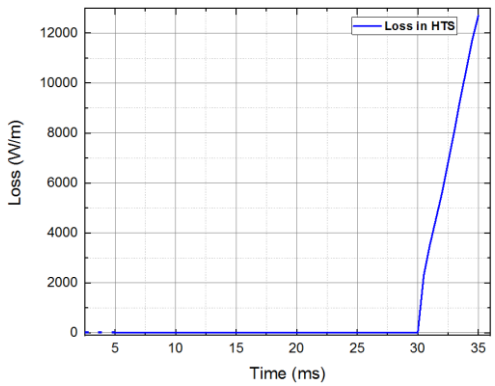

Fig. 5. Corresponding (Fig. 3) instantaneous loss (Watts/meter) per cross-section in the DC superconducting coil, with a DC current 275 A.

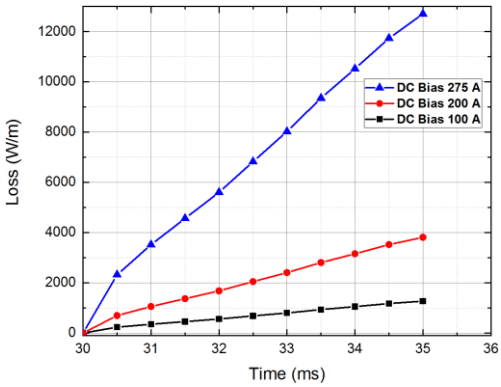

Fig. 6. Instantaneous losses (Watts/meter) per cross-section in the DC bias superconducting coil, with DC current rising from 100 A to 275 A.

magnetic field was generated to repel against the DC bias superconducting coil, and thus the iron-core returned back to the unsaturated state, and therefore a reasonable inductive impedance was induced in the grid to limit the fault current from further rising.

Fig. 4 shows the corresponding (Fig. 3) magnetic field in the iron-core in these three stages. Fig. 4 (a) demonstrates the charging process of the DC bias, and the magnetic field inside the iron-core was mostly uniform but relatively stronger in the right brunch with DC bias superconducting coil. As shown in Fig. 4 (b), in the normal running, the iron-core was saturated, and the magnetic field was almost uniform in the whole core domain. Fig. 4 (c) reveals the magnetic field in fault current limiting stage where it can be seen that the iron-core was no longer unsaturated. In the left brunch with DC grid winding, the total interacting magnetic field decreased to low level (below 0.5 T), and in this occasion tremendous inductive impedance was generated if there was a sharp increasing rate of the fault current.

Fig. 5 presents the corresponding (Fig. 3) instantaneous loss (Watts/meter) per cross-section in the DC superconducting coil. The loss only occurred in Stage 3, during the fault current limiting. Therefore, we focused on the fault period, and assumed the fault current did not change with different DC bias currents. Fig. 6 shows the instantaneous losses (Watts/meter) per cross-section in the DC bias superconducting coil, with DC current rising from 100 A to 275 A. The increment rate of loss with DC bias current 275 A was much higher than those with DC bias currents 100 A and 200 A. The reasons of the loss increasing rapidly with bigger DC bias current could be that the dynamic resistance loss was larger with greater DC current, and the higher DC current created higher magnetic field that added more field dependency and thus induced more loss. Similar phenomenon and discussion can be found in [11].

To conclude, even the SISFCL model is designed for a DC system, but if the VSC-HVDC system encounters a current fault in the DC grid, the huge fault current can generate higher magnetic field in the iron-core, and thus apparently more alternating fields could leak into the HTS components and cause more loss. For instance the case with DC bias current 275 A, if the fault current reaches the peak, the instantaneous loss per cross-section in the DC superconducting coil was 12703 W/m, and if multiplying by the perimeter of DC superconducting coil 0.32 m the overall loss of this SISFCL unit was approximately 4069 W. Although in Section II we mentioned this 2D cross-sectional model provides the worst case, for the real operation kilo Watts level loss will generate heat, and have a non-negligible impact on the stability of cryogenic system, and affect the reliability of SISFCL and VSC-HVDC as well. Therefore, for this SISFCL design a DC bias current around 200 A is recommended.

IV. Conclusion

The modeling of the SISFCL designed for the VSC-HVDC was accomplished using ***H***-formulation implanted into the FEM software COMSOL Multiphysics. The SISFCL model was designed for a practical $\pm$10 kV VSC-HVDC system, and the fault was modeled using PSCAD. The working principle of fault current limiting behavior was verified using the analysis of electromagnetic characteristics by the ***H***-formulation model, and the corresponding variation of magnetic field in iron-core were investigated. Through the process of fault current limiting, the instantaneous power losses in the DC superconducting coil were compared with the different DC currents. Results reveal, even in a DC power system, there were a considerable amount of loss up to kilo Watts level generated from the DC superconducting coil, during the SISFCL suffered a fault current surge. For real operation, the cryogenic system should design to be competent for the maximum loss to secure the safety and reliability of SISFCL and VSC-HVDC system.

References

[1] G. Tang, Z. He, and H. Pang, "Research application and development of VSC-HVDC engineering technology," *Automation of Electric Power Systems*, vol. 37, no. 15, pp. 3-14, 2013.

[2] R. H. Yang, and J. X. Jin, "Unified power quality conditioner with advanced dual control for performance improvement of DFIG-based wind farm," *IEEE Trans. Sustain. Energy*, vol. 12, no. 1, pp. 116-126, 2020.

[3] J. Yang, J. E. Fletcher, and J. O'Reilly, "Short-circuit and ground fault analyses and location in VSC-based DC network cables," *IEEE transactions on Industrial Electronics*, vol. 59, no. 10, pp. 3827-3837, 2011.

[4] M. Noe, and M. Steurer, "High-temperature superconductor fault current limiters: concepts, applications, and development status," *Supercond. Sci. Technol.*, vol. 20, no. 3, 2007.

[5] J. Jin, S. Dou, H. Liu, C. Grantham, Z. Zeng, Z. Liu, T. Blackburn, X. Li, H. Liu, and J. Liu, "Electrical application of high Tc superconducting saturable magnetic core fault current limiter," *IEEE Trans. Appl. Supercond.*, vol. 7, no. 2, pp. 1009-1012, 1997.

[6] J. Jin, S. Dou, H. Liu, and C. Grantham, "Preparation of high Tc superconducting coils for consideration of their use in a prototype fault current limiter," *IEEE Trans. Appl. Supercond.*, vol. 5, no. 2, 1995.

[7] B. Li, F. Jing, B. Li, X. Chen, and J. Jia, "Study of the application of active saturated iron-core superconductive fault current limiters in the

VSC-HVDC system," *IEEE Trans. Appl. Supercond.,* vol. 28, no. 4, 2018.

[8] Y. Jia, M. D. Ainslie, D. Hu, and J. Yuan, "Numerical simulation and analysis of a saturated-core-type superconducting fault current limiter," *IEEE Trans. Appl. Supercond.*, vol. 27, no. 4, 2017, Art. no. 5600805.

[9] B. Shen, C. Li, J. Geng, Q. Dong, J. Ma, J. Gawith, K. Zhang, J. Yang, X. Li, Z. Huang, and T. Coombs, "Investigation on Power Dissipation in the Saturated Iron-Core Superconducting Fault Current Limiter," *IEEE Trans. Appl. Supercond.*, vol. 29, no. 2, 2019, Art. no. 5600305.

[10] M. Zhang, J. Kvitkovic, S. Pamidi, and T. Coombs, "Experimental and numerical study of a YBCO pancake coil with a magnetic substrate," *Supercond. Sci. Technol.,* vol. 25, no. 12, 2012.

[11] B. Shen, C. Li, J. Geng, X. Zhang, J. Gawith, J. Ma, Y. Liu, F. Grilli, and T. A. Coombs, "Power dissipation in HTS coated conductor coils under the simultaneous action of AC and DC currents and fields," *Supercond. Sci. Technol.,* vol. 31, no. 7, 2018, Art. no. 075005.

[12] B. Shen, F. Grilli, and T. Coombs, "Review of the AC Loss Computation for HTS using H formulation," *Supercond. Sci. Technol.,* vol. 33, no. 3, 2020, Art. no. 033002.