A Compact Design Using GaN Semiconductor Devices for a Flying Capacitor Five-Level Inverter

Majid Farhangi*, Yam P. Siwakoti*, Reza Barzegarkhoo*, Saad Ul Hasan*, Dylan Lu* and Dan Rogers**
**Department of Engineering Science, University of Oxford, Oxford, United Kingdom
*School of Electrical and Data Engineering, University of Technology Sydney, Sydney, Australia

***Abstract*—Multilevel inverters (MLIs) based on the flying-capacitor (FC) concept are beneficial in many renewable energy-based applications due to their compactness, low current stress on semiconductor devices, and reasonable thermal behavior for high-power applications. However, the recently developed FC-based topologies suffer from half dc-link voltage utilization and a variable high-frequency common-mode voltage (HF-CMV). The aim of this paper is to propose an FC-based family of MLIs with a five-level (5L) output voltage, full dc-link voltage utilization, and low HF-CMV. Using redundant states and the phase-shifted sinusoidal PWM technique, the value of the flying capacitor has been reduced significantly. The performance of the converter has been verified using Gallium Nitride (GaN) power switches. Circuit description and a brief comparative study with existing MLIs are given to justify the suitability of the topology.**

***Keywords*—Flying capacitor, GaN semiconductor devices, Multilevel inverters, Reduced CMV**

I. Introduction

Flying-capacitor (FC)-based multilevel inverters (MLI) are known as a viable and robust solution for many renewable energy conversion systems. The main features of FC-based MLIs are their applicability in high-power applications owing to their uniform loss distribution, low peak inverse voltage (PIV) across the switches, low current stresses profile of the switches, reasonable capacitance of the FC cells and high reliability. All these features can contribute to a compact design for high-power applications. However, the recent research gap shows that some improvements such as the ability for full-dc-link utilization and reduction in the overall value of the common-mode voltage (CMV) are still necessary to make them more attractive in the industry [1]-[4].

Conventional active-neutral point FC-based MLIs suffer from full-dc-link utilization issue and variable high-frequency CMV. Therefore, many developed structures have tried to integrate the switched-capacitor (SC) technique into this area. Apparently, with such an SC-based integration, the full-dc-link utilization issue can be improved, but with the cost of having an excessive current stresses profile for the capacitive charging loop. The active-boost neutral point clamp (ABNPC)-MLIs are an example of such developed topologies [5]-[6]. Packed U Cell (PUC)-MLIs also have recently emerged and solved the full dc-link voltage utilization shortcomings of the conventional FC-based topologies [7]-[8]. However, some improvements are still needed to reduce its large high frequency (HF)-CMV.

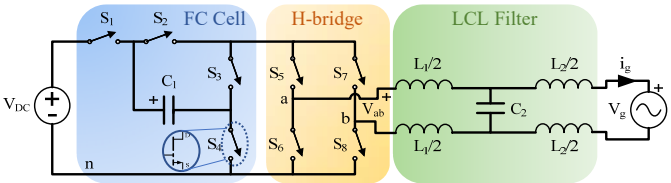


Fig. 1. The schematic of the FC-based 5L inverter.

This paper aims to propose an FC-based five-level (5L)-inverter with the ability of 1) keeping the current stress profile of all the involved switches within the peak of ac output current, 2) full dc-link voltage utilization of the input dc source, 3) reduced capacitance value for the FC cell, 4) reduced value of HF-CMV, and 5) potential for low voltage GaN device application to reduce loss and associated cost.

The working principle of the presented FC-based 5L-inverter is described in Section II. The modulation and FC capacitance determination is discussed in Section III. A brief comparative study is conducted in Section IV, and some simulation and experimental results are presented in Section V.

II. Circuit Topology

The overall circuit schematic of the FC-based 5L-inverter has been illustrated in Fig. 1. The topology is comprised of eight power switches: An FC cell, a typical un-folding H-bridge cell and an LCL output filter. As shown in Fig. 1, the converter is formed by four identical half-bridge (HB) switches. Regarding the shared ground between three out of four identical HB switches, the switch pairs of (S_3, S_4), (S_5, S_6), and (S_7, S_8) can be driven using a single isolated dc-dc power supply for the gate driver. The remaining switch pair (S_1, S_2) needs another isolated dc-dc supply for the gate driver circuit. Due to the shared source connection for six out of eight power switches, the gate driver circuit can be accommodated in a compact area and the overall cost of the converter can be reduced.

Table I: ON-switching states, the FC status, the overall CMV, and the output voltage level of the 5L-FC-based inverter

States	ON Switches	C_1 Status	V_{ab}	CMV
1	S_1, S_2, S_5, S_8	-	V_{dc}	$V_{dc}/2$
2	S_4, S_2, S_5, S_8	Discharging	$V_{dc}/2$	$V_{dc}/4$
3	S_1, S_3, S_5, S_8	Charging	$V_{dc}/2$	$V_{dc}/4$
4	S_4, S_3, S_5, S_7	-	0	-
5	S_4, S_3, S_6, S_8	-	0	-
6	S_4, S_2, S_6, S_7	Charging	$-V_{dc}/2$	$V_{dc}/4$
7	S_1, S_3, S_6, S_7	Discharging	$-V_{dc}/2$	$V_{dc}/4$
8	S_1, S_2, S_6, S_7	-	$-V_{dc}$	$V_{dc}/2$

Table I summarizes the ON switching states of the involved power switches per each output voltage level. The charging/discharging status of the capacitor, and the instantaneous CMV per each output level, have also been included in this table. Herein, the CMV is equal to the following relation:

$$V_{CMV} = \frac{V_{an} + V_{bn}}{2} \quad (1)$$

As indicated in Table I, the maximum output voltage of the 5L-FC-based inverter is equal to the input dc voltage, which is its major advantage in comparison to the conventional eight-switch 5L-FC- based inverter. The topology has been implemented using four high frequency (HF) switches at the FC cell side and four line-frequency switches at the H-bridge cell. The four HF power switches are working as complementary pairs ($S_4 = \overline{S_1}$ and $S_2 = \overline{S_3}$). In this case, both the first positive and first negative output voltage levels can be synthesized by two redundant switching states. Having two redundancies for the middle output voltage level allows charging and discharging the flying capacitor (C_1) at high frequency. Hence, it is naturally balanced at half of the input dc voltage. Also, because of such redundant states (and similar to the conventional FC-based inverters), the required capacitance of the FC side can be reduced significantly for a given ripple voltage and output power without requiring any voltage sensors or closed-loop control operation. Also, unlike the PUC5 [7] and the conventional eight-switch 5L-FC- based inverter [1], the CMV per each output voltage levels is varied with a fraction of full-dc link value (Table II). Such a promising feature can reduce the Electro-Magnetic Interference (EMI) noises and the leakage current in photovoltaic (PV) applications. Similar to the conventional types of 5L-FC-based inverter, the four switches located at the H-bridge side need to block the input dc voltage, while the HF-based switches located in the FC cell withstand half of the input dc voltage. Since the load/grid current is passing through all the power switches in different switching states, the current stresses of all the involved power switches are limited within the peak value of the load current.

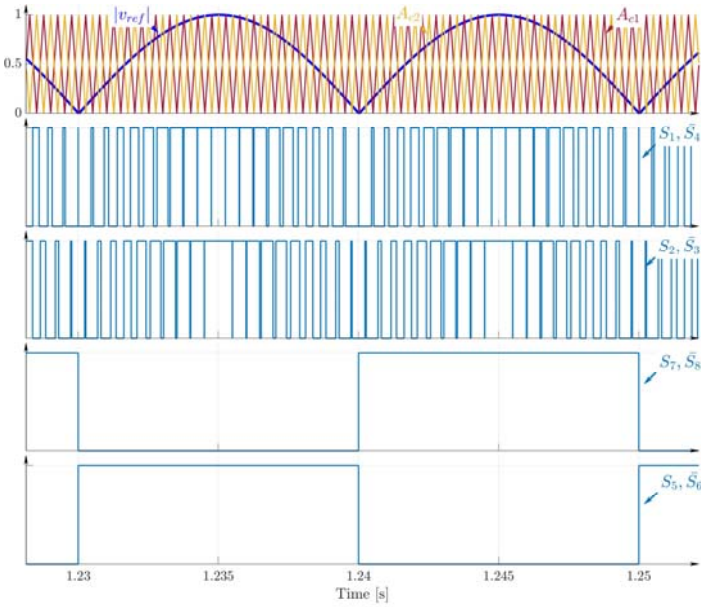


Fig. 2. PS-SPWM and gate switching pulses.

III. Phase-Shifted Modulation and FC Capacitance Determination

Fig. 2 shows the details of the Phase-Shifted Sinusoidal Pulse Width Modulation (PS-SPWM) strategy of the FC-based 5L inverter. Thanks to the paired switches used in this topology, the PS-SPWM technique can double the effective apparent switching frequency at the input of the LCL filter. Herein, two identical phase-shifted carriers with an absolute function of sinusoidal reference waveform $|M\sin(\omega t)|$ have been used, where M represents the modulation index of the PS-SPWM technique.

Considering I_m as the peak value the grid current and ΔV_{ripple} as the maximum allowable ripple voltage across C_1, the following equation can be derived to determine the required capacitance of FC:

Table II. A comparative study among some of the most well-known 5L inverters.

Type of Converter	No. of Switches	No. of Caps	Full-DC Link Utilization	Current Stress within I_m	Maximum PIV (p.u.) (No. of Switches)	Maximum CMV (p.u.)	Ability for Applying PS-SPWM Technique
Standard FC-5L [1]	8	3	NO	YES	1(4)	1	YES
ABNPC [5]	8	3	YES	NO	1(4)	1	NO
ABNPC [6]	6	3	YES	NO	1(4)	1	NO
PUC5 [7]	6	1	YES	YES	1(2)	1	YES
Presented Topology	8	1	YES	YES	1(4)	0.5	YES

$$C_1 = \frac{I_m \Delta t_c}{\Delta V_{ripple}} \tag{2}$$

where, Δt_c is the maximum duration of charging/discharging cycles of C_1 in one switching period. Hence, considering the half value of switching frequency seen by the FC cell switches in the PS-SPWM technique, and regarding (2), the minimum required value of C_1 can be obtained as follows:

$$C_1 = \frac{I_m}{2 f_{sw} \Delta V_{ripple}} \tag{3}$$

Regarding (3) and considering the high switching frequency modulation applied to the GaN switches, a very small value of the flying capacitance can be adopted in practice, which leads to improved power density.

IV. Comparative Study

Table II summarized the salient features and differences of the presented FC-based 5L inverter over the standard eight-switch FC-based 5L inverter in [1], the ABNPC-5L inverters in [5], [6], and the PUC5 inverter in [7]. The comparative items are the number of required active-power switches, the number of required capacitors, the full dc-link utilization ability, the current stress profiles of the switches within the peak value of the load/grid current, the per-unit value of PIV across the switches with the number of switches that should withstand such maximum PIV, the per unit value of CMV, and the ability for applying PS-SPWM technique to reduce the effective switching frequency of the switches. As stated in Table II, the presented converter offers a comparable performance among all the above-mentioned 5L inverters, specifically in reduction of CMV, and full dc-link voltage utilization using a very small flying capacitor. Moreover, although it has used two more switches than the 5L-ABNPC presented in [6], the maximum current stress profiles of all the involved switches are within the I_m.

Table III. Parameters used for analysis and measurements

Element	Type	Description
Power Switches	GS66516	650 V/60 A
Gate Drivers	NCP51820	IC Chip
Isolated DC Supply of Gate Drivers	MTU1S0512MC	dc-dc converter
Microcontroller	TMS320F28379D	DSP
Switching Frequency	100 kHz	-
C_1	MLCC	22 µF
C_2	MLCC	4.4 µF
Filter inductor	Ferrite Core	22 µH

V. Simulation And Experimental Results

To verify the performance of the converter, some simulation and experimental results are presented in this section. Details of the components used in the experimental prototype are summarized in Table III. Fig. 3 shows the prototype with area of 90 mm x 100 mm x 30 mm using GaN switches (GS66516) and gate drivers (NCP51820).

The current and voltage stresses of all switches in a simulation scenario (input voltage of 400 V, 1 kW R-L load) have been illustrated in Fig. 4 (a) and (b), respectively. As can be seen, four high-frequency switches in the FC cell block half of the inverter output voltage, 200 V. The FC voltage and current are also shown.

For the experimental prototype, ten high-energy-density multi-layer ceramic capacitors (MLCCs), each with 2.2 µF capacitance, were incorporated as the FC capacitance. The input voltage is set at 360 V through an Elektro-Automatik (EA) PV emulator (model EA-PSI-9750-12). Fig. 5 (a) shows the FC voltage, the 5L inverter output voltage, and the load current at 880 W, while the dynamic results related to the step

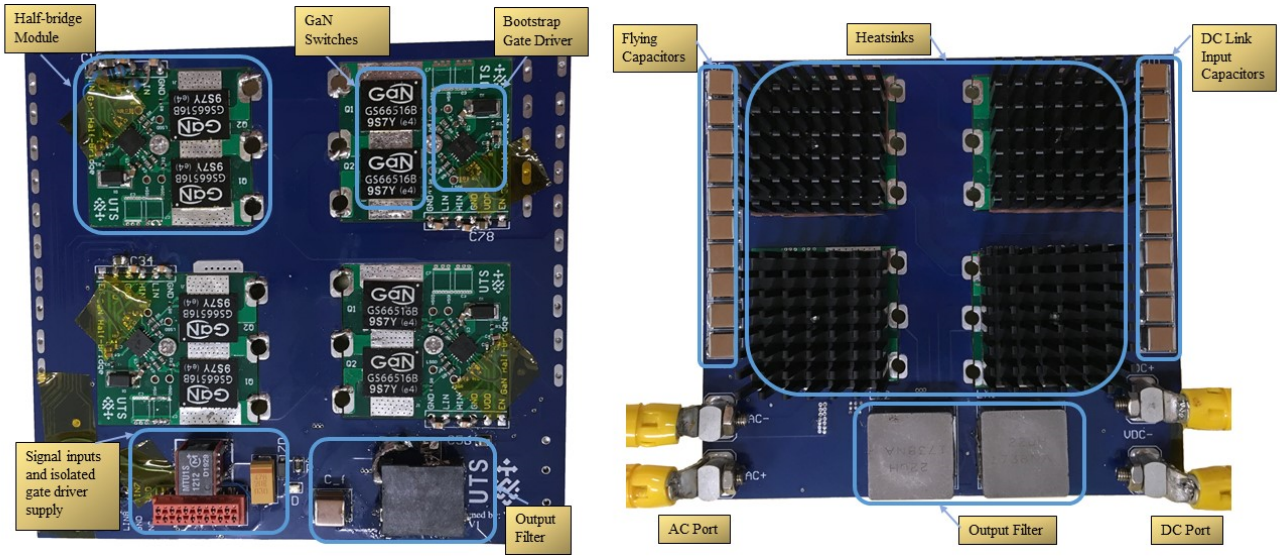


Fig 3: The GaN-based prototype (a) top side (b) bottom side.

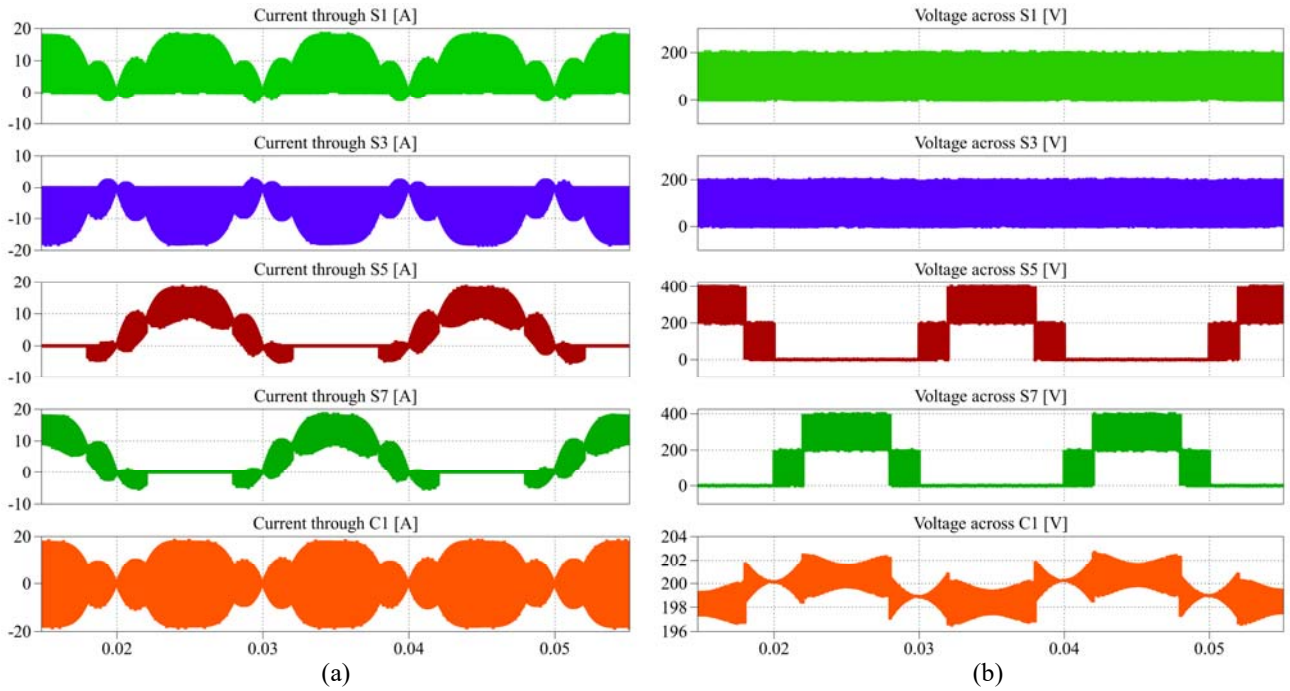
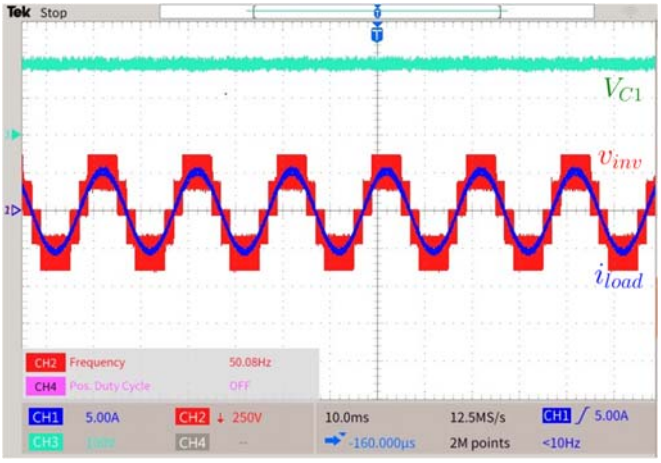


Fig. 4. Simulation results using PLECS (a) current stress of the switches, (b) voltage stress of the switches at 1 kW output power.

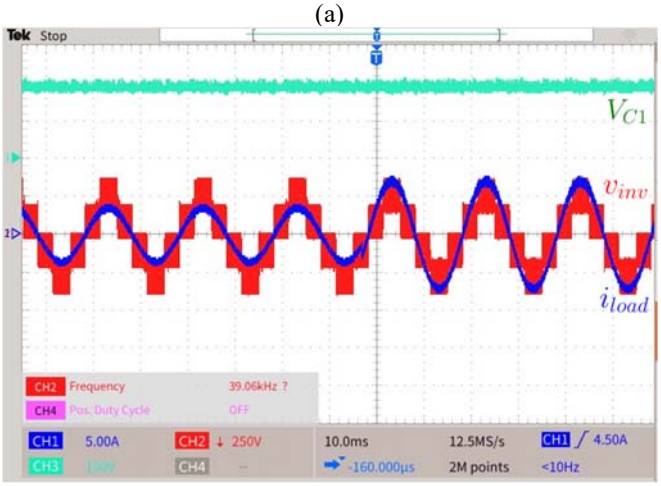
change in load from 500 W to 1 kW and from the modulation index from 0.6 to 0.85 are shown in Fig. 5 (b) and (c). As can be seen, the quality of the inverter output voltage and current waveforms are acceptable using the GaN power switches. Since the PS-SPWM technique has been used to generate the PWM pulses with 100 kHz effective switching frequency, the cluster of higher-order harmonics in the output voltage spectrum is located at 200 kHz. As a result, it can reduce the sizes of filter inductors and the capacitors.

Finally, Fig. 6 shows the experimental results, emphasizing the HF-CMV reduction. In this case, the input voltage is 250 V, while the maximum value of the HF-CMV is 125 V, which is in agreement with the theory presented.

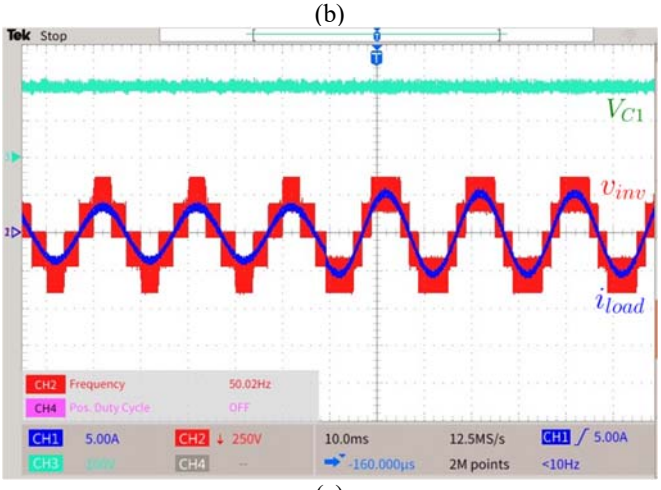
Due to the use of GaN devices, and the low current stress profile of the presented FC-based 5L-inverter, a measured efficiency above 98% was achieved at the full rated power of 1 kW at 100 kHz switching frequency. The maximum case temperature of GaN devices was below 45°C at the rated power.



(a)



(b)



(c)

Fig. 5. Experimental results including the FC voltage (100V/div), and the 5L output voltage of the inverter (250 V/div) with the load current (5 A/div), (a) at 880 W output power and maximum modulation index equals to 0.85. (b) dynamic results from 500 W to 1 kW, (c) step-change results in modulation index from 0.6 to 0.85.

VI. Conclusion

This paper presented a GaN-based structure for an FC-based 5L-inverter with some notable features (full dc-link utilization and reduced value of the overall CMV). The working principle and modulation strategy of the circuit have been introduced. A comparative study and simulation and experimental results have been presented to demonstrate the circuit feasibility and effectiveness.

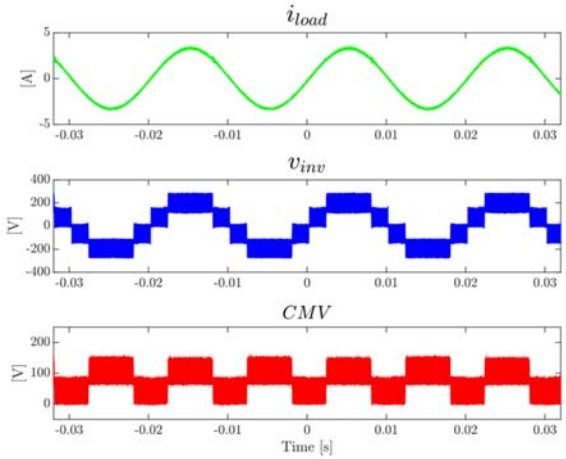


Fig. 6. Experimental inverter output current, inverter output voltage and the HF-CMV at Vin=250 V.

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