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# Switched-Boost Common-Ground Five-Level (SBCG5L) Grid-Connected Inverter With Single-Stage Dynamic Voltage Boosting Concept

Reza Barzegarkhoo\*, Majid Farhangi\*, Ricardo Aguilera\*, Yam P. Siwakoti\*, and Sze Sing Lee\*\*

\*School of Electrical and Data Engineering, University of Technology Sydney, Sydney, Australia

\*\*Department of Electrical Engineering, Newcastle University in Singapore, Singapore.

**Abstract**—Dynamic voltage boosting feature in photovoltaic (PV) grid-integrated application is a necessity to achieve the maximum power point of PV arrays as well as boost the input voltage to the necessary dc-link voltage requirement. Such feature is usually achieved by incorporating a front-end boost or buck-boost dc-dc converter associated with a conventional two or three-level inverter. However, such an integration cannot efficiently meet many IEEE strict grid codes from the power quality, ground leakage current, and the overall efficiency per power density aspects. The aim of this paper is to present a new five-level (5L) inverter with an integrated single-stage dynamic voltage-boosting concept and a common-grounded (CG) feature. As a result, the concern of ground leakage current is addressed through the provided CG feature, whilst both the power quality and overall efficiency of the system are improved with a 5L single-stage boosted output voltage waveform. To confirm the effectiveness of the proposal, apart from the circuit description, some experimental results are also presented.

**Key words:** Common-ground inverters, Dynamic voltage boosting capability, Switched-boost cell.

## I. INTRODUCTION

Grid-integrated systems feeding through renewable energy resources like photovoltaic (PV) arrays demand highly-efficient power converters with an improved performance in injecting the power to the grid and higher overall efficiency. The commercially available solution to target this perspective is to use the bidirectional front-end boost converters associated with a two or three-level inverter. The main merit of such a front-end boost converter is the dynamic voltage boosting ability to capture the maximum power point of the PV panels. It can also decouple the ac ripple component of the input PV panel [1]. Having taken the recent advances of the power-electronics devices into account, such an integration still needs some proper modification in terms of power quality enhancement, power density improvement, and overall efficiency amplification [2].

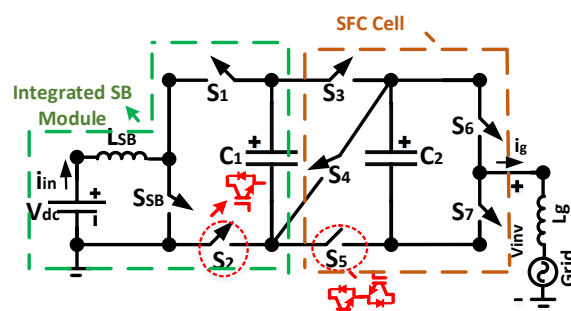


Fig. 1. The proposed SBCG5L-TL inverter.

Single-stage transformerless (TL) inverters with an inherent dynamic voltage-boosting feature and a CG concept have been a popular solution to address most of the IEEE strict grid codes in this area [3]. The dynamic voltage boosting feature can ease the closed-loop control implementation of a single-stage grid-tied system since the converter can inject the power to the grid irrespective of a wide input voltage changes. The CG concept also can address the safety standards associated with detaching the galvanic transformer. It can effectively mitigate the ground leakage current concern, as well. The power quality enhancement and power density improvement can also be obtainable as long as a multilevel output voltage inverter is to be adopted [4]. Regarding such concept, plenty of three-level (3L) [5] and five-level (5L) CG-based TL inverters [6]-[7] with the ability of dynamic voltage boosting feature within a single power processing stage have been reported in the literature. Nevertheless, either their control complexity is still high or more number of passive and active elements are to be employed in their circuit configurations.

In this paper, a new 5L-TL inverter named as switched-boost common-grounded 5L (SBCG5L)-TL inverter is proposed, which possesses the above-mentioned features of a highly-efficient converter. The circuit description, modulation strategy, comparative study and the relevant experimental results are presented to justify the effectiveness of the proposed topology.

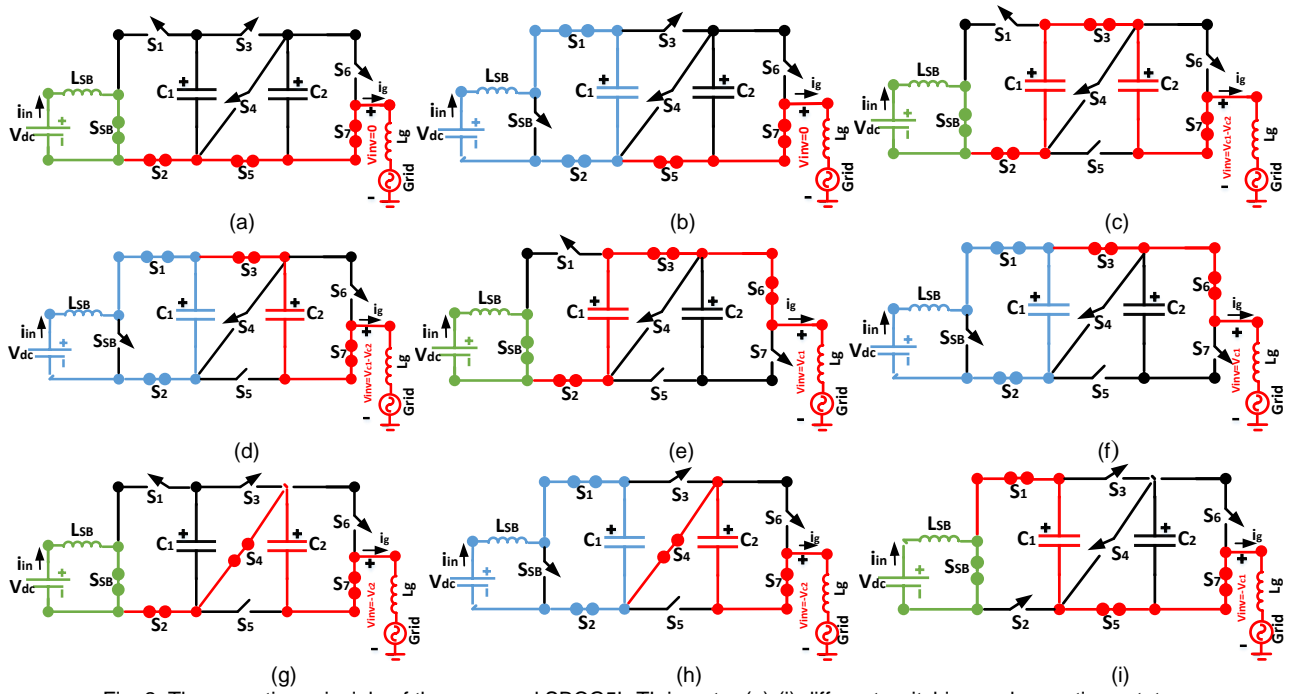


Fig. 2. The operating principle of the proposed SBCG5L-TL inverter (a)-(i) different switching and operations states.

## II. WORKING PRINCIPLES OF THE PROPOSED SBCG5L-TL INVERTER

The overall circuit configuration of the proposed SBCG5L-TL inverter connecting through a simple L-type filter ( $L_g$ ) to the grid with different switching devices realization is illustrated in Fig. 1. As can be inspected, the proposed topology offers a CG feature through a direct connection between the negative terminal of the input dc-source and the neutral point of the grid. Herein, excluding switch  $S_5$  with a bidirectional configuration, all the remaining involved power switches are unidirectional. As can also be observed, the proposed SBCG5L-TL inverter is comprised of an integrated SB module and a switched-flying-capacitor (SFC) cell. The integrated SB module requires one input inductor ( $L_{SB}$ ), three power switches and a single capacitor ( $C_1$ ), whereas the incorporated SFC cell needs a flying capacitor ( $C_2$ ), four unidirectional and one bidirectional switches. Here, through a proper switching conversion of the switches integrated in the SB module,  $C_1$  is balanced at a required boosted voltage value in respect to the dc input voltage ( $V_{dc}$ ). Also, by the help of the grid/load current and such a boosted voltage across  $C_1$ ,  $C_2$  is balanced at the half value of the boosted voltage across  $C_1$  without any additional voltage sensors. Hence, considering  $V_{C1}$ , and  $V_{C2}$ , as the steady state voltages across  $C_1$ , and  $C_2$ , respectively, the proposed topology is able to generate five distinctive boosted output voltage levels as  $\pm V_{C1}$ ,  $\pm V_{C2}$ , and zero within a single-stage energy conversion operation over each fundamental grid frequency.

Fig. 2 (a)-(i) show different switching states and current flowing paths representation of the proposed topology within such a 5L output voltage generation. Excluding the top negative

output voltage level,  $-V_{C1}$ , the operating principle of the proposed SBCG5L-TL inverter is based on two sub-modes per each output voltage level, in which one of such Sub-Modes (sub-mode I) is related to the charging operation of  $L_{SB}$  implied by the green lines, and the other one (sub-mode II) pertains to the charging operation of  $C_1$  highlighted with the blue lines. Herein, the grid current flowing path is determined by the red color. Concerning the ideal condition of all the involved switches and the passive elements, the working principle of the proposed SBCG5L-TL inverter is discussed within nine different switching states as follows:

### A) At the zero-level of the output voltage (Sub-Mode I)

As shown in Fig. 2 (a), the zero output voltage level of the proposed SBCG5L-TL inverter ( $V_{inv} = 0$ ) in both half-cycle is made by the ON-state switching condition of  $S_2$ ,  $S_5$ , and  $S_7$ . Here,  $L_{SB}$  is charged to  $V_{dc}$  through  $S_{SB}$  as implied by the green lines. Hence, the input current ( $i_{in}$ ) is linearly increased with the slope of  $\frac{V_{dc}}{L_{SB}}$ , and both the involved capacitors are disconnected from the input dc-source and the grid.

### B) At the zero-level of the output voltage (Sub-Mode II)

The same zero-level of the inverter output voltage can be continuously made through the ON-state switching path of  $S_2$ ,  $S_5$ , and  $S_7$  as shown in Fig. 2 (i). Nonetheless, by turning ON operation of  $S_1$ , and with the help of internal body diode of  $S_2$ , the stored energy of  $L_{SB}$  is transferred to  $C_1$  as illustrated by the blue lines. Therefore, considering  $v_{L,SB}$  as the instant voltage across  $L_{SB}$ ,  $C_1$  is charged to  $v_{L,SB} + V_{dc}$  within a

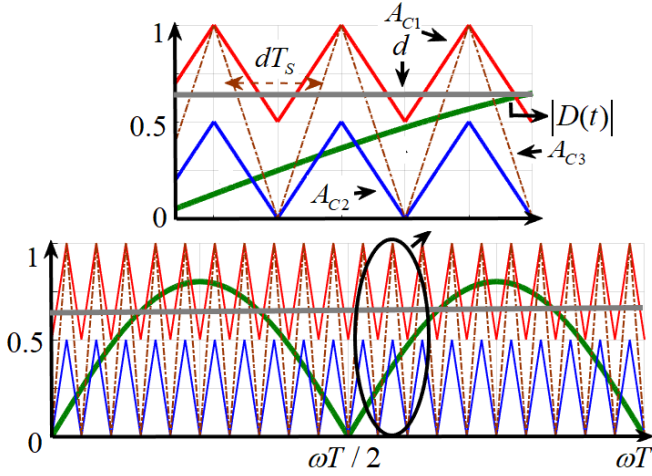


Fig. 3. The principle of maximum-boost LS-SPWM technique.

TABLE I. ON-SWITCHING STATES OF THE PROPOSED SB/QSBCG5L-TL INVERTER WITHIN THE PROPOSED LS-SPWM/DB3CS TECHNIQUE

$D(t)$ POLARITY	MODULATION CONDITION	ON-SWITCHING STATES	$v_{inv}$
POSITIVE	$ D(t)  \geq A_{C1} \& d \geq A_{C3}$	$S_2, S_3, S_6, S_{SB}$	$V_{C1}$
	$ D(t)  \geq A_{C1} \& d \geq A_{C3}$	$S_2, S_3, S_6, S_1$	$V_{C1}$
	$A_{C2} \leq  D(t)  < A_{C1} \& d \geq A_{C3}$	$S_2, S_3, S_7, S_{SB}$	$V_{C1} - V_{C2}$
	$A_{C2} \leq  D(t)  < A_{C1} \& d \geq A_{C3}$	$S_2, S_3, S_7, S_1$	$V_{C1} - V_{C2}$
NEGATIVE	$ D(t)  \geq A_{C1} \& d \geq A_{C3}$	$S_1, S_5, S_7, S_{SB}$	$-V_{C1}$
	$ D(t)  \geq A_{C1} \& d \geq A_{C3}$	$S_2, S_4, S_7, S_{SB}$	$-V_{C2}$
	$A_{C2} \leq  D(t)  < A_{C1} \& d \geq A_{C3}$	$S_2, S_4, S_7, S_1$	$-V_{C2}$
POSITIVE/ NEGATIVE	$ D(t)  < A_{C2} \& d \geq A_{C3}$	$S_2, S_5, S_7, S_{SB}$	0
	$ D(t)  < A_{C2} \& d \geq A_{C3}$	$S_2, S_5, S_7, S_1$	0

negative slope of  $\frac{V_{dc}}{L_{SB}}$  for  $i_{in}$ , while  $C_2$  is disconnected from both the grid and the input dc-source. Having taken both the Sub-Mode I and Sub-Mode II into account, and concerning  $d$  as the fixed dc duty cycle of the integrated SB module over the switching time,  $T_s$ , a volt-second-balance principle can be applied to  $L_{SB}$ . Hence, the steady state voltage across  $C_1$  can be written as follows:

$$V_{C1} = \frac{V_{dc}}{1-d} \quad (1)$$

C) *At the first positive-level of the output voltage (Sub-Mode I)*

The first positive-level of the output voltage is made by the aim of both the involved capacitors' voltages and the ON state contribution of  $S_2, S_3$ , and  $S_7$  as illustrated in Fig. 2 (c). Hence, the output voltage of the proposed inverter will be equal to  $v_{inv} = V_{C1} - V_{C2}$ . Regarding the direction of the grid current ( $i_{in}$ ) as for the unity power factor (UPF) condition, and considering the same charging principle of the  $L_{SB}$  for operation in the Sub-Mode I,  $C_1$  is discharged, whereas  $C_2$  can be charged to the steady-state middle level output voltage value of the inverter with the help of grid-impedance.

D) *At the first positive-level of the output voltage (Sub-Mode II)*

As depicted in Fig. 2 (d), the same output voltage level ( $v_{inv} = V_{C1} - V_{C2}$ ) can be continuously generated, while  $C_1$  is charged to the desired boosted value expressed in (1) during the

operating in Sub-Mode II. It is apparent from the blue-lines of Fig. 2 (d) that such charging operation of  $C_1$  is accomplished by the aim of ON state switch  $S_1$  and the internal body diode of  $S_2$  in the integrated SB module, while other ON state switches such as  $S_2, S_3$ , and  $S_7$  are involved in the grid current flowing path to generate the desired output voltage level.

E) *At the top positive-level of the output voltage (Sub-Mode I)*

Top positive output voltage level of the proposed inverter is the boosted voltage across  $C_1$  ( $v_{inv} = V_{C1}$ ), which has to be converted to the output by the aim of  $S_2, S_3$ , and  $S_6$  as shown in Fig. 2 (e). Similar to the previous operating principle of the proposed topology in Sub-Mode I,  $L_{SB}$  can be again charged to  $V_{dc}$  with the ON state contribution of  $S_{SB}$  over  $dT_s$  switching time interval. Here,  $C_2$  is disconnected from both the grid and the input dc source.

F) *At the top positive-level of the output voltage (Sub-Mode II)*

The charging operation of  $C_1$  can also be established as shown in Fig. 2 (f), while the top positive level of the output voltage ( $v_{inv} = V_{C1}$ ) is generated. Regarding the operating principle of the proposed topology within switching operation in Sub-Mode II, the ON state contribution of  $S_1$  and the internal body diode of  $S_2$  can facilitate the charging operation of  $C_1$  in this case.

G) *At the first negative-level of the output voltage (Sub-Mode I)*

As shown in Fig. 2 (g), the first negative-level of the inverter output voltage ( $v_{inv} = -V_{C2}$ ) is generated by the sole contribution of  $C_2$  in the grid-current flow path. Here,  $S_2, S_4$ , and  $S_7$  must be ON, while considering a UPF condition of the injected grid current,  $C_2$  is discharged via the grid impedance. The ON-state contribution of  $S_{SB}$  in the integrated SB module can also complete the charging operation of  $L_{SB}$  within switching operation of the converter in Sub-Mode I. Considering the switching operation of the proposed inverter in both the first positive and first negative output voltage levels and regarding a Kirchhoff's Voltage Law, the steady-state voltage of  $C_2$  can be determined by the following expressions:

$$V_{C2} - V_{C1} + L_g \frac{di_{c,2+}}{dt} + v_g = 0 \quad (2)$$

$$V_{C2} + L_g \frac{di_{c,2-}}{dt} + v_g = 0 \quad (3)$$

where,  $v_g$  is the grid voltage and  $i_{c,2+}$  and  $i_{c,2-}$  are related to the current passing through  $C_2$  during the generation of the first level of the output voltage in the positive and negative half cycle, respectively. Hence, considering the ampere-balanced principle for  $C_2$  and regarding the same switching duration for the positive and negative cycle, the balanced voltage of  $C_2$  can be obtained as follows:

$$V_{C2} = \frac{V_{C1}}{2} = \frac{V_{dc}}{2(1-d)} \quad (4)$$

H) *At the first negative-level of the output voltage (Sub-Mode II)*

Similar to previous switching operation of the proposed SBCG5L-TL inverter during the Sub-Mode II, the first negative level of the output voltage can be again generated, whereas

Table II. A comparison between the proposed topology and some recently proposed TL 5L-inverter with CG concept.

Type of Converter	No. of Components				Max No. of ON-Switches	Presence of DC offset	Charge Balancing Requirement	Type of Gain	Soft Charging Capability
	S	D	C	L					
CG-SC-based [4]	7	2	4	1	3	YES	NO	Static	NO
CG-SB-based [6]	10	-	3	2	4	NO	YES	Dynamic	YES
CG-SB-based [7]	14	-	3	2	6	NO	NO	Dynamic	YES
<b>Proposed SBCG5L</b>	<b>9</b>	<b>-</b>	<b>3</b>	<b>2</b>	<b>4</b>	<b>NO</b>	<b>NO</b>	<b>Dynamic</b>	<b>YES</b>

Table III. Parameters Used for Analysis and Measurements.

Element	Type	Description
Power Switches	UJ4C075018K4S	750 V/80 A
Gate Drivers	UCC21520DW	IC Chip
Isolated DC Supply of Gate Drivers	MGJ1D051505MPC	IC Chip
Microcontroller	DSP	TMS320F28379D
Switching Frequency	50 kHz	-
C <sub>1</sub> and C <sub>2</sub>	Film Capacitor	0.94 and 0.68 mF
SB Inductor	Ferrite Core	300 uH

$C_1$  is charged to  $v_{L,SB} + V_{dc}$  with the help of  $S_1$  and the internal body diode of  $S_2$  as shown in Fig. 2 (h).

*l) At the top negative-level of the output voltage (Sub-Mode I)*

As illustrated in Fig. 2 (i), the top negative level of the output voltage ( $v_{inv} = -V_{C1}$ ) can be made with the sole contribution of  $C_1$  and the ON-state aims of four power switches as  $S_1$ ,  $S_5$ ,  $S_7$ , and  $S_{SB}$ , while  $C_2$  is disconnected from both the grid and the input dc-source. Here,  $L_{SB}$  is charged to  $V_{dc}$ , whereas operation of the proposed topology within the Sub-Mode II is not possible during this output voltage level since to convert the boosted voltage across  $C_1$  to the output with the negative polarity, the status of switch  $S_{SB}$  must be always ON.

Regarding the above-mentioned working principle of the proposed SBCG5L-TL inverter, the following remarks can be stated:

*i)* The proposed SBCG5L-TL inverter can generate all the desired 5L of the output voltage with an adjustable boosted peak value of  $V_{dc}/1 - d$ . Hence, with a wide range of input voltage changes, the peak of inverter output voltage can be remained fixed within a 5L desired waveform. By the dynamic adjustment of  $d$  over a grid fundamental cycle, the Maximum Power Point Tracking (MPPT) operation of the PV-based TL-inverter can also be possible within a single-stage energy conversion platform.

*ii)* Both the involved capacitors of the proposed SBCG5L-TL inverter are self-balanced over a full grid fundamental cycle without any need of complex voltage balancing procedure.

*iii)* Owing to the incorporated boosted inductor in the SB-module, the current stress profile of all the switches that are involved in the charging path of  $C_1$  is limited to a permissible input current range. Alternatively, all the involved switches of the SFC cell can only experience the stress of the

injected grid current since the charging/discharging operation of  $C_2$  is fully soft with the help of grid current.

*iv)* All the positive and negative output voltage levels are made by the contribution of the capacitors' voltages. Hence, the dc-offset problem associated with most of the available CG-based TL-inverters can be removed.

*v)* Per each output voltage level, less than 50% of the involved switches (only four out of nine) must be ON at the same time. Also, depending on different values of  $d$  (less or greater than 0.5), the input current waveform can possess a Continuous Control Mode (CCM) operation over a wide range of fundamental grid frequency cycle. All these mentioned features can contribute to a significant reduction in the overall conduction losses of the proposed SBCG5L-TL inverter.

*vi)* The peak inverse voltage (PIV) of the switches, which corresponds to the maximum OFF-state drain-source voltage value of the switches can also possess an acceptable value as summarizing in (5) and (6):

$$V_{S,i} = \frac{V_{dc}}{1-d} \quad i = SB, 1, 2, 3, 4 \quad (5)$$

$$V_{S,j} = \frac{V_{dc}}{2(1-d)} \quad j = 5, 6, 7 \quad (6)$$

### III. MODULATION STRATEGY

As it has been discussed, all the integrated capacitors in the proposed SBCG5L-TL inverter are self-balanced. Therefore, the only controllable variable in grid-connected condition of the proposed TL-based inverter is the injected grid current,  $i_g$ . There have been plenty types of control strategies that can govern the proposed system in injecting the power to the grid. The output of these controllers is a sinusoidal reference duty cycle,  $D(t)$ , which should be sent to a level-shifted sinusoidal pulse width modulator (LS-SPWM). To control the required range of voltage boosting operation, the dc duty cycle of  $d$ , should also be taken into account in LS-SPWM. The details of such an LS-SPWM strategy has been illustrated in Fig. 3, where three LS carriers of  $A_{c1}$ ,  $A_{c2}$ , and  $A_{c3}$  are used to be compared with the instantaneous values of  $D(t)$  and  $d$  per each switching time,  $T_s$ . Regarding this operation and the working principles of the proposed SBCG5L-TL inverter, the ON switching states per each output voltage level can be deduced from Table I.

### IV. COMPARATIVE STUDY

A comparison between the proposed SBCG5L-TL inverter and those 5L-TL inverters presented in [4], [6] and [7] is conducted as tabulated in Table II. The comparative items are the number of switching devices and passive elements including the input

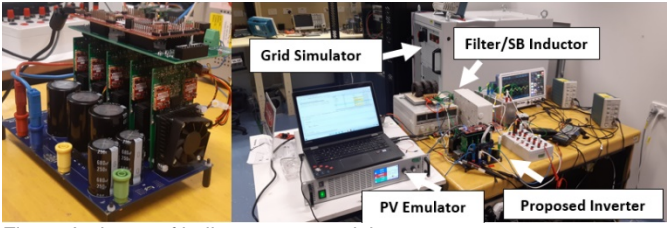


Fig. 4. A picture of built prototype and the measurement setup.

capacitor for PV application and the extra inductor for a simple L-Type filter, maximum number of ON state switches per each output voltage level, the presence of dc offset in the output voltage of the inverter, capacitors charge balancing requirement, type of output voltage gain with respect to the available input voltage, and the possibility of soft charging operation, which can reflect the amount of current stress passing through the switches. Herein, the structure proposed in [4] is a switched-capacitor (SC)-based 5L-TL inverter with an static voltage gain of two, whereas, both the 5L CG-based TL inverter topologies presented in [6] and [7] are based on single-stage SB technique. As can be realized from Table II, the proposed topology requires the least number of switching devices in compare to [6] and [7], while it can offer a dynamic voltage boosting gain which is not the case in the presented SC-based CG-TL inverter of [4].

## V. EXPERIMENTAL RESULTS

To further evaluate the performance of the proposed SBCG5L-TL inverter in the grid-connected condition, some experimental results are presented in this section. Fig. 4 shows the 1.5 kW laboratory-built prototype with the measurement setup, while the details of used components in the prototype has been tabulated in Table III. The 50 Hz grid-voltage is also generated by a four-quadrant grid-simulator REGATRON TC30.528.43-ACS, where the grid peak voltage is adjusted to be 311 V throughout the experiment. To connect the proposed inverter to the grid, an L-type filter with value of 3.8 mH and is utilized. Regarding the integrated-boosting property of the proposed SBCG5L-TL inverter, the input voltage is set at 120 V, while the peak of 5L inverter output voltage is supposed to be 400 V with a dc duty cycle of 70% as per (1). Regarding the SiC power switches used in the prototype, a 50 kHz switching frequency is chosen. Taking Table I into account, the required gate switching pulses have also been provided using the DSP with the model number of TMS320F28379D. A peak of 9 A as for the reference current has also been chosen to inject 1.5 kW active power to the grid. The controller is based on a simple proportional-resonant (PR) action.

Considering the above-mentioned notions, the grid voltage, the injected grid current, the 5L inverter output voltage, and the voltage across  $C_1$  and  $C_2$  have been shown in Fig. 5 (a) and (b). As can be seen, through the proper balanced voltage of the capacitors, e.g. 400 V, 200 V as for the voltage across  $C_1$  and  $C_2$  respectively, all the 5L output voltage with a quality injected grid current are generated, whereas the maximum output voltage of the inverter is 400 V reflecting the integrated voltage boosting feature of the converter.

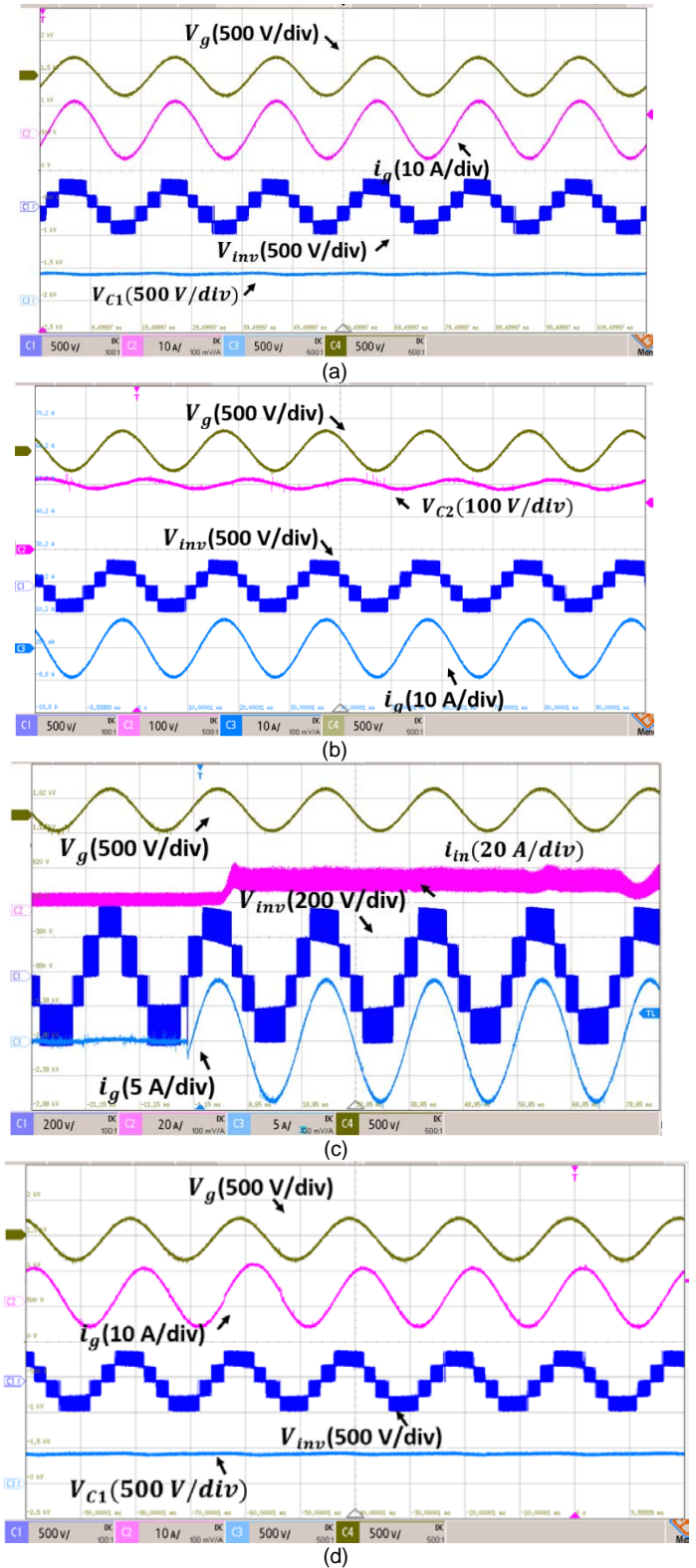


Fig. 5. Experimental waveforms of the proposed SBCG5L-TL inverter in the closed-loop grid-tied condition showing the grid voltage, the injected grid current, and 5L inverter output voltage at 1.5 kW injected power (a) with the voltage across  $C_1$  (b) with the voltage across  $C_2$ , (c) with a dynamic condition from zero to 1.5 kW injected power, and (d) within a lagging reactive power support mode and 1.3 kW apparent power.

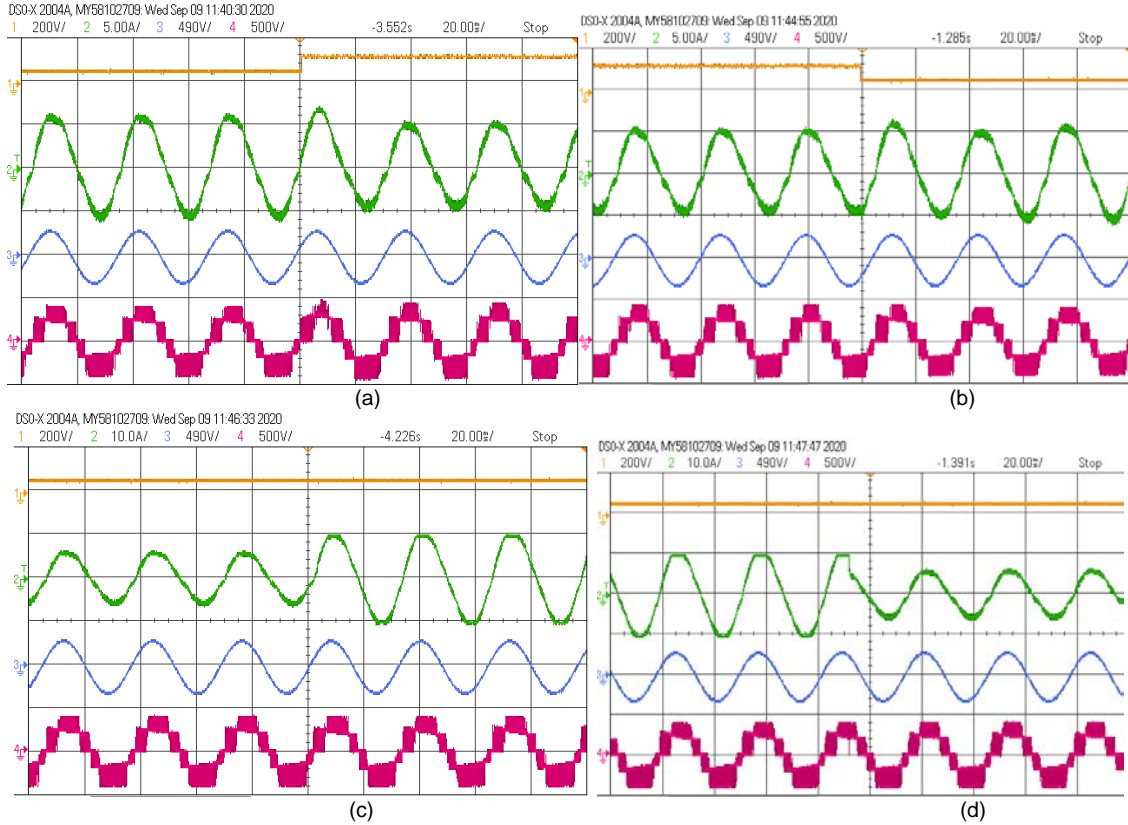


Fig. 6. Real time measurement results showing the input voltage (yellow trace), injected grid current (green trace), grid voltage (blue trace), and the 5L-inverter output voltage (red trace) during the dynamic operation (a) when the input voltage is changed from 80 V to 150 V, (b) when the input voltage is changed from 150 V to 80 V, (c) when the amplitude of the reference current is changed from 5 A to 10 A (d) when the amplitude of the reference current is changed from 10 A to 5 A.

To attest the acceptable dynamic performance of the proposed converter, a step change from zero to full rated power in the reference current is applied. The robust performance of the proposed SBCG5L-TL inverter with its associated closed-loop controller can be confirmed through the obtained results shown in Fig. 5 (c), while the input current is free from any large inrush current as opposed to other available CGSC-based TL inverter with static voltage gain technique. Alternatively, the reactive power support performance of the proposed system in lagging injected grid current conditions have been shown in Fig. 5 (d). In this case, the converter could inject around 1.3 kVA apparent power to the grid.

To show the accurate performance of the proposed topology from dynamic condition viewpoint, some additional measurement results obtained from the real-time simulation OPAL-RT platform are shown in Fig. 6. Considering this, the input voltage value is intentionally changed from 80 V to 150 V, in both directions. The aim of this test is to maintain a 400 V fundamental value for the output voltage of the proposed inverter. Hence, the duty cycle of integrated SB module should be able to change from 80% (for input voltage 80 V) to 62.5% (for input voltage of 150 V). As can be seen from Fig. 6 (a) and (b), all the desired 5L output voltage can be generated irrespective of a wide range of input voltage changes. The stable performance of the proposed system while the input

voltage is set at 80 V, and the peak of reference current is changed from 5 A to 10 A (peak value) in both directions, can also be seen in Fig. 6 (c) and (d), respectively.

## VI. CONCLUSION

A novel 5L single-stage boost inverter with a common-grounded feature is presented in this paper. The proposed topology requires less components in comparison to the recently developed 5L-TL inverters with the same switched-boost concept. The dynamic voltage-boosting feature of the proposed topology makes it an applicable choice for PV-grid-tied application. The details of the proposed inverter operation has been discussed. Finally, a laboratory-built prototype of 1.5 kW injected power to the grid is demonstrated to show the circuit feasibility and effectiveness of the proposed topology.

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