UTS UNIVERSITY OF TECHNOLOGY SYDNEY

Design of Miniaturized On-Chip Passive Circuits in Silicon-Based Technology for 5G Communications

by Zeyu Ge

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under the supervision of

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Certificate of Authorship/Originality

CERTIFICATE OF ORIGINAL AUTHORSHIP

I, Zeyu Ge declare that this thesis, is submitted in fulfilment of the requirements for the award of Doctor of Philosophy, in the Faculty of Engineering & IT at the University of Technology Sydney.

This thesis is wholly my own work unless otherwise referenced or acknowledged. In addition, I certify that all information sources and literature used are indicated in the thesis.

This document has not been submitted for qualifications at any other academic institution.

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Abstract

In any given wireless communication system, the RF filter is an indispensable device. This is especially true for the RF front-end module, which is designed to process the selecting frequency band for different RF signals, and reduce any spurious items in the transmitter and receiver chain and interference signals outside the whole transceiver system. As far as on-chip filtering solutions are concerned, recently devised solutions mainly concentrate on different types of semiconductor processes, namely gallium arsenide (GaAs), and silicon-based ones, such as CMOS and silicon germanium (SiGe). In this research, some fundamental design challenges, especially device miniaturization, will be fully addressed through some novel design methodologies. To explain the low-cost requirements for both prototyping and mass production, a silicon-based technology is used. Consequently, the designs presented in this thesis may be suitable for some high-performance on-chip transceiver systems. In this thesis, designed miniaturized on-chip passive filters in silicon-based technology will be presented. Both BSF and BPFs are implemented and characterized in the mm-wave frequency region. Three unique design approaches will be presented.

The first approach is used to design an on-chip absorptive BSF in a 0.13-μm complementary metal-oxide-semiconductor CMOS technology. Taking advantage of metal stack-up provided in this technology, this design utilizes a two-path transversal configuration in a multi-layer structure. It consists of a direct transmission line (TL) for the main path and two lossy edge-grounded spiral-shaped resonators. The TL is implemented in the top-most metal layer, namely TM2, while the resonators are implemented in a layer below TM2, known as TM1. They are coupled with each other through a broadside-coupled structure. Using this approach, a 24.5-GHz BSF is designed and it has a 10-dB-attenuation-referred absolute bandwidth of 1.54 GHz and maximum attenuation 23.1 dB. The maximum power attenuation level in the pass band region is 0.95 dB at 60 GHz and the size excluding pads is 0.316 × 0.12 mm². A good

agreement between simulated and measured results is obtained. The performance of this design can be considered for some systems which are isolator-less mm-wave transceivers.

The second approach serves to design a wideband BPF also based on a broadside-coupled structure. The design strategy for this work is that a highpass-type filtering response is obtained through a structure that is implemented by TM2, and an upper stopband frequency response is achieved by the bottom layer when the two structures are coupled. Consequently, a composite overall quasi-elliptic-type wide-band BPF functionality can be obtained. Using this approach for BPF design, a wideband 34.5-GHz BPF is devised. It has a 3-dB absolute bandwidth equal to 21.1 GHz and the minimum in-band insertion loss is 1.6 dB which is 0.264 × 0.124 mm^2 in size. This design is suitable for miniaturized broad-band RF transceivers when compared with previously published literature.

The final part of this work is an investigation of wideband BPF design using 3-D lumped inductors. In contrast to conventional studies that have been published in the literature, the approach presented here utilizes parasitic capacitances from the implemented 3-D inductor to introduce a transmission-zero (TZ) at upper stopband. For the purpose of proof-of-concept, a BPF prototype is designed and implemented. The on-wafer measurements show that the designed filter operates at center frequency with a 68.5% 3-dB bandwidth. Due to the proposed 3-D inductors, the overall size of the prototype excluding measurement pads is only 0.054 mm^2.

Chapter 1 Introduction

With progress being made in the miniaturization of today's monolithic microwave integrated circuit (MMIC) transceiver systems, devices of a considerably compact size and high performance built on integrated circuits, also known as chipsets, are becoming increasingly accepted as an ideal solution. They offer new kind of wireless communications that can meet the emerging challenges, such as low cost and wideband requirements. Section 1.1 introduces the background of the thesis for both the mm-wave frequency range illustration and compact size of system advantages. Section 1.2 looks at the challenges and motivations behind this thesis from the technology and application points of view. Section 1.3 explains the main objectives and scope of this thesis. For the last, Section 1.4 describes how this thesis is structured.

1.1 Background

1.1.1 5G and Millimeter-Wave

The 5th-Generation New Radio (5G NR) networks are introducing the latest wireless revolution which supports not only significantly faster mobile broadband speeds but also much lower latencies than previous generations. These unique features make many emerging applications feasible. It is now possible to autonomous vehicles which are fully equipped with ultra-wideband and high-speed communication devices, which could safely steer through and maintain awareness of the traffic around them using the 1-ms latency provided by 5G networks. Moreover, billions of Internet-of-Things (IoTs) devices may be adding their data contributions to 5G networks within the next decade, giving people instant access to information about different items and environments around them. Currently, 5G NR mainly employs sub-6 GHz which significantly limits its performance. To reach its full potential, one of the cornerstone technologies required is to develop low-cost and miniaturized RF front-end modules (FEMs) operating at millimeter-wave (mm-wave) frequencies [1-20].

The global 5G system integration market size is expected to reach US$43.7 billion by 2027 [21]. Some countries have pre-defined some spectra for the usage of 5G NR, which is shown in Figure 1.1. The implementation of new 5G NR standards and the use of mm-wave spectrum is expected to be revolutionary and will provide seamless connectivity for an increasing number of users and networked devices. As 5G mm-wave starts to be deployed in low-cost, small-cell networks using massive MIMO antennas to deliver as much as 20 Gbps download rates to users, the great promise of 5G NR mm-wave will become apparent. At that point, there is likely to be an explosion in the number of new applications and deployment scenarios that exploit the new technology.

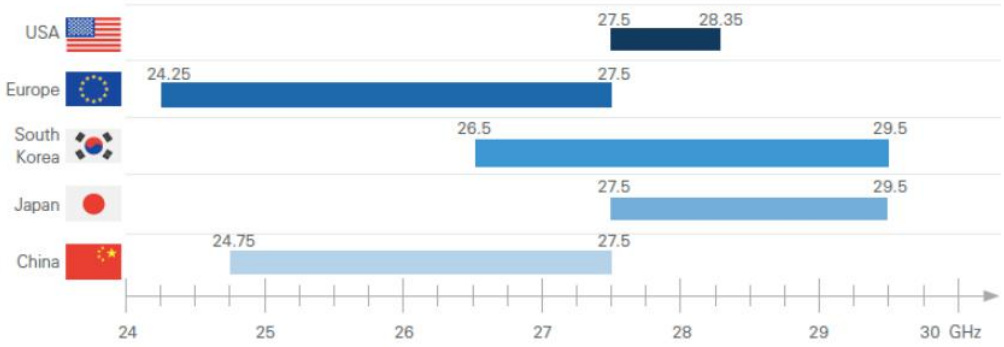


Figure 1.1. The pre-defined mm-wave spectrum for 5G NR. [1]

Additionally, the 5G NR technology will help to safeguard Australian businesses in a fast-growing and rapidly changing digital world. The mm-wave technology will be found everywhere – from the eyes of autonomous vehicles, to ultra-high-speed backhaul links that can match the performance of optical fibers at a fraction of the cost, ultimately providing hundreds of sensors per person, and making the tasks of daily life easier. Therefore, this project will significantly benefit end-users in deploying mm-wave technology for not only wireless industries, but also advanced manufacturing such as Industry 4.0.

Currently, integrated circuits (ICs) are the core components for not only microwave and mm-wave communication systems, but also radar sensing systems. High-performance ICs are playing a critical role in current technology development. People from both academia and industry are looking for solutions to improve the

performance of RF devices operating in the 5G mm-wave bands, especially the increasing demands for device miniaturization and integration. In this scenario, designing high-performance RFIC for a qualified 5G NR mm-wave transceiver is required and must attain a higher level. Moreover, given the diversity of today' applications, some specific RF on-chip devices are needed to accommodate different kinds of application scenarios. Returning to the topic of this thesis, on-chip integrated RF filters, especially with the mm-wave frequency range, new design approaches and innovative electromagnetic (EM) structures are required for on-chip filtering solution implemented in low-cost silicon-based technology.

1.1.2 Filtering Technology Development

Over a century ago in 1915, the German scholar K.W. Wagner designed the first "Wagner filter" with inductors and capacitors as the unit structure [22]. Building on this, the American scientist G. A. Canbell used the image parameter method to conduct a theoretical analysis of the filter design. This invention directly promoted the birth of the first multiplexing system worldwide in 1916. In 1937, W. P. Mason and R. A. Sykes used the *ABCD* matrix to successfully extract the phase parameters and attenuation characteristics of the filter [23]. By the 1950s, the theory and practical application of passive filters had gradually matured. In recent years, with the emergence of many different new materials and the continuous updating of various integration processes, the development of microwave filters has significantly improved. This is especially the case with the emergence of personal computers. The subsequent appearance of various electromagnetic simulation software has reduced the difficulty of filter designs.

Furthermore, a few milestones in the history of filter design should be acknowledged. The American scientist S. B. Cohn deduced the theory of direct coupling resonant cavity filter based on the low-pass prototype structure in 1957 [24]. In 1966, the American scientist Kurzrok and his team introduced cross-coupling into the multi-cavity, and successfully designed the multi-cavity filter [25]. In 1997, the

insertion loss of the filter was introduced and used with polynomial function to characterize filters so that a frequency response could be obtained. In 1999, Cameron invented the cross-coupling method to generate transmission zeros [26]. This analytical synthesis method can achieve the asymmetry in frequency response. In 2000, Amari proposed the non-resonant node technology and used an optimized method to extract the coupling matrix [27]. The biggest advantage of this technology is that the generation of transmission zeros (TZs) does not require cross-coupling of diagonal components. Instead it requires horizontal and vertical components to produce the transmission zero point.

In modern applications, different kinds of RF filter are used to build different systems. Cavity filters are widely used in communication equipment such as base stations because of their very low insertion loss, extremely high Q value and good out-of-band suppression. However, such designs are very difficult to be miniaturized and integrate them with other technologies. Conversely, the low-temperature co-fired ceramic (LTCC) technology can achieve miniaturized designs which are able to be "integrated" with other technologies [28]-[29]. Therefore, it has attracted worldwide attention from industry and academia. However, there are still some disadvantages such like complex processing techniques, large in-band insertion loss and high cost. To further reduce fabrication cost and minimize the physical sizes of the designed filters, development of fully-integrated filters, also known as on-chip filters, has been ongoing in the last decade [30]-[63]. Taking advantage of Moore's law, there are usually multiple metal layers which could be used in any modern silicon-based technologies. In particular, there is at least one thick metal layer that is designed for low-loss microwave circuits [64]-[70]. Moreover, unlike the conventional approach for microwave planar circuits design that usually use distributed elements, such as transmission lines and open/shot stubs, there are lump elements. These include, for example, capacitors and inductors and even transformers, could be used for filter design, which could significantly reduce the physical dimensions of the microwave filter.

Advances in semiconductor and integrated circuit (IC) technologies will play significant roles in developing the complex hardware of these emerging technologies. It is of great interest to establish a low-cost integrated circuit solution for 5G systems, Internet-of-Things module, big data networks technologies and mm-wave enabled radio circuits [71]-[80]. The components for mm-wave enabled circuits and systems are both active and passive, and furthermore traditionally expensive and cumbersome in size. These have garnered the attention of many firms in the semiconductor industry who are developing high-frequency devices, and they need to create a cost-effective, high-performance device with a smaller footprint. The emergence of low-cost mm-wave devices has evolved through research carried out throughout the world. Recent developments of silicon-based technology allow the implementation of low-cost chips which are suitable for a broad consumer market. For instance, the combination of cost-effective CMOS technology that can now operate in the mm-wave frequency band, allowing the design of a high-gain, phase array antenna, strengthens the viability of mm-wave radio communication [71]-[74].

1.1.3 Advanced Semiconductor Technologies

The IC fabrication is a complex and expensive process. The choice of a specific fabrication technology will depend on a number of specification requirements including cost, availability and circuit component capabilities. The technology scaling is another critical factor for IC design. In 1965, Gordon Moore, the co-founder of Intel Corporation, predicted that the number of transistors that would fit in on an integrated circuits chip will double every year. This forecast has held true for more than 50 years [64]-[70]. The key technology concerning this development reflects on the further evolution in the complexity of ICs by building systems in which all the individual components are assembled in circuit blocks. Included here are radio-frequency front-end, RAM/DRAM memory and digital logic, which are incorporated into a single chip substrate. Moore’s Law was an elegant prediction of how an IC has become

smaller and cheaper over the years. Moreover, the law has been used by industries for several decades as they set targets for the development, marketing and sale of their new products. Evidently, the law serves as a driving force for social change and economic growth [66].

Nowadays, semiconductor businesses have successfully demonstrated technology scaling down to the sub-micron level. This has allowed both analog and digital circuits to be integrated on the same substrate [81]-[83]. This began during the 1920s when the active devices could operate at several hundreds of gigahertz in a silicon-based process. It is also around this time when foundries added the specialized feature of utilizing the thick metal layer for the back-end-of-line (BEOL) process [84]-[85]. The introduction of the new material during the BEOL process can help to improve chip performance, especially regarding the RF circuits. Innovations were made to the materials used for both the metal wires and the dielectric insulation in order to meet conductivity requirements and reduce the dielectric permittivity [85].

The twentieth century has witnessed a tremendous amount of technological change and growth, touching and improving the daily lives of people around the world. A good example of this version of Moore's law is the statement that appeared in one prominent business and technology journal, which states that: "Moore's law, celebrated as the defining rule of the modern world, states that the computer chip performance doubles every eighteen months"[15]. However, recently it is thought that Moore's law is expected to no longer be the main driving force for improving IC performance.

1.1.4 Miniaturized Passive Devices

Towards to the end of Moore's law, the full potential of active devices has almost been reached. It is unclear how to further improve the overall performance of RFICs, while the operation frequency being pushed to the mm-wave region. We believe that a possible way to support the high-performance mm-wave RFIC design is to use

passive-inspired strategies. In this thesis, we therefore focus on passive devices design and implementation for mm-wave applications. Passive devices are the main components used in RFICs such as inductors, capacitors and transformers. As their name implies, passive devices are electrical components that do not need any form of electrical power to operate, unlike active devices. Passive devices do not provide gain or amplification but instead, they provide attenuation as they always have gains of less than unity. Passive devices can increase current or voltage by an LC circuit, a series or parallel combination of inductor and capacitor, where they can store electrical energy from a resonant frequency. They can be designed individually or co-designed with other components to build and control complex signals and systems [89]-[96].

It is well known that IC design offers a significant advantage of developing a compact, lightweight design with enhanced performance, high reliability and cheaper manufacturing cost. These are the same for microwave and mm-wave ICs but sometimes the cost of fabrication is compromised. Thus, device miniaturization is very important. Microwave and millimeter-wave circuits can be implemented using either planar or non-planar technologies. Some examples of non-planar circuits are waveguides; these are often used for an application with a high-quality factor, low loss, and high power. On the other hand, planar circuits are popular due to their ease in integration. With the increase in frequencies in mm-wave applications, all metal lines are treated as either distributed- or lumped-elements.

1.2 Challenges and Motivations

This thesis aims to address the challenges incorporated in developing an integrated solution for the emerging technologies on the mm-wave application and the trend toward miniaturization. This thesis aims to explain the recent trend in the industry to design smaller, faster and less expensive electronic passive devices that function very reliably. They should be able to integrate both passive and active components on the same substrates. This thesis presents a methodology that could offer a promising

solution not only in device miniaturization but also a way to minimize the fabrication and packaging cost, which are also key advantages. Also, it diminishes the complexity of the system using higher functional passive silicon integration [80]-[89]. This offers excellent potential for future wireless communication systems including millimeter-wave and 5G networks.

As mentioned earlier, challenges including high performance, miniaturization and low cost have become the basic requirements of new wireless communication equipment. Furthermore the filtering performance of the RF front-end plays a vital role in the quality of the entire communication system. Millimeter-wave filters affect the channel selection, image suppression, noise attenuation, and High-Q oscillators. Therefore, how to design and process a fit filter product according to the given technical indicators in a short time is a challenge that researchers need to face. With the continuous innovation of new materials, new processes and semiconductor technologies, especially the emergence of a series of new technologies represented by LTCC, high temperature superconductors (HTS), and micro-electro-mechanical systems (MEMS), the filters of microwave frequency band have made great progress. At the same time, the existence of electromagnetic simulation software such like ANSYS HFSS, CST and Keysight ADS, has massively reduced the design/invention period of the filter made higher performance requirements achievable.

As a frequency selection component, the filter is expected to be able to transmit signals without distortion in a specific frequency range, and completely suppress useless signals and the interference coming out of the channel. In fact, this kind of filter with ideal channel characteristics is difficult to realize in practice. However, in the filter designing process, the characteristics of the filter should be as close as possible to achieve the ideal characteristics. Normally, the challenges of filter design are mainly focused on the passband bandwidth, insertion loss, return loss, out-of-band suppression, and the physical sizes of filters.

As is now widely known, 5G communication equipment is now moving in the direction of miniaturization and multiple frequency bands. Especially with the rapid development of mobile terminal equipment, more and more functions need to be fully integrated into one “smart” communication device. For example the size of the microwave filter has more stringent requirements. Also, with the introduction of more different communication standards, multi-band and ultra-wideband communications systems have progressed rapidly to satisfy access to information anytime and anywhere.

1.3 Contributions

The contributions this thesis makes to the knowledge on this subject are as follows:

- A mm-wave passive-integrated bandstop filter (BSF) using 0.13-μm SiGe with absorptive (reflectionless) behavior is reported. It can avoid the creation of RF-power reflections for filtered signals. It has a structure consisting of a two-path transversal configured into a multi-layer structure. This structure comprises separate parts, a direct transmission line for the main top layer metal and two lossy edge-grounded spiral-shaped resonators for the secondary bottom layer that are coupled between them and the top metal layer. This proposed design has a bandstop filtering (BSF) frequency response. The center frequency is located at 25.5 GHz. It can absorb the non-transmitted RF signal within its stopband region instead of returning it back to its input terminal. With this design, some RF front-end applications in mm-wave transceivers that require no earlier active stage can be realized to have less isolation and more energy-efficient [103].

- A novel mm-wave silicon-passive-integrated wide-band BPF based on a two-layered implementation is designed and demonstrated when 130-nm CMOS technology is used. This on-chip RF filter consists of a compact-size composite highpass approach in the top layer and is suitable for some broad-band

applications. An upper stopband is created by the bottom layer part coupled to the top layer to obtain a composite overall quasi-elliptic-type wide-band BPF functionality. The out-of-band TZs at both passband sides to the overall frequency response can obtain sharp-rejection filtering capabilities. The center frequency is located at 34.5 GHz while the 3-dB absolute bandwidth is 21.1 GHz which equates to 61.2% in relative terms. When compared with the other previously published wideband BPFs, this filter features a lower in-band insertion loss, compact die size, and a higher in-band power matching [104].

- A group of broadband RF bandpass filter (BPF) is designed in the bulk CMOS technology. The design is conducted by cascading a lowpass and a highpass filtering stage together. To minimize the footprint, 3-D inductors are extensively used whose parasitic capacitances are carefully exploited. In particular, the 3-D inductors turn the basic inductors into an LC tank, which enables an upper transmission zero (TZ) for the designed BPF to improve the selectivity and out-of-band power-rejection levels of the filters. The 3-dB fractional bandwidth is 68.5% for the RF bandpass filter design and is proof at the center frequency of 11 GHz. As the experimental results show, the minimum attenuation of the upper stopband is 31.7 dB for the test frequency range. It refers the filtering ability of the design BPF.

1.4 Organization of the Thesis

The thesis is structured as follows. In Chapter 2, the studies that have been done on this topic and the significance of microwave filters are evaluated. Starting from the low-pass prototype filter to the high-pass filter, the frequency conversion technologies are reviewed from the bandpass to the bandstop structure. The status of research into the filter is further indicated by reviewing the development of its foundry processes.

In Chapter 3, a millimeter-wave on-chip BSF with absorptive/reflectionless behavior is presented. Using such absorptive capability, the designed BSF could avoid the creation of RF-power reflections for filtered signals which can deteriorate earlier active stages in integrated RF front-end chains. It exploits a two-path transversal configuration in a multi-layer structure. Specifically, it is composed of a direct transmission line for the main path (top layer) and two lossy edge-grounded spiral-shaped resonators for the secondary path (bottom layer) that are coupled between them and to the main path. Thus, a sharp second-order stopband is created through destructive signal-interference effects between the two signal paths with intrinsic RF-power absorption within the volume of the lossy resonators.

In Chapter 4, an on-chip millimeter-wave (mm-wave) broad-band BPF developed in CMOS technology is reported. It is based on a two-layered implementation in which the circuit structure patterned in the top layer exhibits a highpass-type filtering response, whereas an upper stopband is created by the bottom-layer cell when coupled to the top-layer one to obtain a composite overall quasi-elliptic-type wide-band BPF functionality. The locations of the transmission zeros (TZs), which confer sharp-rejection capabilities to the total BPF, can be flexibly adjusted with the values of the capacitors that are employed in both layers. An equivalent lumped-element circuit model of the proposed wide-band BPF approach is also provided and applied to multi-stage BPF arrangements for higher-selectivity designs.

In Chapter 5, another RF broad-band BPF in bulk CMOS technology is reported. The reported solutions are mostly aimed at further reducing the physical footprint of the on-chip filter by means of different design strategies to generate cost-effective highly-integrated RF systems. Among these RF techniques, the employment of alternative 3-D inductor implementations, in which their parasitic capacitance is properly exploited to use them as *LC* tanks in more-compact BPF schemes that are prescient of some capacitors.

Finally, in Chapter 6 the conclusions of this thesis are drawn and further research avenues are suggested.

Chapter 2: Literature Review

In any radio frequency system, the role of the filter is to transmit and attenuate the signal at a specific frequency. Thus, it has become an indispensable part of the wireless communication system. This chapter will mainly introduce the theoretical basis, related background of the on-chip filter, the comparison of the research status of different filters, and the previous literature.

In this thesis, some related literature is reviewed. The main features of those previous published works are summarized and to prepare the comparisons of the works in this thesis. In section 2.1, some theoretical basics are introduced. Section 2.2 summarizes the fabrication processes. Section 2.3 presents a review of related researches with the technical specifications. At last, the summary is given in Section 2.4.

2.1 Theoretical Basics

2.1.1 The Basic Technical Indicators of the Filter

Theoretically speaking, the insertion loss in the pass band of the ideal filter is zero, the attenuation of the stop band is infinite, and the roll-off slope of the transition band is 90 degrees. However, the actual filter performance cannot achieve these results. There are many technical parameters in the actual filter characterization, such as center frequency, bandwidth, insertion loss, stopband suppression, return loss, etc. All of these design parameters are linked to each other. The designer can achieve a better filtering outcome by continuously improving the basic parameters of the filter.

The basic technical indicators of the filter are listed below:

- Insertion Loss (IL): Under ideal conditions without any losses, the filter inserted into a system will not produce any attenuation at in-band. In reality, the filter consumes a certain amount of power in the radio frequency system. Insertion loss is defined as the ratio of the incident power to the power output by the filter load. As far as filter design in concerned, the smaller the insertion loss of the device can be, the better it will perform.

- Bandwidth: The bandwidth (BW) of the filter is simply the difference between the upper and lower cut-off frequencies. The cut-off frequency is usually defined with a 3-dB attenuation with in-band frequency response. Additionally, the parameter of fractional bandwidth (FBW) is employed for filter design, which is simply the ratio between center frequency and the BW. Based on the calculated values for FBW, the filter can be divided into a narrowband filter and a wideband filter.

- Ripple: Ripple describes the fluctuation amplitude of the signal in the passband of the filter. It can be defined as the difference between the maximum and minimum of the filter's amplitude-frequency response.

- Rejection: Rejection is an indicator that reflects the filter's ability to suppress out-of-band interference signals or useless signals. The greater the out-of-band suppression can be; the better filter performance it will achieve.

- Shape factor: Describes the degree of curve transformation of the filter transition. The larger the rectangular coefficient with the steeper the roll-off of the filter transition can be, the better the frequency selectivity it will achieve. Its expression is $SF = \frac{\text{BW\_3dB}}{\text{BW\_20dB}}$.

- Return loss (RL): Because the working principle of the filter is to let the signal

in the pass band pass, so that the signal in the stop band is reflected back to the signal source. This index is mainly used to describe the situation where the incident power is reflected back to the signal source. It is defined as the ratio of incident power to reflected power.

2.1.2 Design Methodologies for On-Chip mm-wave Filters

Passive components usually refer to and are not limited to commonly well-known capacitors, and inductors but also include most non-switching analog devices. The concept of integrated passive devices involves the fabrication of passive circuits on a common substrate instead of them having their own individual packages. In this thesis, we are primarily focused on resonator and filter designs. There are three different design methodologies for passive components as mentioned, and they are as follows. Firstly, the distributed-element-based designs, which utilizes the classical microwave theories, such as transmission line. For the second type, this is the lumped-element-based designs, which utilizes on-chip discrete passive components, such as inductor, capacitor and transformer. The third type combines the advantages of distributed- and lumped-element-based approaches, namely hybrid-element-based design. One typical design example for this kind of design is to utilize lumped-element capacitors, such as metal-insulator-metal (MIM) caps, to replace distributed-element capacitors. Consequently, the overall physical dimensions of the filter could be significantly reduced.

2.1.3 Manufacturing Technologies

The arrival of the 5G era has resulted in the structural growth of data transmission, and it is changing people's daily lives. In order to manage the transmission of massive data, system it requires not only new complex modulation methods, but also a wide radio frequency spectrum to support high-speed broadband communications. Therefore, frequency bands in the mm-wave regions have been widely used to support the required

high-speed transmission. Traditionally, most mm-wave filters are manufactured using PCB technology such like the LTCC and SIW technology. This is despite the traditional manufactured millimeter waves bandpass filters perform well, low insertion loss and high frequency selectivity. The miniaturization of mm-wave filters is also limited due to the influence of the narrowest metal line in the above processes. With the development of semiconductor lithography technology, manufacturing accuracy has reached the micron and nanometer levels that provide the basis for further miniaturization of mm-wave bandpass filters. In contrast, in order to get the system to consume less power, more and more devices are integrated on the chip to form a system on chip (SoC). Therefore, the advantages of on-chip mm-wave filters have become increasingly prominent.

Among the many chip processing technologies, it is particularly important to select the appropriate manufacturing technology. Especially, for large-scale commercial chips, tape-out prices have a particularly large impact on market competitiveness. Therefore, the processing technology needs to be chosen to minimize the cost of tape out while meeting the design indicators. The following figure shows the tape-out prices of various processing technologies and foundry factories. On the premise of satisfying designed results, one of the studies in this thesis adopts the most economical 0.13-μm SiGe processing technology to fabricate the filter.

As compared, some main used fabrication processes are listed in this section:

- Gallium Arsenide (GaAs) and Gallium Nitride (GaN) technologies. As processes for designing millimeter wave circuits, they have also become hot topics of current research. Dr. Yang and colleagues used edge cross-finger coupling to design two low-loss and high-selectivity filters [43]. The lumped parameter circuit helped to analyze the transmission zero point and resonance characteristics of the filters and received good frequency selection characteristics. In [105], two dual-mode resonators are used for coupling. A

second-order filter is constructed with slot electrical coupling for feeding which achieves low insertion loss and good design selection. However, the fabricating cost of GaAs and GaN technology is far higher than that of CMOS technology. Consequently, they are not suitable for integration with baseband processers at present, which restricts their use in millimeter wave circuits.

- Silicon germanium (SiGe) is widely used in the design of millimeter wave circuits due to its high compatibility and low processing cost. The highest cut-off frequency of the SiGe technology used in this thesis is 200 GHz [89]. However, this technology also has certain limitations, for example, it is difficult to transfer the design method on the PCB board to the IC design. The high loss of the dielectric substrate and the low quality factor of the device, the fixed thickness of the dielectric layer and the strict design specifications are different from PCB to integrated circuits. These technical limitations still cannot hinder the development of RFIC.

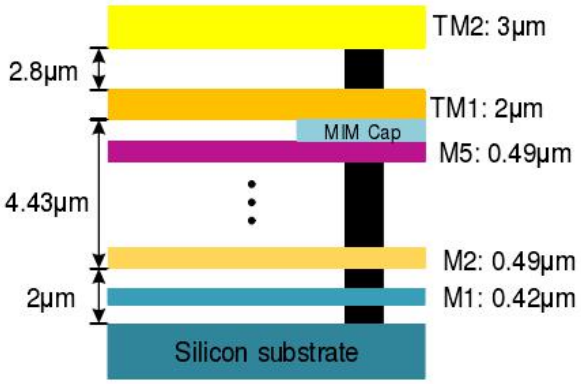


Figure 2.1. Metal stack-up in 0.13-μm SiGe (Bi)CMOS

2.2 Review of Related Passive Researches

As far as on-chip filter is concerned, some kinds of classical EM structures have been published in the literature. In this section different EM structures will be described, and challenges for further improving the performance of designed on-chip filter will be summarized.

2.2.1 Interdigital Structure

As the modern communication systems now have some new modulation versions like the Orthogonal Frequency Division Multiplexing(OFDM), RF filters are made to be qualified to those high speed and frequency applications. Some know-how structures for new filtering passive devices will be reviewed in this section.

- **CMOS 5-order symmetric Interdigital BPF**

  Miniaturization is always the core issue for integrating the passive components on a CMOS structure. Bo Yang and team devised a fabricated structure working at a center frequency of 55GHz as a bandpass filter [30]. A coupling part is added between the two resonators in the filter. Then the designed interdigital filter is working well as a compact size instead. The figure below is the schematic of the design principle.

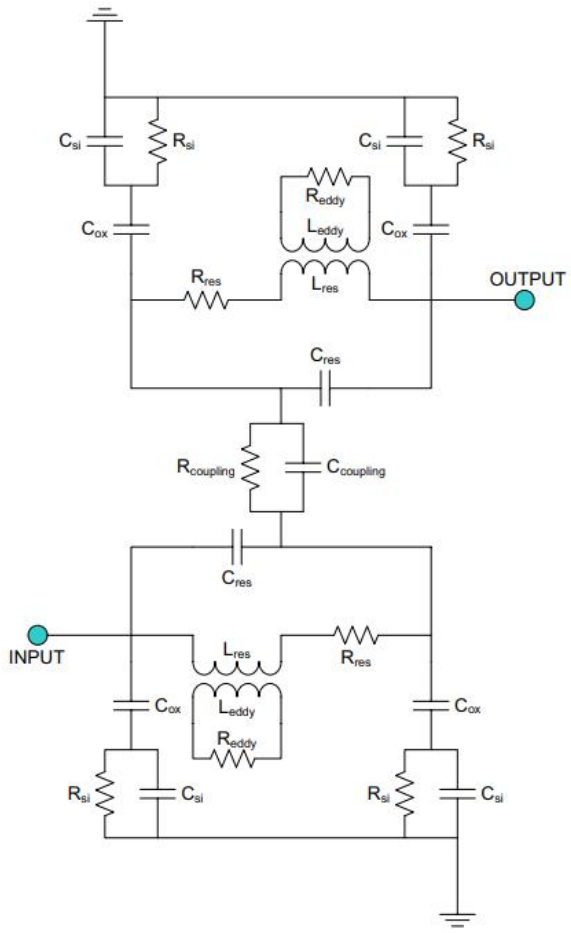


Figure 2.3. Schematic of the coupling structure [30].

Then, with this methodology, authors designed and fabricated a bandpass filter as this structure with CMOS substrate for the RF front end module (FEM). As tested, the operating frequency is located at 55.3GHz deliberately. However, the bandwidth of the final solid result is only 3.25% which is not quite suitable for those applications working at mm-wave frequency ranges.

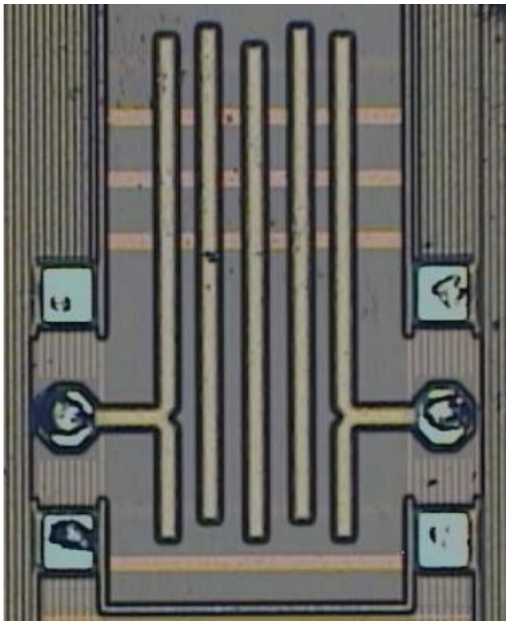


Figure 2.4. Die photo of the designed filter following the structure in Figure 2.2.[30]

- **U-Shaped Interdigital Resonator**

In the article presented by Islam Mansour et al. [31], a U-shaped resonator is designed with a U-shaped inductor and finger capacitors to build a Ku-band voltage controlled oscillator (VCO). For this design to be feasible, the fabricated integrated circuit has a compact size of 0.0015 mm^2 on its resonator part. Q factor reaches 2.06 due to this structure exhibiting low resistance. The frequency range of this notch filter is from 68 GHz to 88 GHz for the VCO operation. Respectively, this U-shaped filter is suitable for some specific structures with small size and broad band requirements. Also, this passive device in the article employs the 180 nm CMOS technology along

with its whole structure. It means that this filter could be integrated into some other silicon based mm-wave structures.

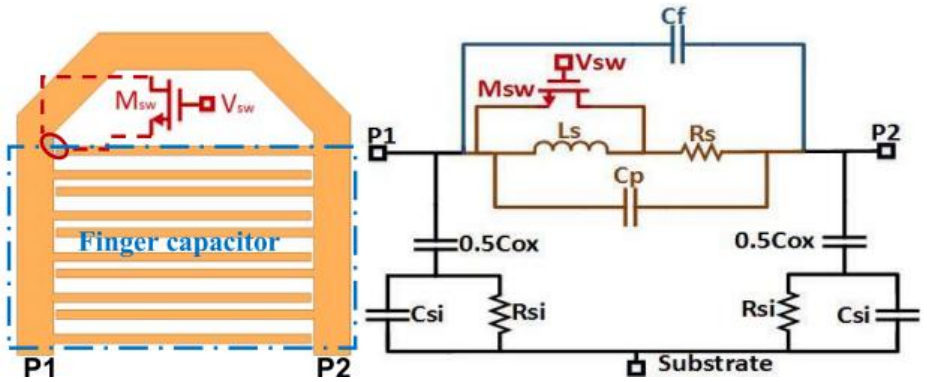


Figure 2.5. U-shaped interdigital resonator and its equivalent circuit model in [31].

- **Integrated BPF using Interdigital Capacitors**

  Z. Chuluunbaatar and colleagues brought out a novel structure using interdigital capacitors operating on the sub-6 frequency range. Since its purpose was to be utilized in the WiMax systems, this BPF is fabricated with the GaAs technology. Thus, its center frequency is 2.31 GHz and the total chip size is up to 900 μm × 700 μm [32]. To meet the requirements of filtering implementation, an integrated passive device is widely used to form a BPF. The structure depicted in the following figure is made of a spiral-shaped inductor with an interdigital capacitor inside. Compared to others, this design has good features of size, insertion loss and fabrication cost as its metal layers. However, the GaAs technology limits its operational frequency range to the mm-wave frequency bands.

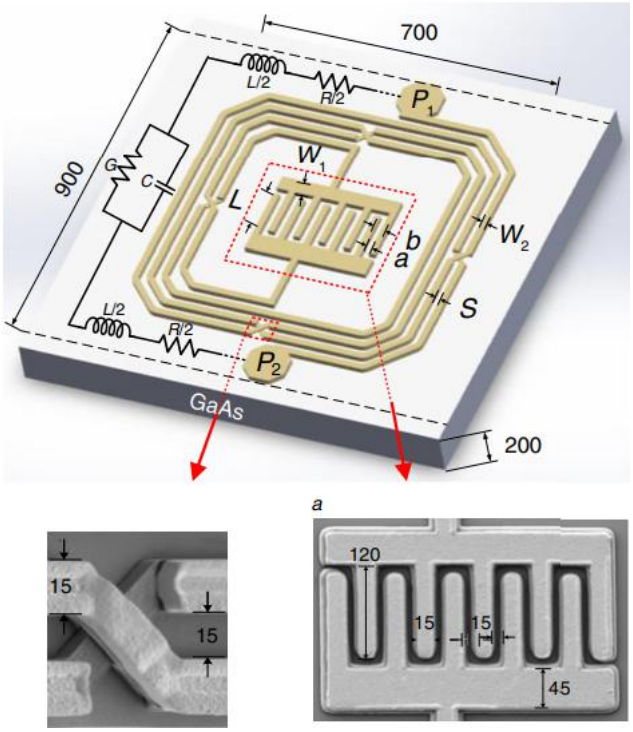


Figure 2.6. Layout of the BPF with its equivalent circuit and die photo with physical details in [32].

Dr. Yang Yang and his team also implemented the interdigital structure with the GaAs-based technology to design a bandpass filter in [43]. They built a unique LC circuit with edge-coupled cells (ECCs). Compared with the silicon-based designs, GaAs on-chip passive integrated circuits have a big advantage concerning the miniaturization task. Furthermore, this proposed filter is operating at the center frequency of 23.5 GHz with a significant 3-dB bandwidth of 22.2%. Using this technique, the loaded ECCS can be converted into a resonator and shrink the chip size as much as possible. The size of the fabrication reached 0.18 mm^2 with a commercial technology, 0.1- µ m Gallium Arsenide.

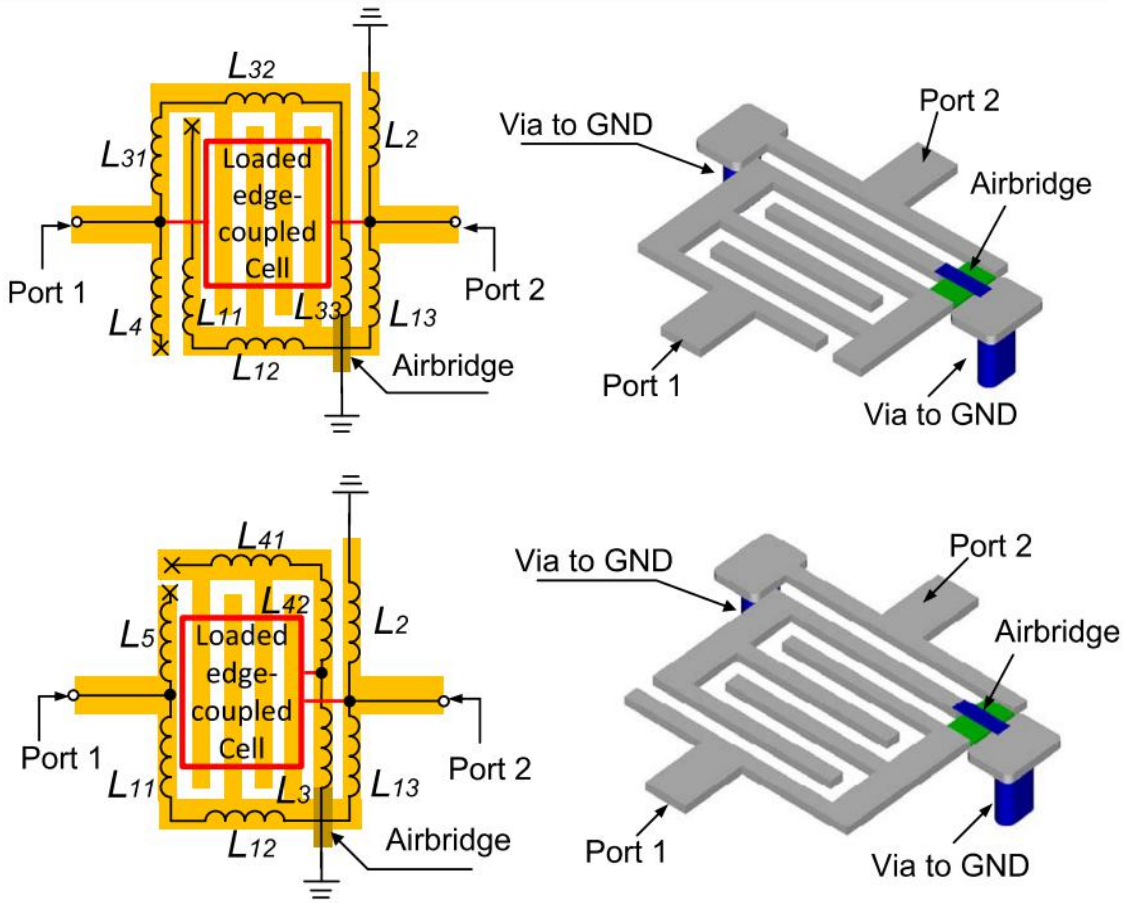


Figure 2.7. Different resonator structures with loaded edge-coupled cells [43].

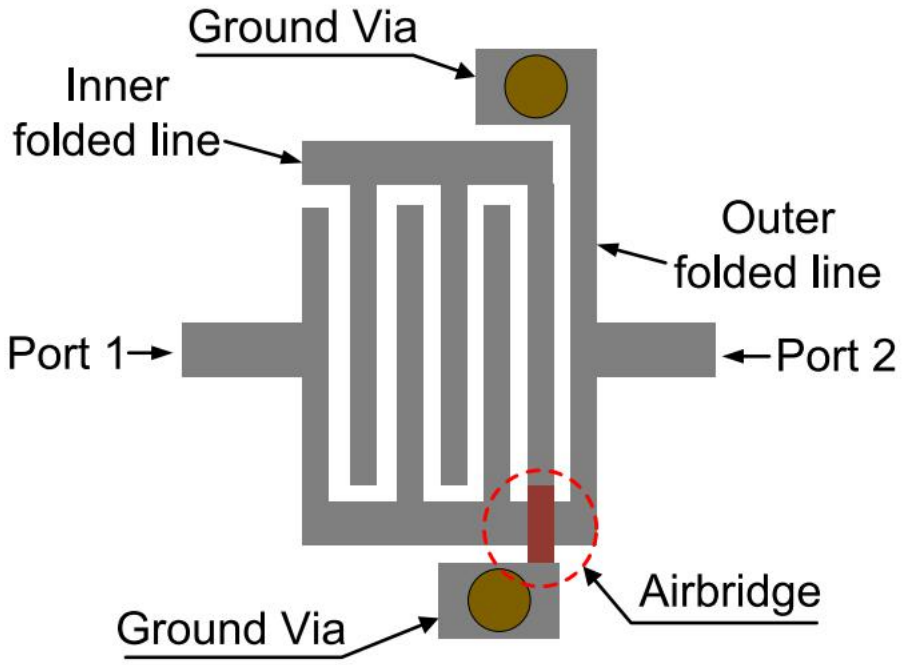


Figure 2.8. Implementation of the interdigital resonator [43].

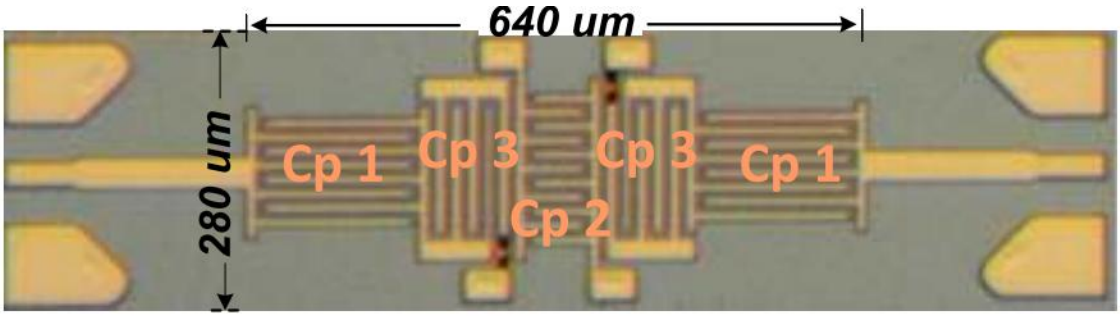


Figure 2.9. Die microphotograph [43].

2.2.2 Stepped Impedance Technique

The so-called stepped impedance technique is another well-established one in the literature. In this sub-section, an overview of integrated filters design using this technique will be given.

- **Meandering Hairpin Resonator**

  In 2008, Bo Yang and his colleagues working at University of Melbourne published an article about the meandering hairpin resonator [33]. This device is operating at the center frequency of 60GHz with a 8.5GHz bandwidth. Figure 2.9 depicts a 4th-order Stepped Impedance Resonator(SIR) bandpass filter which is formed by two miniaturized meandering hairpin (MH) resonators and two stepped impedance resonators. It was fabricated on IBM 0.13 μ m CMOS technology, and miniaturized to a size as small as 0.346 m^2 .

  Recalling the theoretical parameter described in [106], the n^{th}-order BPF could be switched up and down with the known Q-value of the input and output loaded resonators. In the design done by [33] the fabricated circuits are shown below in Figure 2.10.

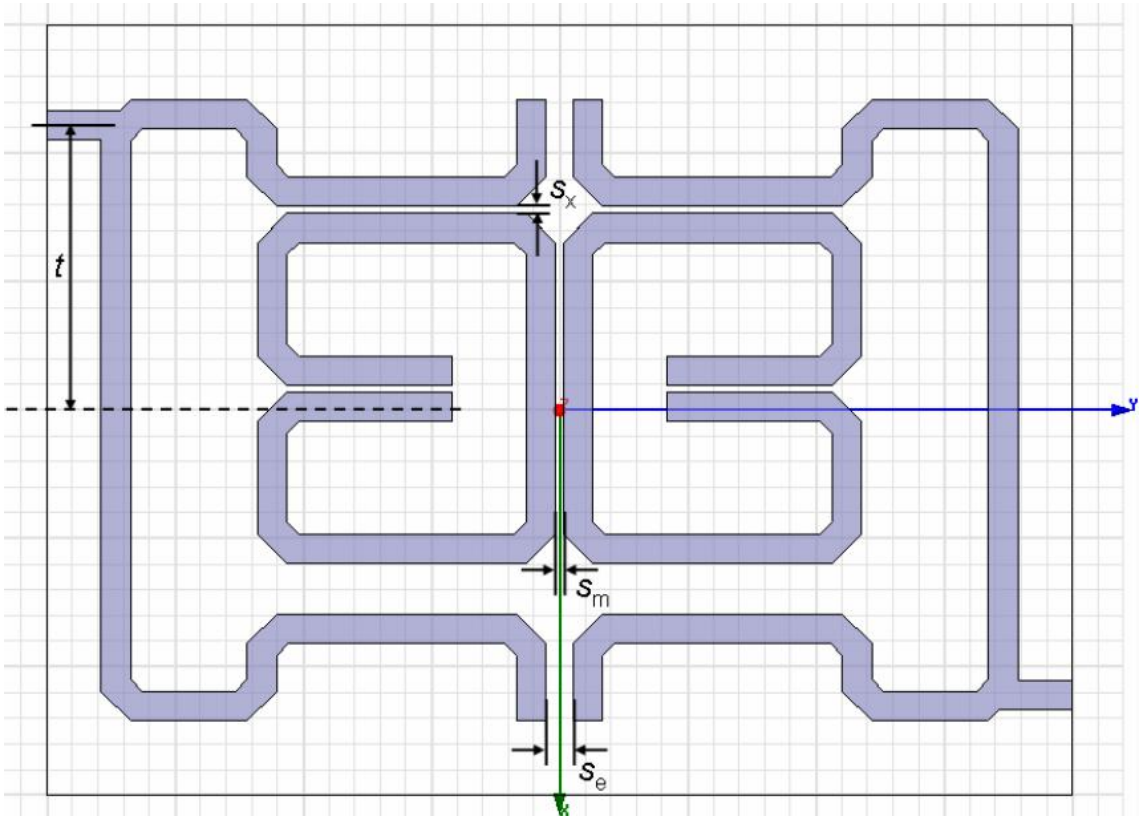


Figure 2.10. The design of the presented 4th-order cross-coupled SIR-MH filter [33].

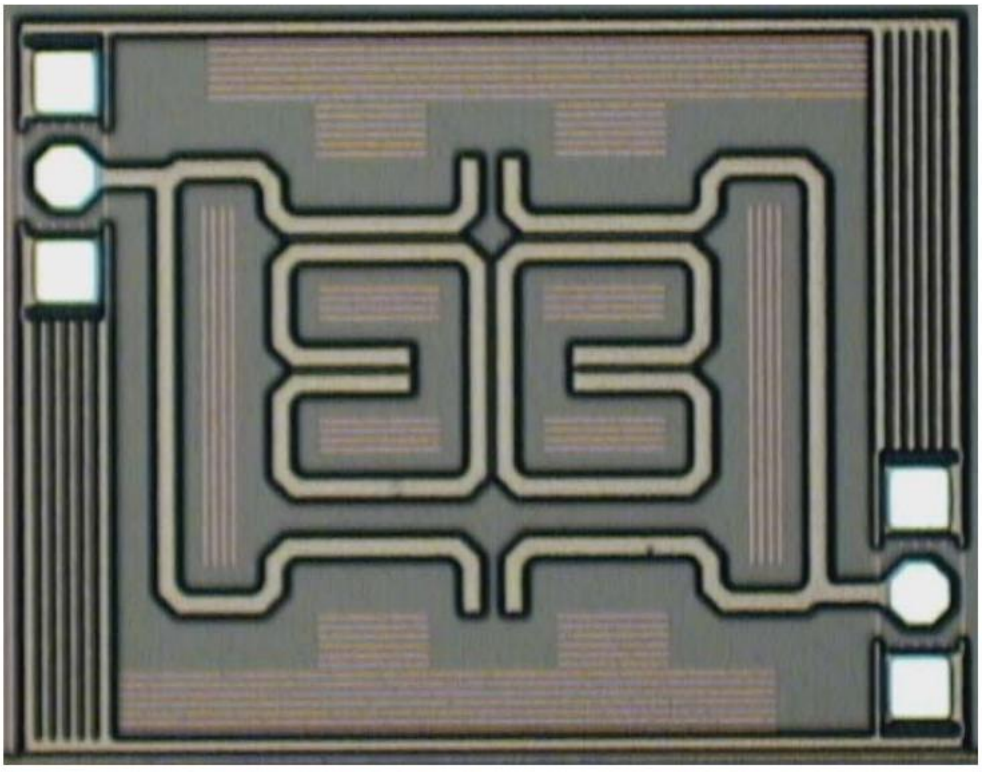


Figure 2.11. Die photograph of the designed Bandpass Filter in [33].

- **Stepped Impedance Technique with Grounded Pedestal**

Shuen-Chien Chang and his team brought another stepped impedance structure to form a CMOS based millimeter-wave band pass filter. To be integrated in the transceiver system, the chip size should be miniaturized as small as possible. With this design, the filter reached the size of 0.37 x 0.2 mm^2 . It brought a new solution to the devices operating between 40 and 78 GHz.

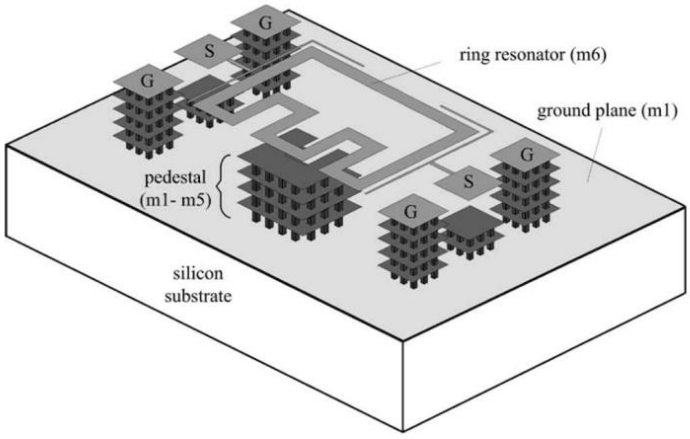


Figure 2.12. The designed bandpass filter [34].

A similar design technique is used in the paper presented in [35], and it is illustrated in Figure 2. 12 with a different design structure. A stepped-impedance cross-resonator using M2 to M7 forms the ground. The two open stubs with the grounded pedestal are designed to further improve the TZs found below and above the passband. The TZ will vary depending on the number of metal layers stacked on top of each other to form the pedestal. The height of the metal stacked up will have an effect on the impedance of the system. Therefore, the TZ can be effectively controlled by the level of the pedestal. The design in [35] resonates at 77 GHz with insertion loss less than 3 dB and return loss of greater than 40 dB. The 3-D view of the layout is illustrated in Figure 2.13.

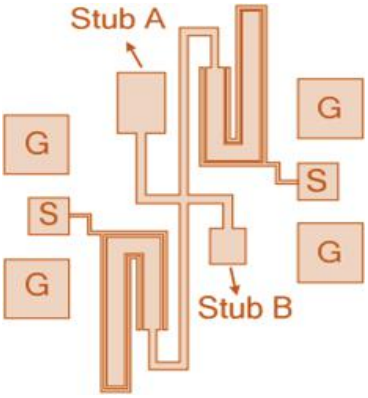


Figure 2.13. The 2-D view of the designed BPF using stepped-impedance resonator in [35].

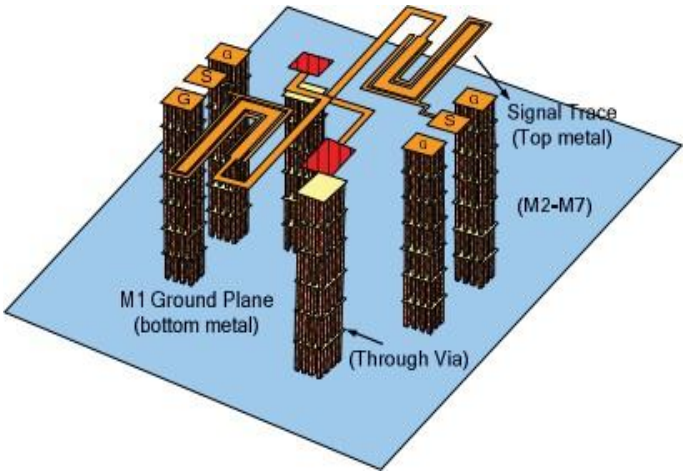


Figure 2.14. The 3-D view of the designed BPF shown in Figure 2.12 [35].

- **Stepped-Impedance-Based Resonator**

Another design example presented in [34] uses an open resonator. One shortcoming of this design structure is that the TZ does not exist. In order to address this issue, an open stub is shunted at the center position of two TZs. This structure creates a virtual short at the center of the resonator at the fundamental odd-mode frequency, thus providing TZs at the desired frequency. Figure 2.14 illustrates the design presented in [34]. As can be seen, it is implemented using an open-ended stub. Based on the simulation results the height and width ratio is proportional to the resonance frequency. Thus, a shorter resonator length is favorable in order to achieve the desired target frequency.

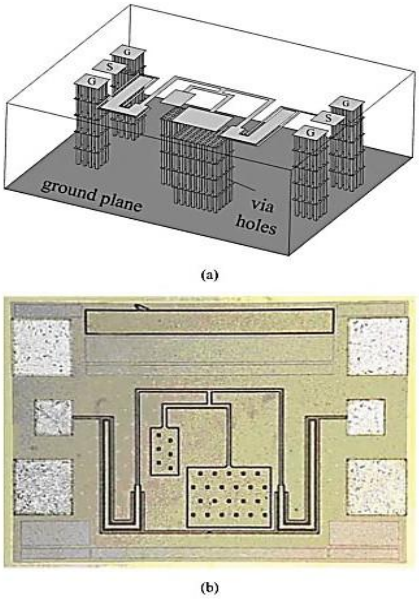


Figure 2.14. The designed BPF, (a) the 3-D view of the BPF, (b) die photo of the design.

2.2.3 Slow-Wave Structures

Slow wave concept is another classical one that has been widely used in microwave passive components design, especially miniaturized circuits design. In this sub-section, an overview of the previously published works is given. In slow wave propagation, the electromagnetic wave is transmitted in the guided- wave medium with a slow phase velocity by modifying the electric and magnetic field in the media. A conventional slow-wave structure, such as photonic bandgap (PBG), has been studied in microwave and millimeter wave frequency ranges to reduce physical dimensions of passive components. As presented in [36], a filter is designed using a slow-wave structure. In order to minimize the footprint, a frequency selective ground plane is implemented as a PBG ground plane. The structure has a periodic rectangular slot etched along the direction of signal transmission to exhibit a select band function; however, it needs to satisfy a certain condition, $\beta\alpha = \pi$, where β is the propagation constant and α is the lattice periodicity, which is equal to the pitch P_g $(W_g + S_g)$ of the slot. To demonstrate the proposed slow-wave structure a 2nd-order rectangular open loop filter was designed using IBM 65-nm bulk CMOS technology with 1-dB bandwidth of 57-66 GHz.

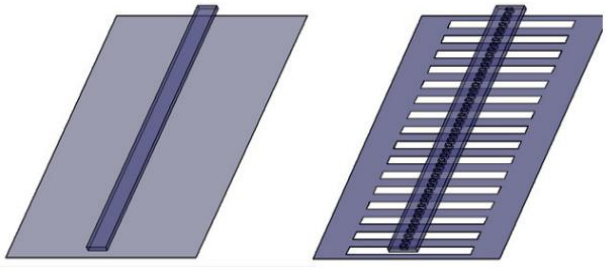


Figure 2.15. The top- and 3-D views for the designed filter in [36].

2.2.4 Coplanar Waveguide (CPW) Structures

- **Combline-Based BPFs**

A coplanar waveguide structure was studied in [37]. It demonstrated a combline-type structure based on co-planar waveguide (CPW) and applied to the proposed filter design. The resonator in this design is composed of multiple coupled transmission line as shown in Figure 2.16, the end section of the transmission line describing the TEM mode of propagation is short-circuited and open at the other end. The open end exhibits a different capacitive reactance. This capacitive reactance is inversely proportional to the transmission line length. Consequently, a miniaturized structure can be implemented with a wide rejection band. However, the capacitance is not large enough to miniaturize the size and the skirt selectivity is not good enough either. In order to address these issues, the resonator transmission line is designed to have a quarter-wavelength and is folded into a meander-like structure to make the design more compact as illustrated in Figure 2.17. A MIM capacitor is used for capacitive loading; this structure further reduces the design footprint. Another design based on combline structure is presented in [38], constructed using a thin-film microstrip transmission lines (MSTL) and interdigital capacitor. It is implemented in a standard 0.13-μm 1 poly 8 metal CMOS technology using the top layer Metal 8 as MSTL and connecting to ground via stacks of vias. The interdigital capacitor is implemented using metal 5, metal 6 and metal 7 stacked on top of each other. During simulation, the characteristic impedance is kept constant when the frequency sweeps from 50 GHz to 250 GHz. The author noted that the quality factor of the microstrip line

is proportional to the square root of the frequency ranges from 50 GHz to 100 GHz. However, beyond 100 GHz the quality factor starts to drop. Similarly, the capacitance increases with rising frequency. In the presented design [38], the capacitance value is 29 fF and the quality factor is 120 at 170 GHz resonance frequency.

A 2nd-order combline filter [38] is shown in Figure 2.18. The design resonates at 170 GHz with 2.7-dB insertion loss at 10.5-GHz bandwidth, -15 dB return loss and 0.04-dB in-band ripples. The design occupies a chip area of 125μm × 110μm.

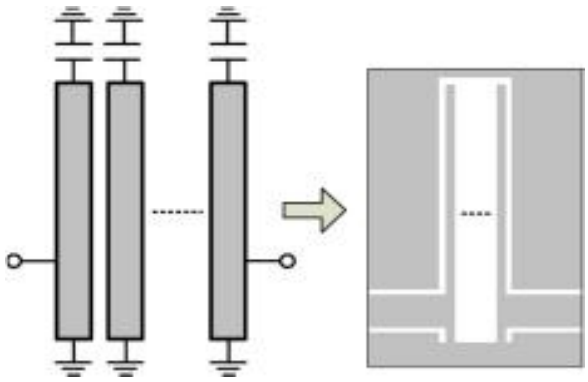


Figure 2.17. Illustration of the conventional combline type BPF [37].

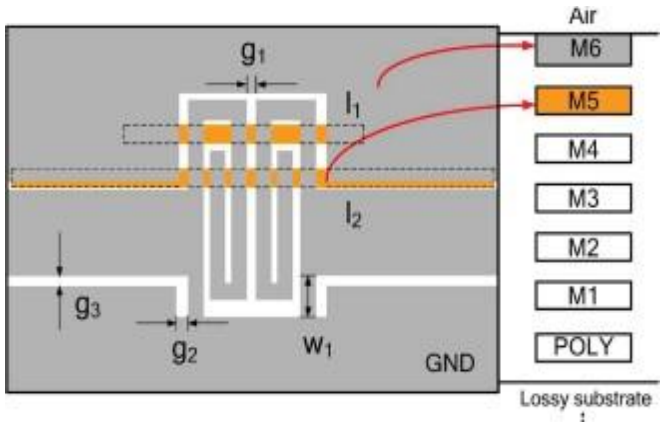


Figure 2.18. The top-view of the designed BPF shown in Figure 2.16.

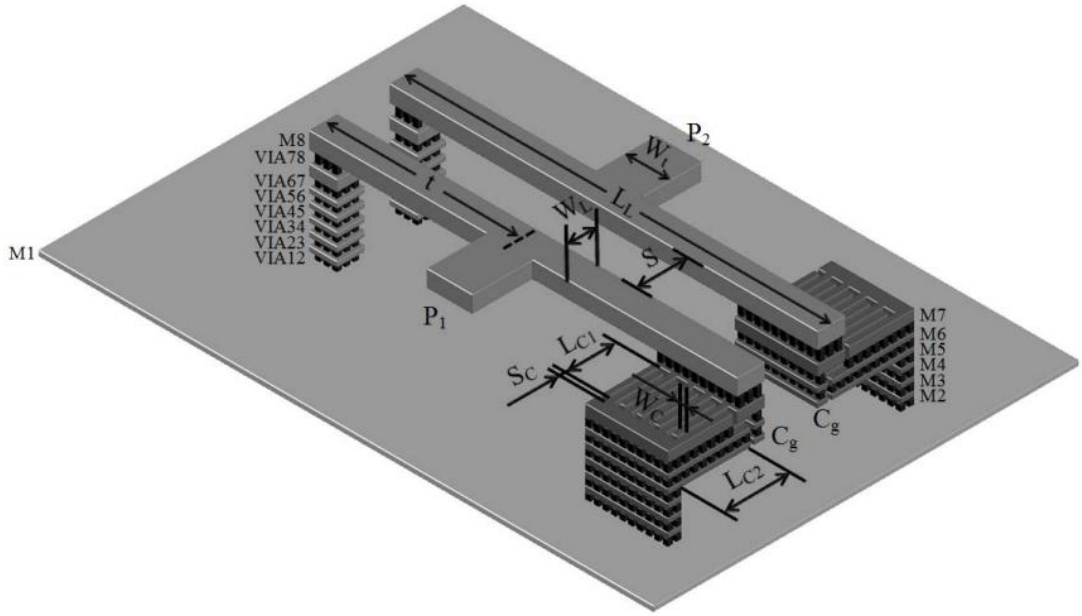


Figure 2.19. The 3-D view of the 2nd combline-based BPF presented in [38].

2.2.5 Shielded Coplanar Waveguide

A floating strip has been studied in [39] using a quasi-static approach in simulation at 60 GHz to analyze the eddy current characteristic of the metal strip. It was observed that the eddy current circulates in various directions causing loss to the structure. Based on the simulation in [39], the thicker the strips then the more power will be dissipated. Considering this issue, a unique shielding transmission line CPW is implemented. The patterned floating strips are constructed in the lowest layer using the thin metal layer in order to minimize the losses caused by the eddy currents. The distance h between the CPW and the floating strips is optimized and adjusted to achieve the target characteristic impedance using vias to reduce the conductor loss as illustrated in Figure 2.19. Meanwhile Figure 2.20 shows the die microphotograph of the implemented 1st-order T-junctions using a S-CPW-based design. As compared to the conventional microstrip line, the presented structure is electrically long because of the exhibited strong slow-wave effect.

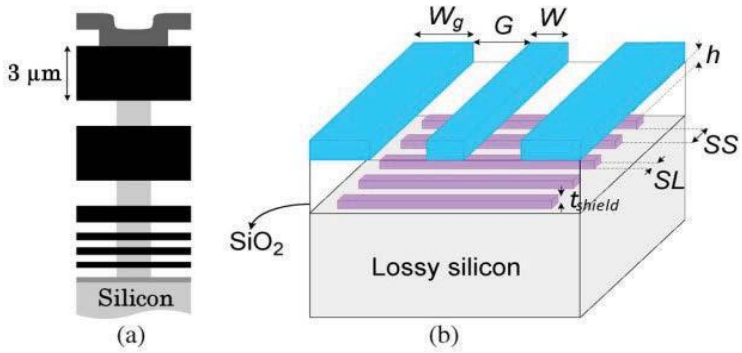


Figure 2.20. (a) Metal stack-up of a BiCMOS 9MW technology (b) the 3-D view of the S-CPW-based design [39].

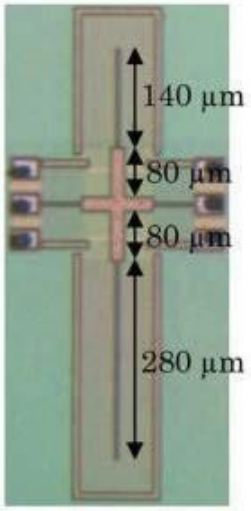


Figure 2.21. Die microphotograph of the designed 1st-order resonator shown in Figure 2.19.

2.2.6 Meander-Liner Resonator

A unique structure based on meander-line type transmission lines is illustrated in [41]. Two meander lines are identical in dimension and set in a broadside-coupled to each other with opposite orientation as shown in Figure 2.21. It is constructed using the topmost metal layer using 0.13-µm CMOS technology. To demonstrate the impact of the bottom transmission line, an EM tool was used and it simulated the effect with the following cases; when completely removed and when placed on the same orientation. By removing the bottom line or placing it in the same orientation, this dramatically affects the design's resonance. Furthermore the effect of metal length and width are

investigated. The variation is mainly due to the metal loss and parasitic capacitance. Thus the resonance frequency can be altered by varying the total length of the line. A simplified equivalent lumped-element model was investigated to verify the performance of the presented design [41].

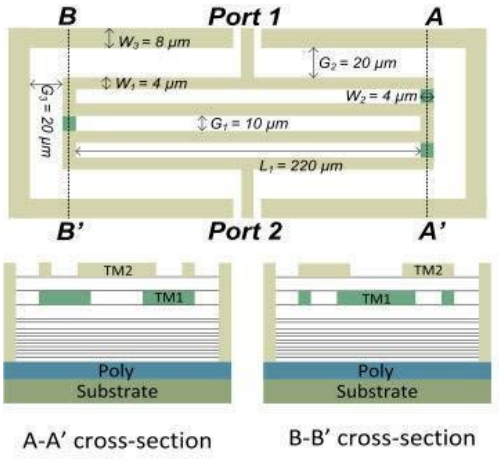


Figure 2.22. The top- and the cross-section views of the broadside-coupled resonator presented in [41].

The design is further investigated in the paper presented in [42], where the author extended the structure shown in [41] by adding an edge-couple to the ground ring and with a defected ground structure (DGS) using the lower metal layer. The defected ground structure can be modeled by a simplified equivalent LC tank, which creates resonance at the specific frequency. A parallel simulation of implementation of the broadside couple meander line structure with and without defected ground defect is shown in [42]. The effect of adding DGS greatly enhances the stopband attenuation of the circuit but exhibits trade-off regarding frequency selectivity. As investigated, this selectivity issue is due to the additional capacitance induced by the added DGS. It is also noted that fine-tuning can be done between the mutual couplings of the BCMLR that could effectively vary the resonance frequency by changing the physical dimension, the exhibits advantages in terms of design flexibility. The proposed design in [42] is illustrated in Figure 2.22.

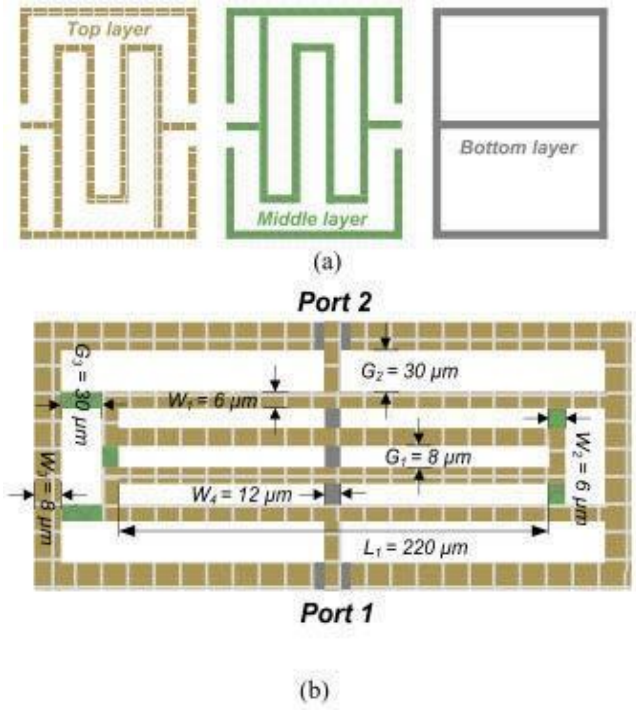


Figure 2.22. A BPF designed in [42], (a) 2D view of the three layers of the presented edge-coupled resonator, (b) the top view of the designed BPF with dimensions.

2.2.7 Closed- and Open-Loop Structures

The folded loop is another design structure that exhibits potential for device miniaturization. In [44], a dual-mode ring resonator is presented for 70 GHz mm-wave frequency applications. The resonator is designed to have one wavelength in the total perimeter, and the perturbation section creates the dual-mode generation. To reduce the substrate loss M1 is used for grounding and M6 is used to implement the resonator. In Figure 2.23, it shows the schematic of the proposed folded loop dual mode resonator. As compared to the conventional rectangular loop configuration the proposed folded loop dual mode resonator hada reduced size of 60% as reported in [44] and illustrated in Figure 2.24. To excite a two degenerative mode, a pair of the orthogonal lines is fed in the microstrip line to create two TZs and reject adjacent interference. However, the orthogonal lines may not be suitable for RFIC on chip design.

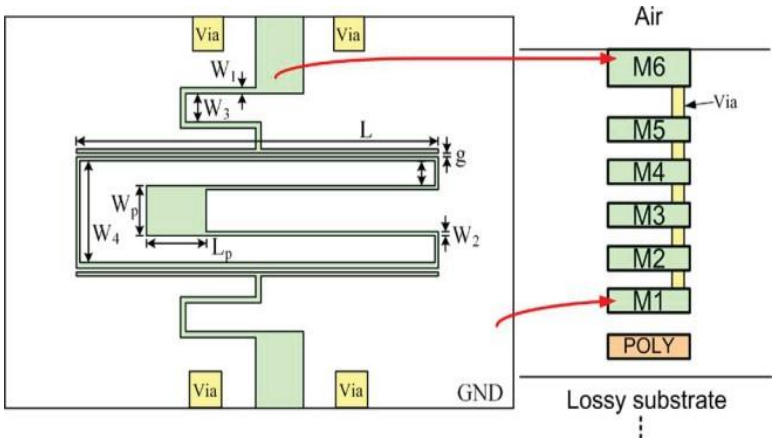


Figure 2.23. The top-view of the designed filter with illustration of metal stack-up [44].

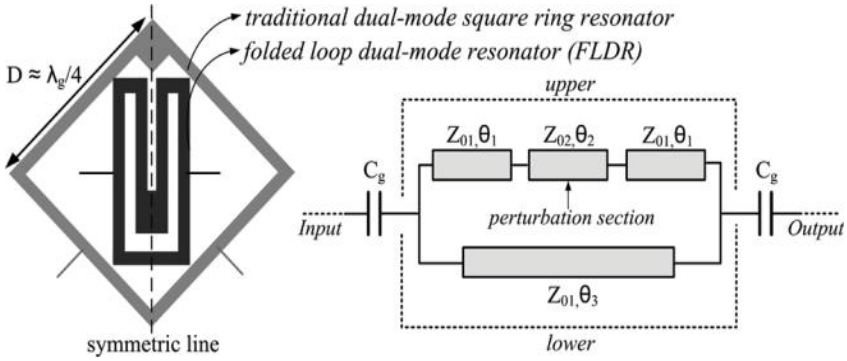


Figure 2.24. The structure of the folded loop dual mode resonator with its transmission line model [44].

2.3 Trends and Issues of the State-of-the-Art Designs

Based on the presented literature review, it is clearly shown that there is a demand for miniaturized passive components with enlarged bandwidth and reduced insertion loss. Moreover, the great bulk of previously published designs concentrate mainly on BPF design, and not much has been done on BSF design, which also plays a very critical role in modern wireless systems. Thus, in this thesis, we will discuss both BPF and BSF designs.

2.3.1 Issues with Wide-Band BPF Designs

The 5G wireless communication targets for at least 10× data-rate increasing, which radically changes future wireless connectivity. The mm-wave bands can potentially

deliver such high data rates and capacity compared to low-GHz bands [6]-[19]. The 3GPP 5G NR standard specifies n257 band (26.50 to 29.50 GHz), n258 band (24.25 to 27.50 GHz), and n260 band (37.00 to 40.00 GHz) for Frequency Range 2 (FR2) [7]. Different FR2 bands or their subsets are adopted by various countries/regions worldwide, which necessitates wideband/multiband mm-wave 5G systems to support international/cross-network roaming, particularly for user equipment (UE) devices [9]-[12]. To cover such a wide bandwidth, from 24 GHz to 40 GHz (approximately 50% FBW), it requires miniaturized on-chip BPF implemented in silicon-based technology, so that the filter can be integrated with the other critical building blocks at RF front-end.

Currently, most broadband filters usually are including interdigital filters, parallel coupling filters, and hairpin filters. However, these solutions inherently result in relatively large die area and thus need to be significantly miniaturized before they could be used for on-chip implementation. Moreover, the selectivity of the designed BPF is also important. To maintain a good selectivity, a higher-order filter is required. However, as the order of filters increases, the size of the filter is getting larger, which is not conducive to the miniaturization of the system. Therefore, there are some major design issues need to be solved for wideband on-chip BPF design.

2.3.2 Issues with BSF Designs

Most filters provide rejection by reflecting signals back outside of the passband. This can sometimes cause a problem, especially when two filters are cascaded to “improve” rejection. As rejection of a filter depends on what matched impedance that filter seeing, simply cascading two BSFs together might not achieve a combined rejection. Moreover, in active non-linear circuits such as power amplifiers and mixers, there is an urgent need for filters that can eliminate strong interference and noise in the stop band. As the parasitic passband caused by higher harmonics will seriously deteriorate the out-of-band suppression performance of the band-pass filter, the study of reflection-less BSFs has also become a problem that must be urgently solved.

To the best of our knowledge, most reflectionless filters require resistors to absorb the reflected energy. However, using lumped-element resistors has two drawbacks. Firstly, unlike the implementation of other lumped-element components such as inductor, capacitor and transformer, which only need the BEOL process, applying resistors requires FEOL, which in turn requires additional masks for fabrication. Consequently, it increases the costs for fabrication. Secondly, there might be a reliability issue concerning the resistors, as these usually having limited power-handling capability. For this reason, it would be interesting to see if it is possible to design a reflectionless filter without using any lumped-element resistors.

Chapter 3: On-Chip Millimeter-Wave Integrated Absorptive Bandstop Filter in (Bi)-CMOS Technology

Abstract—A millimeter-wave passive-integrated bandstop filter (BSF) with absorptive/reflection less behavior is reported. It avoids the creation of RF-power reflections for filtered signals which can deteriorate earlier active stages in integrated RF front-end chains. In the conventional designs, lumped-element resistors are usually used to absorb the reflected energy. However, there are two major issues related to the conventional approach. The first one is that the implmenetation of lumped-element on-chip resistors require more mask layers for fabrication, which results in additional costs for both prototyping and mass production. The second one is that the reflected RF energy needs to be completely absorbed by the resistors only. In theory, there is no other componenet has the absorbsion feature. It means that the resistors needs to be able to handle thermal stress for a reasonable aount of period. This might not be possible when the reflected power becomes stronger and stronger. To solve these two issues, a novel resistor-less approach is proposed in this Chapter. It exploits a two-path transversal configuration in a multi-layer structure. Specifically, it is composed of a direct transmission line for the main path (top layer) and two lossy edge-grounded spiral-shaped resonators for the secondary path (bottom layer) that are coupled between them and the main path. Thus, a sharp second-order stopband is created through destructive signal-interference effects between the two signal paths with intrinsic RF-power absorption within the volume of the lossy resonators. As practical validation, a 24.5-GHz on-chip millimeter-wave absorptive BSF circuit is built in a 0.13-μm CMOS technology and tested. A close agreement between simulated and measured results for this on-chip BSF circuit is achieved.

3.1 Introduction

RF filters are essential devices in RF front-ends to carry out RF-signal-band

selection processes [i.e., BPFs], and to mitigate spurious terms and out-of-system interference signals [i.e., BSFs] in the transmitter and receiver chains. Recent works on on-chip filters for mm-wave applications using different technologies, such as gallium arsenide (GaAs), complementary metal-oxide-semiconductor (CMOS), and silicon germanium (SiGe), have focused on reflective-type filters [30]-[59]. In the case of BSFs, this means that the non-transmitted RF-signal energy within the stopband regions is reflected back to the source. Such an effect can deteriorate the behavior of active components that are placed before filters in the integrated transceivers. An example of this making RF amplifiers to become unstable or by increasing the number of spurious terms generated by mixers in frequency-conversion stages due to the re-mixing of the reflected RF signal with its local oscillator (i.e., intermodulation expansion) [107]. Moreover, for some extreme cases, these active components might even be permanently damaged by reflected strong RF signals. Such problems can be avoided by using the inter-block active-isolation stages, as they increase DC power consumption, cost, and size in the full transceiver chain.

A more convenient solution to the aforementioned problem of RF-power-reflection mitigation is to use reflectionless or absorptive RF filters. This type of filter dissipates the non-transmitted RF-signal energy inside their lossy-circuit structures instead of reflecting it at the input terminal [107]-[111]. In the case of absorptive BSFs, several solutions have been proposed based on different circuit topologies. Among them are the following: (i) circuits with even- and odd-mode subnetwork compensation [111]– [113]; (ii) balanced-circuit architectures [114]; and (iii) complementary-diplexer networks [115]-[116]. However, most of these solutions need additional resistors for the RF-power-absorption process, and additional passive circuits (e.g., power dividers/couplers in the case of [114]), which could limit the operational range of these BSFs. Moreover, most of them have been developed for off-chip designs, with a few exceptions such as those in [116] but for BPFs and operating in low-frequency regions of the microwave spectrum. Other examples of absorptive BSFs are the ones reported in

[117]-[120].

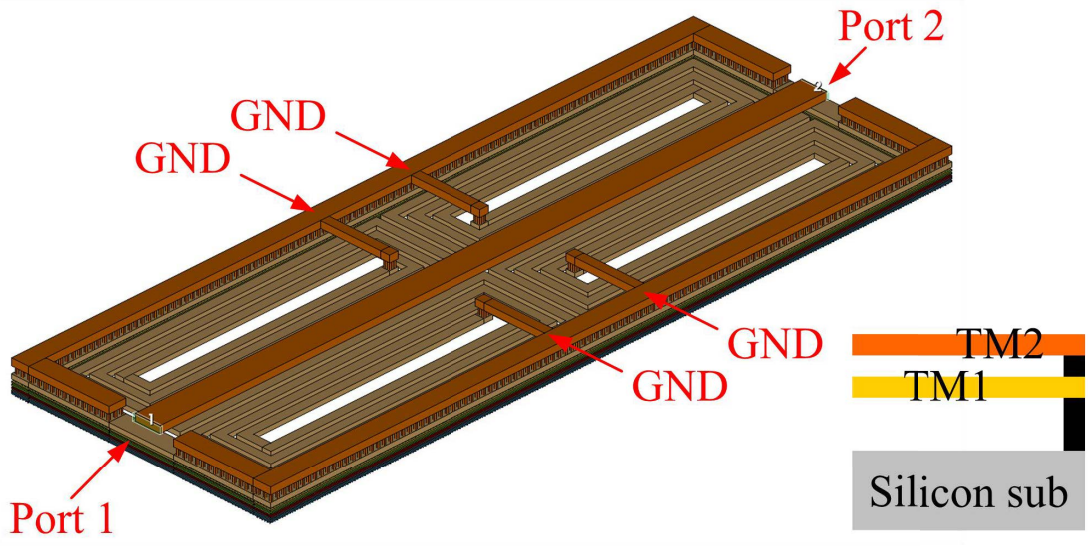
These BSFs share some of the operational principles of those in [111]-[113], but are simpler in terms of circuit configuration while being able to circumvent some of these deficiencies. Nevertheless, they were also validated in the low region of the microwave band for off-chip RF devices by using different technologies, such as surface-acoustic-wave, lumped-element, and microstrip ones. In [121], an on-chip absorptive notch filter with tunable differential-mode operation was presented. However, it was designed to work in a lower region of the microwave spectrum (2.9–4.3 GHz), and its theoretical circuit model exhibits a quasi-reflectionless behavior instead of a perfectly-absorptive one. As a result, there is a clear necessity for on-chip absorptive/reflectionless BSFs operating in the mm-wave range, aimed at devising energy-efficient/isolator-less RF integrated front-end chains for modern wireless-communication and radar applications.

Note that, when compared to off-chip components, on-chip solutions offer some remarkable advantages not only in terms of miniaturized physical dimensions but also in terms of enhanced reliability and robustness with reduced production cost. The design of an on-chip mm-wave absorptive BSF in CMOS technology is reported in this work. It consists of a symmetrical two-path transversal scheme that is inspired by the absorptive BSF concept in [117]. In the current BSF device, the lossy properties of silicon-based distributed-element resonators are conveniently exploited to attain the two-port reflectionless behavior without additional resistors for the stopband RF-power absorption. This is done while achieving a second-order deep-notch BSF response. The layout and the theoretical foundations of the developed mm-wave absorptive BSF are presented in Section 3.2. A 24.5-GHz on-chip prototype is designed, fabricated, and measured in Section 3.3. Finally, the conclusions are articulated in Section 3.4.

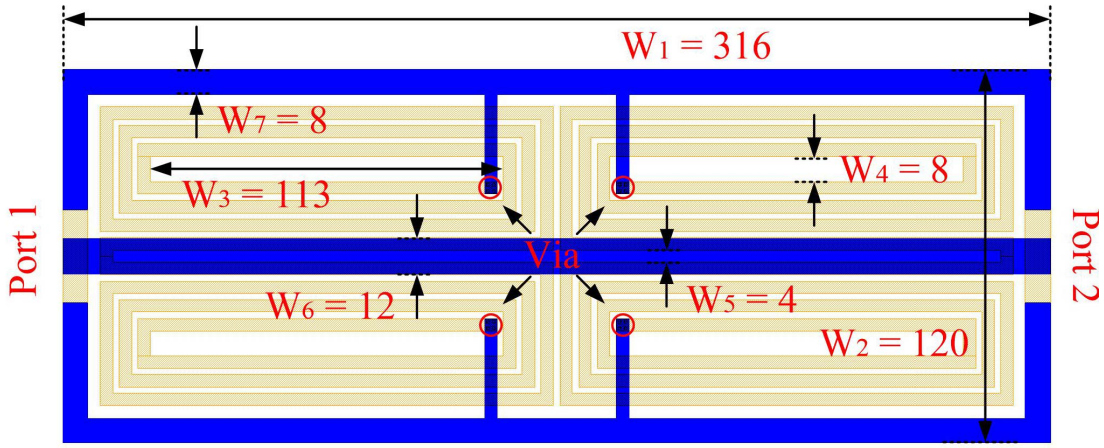
3.2 Design of On-Chip Passive-Integrated Millimeter-Wave Absorptive BSF

The 3-D and 2-D views corresponding to the designed passive-integrated mm-wave absorptive BSF are shown in Figure 3.1 (a) and (b), respectively. As illustrated in Figure 3.1 (a), this design consists of three parts: a metal strip line, two spiral-shaped resonators, and a ground ring. The metal stack-up used in this design is also depicted at the bottom right-hand corner of Figure 3.1 (a). In Figure 3.1 (b), the physical dimensions of the designed filter are illustrated. It is noted that the width of the metal strip and the gap between them is 4 μm and 2 μm, respectively, unless otherwise marked. The dielectric constant of SiO_2 is 4.1 and the loss tangent is 0.01. Figure 3.1 (c) depicts the equivalent lumped-element circuit. It consists of a two-path transversal BSF network, whose electrical paths are as follows: reference impedance Z_0 = 50 Ω and a BSF center frequency f_0 = 25.5 GHz.

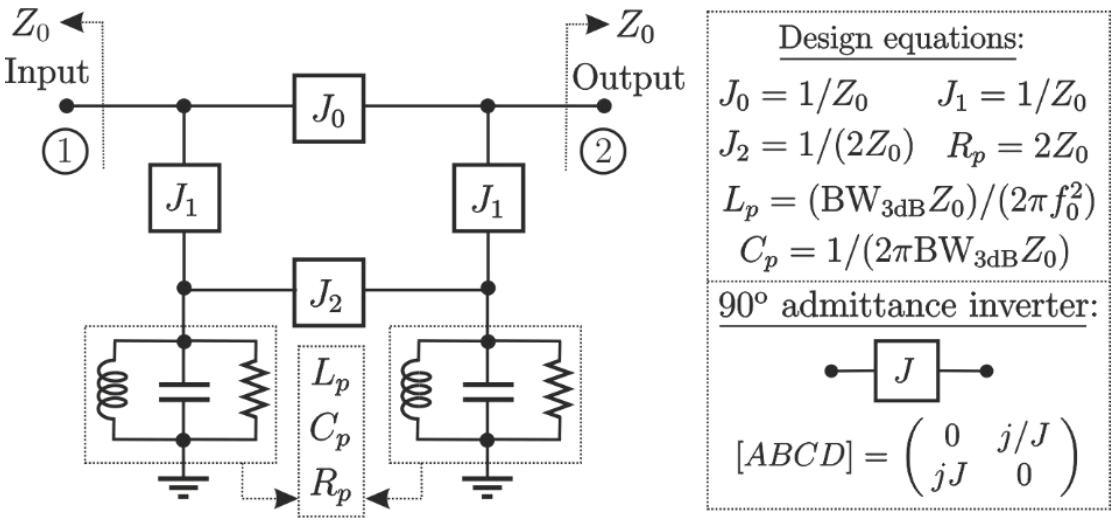
The primary signal-propagation path is implemented in the top metal layer (marked as TM2). It is made up of a quarter-wavelength transmission-line segment at f_0 with a Z_0 characteristic impedance. It can be represented as a 90° admittance inverter between input and output at f_0 with $J_0 = 1/Z_0$. The secondary signal-propagation path is implemented in the bottom metal layer (marked as TM1). It is shaped by two short-ended spiral-shaped transmission-line resonators (modeled as parallel-type resonators R_p, L_p, C_p). These resonating lines are inductively coupled between them and to the main path. Thus, these couplings can also be modeled through 90° admittance inverters with admittance-inversion constants J_1 and J_2, respectively.


Port 2
GND
GND
GND
GND
TM2
TM1
Silicon sub
Port 1

(a)


W1 = 316
W7 = 8
W3 = 113
W4 = 8
Port 1
Via
Port 2
W6 = 12
W5 = 4
W2 = 120

(b)


Z0
Input
Z0
Output
J0
J1
J1
J2
Lp
Cp
Rp
Design equations:
J0 = 1/Z0
J1 = 1/Z0
J2 = 1/(2Z0)
Rp = 2Z0
Lp = (BW3dB Z0)/(2π f0²)
Cp = 1/(2πBW3dB Z0)
90° admittance inverter:
J
[ABCD] = (0 j/J; jJ 0)

(c)

Figure 3.1**.** Designed on-chip passive-integrated mm-wave absorptive BSF. (a) Layout (3-D view). (b) Layout (2-D view with indication of dimensions in μm). (c) Equivalent lumped-element circuit (Z_0: reference impedance; f_0: BSF center frequency; R_p, L_p, and C_p: resistance, inductance, and capacitance of the lossy parallel-type lumped-element resonators; J variables: 90°-admittance-inverter constants).

In this manner, by means of a destructive-signal-interference phenomenon between the two signal paths, a second-order BSF response with infinite attenuation at f_0 can be ideally attained. Furthermore, theoretically-null power reflection at any frequency is simultaneously achieved in the equivalent lumped-element circuit in Figure. 3.1 (c). This is achieved when the equations therein shown are satisfied. In the physical implementation in Figure. 3.1 (b), this is done by properly optimizing the geometrical variables, mainly the coupling regions associated to the admittance inverters and the lossy resonators at the bottom layer. In this manner, low-RF-power-reflection capability and a deep-notch second-order BSF transmission response are obtained.

For illustration purposes, Figure. 3.2 shows a comparison between the electromagnetically-(EM)-optimized power transmission and reflection responses of the absorptive BSF layout in Figure. 3.1 (a) and (b) and the theoretical ones of its equivalent lumped-element circuit in Figure. 3.1 (c). The EM simulations were performed with the commercial tool AXIEM from Cadence-AWR. As demonstrated, a reasonably close agreement between theoretical and EM-simulated responses is obtained. In the EM results, a notch maximum-attenuation level of 23 dB at 25.5 GHz and a minimum input-power-matching level of 18.8 dB in the represented frequency range from DC to 60 GHz are obtained.

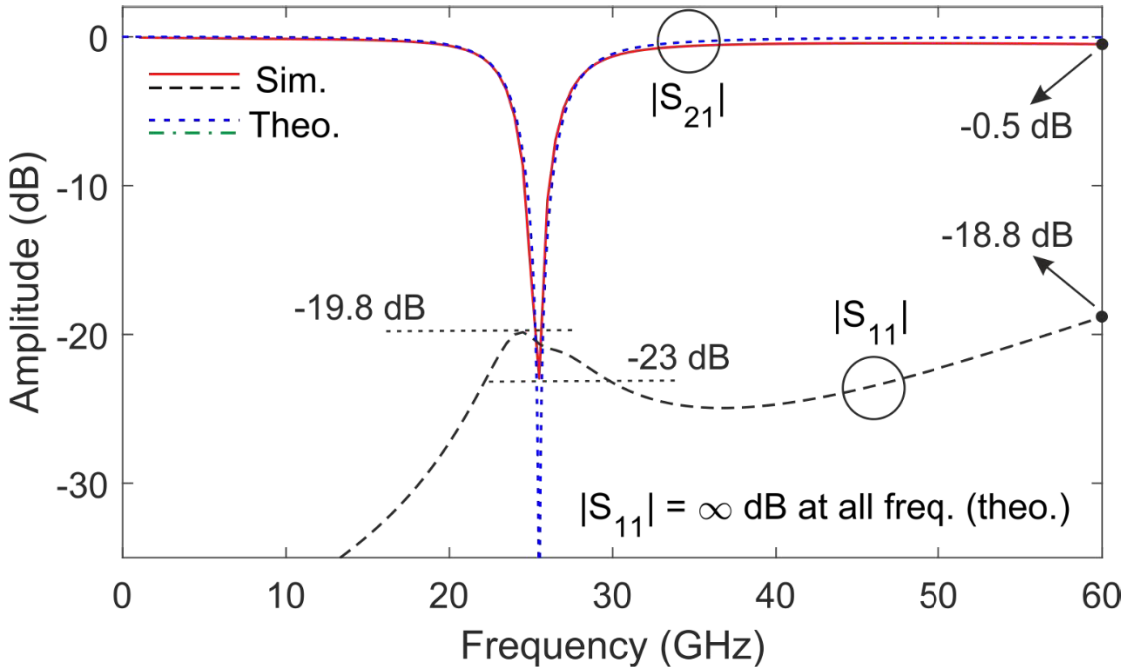


Figure 3.2**.** EM-simulated [layout in Figure 3.1.(a) and (b) with dimensions therein indicated] and theoretical [equivalent lumped-element circuit in Figure 3.1.(c) for Z_0 = 50 Ω, f_0 = 25.5 GHz, and BW_{3dB} = 4.58 GHz: J_0 = J_1 = 0.02 S, J_2 = 0.01 S, R_p = 100 Ω, L_p = 56.05 pH, and C_p = 0.693 pF] power transmission ($|S_{21}|$) and reflection ($|S_{11}|$) responses of the designed absorptive BSF.

Moreover, to further demonstrate that the proposed approach is flexible for BSF design, parametric studies are conducted here as well. Particularly, the values of W1 and W12 are varied to show that the center frequency of the designed BSF could be effectively shifted to some extent. As can be seen from Figure 3.3, by varying the value of W12, the notch frequency could be fine-tuned without significantly affecting the absorptive natural.

To support course-tuning of the notch frequency, the value of W1 is used and the EM-simulated results are plotted in Figure 3.4. As can be seen, by valuing the value of W1 from 120 μm to 80 μm with a step of 20 μm, the notch frequency could be significantly changed without affecting the absorptive nature.

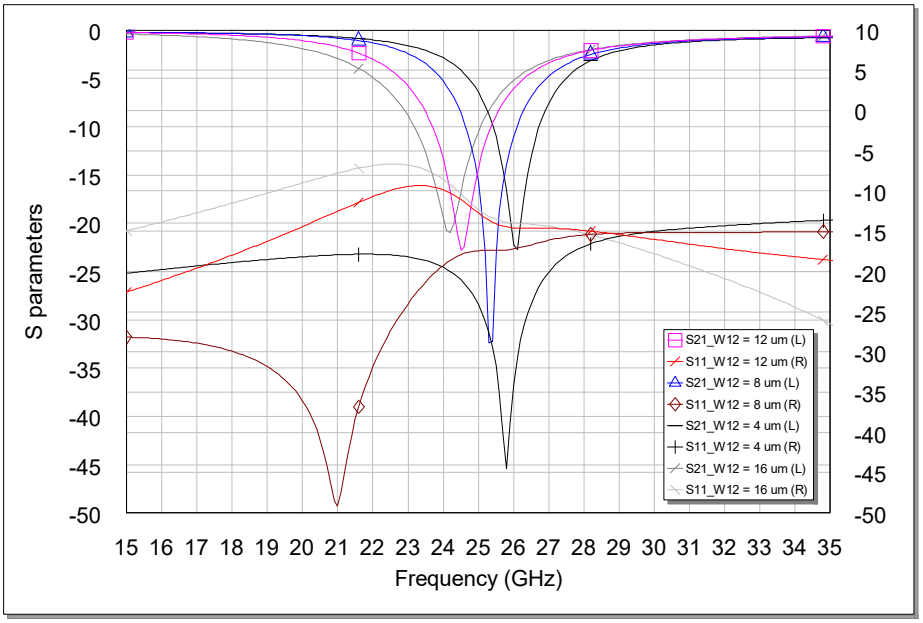


Figure 3.3. EM-simulated S-parameters of the designed BSF with different values of W12. Note: the left and right Y-axes are referred to S_{21} and S_{11}, respectively.

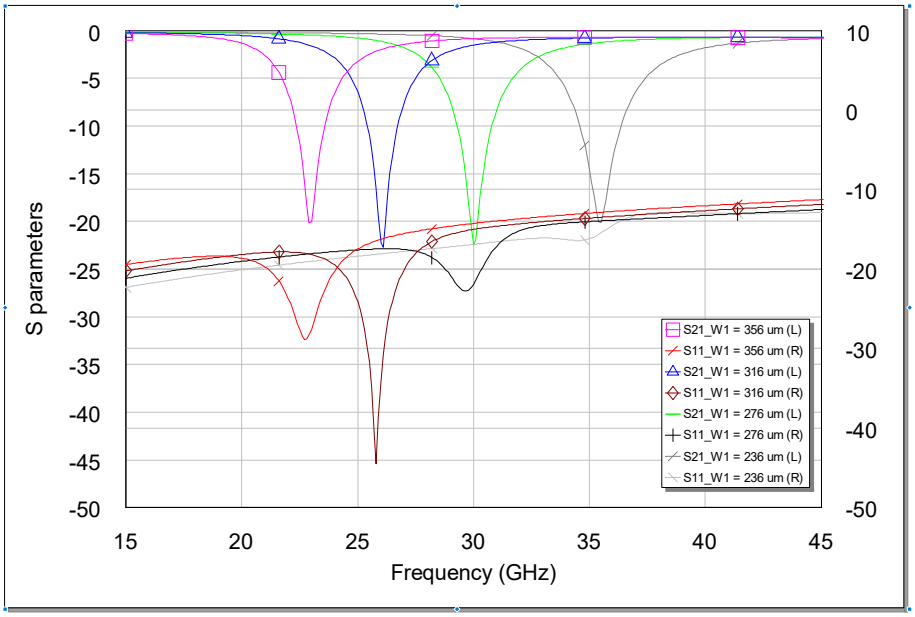


Figure 3.4. EM-simulated S-parameters of the designed BSF with different values of W1. Note: the left and right Y-axes are referred to S_{21} and S_{11}, respectively.

Finally, in order to check the robustness of the designed filter layout to manufacturing tolerances, a sensitivity analysis [i.e., variation of 5% of the line widths and spacing with regard to the values indicated in Figure 3.1 (b)] has been conducted. As shown in Figure 3.5, where the resulting power transmission and reflection

responses are represented, the absorptive behavior is well preserved, thus being tolerant to these variations. The attenuation-notch level is also kept to a large extent, although the relevant spectral location is slightly shifted.

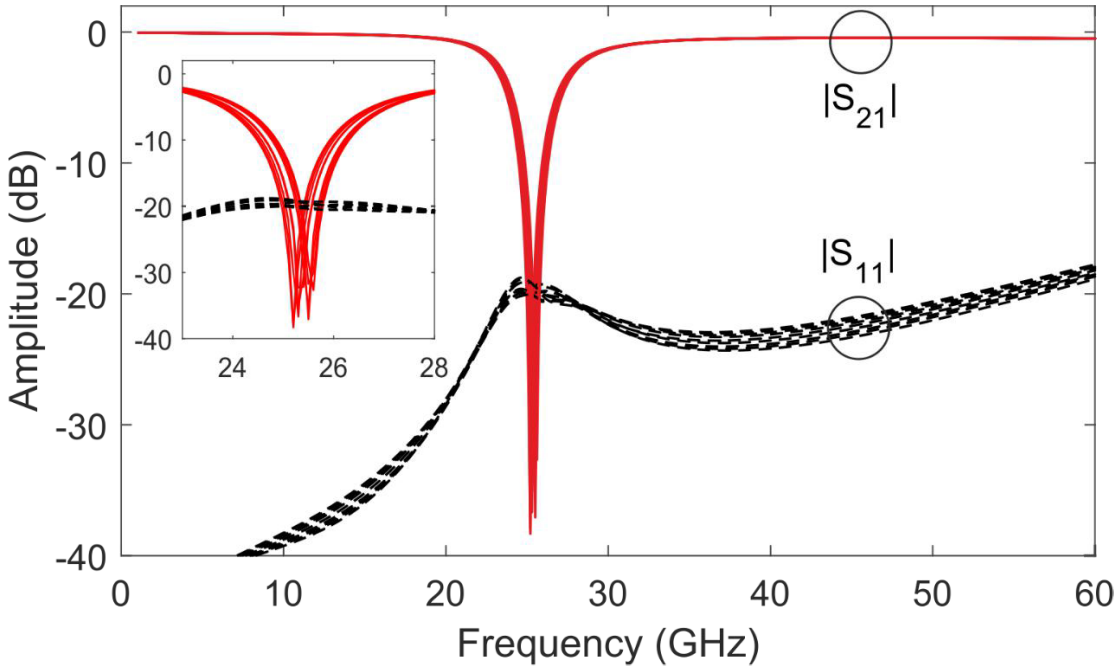
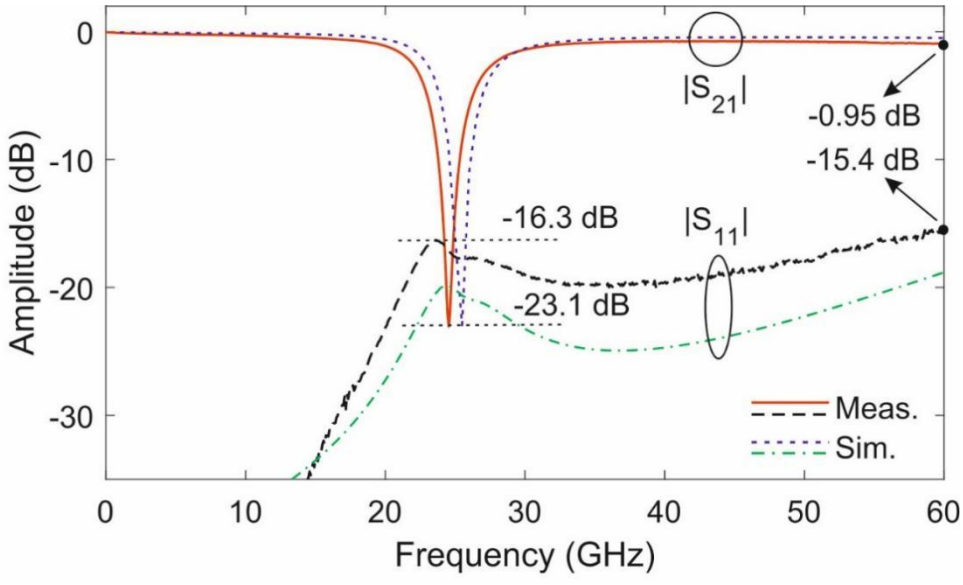


Figure 3.5. Sensitivity analysis of the designed on-chip passive-integrated mm-wave absorptive BSF in terms of EM-simulated power transmission ($|S_{21}|$) and reflection ($|S_{11}|$) responses (variation of 5% of line widths and spacing with regard to the values indicated in Figure 3.1 (b)).

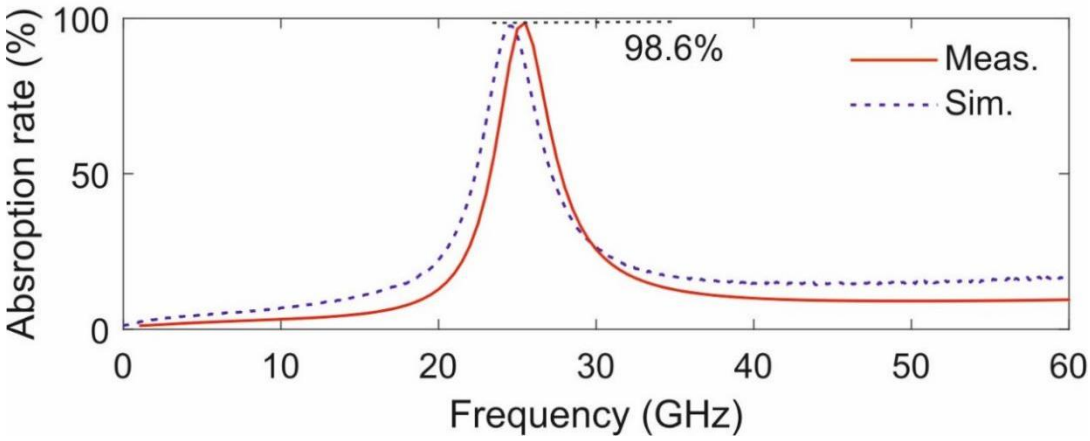
3.3 Experiment Results

A prototype of the designed passive-integrated mm-wave absorptive BSF has been fabricated in standard 0.13-μm CMOS technology and tested. For its measurements in terms of *S*-parameters up to 60 GHz via on-wafer ground-signal-ground (G-S-G) probing, an N5290A vector network analyzer from Keysight was used. The simulated and measured power transmission and input-reflection responses of the prototype are compared in Figure 3.6, along with its simulated and measured power-absorption rates. As observed, apart from a frequency shifting as predicted by the sensitivity analysis carried out in the Section II, a fairly close agreement between predicted and experimental results is obtained from which it can be concluded that the developed filter

concept is verified.



(a)



(b)

Figure 3.6**.** Measurement results of the designed BSF, (a) simulated and measured power transmission ($|S_{21}|$) responses of the designed absorptive BSF, and (b) simulated and measured power-absorption rates of the designed absorptive BSF. Note that for a classic reflective-type BSF the power-absorption rate would be theoretically equal to 0% at any frequency.

The minor discrepancies observed between simulated and measured power-reflection levels are attributed to the probes and G-S-G pads, which were not considered in the simulation process due to the increased computational cost. The main

measured performance metrics of the designed BSF are as follows: second-order notched band with center frequency of 24.54 GHz, 10-dB-attenuation-referred absolute bandwidth of 1.54 GHz (i.e., 6% in relative terms), and maximum attenuation equal to 23.1 dB. The minimum input-power-matching level in the proximities of the stopband is 16.3 dB and below 15.4 dB for the full plotted frequency range. The maximum power-attenuation level in the passband region is 0.95 dB as measured at 60 GHz. Moreover, the power-absorption ratio at the notch frequency is 98.6%, as a demonstration of its absorptive nature. Last, a microphotograph of the fabricated chip is also included in Figure 3.7 with indication of its main parts/elements, whose size (excluding pads) is 0.32 mm × 0.12 mm.

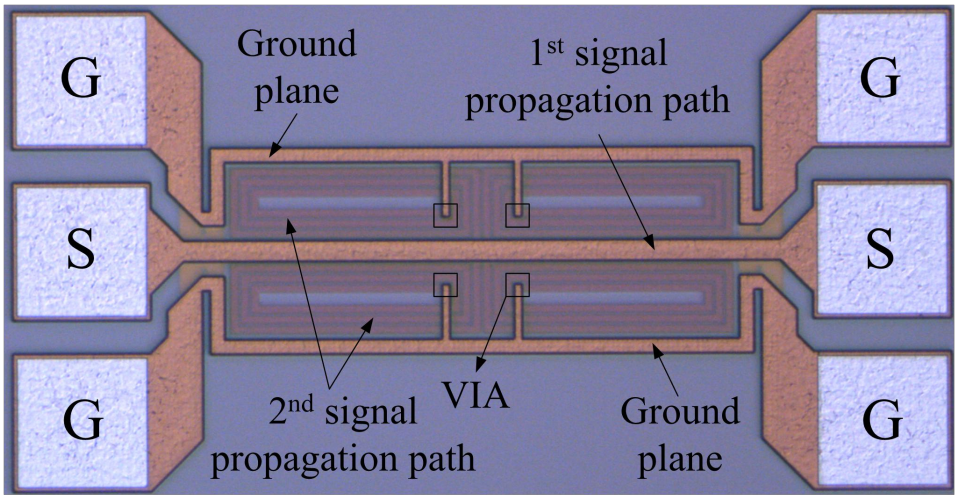


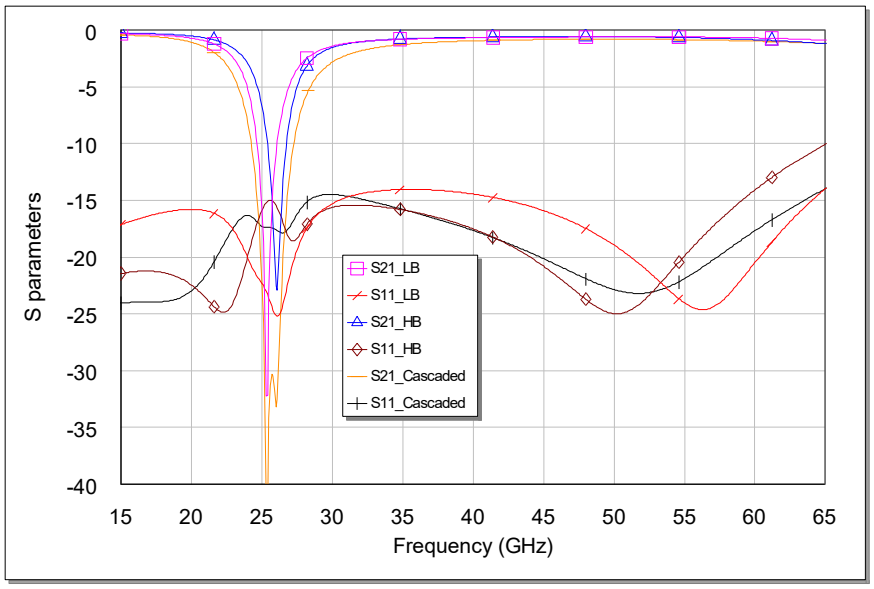
Figure 3.7. Die microphotograph of the designed BSF in Figure 3.5.

Table 3.1 Performance comparisons with state-of-the-art BSFs

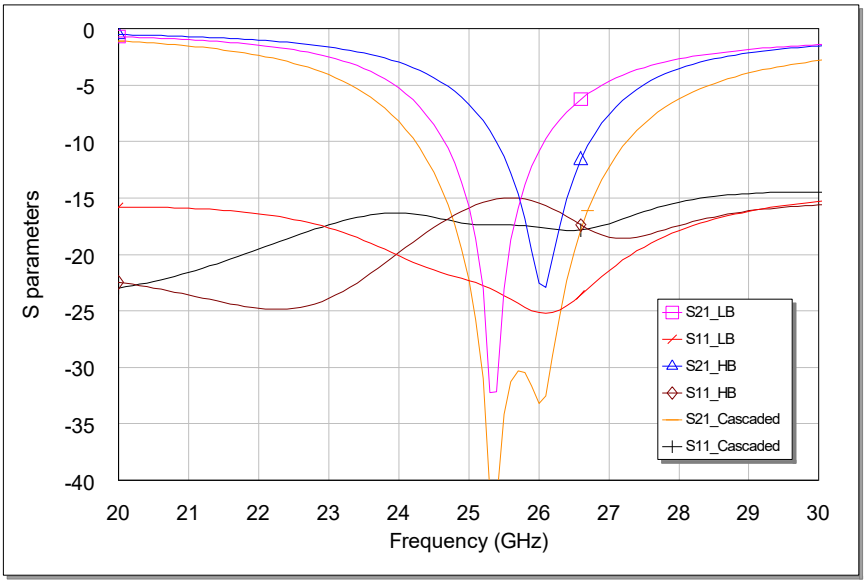
	Center freq. (GHz)	S21 (dB)	S11 (dB)	Tech.
Lee, T-MTT 2020	2	25	25	PCB
Guyette, M-TTS 2009	2	42	10	PCB
Psychogiou, T-MTT 2017	0.23	30	30	Lump elements
Snow, MTT-S 2012	3.6	18	30	Sub-integrated resonators
This work	24.5	23	15	130-nm CMOS

3.4 Furtherwork

In order to further demonstrate that the presented design approach for on-chip absorptive BSF is feasible for multi-band applications, two additional design examples are described in this section. In the 1st example, two BSFs operating at close frequency bands are presented; one is located at 25.3 GHz and the other is at 26.1 GHz. The EM simulation results are given in Figure 3.8 (a) and a more detailed view between 20 and 30 GHz can be seen in Figure 3.8 (b).



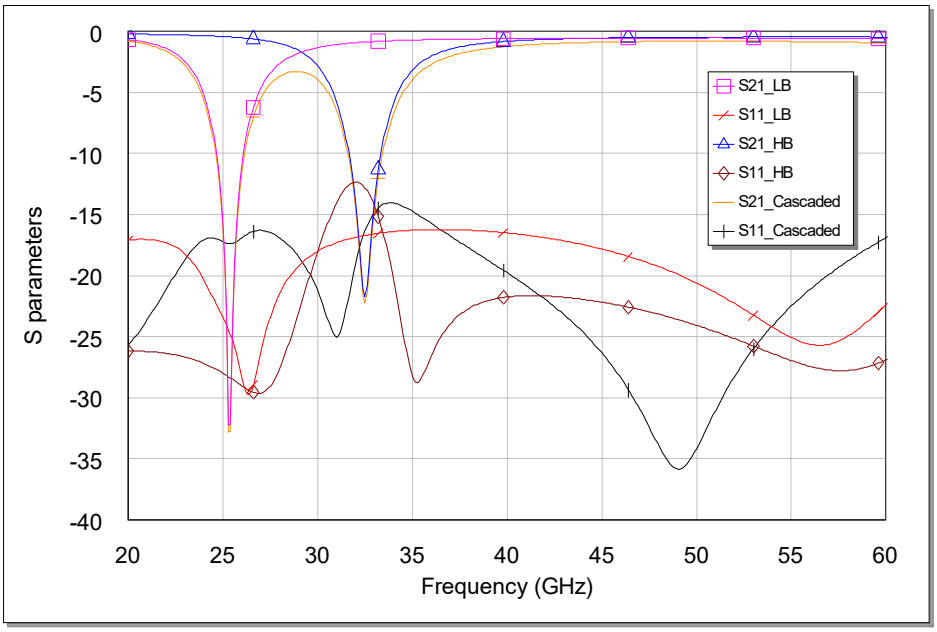
(a)



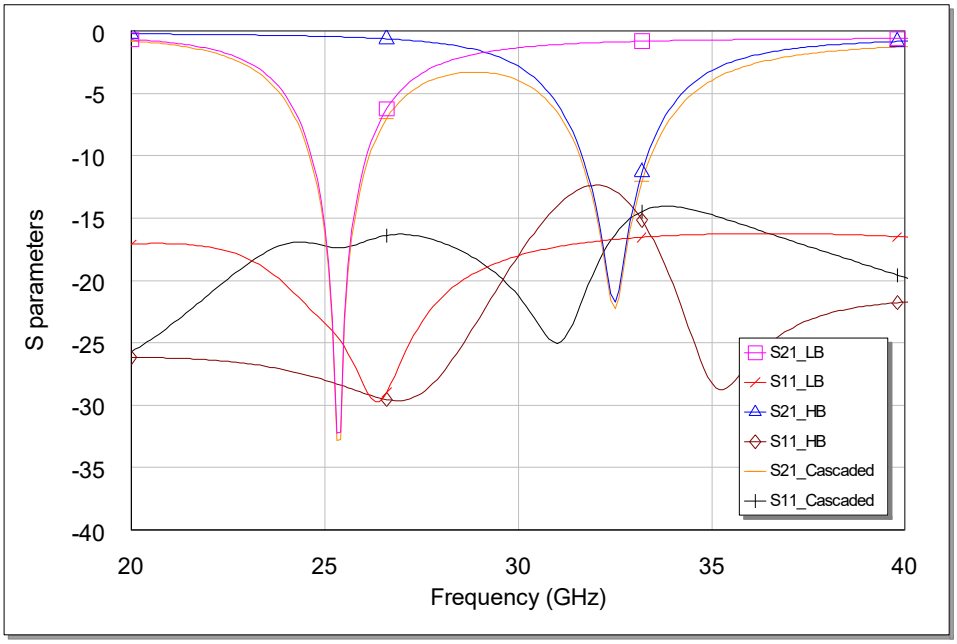
(b)

Figure 3.8. EM simulated S-parameters for two cascaded BSFs. Note: the operatiton frequencies of these two BSFs are close to each other.

In the 2nd design, two absorptive BSFs are also cascaded like the one presented in the 1st example. The difference is that their operation frequencies are quite some distance from each other. The EM simulation results are given in Figure 3.9. As can be seen, the absorptive feature is still valid even if two BSFs are cascaded and their operation frequencies are very far from each other. In this design, the lower frequency notch remains unchanged and it remains at 25.3 GHz. The higher frequency notch is shifted to 32.5 GHz by reducing the overall length of the EM structure. Therefore, it once again demonstrates that the presented design approach is feasible in practice.



(a)



(b)

Figure 3.9. EM simulated S-parameters for two cascaded BSFs. Note: the operatiton frequencies of these two BSFs are far from each other.

3.5 Conclusions

In this chapter the design of a mm-wave passive-integrated absorptive BSF has been reported. This BSF device absorbs the non-transmitted RF-signal energy within its

stopband region instead of retuning it back to its input terminal. In this manner, the creation of RF-power reflections, which can compromise the operation of earlier active stages in modern energy-efficient isolator-less integrated RF front-ends, can be avoided. A 24.5-GHz prototype has been successfully fabricated in 0.13-μm CMOS technology and measured. A close agreement between the simulated and measured results is obtained, which proves the feasibility of this concept. Based on these results, it is concluded that the proposed structure might be useful in practice for isolator-less mm-wave transceivers.

Chapter 4: Millimeter-Wave Wide-Band Bandpass Filter in CMOS Technology Using a Two-Layered Highpass-Type Approach with Embedded Upper Stopband

Abstract—An on-chip mm-wave broad-band BPF developed in CMOS technology is reported. It is based on a two-layered implementation in which the circuit structure patterned in the top layer exhibits a highpass-type filtering response, whereas an upper stopband is created by the bottom-layer cell when coupled to the top-layer one to obtain a composite overall quasi-elliptic-type wide-band BPF functionality. The locations of the TZs, which confer sharp-rejection capabilities to the total BPF, can be flexibly adjusted with the values of the capacitors that are employed in both layers. An equivalent lumped-element circuit model of the proposed wide-band BPF approach is also provided and applied to multi-stage BPF arrangements for higher-selectivity designs. Furthermore, for practical-demonstration purposes, an on-chip passive-integrated single-stage broad-band BPF prototype on silicon with 34.5-GHz center frequency and 61.2% 3-dB relative bandwidth is designed, manufactured, and characterized.

4.1 Introduction

With the future deployment of upcoming RF wireless systems operating at ever higher frequency ranges (e.g., beyond 5G), the demand of high-performance RF circuits designed at mm-wave regions is increasing. Within this trend, the development of silicon-based mm-wave ICs for system-on-chip (SoC) modules is attracting considerable attention as enabling technology to support these modern RF applications. On-chip passive BPFs are critically important RF devices at both the transmitter and receiver ends, as they make it possible to mitigate spurious signals created by active stages (e.g., frequency converters and amplifiers). They also reject out-of-system

interference signals and out-of-band noise that can degrade the quality-of-service (QoS) at the customer end. Moreover, wide-band operational characteristics for pre-selection RF BPFs in mm-wave receivers are now very much in demand in multiple scenarios, such as ultra-high-data-rate wireless-communication or for ultra-wideband radar systems.

In the technical literature, several examples of mm-wave BPFs have been reported; among them are those based on passive-integrated[122], substrate-integrated-waveguide (SIW) [123], [124], and microelectromechanical-systems (MEMS) technologies [125]. Nevertheless, they cannot be completely integrated in SoC solutions, which makes them less appealing for ultra-compact mm-wave transceiver modules. On the other hand, recent studies on on-chip BPFs for mm-wave applications using different technologies, such as GaAs, CMOS, and SiGe, have mostly focused on designs with absolute bandwidths lower than 40% [34], [53]-[58]. Some examples of on-chip mm-wave BPFs with fractional bandwidths above this value were reported in [126]-[128], but they show drawbacks in terms of large in-band power-insertion loss (higher than 3 dB) as a drawback and/or poor out-of-band power-rejection levels (close to 5 dB is some cases). Clearly, there is a need of new circuit solutions for ultra-broad-band low-loss mm-wave integrated BPFs.

In this section, a new approach to on-chip mm-wave wide-band BPF with sharp-rejection characteristics is proposed. It exploits a two-layered structure, in which the top-layer cell exhibits a quasi-elliptic-type highpass filtering response whereas the bottom-layer structure adds a wide upper stopband into it when coupled to the top-layer circuit part. In this manner, a wide-band BPF response with low in-band insertion-loss levels can be realized in the entire RF device.

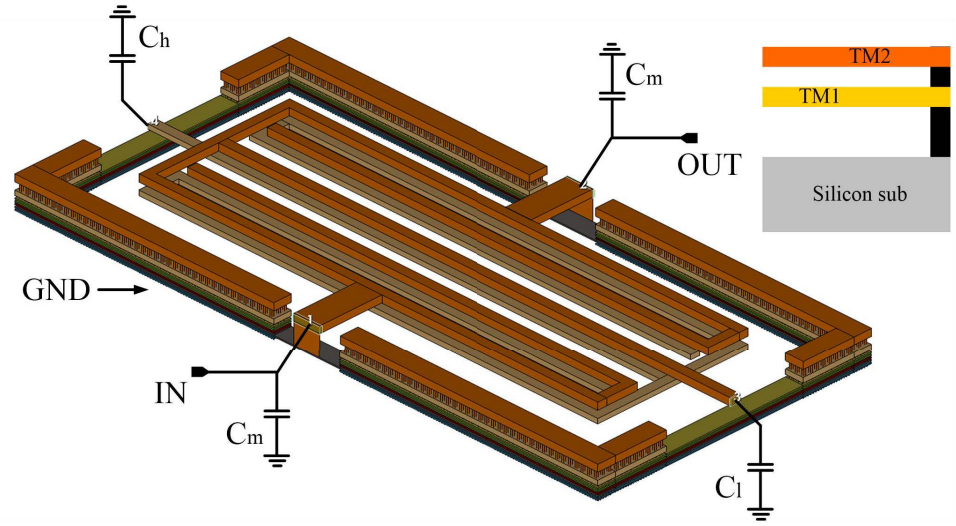
The organization of the rest of this chapter is as follows. In Section 4.2, the physical structure, RF operational principle with associated parametric analysis, and equivalent lumped-element circuit model of the engineered passive-integrated wide-band BPF are

presented. In Section 4.3, for demonstration purposes, an on-chip silicon-based wide-band BPF prototype with center frequency of 34.5 GHz and 3-dB fractional bandwidth of 61.2% is developed, characterized, and compared with the other state-of-the-art designs. Finally, Section 4.4 provides a summary and the main concluding remarks of this study.

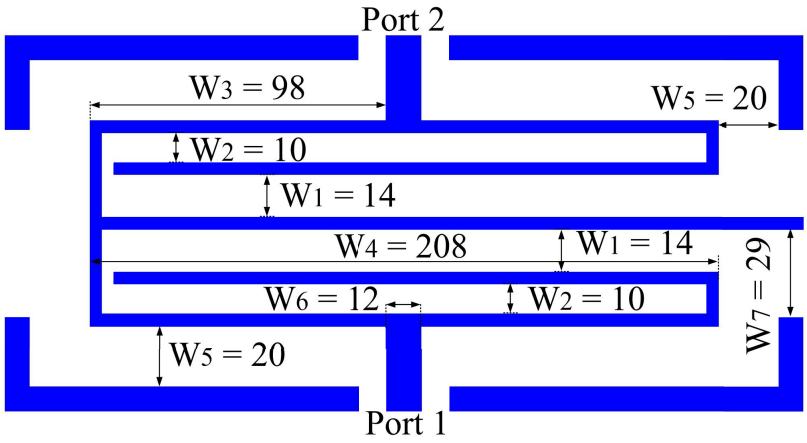
4.2 On-Chip Passive-Integrated Millimeter-Wave Wide-Band BPFs

4.2.1 Structure, Operational Principle and Parametric Analysis

The 3-D and 2-D views of the layout of the proposed on-chip mm-wave passive-integrated wide-band BPF are provided in Figure 4.1 (a) and (b), respectively. As shown in Figure 4.1 (a), the circuit consists of a two-layered realization with three parts, as follows: (i) a spiral-shaped metal-strip cell with a middle stub ended in a capacitor C_l in the top layer that is connected to the input/output ports with capacitors C_m in the top layer, (ii) a mirrored-oriented replica of the previous cell in the bottom layer with loading capacitor C_h in the middle stub and coupled to the top layer, and (iii) a ground ring that uses all metal layers stacked together. The metal stack-up employed in this design is also provided at the top right corner of Figure 4.1 (a). The thickness of TM1 and TM2 are 2 μm and 3μm, respectively. The vertical gap between them is 2 μm. Furthermore, the top-view of the designed BPF with dimensions is shown in Figure 4.1 (b). It is noted that only the top metal layer is shown for a better visibility, since the mirrored structure implemented in bottom layer has identical physical dimensions. The width of metal strip is 4 μm, unless otherwise indicated.



(a)



(b)

Figure 4.1. Designed on-chip CMOS passive-integrated mm-wave wide-band BPF. (a) Layout (3-D view). (b) Layout (2-D view of the top layer with indication of dimensions in μm).

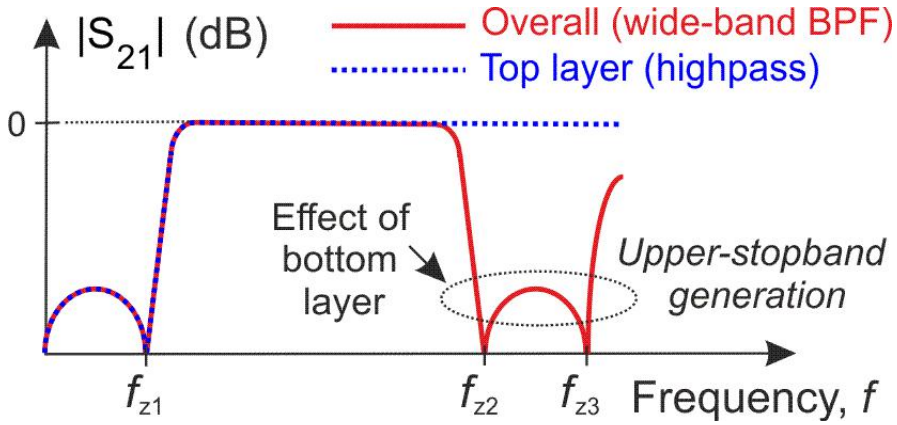
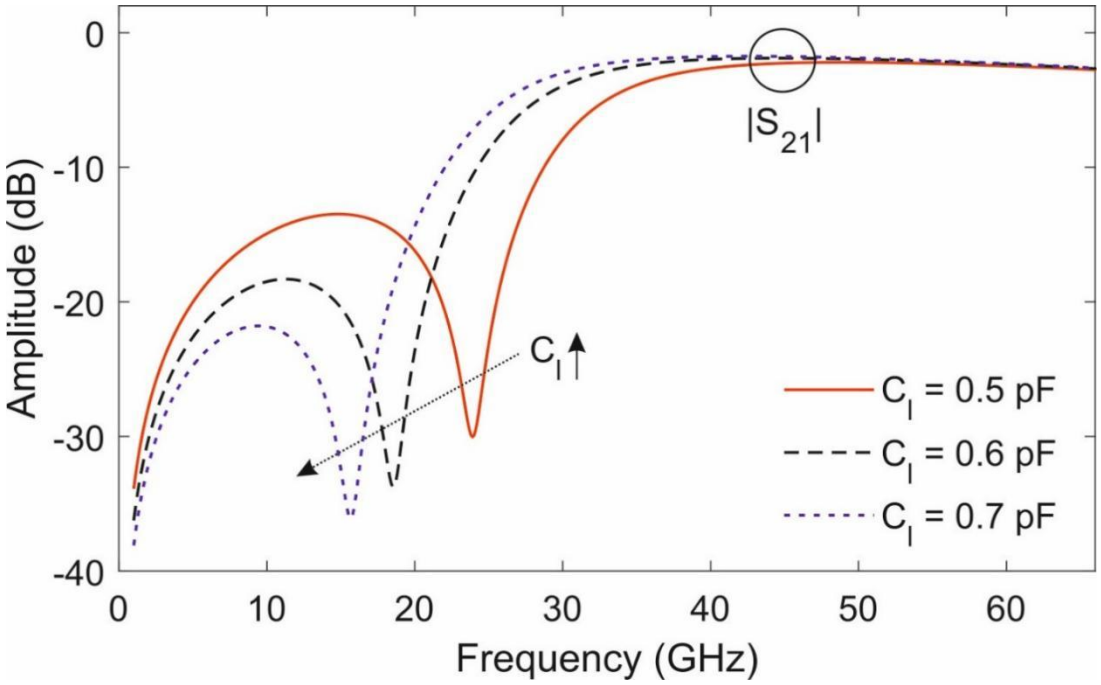


Figure 4.2. The concept of the designed BPF.

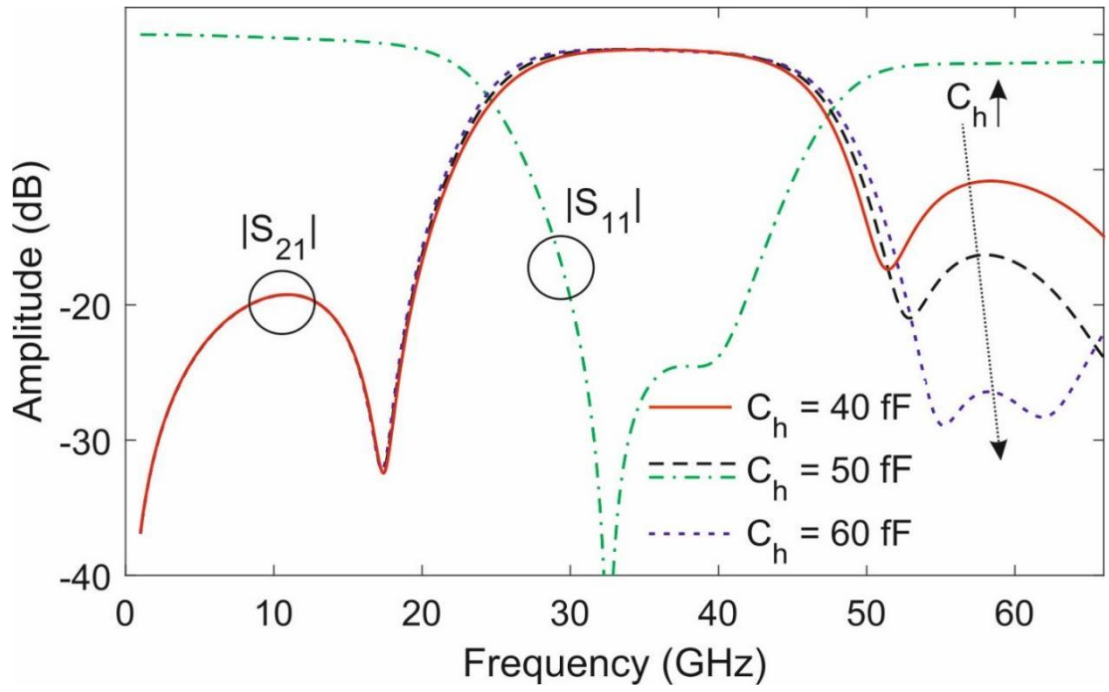
As illustrated in Figure 4.2, the conceptual RF operational principle of this wide-band BPF circuit in terms of power transmission response is as follows:

- The structure in the top layer (TM2) exhibits a quasi-elliptic-type highpass response, where the position of the lower TZ at f_{z1} can be adjusted by means of the capacitor C_l that loads the middle stub on it. The input/out capacitors C_m and input/output open-ended stubs make it possible to control the in-band power-matching levels in the overall BPF passband.
- The mirrored-oriented spiral-shaped metal-strip cell in the bottom layer (TM1) introduces two upper TZs at f_{z2} and f_{z3} in the overall transfer function when coupled to the upper layer so that a composite wide-band BPF response is obtained. In this case, the locations of the upper TZs can be flexibly tuned with the capacitor C_h.

In order to verify the aforementioned RF operational principles, electromagnetic-(EM)-based simulations with the commercial tool AXIEM from NI-AWR have been carried out, as depicted in Figure 4.3. Specifically, Figure 4.3 (a) shows the EM-simulated power transmission response of only the top-layer structure [i.e., circuit in Figure 4.1(a) and (b) without the bottom layer] for different values of C_l. As observed, sharp-rejection highpass filtering profiles are obtained in all cases, where higher values of C_l result in lower spectral locations for the finite TZ at f_{z1}. Conversely, Figure 4.3 (b) represents the EM-simulated power transmission and input-reflection responses of the overall BPF in Figure 4.1(a) and (b) for distinct values of C_h. As demonstrated, larger values of C_h lead to deeper upper-stopband rejection levels by controlling the locations of the upper TZs at f_{z2} and f_{z3} in the overall wide-band BPF response.



(a)



(b)

Figure 4.3. (a) EM-simulated power transmission response ($|S_{21}|$) of the top-layer structure for different values of C_l: lower-TZ control (C_m = 0.16 pF). (b) EM-simulated power transmission response ($|S_{21}|$) and input-reflection responses of the overall wide-band BPF for different values of C_h: upper-TZ control (C_m = 0.16 pF and C_l = 0.6 pF). The values of the physical dimensions in all cases are as indicated in Figure 4.1(b).

Finally, to check the robustness of the designed on-chip wide-band BPF to manufacturing tolerances, a sensitivity analysis was carried out. Figure 4.3 shows the obtained EM-simulated power transmission and input-reflection responses for variations in the values of the line widths and capacitances of 5% and 10%, respectively, with regard to the ones indicated in the layout in Figure 4.1 (b). Whereas the variations in the line widths in this range have almost no effect in the filter performance, the TZ locations are slightly affected by the modifications of the capacitance values. As observed in Figure 4.4, although this can lead to a minor displacement of the overall passband and some variation of the upper-stopband attenuation levels, the BPF characteristics, including in-band power matching, are reasonably maintained.

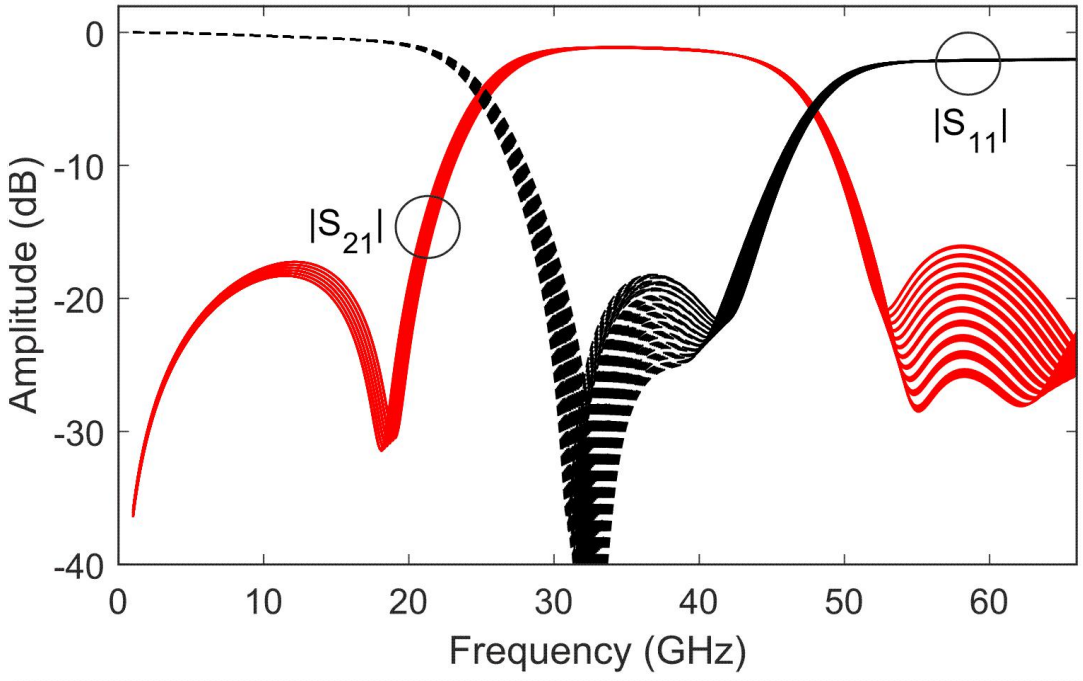


Figure 4.4**.** Sensitivity analysis of the designed on-chip CMOS mm-wave wide-band BPF in terms of EM-simulated power transmission ($|S_{21}|$) and reflection ($|S_{11}|$) responses [variation of 5% of line widths and of 10% of capacitance values with regard to the values indicated in Figure 4.1(b)].

4.2.2 Simplified Equivalent Lumped-Element Circuit Model

From direct inspection of the different physical phenomena and building circuit elements of the passive-integrated mm-wave wide-band BPF schematic represented in

Figure 4.1, an equivalent lumped-element circuit model can be extracted. Such lumped-element-based circuit equivalent is shown in Figure 4.5, along with its application to a two-stage BPF arrangement (generalizable to N stages) for higher-selectivity realizations. In this circuit equivalent, C_m is the matching capacitor, C_c is the coupling capacitor, C_l is used to control the low-frequency TZ, and C_h is employed to adjust one of the high-frequency TZs. Moreover, L_1 and L_2 are the coupled inductors (with coupling coefficient k_{12}) implemented by the top and bottom metal layers (namely TM1 and TM2 as shown in Figure 4.1), respectively, whereas L_3 and L_4 have also an influence on the locations of the low- and high-frequency TZs, respectively. Also note that, in the two-stage design, a cascade capacitor C_{casc} between replicas of the same wide-band BPF cell is exploited.

In order to demonstrate the validity of the equivalent lumped-element circuit illustrated in Figure 4.5, a comparison between the EM-simulated power transmission and reflection responses in Figure 4.3 (a) (C_h = 50 fF) of the wide-band BPF layout in Figure 4.1 and its equivalent lumped-element circuit in Figure 4.4 is provided in Figure 4.5 for a very-broad frequency range. As can be seen, apart from the loss effect that is not considered by the ideal equivalent circuit, it is clear that this lumped-element circuit model properly models all the characteristics of the filter in terms of bandwidth, out-of-band TZs, and rejection levels.

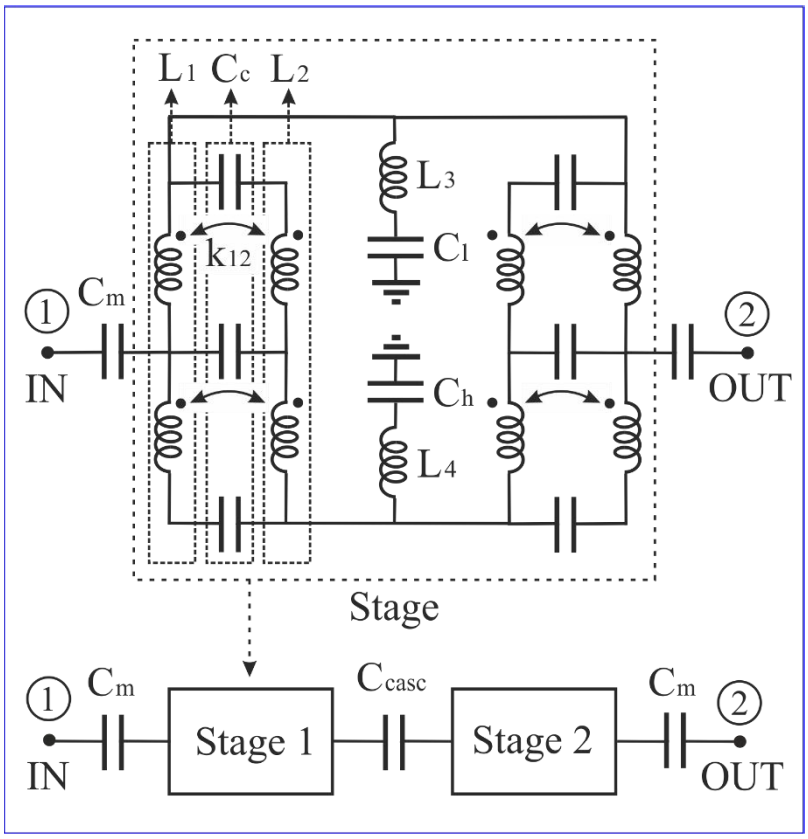


Figure 4.5. Equivalent lumped-element circuit model of the passive-integrated mm-wave wide-band BPF in Figure 4.1 and application to an in-series-cascade two-stage BPF design.

On the other hand, a comparison between the single-stage wide-band BPF circuit and the two-stage arrangement in Figure 4.5 (which was optimized to exhibit a 3-dB bandwidth close to the one in Figure 4.4) is given in Figure 4.6. As shown, increased stopband-attenuation levels are obtained for the two-stage case when compared to the single-stage one, hence proving the suitability of the in-series-cascade approach for higher-rejection filter realizations. Note that the appearance of some narrow-band spurious peaks in the stopband region of the two-stage design is a common phenomenon inherent to the in-series-cascade process as studied in [129], although they become largely mitigated when considering the loss in the practical circuit.

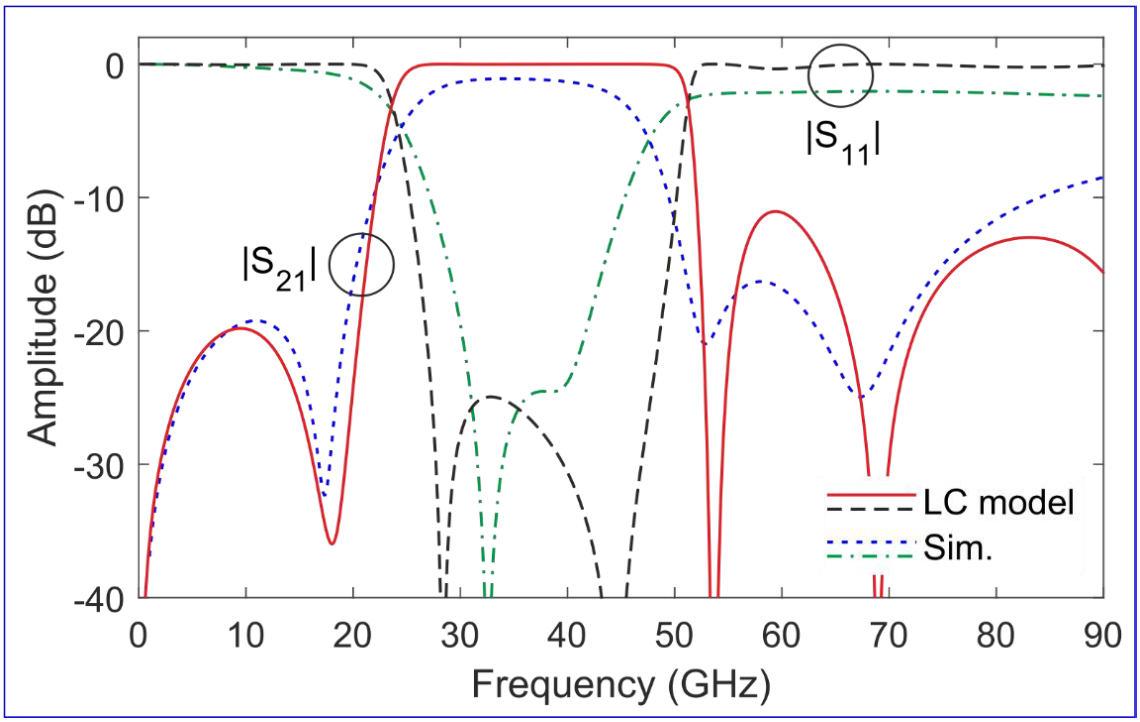


Figure 4.6. Comparison in terms of power transmission ($|S_{21}|$) and input-reflection ($|S_{11}|$) responses between the EM-simulated results in Figure. 4.1 (b) (C_h = 50 fF) and its equivalent lumped-element circuit model in Figure 4.5 (C_m = 0.2 pF, C_c = 55 fF, C_l = 1.1 pF, C_h = 60 fF, $L_1 = L_2$ = 0.16 nF, k_{12} = 0.5, L_3 = 0.1 nH, and L_4 = 0.08 nH).

4.2.3 Extension of the Designed BPF presented in Section 4.2.1

Using the exactly same analysis presented in the previous sub-section, the work could be further extended. In this sub-section, two additional designs will be presented, namely Design 2 and Design 3. As has been shown here, the broadside-coupled structure has the ability to generate a high-frequency TZ. Therefore, by carefully optimizing the physical dimensions of this structure, a BSF or notch filter could be achieved. To further support this point of view, a 3-D view is given in Figure 4.7. What is notable is that the fundamental difference between the Design 1 and Design 2 is one where the filter is not AC-coupled. Furthermore the relatively large capacitor used to generate a low-frequency TZ is no longer required for Design 2.

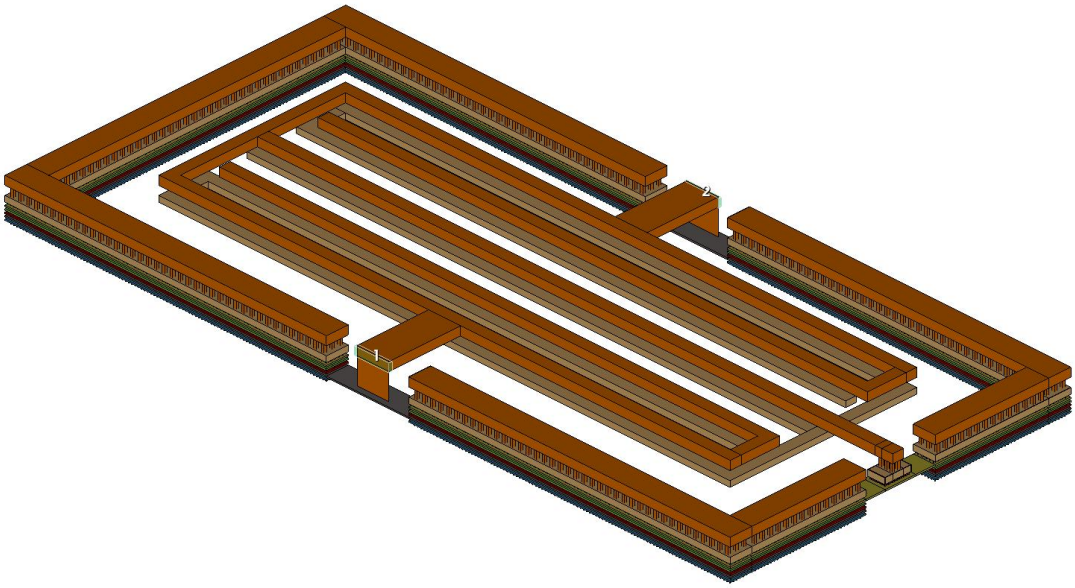


Figure 4.7. The 3-D view of the Design 2.

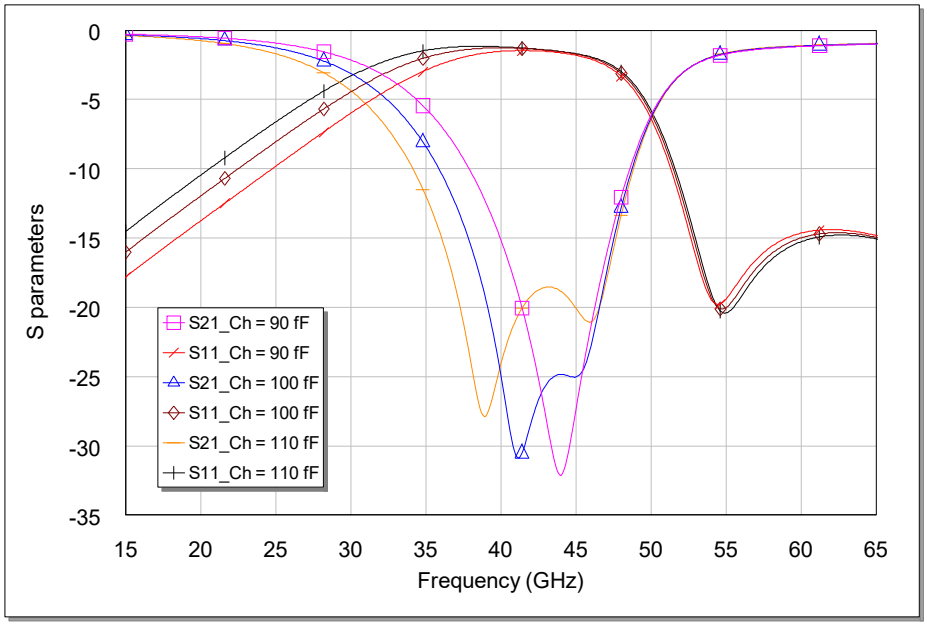


Figure 4.8. Simulated frequency responses of Design 2 with different values of Ch applied.

As Design 2 shares similar features with Design 1, it also has similar behavior as Design 1. By carefully varying the value of ground capacitance, the notch frequency could be effectively tuned, which is shown in Figure 4.8. As illustrated, the bandwidth could be effectively enlarged, if the value of the grounded capacitance, Ch is increased from 90 fF to 110 fF. Furthermore, the 3-D view of Design 3 is given in Figure 4.8.

Comparing with this design with Design 2, the main difference is that the grounded capacitor is connected with the bottom metal layer instead for this design.

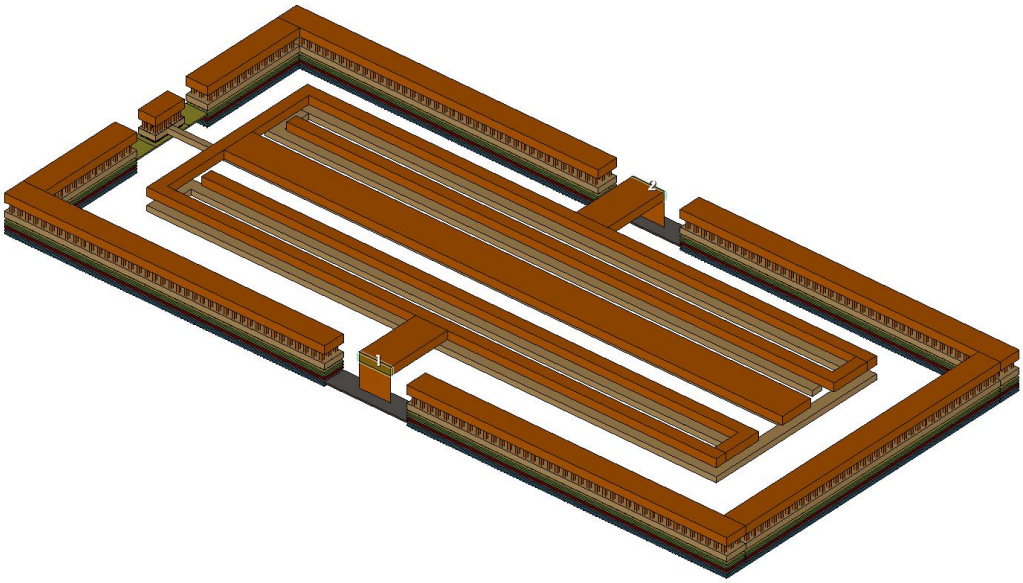


Figure 4.9. The 3-D view of the Design 3.

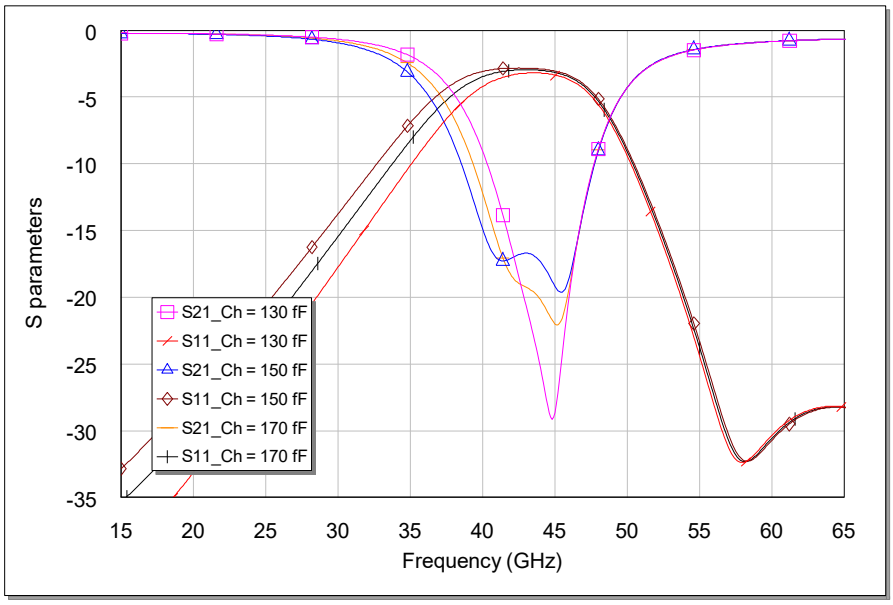


Figure 4.10. Simulated frequency responses of Design 3 with different values of Ch applied.

The simulated frequency responses of Design 3 are shown in Figure 4.9. As illustrated, the bandwidth could be effectively enlarged, if the value of the grounded capacitance, Ch is increased from 130 fF to 170 fF.

To summarise the design procedure used in this work,a simplified flow chart is

presented in Figure 4.11. As illustrated, there are three steps that need to be followed for a BPF design with sharp selectiviey. In Step 1, the resonator needs to be implemented first. As exlianed previously, the metal layers need to be selected. The top metal layers are using thick metal. As a result, the insertion loss could be minimized. However, there vertical gap is limited which has adverse impact on TZ generation at high-freuqency band (HB). In contrast, tight coupling could be obaitned by using low metal layers, but the insertion loss could be large. Thus, there is a design trade-off. Once the metal layers are selected, the first TZ at HB could be optimised accordingly. To do so, either meander line structure or spiral structure could be used. The number of turns, width and length of metal lines need to be carefully determined until the required design specification in terms of out-of-band rejection is met. Follow by this step, an additional TZ could be generated by adding a “small” MIM capacitors. The theroticoal analysis of how to select the value of this capacitor has been presented previously. This additional TZ could be used along with the original TZ generated by the resonstor together to enlarge the out-of-band bandwidth as well as rejection level. Once a satisifactory perfroance is obtained, the design could move to the next step. In Step 3, the main focus is how to generate a TZ at low-frequency band (LB). As previously presented , a relatively “large” MIM capacitor is required. As adding this “large” capacitor will not affect the TZs designed for HB, this step could be treated as an independent design activity. Once the requirement for out-of-band

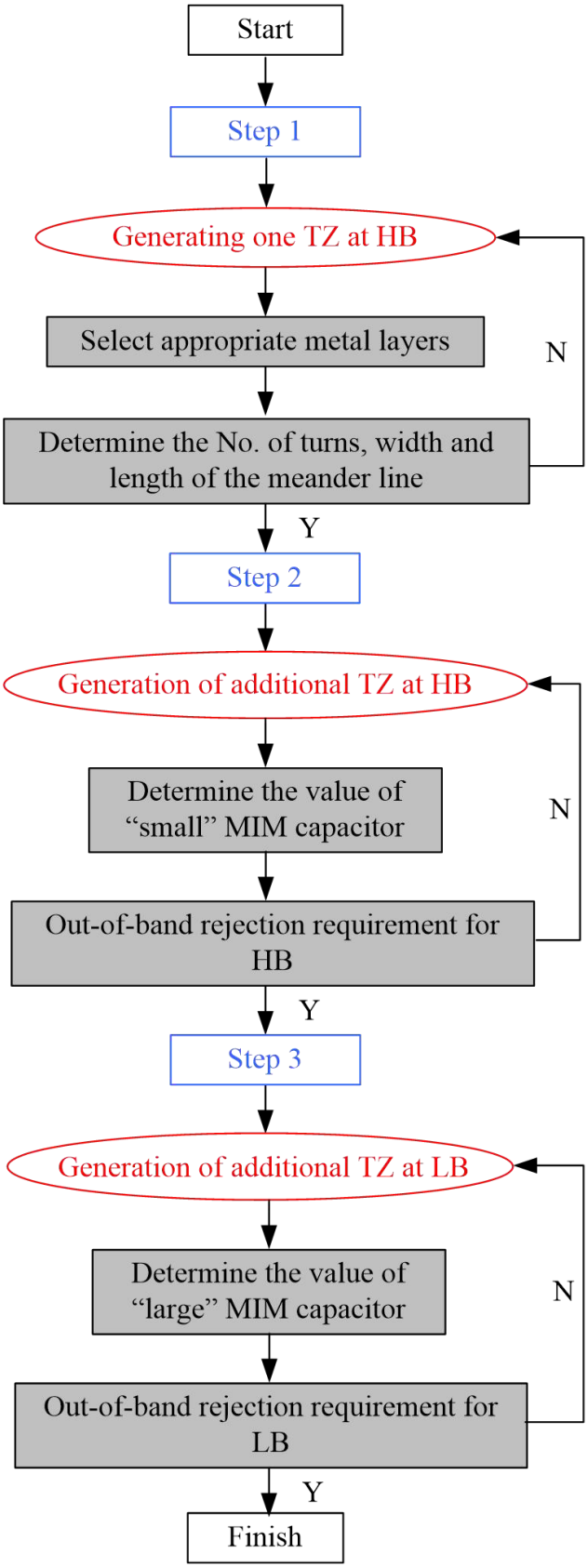


Figure 4.11. Design flow used in this work.

4.3 Experimental Results

4.3.1 Fabrication, Simulation and Measurement

As experimental demonstration of the designed on-chip mm-wave wide-band BPF whose layout was detailed in Figure 4.1. (b), a proof-of-concept prototype was manufactured in CMOS technology and tested. Its characterization process in terms of *S*-parameter measurement up to a maximum frequency of 67 GHz was done by using on-wafer ground-signal-ground (G-S-G) probing and an N5290A vector network analyzer from Keysight. Distributed capacitor for C_h and lumped capacitors for C_m and C_l were employed, respectively.

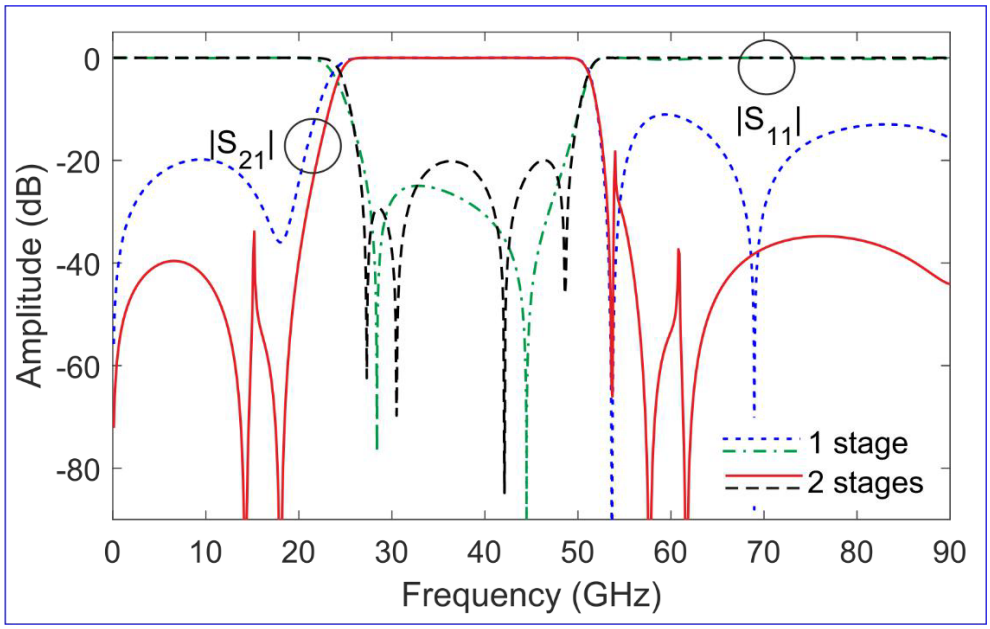
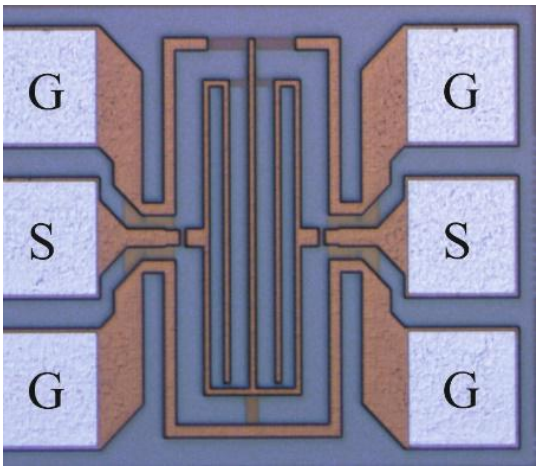


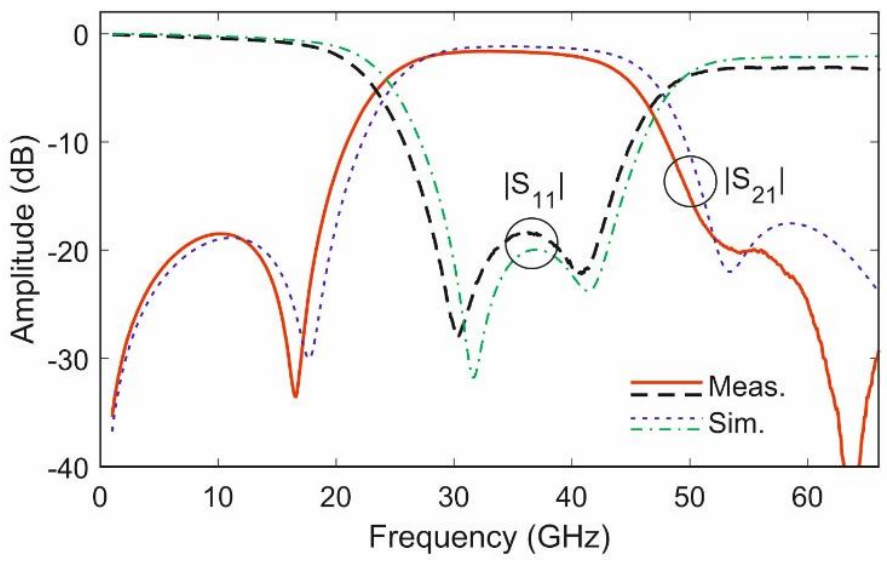
Figure 4.12**.** Comparison in terms of power transmission ($|S_{21}|$) and input-reflection ($|S_{11}|$) responses between the ideal lumped-element single-stage and two-stage designs in Figure 4.6 (single-stage design: same parameters as in Figure 4.6; two-stage design: C_m = 0.3 pF, C_c = 53 fF, C_l = 1.6 pF, C_h = 63 fF, C_{casc} = 0.2 pF, L_1 = 0.2 nF, L_2 = 0.154 nF, k_{12} = 0.53, L_3 = 0.1 nH, and L_4 = 0.089 nH).

The simulated and measured power transmission and input-reflection responses of the developed on-chip CMOS mm-wave wide-band BPF circuit with quasi-elliptic-type filtering response are compared in Figure. 4.12, where its photograph whose size (excluding pads) is 0.264×0.124 mm^2. As can be seen, a reasonable agreement between

predicted and experimental results is obtained. Some minor discrepancies are observed in terms of a frequency shifting to a lower frequency of the overall transfer function and the upper-stopband rejection levels, as also contemplated by the sensitivity analysis in Figure 4.4.



(a)

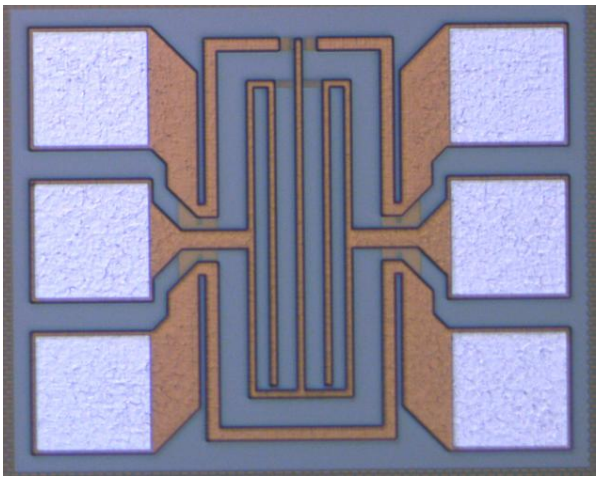


(b)

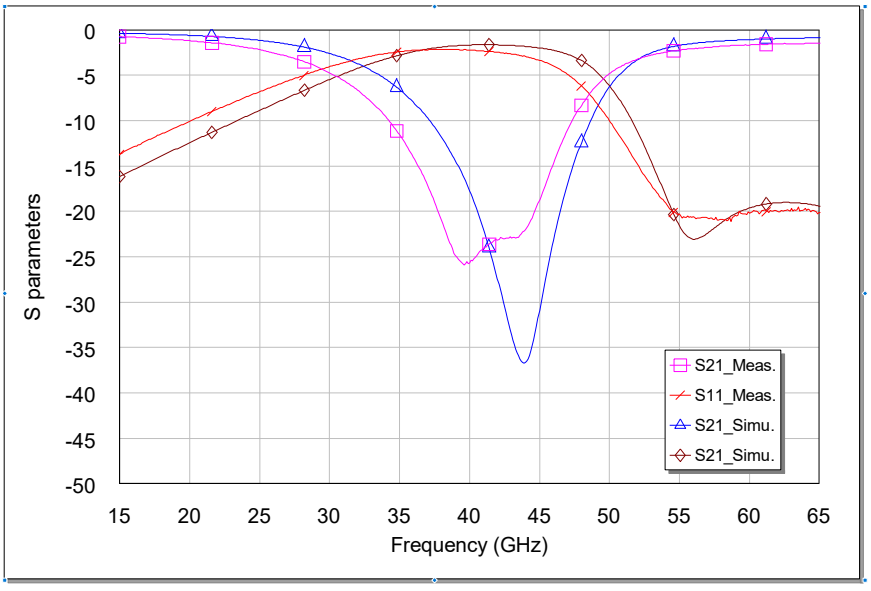
Figure 4.13**.** Manufactured on-chip CMOS mm-wave wide-band BPF prototype (Design 1). (a) Die microphotograph. (b) Simulated and measured power transmission ($|S_{21}|$) and input-reflection ($|S_{11}|$) responses.

The main measured characteristics of this on-chip CMOS mm-wave wide-band BPF prototype are as follows: center frequency of 34.5 GHz, 3-dB absolute bandwidth equal

to 21.1 GHz (i.e., equal to 61.2% in relative terms), minimum in-band power-insertion-loss level of 1.6 dB, and in-band input-power-matching levels higher than 18.3 dB. If needed for the intended application, lower in-band insertion-loss levels could be obtained by using a less-lossy substrate in the filter chip realization, such as SOI CMOS technology.

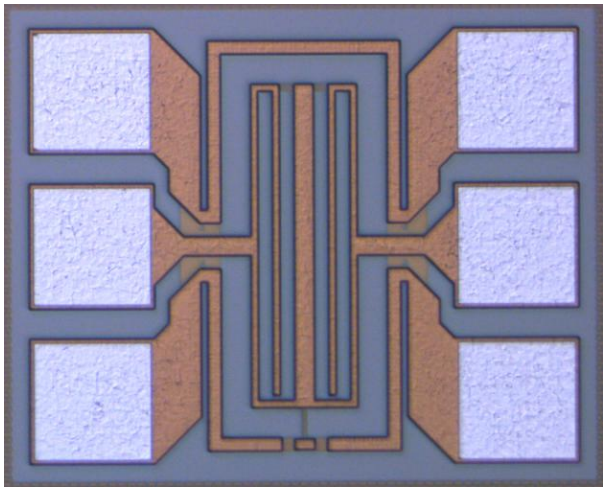


(a)

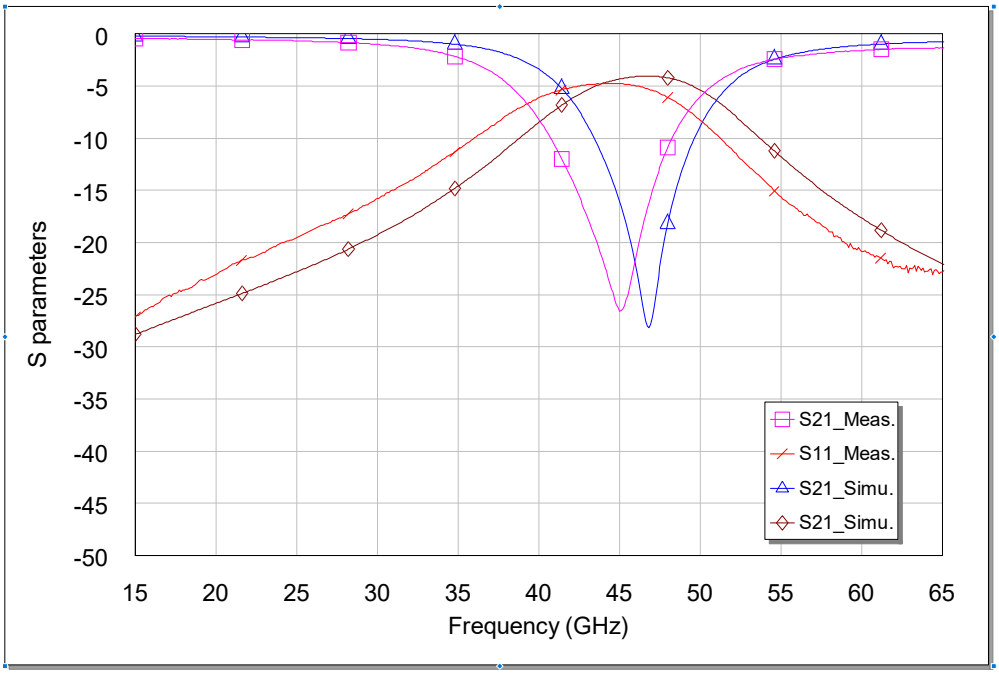


(b)

Figure 4.14**.** Manufactured on-chip CMOS mm-wave resonator prototype, Design 2. (a) Die microphotograph. (b) Simulated and measured power transmission ($|S_{21}|$) and input-reflection ($|S_{11}|$) responses.



(a)



(b)

Figure 4.15. Manufactured on-chip CMOS mm-wave resonator prototype, Design 3. (a) Die microphotograph. (b) Simulated and measured power transmission ($|S_{21}|$) and input-reflection ($|S_{11}|$) responses.

As mentioned earlier, in order to demonstrate that the feasibility of the proposed broadside-coupled approaches is sound, two additional resonators are designed and fabricated. The die microphotographs and the comparisons between EM simulated and measured results are given in Figures 4.13 and 4.14, respectively. As can be seen, both designs are also compact due to using the broadside-coupled structures. Added to this,

good agreements between the EM simulation and measurement results also obtained. It therefore once again proves that the presented approach is feasible for resonator design. Using such resonators along with additional matching capacitors as demonstrated in Design 1, multiple BPFs could be designed and implemented.

4.3.2 Comparison with the State-of-the-Art Designs

A comparison of the developed passive-integrated mm-wave wide-band BPF with the other state-of-the-art designs in this area is provided in Table 4.1. As demonstrated, the filter in this work features lower in-band power-insertion-loss levels, smaller die size, and higher in-band power-matching levels when compared to the wide-band BPFs in [126]-[128]. Furthermore, when compared to the one in [56] with narrower bandwidth, is shows benefits in terms of broader-band operation and higher number of out-of-band TZs.

	Center freq. (GHz)	TZs	3-dB BW (%)	Inser. loss (dB)	Return loss (dB)	Harmonic sup. (dB)	Die size (mm^2)	Tech.
[56]	40	1	20	1.7	19	20	0.012	130-nm SiGe
[122]	40	2	16.5	1.4	14	n/a	5.2	Glass
[126]	35	2	50	3.1	12	35	0.075	130-nm SiGe
[127]	18	3	66.7	2.9	24	22	0.125	130-nm SiGe
[128]	26.5	3	50.9	3.8	15.8	36	0.176	130-nm SiGe
This work	34.5	3	61.2	1.6	18.3	20	0.033	130-nm CMOS

Table 4.1 Performance comparisons with state-of-the-art on-chip BPFs

4.4 Conclusions

The design of a mm-wave silicon-passive-integrated wide-band BPF based on a two-layered implementation has been reported. It consists of a compact-size composite highpass/ upper-bandstop approach, which makes it well suited for broad-band applications, where out-of-band TZs at generated at both passband sides to obtain sharp-rejection filtering capabilities. The experimental viability of this broad-band BPF concept has been demonstrated with the manufacturing in CMOS technology and characterization of a 34.5-GHz on-chip circuit with relative bandwidth of 61.2%.

Chapter 5: RF CMOS Broad-Band Bandpass Filters with 3-D Inductors

Abstract—Different types of RF passive-integrated wide-band bandpass filters (BPFs) and bandstop filters (BSFs) in CMOS technology that operate at the sub-millimeter-wave region are presented. Firstly, the use of integrated 3-D inductors that exploit their parasitic capacitance to functionalize as *LC* tanks is shown. They enable highly-miniaturized on-chip wide-band BPF design as a result of the 3-D structure, along with transmission-zero (TZ) creation in the BPF response. Afterwards, a class of on-chip BSFs based on broadside-coupled meandered-line resonating cells is reported. Simulated and measured results of various built proof-of-concept RF-CMOS chips of the addressed BPF and BSF concepts are provided. These families of passive-integrated RF filtering components may find application in future wireless-communication radio systems as 5G.

5.1 Introduction

The ever-growing congestion of the radio spectrum as a very scarce resource, along with the need for transmitting very-large data volumes to support the wireless-communication services of tomorrow (e.g., 5G-and-Beyond, Internet-of-Things, and Big-Data networks), is leading to the exploitation of very-high frequency ranges where large portions of usable bandwidth can still be found. However, this imposes remarkable technological challenges regarding the development of advanced RF hardware to enable these modern radio systems to function smoothly. Without any doubt, millimeter-wave bandpass filters (BPFs) and bandstop filters (BSFs) are key exponents in this trend, as they are needed to acquire such ultra-wideband radio signals and mitigate out-of-band interferences coming from external RF sources. On-chip passive-integrated solutions are especially desired for such components to minimize DC-power consumption and physical size, thus rendering them compatible

with system-on-chip (SoC) low-power/energy-efficient RF front-end implementations.

In the aforementioned scenario, it is noticed that most currently available millimeter-wave filters mainly translate well-known microwave-passive-filter design techniques and technologies to frequency-scaled versions in more-compact physical realizations. Under this framework, various examples of very-high-frequency filtering devices can be found in the specialized technical literature. However, they could not be integrated with SoC devices. To further reduce fabrication cost and minimize the filter's size, the development of fully-integrated filters, also known as on-chip filters, has become an emerging research area in the last decade. In particular, recent developments in silicon-based technology make possible the implementation of low-cost chips suitable for a broad consumer market. Taking advantage of Moore's law, there are usually multiple metal layers that can be used in modern silicon-based technologies. Indeed, there is at least one thick metal layer that can be exploited for low-loss microwave-circuit development.

Hence, highly-miniaturized millimeter-wave on-chip passive filters able to perform competitively can be realized, such as those that rely on different design principles, for instance highpass-filter stages with an inserted upper stopband, broadside-coupled meandered-line resonant cells, and stub-loaded stepped-impedance resonators for wide-band BPF designs. Nevertheless, whereas some of these BPFs exhibit fractional bandwidths below 50%, insertion-loss performance, upper-stopband bandwidth (i.e., spurious-free behavior), and overall physical size (to be further miniaturized) must still be addressed in some others. Regarding on-chip BSFs, it must be stated that less effort has been detected despite their unquestionable relevance to ensure the operational robustness of the RF system in highly-congested radio environments with various out-of-system interference/ jamming sources. Other aspects beyond the scope of this work, such as the incorporation of high-Q electronic tuning and power-handling issues in such tiny RF electronic devices, are crucial aspects that must be further explored in the near future.

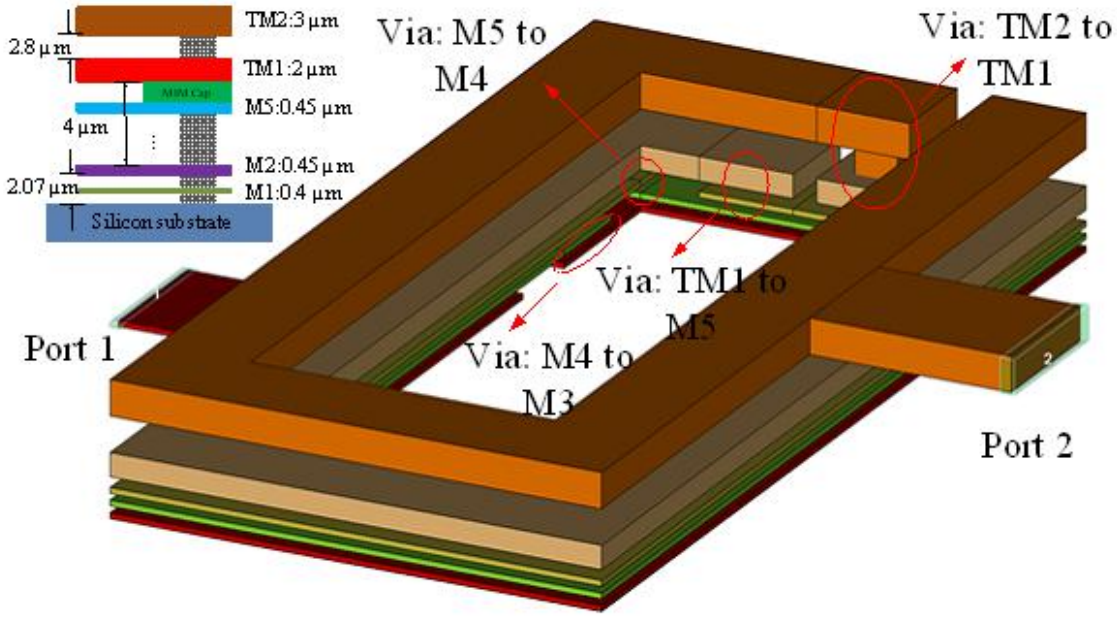
In this study, several classes of sub-millimeter-wave broad-band BPFs and BSFs in

low-cost bulk CMOS technology are presented. Comparing with the work presented in [135], the reported solutions are mostly aimed at further reducing the physical footprint of the on-chip filter by means of different design strategies for use in cost-effective highly-integrated RF systems. Among these RF techniques, the employment of alternative 3-D inductor implementations, in which their parasitic capacitance is properly exploited to use them as *LC* tanks in more-compact BPF schemes that can foreshadow some capacitors, or broadside-coupled meandered-line cells for BSF realization. The basic operational foundations of these RF filtering devices are expounded on. Besides, the simulated and measured results of various proof-of-concept on-chip circuits developed on silicon-integrated CMOS process are provided.

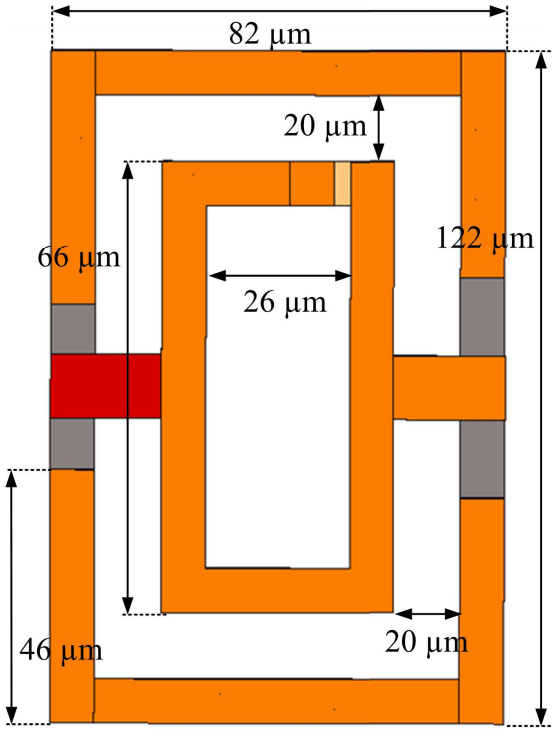
5.2 Wideband Bandpass Filters with 3-D Inductors

5.2.1 Four-3-D-Inductor BPF Cells designing

Whereas it is well known that both inductive and capacitive components are mostly needed in RF BPF design, the saving of some of these elements can lead to reduced-size developments. To achieve this goal, a class of integrated 3-D inductor that makes use of its parasitic capacitance to functionalize as *LC* tank (i.e., without additional capacitors) is proposed here. Its 3-D view for 0.13-μm bulk CMOS is shown in Figure 5.1. Specifically, only the top five metal layers (from TM2 to M3) are exploited to realize the 3-D inductor, as the bottom two metal layers are reserved solely for DC connections only. It is noted that the substrate details have been modified properly with the thickness of 200 μm, the dielectric constant of 4.1 and the loss tangent of 0.01.



(a)



(b)

Figure 5.1. Designed 3-D inductor cell, (a) Geometrical view of the 3-D inductor, (b) top view of the cell with dimensions.

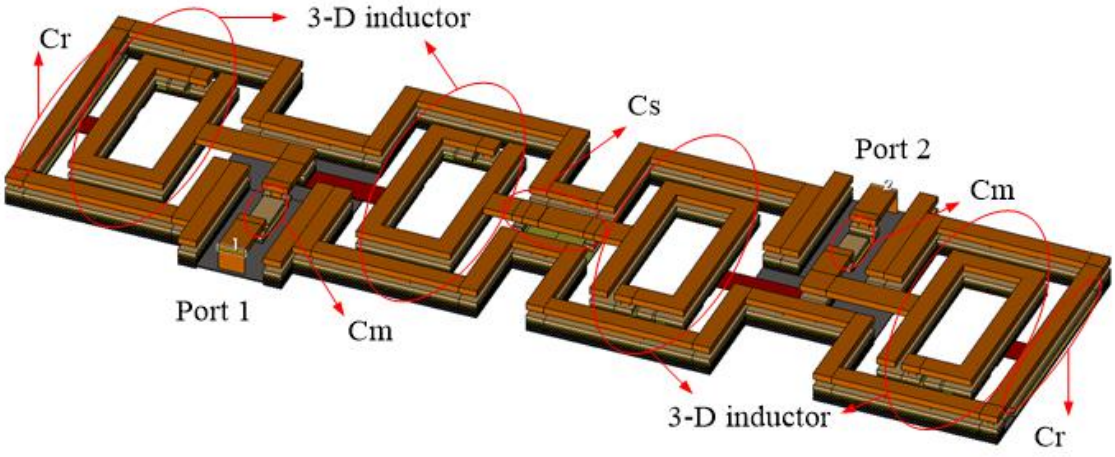


Figure 5.2**.** Series-cascading inductors in Figure 5.1 with MIM capacitors. Note: the four spiral-shaped 3-D inductor cells have identical physical sizes.

5.2.2 Equivalent Lumped-Element Circuit

To experimentally validate the usefulness of the engineered integrated 3-D inductor as *LC* tank by exploiting its parasitic capacitance in RF BPF design (i.e., capacitor-less resonant tank), two different on-chip prototypes have been designed in CMOS technology, built, and measured. They consist of two-3-D-inductor and four-3-D-inductor BPF circuits, as follows:

- The first prototype (Filter I) is based on the direct connection of two 3-D-inductor-based *LC* tanks. Metal-isolator-metal (MIM) capacitors C_m are used at the input/output ports for in-band power-matching and DC-isolation purposes, and MIM capacitors C_s are utilized for the inter-stage connection. A transmission zero (TZ) is created at the *LC*-tank resonant frequency (i.e., $f_z = 1/(2\pi\sqrt{LC_p})$) for sharp rejection at the upper passband side. Its equivalent lumped-element circuit and microphotograph are depicted in Figure. 5.3
- The second prototype (Filter II) incorporates the previously designed two additional 3-D-inductor-based *LC* tanks in parallel branches ending in MIM capacitors C_r just after the input/output capacitors C_m. This makes it possible to increase the filter order and produce an additional TZ at the lower passband side

through this parallel branch (i.e., $f_{z1} = 1/(2\pi\sqrt{LC_p})$ and $f_{z2} = 1/(2\pi\sqrt{L(C_q + C_r)})$). As a result this filter has a quasi-elliptic-type response as shown below. Figure 5.3 shows its equivalent lumped-element circuit model and micro photograph.

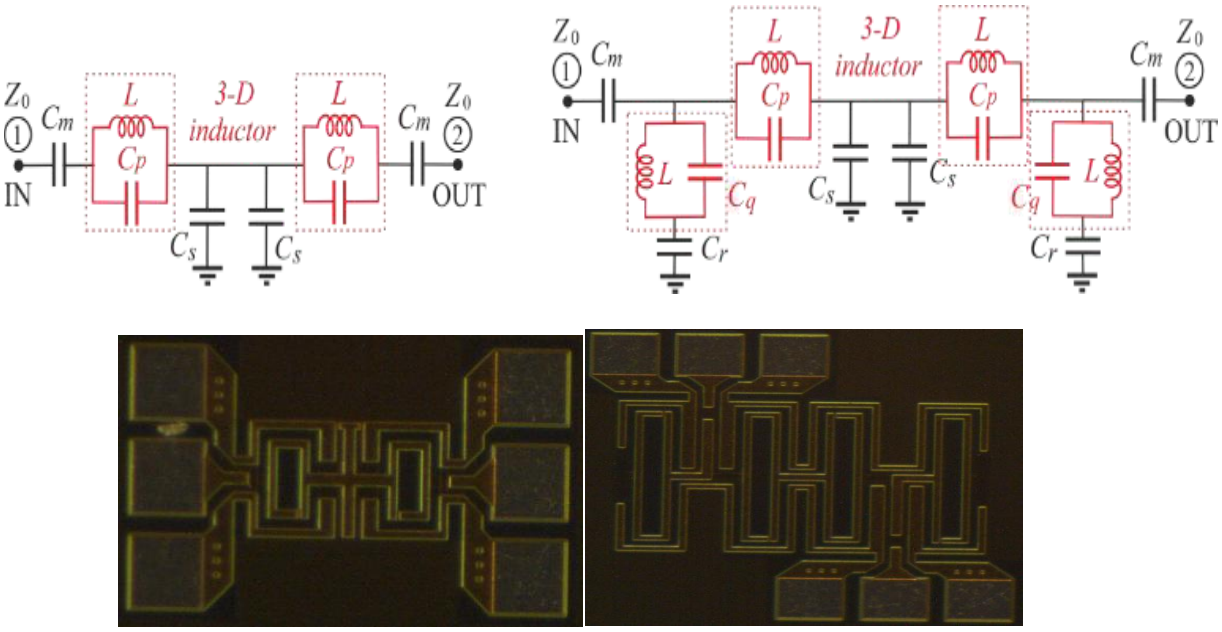


Figure 5.3**.** Lumped-element model and microphotograph of the developed BPF chips with 3-D inductors (red color: 3-D inductors with parasitic capacitances C_p and C_q). and Filter I./ Filter II.

The electromagnetically-simulated and measured power transmission and reflection responses of these on-chip BPF prototypes are compared in Figure 5.4, and their agreement is fairly close. Sharper-rejection capabilities are obtained for Filter II with regard to Filter I, due to its higher order and closer-to-passband creation of TZs at both passband sides. The main measured performance metrics of Filters I and II, respectively, are as follows: center frequencies of 9.97 GHz and 10.3 GHz, 3-dB bandwidths of 6.03 GHz and 6.02 GHz (i.e., 60.5% and 58.5%), minimum in-band insertion-loss levels of 3.7 dB and 4.2 dB, maximum in-band power-matching levels of 17.95 dB and 22.8 dB,

and 29.4-dB upper stopband ranges of 20-54.5 GHz and 17.8-52 GHz. Note that Filter II was realized with three metal layers (when compared to Filter I and its initial counterpart in [12] with five metal layers) for a less complex design.

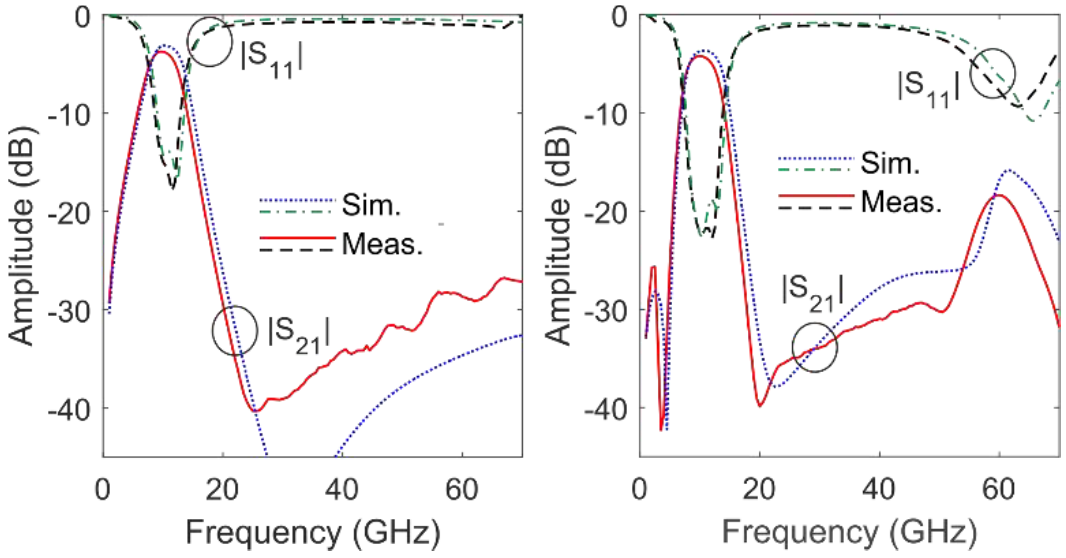
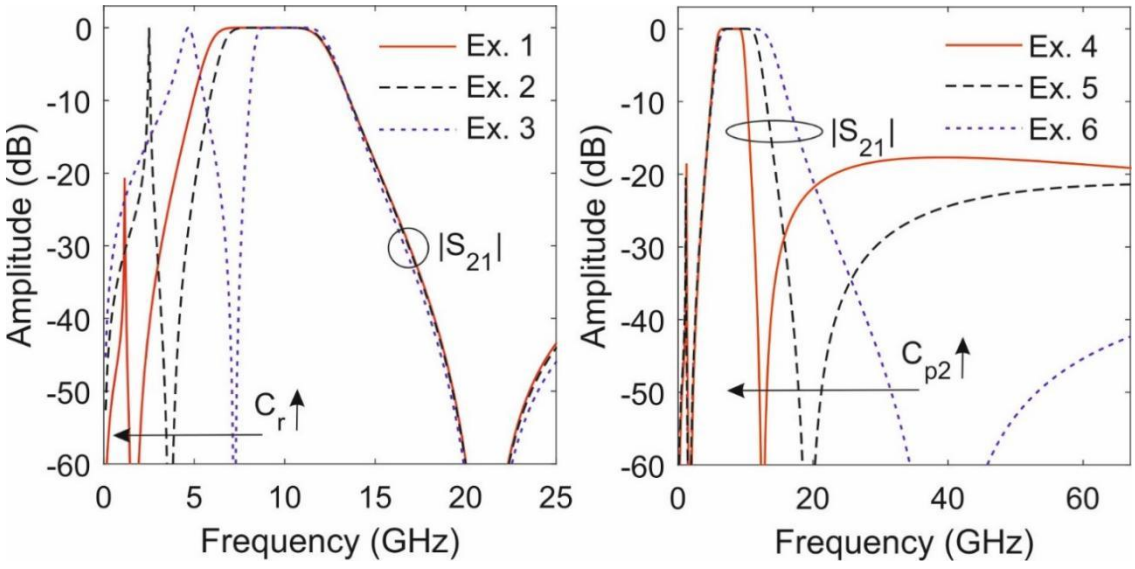


Figure 5.4. Simulated and measured power transmission ($|S_{21}|$) and reflection ($|S_{11}|$) responses of the developed RF CMOS wide-band BPF chips with 3-D inductors for Filter I. and Filter II



(a) (b)

Figure 5.5. TZ control in ($|S_{21}|$) of the lumped-element circuit in Figure 5.3. (a) Lower-TZ control (b) Upper-TZ control

In Figure 5.5 several exercises with different values of C_r and C_{p2} are compared. It

is concluded that the lower and upper transmission zeros could be shifted with the change of C_r and C_{p2}. Figure 5.5 (a) reveals that the lower TZs can be controlled so that a bigger passband with a bigger C_r can be obtained. In Figure 5.5 (b), the upper TZ is shifting to the lower frequency range leading to a smaller passband as the value of C_{p2} is increased. It is a trade-off between the passband and the sharp cut-off curve for both the lower and upper stopbands.

Although, in [134], [135], sharp-rejection filtering features could be found as the cascading structure, great attenuation will be in the fabricated device as the substrate loss.

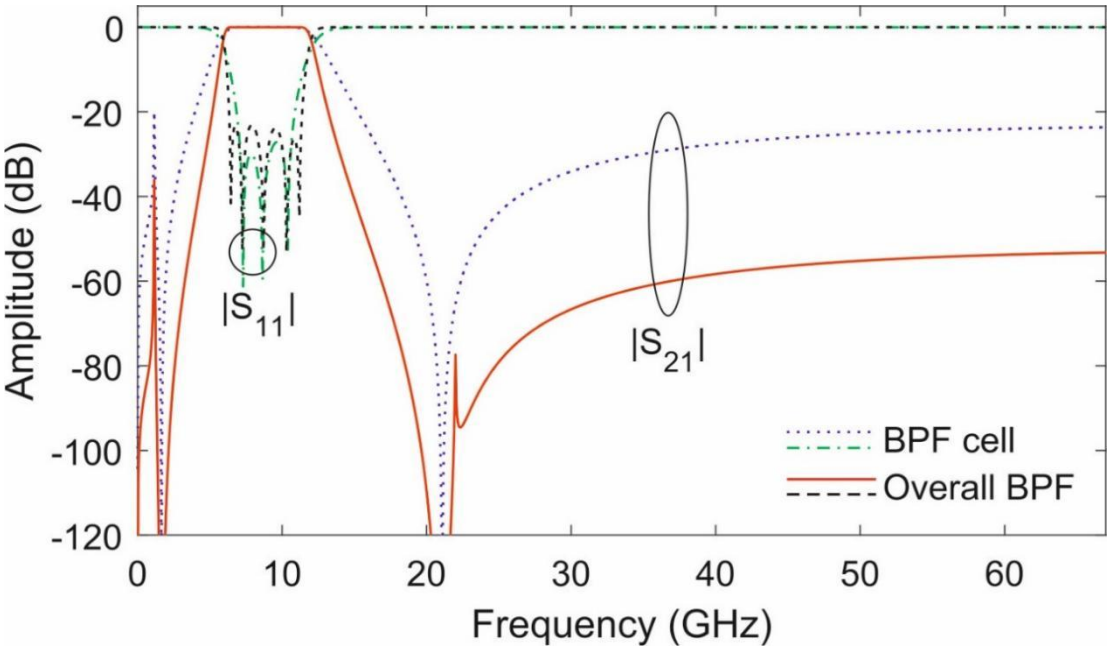


Figure 5.6. Examples of ($|S_{21}|$) and ($|S_{11}|$) of the two-stage BPF

5.2.3 Extension of the Designed BPF presented in Section 5.2.2.

To demonstrate that the presented concept of using 3-D inductors for BPFs design is a generic approach, another two examples are offered. To differentiate these two designs with the one presented in the last sub-section, these two designs are called Design 2 and Design 3. Unlike Design 1, only two 3-D inductors are used for Design 2, so that it is potentially suitable for miniaturized designs. The 3-D view of the

implemented BPF is given in Figure 5.7. As illustrated, it is very similar with the one designed in the last sub-section. The 3-D inductor is implemented with five metal layers, from TM2 to M3. Additionally, only two in-series-connected 3-D inductors are used in this design. As previously analyzed, this configuration could provide a superior out-of-band performance with a sharp selectivity. As the shunt-connect branch is no longer applied in this design. It is expected that there will be no TZ at the lower frequency band. The comparisons between the EM simulated results and the measured results will be given in the next section.

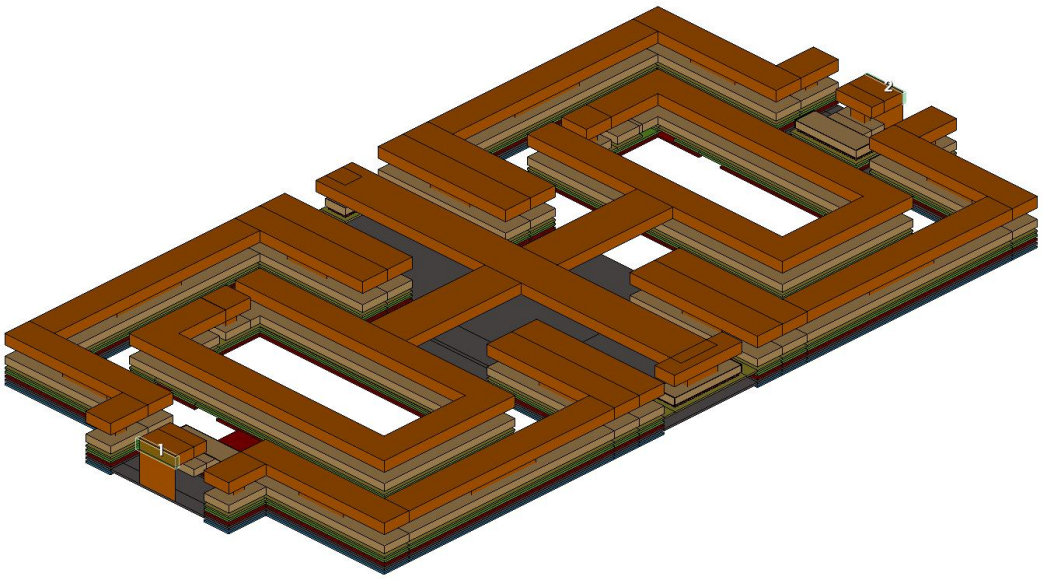


Figure 5.7. 3-D view of Design 2

Furthermore, the 3-D view of Design 3 is given in Figure 5.8. As can be seen, it uses an exactly same circuit configuration with Design 1. Thus, four 3-D inductors are used. Unlike the previous two designs that five metal layers are used, only three metal layers are used in this design, which is from TM2 to M5. The motivation behind this design is that the insertion loss could be reduced to some extent, if using of the thin metal layers, such as M4 and M3, could be avoided. However, as the number of metal layers used in the 3-D inductor is reduced, the physical dimensions of the inductor are increased. Thus, there is a design trade-off between insertion loss and die area. The EM simulated and measurement results will be shown in the next section.

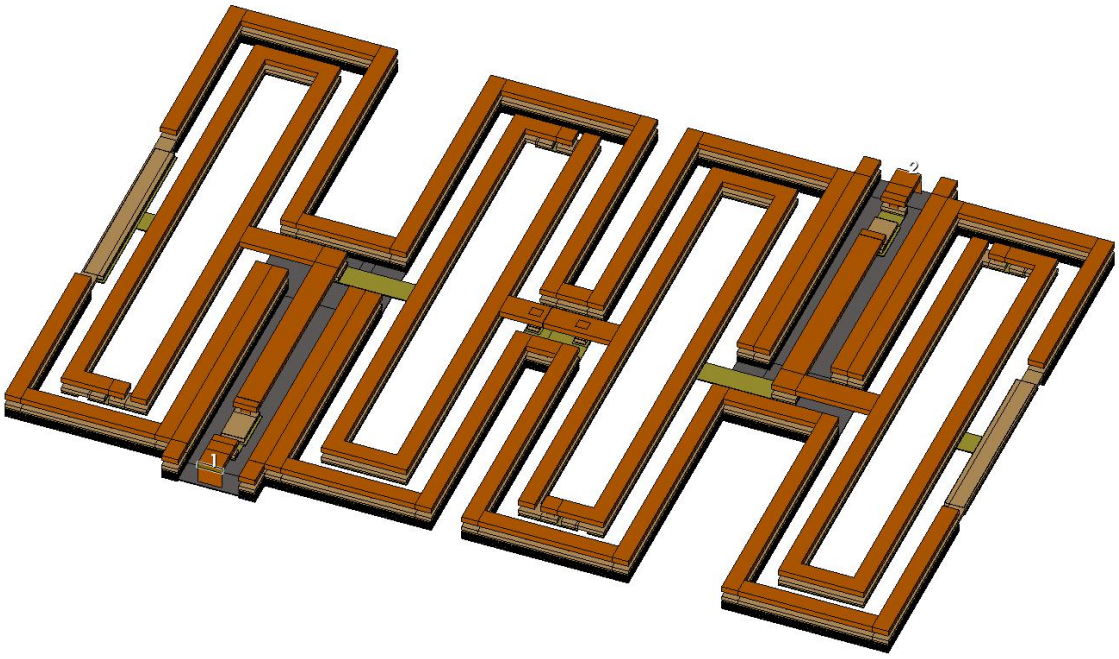
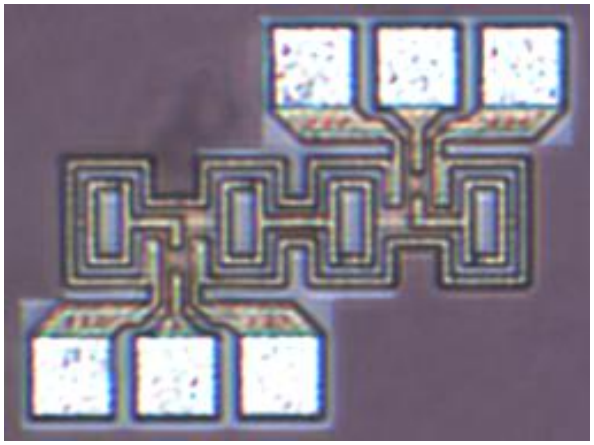


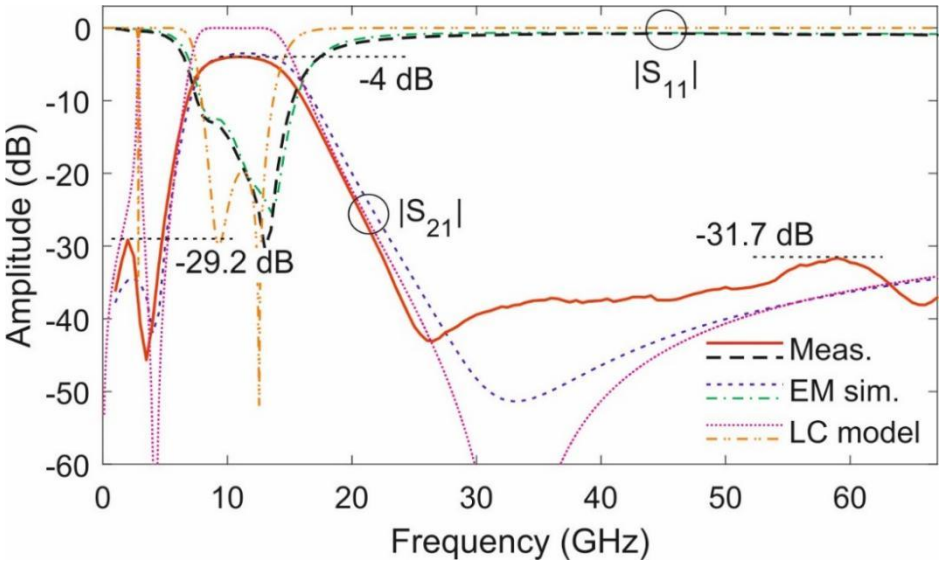
Figure 5.8. 3-D view of Design 3.

5.3 Experimental Results

Figure 5.9 (a) is the die microphotograph of the fabricated BPF circuit. The device size of 0.122 mm × 0.442 mm is very large excluding the pads for pins. In Figure 5.9 (b), revealed here is a close agreement between simulated and experimental results.



(a)



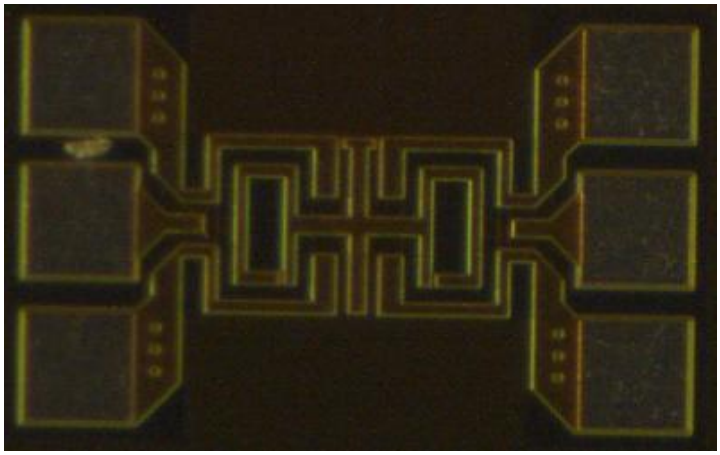
(b)

Figure 5.9**.** Design 1. (a) Fabricated device (b) ($|S_{21}|$) and ($|S_{11}|$) comparison between designed and experimental results

To further demonstrate that the presented design methodology is feasible for other type of BPFs design. The so-called Design 2 and Design 3 are also fabricated and their performance is evaluated through on-wafer measurement as well. The die microphotograph of Design 2 is given in Figure 5.10 (a). As previously shown in Figure 5.7, only two 3-D inductors are used for this design. Thus, the physical dimensions of this design is smaller than Design 1. The comparisons are presented in Figure 5.10 (b).

For Design 3, the die microphotograph and its measurement results are presented in Figure. 5.11 (a) and (b), respectively. As illustrated, a good agreement between the results is obtained. Comparing with Design 1, as the 3-D inductor only involves three metal layers, the physical dimensions of this design are larger than Design 1. However, the insertion loss is reduced by 0.5 dB. It is because that the thin metal layers are not used in the implementation. Therefore, it is clearly that there is a design trade-off between footprint and insertion loss. Using more metal layers to form the 3-D inductor is useful for miniaturised design with a penalty of increased insertion loss. In contrast, if a realtively low insertion loss is required, then the 3-D inductor should be only implemented using the thick metal layers, which indeed enlarges the physical

dimensions of the filter to some extent.



(a)

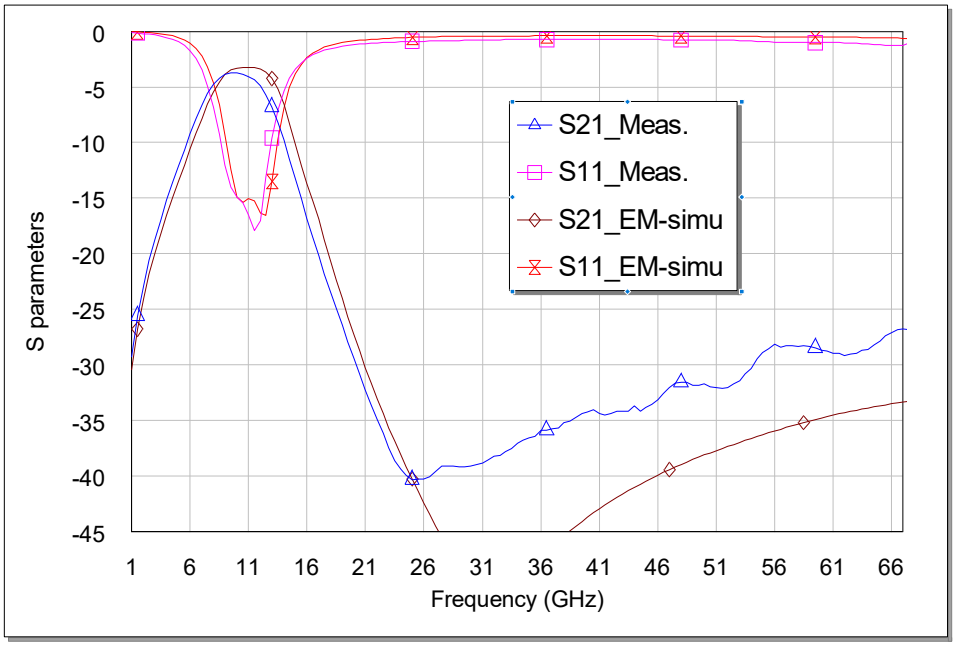
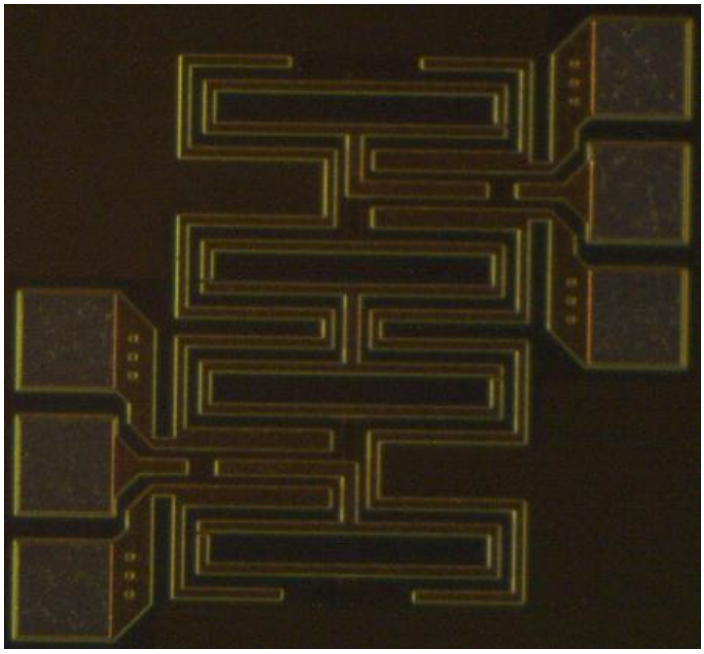
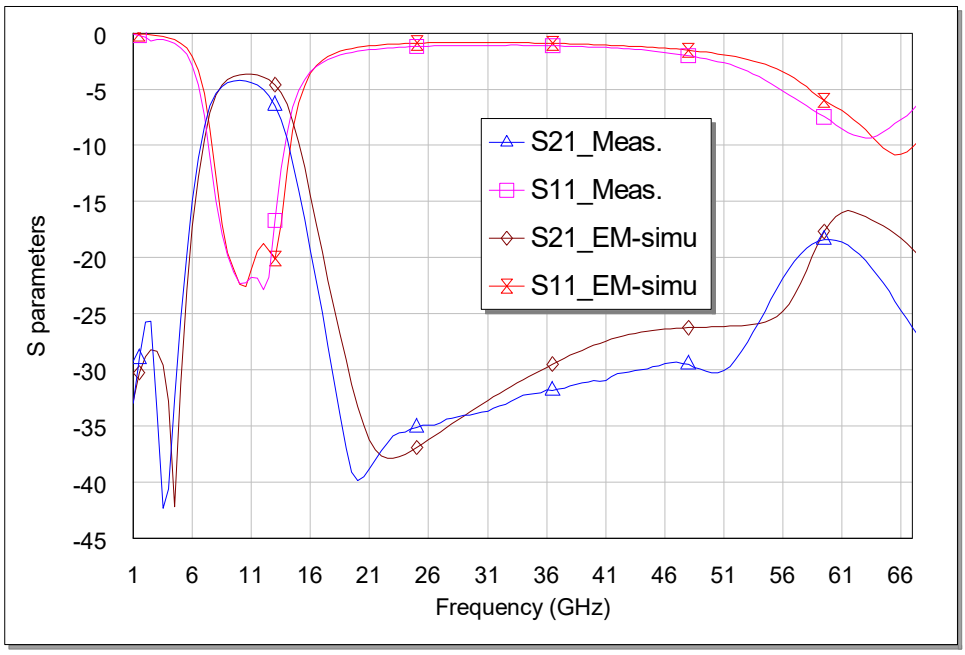


Figure 5.10**.** Design 2. (a) Die microphotograph (b) EM-simulated, and measured power transmission ($|S_{21}|$) and reflection ($|S_{11}|$) responses.



(a)



(b)

Figure 5.11**.** Design 3. (a) Die microphotograph (b) EM-simulated, and measured power transmission ($|S_{21}|$) and reflection ($|S_{11}|$) responses.

	Center Freq. (GHz)	TZs	3-dB BW (%)	Inser Loss (dB)	Return Loss (dB)	Harm. Sup. (dB)	Die Size (mm^2)	Tech.
[104]	34.5	3	61.2	1.6	18.3	20	0.033	130-nm CMOS
[58]	40	1	20	1.7	19	20	0.012	130-nm CMOS
[126]	35	2	50	3.1	12	35	0.075	130-nm CMOS
[127]	18	3	66.7	2.9	24	22	0.125	130-nm CMOS
[128]	26.5	3	50.9	3.8	15.8	36	0.176	130-nm CMOS
This work	11	2	68.5	4	30.3	32	0.054	130-nm CMOS

Table 5.1 COMPARISONS WITH STATE-OF-THE-ART BPFs

5.4 Conclusions

A broadband BPF is designed and tested with the results of a quasi-elliptic-type response after fabrication. It is based on 3-D inductors that exploit the parasitic capacitances to operate as MIM-capacitor-less *LC* tanks and broadside-coupled meandered-line resonating cells, respectively, for cost-effective highly-compact realizations. Experimental results of various on-chip prototypes confirm the practical validation, proving that they have potential for RF-front-ends in SoC modules aimed at 5G radio systems.

Chapter 6: Conclusions and Future Works

Abstract— This thesis has presented the research studies that have been done on designing miniaturized on-chip passive device for mm-wave applications using 0.13-μm (Bi)CMOS technology. Specifically, the design and implementation of resonator, reflectionless BSF and wideband BPFs are presented. The different design structures have also been comprehensively reviewed. Based on the measurement results obtained for the three different designs presented in this thesis, it could be firmly concluded that design of high-performance on-chip filters in standard CMOS technology is feasible. In this chapter, the innovations of this thesis will be summarized again in Section 6.1 and then some recommendations for future research will be presented in Section 6.2.

6.1 Conclusions

This thesis developed three novel design approaches for miniaturized on-chip passive components designs in silicon-based technology. The summaries of these designs in terms of their novelties are given below.

- The first design is concerned with a reflection-less BSF without using any lump-element resistors. From the fabrication cost of view, implementation of on-chip resistors requires multiple mask layers, which could significantly increase fabrication costs. Using the approach described in this thesis, a novel BSF is designed that generates a notch at the center frequency of 24.5 GHz with an attenuation over 26 dB and more than 98% of RF energy could be absorbed. The physical size of the designed BSF without the testing pad is only 0.034 mm^2.

- The second design is concerned with a wideband BPF using broadside-coupled structures. Using the broadside-coupled structure along with lump-element capacitors, the physical dimensions of the designed BPFs could be significantly

reduced. A novel BPF is designed that has a center frequency at 34.5 GHz with a relative bandwidth of 61.2%. It is noted that three TZs could be generated using the presented structure and all of them could be adjusted independently. Due to using the broadside-coupled structure, the physical dimensions of the designed filter amount to only 0.033 mm^2, excluding the measurement pads.

- The third design is also concerned with the miniaturized BPF. Unlike the approaches presented for the second design, using 3-D inductors for wideband BPFs designs is investigated in this thesis. To demonstrate that the approach is feasible for wideband BPFs, two wideband BPFs are devised and both show a wideband frequency response with superior out-of-band performance with significantly minimized physical sizes. The performance of the out-of-band suppression is also superior, and is in fact better than 20 dB up to 67 GHz. As the bulky inductors are implemented in a 3-D form, the physical dimensions of the designed filter are only 0.054 mm^2, excluding the measurement pads.

As presented in this thesis, the design trade-offs are mainly focused on physical diemsions, insertion loss, bandwidth, selectivity and operating frequencys etc. Depending on different design specifications, design choice could be made accordingly. It is noted that while the operating frequency is pushed to higher and higher, the physical dimensions of the filter will be inherently reduced. As a result, the insertion loss may be effectively reduced as well. Moreover, as deomstrated in Chapter 5, the insertion loss of the filter could be minimized, if a relatively wide bandwidth is used. Finally, the selection of the selectively of the filter is also ciritical. To achieve a relatively sharp selectivity, a high-order filter is required. Usually, more than two stages are cascaded to obtain a high-order selectively. Consequently, the insertion loss could be deteriorated.

6.2 Future Works

This thesis presented a design methodology of a miniaturized passive integrated circuit ideal for system-on-chip solutions. There are many opportunities to extend the presented concept to develop high-performance compact devices for a future wireless communication system. The potential topics for future research directions are briefly given below,

- Designing and implementation a new circuit structure of other passive devices, like impedance matching circuits, couplers, and baluns using the proposed design methodology for mm-wave applications.

- Also, it is worthwhile investigating the performance of the circuits having both active and passive components in a single chip for system-on-chip solutions. Co-designing the presented mm-wave passive circuits with active circuits on a single chip may provide a cost-effective solution for the single-chip receiver, transmitter, transceivers, and mm-wave sensors.

- As discussed in this thesis, our design focuses on utilizing the mm-wave spectrum to develop mm-wave enabled passive integrated circuits. The presented designs are limited to between 20 to 80 GHz. However, there is also a growing potential for sub-terahertz and terahertz applications. Thus designing a new building block and functional modules operating in the terahertz frequency band may provide new services.

The evolution of integrated circuits requires a significant amount of research in order to address the various issues and design requirements of emerging technologies. Future research will allow this novel design methodology to be used in many practical applications and eventually this will lead to more advanced and compact devices in the future.

ABBREVIATIONS

ACMA	Australian Communication and Media Authority
AWGN	Additive White Gaussian Noise
1G	First Generation
2D	Two-Dimensional
3D	Three Dimensional
4G	Fourth Generation
5G	5-Generation / Fifth Generation
ABCD	ABCD Conversion
AWR	Applied Wave Research
BCMLR	Broadside Coupled Meander-line Resonator
BEOL	Back-End of the Line BPF Bandpass Filter
CAD	Computer Aided Design
CISCO	Computer Information System Company
CMOS	Complementary Metal Oxide Substrate
CPW	Coplanar Waveguide
CST	Computer Simulation Technology
dB	decibel
DBC	Direct Bond Copper
DC	Direct Current
DGS	Defected Ground Structure

DRAM	Dynamic Random Access Memory
DRC	Design Rule Check
EB	Exabyte
ECC	Edge-Couple Cell
EM	Electromagnetic
ERC	Edge-Coupled Resonator
FBW	Fractional Bandwidth
FCC	Federal Communication Commission
FEOL	Front-end-of-line
FL	Finline
FLDR	Folded Loop Dual-Mode Resonator
GaAs	Gallium Arsenide
GaN	Gallium Nitrite
GHz	Giga Hertz
G-S-G	Ground-Source-Ground
I/O	Input-Output
IBM	International Business Machines
IC	Integrated Circuits
IDC	Interdigital Capacitor
IHP	Innovation for High Performance
IPD	Integrated Passive Devices
LC	Lumped Component

LE	Lumped-Element
LTCC	Low-Temperature Co-Fired Ceramic
LTE	Long Term Evolution
M1	Metal layer 1
M2	Metal Layer 2
M3	Metal Layer 3
M4	Metal Layer 4
M5	Metal Layer 5
M6	Metal Layer 6
MEMS	Micro-Electro-Mechanical System
MIM	Metal-Insulator-Metal
ML	Microstrip Line
MMIC	Millimeter-wave Integrated Circuit
MSTL	Microstrip Transmission Line
NI	National Instrument
PCB	Printed Circuit Board
PIP	Poly-Insulator-Poly
PIS	Poly Insulator Single
QAM	Quadrature Amplitude Modulation
Q-Factor	Quality Factor RF Radio Frequency
RFIC	Radio Frequency Integrated Circuit
SG-CPW	Stacked Grounded Coplanar Waveguide

SiGe	Silicon Germanium
SiO2	Silicon Dioxide
SIP	System-In-Package
SIR-MH	Stepped Impedance Resonator Meandering Hairpin
SL	Stripline
SLL	Slotline
SLOT	Short-Load-Open-Thru
SOC	System-on-Chip
SRF	Self-Resonating Frequency
SSL	Suspended Stripline
TEM	Transverse-Electromagnetic
TM1	Top Metal Layer 1
TM2	Top Metal Layer 2
TZ	Transmission Zero
UHF	Ultra High Frequency
VCO	Voltage Controlled Oscillator
VHF	Very High Frequency
VNA	Vector Network Analyzer
VNI	Networking Index
WiMAX	Worldwide Interoperability for Microwave Access

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