320 GHz On-Chip Circularly-Polarized Antenna Array Realized with 0.13 μm Bi-CMOS Technology

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***Abstract*— A 320 GHz on-chip circularly-polarized (CP) antenna array that has been facilitated with 0.13 µm SiGe Bi-CMOS technology is presented. It is the first designed and prototyped THz-band on-chip antenna array with circular polarization and high directivity. The antenna is realized by designing a 4 × 4 microstrip-fed CP patch antenna array inside the silicon dioxide layer on top of a silicon base. A sequential phase rotation scheme is applied to the four 2 × 2 subarrays to achieve wide axial ratio (AR) bandwidth (8.7 GHz). The antenna array was successfully prototyped in a 3.6 × 3.6 mm^2 area on a silicon wafer. Consequently, it easily combined with other integrated circuit (IC) components. The developed THz on-chip CP antenna is highly desired for the emerging ultra-high speed wireless applications.**

***Index Terms*—0.13 µm Bi-CMOS Technology, cicularly-polarized antenna array, integrated circuits, on-chip antennas, satellite communications, THz antennas**

I. Introduction

Terahertz (THz) antennas have drawn much attention during recent years since they can support ultra-high speed data transfer rates, e.g., up to 100 Gb/s, for future wireless applications [1]. THz wireless communication systems are highly promising for space applications due to the significantly reduced path loss when compared to similar THz systems in atmospheric environments. A typical application example is the inter-satellite communications in low earth orbit (LEO) satellite networks illustrated in Fig. 1. High directivity, circularly polarized (CP) antennas operating at THz are highly desired for such an application because CP systems mitigate the polarization mismatch issues associated with linearly-polarized (LP) device-to-device (D2D) communication systems [2]. Future wireless trends require extremely high density component integration and miniaturized electronic devices. Hence, on-chip antennas operating in THz bands with circular polarization and high directivity will be highly desired for any type of ultra-high speed D2D communications. Although quite a few THz LP on-chip antennas have been reported to date [3] – [6], CP antenna arrays have not yet been developed. This paper introduce the first designed and prototyped THz on-chip CP antenna array operating at 320 GHz band that was fabricated with 0.13 µm Bi-CMOS technology.

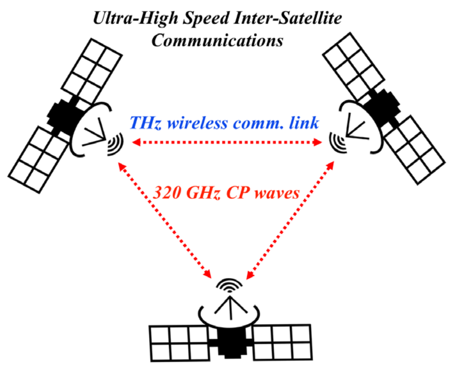


Fig. 1. An example of THz on-chip CP antenna array for ultra-high speed inter-satellite communications in space applications.

II. 320 GHz On-Chip CP Antenna Array Design

The designed CP antenna array is a 4 × 4 microstrip-fed patch antenna array. Each radiating patch element is a square microstrip patch antenna with a cut-corner to achieve the CP performance. A sequential phase rotation scheme is applied to the four 2×2 subarrays to improve its axial ratio (AR) bandwidth.

The 320 GHz on-chip CP antenna array configuration is shown in Fig. 2. The 0.13 µm SiGe Bi-CMOS technology fabrication rules required a multi-layered design. A thick silicon base was located on the bottom. A layer of silicon dioxide was placed on top of the silicon base. The two metallization layers, i.e., the radiating elements and the ground, were enclosed in the silicon dioxide. The array was excited with a coplanar waveguide probe (GSG) probe.

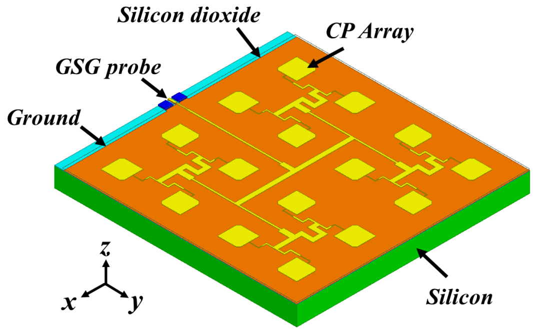
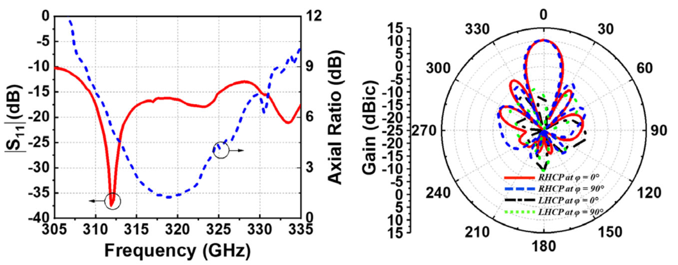


Fig. 2. 320 GHz on-chip CP antenna array configuration that was fabricated with 0.13 μm Bi-CMOS technology.

The simulated $|S_{11}|$ and AR values as functions of the source frequency are shown in Fig. 3(a). The operating bandwidth (the overlapped -10 dB $|S_{11}|$ and AR bandwidth) is 8.7 GHz from 314.5 to 323.2 GHz. The simulated CP radiation patterns at 320 GHz are shown in Fig. 3(b). The peak realized RHCP gain is 10.2 dBic and the sidelobe level is less than -12 dB.



(a) (b)

Fig. 3. (a) Simulated $|S_{11}|$ and Axial Ratio values as functions of the source frequency; and (b) Simulated radiation patterns at 320 GHz.

III. Fabricated Prototype and Measurement

The fabricated on-chip prototype image under microscope is shown in Fig. 4. The total size of the chip is 3.6 × 3.6 mm^2. It is highly compact and can be easily combined with other integrated circuit (IC) components.

The prototype was measured with the robotic anechoic chamber setup at Ulm University [7]. The preliminary measurement results are shown in Fig. 4. Note that we are not able to obtain the data for CP radiation in these initial results. Nevertheless, the measured LP radiation parameters are sufficient to predict the performance of the prototype. Fig. 5(a) presents the measured and simulated LP gain values as functions of the source frequency. It is clearly observed that the trend of the measurements agrees reasonably with simulations. The operating frequency shifted about 10 GHz (3%) towards the lower band. The measured (8.6 dBi) and simulated (8.7 dBi) peak LP gain values are very close. The measured radiation patterns from 300 to 310 GHz are shown in Fig. 5(b). It is seen that the sidelobe levels are less than −11 dB, which also agrees with the simulated value, −12 dB. The full measurement results will be reported in the conference presentation.

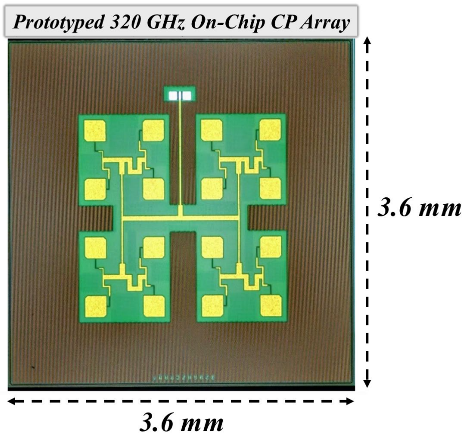
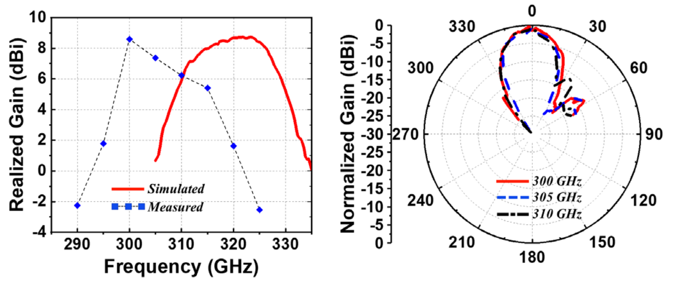


Fig. 4 Microscope image of the fabricated 320 GHz on-chip CP antenna array fabricated with 0.13 μm Bi-CMOS Technology.



(a) (b)

Fig. 5. Preliminary measurement results. (a) Measured and simulated realized LP gain as functions of the source frequency. (b) Measured LP radiation patterns at 300, 305, and 310 GHz.

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