UTS UNIVERSITY OF TECHNOLOGY SYDNEY

Design of millimeter-wave transmitter in silicon-based technologies

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ABSTRACT

Nowadays, with rapid advances being made in wireless communications, the demand for high-performance radio frequency (RF) transmitters has risen dramatically. An increasing number of challenges are evident for radio frequency integrated circuit (RFIC) designers while the operational frequency is being pushed to millimeter-wave (mmWave). The transmitter is an electronic device that can be used to send radio signals. A typical transmitter may contain many components, such as an RF power amplifier and a switch. The efficiency of the transmitter can significantly guide the performance of the whole wireless system. For this reason, it is necessary for RFIC researchers to propose more efficient designs. Therefore, in this thesis, the design methodologies of a high-performance mmWave power amplifier and two silicon-based single-pole double-throw (SPDT) switches are presented.

The first approach is used to design a symmetrical 90 GHz single-pole double-throw switch in CMOS Technology. To improve the power-handling capability of bulk CMOS-based single-pole double-throw (SPDT) switch, a novel design approach that combines both power dividing and impedance transformation techniques is used to improve 1-dB compression point (P1dB). The SPDT switch is implemented in a 55nm bulk CMOS technology and achieves a measured P1dB of 15 dBm and an insertion loss of 3.5 dB and an isolation of 17 dB. The die area is only 0.14 mm^2.

In the second work, to further improve the power-handling capability of the SPDT switch, a 90-GHz asymmetrical SPDT switch is designed. Taking advantage of utilizing a unique passive ring structure, the fundamental limitation for P1dB due to reduced threshold voltage is overcome. The design has achieved an IL of 3.2 dB and 3.6 dB in Transceiver (TX) and Receiver (RX) mode, respectively. Moreover, more than 20 dB isolation is obtained in both modes. The P1dB is 19.5dBm. The die area of this design is only 0.26 mm^2.

In the third work, a wideband millimeter-wave (mm-Wave) power amplifier (PA) is designed. To ensure the designed PA has sufficient output power and good power-added efficiency (PAE), a balanced amplifier (BA) architecture is used. A prototype PA is fabricated in a 0.13-μm SiGe HBT technology. Supplied by 5V power, the PA can provide more than 15 dBm saturated output power between 85-100 GHz that is equivalent to more than 16% fractional bandwidth. The peak PAE is better than 14% within this frequency range. Including all pads, the die area is only 0.6 mm × 0.9 mm.

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Journal Publications

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2. **L. Chen**, Z. Ge, L. Chen, Y. Sun and X. Zhu, "Design of Millimeter-Wave Asymmetrical Single-Pole Double-Throw Switch with Enhanced 1-dB Compression Point in 55-nm Bulk CMOS Technology" in **IEEE Transactions on Circuits and Systems I: Regular Papers** (*under review*)

Conference Publications

1. L. Chen, L. Chen, Z. Ge, F. Meng and X. Zhu, "A W-band Power Amplifier with 15-dBm Psat and 14% PAE in 0.13-μm SiGe HBT Technology," **2021 IEEE MTT-S International Wireless Symposium (IWS)**, 2021, pp. 1-3, doi: 10.1109/IWS52775.2021.9499688.
2. **L. Chen**, L. Chen, Z. Ge. R. Gómez-Garcia and X. Zhu, " Design of Passive-Inspired Millimetre-Wave Integrated Devices in Low-Cost Bulk CMOS Technology," 2021 Asia-Pacific Microwave Conference (APMC), 2021 (**accepted**)

Co-Authored Journal publications

1. Z. Ge, **L. Chen**, R. Gómez-García and X. Zhu, "Millimeter-Wave Wide-Band Bandpass Filter in CMOS Technology Using a Two-Layered Highpass-Type Approach with Embedded Upper Stopband," in **IEEE Transactions on Circuits and Systems II: Express Briefs**, doi: 10.1109/TCSII.2021.3064387.
2. Z. Ge, **L. Chen**, L. Yang, R. Gómez-García and X. Zhu, "On-Chip Millimeter-Wave Integrated Absorptive Bandstop Filter in (Bi)-CMOS Technology," in **IEEE Electron Device Letters**, vol. 42, no. 1, pp. 114-117, Jan. 2021, doi: 101109/LED.2020.3036036.

Chapter 1: Introduction

Designs of high-performance transmitter for millimeter-wave 5G communication are the4 focus of this thesis. In this chapter an overview of the thesis structure is described for the reader. The background of this thesis will be explained in Section 1.1, which includes an overview of 5th Generation Wireless System (5G), Millimeter-wave (mmWave), power amplifier and switch. Following this, the problems and challenges faced will be provided in the next section 1.2. The contributions of my research will be described in Section 1.3. Finally, the overall structure of the thesis will be provided in Section 1.4.

1.1 Background

1.1.1 5th Generation Mobile Network

Our research objective is to design circuits blocks for RF transmitters using the Fifth Generation Mobile Network (5G). This is a worldwide standard for the wireless network, and it was introduced in July 2016. Compared with previous mobile network standards, such as 3G or 4G, the advantages of 5G are obvious. One of the most important key benefits of 5G network is the high data rate. Taking advantage of high bandwidth, 5G can eventually achieve up to 10 Gbit/s download speed. The second key benefit is the much lower latency obtained. According to some literature [1], a latency of milliseconds can be achieved under perfect conditions.

To provide a reliable and high data throughput, new modulation technologies, such as 512-Quadrature Amplitude Modulation (QAM) or even 1024-QAM [2, 3], are evident in in 5G. Compared with the current Quadrature Amplitude Modulation methods used by 4G, such as 256-QAM or 64-QAM, better QAM technologies can support and provide high-performance and reliable service for end-users. Due to the requirement of a high data rate, high-performance antenna technology [4], has been widely used in 5G technology. By using multiple antennas at both transmitter and receiver ends of wireless devices, MIMO can significantly increase the data transmission efficiency.

An extremely low error rate is also a key feature of 5G technology. Using the Adaptive Signal Coding System [5], 5G can ensure a low error rate in delivering the signal. The high frequency used by 5G may be one of the most important reasons for high performance. Compared with 4G, the frequency used by 5G significantly rises to sub-6GHz, or even 24.25GHz-52.6GHz [6]. Having a higher frequency might generate more data throughout. Although the advantages of introducing 5G are obvious, significant challenges have also been brought for RFIC designers. It is important for us to introduce new design methodologies for FEM operating in higher frequency.

1.1.2 Millimeter-wave(mmWave)

There are multiple frequency bands being used in 5G. It is widely accepted that a higher frequency can usually carry a higher data rate. Consequently, the developments that occur in wireless communication always come with an increase in frequency [7]. It should be noted that low band 5G, such as 600MHz [8], can produce better coverage than the 4G system. However, to achieve all the goals, such as extreme high data speed, set by the 3rd Generation Partnership Project (3GPP), it is necessary to introduce millimeter wave technology into the 5G system [9].

According to the 3GPP Specification #: 38.101-1[10], the 5G NR frequency bands can be divided into two different frequency ranges. The first range of frequency is Frequency Range 1 (FR1), while the second range of frequency is FR2. The frequency defined by FR2 is also known as Extremely High Frequency (VHF) or millimeter waves (mmWave). Figure 1.1 depicts the difference between sub-6GHz and mmWave [11].

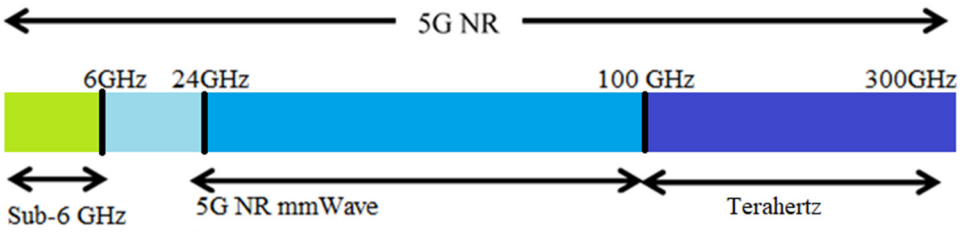


Figure 1.1: Comparison between sub-6GHz and mmWave

Compared with sub-6GHz, the advantages of mmWave are obvious. Due to the high frequency and large bandwidth, much more information can be carried by the waves. Approximately 10Gbps or higher data rates can be easily achieved and so high download and upload speeds, users may have better experiences. The other advantage is low latency, although latency with sub-6GHz has been improved significantly compared with the latency that accompanies 4G or 3G. The latency with mmWave can be further decreased to less than 1ms. With the extremely low latency provided, the traffic load can also be greatly reduced.

However, the drawbacks are also evident. The high frequency usually leads to high loss. Therefore, mmWave signal may not travel as far as the 4G signal does. High atmospheric attenuation means even raindrops can block the signal and diminish the performance. Currently, mmWave can only be used for short-range communication with distances of up to one kilometer. The second drawback concerns the power consumption and the heat created. Modules for mmWave usually cost much more power than those for low band

frequency. The balance between performance and power consumption should be treated seriously by IC scientists and engineers.

In order to solve the issues brought about by higher operating frequencies, such as low power consumption and high output power, RFIC researchers should propose new design methodologies to enhance the performance of RF FEM. Designing high-performance and low-cost 5G mmWave transmitters is the topic I am focused on in this thesis.

1.1.3 W-band

W-band usually refers to the range of the radio frequency from 75 to 110GHz [12] [13]. Due to high frequency, W-band can support a relatively high data rate throughput and wide bandwidth. With the development of 5G, an increasing number of communication service providers are considering introducing additional spectra to provide a better service. Subsequently, the W-band is now widely used. One of the most important applications of the W-band is for 5G backhaul. As communication service providers expand their signal to millimeter-wave bands, significantly higher demand for 5G backhaul has generated concerns for service operators. Compared with equipment with E-band (70 GHz-80 GHz) which are currently used, equipment with W-band can provide much better performance at the same distance.

1.2 Challenges and Motivations

Concerning the difficulties mentioned previously, the main challenges for RFIC design are balancing the performance, cost, power consumption and chip size. For transmitters operating in mmWave, it is particularly true for us to balance all the design targets. To be more specific, the single-pole double-throw (SPDT) switch has been widely used in wireless networks [14] [15] [16] [17], especially in mmWave. Some specifications for designing a high-performance SPDT in mmWave should be considered seriously, such as are insertion loss (IL), isolation (ISO), 1-dB compression point (P1dB), and cost. For this reason, it is very important that engineers treat the design seriously.

According to some latest literature, a typical E-Band or W-band transformer-based 2-way power-combined power amplifier (PA) implemented in bulk CMOS can provide a saturated output power of 15 dBm [18] [19]. Therefore, 15dBm P1dB is the minimum design target of the switch. However, most of the bulk CMOS-based switches operating in E-band or W-band can only provide a P1dB around 10 dBm [20] [21] [22] [23]. Therefore, there is a strong demand to further enhance P1dB of bulk CMOS-based mm-wave switch. The table below shows some switches designed by other researchers.

Ref.	[20]	[21]	[24]	[22]	[23]
f_c (GHz)	50-70	DC-60	50-67	130-180	58-85
Insertion Loss (dB)	1.5	2.5	1.9	3.3	1.8
Isolation (dB)	25	23	20	23.7	22
P1dB (dBm)	**13.5**	**7**	**10**	**11.5***	**10**
Area (mm^2)	0.28	0.04	0.6	0.0035	0.015
Tech. (nm)	90 CMOS	45 SOI	90 CMOS	65 CMOS	65 CMOS
Topology	λ/4-TL with shunt transistors	Series-shunt transistors	λ/4-TL with shunt transistors	Artificial resonator with shunt transistors	Transformer with shunt transistors

Table 1: Performance Summary of Switches from The Other State-Of-The-Art Bulk CMOS-Based Designs

Besides, among different building blocks in the RF front-end, there is no doubt that the power amplifier (PA) is also one of the most indispensable components. Designing a high-performance PA means having to consider several design trade-offs. The most critical design specifications are output power, linearity, efficiency, and stability. When moving into sub-THz, the modeling accuracy of passive components and parasitic elements of active devices become extremely critical. Any undesired modeling errors would cause a severe frequency shift as well as an impedance mismatch. For the worst-case scenario, the impedance mismatch would result in a stability issue. This is particularly true for mm-wave PA design. Table 2 below shows the latest performance of PA. To solve the challenges brought by FEMs operating in the frequency range of mmWave, some valuable design methodologies will be proposed and evaluated in this thesis.

Ref.	Freq. (GHz)	Tech.	Topology	Sat. Power (dBm)	Gain (dB)	Peak PAE (%)
[25]	113	65nm CMOS	3-stage 2-way cascode	13.8	13.4	10
[26]	86	65nm CMOS	3-stage 2-way comb.	11.9	18.6	9
[27]	110	65nm CMOS	3-stage 2-way comb.	14.8	14.1	9.4
[28]	100	65nm CMOS	4-stage	10	13	7

Table 2: Performance Summary of The PA from the Other State-Of-The-Art Designs

1.3 Contributions

To solve the issues brought about by mmWave, some new design methods for high-performance transmitters are introduced in this study. The specific significant contributions of this thesis are as follows.

Firstly, a symmetrical 90-GHz Single-Pole Double-Throw Switch designed in standard 55nm bulk CMOS technology has been described. The key design contributions of this work are using a passive-inspired approach to improve P1dB of mm-wave SPDT switch and using a combination of power splitting and impedance transformation network (ITN) technique. Secondly, a 90-GHz Asymmetrical Single-Pole Double-Throw Switch with >19.5-dBm 1-dB Compression Point in Transmission Mode Using 55-nm Bulk CMOS Technology has also been devised. One of the main contributions of this work is using a unique passive ring structure, which makes it possible for a relatively strong RF signal to pass through the TX branch, while the switching transistors are turned on.

To further build a high-performance transmitter operating in W-band, designing a PA is also one of my research objectives. The design of wideband PA using a balanced amplifier (BA) architecture along with edge-coupled quadrature couplers has been presented. Taking advantage of using of the BA architecture, good input and output impedance matching are achieved through a relatively wide bandwidth. Additionally, insights emerging from an edge-coupled quadrature coupler design are articulated.

Based on my measurements and assessments, it can be firmly concluded that my designs have been proved to meet our research targets and can be introduced in applications in advanced mmWave wireless communication systems.

1.4 Organization of The Thesis

This thesis is organized a shown in Figure 1.5 below.

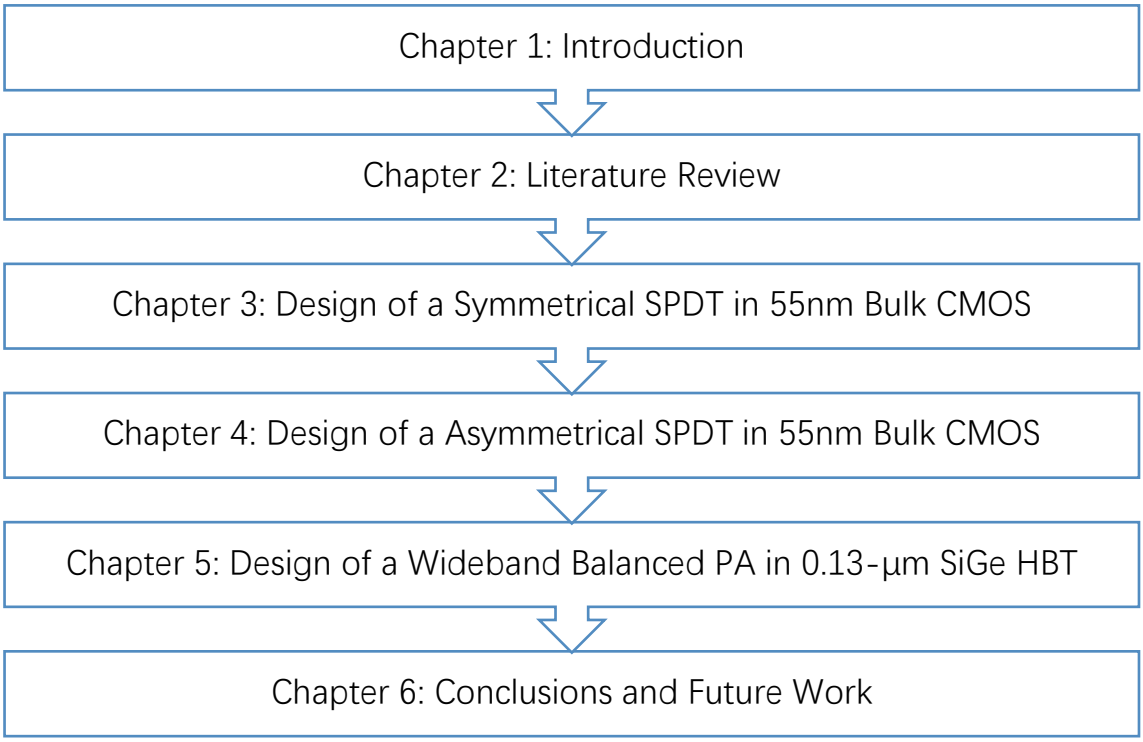


Figure 1.2: Thesis Organization

In Chapter 2 the research topic's background will be presented. Starting from the power amplifier to switch. Some important literature related to this research will be discussed in this chapter. In Chapter 3, a W-band symmetrical Millimeter-Wave CMOS Single-Pole Double-Throw Switch with Enhanced Power-Handling Capability is presented. The key design of this work is using a classical symmetrical architecture along with shunt-connected switching transistors. Furthermore, a novel design approach that combines both power dividing and impedance transformation techniques is described. By using a

symmetrical architecture with impedance transformation and power dividing techniques, this CMOS-based Single-Pole Double-Throw Switch can improve 1-dB compression point (P1dB) significantly at low cost. To prove the presented approaches are feasible in practice, a 90-GHz SPDT switch is designed in a standard 55-nm bulk CMOS technology. The design has achieved P1dB of 15 dBm with 3.5 dB insertion loss and 17 dB isolation. According to the measured results, this design can effectively improve the power-handling capability without significantly compromising other performance. It can be firmly concluded that the presented passive-inspired concept for switch design is useful, and breaks the basic limitation on the power handling capability of silicon-based switch design due to active device scaling.

In Chapter 4, a 90-GHz asymmetrical SPDT switch is presented. The presented approach is based on asymmetrical architecture. A passive ring structure is used to enable the use of ON-state switching transistors at TX mode, which results in a significantly enhanced P1dB. To prove the presented approaches are feasible in practice, the switch is designed in a standard 55-nm bulk CMOS technology. Based on the measurements and tests, it can be found that the presented novel concept is effective for switch designs using shunt-connected transistors. It overcomes the fundamental limitation on P1dB of silicon-based SPDT switch due to active device scaling.

In Chapter 5, a high-performance wideband millimeter-wave PA is also designed. To ensure the designed PA has sufficient output power, good PAE, superior input and output impedance matching across broadband, a balanced amplifier (BA) architecture is used. In particular, edge-coupled quadrature couplers are designed and their performance concerning magnitude error and phase error is minimized through a relatively wide bandwidth. A prototype PA is fabricated in a 0.13-μm SiGe HBT technology. Supplied by 5V power, the PA can provide more than 15 dBm saturated output power between 85-100 GHz that is equivalent to more than 16% fractional bandwidth. The peak PAE is better than 14% within this frequency range. The overall physical dimension of the designed PA is very compact. Including all pads, it is only 0.6 mm × 0.9 mm.

In the last chapter, the conclusion and suggestions for future work are presented.

1.5 Conclusion

In this chapter an overview of the thesis is presented. Introduced here are the background and basic information of 5G, mmWave and W-band. A summary of the author's contribution, as well as the organization of this thesis, are also presented in this chapter. In the next chapter some relevant studies on this topic will be reviewed.

Chapter 2: Literature Review

Transmitter plays an important role in radio frequency communication systems. There are generally many parameters we need to pay attention to when we design a switch, such as frequency, insertion loss, isolation, P1dB, and of course power consumption. The switch, especially SPDT is mainly used in transmitter in wireless communication. It is obvious that the performance of the SPDT can be improved by decreasing the insertion loss, increasing the isolation and P1dB, and minimizing the power consumption [29].

For PA design, there are also several design trade-offs we need to take into account. The most critical design specifications are output power, linearity, efficiency, and stability. In this chapter, some important studies related to this document are commented on.

2.1 Theoretical Basics

2.1.1 The Basic Technical Parameters of The Switch

There are many important technical indicators we need to take care of when designing a high-performance switch. These theoretical basics will be discussed in the sub-sections below.

2.1.1.1 Insertion Loss

Insertion Loss, as known as IL, is the loss of the signal power by inserting into a transmission line. It is usually calculated by decibels (dB). If we decide the original signal power as P_T, the signal power received after the load is P_R. Therefore, the Insertion Loss IL can be calculated utilizing the equation below:

$$IL(dB) = 10\log_{10}\frac{P_T}{P_R}$$

The insertion loss of an SPDT switch is dominated by two factors. The first main reason is the input signal. Since the circuit is not ideal in the real world, the input signal loss cannot be avoided by transferring between the paths. The second reason is the loss in the on-path of the switch [29]. Decreasing the IL should be an important design objective of this research on the SPDT switch.

2.1.1.2 Isolation

Isolation is the attenuation between the ports of the circuit [30]. A switch with high isolation can exhibit good signal integrity. High isolation is one of our design targets.

2.1.1.3 1-dB Compression Point (P1dB)

For linear components, the output power is usually a fixed ratio of the input power. However, for most nonlinear components, such as switches, the output power might loss more with increasing the input power. 1-dB compression point, which is known as P1dB, is also important for engineers to consider when designing the switch. P1dB is defined by calculating the difference between the output power and the output power plus 1dB [31].

In switch design, P1dB can be employed to measure the power-handling capability of the switch. Designing a SPDT switch with high P1dB, as well as superior power-handling capability, is also one of our main design targets.

2.1.1.4 Power Consumption

As many elements are usually used for mm-wave phased-array systems and SPDT switch must be used for each element, the power consumption of the switch cannot be neglected. It is important for researchers to design a high-performance switch which consumes as little power as possible.

2.1.1.5 Fabrication Process

Traditionally, the SPDT switches are designed in III/V technologies [32] [33-35], such as GaAs [32], due to its superior performance. However, the relatively high fabrication cost and limited integration capability are of concern. So, to further reduce the costs involved, tremendous efforts have been made to design efficient silicon-based switches in the last couple of decades [36-40].

Complementary Metal-Oxide-Semiconductor, as known as CMOS, is a type of fabrication process that uses p-type and n-type metal-oxide-semiconductor field-effect transistor (MOSFET) for Integrated Circuits design. The CMOS chips, which contain millions of transistors, can achieve high logic functions [41].

MOSFET was introduced and fabricated in 1960. Compared with some other technologies, such as Transistor-Transistor Logic (TTL), the early CMOS had many advantages, for example, low power consumption. However, due to its low operating speed, CMOS was only used initially in low-power devices, such as calculators and electric watches. The development of CMOS enabled it gradually replace TTL as the most famous MOSFET fabrication process for chip design in the 1980s. Due to low power consumption, low fabrication cost and high operating speed, CMOS plays an important role in the modern integrated circuit industry. According to statistics, more than 99% of

chips are made by CMOS currently [41] [42]. Consequently, to balance the cost and performance, bulk CMOS technology has been chosen as our fabrication process for the designs presented in this work.

2.1.2 The basic technical parameters of the PA

2.1.2.1 Saturated Power (P_{sat})

P_{sat} is the output power when the amplifier is saturated. It is the maximum output power that a PA can reach. The figure below is a presentation of the relationship between P_{sat}.

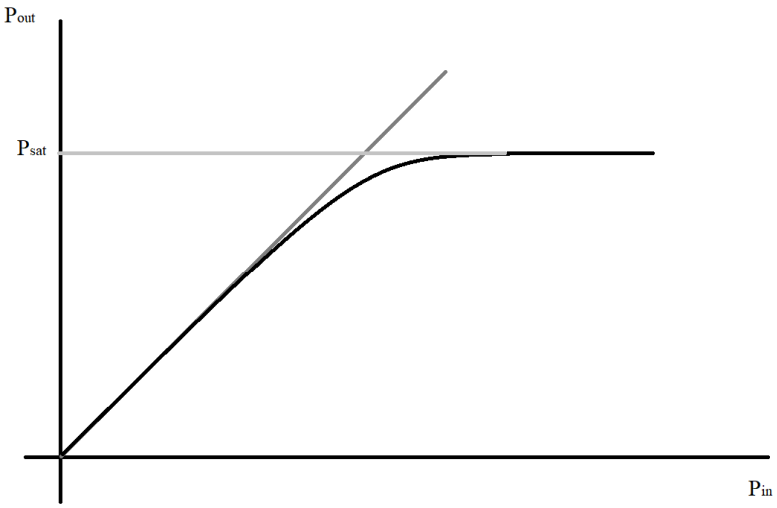


Figure 2.1: Saturated Power (Psat)

P_{sat} is one of the most important design indicators for PA. When the operating frequencies have been pushed from 6GHz to mmWave, the full potential of classical design methods of PA approach their performance limitations. Increasing the output power of PA, as well as P_{sat}, is one of the most important design aims in mmWave PA.

2.1.2.2 Power-Added Efficiency (PAE)

Power-added efficiency, as known as PAE, is also one of the most important specifications of a power amplifier. It is widely used to describe the efficiency of a power amplifier. It is the ratio of effective output power and the DC input power, while the effective output power is determined by the difference between output power and the input power of a power amplifier. The equation of PAE is shown below:

$$PAE(\%) = \left(\frac{P_{out} - P_{in}}{P_{DC}}\right) \times 100$$

In summary, PAE can be used to measure the efficiency of a power amplifier. According to some statistics [43], the power amplifier is the highest power consumption component in RF-related modules in a 5G base station. It is in fact quite necessary for the PAE of a PA to be enhanced.

2.2 Review of Related Research

2.2.1 Review of Related Research In SPDT Switch

The single-pole double-throw (SPDT) switch is perhaps the most indispensable building block in the time-division multiplexing (TDD) system, which makes it possible to share a single antenna for both TX and RX [44-47]. The design of a high-performance SPDT switch is a complicated task, one that involves several trade-offs among, insertion loss (IL), isolation (ISO), 1-dB compression point (P1dB) and cost.

Traditionally, SPDT switches are designed in III/V technologies [32], such as GaAs, due to its superior performance. However, the relatively high fabrication cost and limited integration capability are of concern. To solve these issues, tremendous efforts have been made in the last couple of decades for silicon-based switch design, from sub-GHz all the way to sub-THz[36-40]. For SPDT switch design operating below 30 GHz, many valuable designs have been described in several studies [36-40]. Using them, the SPDT switches designed in silicon-based technology can achieve good overall performance with dramatically reduced cost.

However, for designing switches which are operating in millimeter-wave (mm-wave) region, there is still a critical design issue that needs to be solved. The critical issue is about the limited P1dB. This is particularly true for switch design implemented in bulk

CMOS technology. According to our research, the latest bulk CMOS power amplifiers (PAs) operating at E- and W-band can achieve 15 dBm saturation power with a simple 2-way differential power combining [48]. Therefore, the required P1dB of a SPDT switch must be significantly higher than 15 dBm, which is currently not available. Most bulk CMOS-based SPDT switches operating in the mm-wave region have a P1dB around 10 dBm only [20-24] [51-54], which is not sufficient to be used along with the above-mentioned PAs to form a highly integrated T/R module.

Furthermore, as far as silicon-based SPDT switch design is concerned, both Silicon Germanium (SiGe) BiCMOS and SOI CMOS technologies have demonstrated great potential for power-handling enhancement [55, 56]. Effectively utilizing Heterojunction Bipolar Transistors (HBTs) in simple shunt-connected configuration, less than 2 dB IL, approximately 19 dB ISO and 17 dBm P1dB (without using negative control voltage) can be obtained for a 90-GHz SPDT switch with a power consumption of 5-6 mW [56]. However, it is still desirable to reduce the power consumption to as low as possible for the SPDT switch. Since a large number of elements are usually used for mm-wave phased-array systems and SPDT switch for each element, the power consumption of the switch cannot be neglected [44]. Furthermore, most advanced SiGe BiCMOS technology only has limited ability to deal with digital-intensive designs. As a result, the SiGe-based design is primarily limited to analog-intensive design, such as RF front-end modules. In

order to support both analog- and digital-intensive designs, an alternative strategy is to use SOI CMOS technology. It should be noted that using a simple shunt-connected configuration alone, the P1dB of SPDT switch designed in SOI CMOS is similar to its counterpart designed in bulk CMOS technology [21]. To significantly improve P1dB of SPDT switch, the negative control voltage along with stacked transistors must be utilized. However, the design of negative control voltage is not straightforward, and it might significantly increase die area overhead [57]. In addition, this approach cannot be simply transferred into designs implemented in bulk CMOS technology due to the physical limitations of MOSFET.

Thus, it is obvious to ask if it is possible to design mm-wave SPDT switches with enhanced P1dB in bulk CMOS technology, particularly using “shunt” switching transistors. As previously mentioned, the P1dB-related issue for switch design below mm-wave frequency region has been very well documented. Can these design techniques be directly transferred into mm-wave SPDT design? If not, what is the design limitation and how is it going to be solved? The main issues are the reduced threshold voltages (VTH) and the breakdown voltages of MOSFETs. As device is continuously scaled, the values of VTH and breakdown voltage are getting lower and lower. As a result, the P1dB-related issue becomes increasingly severe. It is noted that using classical design techniques, such as negative control voltage and AC-floating bias [39], the P1dB of the bulk CMOS-based

switch could be significantly improved. However, both techniques require special physical treatment, such as Deep N-well (DNW) technology, which results in additional fabrication cost. A simple but effective design approach that does not rely on negative control voltage must be presented to solve the P1dB-related issue in a cost-effective way. Since the limited P1dB is mainly constrained by active devices, it is worthwhile exploring a possible solution based on a passive-inspired approach [58-60], which is the motivation for undertaking this work. Another advantage of the passive-inspired approach is that it might be directly transferred to designs implemented in either SiGe or SOI CMOS processes as well and also can be used in conjunction with a negative control voltage if it is required. Finally, as will be seen in this thesis, the proposed approach can also be "scaled" to different operation frequencies by changing the length of transmission lines (TLs) used in the ring structure.

2.2.2 Review of Related Research In PA

mmWave integrated circuits designed in silicon-based technology have come a long way since the early 20s. Several ingenious circuit design techniques, including both passive and active components, have been extensively developed in the last decade [59, 61-68]. One of the main design issues related to PAs operating at sub-THz is low output power. For PAs operating at 60 GHz and below, power-combining techniques using a transformer have been widely adopted [69].

However, a 2-way power combining technique does not seem to provide a reasonable output power for PA operating at 100+ GHz. Thus, a more sophisticated output power combining network that is capable of 4-way power combining is required [25-28, 70-74]. Apart from this, to achieve a good output power with good stability across a broad bandwidth, balanced amplifier (BA) structures have been widely used in some literature [62, 75, 76].

The classical BA structure was first introduced in 1965 [75]. By implementing the BA structure, good input and output impedance matching can be achieved. Furthermore, compared with the standard structure of a single PA, high stability and linearity can also be obtained. BA is a structure with two identical amplifiers and two 90° couplers [76]. The figure below shows the simplified block diagram of the standard BA structure.

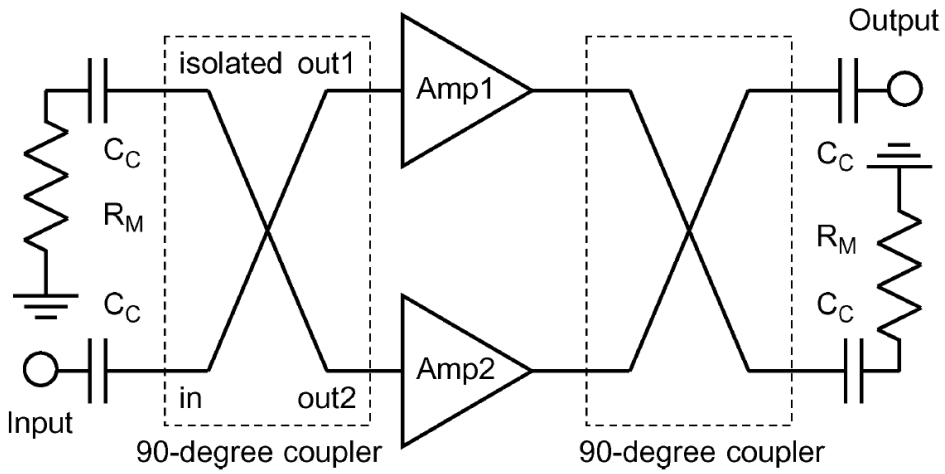


Figure 2.2: Simplified block diagram of the standard BA structure [76]

The above-mentioned BA has been used for many decades in any case [77-83]. However, as the science moves to sub-terahertz (sub-THz) or even terahertz (THz), these classical structures of BA may not be enough to meet the increasing requirements of high operating frequencies. It is now quite urgent for researchers to propose new structures.

Chapter 3: Design of a Symmetrical 90-Ghz Single-Pole Double-Throw Switch in Standard 55nm Bulk CMOS Technology

3.1 Abstract

Power-handling capability of bulk CMOS-based single-pole double-throw (SPDT) switch to operate in millimeter-wave (mm-wave) region is significantly limited by the reduced threshold voltage of active devices. The reason for this is device scaling. A passive-inspired solution is proposed in this paper. It still utilizes a classical symmetrical architecture along with shunt-connected switching transistors, but a novel design approach that combines both power dividing and impedance transformation techniques is used to improve 1-dB compression point (P1dB). Thus, the fundamental limitation of the power handling capability due to the reduced threshold voltage is removed. The 90GHz SPDT switch is implemented in a 55nm bulk CMOS technology and achieves a measured P1dB of 15 dBm and an insertion loss of 3.5 dB and an isolation of 17 dB. The total area of the chip is only 0.14 mm^2. Thus, the feasibility of the passive-inspired approach can be proved by the measured results.

3.2 Introduction

The single-pole double-throw (SPDT) switch is popular in modern information systems, especially time-division multiplexing (TDD) systems [17, 45, 46, 84]. According to the literature and basic knowledge, standard SPDTs may have two kinds of structures, asymmetrical and symmetrical ones. The asymmetrical architecture could potentially offer a better power handling capability than its counterpart designed in a symmetrical architecture. However, the design procedure for a SPDT switch using an asymmetrical architecture is more complicated than a symmetrical design. Thus, most previously published studies concentrated on symmetrical SPDT switch design. There are a few design parameters that should be taken into consideration, including insertion loss (IL), isolation (ISO), power-handling capability (both 1-dB compression point (P1dB) and cost. Although several high-performance SPDT switches implemented in bulk CMOS technology have been reported in [20-24, 37, 39, 40, 49, 55, 56, 84-86], for SPDT switch design operating at millimeter-wave (mm-wave) region, it is still preferred to be implemented in III/V technologies due to their superior performance.

To further reduce the design costs for SPDT switch design and anticipate the enactment of Moore's Law, extensive academic and industry-based silicon-based mm-wave SPDT switch design, especially using bulk CMOS technology, has been done in the last ten years. Several breakthroughs have been achieved for low-loss and high-isolation switches

design [20, 23, 55, 56, 85]. However, the limited power-handling capability, particularly P1dB, continues to be a problematic issue. It is noted that although the P1dB can be significantly improved by using negative bias voltages along with stacked transistors, it is usually not used for bulk CMOS-based design due to physical limitations. Therefore, bulk CMOS-based SPDT switch design is still preferred for employing the shunt-connected structure with quarter-wavelength transmission lines (TLs) for the sake of design simplicity.

As far as the requirement for P1dB of a SPDT switch is concerned, a typical E-Band or W-band transformer-based 2-way power-combined power amplifier (PA) implemented in bulk CMOS can provide a saturated output power of 15 dBm [86] [19]. Therefore, the required P1dB for a SPDT switch must be at least more than 15 dBm. However, bulk CMOS-based designs and most CMOS switches operating in E- and W-band can only provide a P1dB around 10 dBm [20, 21] [22] [23]. To support applications operating in these frequency bands, the current solution is to use Silicon Germanium (SiGe) technology [55] [56]. Taking advantage of relatively high threshold voltage (VTH) of HBTs, more than 17 dBm P1dB (without using negative bias voltage) can be obtained for a 90 GHz SPDT switch with a power consumption of 5-6 mW[56]. To further minimize power consumption and improve integration capability, it is highly desirable to design a bulk CMOS-based switch with significantly enhanced P1dB. To achieve this goal, a novel

design methodology for symmetrical SPDT switch operating at E- and W-band band will be proposed in this chapter.

In section 3.2 below, the fundamental issue causing the limited P1dB is emphasized first and then some classical designs used for SPDT design are summarized and then compared with the proposed approach in this work. The design considerations of the presented SPDT switch are reported in section 3.3. In section 3.4 the measurement results of the design are given. The conclusions are finally drawn in section 3.5.

3.2 Overview of Different Approaches for SPDT Switch Design and The Proposed Methodologies

As previously mentioned, the possibility of designing mm-wave CMOS switches using shunt-connected transistors along with a quarter-wavelength transmission line only for an enhanced power-handling capability is worth researching. The P1dB-related issue for switch design operating below the mm-wave frequency region has been very well documented in [37] [38] [39]. Is it possible to directly transfer these design techniques into mm-wave SPDT design? If not, what is the limiting factor and how is it going to be solved? The main issue is the reduced V_{TH} of transistors. Since the size of transistor is continuously shrinking, V_{TH} is getting smaller and smaller. Based on the analysis provided in [86], the P1dB issue becomes more and more severe.

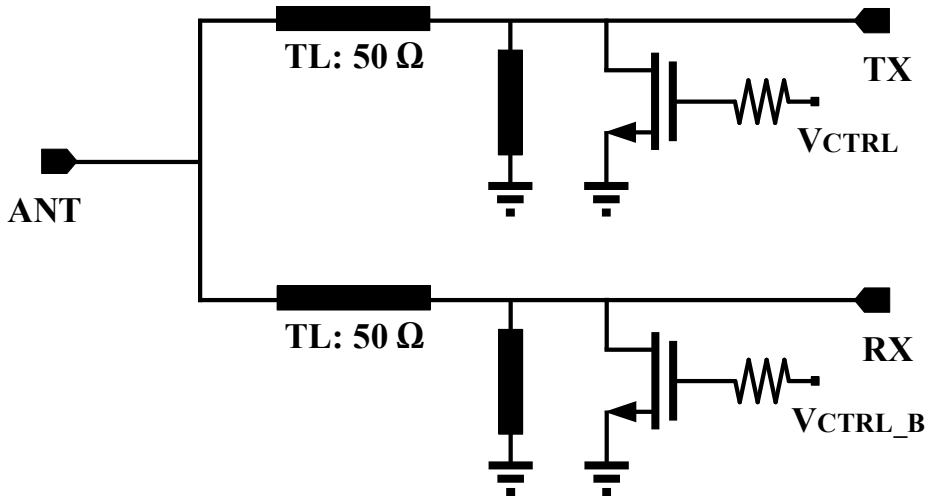
As mentioned before, the P1dB is mainly restricted by active devices, and for this reason, some possible passive-inspired methodologies will be discussed in this paper. The most important contributions of this work are summarized below:

- The concept of using a passive-inspired approach to improve P1dB of mm-wave SPDT switch is proposed.
- A combination of power splitting and impedance transformation network (ITN) technique is adopted for symmetrical bulk CMOS-based SPDT switch design.

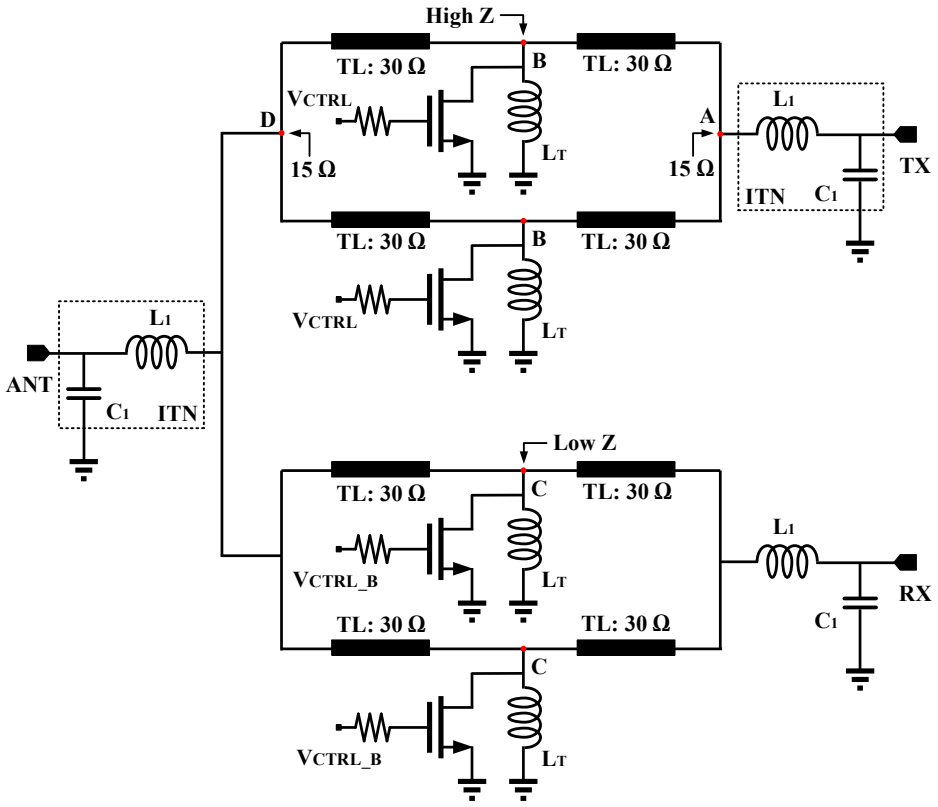
3.2.1 Overview of the Classical Designs

In order to obtain an improved P1dB without significantly affecting other performance parameters of the designed SPDT switch, a widely used solution for a SPDT switch design is based on an asymmetrical architecture [39] [40]. However, this solution usually requires series-connected transistors, which might not be suitable for the SPDT switch design operating at mm-wave region, particularly when operation frequency is pushed beyond 60 GHz. The factors that contribute to this situation include adding loss to the on-state and producing capacitive feeding through in the OFF-state of a switch with series-connected transistors [49, 85]. Therefore, most SPDT switches operating in mm-Wave might only use shunt-connected transistors.

The simplified schematic is shown in Fig. 3.1(a) [20]. However, this solution also has its own weaknesses that have been very well documented in the literature [56]. As the switch operates at TX mode, the shunt-connected transistor is turned off and it provides a high-impedance along with the shunt-connected TL by looking into ground. Thus, the RF signal can be transmitted from TX port to ANT port. According to the calculated data presented in [56], for a 65-nm CMOS technology, the measured value of P1dB from a typical switch is usually a few decibels higher than the simulated value. However, the OFF-state switching transistors might be turned on when a 3.6 dBm RF signal is transmitted. Thus, innovative designs must be put into practice to tackle this issue.


TL: 50 Ω
TX
VCTRL
ANT
TL: 50 Ω
RX
VCTRL_B

(a)


High Z
TL: 30 Ω
B
TL: 30 Ω
VCTRL
D
A
L1
15 Ω
LT
15 Ω
TX
ITN
C1
TL: 30 Ω
B
TL: 30 Ω
VCTRL
LT
L1
ANT
C1
ITN
Low Z
TL: 30 Ω
C
TL: 30 Ω
L1
VCTRL_B
LT
RX
C1
TL: 30 Ω
TL: 30 Ω
C
VCTRL_B
LT

(b)

Figure 3.1 The simplified circuit schematic of symmetrical SPDT switch, (a) classical shunt-connected transistor with quarter-wavelength transmission line, (b) the proposed power dividing and impedance transformation network-based design.

3.2.2 Description of the Proposed Passive-Inspired Design

Since the active device has almost reached its fundamental limitation, the only way to solve the above-mentioned issue is to explore the possibility from a passive design perspective. A possible solution is proposed in this paper and its simplified schematic can be found in Fig. 3.1(b). As it can be observed from this figure, this design is based on a symmetrical SPDT architecture, which employs a combination of power dividing and impedance transformation techniques. When an RF signal is injected into the TX port, it goes through an ITN unit first, which is formed by an LC network that consists of L_1 and C_1. It is noted that the ITN-related techniques have been previously presented in the literature [87, 88], but they have primarily been used for switch design operating at sub-GHz. Using the ITN unit, the common-mode impedance looking into node A is transferred from 50 to 15 Ω. Then, the RF signal is divided into two paths.

Each path consists of two 30-Ω quarter-wavelength TLs, a switching n-type field-effect transistor (nFET) and a lumped inductor, L_T. At TX mode, the two nFETs are switched off. In this way a shunt LC network is built by the parasitic capacitance (known as C_{OFF}) and the L_T. By looking into the ground, the constructed network can produce the required high impedance at node B. Meanwhile, the two nFETs at the RX branch are switched on,

which results in a low impedance at node C by looking into the ground. Consequently, the RF signal will not flow into the RX branch at TX mode. Once the RF signal passes through the switching section, the two divided signals are combined at node D and the impedance is transferred back to 50 Ω at the ANT port. It must be noted that the power-combining network used at the input of the designed switch may not be necessary if a power-combined PA is used. For such a case, the power-splitter network and the ITN unit could be co-designed with each power cell used for the PA. As a result, the ITN unit could be embedded into the power-combining network to further minimize the overall insertion loss of the switch.

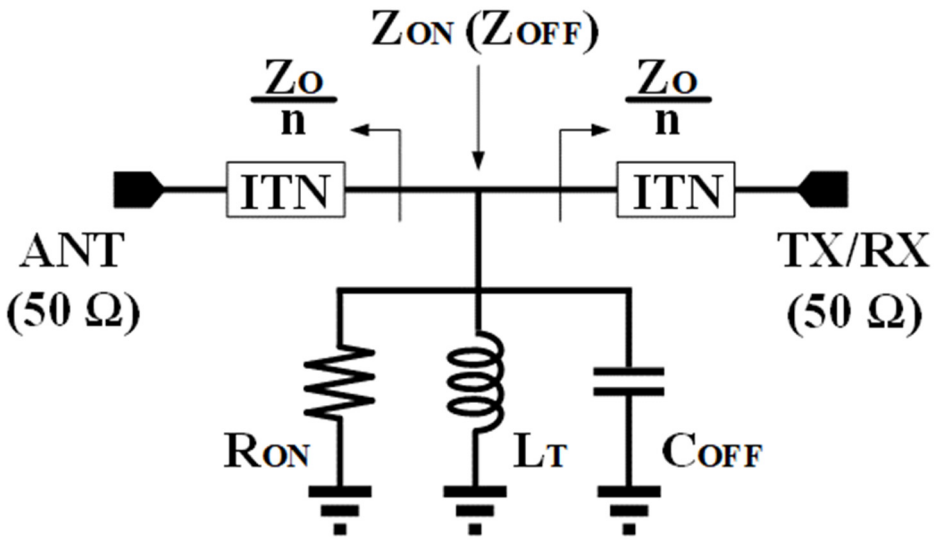


Figure 3.2: The conceptual block diagram of using ITN units for switch design.

3.3 Design Considerations for the Symmetrical SPDT Switch

In order to effectively improve the power-handling capability of a SPDT switch, it is necessary to understand the relationship among different design specifications, especially P1dB, IL and ISO. The P1dB limitation of a SPDT switch using shunt-connected switching nFET along with quarter-wavelength TLs can be estimated using the equation given below,

$$P_{1dB\_min} = \left(\frac{2V_{TH}}{\sqrt{2}}\right)^2 \times \frac{1}{Z_o} \quad (1)$$

where Zo is the load/source impedance that is typically 50 Ω. As shown in (1), to improve P1dB, two approaches can be used. One is to increase the value of V_{TH} and another is to reduce the value of Zo. As previously mentioned, the threshold voltage cannot be simply changed from the circuit design perspective.

On the other hand, the value of Zo can be potentially controlled using the previously mentioned impedance transformation technique. The key idea is that instead of using a standard 50-Ω impedance for internal matching, two ITN units can be inserted between the load/source terminals and the drain terminal of the switching nFET. The conceptual block diagram of this arrangement is given in Fig. 3.2 above. The internal impedance looking into the ITN unit from the drain terminal of a nFET is expressed in (2),

$$Z_{Int} = \frac{Z_o}{n} \quad (2)$$

where n is a ratio between the standard 50-Ω impedance and Z_{Int} that is transferred by the ITN unit. The value of n can be selected accordingly. Substituting (2) into (1), the expression of P1dB is rewritten as,

$$P'_{1dB\_min} = \left(\frac{2V_{TH}}{\sqrt{2}}\right)^2 \times \frac{n}{Z_o} \tag{3}$$

According to (3), if the value of n is greater than 1, the power handling capability of the switch can be improved. However, the impedance mismatch between the internal impedance, Z_{Int} and the impedance looking into the drain terminal of the switching nFET may also exert an impact on other aspects of performance, such as IL and ISO. This impact can be calculated by using S_{21} parameter and expressed in (4a) and (4b), respectively:

$$IL_{Imp\_mismatch} = \frac{2}{2+\frac{Z_o}{Z_{OFF}}\times\frac{1}{n}} \tag{4a}$$

$$ISO_{Imp\_mismatch} = \frac{2}{2+\frac{Z_o}{Z_{ON}}\times\frac{1}{n}} \tag{4b}$$

As shown in (3) and (4), although using a large value of n is preferred for an improved P1dB and IL, it could deteriorate ISO of the switch. A design trade-off between different design specifications emerges and thus the value of n must be carefully selected. Moreover, the ideal loss-less passive network does not exist in practice. The additional IL due to parasitic loss effects of non-ideal ITN units also needs to be taken into

consideration. The additional IL caused due to limited Lossy_Q of passive devices is defined as,

$$IL_{Lossy\_Q} = -20 \times Log_{10}(1 + \frac{Q}{Q_c}) \quad (5)$$

where $Q = \sqrt{n-1}$, Q_c is the Q-factor of the ITN unit. In general, the value of Q_c is around 10 for a standard bulk CMOS technology, if a simple LC network is used. Thus, (5) can be rewritten as,

$$IL_{Lossy\_Q} = -20 \times Log_{10}(1 + \frac{\sqrt{n-1}}{10}) \quad (6)$$

Therefore, the overall IL and ISO of the switch using the block diagram shown in Fig. 3.1b can be empirically calculated using (7a) and (7b).

$$IL_{Total} = -40 \times Log_{10}\left(1 + \frac{\sqrt{n-1}}{10}\right) + 20 \times Log_{10}\left(\frac{2}{2+\frac{Z_o}{Z_{OFF}} \times \frac{1}{n}}\right) \quad (7a)$$

$$ISO_{Total} = -40 \times Log_{10}\left(1 + \frac{\sqrt{n-1}}{10}\right) + 20 \times Log_{10}\left(\frac{2}{2+\frac{Z_o}{Z_{ON}} \times \frac{1}{n}}\right) \quad (7b)$$

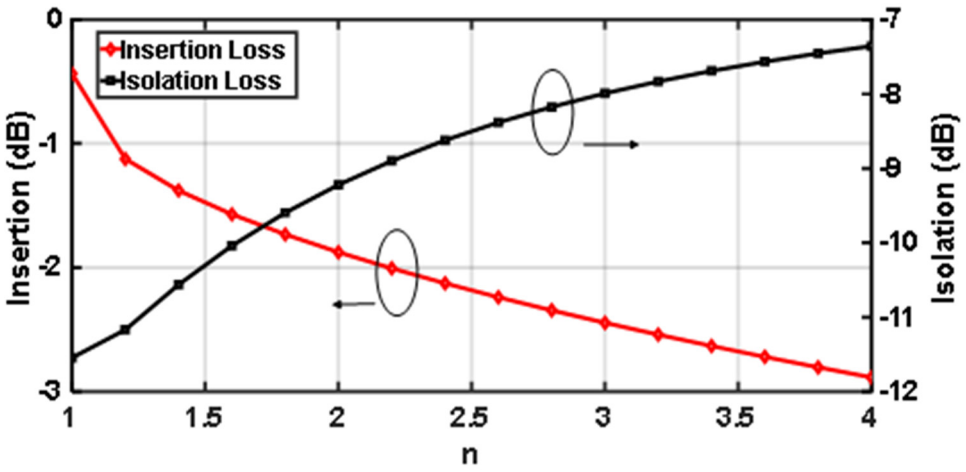


Figure 3.3: Design trade-offs between insertion loss and isolation of the designed switch by selecting different values of n

Using these equations both the IL and ISO are calculated and plotted. The results are given in Fig. 3.3. As illustrated, although a large impedance transformation ratio results in a significantly improved P1dB, the deterioration of IL and ISO is quite severe. For an optimized design, the value of n is selected to be 1.7, which gives an approximately 30-Ω internal impedance.

As previously stated, power-combining techniques have been widely used for designing PA to enhance the saturated output power. From SPDT switch design point of view, if the designed switch is placed after the power-combining network, it must have a superior power handling capability that might not be achievable in practice for bulk CMOS-based designs. Therefore, an alternative design approach is to include the switch design (like the one presented in Fig. 3.2) into each power cell. In such a way, the power handling requirement could be greatly relaxed.

To verify the presented concept is useful in practice, the 55-nm bulk CMOS is chosen as the fabrication process for our designed SPDT switch. The selected technology has many advantages. First, the chosen technology can provide high-performance nFET with ft of 200 GHz. It can also provide 8 metal layers of aluminium as the thick top metal layers. The size of switching nFETs must be carefully determined first. The classical figure-of-merit (FoM) – product of R_{ON} times C_{OFF} is used in this design because it gives a good first-order indication of switching capability of the selected transistors. The simulated switching performance in terms of R_{ON} and C_{OFF} as a function of the width of a nFET is given in Fig. 3.4, while the length of the nFET is kept to be the minimum that is 55 nm. As can be seen from Fig. 3.4, an optimized performance can be achieved, while the value of nFET's width is 50 μm.

Furthermore, as previously discussed, the inductor LT is required to form a resonator with the switching nFET. By using a grounded inductor at the designed frequency, the L_T can be determined as 170 pH. This nFET-microstrip-line-based LC tank will provide 480-Ω and 9-Ω impedances, respectively, when the nFETs are switched off and switched on from a schematic simulation. Moreover, as shown in Fig. 3.1, a resistor is always used at the gate terminal of the switching nFET. The selected value for this resistor is critical as it has some adverse impacts on the overall performance of the designed SPDT switch, such as switching speed between TX and RX modes and isolation/insertion loss. To improve

the switching speed, relatively less resistance is desirable. However, using a smaller value of the resistor at the gate terminal reduces the isolation between the gate and ground, which results in a deteriorated IL of a switch [24]. Thus, the value of this resistor needs to be carefully determined through design optimization.

Finally, as shown from Fig. 3.1, TLs are extensively used. Fig. 3.5 shows the cross-section view of the designed transmission line. To avoid unnecessary coupling, TLs use metal walls built by stacking all metal layers together. It can be measured that the topmost metal layer has a thickness of 1.325 μm. In addition, Metal 1 is only reserved for DC and the ground plane is made by using a combination of M2 and M3. As the TLs with different characteristic impedance are used in this design, depending on the required impedance, the width of TL can be effectively adjusted. Based on the EM simulated results, the 30-Ω TL has a width of 10 μm for signal path and a width of 4 μm for the gap between the signal path and the ground wall, while the width of the signal path and the gap are both 10 μm for a 50-Ω TL.

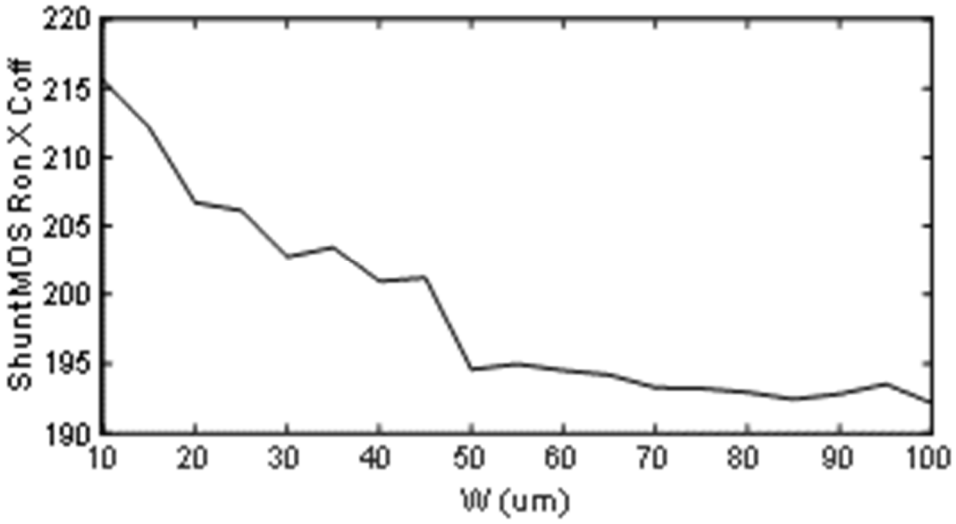


Figure 3.4: The simulated $R_{ON} \times C_{OFF}$ as a function of the width of the nFET.

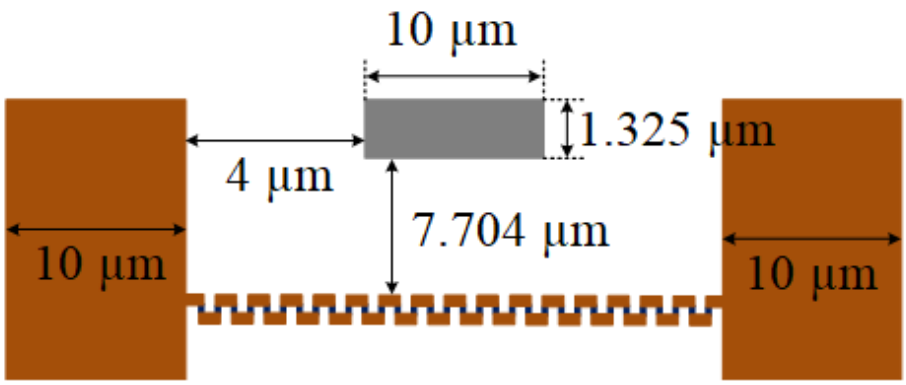


Figure 3.5：Cross-section view of the implemented TL (for 30-Ω impedance) used in this design with physical dimensions.

3.4 Measurement Results

To find out how well the design performs the design is fabricated in bulk CMOS. Without the pads, the die size of this design amounts to only 0.3 × 0.44 mm^2. The die microphotograph is illustrated in Fig. 3.6. The on-wafer test results are measured by using 100-µm pitch Ground-Signal-Ground (G-S-G) Infinity Probes with 1-mm connectors from FormFactor™, Inc. The frequency set by the vector network analyzer (VNA) is up to 110GHz. The model of VNA is N5290A, which is produced by Keysight™.

The short-load-open-thru (SLOT) has been widely used for on-wafer calibrate. It is a method of moving the reference plane from the equipment connectors to the tips of the G-S-G RF probes. To better compare the results, both S-parameters from EM simulation and measurement are recorded and presented clearly. The frequency responses of this design in terms of input and output return losses are given in Fig. 3.7. Added to this, the output return loss is the same. As can be seen, the input return losses are better than -10 dB between 87 GHz and 110 GHz (limited by the VNA). Therefore, broadband matching is achieved for the designed SPDT switch.

It is noted that as this design is based on a symmetrical configuration, one of the TX/RX ports is terminated with an on-chip 50-Ω resistor. When the V_{CTRL} = 0 V and the V_{CTRL_B} = 1.2 V are applied, the IL of the designed switch is measured. The result is presented in Fig. 3.8(a). As shown, from 87-100 GHz, the insertion loss is approximately 3.5 dB and

it is slightly increased to 4.1 dB beyond 100 GHz. On the other hand, when the $V_{CTRL} = 1.2V$ and the V_{CTRL_B} = 0 V are applied, the ISO of the switch is taken, which is shown in Fig. 3.8(b). As illustrated, the measured ISO varies from -18 dB to -16 dB across the bandwidth between 87 to 110 GHz, which is to be expected. At 90 GHz, the insertion loss and the isolation are better than 3.5 dB and 17 dB, respectively.

In order to further verify the power-handling capability of the designed SPDT switch, power measurements are also conducted using the set-up given in Fig. 3.9(a). On the input side, a low-frequency signal is generated by a signal generator (E8257D) made from Keysight™. On the input side, a low-frequency signal is generated by a signal generator (E8257D) produced by Keysight. After that, the generated signal is fed into a Signal Generator Extension Module (SGX) made from Virginia Diode (VDI™). The specific model number is WR12SGX. The selected SGX is an E-band source module that can generate up to 16 dBm output power at 90 GHz. The signal source is then connected to a SAGE™ voltage-controlled attenuator (VCA) along with a SAGE™ W-band power amplifier (PA) module that features a P1dB above 28 dBm at 90 GHz. A 10-dB coupler is used along with a power sensor (U8489A) made by Keysight™ to monitor the power level of the switch. On the output side a power meter (PM5B) from VDI™ is used. Power levels from both the input and output side were calibrated to the probe tips. The power difference between the input probe tip and the coupled port is fixed, enabling the

power levels of the input and output to be measured at the same time [55, 56]. It is noted that the large signal is injected into the TX port in the measurements. The measured P1dB and the insertion loss of the designed switch are given in Fig. 3.9(b). As illustrated, a P1dB of approximately 15 dBm is achieved.

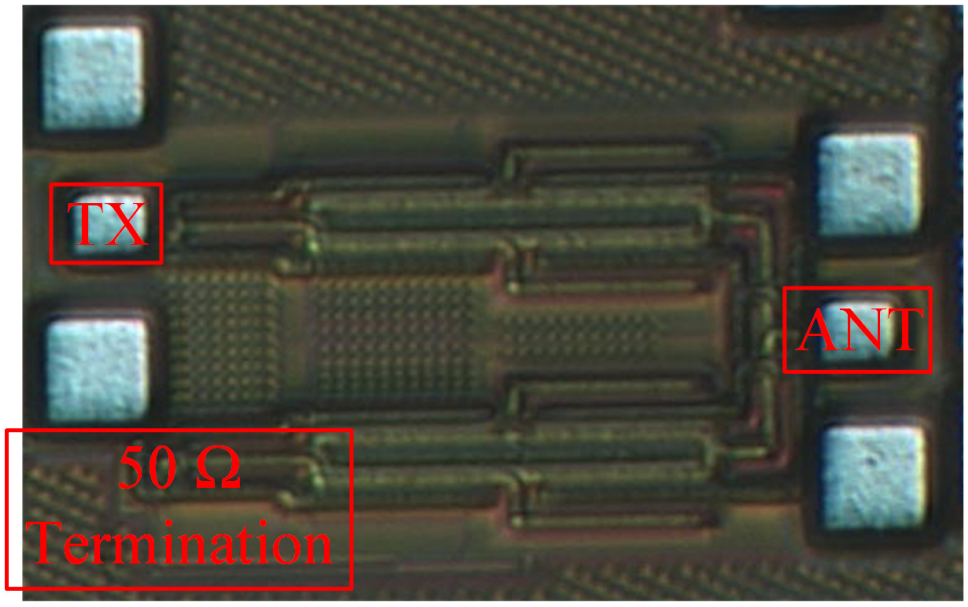


Figure 3.6: Die microphotographs of the designed SPDT switch.

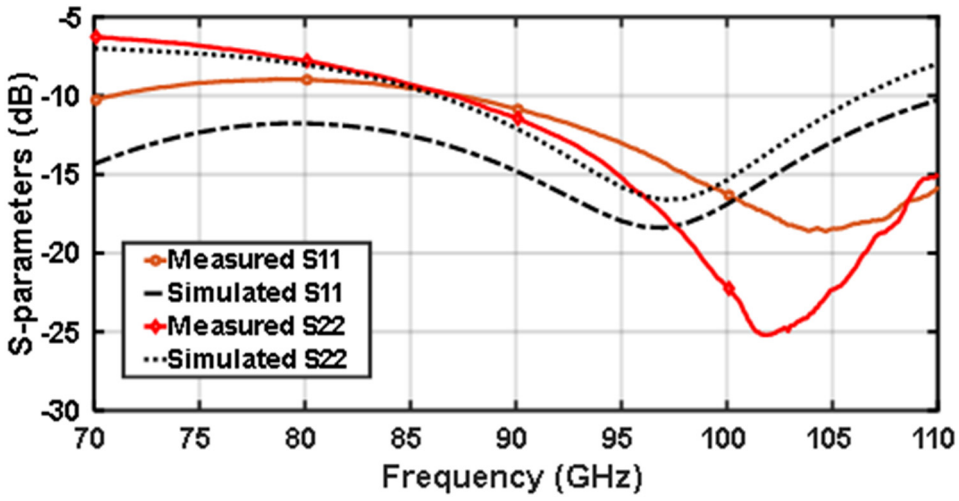
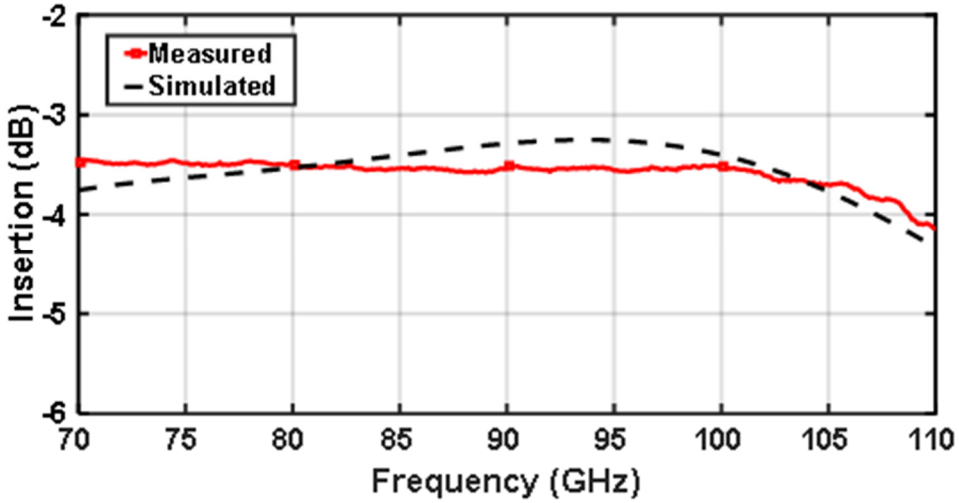
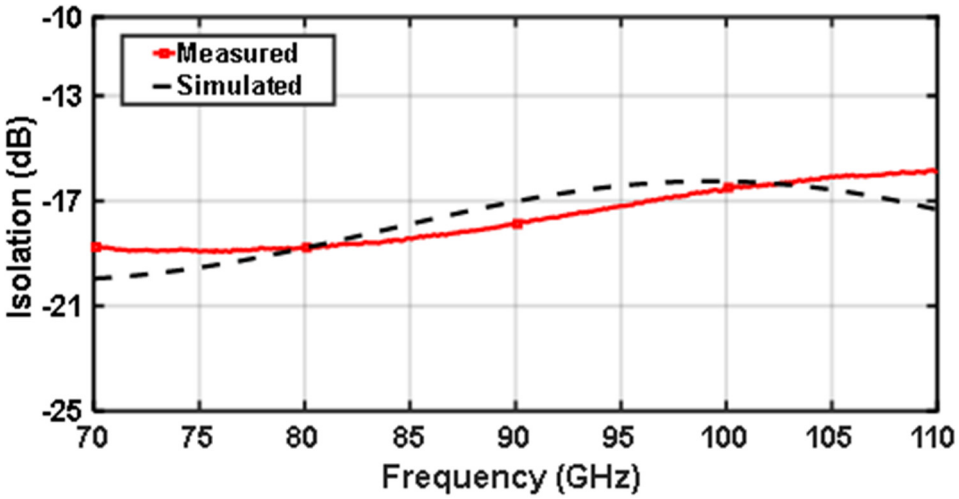


Figure 3.7: Measured and simulated input and output return losses of the designed SPDT switch.

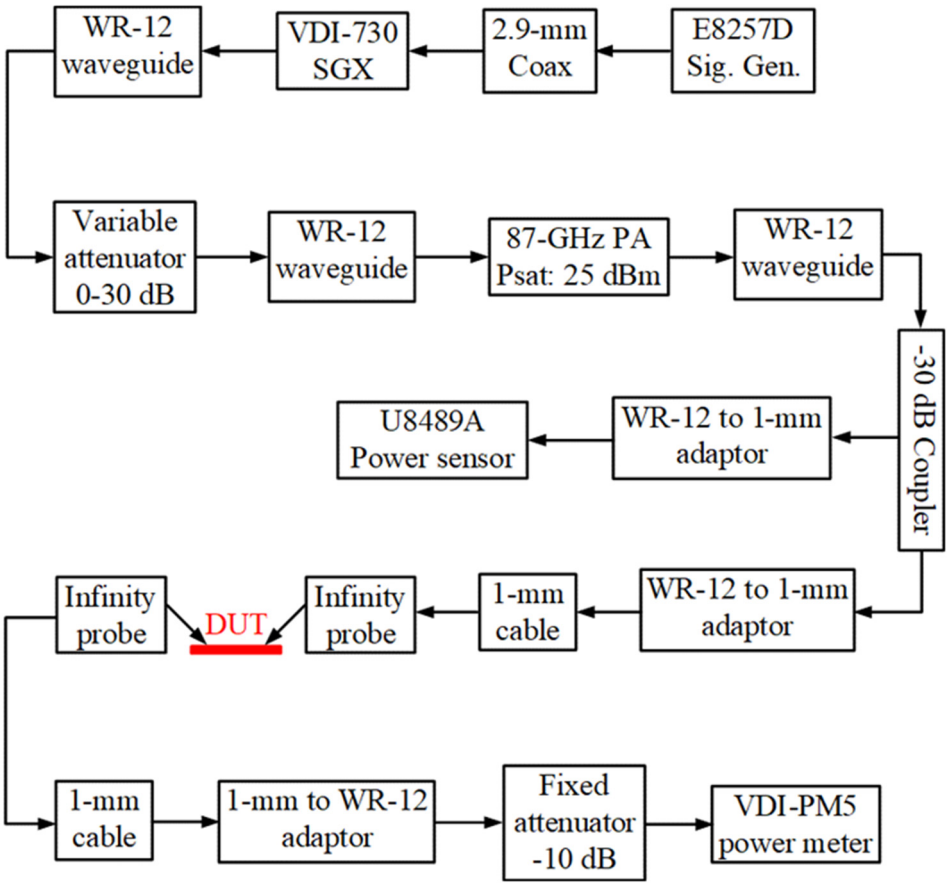


(a)

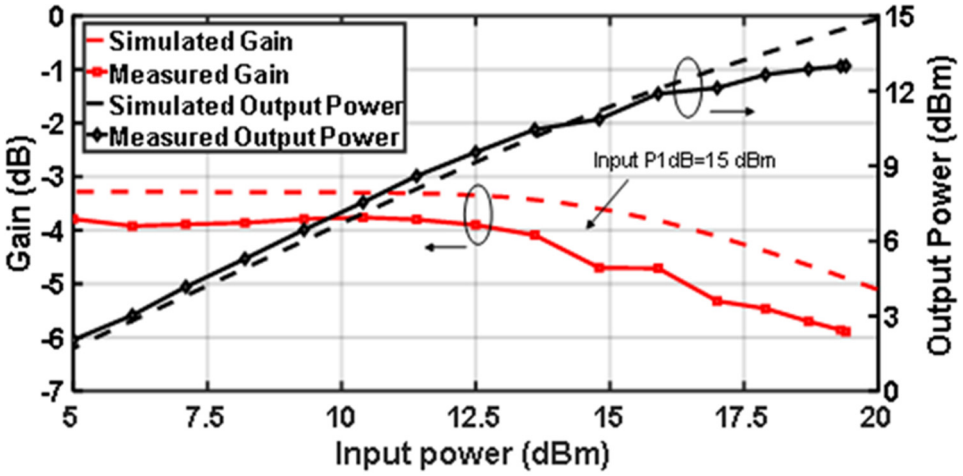


(b)

Figure 3.8: Measured and simulated insertion loss and isolation of the designed SPDT switch, (a) insertion loss, (b) isolation.



(a)



(b)

Figure 3.9: Measured power-handling capability of the designed switch (a) measurement set-up for P1dB characterization (b) the measured P1dB for the designed switch.

Comparisons of the performance between the presented symmetrical SPDT switch and the other state-of-the-art designs are given in Table 3 below. The following observations can be made by comparing with these results. First, as shown in the table, the HBT-based designs, including both InP and SiGe, have demonstrated superior performance in terms of IL, ISO and P1dB. However, the disadvantages of these solutions are also obvious. Compared with CMOS-based solutions, the power consumption of HBT-based designs is fairly higher. Consequently, these designs may not suitable for low-energy devices.

REF.	f_c (GHz)	Insertion loss (dB)	Isolation (dB)	P1dB (dBm)	Power consumption (mW)	Area (mm^2)	Tech. (nm)	Topology
[46]	92-98	2	20	n/a	4.8	n/a	130 InP HBT	λ/4-TL with shunt transistors
[55]	77-110	1.4	19.3	19	8	0.14	90 SiGe HBT	λ/4-TL with shunt transistors
[56]	73-110	1.1	22	17	5.9	0.213	90 SiGe HBT	λ/4-TL with shunt transistors
[36]	DC-20	2	21	30	0.0	0.17	130 CMOS	Series-shunt Transistors
[20]	50-70	1.5	25	13.5	0.0	0.28	90 CMOS	λ/4-TL with shunt transistors
[24]	50-67	1.9	20	10	0.0	0.6	90 CMOS	λ/4-TL with shunt transistors
[23]	58-85	1.8	22	10	0.0	0.015	65 CMOS	Transformer-based-TL with shunt transistors
[21]	DC-60	2.5	23	7	0.0	0.04	45 SOI	Series-shunt transistors
[22]	130-180	3.3	23.7	11.5*	0.0	0.0035	65 CMOS	Artificial resonator with shunt transistors
THIS DESIGN	**87-100**	**3.5**	**17**	**15**	**0.0**	**0.14**	**55 CMOS**	**ITN & input power dividing**

Table 3: Comparison of the presented switches with some other designs described in various studies

Secondly, the achieved P1dB for most of state-of-the-art CMOS-based designs that using shunt-connected switching transistors are quite similar. As shown in [22] and [23], both of them are designed in standard 65-nm bulk CMOS technology. The operational frequencies of them do differ but all the obtained P1dB are limited to be about 10 dBm. Therefore, the factor that contributes to the limited P1dB is not the operating frequency but the value of V_{TH}. Another example can be found in [21], without using stacked transistors with negative bias voltage, a SPDT switch fabricated in a 45-nm SOI CMOS

can only provide a P1dB of approximately 7 dBm. It can be concluded that designing a SPDT switch in a fabrication node with a relatively higher V_{TH} might be a possible solution to significantly enhance power-handling capability. As demonstrated in [20], a 90-nm CMOS process is used for SPDT switch design operating at 60 GHz. Comparing with the P1dB performance presented in [22, 23], this one has improved by approximately 3 dB. However, to enhance the performance of other circuit building blocks in the transmitter, for example, power amplifiers, it is important to design and fabricate the circuits with a technology node with lower V_{TH}. Consequently, the contradictory choice between selecting the proper designs in RF front-end blocks might be inevitable.

In this work, the presented design uses a symmetrical configuration that is the same as the other classical designs. Additionally, the design is implemented in a 55-nm CMOS that has a similar threshold voltage with a 65-nm CMOS. Subsequently, the expected P1dB from the benchmarks should be around 10 dBm as well. However, using the presented design approach – a combination of impedance transformation and input power dividing technique, the P1dB of this design is improved by 5 dB. This design's drawback is approximately 1.5 dB more insertion loss compared with the other state-of-the-art designs, but this can be fully justified by the significantly improved power-handling capability. Furthermore, the insertion loss could also be reduced by using an ultra-thick metal layer (that is currently not available in this process) for the implementation of

passive components, such as TLs and inductors, in this case. Finally, the presented switch is based on a passive-inspired solution. Therefore, the demonstrated concept of design might also be efficiently used along with high V_{TH} devices and negative bias voltage. It can be predicted that this new CMOS-based SPDT switch can finally reach the same P1dB performance which can be achieved by HBT-based designs.

3.5 Conclusion

The passive-inspired approach for millimeter-wave CMOS-based SPDT switch with improved power-handling capability is presented in this work. A symmetrical architecture is used along with impedance transformation and power dividing techniques. The designed switch is implemented in a standard bulk 55-nm CMOS technology to prove the feasibility of this concept. By analysing the measured results, it is found that the design can effectively improve the power-handling capability without significantly compromising other performance. The main conclusion that can be drawn is that the presented passive-inspired approach for switch design is useful. It also breaks the fundamental limitation on the power handling capability of silicon-based switch design due to active device scaling.

Chapter 4: Design of a 90-GHz Asymmetrical Single-Pole Double-Throw Switch with >19.5-dBm 1-dB Compression Point in Transmission Mode Using 55-nm Bulk CMOS Technology

4.1 Abstract

The millimeter-wave (mm-wave) single-pole double-throw (SPDT) switch designed in bulk CMOS technology has limited power-handling capability in terms of 1-dB compression point (P1dB). This is mainly due to the low threshold voltage of the switching transistors used for shunt-connected configuration. To solve this issue, an innovative approach is presented in this work, which utilizes a unique passive ring structure. It allows a relatively strong RF signal passing through the TX branch, while the switching transistors are turned on. In this way the fundamental limitation for P1dB due to reduced threshold voltage is overcome. To measure the real performance in the lab, a 90-GHz asymmetrical SPDT switch is designed in a standard 55-nm bulk CMOS technology. The design has achieved an IL of 3.2 dB and 3.6 dB in TX and RX mode, respectively. Moreover, more than 20 dB isolation is obtained in both modes. Because of using the proposed passive ring structure, a remarkable P1dB is achieved. No gain

compression is observed at all, while a 19.5 dBm input power is injected into the TX branch of the designed SPDT switch. The die area of this design is only 0.26 mm^2.

4.2 Introduction

The single-pole double-throw (SPDT) switch is perhaps the most indispensable building block in a time-division multiplexing (TDD) system, which enables sharing of a single antenna for both TX and RX [47] [33-35]. The design of a high-performance SPDT switch is a complicated task. For IC designers, it is very important to balance multiple parameters, such as insertion loss (IL), isolation (ISO), 1-dB compression point (P1dB) and cost. Traditionally, the SPDT switches are designed in III/V technologies, such as Gallium Nitride (GaN) and so on [32]. However, the relatively high fabrication cost and limited integration capability are of real concern. To solve these issues, much effort has been expended in the last couple of decades to improve silicon-based switches design, from sub-GHz all the way to sub-THz [37] [36] [38] [40]. For a switch design operating below 60 GHz, SOI and bulk CMOS technologies are the most popular ones due to their relatively lower fabrication mass production costs. Several novel design have been presented by many other researchers [37] [36] [38] [39] [40] [20] [89] [90] [34, 51-54]. When the operating frequency is pushed to above 60 GHz, a few problems remain for silicon-based SPDT switch design, especially bulk CMOS-based designs. One of the

critical issues is the limited power-handling capability in terms of 1-dB compression point (P1dB).

As described in the latest developments of E- and W-band power amplifiers (PAs) designed in bulk CMOS technology, it can be concluded that the latest PAs can have more than 15-dBm saturation power with a simple power combining structure [48] [19]. The P1dB of a SPDT switch must be significantly higher than this value, which is currently not available. Most bulk CMOS-based SPDT switches operating in millimeter-wave (mm-wave) region have a P1dB around 13 dBm only [49] [23] [56] [91] [91] [92] [93] [94] [95] [96] [97] [98] [90] [99] [100] [101], which is not sufficient to be used along with the above-mentioned PAs to form a highly integrated T/R module. The question needs to be asked, if it is possible to design mm-wave SPDT switches with an enhanced P1dB in bulk CMOS technology. To address this issue, an innovative passive-inspired design approach will be presented in this work.

The rest of this paper is organized as follows. In section 4.3, the classical design techniques for P1dB enhancement are overviewed. In section 4.4, the concept of using the proposed approach for asymmetrical SPDT switch design is explored. The detailed device-level implementation is shown in section 4.5. The measurement results are given in section 4.6 and the conclusions are finally drawn in section 4.7.

4.3 Overview of Design Approaches for Enhanced Power-Handling Capability

Regardless of the operation frequency of the SPDT switch, one of the limiting factors for achieving an enhanced P1dB is the reduced threshold voltage (VTH) of MOSFETs, which has been very well documented in [37] [38] [39] [56]. This is particularly true for the designs that only utilize the so-called shunt-connected transistors. As the active device is continuously scaled for mm-wave circuit design, the values of VTH and breakdown voltage are getting lower and lower. As a result, the P1dB-related issue becomes increasingly severe. This is particularly true for the designs that are made in bulk CMOS technology. A simple but effective design approach must be proposed to enhance the capability of handling power in a low-cost way.

As far as SPDT switch design is concerned, it could be categorized into two parts. One is an active-inspired design, and another is a passive-inspired one. The former has been used as the driving force for several years. Many classical design techniques, such as negative control voltage and AC-floating bias [39], have been extensively used to improve the P1dB of the bulk CMOS-based design. However, both techniques require using special physical treatments, for instance Deep N-well (DNW) technology, which results in additional fabrication costs. Another classical design approach is to use a combination of the stacked transistor with negative bias voltage. Although this approach can be used in SOI CMOS-based designs, it cannot be simply transferred into bulk CMOS-based design

due to the physical limitation of MOSFET. Additionally, the design of a negative control voltage generator is not straightforward, and it might significantly increase die area overhead [57].

To further understand the principles of how to enhance the power-handling capability for SPDT switch design, four classical design approaches are overviewed in Fig. 4.1. As can be seen in Fig. 4.1(a), the concept of using an impedance transformation network (ITN) for symmetrical SPDT switch design is presented [37]. However, this approach results in an inherent design trade-off between P1dB and ISO for a symmetrical SPDT switch. To obtain both high P1dB and ISO for a SPDT switch, an asymmetrical structure is used. A typical asymmetrical SPDT structure is given in Fig. 4.1(b) [39] [24]. Utilizing the design flexibility obtained from the asymmetrical structure, the performance of P1dB and ISO can be optimized separately. If a DNW or SOI technology is available, the P1dB could be even further enhanced by stacking of multiple transistors, as demonstrated in Fig. 4.1(c) [38].

It is noted that although using asymmetrical structures for SPDT switch design has successfully demonstrated a great performance improvement at 30 GHz and below, none of these techniques might be fully functional. This is especially the case if the operational frequency is further pushed into E- and W-band, and mainly because all these classical approaches use series-connected transistors. This may severely affect the overall

performance of a SPDT switch operating beyond 60 GHz. The series-connected transistors not only add loss to the ON-state of a switch, but also cause capacitive feed through in the OFF-state of a switch [49] [21]. Most mm-wave switches use shunt-connected transistors only. A classical structure for symmetrical SPDT design operating beyond 60 GHz is given in Fig. 4.1(d) [20]. As illustrated, the shunt-connected transistors are used along with λ/4-wavelength TLs to provide high-impedance nodes. However, the drawback of only using shunt-connected transistors for SPDT switch design has been very well documented in the literature [56], which is the significantly constrained P1dB. According to the calculated data presented in [56], a 3.6-dBm transmitted RF signal could potentially turn on the OFF-state switching transistors implemented in standard 65-nm CMOS technology, although the actual value of P1dB is typically several decibels higher than this value. Thus, an innovative design approach is required to further enhance P1dB of the switch.

Since the limited P1dB is mainly constrained by active devices, it is worthwhile exploring a possible solution based on a passive-inspired approach [102] [58] [59] [60], which is the motivation for undertaking this work. An advantage of the passive-inspired approach is that: firstly, it might be directly transferred to designs implemented in either SiGe or SOI CMOS technologies; and secondly, it also can be used in conjunction with other techniques, such as negative control voltage, if it is required. Finally, as the passive-

inspired approach is based on passive structures, it can be “scaled” to different operation frequencies by changing the physical dimensions of the passive structures.

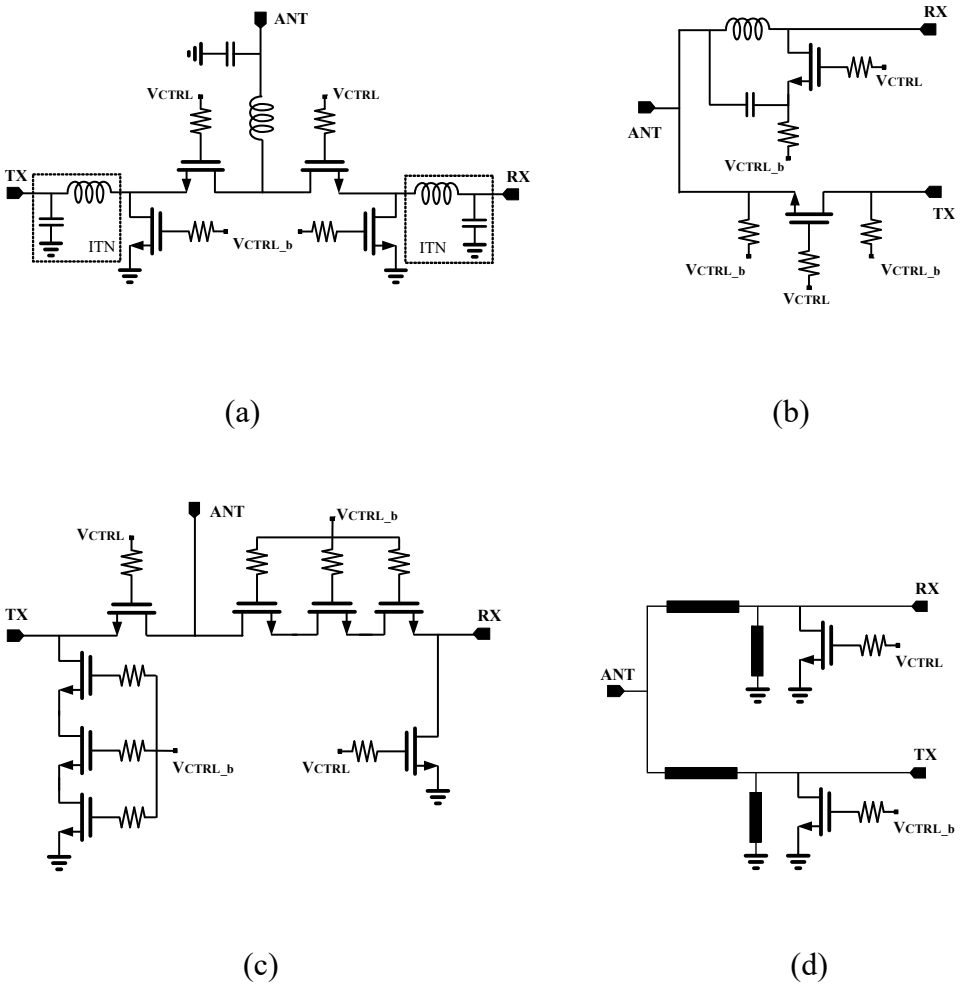


Figure 4.1: Overview of the classical SPDT switch structures in the literature, (a) impedance transformation network, (b) asymmetrical structure, (c) asymmetrical structure with stacked transistors and (d) symmetrical structure with “shunt-connected” switching transistors only.

4.4 Concept of the Proposed Asymmetrical SPDT Switch Using Passive Ring Structure

As discussed earlier, there are inherent trade-offs between P1dB and ISO/IL for symmetrical SPDT switch design. To enhance the P1dB of a switch without significantly deteriorating other design specifications, an asymmetrical structure has been presented in [39] [24]. Thus, this work is also focused on asymmetrical SPDT switch design. However, the design of an asymmetrical SPDT switch usually requires the use of series-connected switching transistors. As mentioned in section 4.3, there are issues with them at a very high frequency, such as 90 GHz. It is subsequently difficult to directly transfer the presented approach in [39] to a mm-wave SPDT switch design. To enable an asymmetrical design without using any series-connected transistors, an innovative passive structure is presented in this work. The simplified schematic is given in Fig. 4.2.

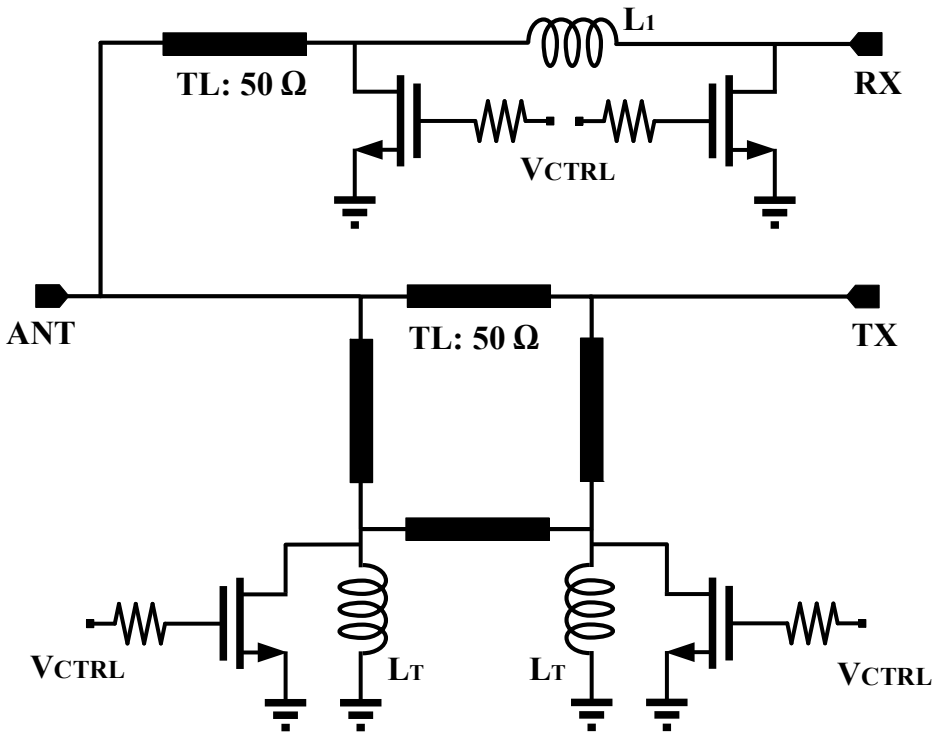


Figure 4.2: Schematic of the designed asymmetrical SPDT switch. Note: All TLs are quarter-wavelength TLs.

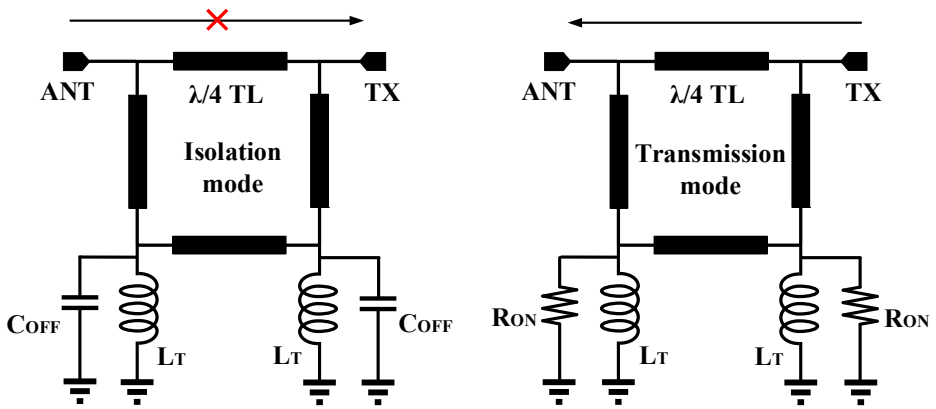
As can be seen, a classical double-shunted structure is used along with a λ/4-wavelength TL in RX branch [20] [103] [104, 105]. In theory, as the SPDT switch works in RX mode, the impedance looking into the TX port should be relatively high, so that the received RF signal at ANT port will not flow into TX branch. However, the impedance could be significantly lowered in practice due to parasitics of switching transistors and the limited Q-factor of the λ/4-wavelength TLs. Consequently, the IL of the SPDT in RX mode will deteriorate. Moreover, in this design, as the targeted P1dB is relatively high, sufficient ISO is required to ensure that the transmitted RF signal has minimized influence on RX

branch. To achieve this goal, the double-shunted transistors along with an inductor L1 are used to form a C-L-C network [20, 103, 104] [105]. As a result the ISO can be greatly enhanced.

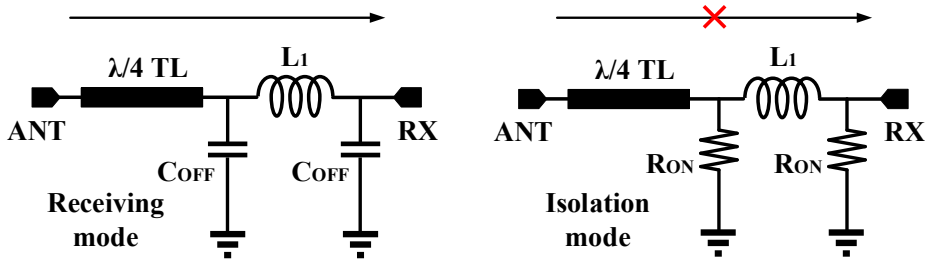
For the TX branch, it utilizes four λ/4-wavelength TLs to form a "ring resonator". Additionally, the tuning inductors LT are used along with the switching transistors. The parasitic capacitance (known as C_{OFF}) of the transistors together with LT form a shunt LC tank that provides the required high impedance nodes by looking into the ground. The size of switching transistors can be determined in a straightforward way using the approaches presented in [36, 37, 39, 40, 89]. Once the size is determined, the value of LT can be optimized accordingly to achieve a relatively high impedance at the designed frequency. Furthermore, in contrast to all conventional designs that required switching transistors to be turned OFF in TX mode, in this design, the switching transistors are turned ON in TX mode. Consequently, the fundamental design issue related to power-handling capability in terms of P1dB due to the reduced VTH is simply overcome.

To further elaborate the presented approach for SPDT switch design, the simplified circuit models for the classical and the proposed approaches are compared in Fig. 4.3. As illustrated in Fig. 4.3(a), the circuit model for RX branch is given. To transmit a RF signal from ANT port to RX port, the shunt-connected transistors must be turned off to create a high-impedance path between RX port and ground. Moreover, to improve ISO between

ANT and RX ports, the transistors must be turned on to create a low-impedance path to the ground. The drawback of this approach has been explained earlier. As the expected RF signal that appeared at ANT port is not strong enough (around 0 dBm for most cases), the shunt-connected transistors should be able to handle it without any problem. However, the situation would be different in TX mode. To avoid the power-handling issue completely, an opposite mechanism is used for TX branch, which is given in Fig. 4.3(b). In TX mode, the shunt-connected transistors are tuned on while in RX mode, they are turned off. As the transistors are turned on in TX mode, the power-handling capability of the switch could be significantly enhanced. On the other hand, the ISO between the ANT and TX ports of the presented design is realized by utilizing a signal canceling mechanism.



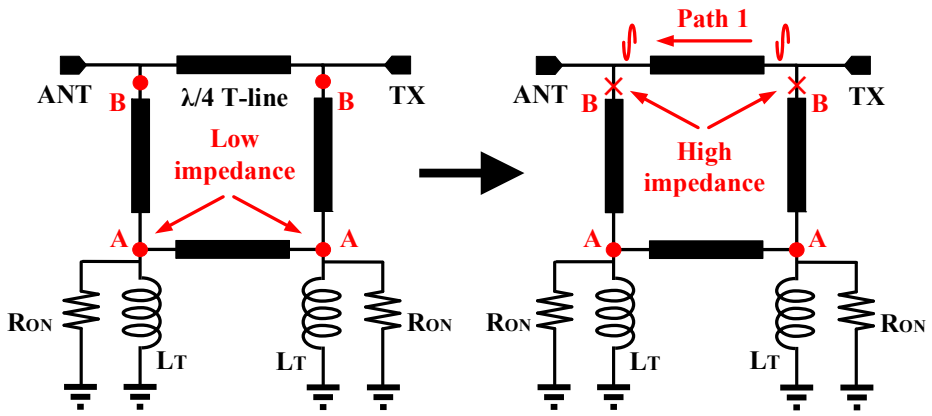
(a)



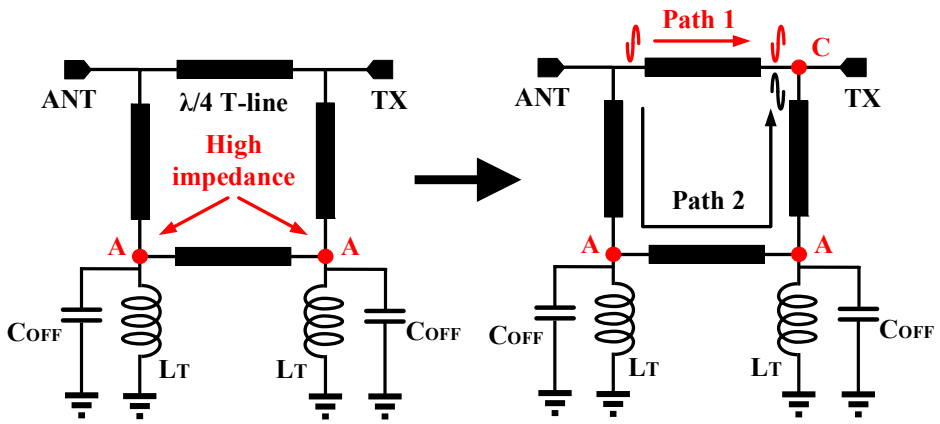
(b)

Figure 4.3: Operation principles of the proposed asymmetrical SPDT switch, (a) RX branch, and (b) TX branch

To further explore the insights made possibly the presented concept, the simplified operating mechanisms of this design are given in Fig. 4.4.



(a)



(b)

Figure 4.4: Simplified models for the TX branch of the asymmetrical SPDT switch in different operation modes, (a) transmission, and (b) isolation.

As shown in Fig. 4.4(a), the shunt transistors are turned on in TX mode. Thus, the impedance at the point A is relatively low and the impedance looking into point B is relatively high. As a result, the transmitted RF signal flows from TX port to ANT port through Path 1. On the other hand, as shown in Fig. 4.4(b), the isolation mode is realized, while the shunt transistors are turned off. In this case, the capacitor C_{OFF} along with the inductor LT form an LC-network, which presents a relatively high impedance at point A. As a result, two paths are created between the ANT and TX ports, namely Path 1 and Path 2, and their electrical lengths are λ/4 and 3λ/4, respectively. As a rule of thumb, the RF signals traveling through these two paths will have a 180° phase shift, while the signals are combined at point C, which results in a RF signal cancellation. This means that the RF signal cannot travel from the ANT to TX port. Indicated here is a good isolation. To

prove the concept is theoretically sound, a signal given in (1) is injected into the ANT port at isolation mode,

$$\mathrm{ANT_{SIG}} = \mathrm{A}\cos(\omega t + \theta_0) \quad (1)$$

where A, ω and θ0 are the amplitude, angular frequency, and phase of the injected signal, respectively. Then, the signal through the Path 1 and Path 2 can be expressed as,

$$\mathrm{ANT_{SIG\_path1}} = \mathrm{A_1}\cos(\omega t + \theta_0 - \frac{1}{4}\lambda \times \frac{2\pi}{\lambda}) \quad (2a)$$

$$\mathrm{ANT_{SIG\_path2}} = \mathrm{A_2}\cos(\omega t + \theta_0 - \frac{3}{4}\lambda \times \frac{2\pi}{\lambda}) \quad (2b)$$

By adding (2a) and (2b), the signal sensed at TX port is given in (3),

$$\mathrm{TX_{SIG}} = (\mathrm{A_1} - \mathrm{A_2})\sin(\omega t + \theta_0) \quad (3)$$

As can be seen from (3), if the magnitude of the signals that pass through two paths are exactly the same, they will cancel each other out completely. Consequently, there will be no signal leak through to the TX port. However, the parasitic effects due to the switching transistors and tuning inductance LT will trigger some additional phase shift, which deteriorates the switch's ISO. In effect it means that the signal from the Path 2 can be rewritten as,

$$\mathrm{ANT_{SIG\_path2}} = \mathrm{A_2}\cos\left(\omega t + \theta_0 - \frac{3}{4}\lambda \times \frac{2\pi}{\lambda} - \theta_{\mathrm{LC}}\right) \quad (4)$$

where the θLC is the phase delay due to the resulting parasitic LC tank. Substituting (4) into (3), the signal seen at TX port can be rearranged as,

$$TX'_{SIG} = A_1 \sin(\omega t + \theta_0) - A_2 \sin(\omega t + \theta_0 - \theta_{LC}) \quad (5)$$

The magnitude of TX'_{SIG} can be written as,

$$Mag = \sqrt{1 + (1-\alpha)^2 - 2(1-\alpha)\cos\theta_{LC}} \quad (6)$$

where α = (A1 – A2)/A1. After normalizing (6) with (2a), the normalized magnitude of TX'_{SIG} can be calculated and the results are plotted in Fig. 4.5. As stated already, the magnitude of TX'_{SIG} represents the isolation capability of the designed switch. As indicated in Fig. 4.5, the value of "Mag" of the designed switch is limited by two factors, these being α and θ_{LC}. The variable α indicates different insertion losses through the two different paths and the variable θ_{LC} represents additional phase induced by the LC tank. By carefully selecting the values of transistor and LT, an optimized ISO can be created.

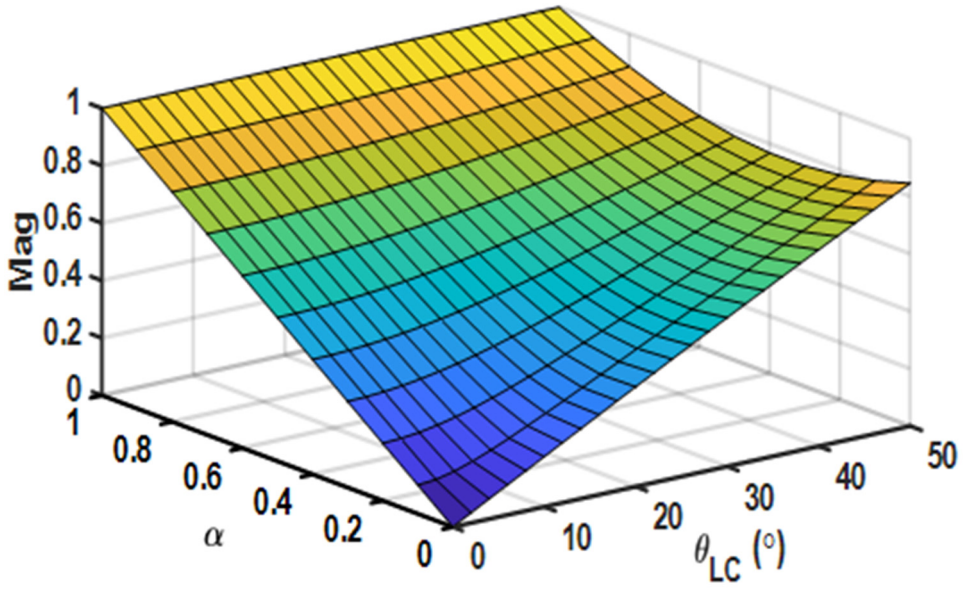


Figure 4.5: Simulated adverse impact on ISO of the designed SPDT switch due to magnitude and phase errors through two paths.

It is noted that an approach presented in [106] also uses the concept of ring resonator for SPDT switch design, which is implemented using discrete components and operates at a relatively low frequency. It should be noted the principle behind that design is quite different from the one presented here. The ring resonator used in this work will improve not only P1dB but also isolation. Contrasting this, the one presented in [106] does not indicate such an improvement. Furthermore, the design shown in [106] utilizes multiple ring resonators that could have a severe impact on insertion loss, if it is implemented on the lossy silicon substrate. Finally, it is important to mention here again that the ring-resonator-based structure is necessary for this design. Although using two λ/4-TLs (instead of using four λ/4-TLs to build the ring resonator) could also improve P1dB of a switch, it has limited isolation capability due to the signal-canceling mechanism. Based

on our simulation, the obtained ISO is only around 10 dB across the interested frequency band.

4.5 Design and Implementation of the Presented Asymmetrical SPDT Switch

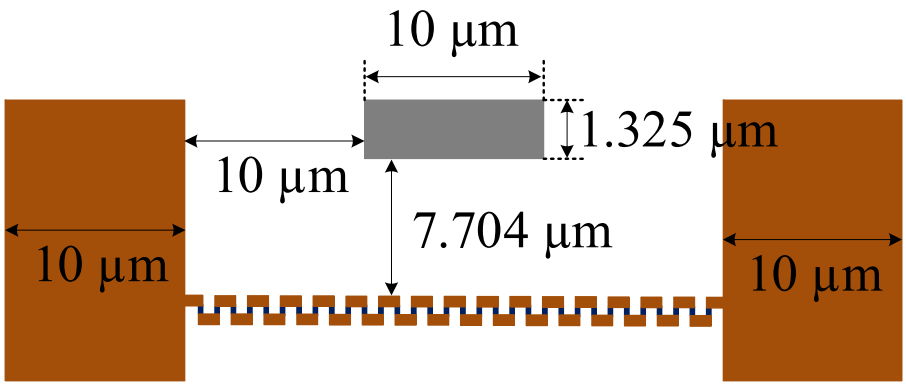


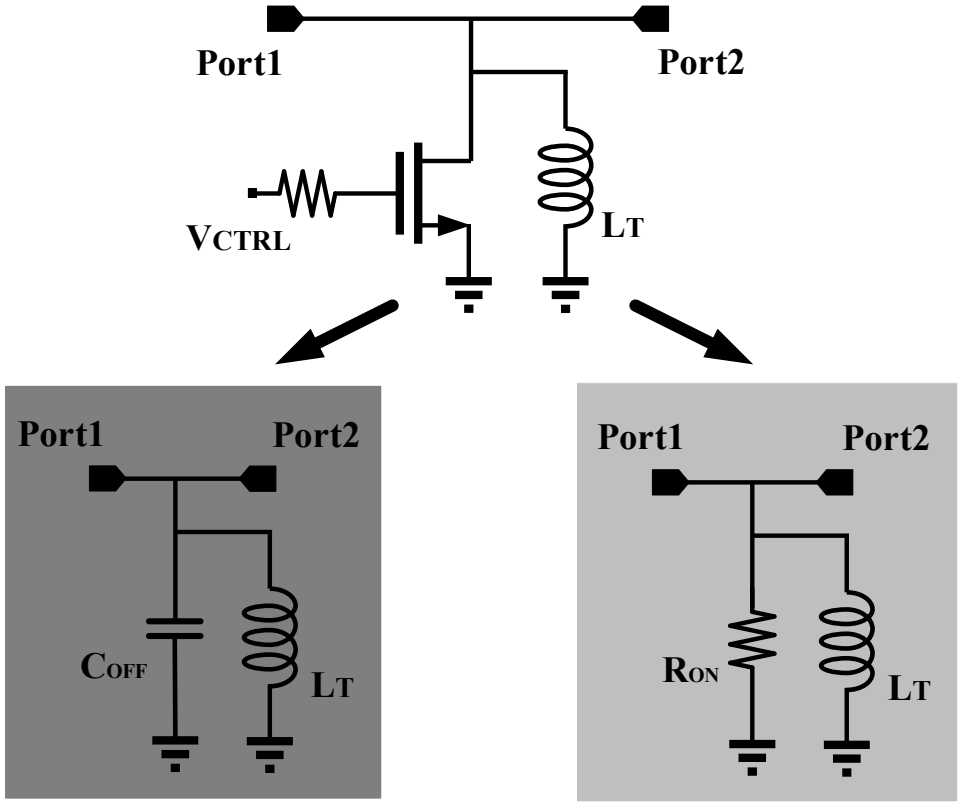
Figure 4.6: Cross-section view of the implemented TL with physical dimensions. Note: The insertion loss in electromagnetic (EM) simulation is approximately 0.5 dB at 90 GHz for a λ/4-TL.

To verify if the proposed passive-inspired concept for SPDT design is feasible in practice, a standard 55-nm bulk CMOS technology is chosen for this work. This technology provides not only high-performance nFET with ft of 200 GHz, but also 8 metal layers with aluminum as the top thick-metal layer. As shown in Figs. 4.3 and 4.4, TLs are extensively used for the design. The cross-section view of the TL used in this design is given in Fig. 4.6. As can be seen, metal walls are constructed by stacking all metal layers and used for all TLs to avoid any unnecessary coupling. The TL is constructed using the topmost metal layer, which has a thickness of 1.325 μm, while the ground plane is implemented using a combination of M2 and M3, and M1 is reserved for DC only. The width of the signal path and the gap are both 10 μm for the 50-Ω TL. Additionally, the height of the silicon substrate is 737 μm. The relative dielectric constant of SiO_2 is 4.1.

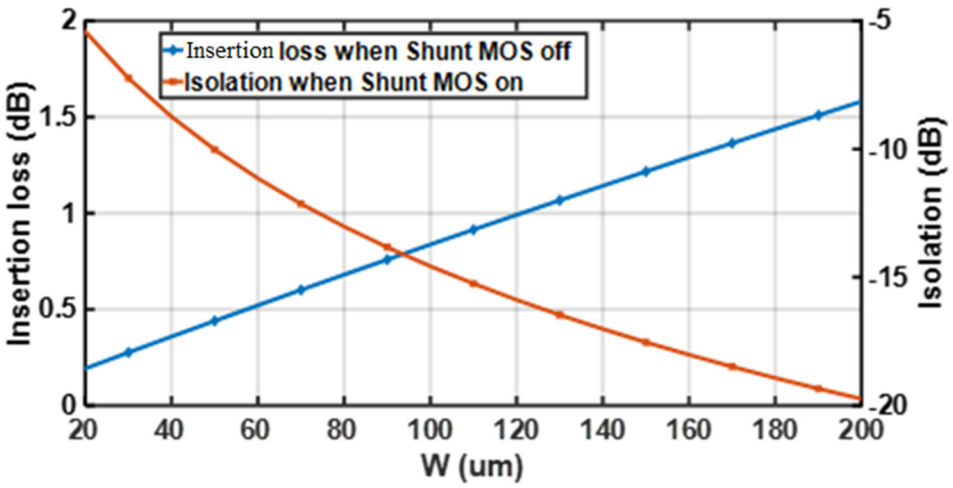
As noted in the previous section, the tuning inductor LT and C_{OFF} form an LC tank, which plays a critical role in TX branch design. Therefore, the size of the switching transistor needs to be carefully co-designed with the value of LT. A simple 2-port network is used to evaluate the characteristics of the LC tank. The schematic is given in Fig. 4.7(a). The simulated results as a function of the width of the switching transistor are plotted in Fig. 4.7(b). Two design specifications, specifically IL and ISO, are deemed to be benchmarks for performance evaluation here. It is noted that the presented IL and ISO here are mainly used to reflect the variations of the LC tank impedance, which are different from the IL and ISO used for a switch. In order to simplify the design procedure, an ideal lumped inductor with a Q-factor of 10 is used for the tuning inductor at the initial design phase. Utilizing the simulation tools, the ISO (when switching transistor is off) and IL (when switching transistor is on) of the LC tank can be directly calculated and the value of the tuning inductor can be determined.

Based on the obtained simulation results, a good trade-off between IL and ISO is achieved, while the width of the switching transistor is retained at 100 μm (20 fingers are used). The value of LT is selected to be 90 pH and implemented using a straight metal line. The inductor LT along with the switching MOSFET forms a MOS-inductor LC tank. Based on the EM simulation, it provides 230 Ω and 12 Ω when MOS nFETs switch off and switch on, respectively. For RX branch design, the same sizes are used for the double-

shunted transistors. The value of L1 is determined to be 120 pH and it is implemented using a folded metal line.



(a)



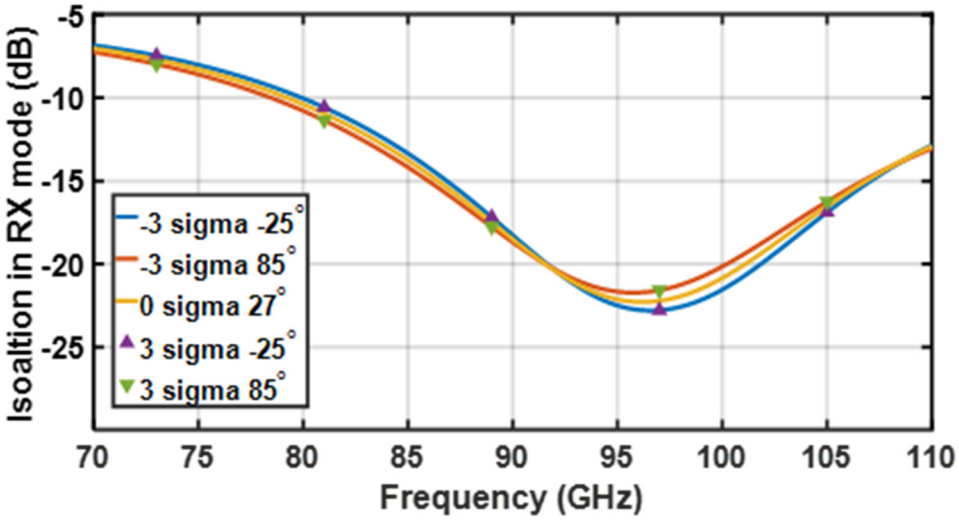
(b)

Figure 4.7: Evaluation of the impedance variations of the LC tank using a 2-port network, (a) test bench, and (b) simulation results with different switching transistor widths.

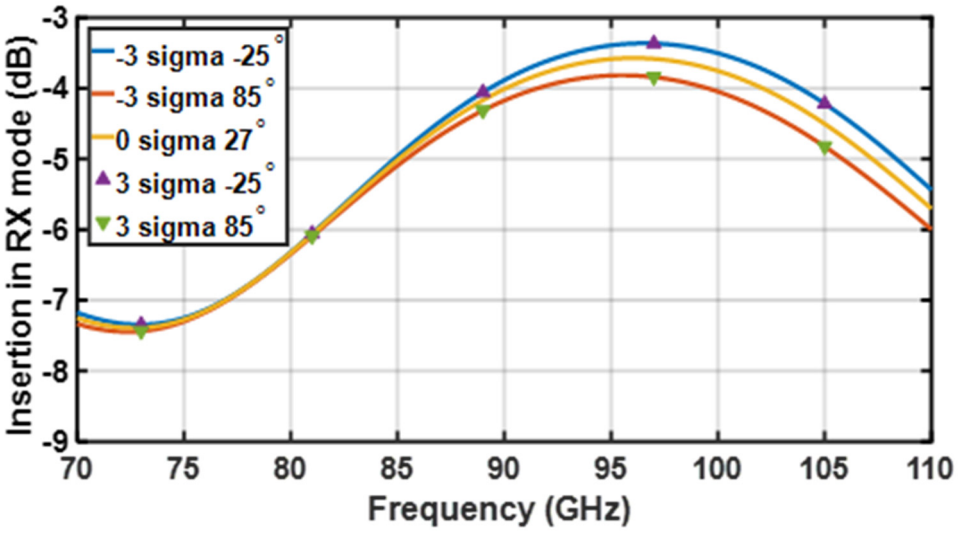
On the other hand, considering the balance between switching speed and isolation loss has been carefully discussed in [56]. In this design, it should be noted that the switching transistors are turned on in TX mode, so the insertion loss is insensitive to the gate resistance. Selecting the gate resistance value is mainly considered for switching time and Insertion Loss of the RX branch. A 10-kΩ resistor provides the best possible solution for this design.

Finally, to further demonstrate the presented ring structure is useful for switch design in practice, the impact on frequency responses due to process and temperature variations are taken into consideration, including ±3 Sigma for process variations with a temperature varied from -25 °C to 85°C. The simulated results are given in Fig. 4.8. It observed that

there is only marginal performance variation, and this tends to confirm the good reliability of the proposed design approach. It is noted that the simulations are only conducted in RX mode because the performance of the designed SPDT switch in this mode is reflected by the presented ring structure used at TX branch.



(a)



(b)

Figure 4.8: Simulated frequency responses in of the asymmetrical SPDT switch in RX mode, (a) ISO, and (b) IL

4.6 Measurement Results and Discussion

To evaluate the performance of the presented asymmetrical SPDT switch, a prototype is fabricated. The die microphotograph is shown in Fig. 4.9. Excluding the testing pads, the die size is only 0.26 × 0.98 mm^2. The measurement was conducted using on-wafer G-S-G probing up to 110 GHz by means of a vector network analyzer N5290A manufactured by Keysight™ and 100-µm pitch (GSG) Infinity Probes with 1-mm connectors provided by FormFactor™. The on-wafer calibration was created utilizing a conventional short-load-open-thru (SLOT) to move the reference plane from the connectors of the equipment to the tips of the RF probes. For comparison purposes, both the EM simulated and measured S-parameters are given.

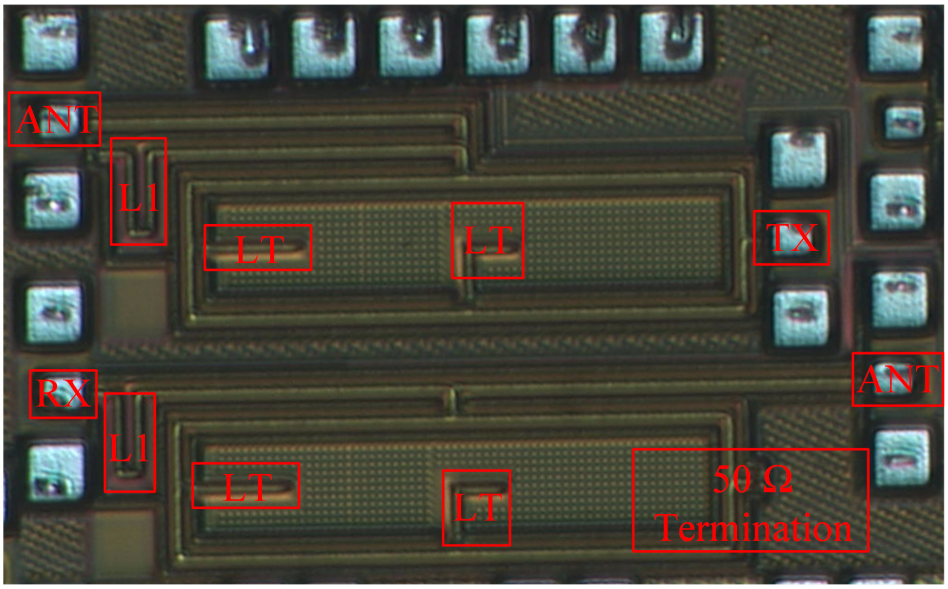
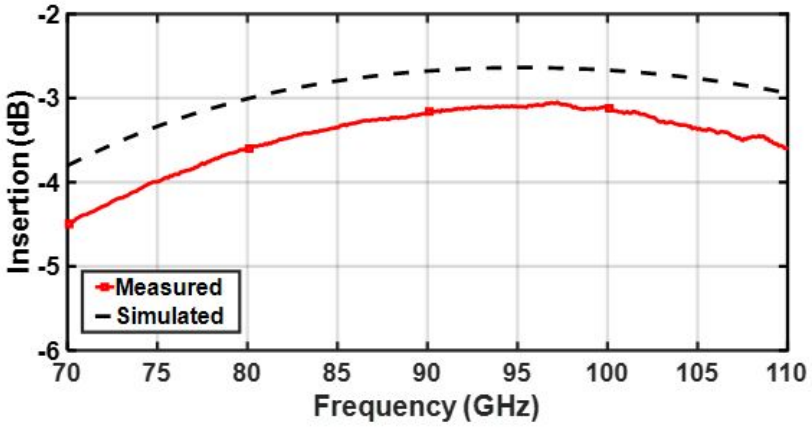


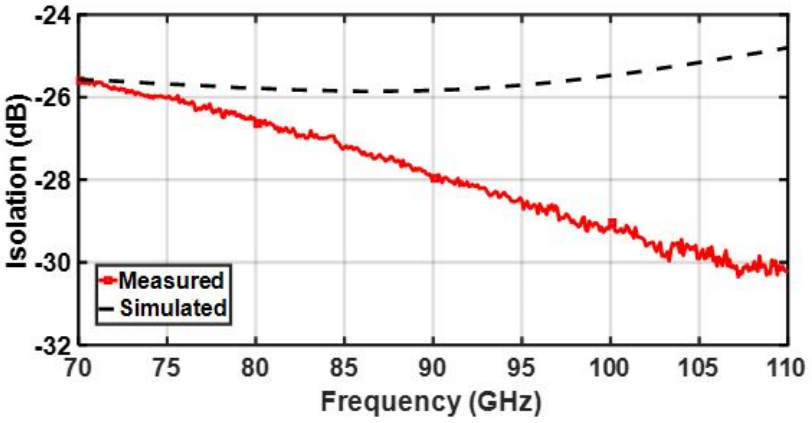
Figure 4.9: Die microphotograph of the designed SPDT switch.

Since the designed SPDT switch is asymmetrical, two different prototypes are fabricated in which RX and TX ports are terminated with a 50-Ω load, respectively. A result of this is that the performance can be evaluated using the standard test bench used for symmetrical SPDT switch characterization. Unlike the conventional design that requires two separated control voltages, i.e. V_{CTRL} and V_{CTRL_B}, a single voltage source is sufficient to control this design. To turn the switch into a TX mode, the TX branch needs to allow a RF signal to be delivered from TX port to ANT port. Meanwhile, the RX branch needs to provide an isolation between the ANT port and RX port. To do so, the control voltage $V_{CTRL} = 0$ is applied. The frequency responses of the switch working in TX mode are shown in Fig. 4.10. As can be seen, at 90 GHz, the IL and ISO of this design are 3.2

dB and 28 dB, respectively. Both the input and output impedance matching are better than 10 dB.



(a)



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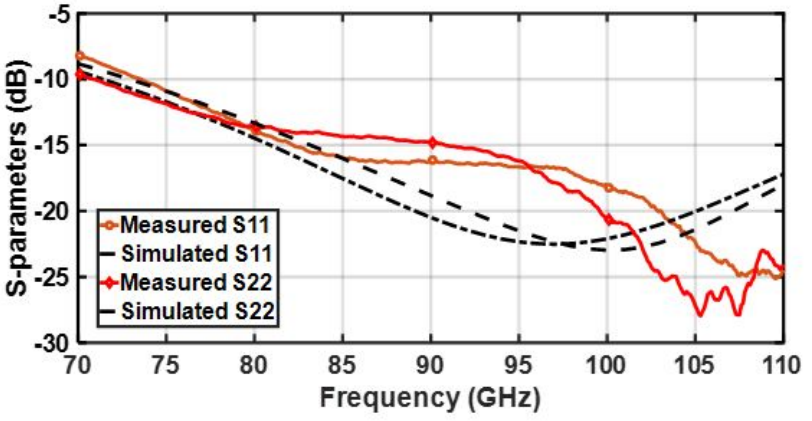
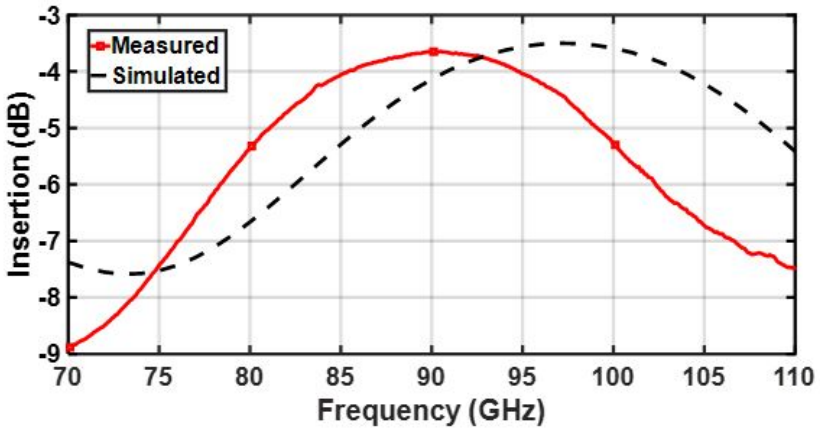


(c)

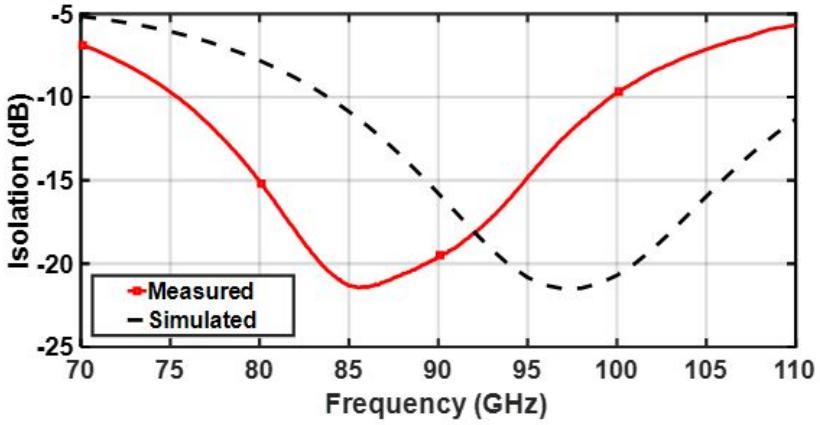
Figure 4.10: Measured frequency responses of the designed SPDT switch in TX mode, (a) IL, (b) ISO and (c) input and output impedance matching. Note: IL is measured between TX and ANT ports, ISO is measured between RX and ANT ports only.

To evaluate the performance of the switch in RX mode, the control voltage V_{CTRL}=1.2 V is applied. This procedure for the TX branch provides isolation between ANT port and TX port. Meanwhile, the RX branch enables the RF signal to pass through from ANT port to RX port. The measured frequency responses are depicted in Fig. 4.11. As illustrated, the IL and ISO are 3.6 dB and 20 dB at 90 GHz, respectively. Both the input and output matching are better than 15 dB. What is noted here is a better frequency shift between the measured and simulated results. This shift is likely to be caused by the fact that the values of the parasitic capacitance of nMOSFETs and LT are under-estimated in EM simulation.

It can also be found that there are some differences between the measurement and simulation results at the higher frequency band in Fig 4.11 (b). The main reason that causes the discrepancy between measurement and simulation is that the vertical interconnection between drain terminal and top metal layer is underestimated in EM simulation. Such parasitic inductance has an impact on impedance looking into the switching FET. Thus, the notch frequency is shifted to a lower frequency at the measurement. However, this imperfection does not affect the primary function of the designed switch. In particular, the achieved P1dB is still enhanced as expected.



(a)



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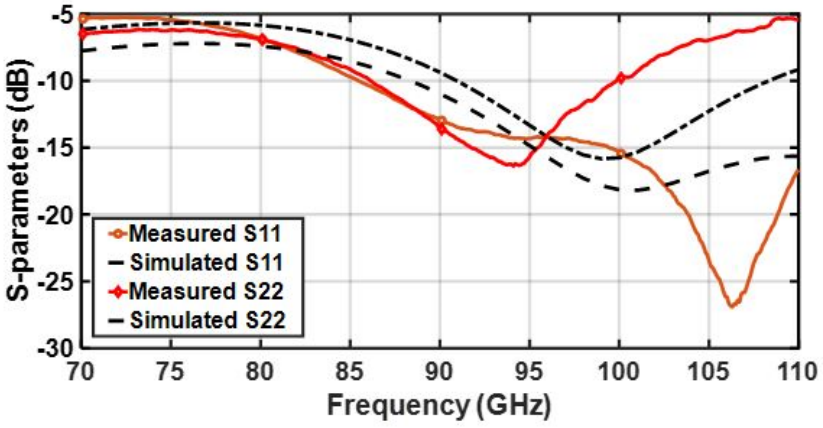


(c)

Figure 4.11: Measured frequency responses of the designed asymmetrical SPDT switch in RX mode, (a) IL, (b) ISO and (c) input and output impedance matching. Note: IL is measured between RX and ANT ports, ISO is measured between TX and ANT ports only.

Due to the equipment limitation, the P1dB can only be evaluated at 87 GHz. The initial power was calculated by using the set-up shown in Fig. 4.12. As can be seen at the input side of the test bench, a signal generator E8257D from Keysight™ serves to generate a low-frequency signal, which is then fed into a frequency extension module WR12SGX from Virginia Diode (VDITM). The WR12SGX is an E-band source module that could provide up to 16 dBm output power at 87 GHz. The signal source is then connected to a 0-30 dB adjustable attenuator along with a 78-87 GHz PA module. Both the attenuator and PA modules are sourced from SAGE™. The PA module features a saturated output power of 25 dBm at 87 GHz. To monitor the input power level injected into the designed SPDT switches, a coupler with 30 dB coupling coefficient is used along with a U8489A power sensor from Keysight™. At the output side of the test bench, a 10-dB fixed attenuator is used along with the PM5B power meter from VDITM. Both the input and output power levels were calibrated. The measured P1dB and the IL as a function of input power for this design are shown in Fig. 4.13. As can be seen, the measured power-handling capability is truly remarkable, no obvious gain compression is observed, when a 19.5 dBm input power is injected into the TX port of the switch.

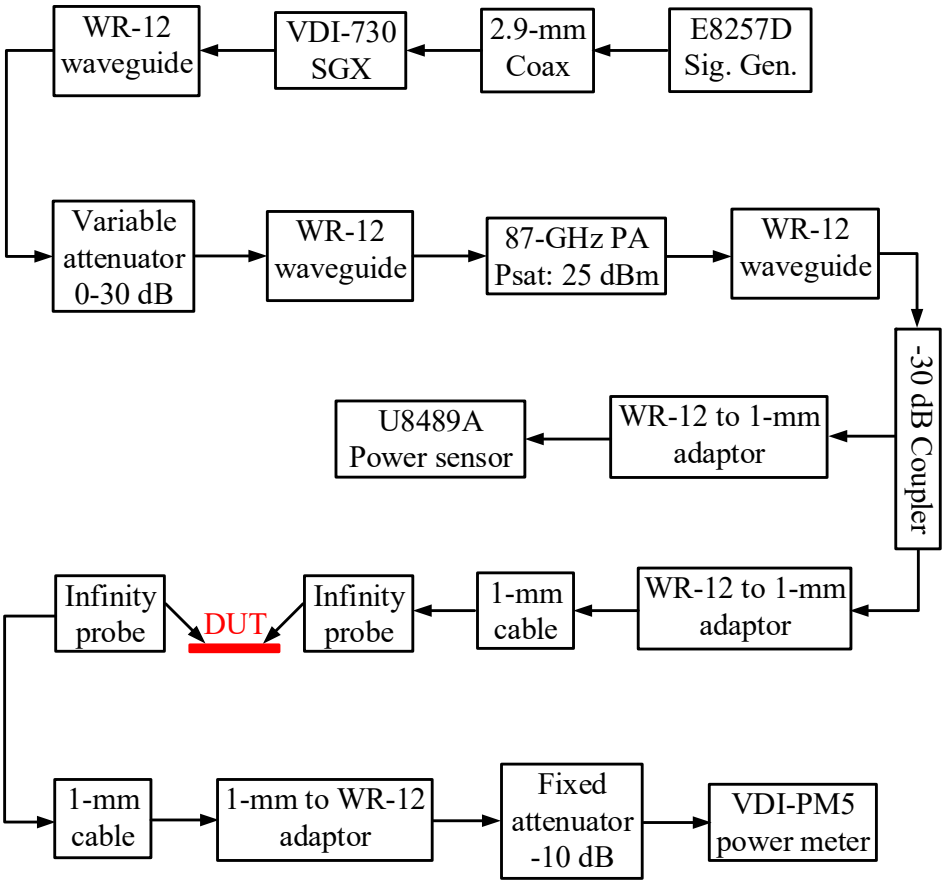


Figure 4.12: The test bench used for P1dB measurements.

The performance summary of the presented asymmetrical SPDT switch is given in Table 1 and also compared with other state-of-the-art designs. By observing the summarized data from different designs, some interesting results can be found. Firstly, as shown in the table, for the bulk CMOS switches operating beyond 90 GHz, it seems to have an IL around 3.5 dB. Meanwhile the SiGe switches offer very competitive overall performance at W-band, especially IL, even when compared to the designs using more advanced III/V technologies, such as the ones presented in [32]. The downside of SiGe-based solutions is the relatively high-power consumption compared with their counterparts in CMOS technology. This may turn out to be critical when enabling them for power-constrained consumer electronics.

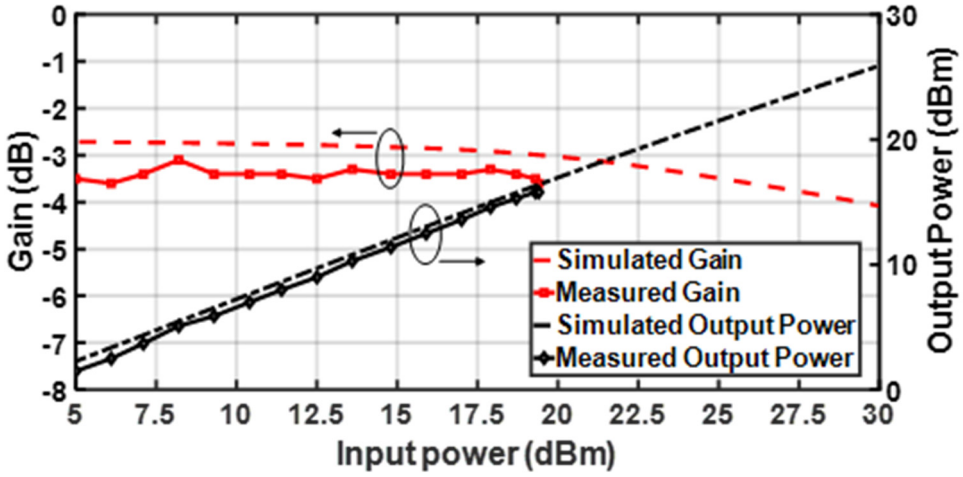


Figure 4.13: The measured P1dB of the designed switch.

Secondly, the obtained P1dB of the different mm-wave CMOS-based designs seem to be quite similar regardless of operating frequency. As shown in [23] and [91], both designs

are implemented in 65-nm CMOS technology. Although the operating frequency is different, the P1dB for both designs are limited to be approximately 10 dBm, which indicates that the limiting factor for P1dB is not the operation frequency. One of the possible ways to improve P1dB is to select a technology node with a relatively higher threshold voltage. As demonstrated in [20], the P1dB may be improved by approximately 3 dB. However, other mm-wave circuits such as amplifiers have to be implemented using reduced threshold voltage for an enhanced performance. There is a fundamental contradictory choice to be made for mm-wave RF front-end design. As shown in [21, 103], the P1dB of a SPDT switch implemented in 45-nm SOI CMOS is further reduced to approx. 8 dBm. As can be seen from Table 4, using the approach presented here, the power-handling capability in terms of P1dB can be improved to a remarkable level, more than 20 dBm. To the best of our knowledge, this is the only silicon-based mm-wave SPDT switch, including those in SiGe and SOI technologies, that achieves a P1dB of more than 20 dBm. This is done without using any special physical treatment, such as high-VTH devices and negative bias voltages, which usually either increase fabrication cost or design complexity.

REF.	f_c (GHz)	Insertion loss (dB)	Isolation (dB)	P1dB (dBm)	Power consumption (mW)	Area (mm^2)	Tech. (nm)	Circuit structure
[89]	DC-43	3	50	19.6	0.0	0.0058	45 SOI	RF signal cancellation
[21]	DC-60	2.5	23	7	0.0	0.04	45 SOI	Series-shunt-connected FETs
[20]	50-70	1.5	25	13.5	0.0	0.28	90 CMOS	λ/4-TL with shunt-connected FETs
[24]	50-67	1.9	20	10	0.0	0.6	90 CMOS	λ/4-TL with shunt-connected FETs
[23]	58-85	1.8	22	10	0.0	0.015	65 CMOS	Transformer with shunt-connected FETs
[46]	50-94	3.3	27	15	0.0	0.24	90 CMOS	Travelling wave with shunt-connected FETs
[104]	60-110	3-4	25	10.5	0.0	0.3	90 CMOS	λ/4-TL with shunt-connected FETs
[56]	73-110	1.1	22	17	5.9	0.213	90 SiGe	λ/4-TL with shunt-connected FETs
[105]	75-110	4.5	48	11	0.0	0.33	90 CMOS	Leakage cancelation
[32]	77-120	1.8	20	19	0.0	0.75	50 GaAs HEMT	λ/4-TL with shunt-connected FETs
[55]	77-110	1.4	19.3	19	8	0.14	90 SiGe	λ/4-TL with shunt-connected FETs
[46]	92-98	2	20	n/a	4.8	n/a	130 InP HBT	λ/4-TL with shunt-connected FETs
[107]	94-110	4.2	25	n/a	0.0	n/a	65 CMOS	λ/4-TL with shunt-connected FETs
[91]	130-180	3.3	23.7	11.5*	0.0	0.0035	65 CMOS	Artificial resonator with shunt-connected FETs
[103]	140-220	3	20	8	0.0	0.29	45 SOI	λ/4-TL with shunt-connected FETs
THIS WORK	**85-95**	**3.2 (TX) 3.6 (RX)**	**>25 (TX) >20 (RX)**	**>19.5^ (TX)**	**0.0**	**0.26**	**55 CMOS**	**Ring resonator with shunt-connected FETs**

Table 4: Comparison of the presented switches with some other designs described in various studies.

Note: * simulation results only, ^ due to the output power limitation of the PA module.

Finally, since the presented design approach is based purely on a passive-inspired concept, it also offers other advantages. The idea presented in this work can be effectively used along with high-VTH devices and negative bias voltage, eventually enabling Watt-level silicon-based switch at the mm-wave region. As well, since TLs are used for the implementation of ring resonator to improve ISO of the designed switch, the presented idea can be used for different operation frequencies. Doing so depends on the implemented TLs having reasonable physical dimensions for on-chip implementation and the insertion losses are relatively low.

4.7 Conclusion

A novel approach for mm-wave SPDT switch design with enhanced power-handling capability, especially P1dB, has been presented in this work. The presented approach is based on asymmetrical architecture. A passive ring structure enables the use of ON-state switching transistors at TX mode, which results in a significantly enhanced P1dB. To prove the feasibility of using this approach for SPDT switch design, a prototype is fabricated in a standard 55-nm bulk CMOS technology. According to the measured results, the presented design can effectively enhance P1dB without compromising other performance aspects. It can be strongly concluded here that the presented novel concept is effective for switch designs using shunt-connected transistors. It overcomes the fundamental limitation on P1dB of silicon-based SPDT switch due to active device scaling.

Chapter 5: Design of Wideband Balanced Power Amplifier Using Edge-Coupled Quadrature Couplers in 0.13-μm SiGe HBT Technology

5.1 Abstract

In this work, a wideband millimeter-wave (mm-Wave) power amplifier (PA) is designed. To ensure the designed PA has sufficient output power, good power-added efficiency (PAE), superior input and output impedance matching across broadband, a balanced amplifier (BA) architecture is used. In particular, edge-coupled quadrature couplers are designed and their performance about magnitude error and phase error is minimized through a relatively wide bandwidth. A prototype PA is fabricated in a 0.13-μm SiGe HBT technology. Supplied by 5V power, the PA can provide more than 15 dBm saturated output power between 85-100 GHz that is equivalent to more than 16% fractional bandwidth. The peak PAE is better than 14% within this frequency range. The overall physical dimension of the designed PA is very compact. Including all pads, it is only 0.6 mm × 0.9 mm.

5.2 Introduction

Several interesting circuit design techniques, including both passive and active components, have been investigated in much detail during the last decade [59, 61-68, 108]. As reported in the previous section the operating frequencies have been pushed from 20+ GHz well to 85+ GHz. This has led to more challenges emerging mainly because the full potential of active devices, namely transistors, are approaching the end of their functioning lives. As the transit frequency (namely ft) of the state-of-the-art Heterojunction Bipolar Transistor (HBT) is approximately 300 GHz, the designed active components, especially the ones used in RF front-end, such as amplifiers, have to operate around one-third of the device's transmit frequency. Consequently, their performance could be significantly limited.

Among different building blocks in the RF front-end, there is no doubt that the power amplifier (PA) is one of the most indispensable components. The design of a high-performance PA will encounter several design trade-offs. The most critical design specifications are output power, linearity, efficiency, and stability. As moving into sub-THz, the modelling accuracy of passive components and parasitic elements of active devices becomes extremely critical. Any undesired modelling errors would cause two things: a severe frequency shift and an impedance mismatch. For the worst-case scenario, the impedance mismatch would result in a stability issue. This is particularly true for mm-

wave PA design, as the output impedance of the PA is not usually very well matched to a standard 50-ohm load under large-signal conditions.

Another design issue related to PAs operating at sub-THz is that their output power is relatively low. Since the standard 2-way power combining technique may not seem to provide reasonable performance at sub-THz, a more sophisticated output power combining network, as known as 4-way power combining, will be presented. In this work, a wideband PA operating at W-band will be described. Compared with previous research, the design presented here uses a wideband edge-coupled quadrature coupler, thus a wideband frequency response is obtained.

5.3 Design of Wide-Band Balanced Amplifier

5.3.1 Overview of the System Architecture

As far as the power-combining network is concerned, most of the previously published research utilizes either power combiner or balun; only a few studies use quadrature coupler. In contrast to these classical approaches, the BA architecture has some distinguished advantages, such as superior input/output impedance matching across a wide bandwidth, and load variation insensitivity [62, 75, 76]. The load variation insensitivity is very critical for the phased-array-based system, because the load conditions are unpredicted and varied in such a system, depending on the controlled beams.

The system architecture used in this work is shown in Fig. 5.1. As it can found in the figure, the designed PA contains three parts - an input coupler, two power cells and an output coupler. The input signal is split firstly into two paths by the input coupler with an equal power splitting ratio. In theory, the phase difference between these two paths is 90°. These two signals are then amplified by the two differential power cells and finally combined by the output coupler (that is identical with the input coupler) with a reversed 90° phase shift. Moreover, the isolation ports of both couplers are terminated by on-chip 50-Ω resistors. Using this architecture, any reflected energy due to load condition

variations will be absorbed by the terminated 50-Ω resistors that are connected to the isolation port of the couplers.

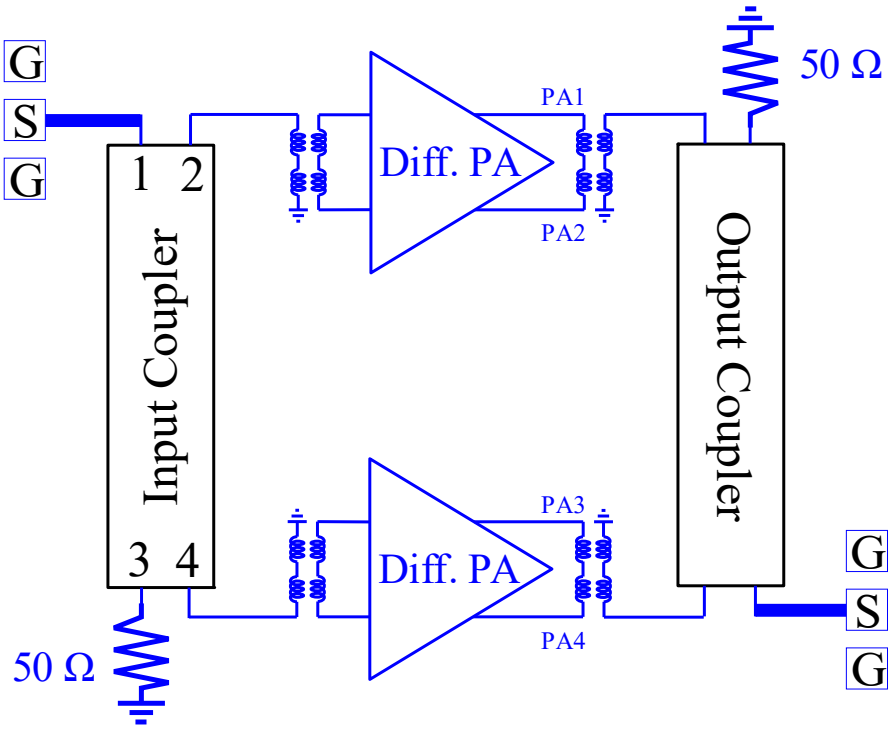


Figure 5.1: Simplified block diagram of the designed PA using BA architecture

5.3.2 Design Considerations for Quadrature Couplers

As far as quadrature coupler design is concerned, both branch-line- and coupled-line-based structures could be used. The branch-line-based structure performs better in terms of isolation. Moreover, the layout of such a coupler is potentially suitable for BA design since both the coupled and through ports are located at the same side of the coupler that makes interconnection between power cell and coupler relatively simple [75, 76, 109-111]. However, a single-stage branch-line coupler is inherently narrowband. To achieve a wider bandwidth, it needs to cascade at least two stages, which results in a relatively large die area. Thus, a coupled-line-based structure is selected in this design.

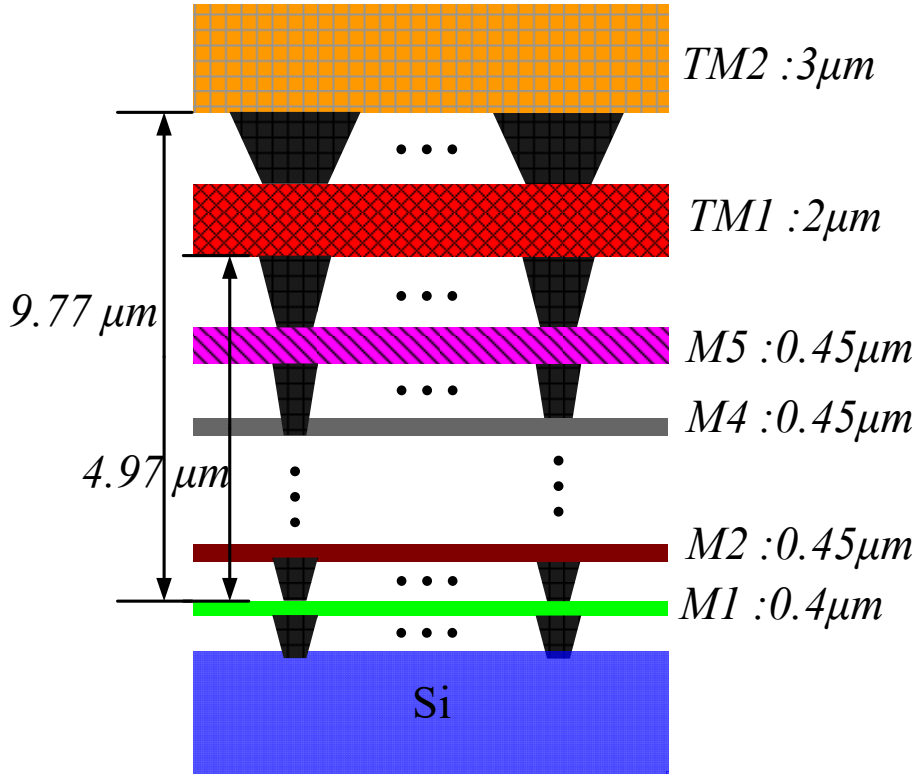
The coupled-line-based structure is potentially suitable for wideband quadrature coupler design. This is particularly true for on-chip implementation as multiple metal layers are provided in modern silicon technology. These have been extensively studied in the literature [111]. Most research focused on broadside-coupled ones due to their strong coupling between two metal lines. Additionally, the broadside-coupled structure enables interconnection between power cells and quadrature coupler much easier compared with the edge-coupled ones. Not much has been published on the edge-coupled structure to date so an in-depth investigation of this structure must be conducted. As can be seen from Fig. 5.2, the designed quadrature coupler is shown. Unlike the conventional edge-coupled structure, a cross-over is applied in this design along with two additional metal-oxide-

metal (MOM) capacitors for performance compensation. The top-most metal layer, namely TM2, is used to implement the two coupled lines and TM1 is also used for the cross-over. To understand what this design is attempting to do, a simplified lumped-element model is presented in Fig. 5.2. The capacitors C1 are mainly used to represent capacitive coupling between two coupled lines and capacitors C2 are used to model the parasitic capacitance between metal lines and ground shielding. Furthermore, the capacitors C3 are used to represent not only the parasitic capacitance but also additional capacitance used for getting the best possible performance in terms of magnitude error of the designed quadrature coupler.

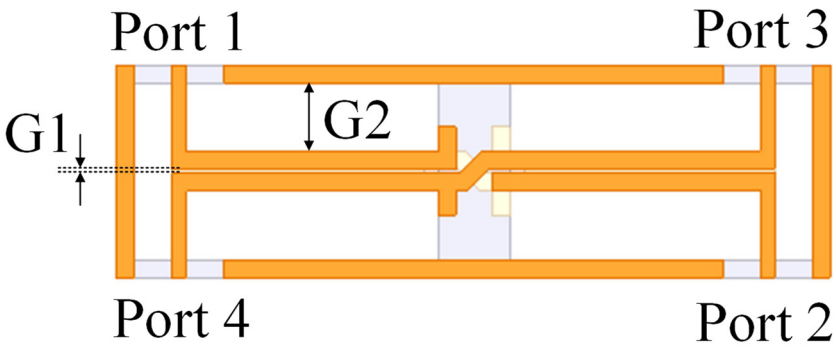
To verify the simplified circuit model is accurate for modeling, parametric studies are also given by using electromagnetic (EM) tools. As illustrated in Fig. 5.2(b), the two gaps, namely G1 and G2 are very critical for the presented edge-coupled quadrature coupler design. The value of G2 indicates the coupling between metal lines and the ground shielding, while the value of G1 represents the coupling between two metal lines. As can be seen from Fig. 5.3(a), the value of G1 is swept from 2 μm to 2.4 μm with a step of 0.2 μm. The 2-μm gap between the top-most metal layers is the minimum allowed value in this process. As illustrated, the phase difference of the coupler is less sensitive than the magnitude difference, while the gap between two edge-coupled metal lines is enlarged. Within a 0.5-dB magnitude difference, the coupler could cover a broad bandwidth from

approx. 75 GHz to 120 GHz, while a 2-μm gap is used. When the gap is enlarged, the bandwidth becomes increasingly narrow. It should be noted that a 0.5-dB magnitude difference confirms the fact that the coupling between the two metal lines is not strong enough.

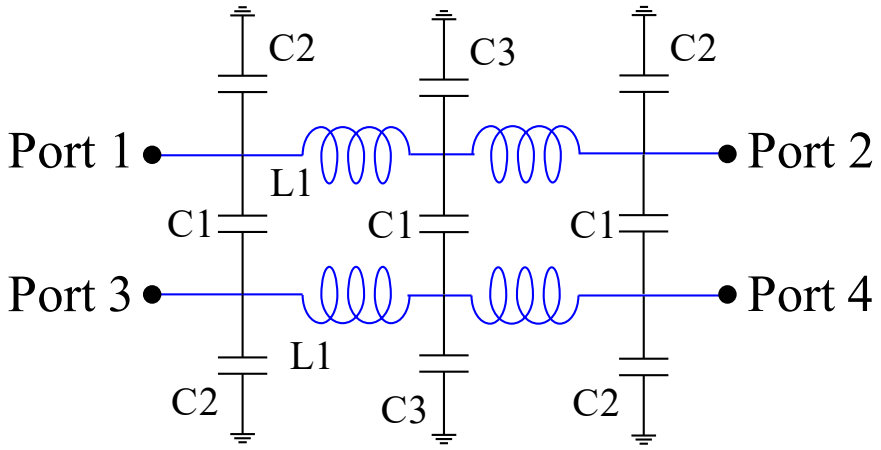
Another critical design parameter is G2 and the impact on phase and magnitude difference of the quadrature coupler due to using different values is given in Fig. 5.3(b). As can be seen, it is desirable to keep the ground shielding away from the coupled metal lines so that the magnitude difference could be minimized. However, there is a design trade-off between phase and magnitude difference. Enlarging the value of G2 could reduce the grounded parasitic capacitance, which has an adverse impact on phase difference that could be observed in Fig. 5.3(b). Additionally, from a device miniaturization point of view, it is also desirable to keep the value of G2 as small as possible.


TM2 :3μm
TM1 :2μm
9.77 μm
M5 :0.45μm
M4 :0.45μm
4.97 μm
M2 :0.45μm
M1 :0.4μm
Si

(a)

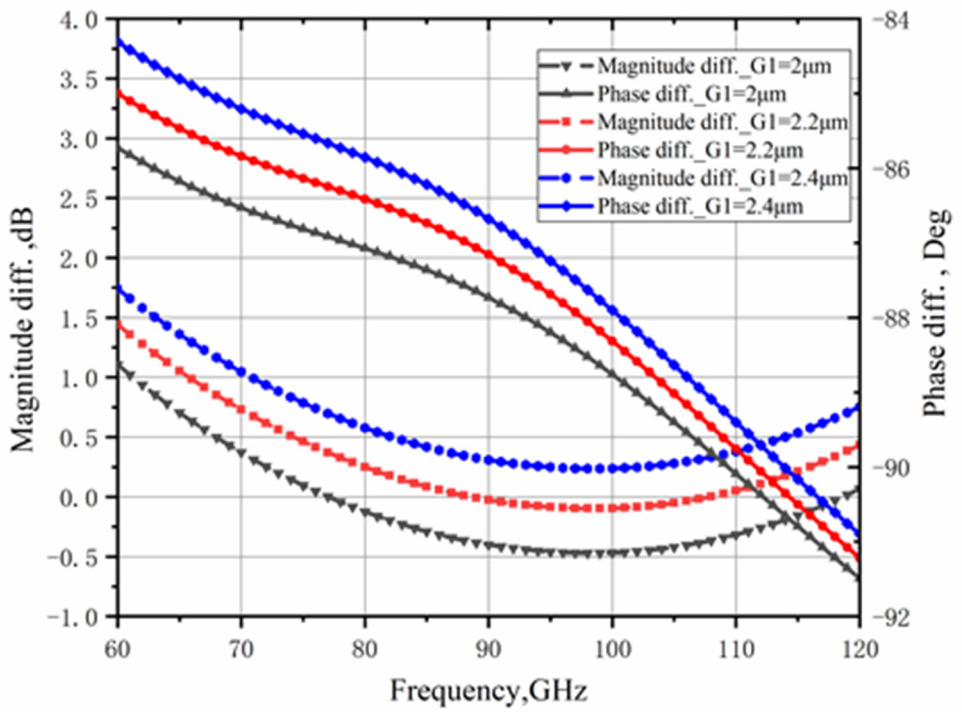

Port 1
Port 3
G1
G2
Port 4
Port 2

(b)

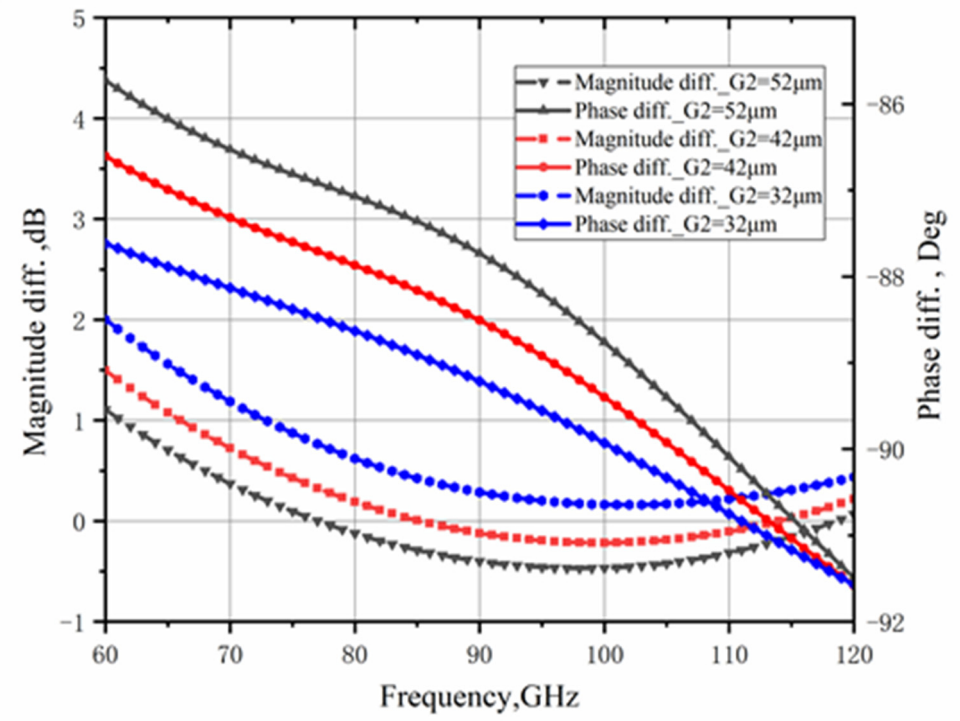


(c)

Figure 5.2: The designed quadrature coupler using edge-coupled structure, (a) simplified metal stack-up used in this work, (b) top-view the designed quadrature coupler, (c) simplified lumped-element model for analysis. Note: the width of the metal strip is 10 µm and the gap between them is 2 µm. The values for C1, C2, C3, L1 and coupling factor K for the coupled inductors are, 14 fF, 5fF, 7 fF, 97 pH and 0.75, respectively.



(a)



(b)

Figure 5.3: Parametric studies for the designed edge-coupled quadrature coupler, (a) different values of G1, (b) different values of G2

5.3.3 Design Considerations for Differential Power Cells

The performance of the designed PA, especially the output power and efficiency, are sensitively dependent on the performance of the wideband differential power cells. On this basis the differential power cells design becomes a critical task in this work. As the goal of this design is to achieve a 16-dBm output power for the balanced PA, the required output power of the power cell used for BA should be 13 dBm. Taking into consideration of insertion loss from passive components (approximately 1.5 dB is assumed in total) as well as leaving sufficient design margin, an output power of 14.5 dBm is determined to be the design target for the power cells used for the BA. Two pairs of HBTs with 1-μm emitter width, 70-nm emitter length and 10 fingers are chosen for the differential power cell design. Moreover, to improve the gain of the power cell, neutralization capacitors are used. By running load-pull simulations at 90 GHz, it has been found that the optimal impedance is 16.1 + j10.6 and the impedance for maximum PAE is 20.1 + j25. Fig. 5.6 shows the simulated results. Given that the ultimate goal of this work is a wideband design, load-pull simulations across a broad bandwidth, from 80 GHz to 110 GHz, are conducted. A transformer-based balun serves to satisfy the required impedance pre-matching. Once the design for the output-stage of the power cell is completed, a driver stage is something that future research should look at. The simplified schematic of the designed power cell is given in Fig. 5.5.

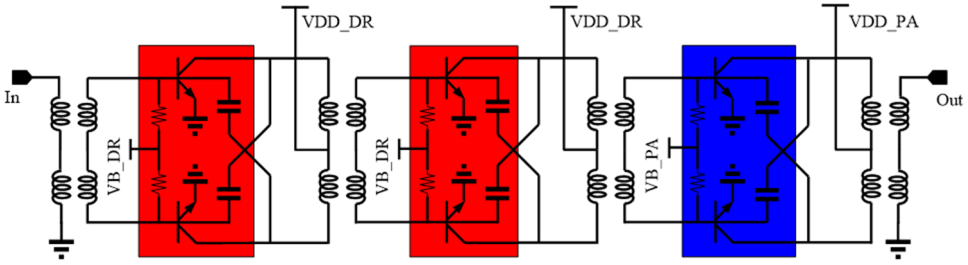


Figure 5.5: Simplified circuit schematic of the designed 3-stage differential power cell.

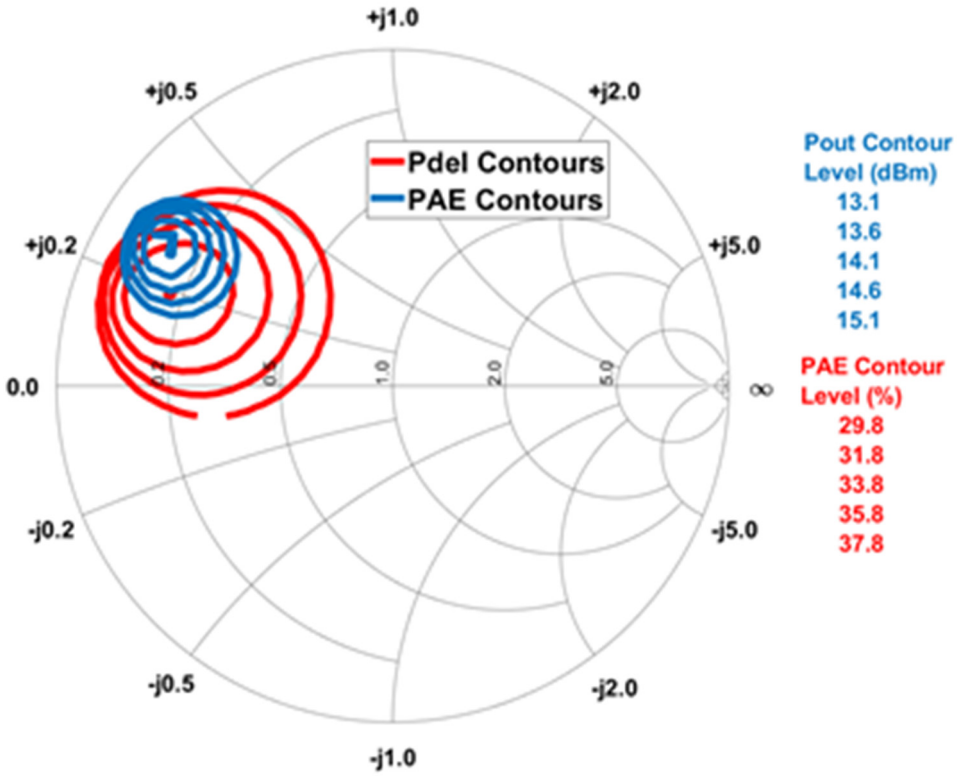


Figure 5.6: Simulated load-pull results at 90 GHz.

5.4 Measurement Results and Discussions

To measure the performance of the PA, a prototype is fabricated. The microphotograph of the designed die can be found in Fig. 5.7. Including the testing pads, the die size is only 0.6×0.9 mm^2. For testing purposes, on-chip probing is used for RF measurement and all DC pads are wire-bonded to a PCB test board.

5.4.1 Small-Signal Performance

In order to test our design, we take some measurements of small-signal performance. The measurement was conducted using on-wafer G-S-G probing up to 110 GHz by means of a vector network analyzer N5290A from Keysight™ and 100-μm pitch (GSG) Infinity Probes with 1-mm connectors from FormFactor™, Inc. The on-wafer calibration was made by using a conventional SOLT to move the reference plane from the connectors of the equipment to the tips of the RF probes.

The measured S-parameters can be found in Fig. 5.8. As illustrated, it shows excellent input and output impedance matching and reverses isolation due to the fact that a BA architecture is used, which indicates good stability. The S_{11} and S_{22} are both less than -15 dB across the frequency band of interest. Additionally, the 3-dB bandwidth in terms of S_{21} covers a frequency range of 80-100 GHz. The measured small-signal gain is 14 dB and 11 dB at 85 and 100 GHz, respectively. To compare the differences, both the EM

simulated and measured S-parameters are given. The EM simulated and measured results show good consistency with each other.

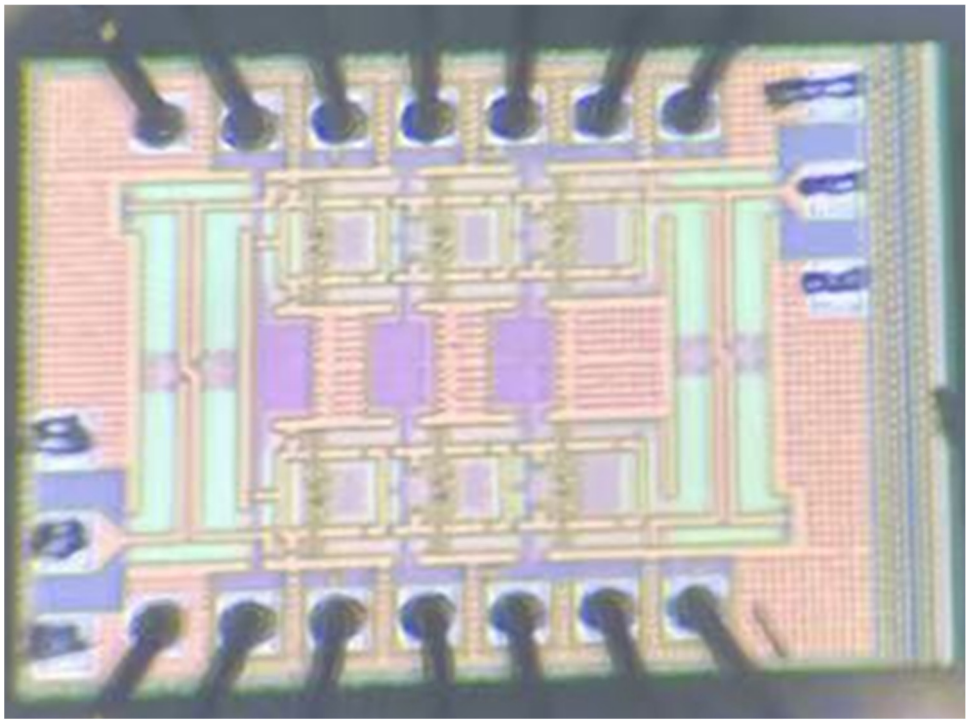


Figure 5.7: Die microphotograph of the designed balanced PA.

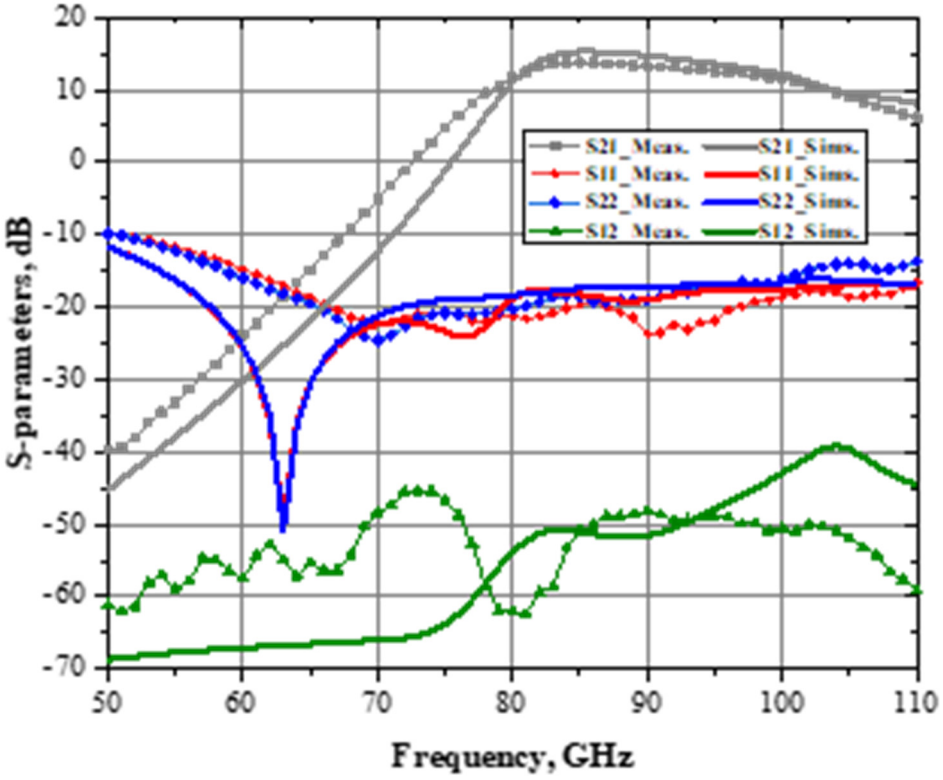


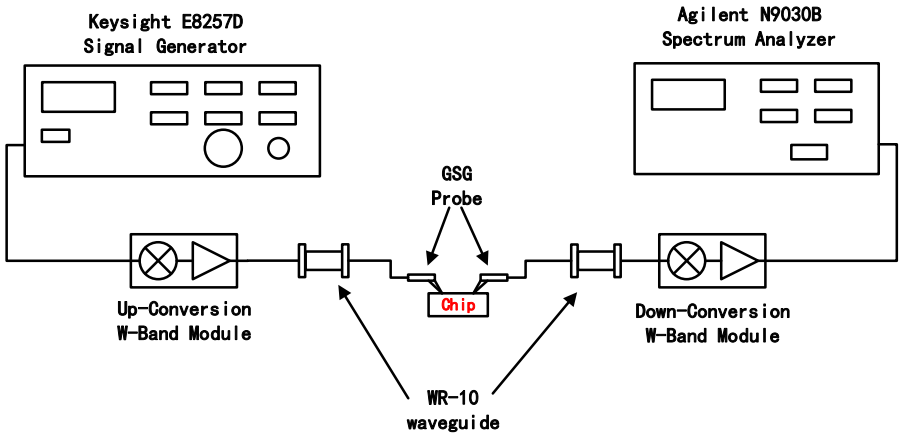
Figure 5.8: Simulated and measured S-parameters of the designed PA using BA architecture.

5.4.2 Large-Signal Performance with Continuous-Wave Signal

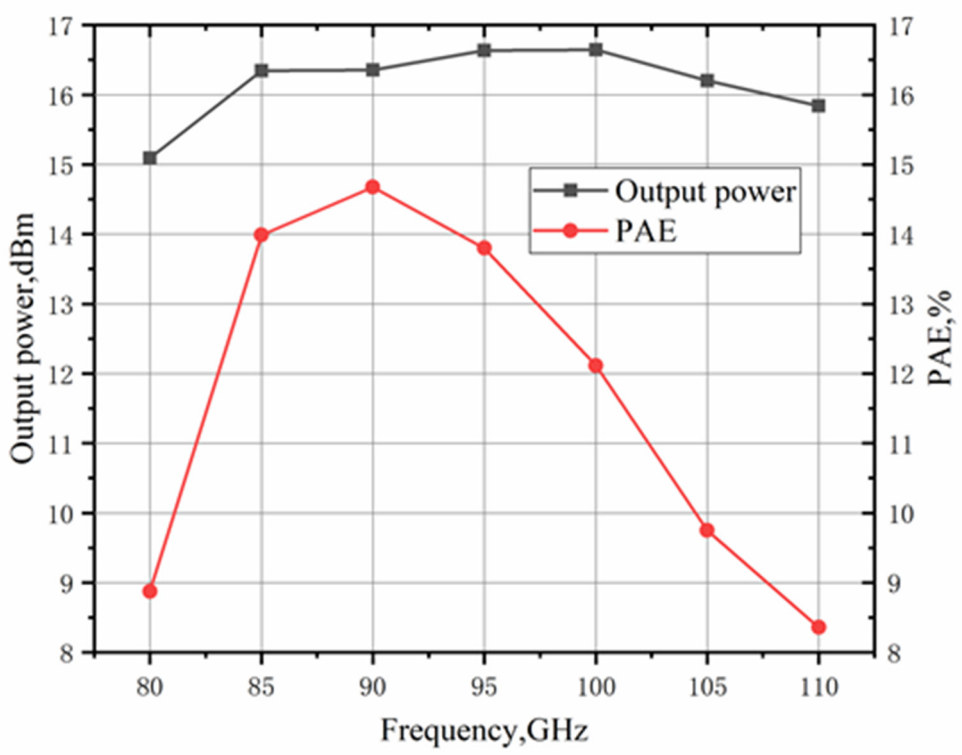
Moreover, our design is tested for its large-signal performance. The block diagram of the testing set-up is shown in Fig. 5.9(a). The E8257D PSG RF Analog Signal Generator from Keysight generates a CW input signal with sufficient power at 15 GHz. Furthermore, two Keysight U8489A USB Thermocouple Power Sensors alo ring resonator ng with two W-band directional couplers monitor the power levels at the input and output of the designed PA. In this set-up, the W-band up-conversion module could provide a maximum

output power of about 11 dBm including the power losses of waveguides, GSG probes and cables for interconnections.

The measured performance in terms of saturated output power and PAE are all given in Fig. 5.9(b). As illustrated, across the frequency range of 80-110 GHz, the Psat is greater than 15 dBm. The peak PAE is better than 8%. The highest PAE is achieved at 90 GHz, which is better than 14%. These outcomes prove that using the presented BA architecture for wideband PA design at W-band is feasible.



(a)



(b)

Figure 5.9: The measured large-signal CW performance of the designed PA, (a) measurement set-up, (b) PAE and output power as a function of operating frequency.

5.4.3 Comparisons and Discussions

A summary of the performance of the presented BA is given in Table 5 and also compared with other state-of-the-art designs (see Table below).

Ref.	Freq. (GHz)	Tech.	Sat. Power (dBm)	Gain (dB)	Peak PAE (%)	VDD (V)	Die Area (mm^2)
[70]	90	65nm CMOS	18.3	12.5	9.5	1.2	0.82
[25]	113	65nm CMOS	13.8	13.4	10	2	0.21
[26]	86	65nm CMOS	11.9	18.6	9	1	0.37
[27]	110	65nm CMOS	14.8	14.1	9.4	2	0.32
[28]	100	65nm CMOS	10	13	7	1.2	0.33
[71]	79	65nm CMOS	19.3	24.2	19.2	1	0.86
[72]	78	180nm SiGe	14	18.3	2	3.2	0.85
[73]	80	130nm SiGe	27.3	19.3	12.4	1.8	6.48
[74]	95	130nm SiGe	22	21.5	5.8	N/A	48
[62]	100	130nm SiGe	16.3	14.5	14.1	2	0.64
This work	**90**	**130nm SiGe**	**16.4**	**14**	**14.5**	**1.6**	**0.54**

Table 5: Comparison of the presented PA with some other designs described in various studies.

By observing the summarized data that is generated by different designs, some interesting results can be observed. Despite the fact that superior saturated power and PAE can be obtained in these works [71] [73], the frequencies they are operating at are below 80GHz, so these designs might not be used in W-band or even sub-THz. Compared with these designs [70, 74], although the PAs have better saturated power, the power efficiency is much worse. It can be firmly concluded that the BA-based architecture is potentially suitable for wideband PA design at the mm-Wave frequency region.

5.5 Conclusions

The design of wideband PA using a BA architecture along with edge-coupled quadrature couplers has been presented in this work. Because the BA architecture has been utilized, good input and output impedance matching are achieved through a relatively wide bandwidth. Additionally, the output of an edge-coupled quadrature coupler design is also shown. Based on the obtained results, it proves two things: firstly, that a sufficient coupling coefficient could be achieved in this simple structure; and secondly, the magnitude and phase errors can be minimized over a relatively wide bandwidth. As a proof-of-concept, a prototype PA is fabricated in a 0.13-μm SiGe HBT technology that operates at 80-100 GHz. A good agreement between the EM simulated and measured results has been achieved. According to the results, the designed PA has a more than 15-dBm Psat with a PAE of more than 14% at 90 GHz. Based on the results, it can be concluded that the BA-based architecture is potentially suitable for wideband PA design at the mm-Wave frequency region.

Chapter 6: Conclusion and Future Work

This thesis presents the current state of research work being done on designing radio frequency transmitters for W-band millimeter-wave 5G communication. After researching as much as possible the growing demand of mmWave communication and reviewing different designs offered by many relevant studies, some high-performance switches and PA for RF transmitters with innovative structures are presented. In this chapter, a summary of the research is presented in Section 6.1 and suggestions for future work to be carried out will be discussed in Section 6.2.

6.1 Research Summary

This thesis developed three novel design approaches for low-cost mm-wave transmitter designs in silicon-based technology. The summaries of these designs in terms of their novelties are given below.

- Power-handling capability of bulk CMOS-based switch to operate in mm-wave region is significantly limited by the reduced threshold voltage of active devices. The reason for this is device scaling. A passive-inspired solution is proposed in this thesis first. It still utilizes a classical symmetrical architecture along with shunt-connected switching transistors, but a novel design approach that combines both power dividing and impedance transformation techniques is used to improve 1-dB compression point. Thus, the fundamental limitation of the power-handling capability due to the reduced threshold voltage is removed. To valid the presented theory, a 90-GHz symmetrical SPDT switch is implemented in a 55nm bulk CMOS technology and achieves a measured P1dB of 15 dBm and an insertion loss of 3.5 dB and an isolation of 17 dB. The total area of the chip is only 0.14 mm^2.

- The second design is also concerned with mm-wave SPDT switch in bulk CMOS technology. To further improve the power-handling capability, an innovative approach is presented, which utilizes a unique passive ring structure. It allows a relatively strong RF signal passing through the TX branch, while the switching transistors are turned on. In

this way the fundamental limitation for P1dB due to reduced threshold voltage is overcome. As a proof-of-concept, a 90-GHz asymmetrical SPDT switch is designed in a standard 55-nm bulk CMOS technology. The design has achieved an IL of 3.2 dB and 3.6 dB in TX and RX mode, respectively. Moreover, more than 20 dB isolation is obtained in both modes. Because of using the proposed passive ring structure, a remarkable P1dB is achieved. No gain compression is observed at all, while a 19.5 dBm input power is injected into the TX branch of the designed SPDT switch. The die area of this design is only 0.26 mm^2.

- The third design is concerned with a wideband mm-Wave PA. To ensure the designed PA has sufficient output power, good PAE, superior input and output impedance matching across broadband, a BA architecture is used. In particular, edge-coupled quadrature couplers are designed and their performance about magnitude error and phase error is minimized through a relatively wide bandwidth. A prototype PA is fabricated in a 0.13-μm SiGe HBT technology. Supplied by 1.6 V power supply, the PA can provide more than 15 dBm saturated output power between 85-100 GHz that is equivalent to more than 16% fractional bandwidth. The peak PAE is better than 14% within this frequency range. The overall physical dimension of the designed PA is very compact. Including all pads, it is only 0.6 mm × 0.9 mm.

6.2 Future Work

With the dramatic development of 5G communication or even the next generation communication system, the demand for high-performance radio frequency transmitters will be increased significantly. Transmitters with lower fabrication cost, less power consumption and better performance are worth being further researched in the future. Here is a simple summary of my future work.

As discussed in this thesis, our designs mainly focused on bands below 100GHz. According to the future roadmap of the next-generation wireless system, it can be confidently forecast that the sub-terahertz (sub-THz) or even terahertz (THz) will be available in the following decades. It is important for researchers to design new front-end modules in higher bands. Improvements in the semiconductor manufacturing process nodes have clearly been made in recent times. By reducing the die area and increasing efficiency, integrated circuit designs with advanced process nodes can further enhance the performance. Classical technology like the bulk 55nm CMOS and 0.13-μm SiGe HBT were used in our design, but they are gradually losing their power. However, the balance between fabrication cost and performance must be taken into account during the design process. It is important for the right technology to be chosen so that future designs are viable and can be implemented in a cost-effective way.

Abbreviations

1G	1-Generation / First Generation
2G	2-Generation / Second Generation
3G	3-Generation / Third Generation
3Gpp	3rd Generation Partnership Project
4G	4-Generation / Fourth Generation
5G	5-Generation / Fifth Generation
5G NR	5-Generation New Radio
ANT	Antenna
BA	Balanced Amplifier
Bi-CMOS	Bipolar Complementary Metal-Oxide-Semiconductor
CLC	Capacitor-Inductor-Capacitor
CMOS	Complementary Metal-Oxide-Semiconductor
Coff	Parasitic Capacitances

dB	Decibel
dBm	Decibel Relative to One Milliwatt
DNW	Deep N-Well
EM	Electromagnetic
FEM	Front-end Module
FoM	Figure-Of-Merit
FR1	Frequency Range 1
FR2	Frequency Range 2
GaAs	Gallium Arsenide
Gbps	Gigabits Per Second
GHz	Gigahertz
G-S-G	Ground-Signal-Ground
HBT	Heterojunction Bipolar Transistors
Hz	Hertz
IC	Integrated Circuit

IEEE	Institute Of Electrical And Electronics Engineers
III/V	3-5 Semiconductor
IL	Insertion Loss
InP	Indium Phosphide
IP3	Third-Order Intercept Point
ISO	Isolation
ITN	Impedance Transformation Network
IWS	International Wireless Symposium
LC	Inductor-Capacitor
LT	Inductance
M1	Metal Layer 1
M2	Metal Layer 2
M3	Metal Layer 3
M4	Metal Layer 4
M5	Metal Layer 5

M6	Metal Layer 6
MHz	Megahertz
MIMO	Massive Multiple Input and Multiple Output
mm-Wave	Millimeter Wave
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MTT-S	The Microwave Theory and Techniques Society
nFET	N-Type Field-Effect Transistor
nm	Nanometer
P1dB	1 Db Compression Point
PA	Power Amplifier
PAE	Power-Added Efficiency
Psat	Saturated Output Power
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit

RX	Receive
SiGe	Silicon Germanium
SiO_2	Silicon Dioxide
SLOT	Short-Load-Open-Thru
SOI	Silicon-On-Insulator
SPDT	Single-Pole Double-Throw
TDD	Time-Division Multiplexing
TL	Transmission Line
TTL	Transistor-Transistor Logic
TX	Transmit
VCA	Voltage-Controlled Attenuator
VDI	Virginia Diode
VHF	Extremely High Frequency
VNA	Vector Network Analyzer
VTH	Threshold Voltage

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