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Design and Validation of a Reduced Switching Components Step-Up Multilevel Inverter (RSCS-MLI)

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Abstract: A reduced switching components step-up multilevel inverter (RSCS-MLI) is presented in the paper. The basic circuit of the proposed MLI can produce 11 levels in the output voltage with a reduced number of switching components. The other features of the proposed circuit include a low value of voltage stresses and the inherent generation of the voltage levels pertaining to the negative half without the requirement of an H-bridge. Fundamental frequency switching technique, also known as Nearest Level Control (NLC) technique, is implemented in the proposed topology for generating the switching signals. The experimental total harmonic distortion (THD) in the output voltage comes out to be 9.4% for modulation index equal to 1. Based on different parameters, a comparative study has been shown in the paper, which makes the claim of the proposed MLI stronger. An experimental setup is prepared to carry out the hardware implementation of the proposed structure and monitor its performance under dynamic load conditions, which is also used to verify the simulation results. Power loss analysis, carried out by using PLECS software, helps us to gain insight into different losses occurring while operating the inverter. The different results are explained and analyzed in the paper.

Keywords: RSCS-MLI; multilevel inverter; NLC; total harmonic distortion

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1. Introduction

Multilevel inverters are the main components in low to high voltage industrial applications such as electric vehicles, HVDC, FACTS devices, renewable power generation plants, micro grids etc. MLIs have low dv/dt characteristics, superior efficiency, better EMC, modularity, and fault tolerance capabilities, making it more advantageous than the two-level inverter [1–3]. Conventionally, there are three categories of the MLIs as cascaded H-bridge (CHB), neutral point clamped (NPC), and flying capacitor (FC) MLIs [4–6]. These topologies have drawbacks such as a high number of dc sources, switches, and other components. Additionally, they suffer from high voltage stress, high harmonic distortions etc. The research performed in the development of MLIs helped in reducing the components of the MLIs, which is essential and recommended. Many of the combinations of the components introduce different topologies of the MLIs. One of the topologies is packed U-cell topologies which have the advantage of the FCMLI but comes with high switching stress [7]. Additionally, capacitor voltage balancing is complex and requires space vector modulation or selective harmonic elimination technique. A reduced component extended topology is presented in [8] with three dc voltage sources. With the increase in level,

the number of the dc source increase. Another 11-level multilevel inverter topology is proposed with fewer components and three dc voltage sources [9]. A MLI topology with voltage boosting capabilities comprises an input inductor, a boost converter with a voltage multiplier circuit is presented in [10]. In [11], various PWM methods are analyzed with a three-phase 11-level inverter and a reduced number of switches.

A topology [12] having reduced power switches to achieve the analogous results of existing CHB configuration with the help of carrier-based sinusoidal technique. The authors discuss a seventeen-level topology focus on the inverter's boosted operation with fewer switches in [13]. The proposed structure utilizes 10 switches along with two dc sources and three capacitors. A PV array input-based eleven-level MLI is proposed in [14] with high output current quality and very low THD value. A multilevel inverter topology with n level is presented in [15]. The topology can be used in high voltage application. A modified switched capacitor is discussed in [16]. The presented topology produces 13 levels with nine switches and three dc voltage sources. Another multilevel inverter with a boosting feature comprising a switched capacitor with 7 achievable voltage levels has been introduced [17]. In [18], a single phase eleven-level inverter based on switched-capacitor is presented. The presented topology has self-balance capability and reduce components. Modulation techniques are vital in determining the total harmonic distortion in an MLI structure. Various modulation/switching techniques are nearest level control (NLC), selective harmonic elimination (SHE) based methods, space vector modulation (SVM) etc. A modified nearest level control method is discussed in [19] which has been implemented on cascaded h-bridge inverters with the aim to reduce THD. A novel configuration of MLI is presented in [20], which is called the K-type module. It requires 14 semiconductor switches, two dc sources, and two capacitors to obtain the 13-level output. Some more recent Switched-Capacitor-based topologies are discussed in [21–25].

The article is presented as follows: Section 1 explains the literature survey which contains work done by researchers previously. Section 2 presents the details of the design and working of the proposed converter. NLC Modulation strategy is explained in Section 3. Power loss analysis, which consists of mathematical expressions and various graphs, is deliberated in Section 4. The comparison with other topologies is presented in Section 5. The simulation results and the hardware implementation of the proposed topology is presented in Section 6. The different results are shown and explained. The article concludes with Section 7.

2. Proposed RSCS-MLI Circuit

2.1. Description and Operation

The proposed inverter (Figure 1) involves two dc sources, one capacitor besides 11 semiconductor power switches i.e., S_1, S_2, S_3, S_4, P_1, P_2, P_3, P4, S_X, S_Y and S_B. The ratio of magnitudes of the dc sources used here is 2:1 i.e., the magnitudes of dc sources are V_{DC} and $V_{DC}/2$. The 11-levels can be generated by the circuit in which five are positive (+0.5 V_{DC}, +V_{DC}, +1.5 V_{DC}, +2 V_{DC} and +2.5 V_{DC}), five are negative levels (−0.5 V_{DC}, −V_{DC}, −1.5 V_{DC}, −2 V_{DC} and −2.5 V_{DC}) and a zero voltage level i.e., $V_o = 0$. The stress on the switches S_x, S_1, S_2, P_1, P_2 and S_B is equal to the input voltage whereas the switches S_3, P_3, P_4 and S_4 have blocking voltage of 0.5 V_{DC}. The floating capacitor's voltage is maintained at V_{DC}.

The switching states pertaining to all the voltage levels are placed in Table 1. The conduction levels are discussed below:

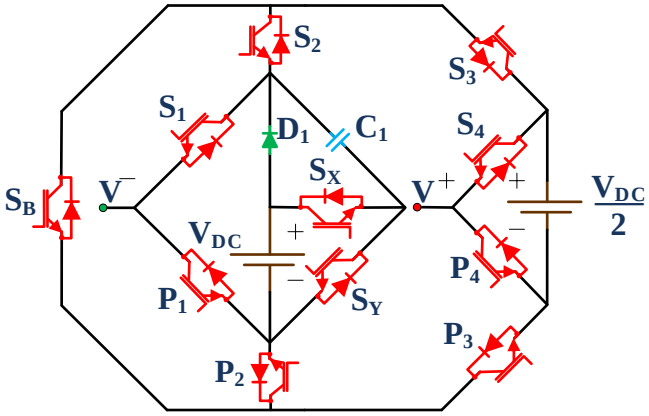


Figure 1. Proposed RSCS-MLI.

Table 1. Switching Table Along with Output Voltage.

	V_o	S_X	S_1	S_2	S_3	S_4	S_B	S_Y	P_1	P_2	P_3	P_4
Positive Voltage Levels	2.5 V_{DC}	1	0	1	0	1	1	0	1	0	1	0
	2 V_{DC}	1	0	1	1	1	0	0	1	0	0	0
	1.5 V_{DC}	1	0	1	1	0	0	0	1	0	0	1
	V_{DC}	0	0	1	1	1	0	1	1	0	0	0
	0.5 V_{DC}	0	0	1	1	0	0	1	1	0	0	1
Zero Voltage Level	0	0	1	1	1	1	0	1	0	0	0	0
Negative Voltage Levels	−0.5 V_{DC}	0	1	0	0	1	0	1	0	1	1	0
	$-V_{DC}$	0	1	0	0	0	0	1	0	1	1	1
	−1.5 V_{DC}	0	1	0	1	0	1	1	0	1	0	1
	−2 V_{DC}	1	1	0	0	0	0	0	0	1	1	1
	−2.5 V_{DC}	1	1	0	1	0	1	0	0	1	0	1

Zero level (0 V): The zero states can be achieved either by turning on the switches S_1, S_2, S_3, S_4 or P_1, P_2, P_3, P_4. The capacitor starts charging with the path VDC, D1, C1, SY during the zero level and settles at the voltage V_{DC}. There is no necessity of an h-bridge to change the polarity as it is an inherent feature of the topology.

First level (+V_{DC}/2): The first level follows the path as P_1, S_Y, C_1, S_2, S_3, $-V_{DC}/2$, and P_4. This result in formation of first level with voltage level 0.5 V_{DC}. The capacitor's voltage remains settled at V_{DC}.

Second level (+V_{DC}): For the second level with voltage magnitude of V_{DC}, the switches which remain in conduction are P_1, S_Y, C_1, S_2, S_3, and S_4. In this mode, no changes are observed in the capacitor voltage.

Third level (+3 V_{DC}/2): In this level, the output is produced by the additive nature of the V_{DC}, capacitor C_1, and the $-V_{DC}/2$. The conduction path is P_1, V_{DC}, S_X, C_1, S_2, S_3, $-V_{DC}/2$, and P_4. The capacitor starts discharging in this mode. The output of this level is $1.5V_{DC}$.

Fourth level (+2 V_{DC}): This level is obtained by following the path as P_1, V_{DC}, S_X, C_1, S_2, S_3, and S_4. The output of this level is 2 V_{DC} which is achieved with the help of capacitor C_1.

Fifth level (+5 V_{DC}/2): In this level the switch SB, conducts for the first time, helping in producing the fifth level whose output is 2.5 V_{DC}. The conduction path is as P_1, V_{DC}, S_X, C_1, S_2, S_B, P_3, $+V_{DC}/2$, and S_4. Similarly, the negative levels are achieved as according to those given in the Table 1. Figure 2 shows the conduction diagram for the various output voltage levels.

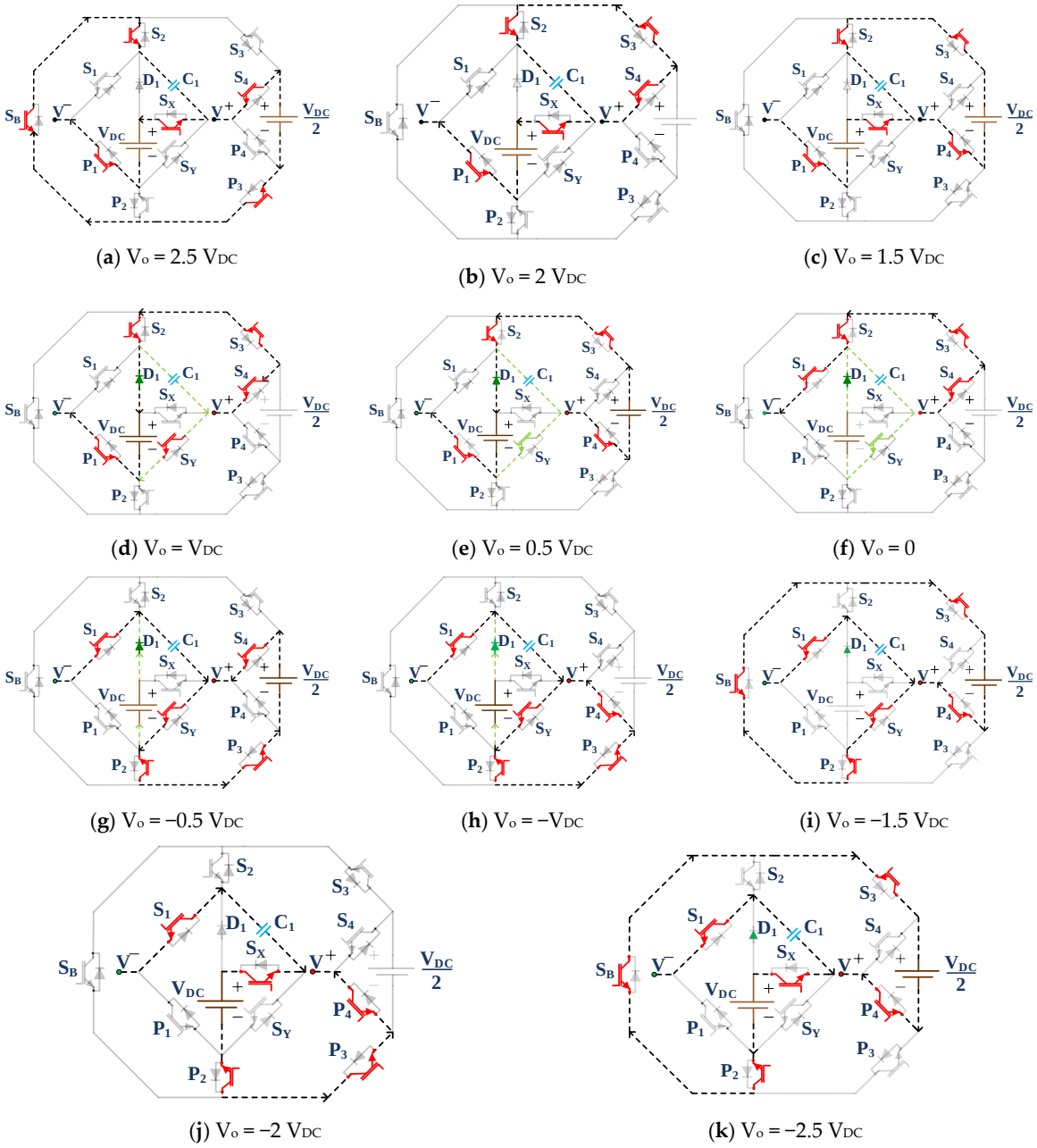


Figure 2. Conduction paths for different voltage levels of the proposed topology.

2.2. Total Standing Voltage

The voltage stress or the voltage required to be blocked by the switches governs the rating of power switches to be used in the implementation of the MLI circuit. Total Standing Voltage (*TSV*) refers to the total sum of the voltage stresses on all the switches in the circuit. Therefore, a low value of *TSV* indicates that the low rating switches can be used, which means the cost of the switches is lower, ultimately deciding the overall cost of the inverter circuit. Additionally, if *TSV* is lower the stress on the switches is low hence the life of the switches increase. In the present topology, the magnitude of DC voltage sources are in the ratio of 2:1. The blocking voltage on different switches are shown in Figure 3.

Mathematically, the TSV for the proposed MLI topology is calculated as given below:

$TSV = V_{S1} + V_{S2} + V_{S3} + V_{S4} + V_{P1} + V_{P2} + V_{P3} + V_{P4} + V_{SB} + V_{Sx} + V_{Sy} + V_{Sb} = (2 + 2 + 0.5 + 0.5 + 2 + 2 + 0.5 + 0.5 + 1 + 1 + 0.5 + 0.5)\ V_{DC} = 12.5\ V_{DC}$

The TSV magnitude can be divided by the maximum output voltage to obtain the per-unit TSV. For the proposed topology here, it is calculated as follows:

$$Per - Unit\ TSV\left(TSV_{p.u.}\right) = \frac{TSV}{Maximum\ Output\ Voltage} = \frac{12.5}{2.5} = 5 \quad (1)$$

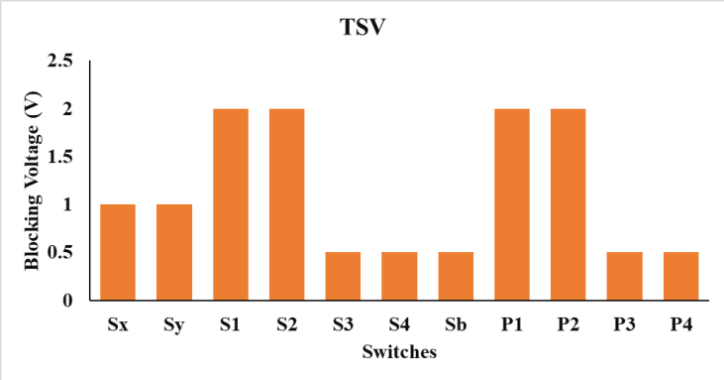


Figure 3. Voltage stress on switches in the proposed topology.

3. Modulation Technique

Various pulse width modulation (PWM) techniques can be used to generate the signals required for giving pulses to different switches. They are broadly categorized into high (sinusoidal PWM, level-shifted and phase shifted PWM etc.) and low frequency (NLC-PWM, SHE-PWM, SVM-PWM etc.) modulation techniques. The advantage with the low frequency switching techniques is the low value of losses in the switches as there is less transition in the *ON* and *OFF* state of the switches [16]. In the proposed work, NLC modulation technique has been in the proposed MLI. To generate switching pulses, a sine wave is taken as a reference. The NLC switching scheme is shown in Figure 4. The Firing angle is calculated [17] as:

$$\alpha_i = \sin^{-1}\left(\frac{i-0.5}{n}\right);\ for\ i = 1,2,3\ldots n = \frac{N-1}{2} \quad (2)$$

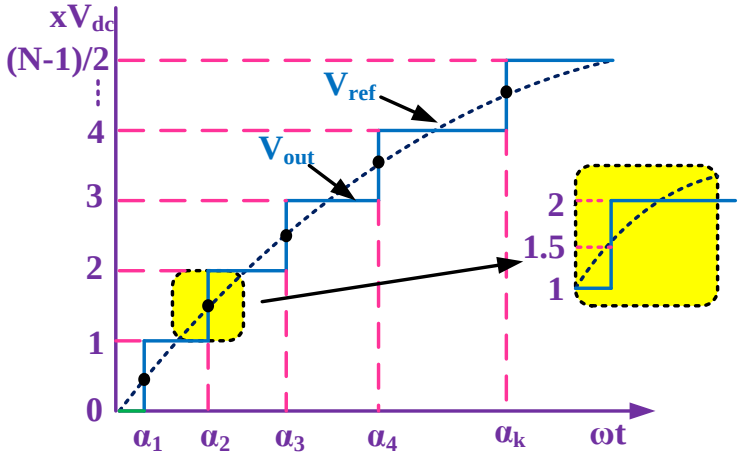
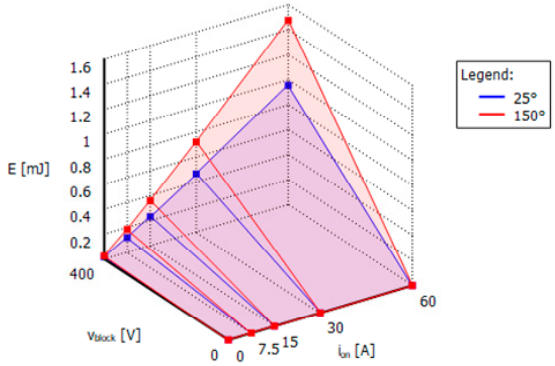


Figure 4. NLC Switching Scheme.

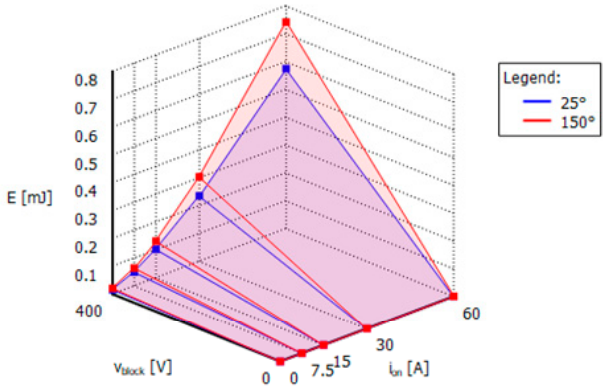
4. Power Loss Analysis

In operating the power circuit, various losses occur in the power switches. These losses are due to switching transitions as well as due to their conduction. The losses pertaining to the transition of switches i.e., turning the switches *ON* and *OFF*, are termed as switching losses. On the other hand, conduction losses are due to the conduction of the

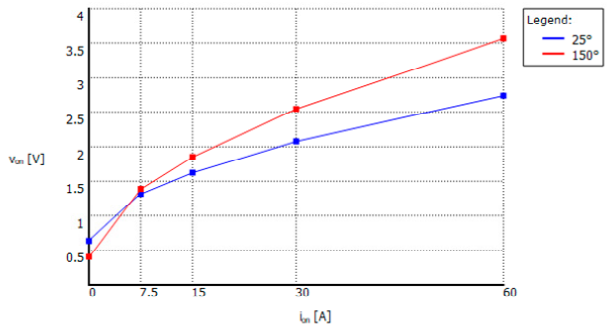
switches. To calculate these losses, the power loss analysis of the circuit should be taken into consideration. Therefore, the thermal modelling of the proposed converter has been done in PLECS software, and different losses have been recorded. The loss can be calculated with the sum of conduction losses and switching losses. The thermal loss profile for the IGBT FGA25N120 is shown in Figure 5. The thermal description depicting the turn-on loss, turn-off loss, and conduction loss have been shown in Figure 5a–c, respectively. This is completed in a PLECS environment with the help of heat sink and the thermal resistance of 1K/W at the ambient temperature of 25 °C. The plot shows the two temperatures as 25 °C and 150 °C which cover loss model based on manufacturers data. The operating junction temperature and storage temperature ranges from −55 to +150 °C. These losses are described as follows:



(**a**) Losses during turning ON



(**b**) Losses during turning OFF



(**c**) Losses during Conduction

Figure 5. Thermal Description for Different Losses for Different Temperature in °C.

4.1. Conduction Losses

When the switches i.e., IGBT, *ON* due to the internal resistance the current experience an oppose to flow which cause losses in the switches. This loss in the switch is called conduction loss. Mathematically the conduction loss can be expressed as:

$$P_{Cond_{Loss}} = \sum_{All\ Switches} {I_{ON}}^2 \times R_{Internal} \tag{3}$$

where I_{ON} is the current flowing through the switches during conduction, $R_{Internal}$ is the internal resistance of the switch.

4.2. Switching Losses

The power dissipated in the switch during turning *ON* and *OFF* is known as switching losses. The switching loss includes the turn-ON losses and the turn-OFF losses which can be calculated as elaborated in [26].

$$\begin{aligned} E_{OFF,n} &= \int_0^{t_{OFF}} v(t)i(t)dt \\ E_{OFF,n} &= \int_0^{t_{OFF}} \left(\frac{V_{sw,n}}{t_{OFF}}t\right)\left(-\frac{I}{t_{OFF}}(t - t_{OFF})\right)dt \\ E_{OFF,n} &= \frac{V_{OFF,n} \times I_{OFF,n}}{6} \end{aligned} \tag{4}$$

Similarly, one can calculate the energy loss occurred during turning *ON* the switch which can be expressed as:

$$E_{ON,n} = \frac{V_{ON,n} \times I_{ON,n}}{6} \tag{5}$$

where $E_{OFF,n}$ and $E_{ON,n}$—turn off and turn on energy loss for the n switch at time t_{OFF} and t_{ON}, respectively. Mathematically, the power loss occurs when the switch changes its state from *OFF* to *ON* is give as:

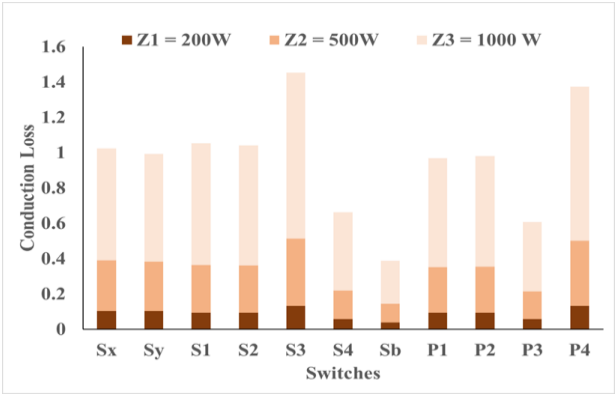
$$P_{SW-LOSS} = \sum_n \sum_{\frac{1}{f_{OUTPUT}}} \frac{V_{ON,n} \times I_{ON,n} \times T_{ON,n}}{6} + \frac{V_{OFF,n} \times I_{OFF,n} \times T_{OFF,n}}{6} \tag{6}$$

where V_{ON}, I_{ON}, T_{ON} and V_{OFF}, I_{OFF}, T_{OFF} are the respective parameters for the *ON* and *OFF* state of the switch. f_{OUTPUT} is output voltage frequency.

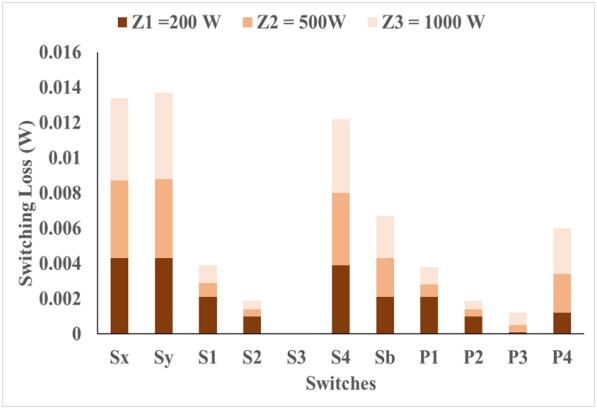
Finally, the total loss can be calculated as the sum of conduction loss and switching loss. Therefore,

$$P_{T-Loss} = P_{Cond_{LOSS}} + P_{SW-LOSS} \tag{7}$$

The simulation results are developed in the environment of PLECS. Three different loading conditions such as Z_1 = 200 W (400 Ω), Z_2 = 500 W (150 Ω + 70 mH), and Z_3 = 1 kW (60 + 100 mH) are analyzed. The reason for low loss in switches is the low switching frequency. Conduction and switching losses are obtained for these loads for different switches and are placed in Figure 6a,b, respectively. The efficiency vs load plot is shown in Figure 6c. At load 200 W (400 Ω), maximum efficiency of 97.81% is obtained.



(**a**)



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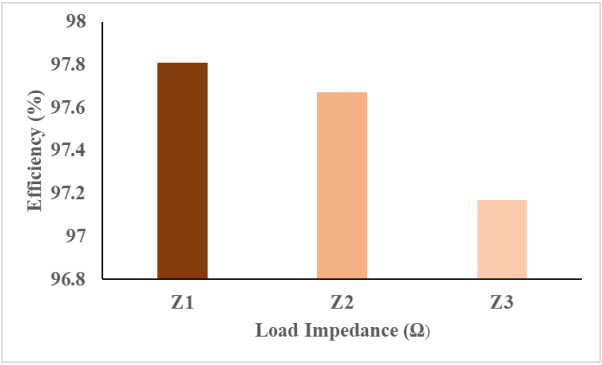


(**c**)

Figure 6. (**a**) Conduction Loss, (**b**) Switching Loss, (**c**) Efficiency Variation with Load.

5. Comparison with Different Topologies

This section contains a comparative analysis between the proposed topology and some other similar inverter structures. It has been done to make the proposed claim stronger. The comparison has been carried out by using different parameters such as count of switches (N_{switch}), diodes (N_{diodes}), dc sources (N_{source}), capacitors (N_{cap}), and levels (N_L). The additional parameters taken are N_T, which is the sum of N_{switch} and N_{diode}, and N_L/N_T i.e., the ratio of N_L and N_T. Table 2 is a comparative analysis of the other topologies with the proposed topologies. In comparison with other topologies, the presented topology requires less DC sources which ultimately will reduce the size of the proposed MLI and make it economic except for the topology present in the [10]. However, this topology requires a higher number of diodes and capacitors, which tends to elevate

the cost of the whole system. For the topology present in the [18], the parameter N_{source} is the same as our topology, but N_{switch} and N_{cap} is more. In [19,20] N_{source} and N_{diode} are both high. Additionally, in [20], N_{switch} is also higher than our proposed topology. The ratio N_L/N_T for the proposed topology is better than [10,18,19,25], which shows that the topology presented in this work stands better than the mentioned topologies.

Table 2. Comparative Evaluation.

Topology	N_{switch}	N_{diode}	N_T	N_L/N_T	N_{source}	N_{cap}	N_L	$TSV_{P.U.}$
[8]	8	0	8	1.4	3	0	11	9.6
[9]	8	0	8	1.4	3	0	11	5.6
[10]	10	9	19	0.6	1	9	11	8
[18]	12	1	13	0.8	2	2	11	6.4
[19]	11	5	16	0.7	5	0	11	5
[20]	14	0	14	0.9	2	2	13	6.33
[25]	10	4	14	0.6	1	4	9	7
Proposed	**11**	**1**	**12**	**0.9**	**2**	**1**	**11**	**5**

The proposed topology and the topology presented in [19] has the lowest value of TSV. In [8,9], however, the number of switches required is less than the proposed topology, but the TSV is more than the proposed topology.

6. Results and Analysis

6.1. Simulation Outcomes

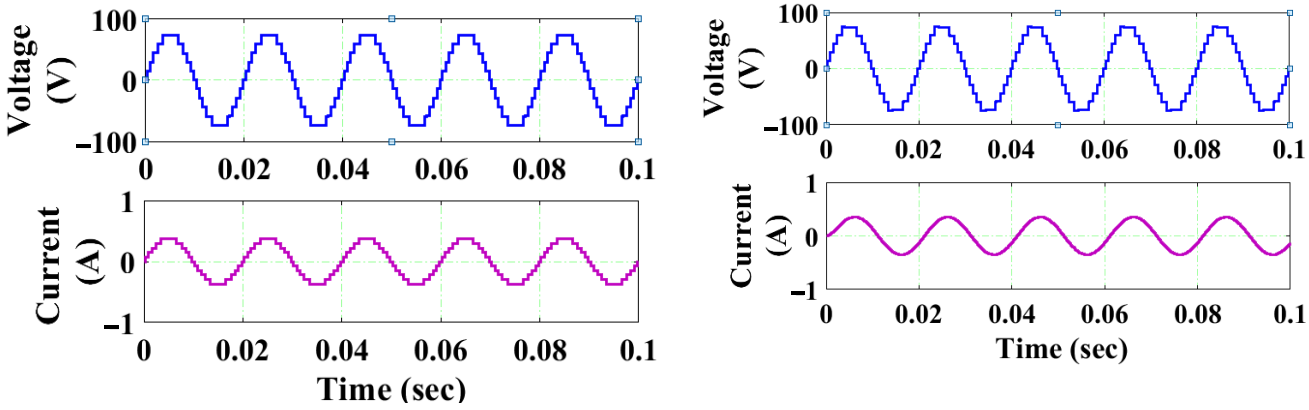
This section presents the different simulation results which were obtained by using MATLAB 2018a platform. Constant loading conditions were taken such as constant R and constant RL load. The topology was also tested under dynamic loading conditions. Results were obtained for modification in load and modulation index. Analysis under different loading conditions is discussed in the following subsections. The simulation parameters are placed under Table 3.

Table 3. Simulation Parameters.

Components	Specification
DC voltage source (2)	20V, 40V
Fundamental frequency	50 Hz
Capacitor	3000 μF
Load	R = 100 Ω, 200 Ω, L = 250 mH

6.1.1. Constant R and RL Load

Figure 7 represents the simulation results for a constant load (R and RL load). The voltage and current waveforms are recorded and displayed here. Figure 7a shows the output voltage and current waveforms for Z = 200 Ω. As it can be seen, the current is in phase with the voltage. The second constant loading result was taken for Z = 200 Ω + 250 mH, which is shown in Figure 7b. Due to the inductive load, the current waveform becomes smoother and it is also displaced in phase with the load voltage.

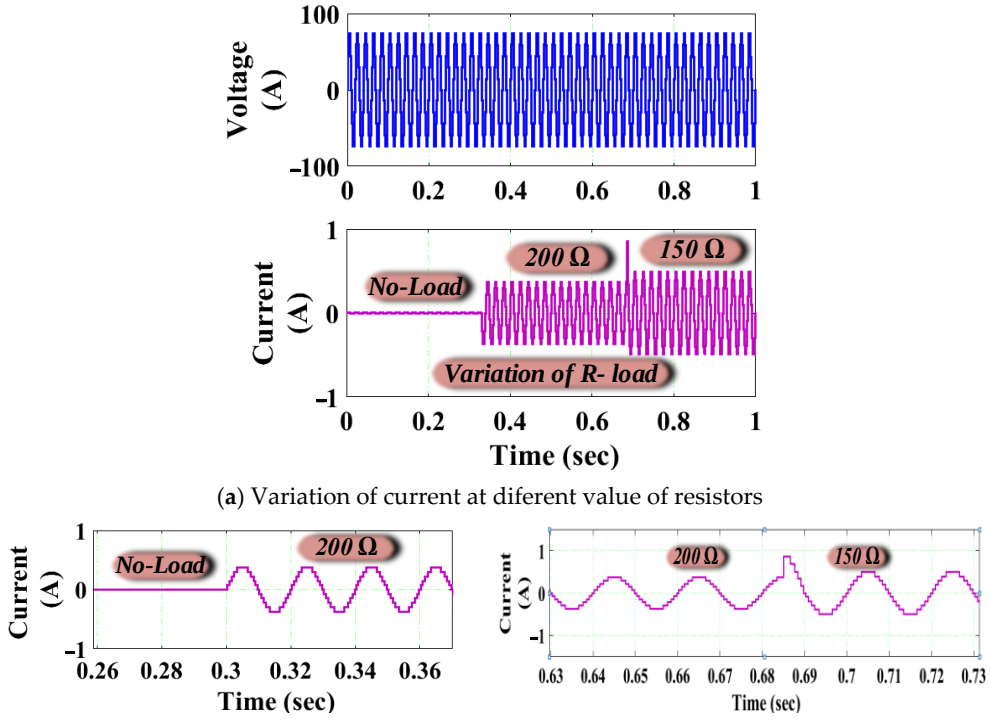


(**a**) Constant R load, Z = 200 Ω. (**b**) Constant RL load, Z = 200 Ω + 250 mH

Figure 7. Simulation Results for Constant Loading Condition.

6.1.2. Variable R and RL Load

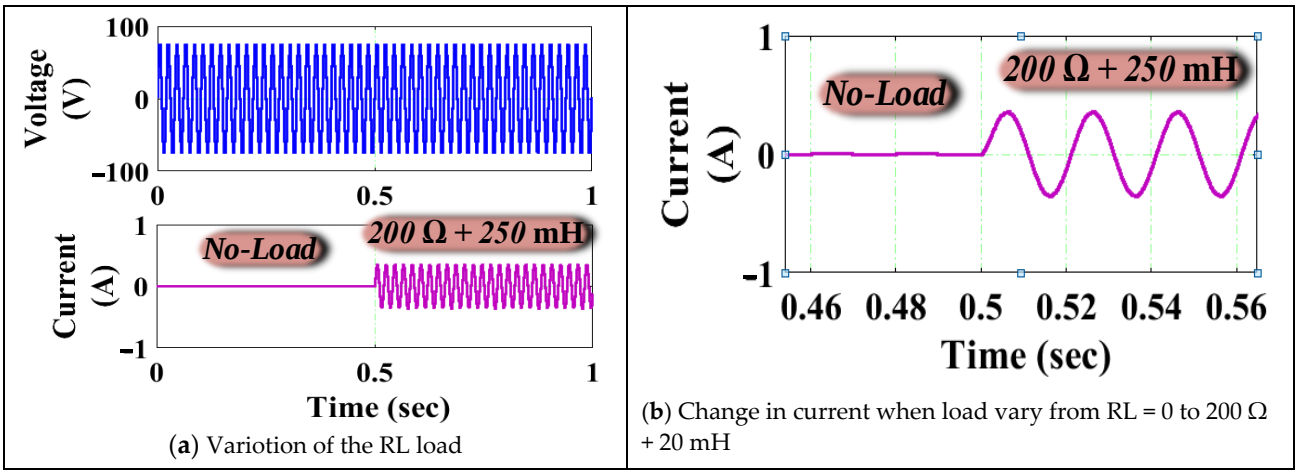
To analyze the topology in a dynamic loading situation, the results were analyzed for changing load conditions. Figures 8 and 9 depicts the load voltage and current waveforms for alteration in R and RL load, respectively. In Figure 8a, from a no-load condition, the load was first changed to Z = 200 Ω and then to Z = 200 Ω. It is visible from the current waveform that the magnitude is varied at the instants of load changing. However, to provide a close view, Figure 8b,c are included, showing the load changing instants from no-load to Z = 200 Ω and from Z = 200 Ω to Z = 100 Ω, respectively. The value of current increase with the decrease in the load. Similarly, the variation in RL load has also been shown in Figure 9a in which load is varied from no load to Z = 200 Ω + 250 mH. The closer view is given in Figure 9b in which output current can be seen to appear just after the change in load.



(**a**) Variation of current at diferent value of resistors

(**b**) Change in current from R = 0 to 200 Ω (**c**) Change in current from R = 200 to 150 Ω

Figure 8. Output Voltage and Current with Variation of the R-Load.



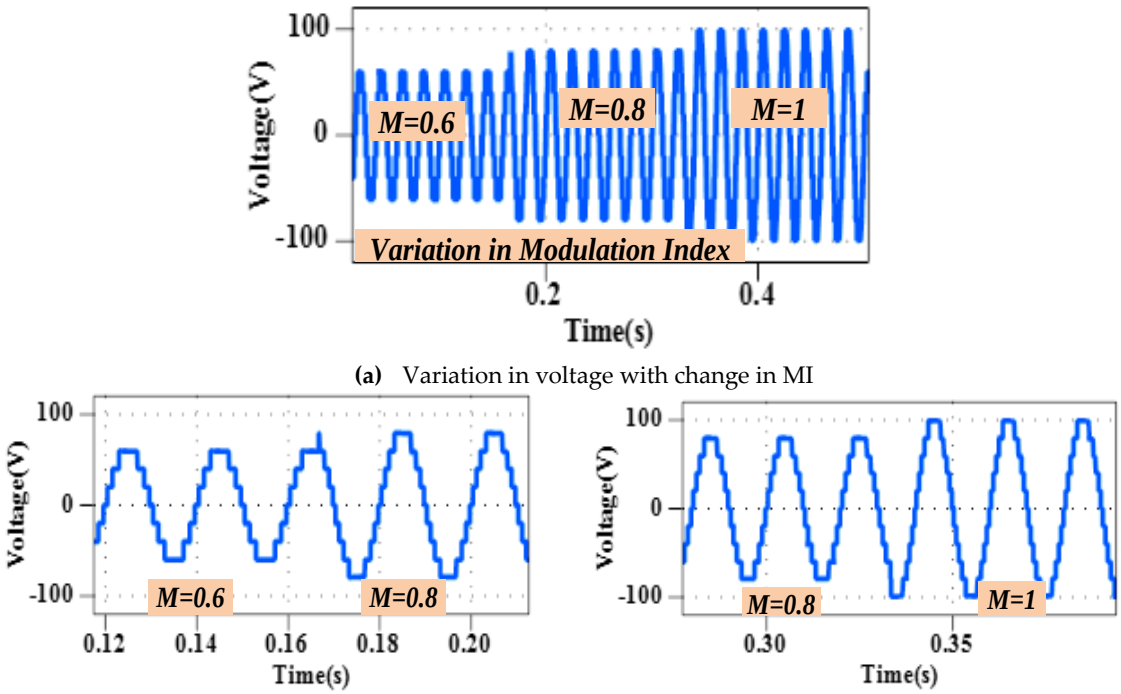
(**a**) Variotion of the RL load

(**b**) Change in current when load vary from RL = 0 to 200 Ω + 20 mH

Figure 9. Output Voltage and Current with Variation of the RL Load.

6.1.3. Variation in Modulation Index

Another dynamic condition that is taken into consideration is the change in the modulation index. Modulation Index (M) is the ratio of the modulating signal voltage to the career voltage. The value of the modulation index lies between 0 and 1. The proposed topology is analyzed with the variation of modulation index and observed the output voltage waveform. From Figure 10, we find that the output voltage levels are reduced when we move from m = 1 to 0.6 via 0.8. For M = 1 we have 11 levels, for M = 0.8 we have nine levels and for M = 0.6 we have seven levels.



(a) Variation in voltage with change in MI

(b) Voltage change when Mi vary from 0.6 to 0.8

(c) Voltage change when Mi vary from 0.8 to 1

Figure 10. Output voltage with variation in Modulation Index.

6.2. Hardware Implementation

A prototype of the proposed circuit is developed in the laboratory environment, as shown in Figure 11. The FGA25N120 IGBT is used as power semiconductor switches for the proposed hardware topology. A C2000 LAUNCHPAD XL TMS320F28379D is used to

generate control signals. With the help of the TLP 250H driving circuit, the IGBTs are fired. Two Scientech DC sources are used as the DC source for the prototype. The value of 200 Ω is taken as a resistive load. A Yokogawa DL 1640 digital oscilloscope is used to display voltages and current waveform. A typical block diagram of the circuit implementation is shown in Figure 12. It includes a TLP250H based driver circuit, and control logic has been implemented in TMS320F28379D.

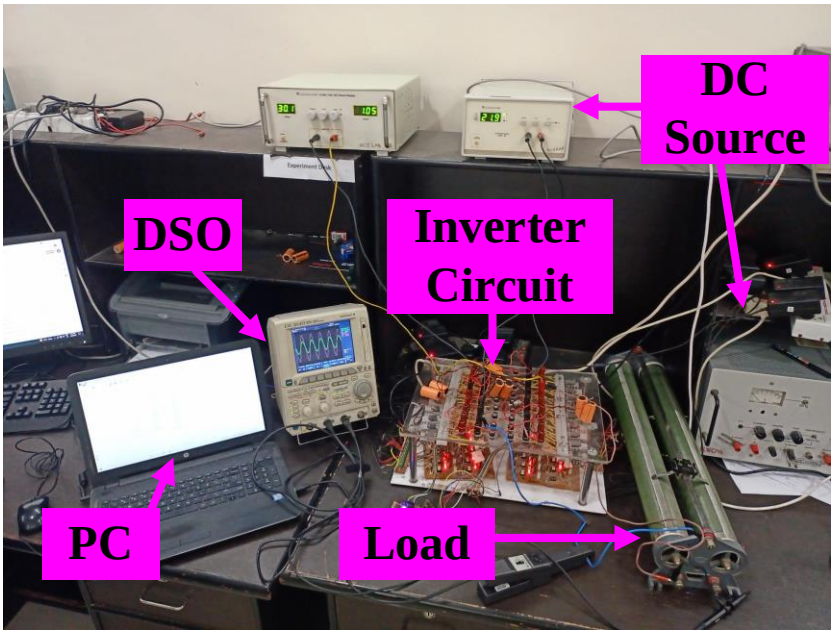


Figure 11. Laboratory Prototype of the Proposed Topology.

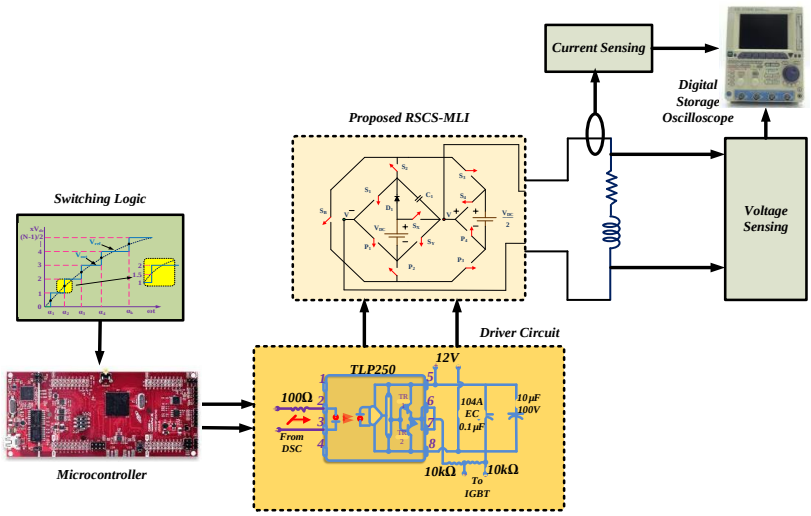


Figure 12. Circuit Used for the Implementation of the Topology.

These output voltage waveforms with 80 V as peak magnitude are shown in Figure 13a in which the different voltage levels are clearly visible. Figure 13b displays the load waveforms (voltage and current) for a resistive load i.e., Z = 200 Ω in which the two waveforms can be seen to be in phase with each other.

Figure 13c shows the variation in load from no load to 250 Ω to 150 Ω. A close view of the two load-changing moments have also been provided to see the change in current magnitude. As the load changes from Z = 250 Ω to Z = 150 Ω, the increase in current magnitude is visible from the given waveforms. The states are stable, and also, in this case, the phase displacement between the voltage and current is zero.

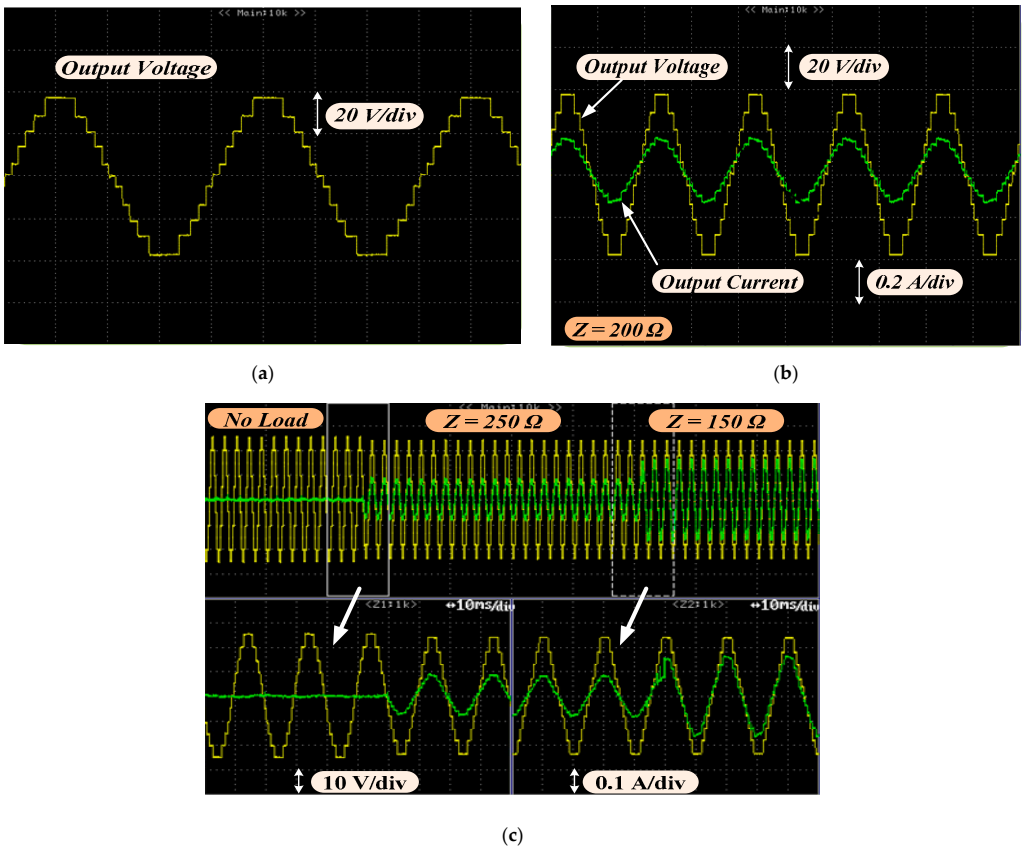


Figure 13. Hardware results of the proposed topology (**a**) Output Voltage (**b**) Voltage and current waveform for resistive load (**c**) Variation of the Current waveform for change in the R-Load.

The experimental THD in the load voltage measured from the power analyzer is 9.4% for a modulation index equal to 1. It is shown in Figure 14.

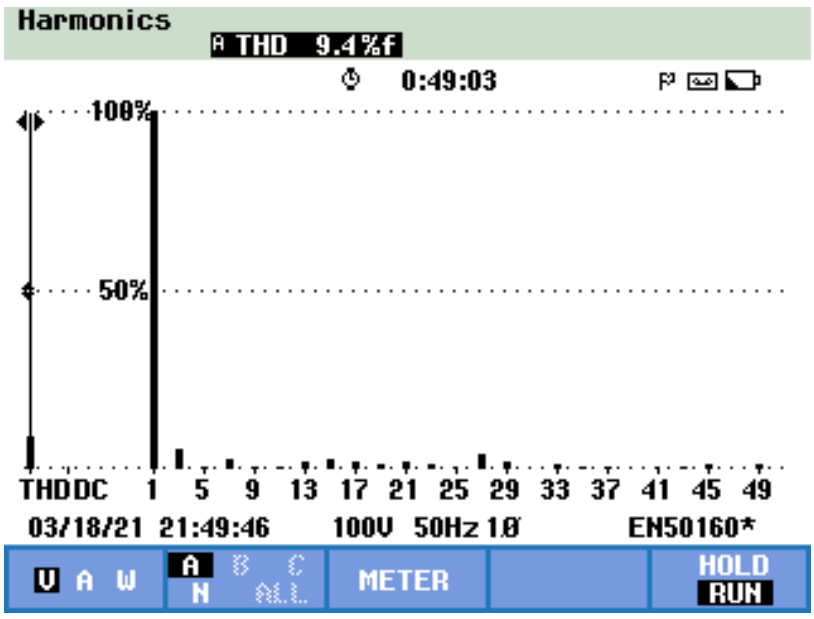


Figure 14. Hardware results for total harmonic distortion.

7. Conclusions

This paper presented and discussed a reduced switching components step-up multilevel inverter (RSCS-MLI). The topology converted the DC voltages in sinusoidal waves with a THD of 9.4%. The NLC modulation techniques were used to provide the pulses to the switches. The simulation of the model was developed in an environment of MATLAB2018a and the thermal analysis was completed in the PLECS environment. A prototype was developed in the laboratory. The simulation results were experimentally verified. A comparative evaluation of performance parameters has also been completed to validate the proposed topology.

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