Design of Efficient, Fast and Accurate Emulators for Photovoltaic Systems

by

Habes Ali Ahmad Khawaldeh

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Declaration

I am Habes Ali Ahmad Khawaldeh, and I certify that the work in this thesis has not previously been submitted for a degree. I recognize what plagiarism is and I hereby declare that this thesis, which is submitted to the School of Electrical and Data Engineering at the University of Technology Sydney, for the partial fulfillment of the requirements for the degree of Doctor of Philosophy is my own work.

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ABSTRACT

Photovoltaic systems (PVSs) continue to face ongoing challenges, such as the reliability of power electronic systems and the effective integration of energy storage. A PV emulator (PVE) provides a testing and analysis platform for PVSs, such as maximum power point tracking and partial shading effect, independent of weather conditions and ease of scaling. Many researchers have proposed different PVE topologies to mimic the real PVSs. A good PVE requires fast computing and power converters with a wide output range. However, the controller bandwidth restricts the emulator's response time, and it must stabilize the converter for many different operating points for a given insolation level. Hence, converter-based solutions generally have a slower response time than real PVSs.

The study's first phase is to devise a simple, reliable, effective circuit-based PVE based on the equivalent PV stacked cells that are cost-effective and perform close to a real PV source. A PVE that physically models a single-diode analytical model is studied. Due to its simplicity, the proposed PVE shows a better dynamic response and shorter settling time than several benchmarked commercial products, where a few power diodes and two resistors are used. Furthermore, the thermal characteristic of the PVE is identified and solved by adding a variable speed fan cooling system.

Phase two proposes a constant current source DC/DC converter (CCSC) for the PVE applications based on a cost-effective and straightforward method. The CCSC simplifies the converter and controller designs as it operates at a fixed point for each insolation level compared with a converter-based solution that requires a voltage-source converter with wide output operating ranges.

Even using a variable speed fan to control the operating temperature of the power semiconductor string, the overall system efficiency is low. The third phase of the study involves the proposed redesign of a PVE, using two new hybrid solutions that consist of a switching circuit (SC) is inserted parallel with the semiconductor string to manage the thermal behaviour of the emulator system. When the operating point

of the PVE moves from the current source region to the voltage source region, the more efficient converter switches in to replace the semiconductor string seamlessly to maintain the circuit operation of the emulator. The SC is only required to handle a narrow operating voltage range than a conventional pure switching converter-based solution. The experimental results show a high performance in terms of temperature, efficiency, and dynamic response.

Dedication

I would like to dedicate my thesis
To my parents:

Najah Al-Khawaldeh and Ali Khawaldeh
for their unconditional love.

To my academic advisor:
Prof. Dylan Dah-Chuan Lu

To my wife and sons:
Mariam Al-Khawaldeh, Ali, Hlayel and Ahmad

To my family and friends
for their great support.

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Habes Ali Ahmad Khawaldeh

Sydney, Australia, 2022.

List of Publications

Journal Papers

J-1. **H. A. Khawaldeh**, M. Al-soeidat, M. Farhangi, D. D. -C. Lu and L. Li, "Efficiency Improvement Scheme for PV Emulator Based on a Physical Equivalent PV-cell Model," in *IEEE Access,* doi: 10.1109/ACCESS.2021.3086498.

J-2. **H. A. Khawaldeh**, M. Al-soeidat, D. D.-C. Lu, and L. Li, "Simple and fast dynamic photovoltaic emulator based on a physical equivalent pv-cell model," *IET The Journal of Engineering*, vol. 2021, no. 5, pp. 276-285, 2021. Available: https://doi.org/10.1049/tje2.12032.

Journal Paper Under Review

J-1. **H. A. Khawaldeh**, M. Al-Soeidat, D. D. -C. Lu and L. Li, "Accurate, Fast and Power Efficient PV Emulator Based on Hybrid Passive and Active Circuits," in *CPSS Transactions on Power Electronics and Applications (CPSS TPEA)*, 2022.

Conference Papers

C-1. **H. A. Khawaldeh**, M. Al-soeidat, D. Dah-Chuan Lu and L. Li, "Fast Photovoltaic Emulator Based on PV-cell Equivalent Circuit Model," *2021 IEEE 12th Energy Conversion Congress & Exposition - Asia (ECCE-Asia)*, 2021, pp. 2121-2126, doi: 10.1109/ECCE-Asia49820.2021.9479298.

C-2. **H. A. Khawaldeh**, H. Aljarajreh, M. Al-Soeidat, D. D. -C. Lu and L. Li, "Performance Investigation of a PV Emulator Using Current Source and

Diode String," *2018 26th International Conference on Systems Engineering (ICSEng)*, 2018, pp. 1-5, doi: 10.1109/ICSENG.2018.8638207.

Conference Paper Under Review

C-1. **H. A. Khawaldeh**, M. Al-soeidat, D. Dah-Chuan Lu and L. Li, "Power Loss Reduction for PV Emulator Using Transistor-based PV Model," *2022 IEEE Energy Conversion Congress and Exposition - USA (ECCE-USA)*, 2022.

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Abbreviations

AC - Alternating Current

ADCs - Analog to Digital Converters

ARM - Advanced RISC Machines

BJT - The Bipolar Junction Transistor

CC - Constant Current

CCM - Continuous Conduction Mode

CCS - Constant Current Source

CCSC - Constant Current Source Converter

CdTe - Cadmium Telluride

CIGS - Copper Indium Gallium Selenide

CSR - Current Source Region

CV - Constant Voltage

DAC - Digital to Analog

DC - Direct Current

DCM - Discontinuous Conduction Mode

DP - Darlington Pair

DS - Diode String

DSP - The Digital Signal Processor

dSPACE - digital signal processing and control engineering

EMI - Electromagnetic Interference

FF - Field Factor

FOCV - Fraction Open-Circuit Voltage

FPGA - The Field Programmable Gate Array

FSCC - Fraction Short-Circuit Current

GaAs - Gallium Arsenide

GNG - The Growing Neural Gas

HC - Hill Climbing Control Method

HCC - Hysteresis Current Control

IC - Integrated Circuit

InC - Incremental Conductance

I-R - Current-Resistance

I-V - Current-Voltage

KCL - Kirchhoff Current Law

LABVIEW - Laboratory Virtual Instrument Engineering Workbench

LED - Light Emitting Diode

LEDs - Light Emitting Diodes

LUT - Look-up Table

MOSFET - Metal Oxide Semiconductor Field-Effect Transistors

MP - Maximum Power

MPP - Maximum Power Point

MPPs - Maximum Power Points

MPPT - Maximum Power Point Tracking

MTTF - The Mean Time To Failure

NIBB - Non-Inverting Buck-Boost Converter

NOCT - The Nominal Operating Cell Temperature

OC - Open-Circuit

OCV - Open-Circuit Voltage

PCB - Printed Circuit Board

PI - Proportional–Integral

PID - Proportional-Integral-Derivative

P&O - The Perturb and Observe

PPVE - Programmable Photovoltaic Emulator

PS - Partial Shading

P-V - Power-Voltage

PV - Photovoltaic

PVE - Photovoltaic Emulator or PV Emulator

PWM - Pulse Width Modulation

RESs - Renewable Energy Sources

RHPZ - Right Half-Plane Zero

RI - Constant Current Area Resistance

RV - Constant Voltage Region Resistance

SC - Switching Circuit

Si - Silicon

SIMO - Single Inductor Multiple-Output Converter

SISO - Single Input Single Output

SMPS - Switched Mode Power Supply

STC - The Standard Test Condition

TI - Texas Instruments

TM - Time-Multiplexing

V-I - Voltage-Current

V-R - Voltage-Resistance

VSR - Voltage Source Region

ZCS - Zero-Current Switching

ZVS - Zero-Voltage Switching

ZVZC - The Zero-Voltage-Zero-Current

1D - The Single Diode PV Model

1D1R - The Single Diode with Series Resistance PV Model

1D2R - The Single Diode with Series and Parallel Resistance PV Model

2D2R - The Two Diode with Series and Parallel Resistance PV Model

List of Symbols

a : Ideally factor for diode.

a_1 : Ideally factor for diode 1.

a_2 : Ideally factor for diode 2.

a_3 : Ideally factor for diode 3.

β_1 : The current gain of the transistor 1.

β_2 : The current gain of the transistor 2.

β_3 : The current gain of the transistor 3.

β_n : The current gain of the transistor n.

β : The multiplication of the cascade transistor current gain.

D : The duty cycle.

D_{boost} : The duty cycle of the boost DC/DC converter.

D_{step} : The constant step size.

E_g : The band-gap energy of the semiconductor material.

f_s : The switching frequency.

G : The Solar Irradiance.

G_n : The Solar Irradiance at the Standard Test Condition (STC) is 1000 $\frac{W}{m^2}$.

I_D : Diode forward current (A).

I_{D1} : The forward current of the Diode 1 (A).

I_{D2} : The forward current of the Diode 2 (A).

I_{D3} : The forward current of the Diode 3 (A).

I_{mpp} : The current at the maximum power point.

I_o : The output current of the PV emulator.

I_{ph} : Photocurrent (A).

$I_{ph,n}$: The light-generated current at the standard test condition (STC).

$I_{PV} \cong I_{sc}$: Short circuit current or photocurrent (A).

I_{ref} : The reference input current.

I_s : Reverse saturation current (A) for the diode.

I_{s1} : Reverse saturation current (A) for diode number 1.

$I_{s1,n}$: The nominal reverse saturation current.

I_{s2} : Reverse saturation current (A) for diode number 2.

I_{s3} : Reverse saturation current (A) for diode number 3.

$I_{sc,n}$: The short circuit current at STC.

$I_{s,n}$: The nominal reverse saturation current.

I_{step} : The current step size.

K : Boltzmann constant,$1.3806503 \times 10^{-}23$ ($\frac{J}{K}$).

K_d : Derivative Gain.

K_i : Integral Gain.

K_I : The PV cells short circuit current temperature coefficient.

K_p : Proportional Gain.

L_p : Flyback transformer primary winding self-inductance.

L_s : Flyback transformer secondary winding self-inductance.

n : The turn ratio of the flyback transformer.

N : Number of series cells or power diodes required to build PVE.

P_{mpp} : The maximum output power from PV emulator at V_{mpp} and I_{mpp}.

q : Electron charge, $1.60217646 \times 10^{-}19$ C.

R_o : The output resistance of the PV emulator.

R_p : The parallel resistance (Ω).

$R_{p,cell}$: The parallel resistance of the PV cell (Ω).

R_{peq} : Equivalent parallel resistance (Ω).

R_{PV} : The output resistance of the real PV system.

R_s : The series resistance (Ω).

$R_{s,cell}$: The series resistance of the PV cell (Ω).

R_{seq} : Equivalent series resistance (Ω).

T : The PV module Temperature.

$\triangle T$: The temperature variation.

T_n : The temperature at the Standard Test Condition is 298 kelvin or 25 °C.

T_s : The switching time period.

V_D : Diode forward voltage (V).

Vin : The input DC voltage source.

V_{mpp} : The voltage at the maximum power point.

V_o : The output voltage of the PV emulator.

V_{oc} : Open-circuit voltage.

$V_{oc,n}$: The open-circuit voltage at STC.

V_{PV} : Output voltage of PV (V).

V_t : Thermal voltage of the diode.

$V_{t,n}$: The PV cells thermal voltage at the nominal temperature T_n at STC.

Chapter 1

Introduction

1.1 Overview

Recently, due to the increase in energy demand, environmental issues, and the scarcity of traditional energy sources, the world is moving towards renewable energy sources (RESs), such as wind, solar, geothermal, biomass, and hydropower energy. Based on an overwhelming need for energy, renewable energy sources generating electricity have increased dramatically in recent years. Renewable energy has been the fastest-growing energy source because it is plentiful, environmentally friendly, and efficient [1, 33]. The electricity generated from renewable energy sources grows by 2.9% yearly [34]. However, the total electricity produced based on the world's renewable energy sources in 2012 equals 22% of the total world demand. Hence, it is proposed that this will rise to almost 29% by 2040 [35]. The photovoltaic (PV) has seen significant growth in the last decades among renewable energy sources for different reasons, including the wide availability of the PV system technology; its long life span, easy installation, and low maintenance; its clean energy and distribution over the earth; and good government incentives such as tax credits. It participates as a primary factor of all other processes of energy production on earth [1,36,37]. In 2020, solar energy had another record-breaking year, with new installations reaching approximately 139GW. This brought the global total to about 760GW, including both on-grid and off-grid capacity [1], as seen in Fig. 1.1.

Moreover, despite the phenomena of reflection and absorption of sunlight by the atmosphere, it is estimated that solar energy incidents on the earth's surface are ten thousand times greater than the world energy consumption. A significant advantage of solar power is the reduction of carbon dioxide emissions. By the year 2030, the annual reduction rate of CO2 due to the usage of PV cells may be around 1Gton/year. According to experts, the energy obtained from PV cells will become an essential alternative renewable energy source until 2040 [1]. Despite all advantages presented by the generation of energy through PV cells, the efficiency of energy conversion is currently low. The initial cost for their implementation is still considered high; thus, it becomes necessary to use techniques to extract the maximum power from these panels to achieve maximum efficiency in operation. The maximum power

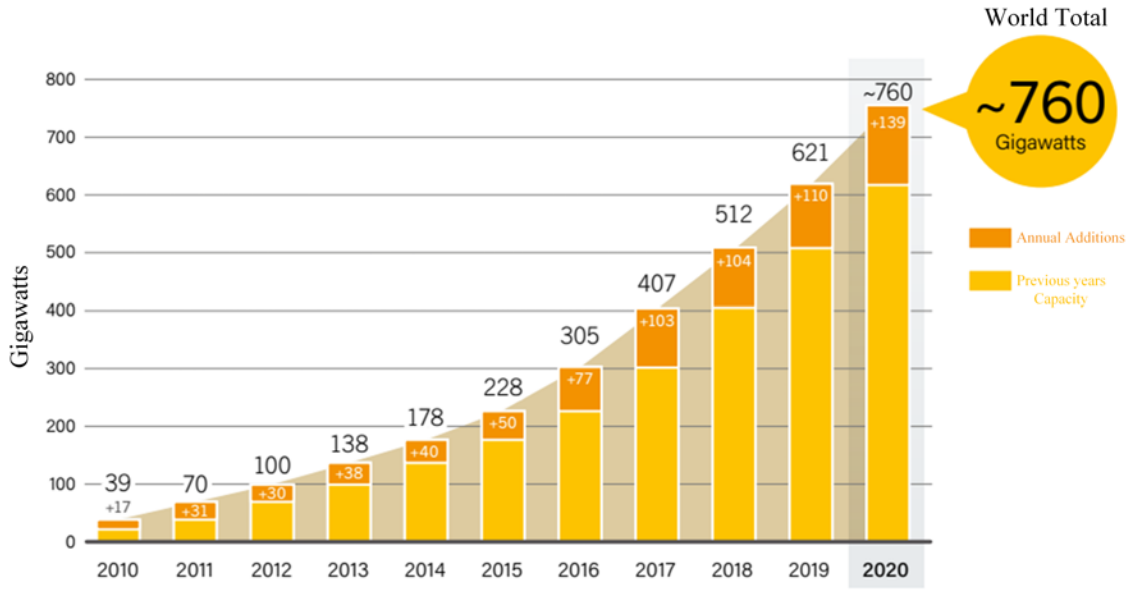


Figure 1.1: Solar energy capacity and annual additions during the years 2010-2020, all over the world [1].

point tracking (MPPT) algorithms are widely used, especially for partial shading conditions. Many MPPT techniques have been reported in recent years, such as fraction open-circuit voltage (FOCV), hill climbing (HC), fraction short-circuit current (FSCC), perturb and observe (P&O), and incremental conductance (InC) [30, 38]. In this thesis, PV panels are used, and the P&O algorithm is selected for its ease of implementation.

The PV system parameters are divided into internal and external. The internal aspects of the PV system include the number of cells linked in either series or parallel collections and the type of the fabrication material such as copper indium gallium selenide (CIGS), silicon (Si), gallium arsenide (GaAs), and cadmium telluride (CdTe) [39]. The external parameters include the number of combination PV cells in a string and the number of strings linked together in parallel using a junction box. The PV system measurement parameters basically include the short-circuit current I_{sc}, open-circuit voltage V_{oc}, voltage, current, and power at the MPP (maximum power point) V_{mp}, I_{mp}, and P_{mp}, respectively [30, 38].

The use of a real PV system is not recommended to thoroughly test the ability and guarantee the robustness of the power electronics. A large area and costly testing facilities of actual PV modules are needed [40, 41]. In addition, issues come from incompatible and challenging forecasting fluctuating operating conditions including solar irradiation and ambient temperature [26]. Due to the rapid increase in research and development in renewable energy systems in recent decades and the intermittent nature of most renewable energy sources that produce inconsistent testing and design conditions, different types of renewable energy emulators have been proposed to mimic the realistic behaviour of renewable energy sources [26, 30]. They are used to facilitate the development of modern and emerging power systems, such as the DC microgrid. Power electronic systems are the enabling technology to interface with these sources and integrate them into the electricity grid. However, to facilitate the testing platform of these power electronic systems, energy emulators based on the power electronics system must be developed. Solar PV emulators have been helpful for indoor testing and provide a convenient tool to develop solar PV power systems and related products. The PV emulator (PVE) is a power conditioning system, which is used to emulate the static and dynamic behaviours of the actual solar cell, panel, or array [42–44]. It is also used to test and verify various MPPT algorithms and mimic partial or total shading scenarios [37].

1.2 PV System Working Principle and Structure

The PV cell is a semiconductor material (PN-junction) used to convert solar irradiation power to electrical power by the photovoltaic impact [45, 46]. In the PV cell, the positive P-type layer and the negative N-type layer are joined together to form a PN-junction, and once it is exposed to the solar radiation, the electrons start moving and generating direct current, as shown in Fig. 1.2 (a). Harvesting the maximum amount of power from the PV system requires studying the behaviour and characteristics of the basic elements used to build the solar system, which is the PV cell. However, the relationship between the current and voltage generated from the PV cell presents the nonlinear I-V and P-V curves, as shown in Fig. 1.2 (b). The I-V performs the relationship between current and voltage. In addition, the P-V curve

represents the relationship between current and power, where the power comes from multiplying the current by the voltage at each operating point. The x-axis shows the voltage of the PV cell for both the I-V and P-V curves, where it has a value range between zero, if there is no solar irradiation, to the open-circuit voltage V_{oc}. Hence, the y-axis represents the solar cell current for the I-V curve, where it has a value range between zero to the short-circuit current I_{sc}. Furthermore, the y-axis for the P-V curve represents the generated power, where its value range is between zero to the maximum power point P_{mpp}, as shown in Fig. 1.2 (b) [30, 38].

The amount of power that is generated from a single solar cell is small. Therefore, some PV cells with similar electrical characteristics are connected electrically in series and/or parallel circuits to harvest higher voltage, current, and power levels. PV modules consist of PV cell circuits closed in an environmentally protective plate and are the principal building blocks of PV systems. A PV panel consists of one or more PV modules assembled as a pre-wired, field-installable unit. However, if more than one PV module is connected in series, they will form a string. A PV array is the whole power-generating system, consisting of any number of PV strings connected in series or parallel collections. Fig. 1.3 shows the variance between the PV system structures, namely the cell, module, string, and array.

1.3 Applications of PV Power Systems

The PV power systems are classified into two main categories, namely the stand-alone PV power system and the grid-connected PV system through DC/AC micro-grids [47, 48], as shown in Fig. 1.4.

1.3.1 Off-grid or Stand-alone PV System

The off-grid or stand-alone power system is defined as a system that generates electricity independently through various RESs, such as wind turbines, biomass, hydropower, PV panels, etc. A PV stand-alone system consists of a PV system as the electricity generation component, a control system for the power passing management, and regulators for the demands. However, some PV stand-alone systems use

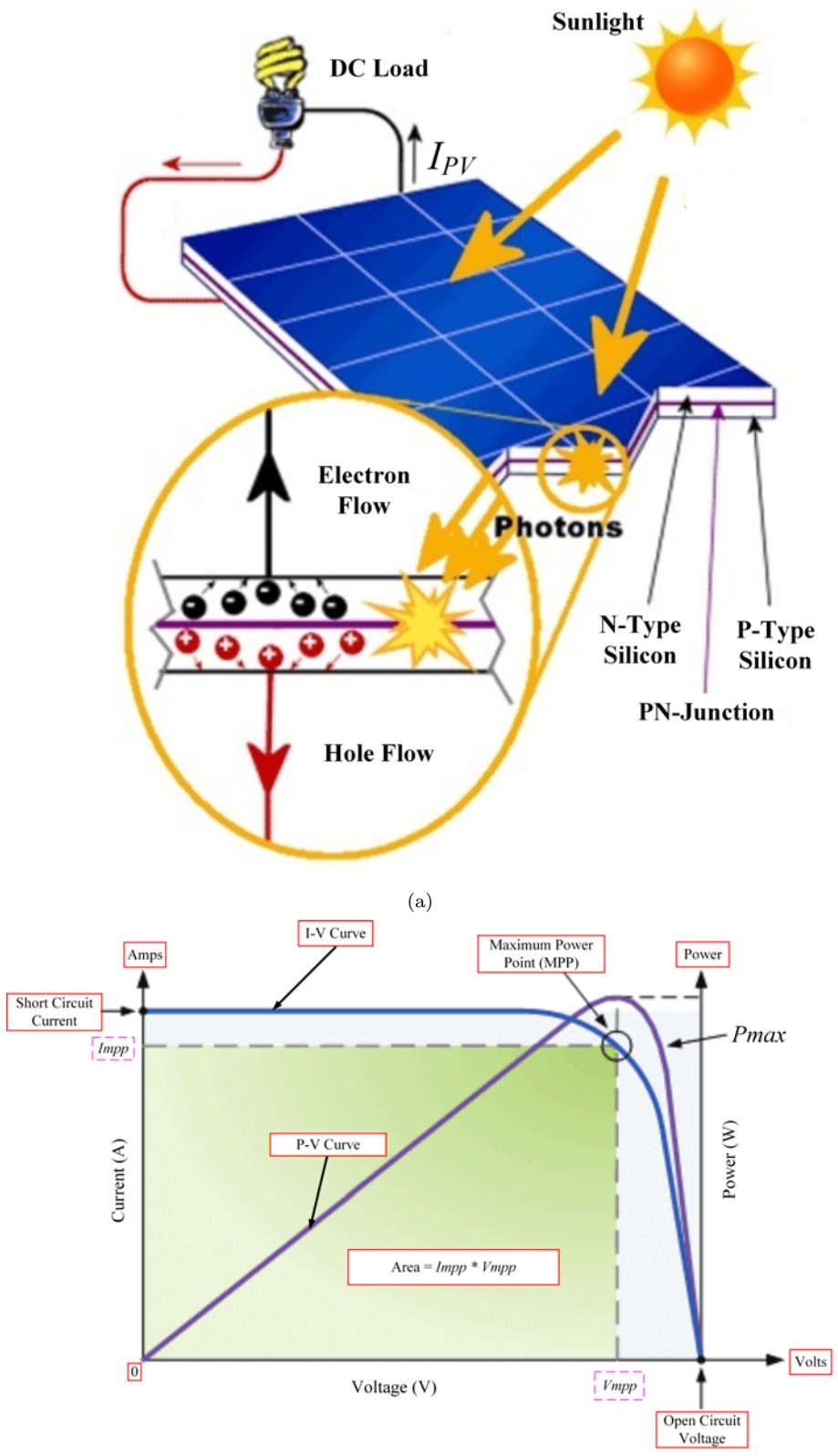


Figure 1.2: The PV cell: (a) Structure and (b) I-V and P-V curves.

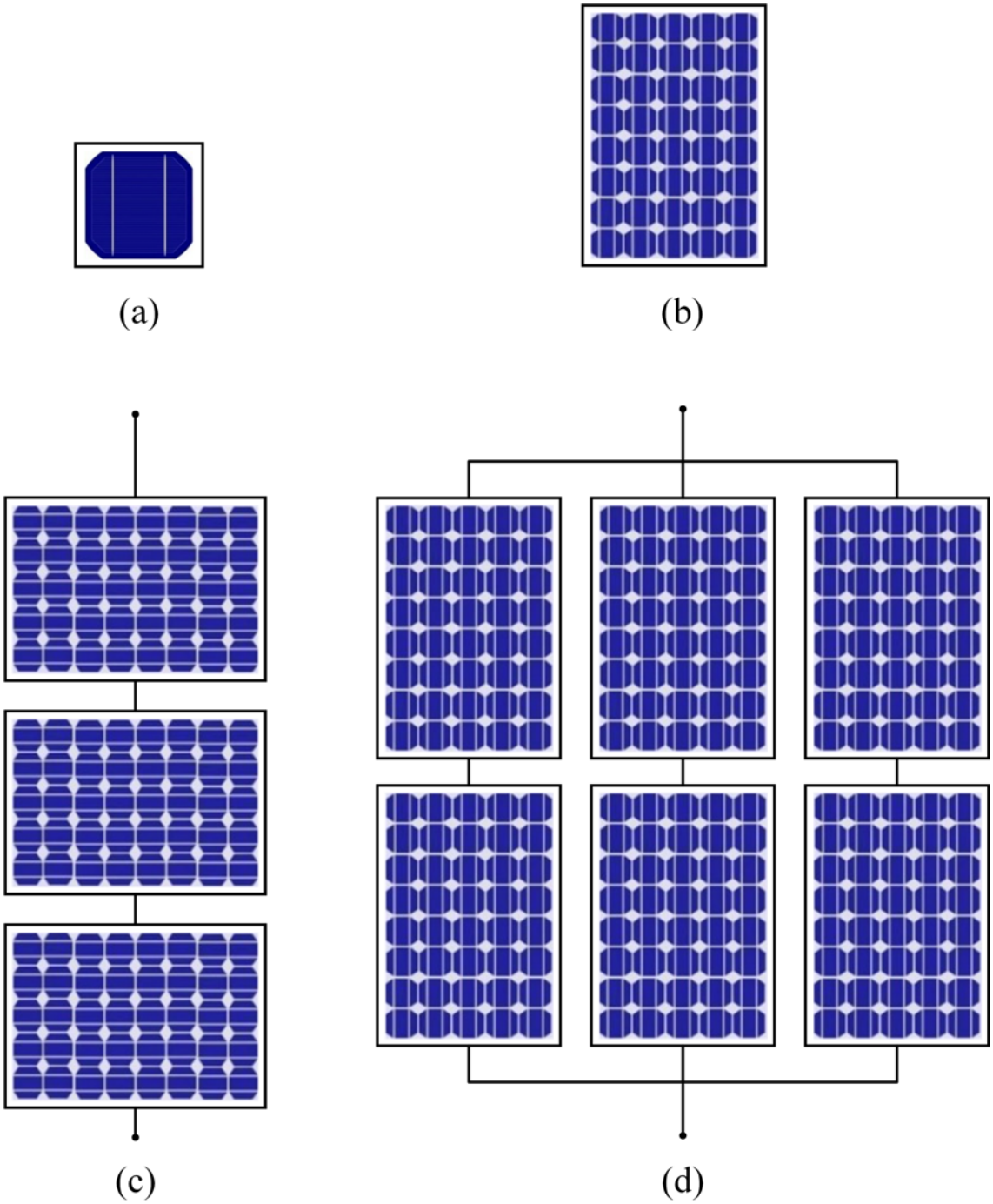


Figure 1.3: PV system structures: (a) Cell, (b) Module/Panel (cells in series), (c) String (modules in series), and (d) Array (Strings in series or parallel combinations).

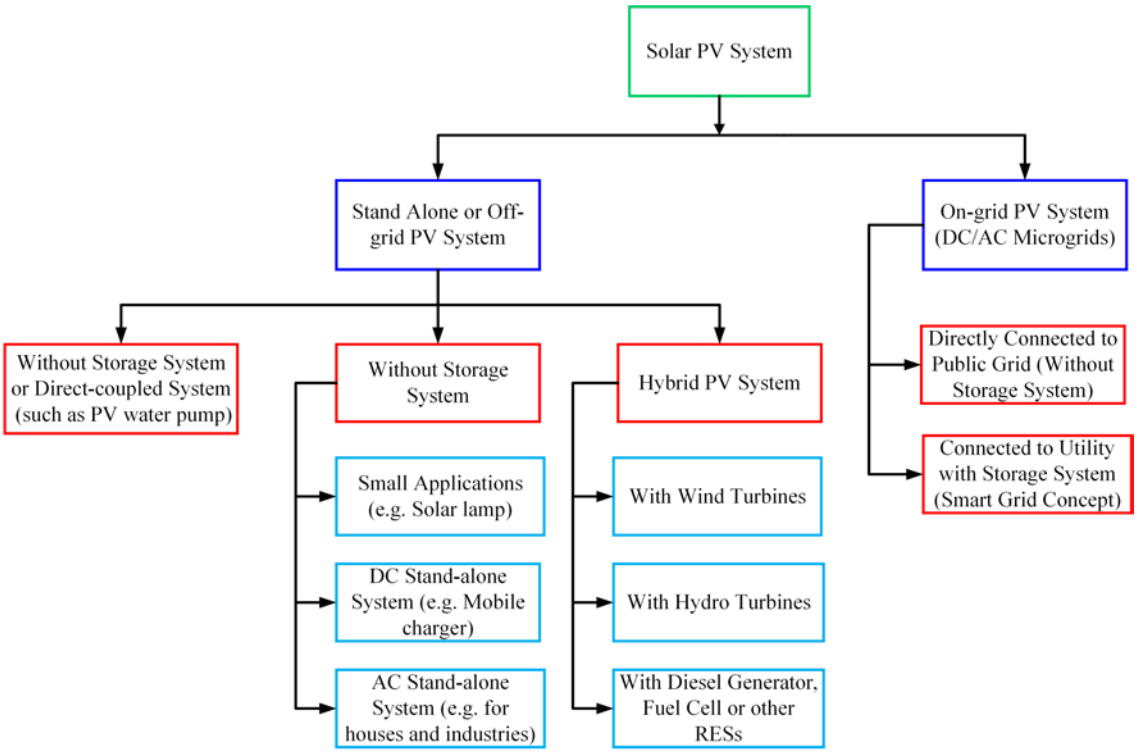


Figure 1.4: The PV power system classification in terms of applications.

a battery as an energy storage device. This system is useful for various applications, such as space, solar vehicles, solar water pumps, road and emergency signs, etc. In addition, it is suitable for distant or rural areas where the utility grid cannot be extended due to both economic viability and geographical constraints [49, 50].

1.3.2 On-grid PV System

The use of the RESs into the utility grid increases day by day [50,51]. Unfortunately, due to the intermittence of the different RESs that are directly linked to the utility grid, the grid stability is affected over time [49]. AC/DC microgrids are used to solve this issue. They are well-suited to connect the RESs with the utility grid. The microgrids are defined as local distribution systems which integrate distributed generation units, such as traditional power sources, RESs, storage systems, and load together with an AC/DC bus [49, 50]. Fig. 1.5 shows the typical distributed generation units connected with AC/DC microgrids. However, they are able to work

on or off-grid mode. Usually, the off-grid scenario occurs when a fault happens at the AC or DC bus bar, through uniform power plant servicing or during a blackout.

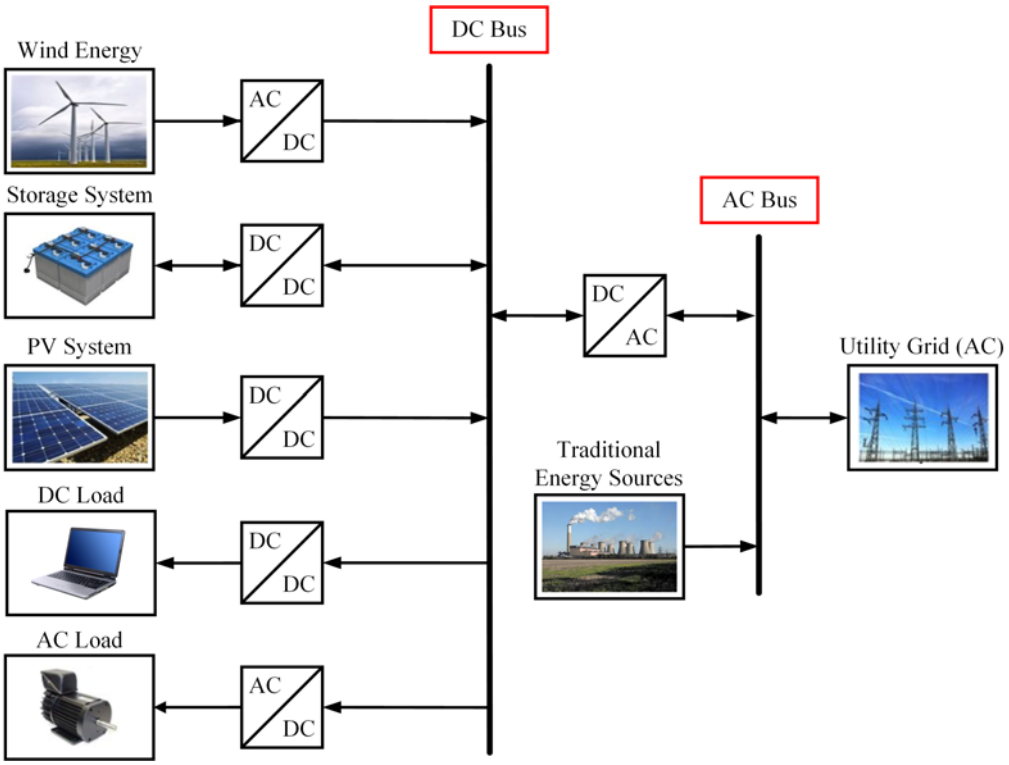


Figure 1.5: AC/DC microgrids structure.

1.4 Design Requirements of PVEs

PVEs come in various implementations but depend mainly on switching converters for power output capabilities. Since PV modules are linked to dynamic loads through inverters and maximum power point (MPP) trackers, much work was done to enhance the performance of the PV emulated output. When choosing or constructing a PV simulator, the following characteristics are of considerable importance:

1. The PVE device has the ability to mimic any PV system within the output limits.
2. It should simulate the behaviour of the real PV system under different operating conditions, such as various temperature, irradiance, and partial shading (PS).

3. It should have modularity and portability.
4. It has no need of a direct cooling system, indicating its high efficiency.
5. It has an acceptable dynamic response compared with the real PV system.
6. It has the ability to test solar system elements such as inverters and MPPT.

1.5 Research Motivation

The photovoltaic emulator is a power conditioning system designed to mimic a nonlinear behaviour of the existing PV system and facilitate energy systems testing and analysis, such as MPPT and the partial shading effect. Unfortunately, existing solutions usually require a sophisticated hardware design, which is costly, and fast computing. Moreover, the dynamic response is slower than the actual PV system. In [52], the authors introduced this application through a hardware platform consisting of a DC constant current source, a power diode string, and two resistors. However, it lacks the details explaining how to design the diode string. Based on the similarity of electro-thermal behaviour between the diodes and a real PV cell, the PVEs used in this model have high potential to achieve a better response for both dynamic and steady-state, which was not confirmed in [52]. The authors of [31] presented a PVE that depends on a transistor string instead of the diode string, where the number of components is greatly reduced. However, both diode and transistor-based solutions have a common high power loss problem, where the worst-case scenario occurs at the open-circuit voltage operating condition and a solution has not been provided yet. In addition, the potential and practicality of the PVE based on the PV equivalent circuit model have not been fully explored, such as the parametric extraction of a real PV panel for the design of diodes or transistors, converter architecture, and the DC constant current source dedicated to this application, and the modification of equivalent circuit model to mimic the partial shading condition. Furthermore, the electro-thermal behaviour of the PVE that uses the one-diode model has not been studied. Based on these reasons, this research presents a simple, reliable, and effective circuit-based PVE based on the equivalent PV stacked cells from different design aspects.

1.6 Dissertation Outline

An overview of the PV system and the PVE requirements are stated in the previous sections. According to the literature survey, there is space to improve the accuracy, efficiency, dynamics, steady-state response, cost and reduce the design size of the PVE system based on a physical single-diode PV model. This dissertation consists of seven chapters, all geared towards the main objective of this work, improving the design of the PVE system. The organization of this thesis is listed as follows:

In Chapter 2, a literature review of the existing PVE system is presented. The literature review includes the main parts of the PVE, namely, the PV model system, the power stage, and the control system. Each is classified and studied from different perspectives by drawing examples from the academic literature review and commercial products. The purpose of this chapter is to summarize the benefits and drawbacks of the existing PVE systems. The main problem with the PVE device in both the literature and the market are the high prices and the large volume of the emulator system. However, it is shown that no one has designed and clearly studied the PVE based on a physical equivalent PV-cell model. Therefore, a physical PV model using a single-diode PV model is selected as a final PVE design.

Chapter 3 presents a simple, reliable, and effective circuit-based PVE based on the equivalent PV stacked cells. The proposed approach has been built based on the key design equations. The I-V and P-V characteristic curves of the emulator have been generated using an LTspice simulator. The PVE is experimentally studied and compared with an actual PV panel and existing emulator products. The experiment results show good agreement with the actual PV panel. The proposed PVE shows a better dynamic response and shorter settling time than several benchmarked commercial products. The increase in the time response is due to the simplicity of the emulator, in which a few power diodes and some resistors are used. Although it is power efficient at the MPP, it suffers from high power loss around and at the open-circuit voltage (OCV) operation condition. In addition to simplicity, the PVE is very cost-effective. The thermal issue related to the diode string has been investigated and solved by adding a variable speed fan cooling system. Then, series

combinations of PV cells are used to investigate and mimic the real PV system under the partial shading effect. In addition, a boost DC/DC converter loaded with a perturbing and observe (P&O) algorithm is used to test and evaluate the proposed PVE platform.

As Chapter 3 demonstrates, a simple one-diode PVE consists of a DC constant current source, diode string, and some resistance. Chapter 4 presents a DC constant current source design for the PVE applications. This study focuses on the selection criteria of the constant current source converter (CCSC), and controller designs are explained. The CCSC is constructed based on a series combination of flyback and buck DC/DC converter. The CCSC simplifies the converter and controller designs as it operates at a fixed point for each insolation level, as compared with a converter-based solution which requires a voltage-source converter with wide output operating ranges. The proposed current source test and verification is based on the MATLAB/SIMULINK program. An experimental prototype is also designed to validate the proposed approach. In addition to steady-state operation, the dynamic response of series-connected cells is also emulated to verify the effectiveness of the proposed platform. The response time of the proposed emulator system is comparable to both a benchmarked commercial product and a real PV system.

Based on the previous work in Chapter 3, the proposed PVE has shown a superior dynamic performance that is compatible with that of an existing PV system. However, it suffers from high power loss where the worst-case scenario occurs at the OCV operating condition. Moreover, the overall system efficiency is low even using the variable speed fan to reduce and control diode string temperature. Therefore, Chapter 5 presents two new hybrid solutions, i.e., topologies A and B, that consist of placing a switching circuit (SC) in parallel with the diode string to minimize power loss and increase system efficiency. The switching circuit consists of a two-switch non-inverting buck-boost DC/DC converter. When the operating point of the PVE moves from the current source region to the voltage source region, the SC starts to work, which is more efficient, to replace the diode string seamlessly to maintain the circuit operation of the emulator. Experimental results show that in addition to

reducing the operating temperature of the diode string, the proposed solutions show a significant improvement in terms of efficiency compared with the DC fan-based solution.

As mentioned before, i.e., Chapter 3, the PVE implemented depends on the physical equivalent PV-cell model. The authors of [31] proposed a PVE based on a transistor string instead of the diode string to design a PVE in which the elements are greatly reduced. However, both diode and transistor-based solutions have a common high power loss problem, where the worst-case scenario happens at the OCV operating condition [31, 40, 44]. This issue is mentioned in [31], but a practical solution has not been provided yet. Furthermore, as briefly mentioned, it is not certain how the transistor string is designed to emulate the electrical characteristics of a selected PV system with high accuracy. In Chapter 6, firstly, a PVE has been designed based on the key design equations. In addition to the work shown in [31], the thermal problem related to the transistor string has been studied and investigated. This problem was solved by adding a DC variable speed fan that works as a cooling system, and with this approach, the total temperature of the proposed PVE is reduced, but the system efficiency is still low. Secondly, this chapter uses the hybrid solution, i.e., topology B, introduced in Chapter 5 to enhance thermal behaviour and improve total system efficiency. In addition to the control method shown in Chapter 5, a new control strategy is implemented to handle the tradeoff between the thermal and dynamic performances of the proposed solution.

Finally, Chapter 7 gives the conclusions and suggestions for future work.

Chapter 2

Review of Existing PV Emulator Systems

2.1 Overview

The PVE consists of three main parts: the PV model system, the power stage, and the feedback control system, as shown in Fig. 2.1 [3]. There are two types of the PV model system in the literature, analog or digital representations. It is used to generate the current-voltage characteristic of the actual PV system (real PV cell, panel, or array) for the PVE, and it impacts the accuracy of the PVE output and the desired capability of the hardware platform required for the PVE. The real PV cell [4], an analog circuit [5], a series-diode stack [6], and a photosensor [7] are examples of a PV model reference based on analog representations. The digital implementation methods are generally more flexible during parameters changes, such as temperature and irradiation level [8–10].

The second part is the power stage, which produces an output similar to the I-V characteristic of the real PV system. It also affects the PVE's dynamic response and efficiency. The power stage is classified into two main categories, namely, the switched-mode power supply (SMPS), and the linear regulator. The switching DC/DC converter-based PVEs have used various DC/DC converter topologies, such as buck [23, 28], buck-boost [20, 30], and forward [29]. There are several drawbacks of PVEs based on the SMPS topologies, for example, higher-order converter dynamics, harmonic intermodulation, and potential instability come from interactions with other power electronics systems such as MPPT converters during switching frequency and the PV inverter. The linear-based PVEs [8, 31, 32] have a stable response, and they do not have higher-order transients compared with the switching-based PVEs. In addition, the quantization issue can be eliminated when the analog controllers method is used. However, the analog-based controller is not as flexible in tuning model parameters under different operating conditions (e.g. temperature, irradiation level) as PVEs based on digital controllers.

The third part is the feedback control system, which connects the PV model system with the power stage to turn out a PVE. The control system impacts the accuracy, dynamics, and steady-state response of the PVE. The main task of the control system is to find the accurate operating point of the PVE on the characteristic

curve of the real PV system. Moreover, the perfect control system is robust, giving an accurate and steady operating point without any effect on both the power stage design and PV model system. Based on the literature, the control system can be divided into analog and digital [19]. The analog controllers are usually built based on the operational amplifiers (op-amps). Besides that, different controlling platforms such as DSPs [20–22], dSPACE [23, 24], FPGAs [25, 53], microcontrollers [26–28], and ARM processors [29] are used to implement the digital control.

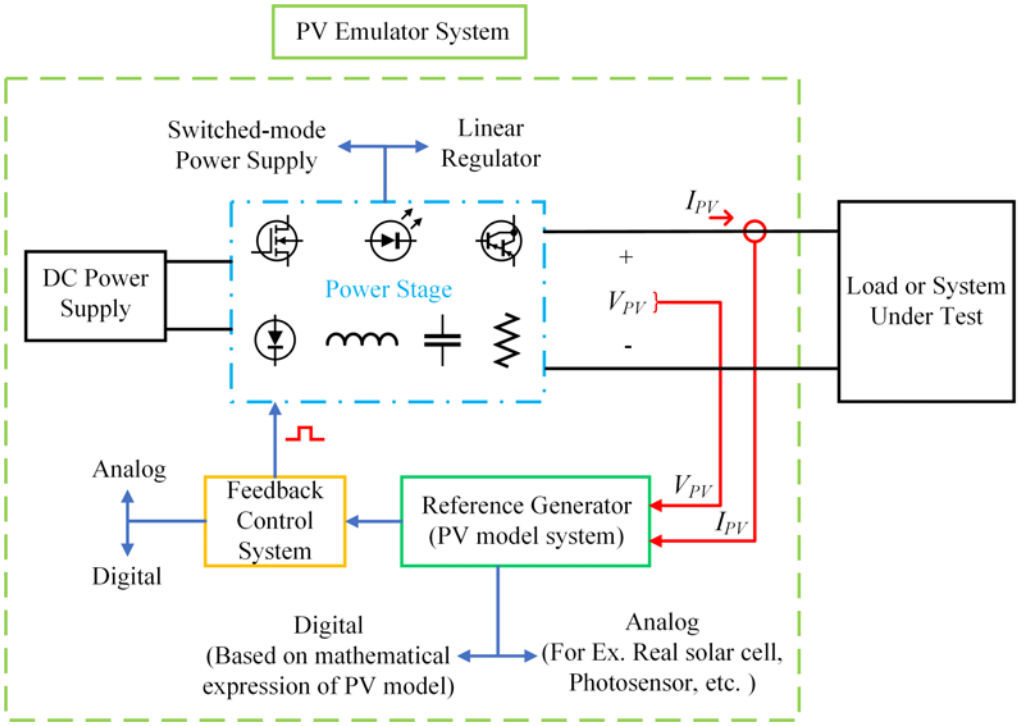


Figure 2.1: An overview of the PV emulator's main parts.

2.2 PV Model System

The PV model system is classified into two major types, namely the model type and the implementation method [3, 42]. The model type is divided into two types, which are the electrical circuit model and the interpolation model, as seen in Fig. 2.2. The electrical circuit model has some of the design topologies: listed, such as the diode characteristic, the simplified model, the parameter extraction, and the environmental factor. The second PV model type is the implementation method.

This method is responsible for achieving the PV model inside the PVE controller unit. The implementation method is categorized into five types: the direct calculation method, the piecewise linear method, the look-up table method, the PV voltage elimination method and the neural network method, as shown in Fig. 2.2.

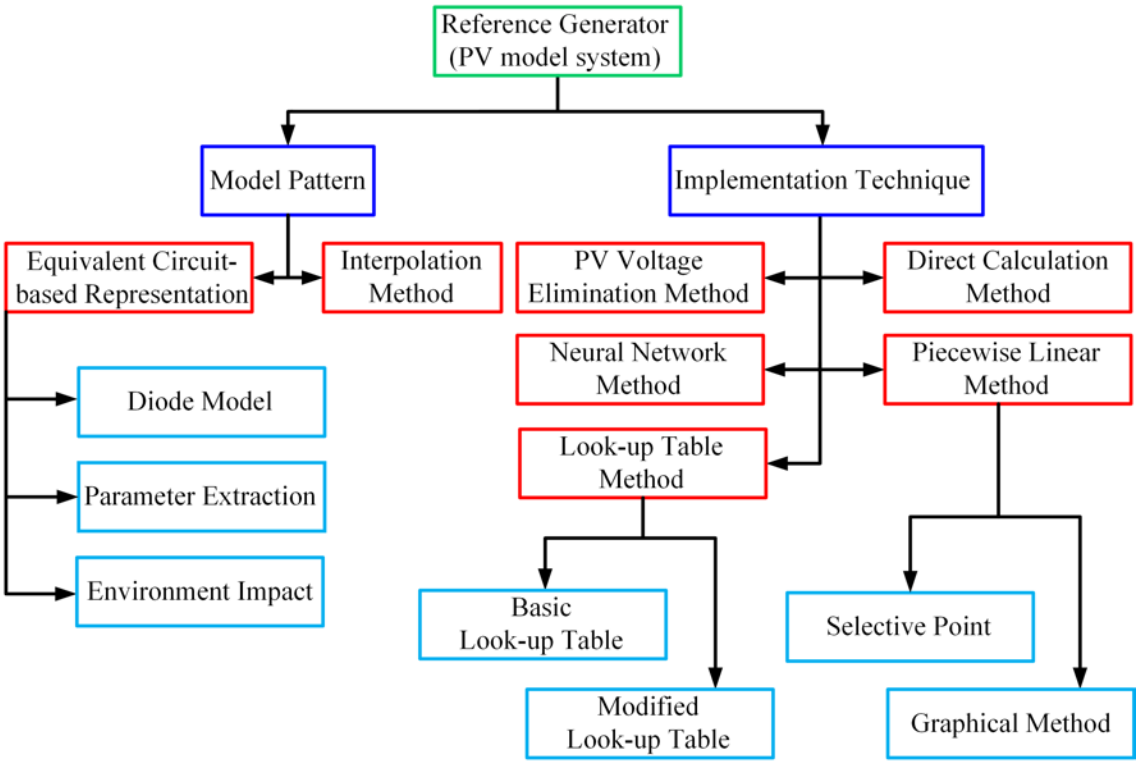


Figure 2.2: The PV model classification.

2.2.1 PV Model Pattern

2.2.1.1 Equivalent Circuit-based Representation

The PV modelling represented in an electrical circuit, commonly used in the PVE design system, is known as the electrical circuit or analytical model. Furthermore, the Kirchhoff current law (KCL) is used to derive the PVE's characteristic equation. Based on the number of diodes used on the PVE, the electrical circuit can be classified into three popular types: the single diode model, the two diode model, and the triple diode model, as shown in Fig. 2.3.

The ideal model, the one diode model or 1D model, is shown in Fig. 2.3 (a), the single diode with series resistance or 1D1R model is seen in Fig. 2.3 (b), and the ideal diode model with series and parallel resistance, the 1D2R model or the five parameters model is shown in Fig. 2.3 (c) [54,55]. The double diode (2D2R model) or the seven-parameter model is shown in Fig. 2.3 (d), and the triple diode model is shown in Fig. 2.3 (e) [54,55]. PV emulator designers use the single diode model to design a PV emulator because of its simple, acceptable and accurate design [53,54].

a) Diode Model

The PVE mathematical representations based on the equivalent circuits shown in Fig. 2.3 [54,55] and by applying KCL at the upper point are as follows:

The single diode, ideal, or 1D model equation is:

$$I_{PV} = I_{ph} - I_D \tag{2.1}$$

Or,

$$I_{PV} = I_{ph} - I_{s1} \times [exp(\frac{q \times (V_D)}{a_1 \times N \times K \times T}) - 1] \tag{2.2}$$

The single diode with series resistance or 1D1R model equation is:

$$I_{PV} = I_{ph} - I_{s1} \times [exp(\frac{q \times (V_{PV} + I_{PV} \times R_s)}{a_1 \times N \times K \times T}) - 1] \tag{2.3}$$

The single diode with series and parallel resistance or 1D2R model equation is:

$$I_{PV} = I_{ph} - I_D - \frac{V_D}{R_p} \tag{2.4}$$

Or,

$$I_{PV} = I_{ph} - I_{s1} \times [exp(\frac{q \times (V_{PV} + I_{PV} \times R_s)}{a_1 \times N \times K \times T}) - 1] - \frac{(V_{PV} + I_{PV} \times R_s)}{R_p} \tag{2.5}$$

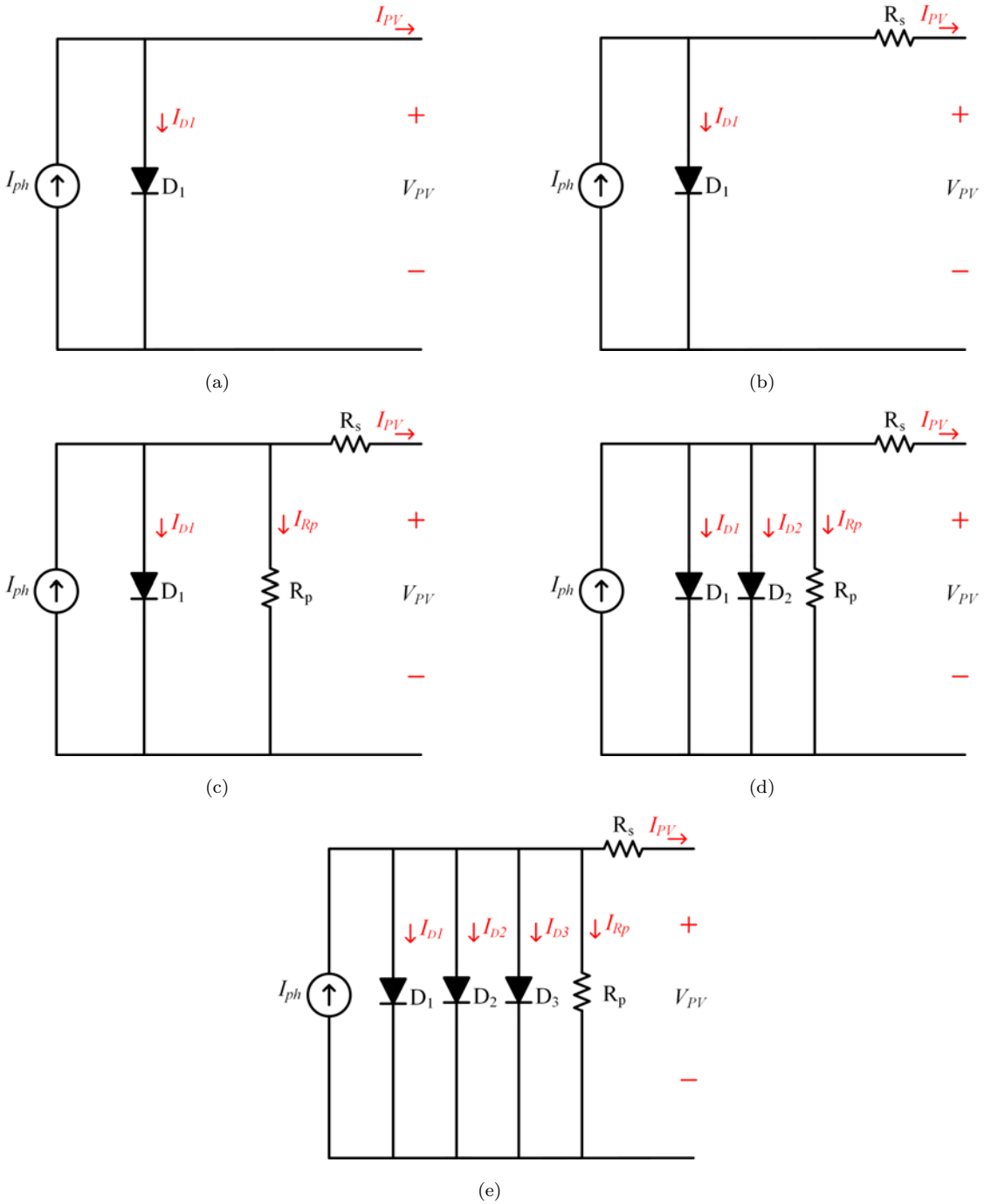


Figure 2.3: The PVE equivalent circuit: (a) The ideal model or ID model, (b) The single diode with series resistance or 1D1R model, (c) The ideal model with series and parallel resistance or ID2R model, (d) The two diode with series and parallel resistance or 2D2R model, and (e) The triple diode with series and parallel resistance or 3D2R model.

The double diode with series and parallel resistance or 2D2R model equation is:

$$I_{PV} = I_{ph} - I_{s1} \times [exp(\frac{q \times (V_{PV} + I_{PV} \times R_s)}{a_1 \times N \times K \times T}) - 1] \\ - I_{s2} \times [exp(\frac{q \times (V_{PV} + I_{PV} \times R_s)}{a_2 \times N \times K \times T}) - 1] - \frac{(V_{PV} + I_{PV} \times R_s)}{R_p} \tag{2.6}$$

The Triple diode with series and parallel resistance or 3D2R model equation is given by:

$$I_{PV} = I_{ph} - I_{s1} \times [exp(\frac{q \times (V_{PV} + I_{PV} \times R_s)}{a_1 \times N \times K \times T}) - 1] - I_{s2} \times [exp(\frac{q \times (V_{PV} + I_{PV} \times R_s)}{a_2 \times N \times K \times T}) - 1] \\ - I_{s3} \times [exp(\frac{q \times (V_{PV} + I_{PV} \times R_s)}{a_3 \times N \times K \times T}) - 1] - \frac{(V_{PV} + I_{PV} \times R_s)}{R_p} \tag{2.7}$$

$$V_t = \frac{N \times K \times T}{q} \tag{2.8}$$

Table 2.1 provides the descriptions of the parameters of the PV emulator. PVE researchers have used the I_{s1} to represent the diffusion mechanism and I_{s2} to study the recombination effect produced by diode 1 on the PVE behaviour, where the three-diode model is used to have the influence of impact, which is not theorized by the previous models [54]. The PVE equivalent circuit can be simplified to the 1D1R model by ignoring the parallel resistance effect [54], and setting the value of R_p in Eq. 2.5 to infinity. The new circuit illustration is shown in Fig. 2.3 (b). Some of the PVE designers used the 1D model [54], which ignores both the series and parallel effects, as shown in Fig. 2.3 (a). The PVE characteristic equation using the 1D model can be rewritten, as seen in Eq. 2.2. However, based on the large effect of the series resistance on the PVE output accuracy, the 1D model is usually not used to represent a real solar cell [54].

Table 2.1: Descriptions and parameters of the PVE

Parameter Name	Parameter Description
I_{ph}	Photocurrent (A)
$I_{PV} \cong I_{sc}$	Short circuit current or Output PV current (A)
V_D	Diode forward voltage (V)
R_s	Equivalent series resistance (Ω)
R_p	Equivalent parallel resistance (Ω)
I_D	Diode forward current (A)
I_{s1}	Reverse saturation current (A) for diode number 1
I_{s2}	Reverse saturation current (A) for diode number 2
I_{s3}	Reverse saturation current (A) for diode number 3
q	Electron charge, $1.60217646 \times 10^{-}19$ C
T	Temperature of the p-n junction (Kelvin)
K	Boltzmann constant,$1.3806503 \times 10^{-}23$ ($\frac{J}{K}$)
a_1	Ideal factor for diode 1
a_2	Ideal factor for diode 2
a_3	Ideal factor for diode 3
V_{PV}	Output voltage of PV (V)
N	Number of series cells or power diodes required to build PVE
V_t	Thermal voltage of the diode

b) Parameter Extraction

The PVE designer used the parameter extraction or parameter guess method to calculate the unknown PVE parameters required to complete the emulator design of the five parameter model, I_{ph}, I_{s1}, R_s, R_p, and a_1, if these values are not given from the manufacturer data sheet [54]. The emulator parameters can be found by two methods, firstly, by using certain values located from the current-voltage and power-voltage curve of a real PV cell, such as the open circuit voltage (V_{oc}), the maximum power voltage (V_{mpp}), the short circuit current (I_{sc}), and the maximum power current (I_{mpp}) [56]. The second method depends on an algorithm representation of the real PV cell's characteristic curve [57, 58]. The hybrid firefly and pattern search algorithms [59] and the particle swarm optimization [57] are examples of this method.

c) Impact of the Environment

The real PV system datasheet contains the parameter values at the standard test condition (STC), where the solar irradiance, G_n, is $1000W/m^2$ and the temperature, T_n, is 298 Kelvin or 25°C. In addition, some manufacturers give the parameter values at a different operating condition called the nominal operating cell temperature (NOCT), where the irradiance level is $800W/m^2$ and the temperature is 20°C [60]. The estimated photo-generated current depends on the value given by the manufacturer listed as V_{oc}, I_{sc}, V_{mpp} and I_{mpp}. The generated value is based on the irradiances and the temperature of the real PV system. The I-V and P-V characteristic curves of the PV module are affected by temperature variation. The I_{sc} increases, the V_{oc} decreases and the P_{mpp} decreases as the temperature increases [54, 57]. As a result, the photo-generated current (I_{PV}) is directly proportional to the solar irradiance level and is also affected by the temperature value according to the following mathematical equation [59, 61]:

$$I_{ph} = (I_{ph,n} + K_I \triangle T)\frac{G}{G_n} \tag{2.9}$$

where $I_{ph,n}$ is the light-generated current at the standard test condition (STC), and $\triangle T$ is the temperature variation, which can be defined by (2.10), K_I is the PV cells's short circuit current temperature coefficient, G $[W/m^2]$ is the irradiation density at the PV cell surface and G_n is the irradiation at the STC.

$$\triangle T = T - T_n \tag{2.10}$$

where T and T_n are the actual and temperatures at the STC $[K]$, respectively.

Based on (2.11), the saturation current (I_{s1}) is affected by the module temperature and is not affected by the irradiance. The thermal voltage (V_t) is directly proportional to the temperature increase, as seen in (2.8).

$$I_{s1} = I_{s1,n} \times (\tfrac{T_n}{T})^3 \times exp[\tfrac{qE_g}{aK}(\tfrac{1}{T_n} - \tfrac{1}{T})] \tag{2.11}$$

where E_g is the band-gap energy of the semiconductor material and $I_{s1,n}$ is the nominal reverse saturation current given by the following equation:

$$I_{s1,n} = \frac{I_{sc,n}}{exp[\frac{V_{oc,n}}{aV_{t,n}}]-1} \tag{2.12}$$

where $I_{sc,n}$ is the short circuit current at the STC. $V_{oc,n}$ is the open-circuit voltage at the STC. $V_{t,n}$ is the PV cells's thermal voltage at the nominal temperature T_n at the STC.

2.2.1.2 Interpolation Method

The second type of PV module is the interpolation model. This type is able to generate the PV characteristic curve. The interpolation model has different types used in the PVE [62]. This method is based on the mathematical function that intercepts the I_{sc} and V_{oc}, using the photovoltaic voltage as an input and the PV generated current as an output. Based on this method, the different PV characteristic curves will be generated at various irradiance and temperature values. The PV interpolation model needs a select point on the I-V characteristic curve. The accepted points are the I_{sc}, V_{oc}, V_{mpp} and I_{mpp} at the STC [59]. This model sometimes requires the value of series resistance (R_s) to calculate the other PVE parameters.

The electrical circuit and interpolation model are based on different concepts. The electrical circuit work is based on the PV module electrical characteristics, while the PV interpolation model work is based on the I-V curve. The electrical circuit uses the implicit equation which requires a numerical method such as the Newton- Raphson method to estimate the PV parameter value [29, 63]. The numerical method or the iteration solutions need a long time to reach the converged value, which means the electrical model takes more evaluation time compared with the interpolation model. Because the interpolation model does not have the iterative equation inside a model, the interpolation model requires a single step of calculation to reach a converged solution. On the other hand, the electrical model requires additional theoretical information, for example, the ideality factor, parallel resistance and series resistance. The theoretical parameters are found according to the parameter

extraction technique. This technique takes a complex mathematical equation and high evaluation power. This complex process does not occur inside the PVE controller but is done outside then uses the parameter value to build the emulator, such as the use of the MATLAB program to solve these complex equations. The interpolation model does not need the parameter extraction process. The interpolation model needs other parameters such as the open-circuit voltage and the short circuit current at both the STC and other conditions. The PV cell manufacturer does not usually give this data. The interpolation model contains an internal parameter, and the trial-and-error method is used to determine its value. The electrical circuit model is more popular than the interpolation model because the electrical circuit model can emulate the real electrical characteristics of the PVE. The electrical circuit model has several designer shapes. Usually, researchers have used the 1D1R model [59, 64] and 1D2R model [65] to simulate the PVE because these two designs simply and accurately simulate the characteristic curve.

The high power from PVE is generated from a high irradiance level, and researchers have used the single diode model with the thick-film deposition technique to reach the high power requirements. The PV module build with the amorphous silicon structure does not display the same knee behaviour as the crystalline type, the I_{s1} due to the diffusion mechanism is assumed to be zero, as seen in (2.2) [66]. As a result, the 1D model is not used with polycrystalline silicon or during low irradiance conditions because the model does not display the space charge reconnected effects [66]. Based on the low solar irradiance and partial shading conditions, the double diode model has an accurate PVE simulation curve compared with the single diode model [67, 68]. The double diode model is also acceptable for both the monocrystalline and polycrystalline silicon used to build the PV module [66, 68]. The R_p does not have a large effect on the constant current (CC) region but only effects the constant voltage (CV) region [66, 69] of the single diode-series resistance model. The PVE usually operates between a constant current and a constant voltage region or around the MPP. Thus, the R_p does not have a crucial effect on the characteristic curve accuracy, and based on this point the designer used two PV

models, the 1D2R or the 1D1R.

Table 2.2 shows a comparison between the interpolation method and the equivalent circuit-based representation used for the PVE application in terms of the numerical solution, convergence time, implicit equation, accuracy, and theoretical parameter, with the equivalent circuit-based showing a high accuracy compared with the interpolation method.

Table 2.2: The interpolation method compared with the equivalent circuit-based representation [3–10]

Parameter	Interpolation Method	Equivalent Circuit-based Representation
Numerical solution	Not suitable	Suitable
Convergence time	Quick	Slow
Implicit equation	Wanting	Present
Accuracy	Low	High
Theoretical parameter	Usually not required	Required through parameter extraction

2.2.2 Implementation Technique

The reference signal of the PVE is found by executing the PV mathematical model inside the controller. The controller is highly loaded because the PV mathematical equation is complex. The PVE reference point calculation process is delayed, giving an inaccurate responses to disturbances. Based on the previous the calculation of the PVE in real time is very important. Therefore, the PVE designers look for an acceptable implementation method based on the control capability and the PV model complexity. The PV model is implemented into the PVE controller by using one of the five methods shown in Fig. 2.2.

2.2.2.1 PV Voltage Elimination Method

The PV voltage elimination method has two different characteristic equations used to generate a single characteristic curve. This curve is divided into two areas based on the critical load to eliminate the load of the photovoltaic emulator controller [12].

The PV voltage is assumed to be zero on the constant current (CC) region because the voltage change creates a small effect on the photovoltaic current. The CC area and the CV area are isolated by the sensitive load lines. These lines intersect on the PV characteristic curve which exists at a point 99% of the I_{sc}. The output voltage of the PV invests in the PV mathematical expression while the output current is lower than or equal to 99%. However, the voltage elimination method is used to minimize the processing load when the PVE works in a constant current area.

2.2.2.2 Direct Calculation Method

This method directly implements the PV model into the PV emulator controller. Furthermore, it usually uses the single diode-series resistance (1D1R) PV model [11,70] because the single diode-series resistance model is less complex than the 1D2R and 2D2R models and is more accurate than the 1D model. The single diode-series resistance model requires the theoretical parameter to create the PVE characteristic curve. The theoretical parameter is calculated by the extraction process [71], the curve fitting process [72] or from the datasheet [11]. Usually, the single diode-series resistance model is simplified to minimize the processing load of the controller. The 1D1R model's complexity comes from the equation of the diode current. The diode equation is improved and simplified to reduce the processing load into the controller [11, 14]. The simplified model only requires a selective point on the PV current/voltage characteristic curve and temperature coefficient at the open circuit voltage. In addition to modifying the diode current equation, another strategy exists for facilitating the current equation. The diode current equation contains the reverse saturation current of the diode itself, and the reverse saturation current has a high complex representation [71]. However, the reverse saturation current complexity can be minimized based on the available parameters listed, such as the temperature coefficient of the I_{sc} and open circuit voltage (V_{oc}) [73].

2.2.2.3 Neural Network Method

The neural network method for PVE implementation is uncommon, in which the memory size and the processing burden are based on the number of neurons used

[13]. Furthermore, it has low flexibility to update the I-V characteristic curve's value when the various kinds of a PV system are emulated [3, 13]. Usually, the characteristic curve points are gained either from the electrical circuit [14] at various loads, the irradiance or temperature and the experimental process [13]. The data is drilled offline before the neuron network PV model is created. The training method creates the photovoltaic hyper-surface in the current, voltage, irradiance and temperature operating area. Since the operating area has four dimensions, the number of neurons is an accurate selection. After the training procedure is completed, the neural network model is put inside the PVE controller. The growing neural gas network (GNG) is applied in an investigation of the neural network photovoltaic model [14]. The growing neural gas is grown from small networks. The GNG required the lower computational load match to the traditional multi-layer perceptron drilled by the support-publishing algorithm.

2.2.2.4 Piecewise Linear Method

The piecewise linear method is the curve-fitting approach using several segmented straight lines that keep track of the I-V characteristic curve for the PV module. This method needs at least two linear lines, the minimum number of lines applied in the photovoltaic emulator design [15]. On the other hand, the PV model accuracy increases by increasing the linear lines used [74, 75]. The piecewise linear method usually uses two approaches to derive the necessary equations. The selective point of the photovoltaic module is the first method. The selective point method depends on the manufacturer datasheet, as this method uses the short circuit current, open circuit voltage and MPP (maximum current and voltage) listed on the datasheet. Because the datasheet only provides these three points at the STC, this method can only create the I-V characteristic curve at the STC [15]. The piecewise linear method is enhanced by inserting the functions that impact the three selective points corresponding to the irradiance and temperature of the PV module [75]. Besides the available point, this method is capable of creating only two linear lines. The first line is from the short circuit current to the MPP, and the second line is from the MPP to the open circuit voltage [15, 74]. This method is improved by adding two more

linear lines to a suitable point to enhance the accuracy of the I-V characteristic curve [75]. The second way is to draw the straight line continuously on the I-V characteristic of the photovoltaic curve [74]. The minimum number of straight lines used is two and the maximum number used is five. However, during the operation of the PVE, the irradiance and temperature do not change.

2.2.2.5 Look-up Table Method

The look-up table (LUT) method is classified as one of the more popular methods used for the PVE application [17, 76]. The look-up table method uses several techniques and types to emulate the PV module characteristic curve. Basically, the look-up table has two major types: the I-V and the V-I. The I-V type uses the PV voltage as the input and the PV current as the output of the table, while the V-I has the PV current as the input and the PV voltage as the output of the table. Usually, the closed loop controller of the converter system for the PVE uses the output of the look-up table (LUT) as a reference signal. Researchers have improved the control method for the PVE that is based on both look-up types, the V-I and the I-V methods.

In addition, the improved method modified the input and output of the two types of look-up table to overcome the limitations of the simple look-up table. The V-R look-up table (PV resistance as the input and PV voltage as the output of the table) gives a more steady reference signal. The output current and output voltage are not simulated through the ripple of the output. The PV resistance array into the look-up table is calculated by dividing the PV output voltage over the PV output current [16]. The V and I-R type is another look-up table method. This type uses the PV resistance as the input, and the PV current and voltage as the output of the table. That means the voltage and current control signals are created based on the PV output resistance [17]. Researchers have developed a new look-up table method (P-V) to solve the compatibility problem together with an MPPT-based PV inverter [18]. Some of the look-up methods do not require the PV current or voltage. The characteristics of the diode are stored in the electrical circuit model using the look-up table. The dynamic irradiance manipulation is created without

the requirement of a sampling point from the characteristic curve for a different irradiance because the diode is not influenced by the irradiance. However, any change in temperature requires the reloading of the diode characteristic data from the look-up table.

Table 2.3 shows a comparison between the PV voltage elimination method, direct calculation method, neural network method, piecewise linear method, and look-up table method used for the PV emulator application according to various parameters, such as computational time, memory requirement, the ability to change the irradiation and temperature values, flexibility, and accuracy. Hence, as the look-up table method requires a low computational time, it was selected for use in this work.

2.3 Feedback Control System Strategies

The control strategy is responsible for finding the PVE operating point. It determines the voltage and current values by the I-V characteristic curve identical to the output resistance. This is different from the maximum power point tracking algorithm since the goal of the MPPT algorithm is to locate the highest point of the power on the P-V characteristic curve. Although the PV control method is a very important part of the emulator control system, researchers have rarely enhanced it. The control strategy using the PVE is clearly shown in Fig. 2.4. In addition, the partial shading and controller implementation methods used for the control unit are described at the end of the section.

2.3.1 The PV Emulator Control Method

2.3.1.1 Direct Referencing Technique

Usually, the control strategy uses the direct reference method for the PVE application. The direct reference technique is well known because it does not require extra algorithm to find the operating point for the PVE [6, 77]. This method is used not only by the SMPS but also by the linear regulator [78]. However, it is usually established in the PVE with the SMPS. This method is divided into two types based on the closed-loop method and the photovoltaic model used to emulate

Table 2.3: The comparison between different implementation methods used for the PV model [11–18]

Parameter	PV voltage elimination method	Direct calculation method	Neural network method	Piecewise linear method	Look-up table method
Computational time	High	High	Based on the number of neurons used	Low	Low
Memory requirement	Low	Low	Based on the number of neurons used	Low	Based on the number of points
Online G and T setting	Able	Able	Able	Usually unable	In discrete form
Flexibility	Depends on the PV model used	Depends on the PV model used	Low	Depends on the PV model used	Low
Accuracy	High	High	High	Low	Based on the number of points

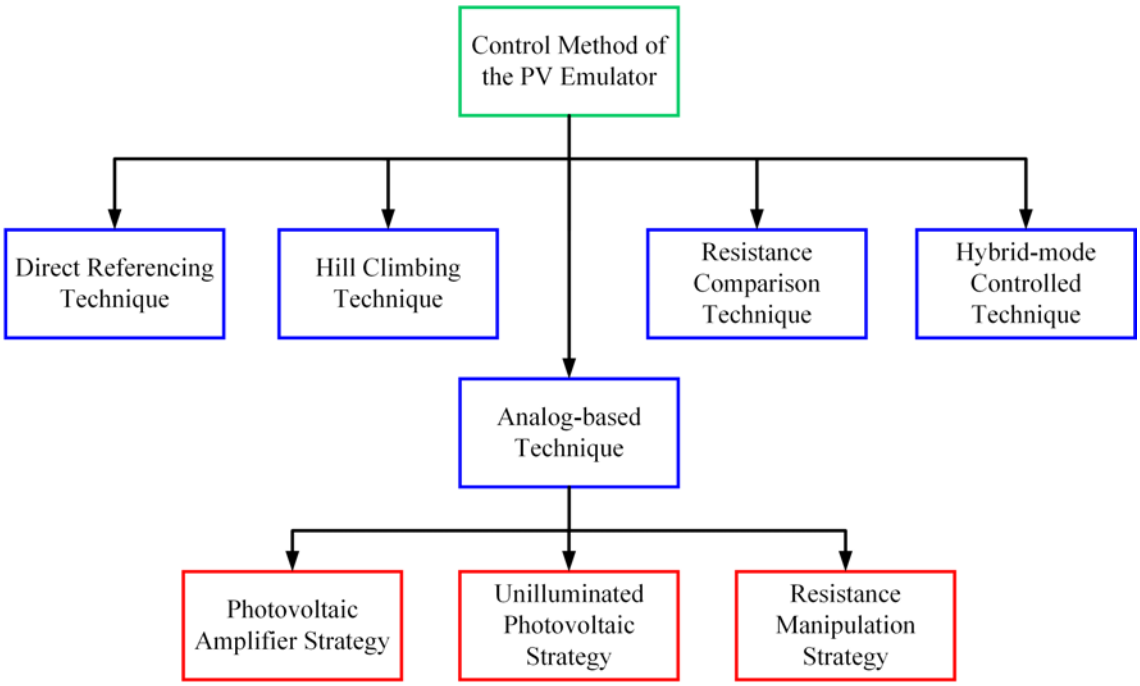


Figure 2.4: The PVE control strategy diagram.

the PVE: the current-mode and the voltage-mode controlled system. The current-mode controlled system needs the PV voltage as an input, as seen in Fig. 2.5 [6,71]. The figure shows the current function of the voltage ($I = f(V)$). On the other hand, the output voltage value is used as a feedback control to the PV model. At the start of the PV operation, the output voltage is zero because the PVE works on the constant current region, meaning the short circuit current is produced as a reference signal at a certain irradiance and temperature of the PV module. Based on the I-V characteristic curve, the short circuit current decreases when the output voltage increases.

The PVE achieves stability when the emulator operates on the point at which the output voltage and current correspond with the output resistance on the I-V curve. The other type of direct reference method is the voltage-mode controlled system. This system uses the output current as an input of the PV model in the mathematical expression in which the output voltage is a function of the output current ($V = f(I)$) [73]. This method produces the open circuit voltage at the beginning of the

operation because the reference current (output current) is equal to zero at the starting operating condition for certain irradiation and temperature values. The direct referencing control employs the dynamic behaviour of the closed loop converter to determine the emulator operation point.

The authors of [79] improve a method using the iteration solution to find the PVE operation point. This method is known as the algorithm, and it is evaluated by a LABVIEW program. The improved method uses the error between the PVE output and the PV model to generate the iteration step size. The operation point is re-calculated if the variation of the voltage and current is large. The researchers of [80] improved the direct reference control strategy by using the adaptive PI controller. The PI is trained by using the artificial neural network at several loads and irradiance values. Thus, the transient response and steady state of the emulator are maintained during various conditions.

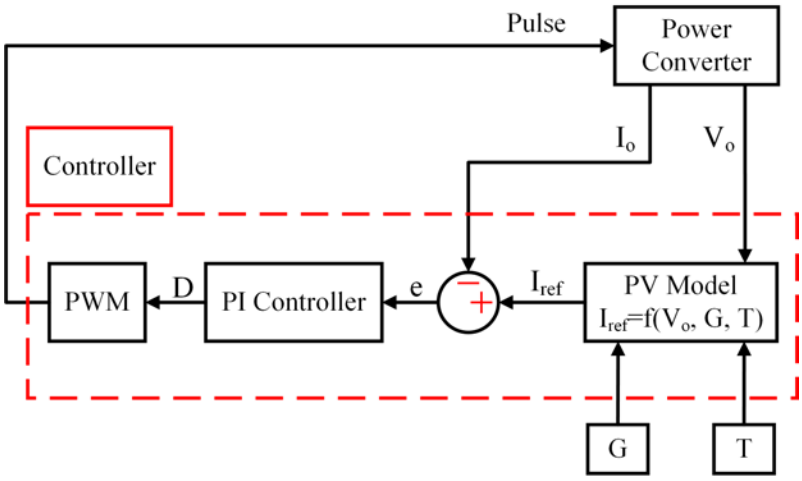


Figure 2.5: General diagram of the PV generator's simulator.

2.3.1.2 Hybrid-mode Controller Technique

The photovoltaic cell has a nonlinear characteristic curve. The characteristic curve has three different regions: the constant current (CC), constant voltage (CV) and MPP. On the CC region, the PV output current almost fixes and is slightly affected by the voltage variation. The reverse scenario occurs in the constant voltage region.

In addition, the traditionally closed loop power converter uses a fixed reference point. However, the reference point is not constant; it varies based on the nonlinear PV module characteristic. This reference variation generates an unstable power converter system even with the presence of closed-loop control. Therefore, the PVE output (voltage or current) oscillates [17]. The emulator stability can be improved by applying various direct referencing methods to the area of the current-voltage characteristic curve of the module. This control strategy is called the hybrid-mode control technique. This technique has two control methods depending on the operation region of the PVE, namely the voltage-mode control and current-mode control systems. On the other hand, two methods are used to design the hybrid-mode strategy based on the power source used. This control method uses either a single power source [81] or a dual power source [17].

The single source method uses only one power converter, whereas the dual method requires two power converters, one for the current and the other one for the voltage. The hybrid-mode method usually uses the switched-mode power supply while the PVE uses a single power source [2]. The PI controller is used to control the PVE power converter. A three LUT is used for this method: the V-R, V-I and I-V tables. Based on the analytical analysis, the current-voltage characteristic curve is classified into two types: the RI (constant current area resistance) and RV (constant voltage region resistance), where the RI is less than the RV resistive value on the curve itself, as shown in Fig. 2.6. The constant current area is classified as the current-mode controlled operation. The I-V table type is used to find the reference current value of the PVE at a CC operation area. The emulator works in this constant current region when the value of the output resistance is less than RI; otherwise, the PVE works in the voltage controlled mode. The PVE current and voltage are not constant at the operation area between RI and RV. The V-R table is used to avoid any oscillation that can occur and to create the reference voltage point of the PVE [2].

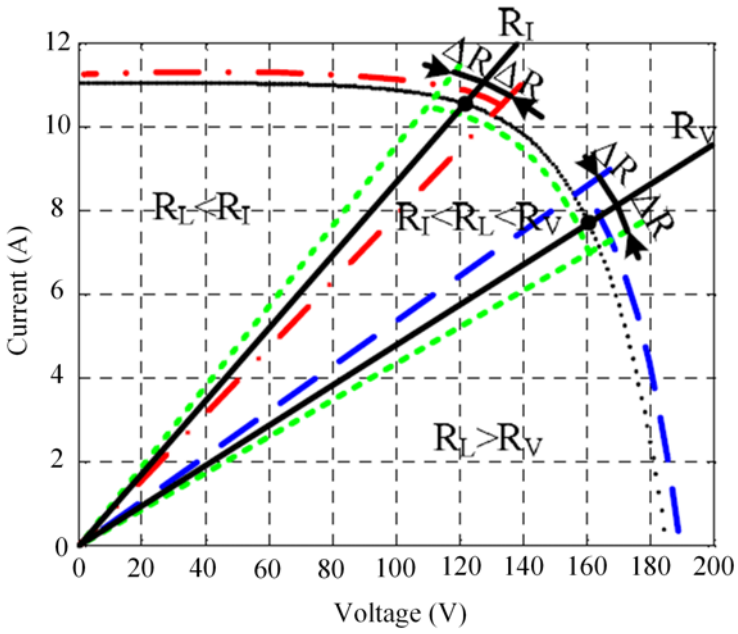


Figure 2.6: The proposed hybrid control strategy, three segments, and overlaps are shown [2]. The red curve is the current control, the green curve is the voltage control obtained by the measured resistance, and the blue curve is the voltage control obtained by the measured current.

On the other hand, the V-I table is used when the output resistance is greater than the RV value. The three operation areas are overlapped to eliminate any unstable switching that can occur during translation from one mode to another. The hybrid-mode dual source controlled method uses the linear voltage and current regulator [17]. These linear regulators are joined in parallel together with the PV load. In order to have a smooth transition between the current and voltage operation regions, a diode is added in series for each of them. This control strategy is known as hysteresis switching [2, 17]. The hysteresis method needs at least two operation voltage points, V_1 and V_2, where $V_1 < V_2$. In other words, when the emulator works at the CC and the R_o is increased, the PVE output voltage increases. If this increment in the output voltage is greater than the value of V_2, then the emulator works as a voltage source. The hybrid-mode method is used to eliminate the instability generated by the direct referencing control method. However, this control method is very complex and expensive because it uses two power converters. In addition, a

large storage memory and more than two look-up tables are required to implement the hybrid-mode controller method.

2.3.1.3 Hill Climbing Technique

The hill climbing (HC) control method and the perturb and observe (P&O) method are used as PVE control methods, as seen in Figs. 2.7 and 2.8 [82]. Compared with the direct referencing method, the hill climbing and P&O methods are used a constant step size that generates a more stable and accurate emulator output [3,82]. The hill climbing method is classified as a simple method compared with the perturb and observe control method because this method does not use a compensator in the control strategy [82]. Fig. 2.7 shows the hill-climbing control method uses a simple algorithm [83]. As Fig. 2.7 demonstrates, when the emulator begins operating, the output current and voltage are measured and the value is transferred to the PVE controller. The value of the PV current (I_{PV}) is calculated depending on the output voltage, irradiance and temperature. The calculated value of the I_{PV} is compared with the output current. If the $I_{PV} > I_o$, the I_o increases. The I_o increases by increasing the V_o during the duty cycle, D. The duty cycle increases using a constant step size, D_{step}. Furthermore, if the $I_{PV} << I_o$, then the I_o decreases, meaning the V_o is decreased by a decrease in the duty cycle value. Even though the hill climbing method is simple, the emulator works on as slow dynamic responses or fluctuating outputs based on the constant duty cycle step size. The P&O control method uses a PI controller in a state of increasing D directly, as seen in Fig. 2.7 [82]. As shown in Fig. 2.8, the D changes replaced by the changes of the reference current. The I_{PV} is a function of V_o, G, and T. The P&O method matches the I_{PV} with I_o. If I_{PV} is larger than I_o, the reference input, I_{ref}, is decreased by subtracting the current step size, I_{step}, from I_{PV}, while if I_{PV} is smaller than I_o, I_{ref} is increased by adding I_{PV} and I_{step}.

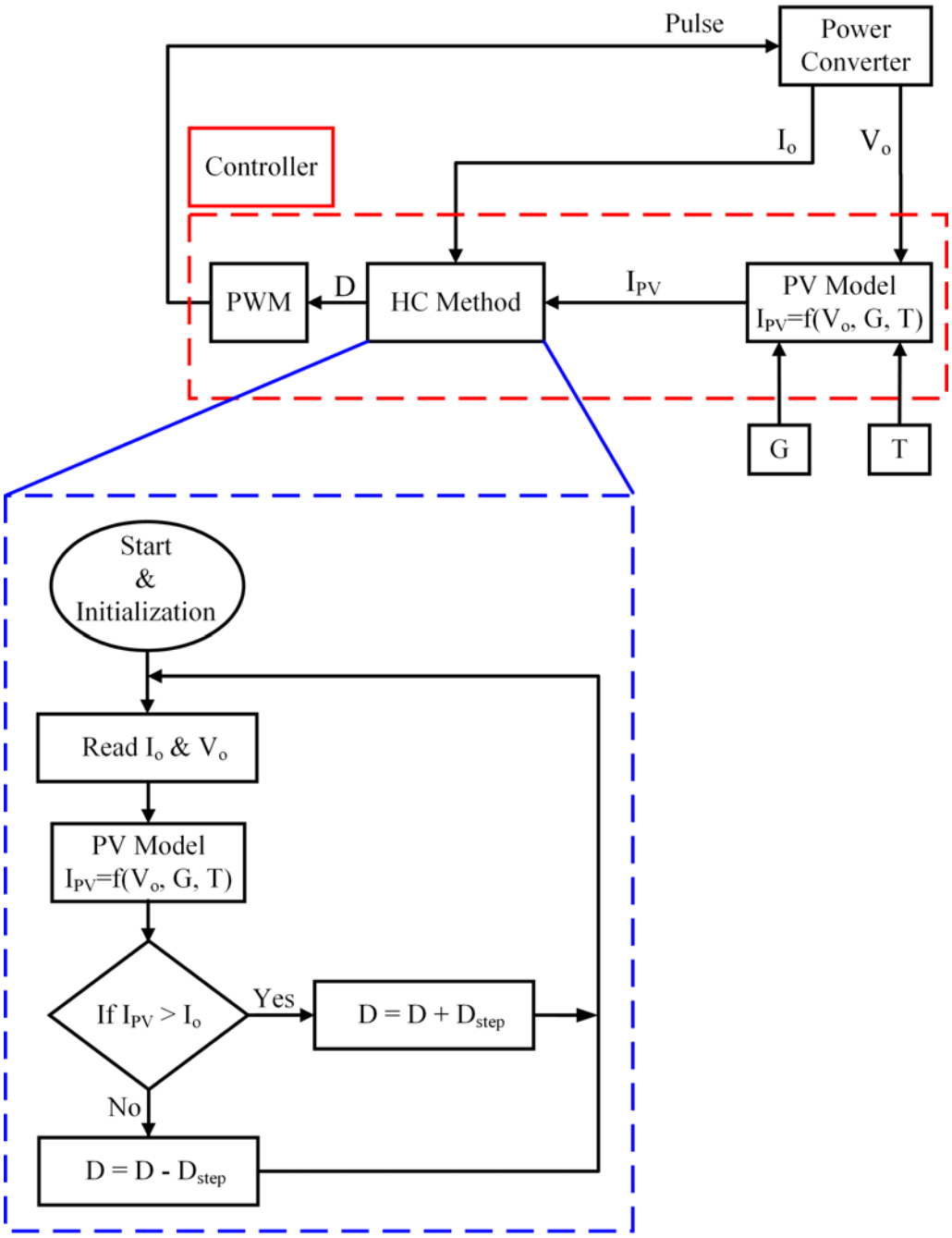


Figure 2.7: The hill climbing method, the block diagram and the control algorithm.

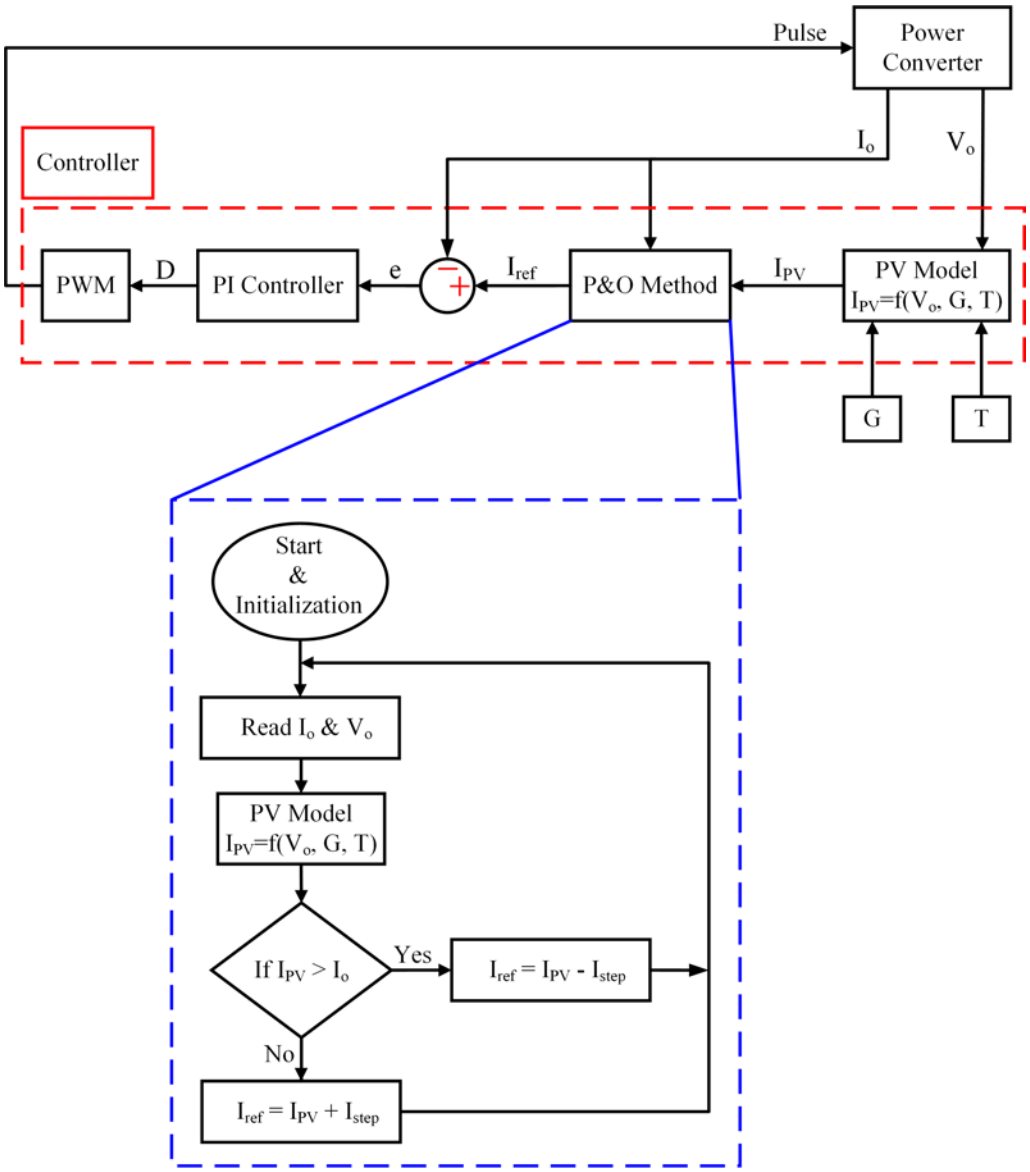


Figure 2.8: The perturb and observe method, the block diagram and the control algorithm.

2.3.1.4 Resistance Comparison Technique

The resistance comparison method is classified as one of the control PVE strategies. The PVE either uses voltage as the input and current as the output, mathematically with current as a function of voltage ($I = f(V)$) or the current as the input and the voltage as the output, meaning the voltage is a function of the current ($V = f(I)$). Therefore, the PVE model is enhanced to use R as the input and both the voltage and current as outputs ($[V, I] = f(R)$). The output resistance value is calculated

by dividing the output voltage value by the output current value, as seen in Fig. 2.9. This control method is used on the current-mode control [64, 65, 84], voltage mode control [65], the SMPS system and the programmable power supply [85]. The programmable power supply supports the current control mode and the voltage control mode. The resistance comparison control method is capable of generating the reference current and voltage at the same time. The programmable power supply uses this method to implement PVE [86]. The resistance comparison method is classified into two methods, known as the iteration-based and the resistance line methods. The basic design of this control method is based on the output resistance, obtained by dividing the output voltage by the output current and comparing the result with the resistance value (R_{PV}), which is calculated by dividing the V_{PV} by the I_{PV}.

As previously mentioned the iteration-based control method is categorized as one of the resistance comparison control methods. In this control method, the PVE uses the V_{PV} or I_{PV} as the input signal of the model. Based on the initial value of the PVE input, the iteration-based control strategies can be divided into two types. In the first, the initial input of the PV model is set at zero [65, 87], while the other uses a non-zero initial input value [64], as seen in Fig. 2.10. In the first method, the iteration begins with an input value of zero (V_{PV} or I_{PV}) [65, 87]. The photovoltaic output voltage increases by the fixed step size up to the V_{PV} equals to V_{oc}; in this way, the PV resistance can be found at all iterations [65]. After the first iteration is completed, the second iteration can be created and used to find the reference current value by matching the R_o with R_{PV}. The iteration-based method requires a full carding of the I-V curve at the start of the iteration or the variation value of either the irradiance or temperature. Therefore, the iteration-based control strategy is not appropriate for the PVE operated together with the dynamic variation for the irradiance or temperature. The authors of [87] proposed a new method based on calculating the R_{PV} and comparing it with the R_o value. This method starts the I_{PV} at zero and increases the value with a constant step size. The reference voltage value is calculated while R_{PV} is equal to or less than R_o, as seen in Fig. 2.10. One

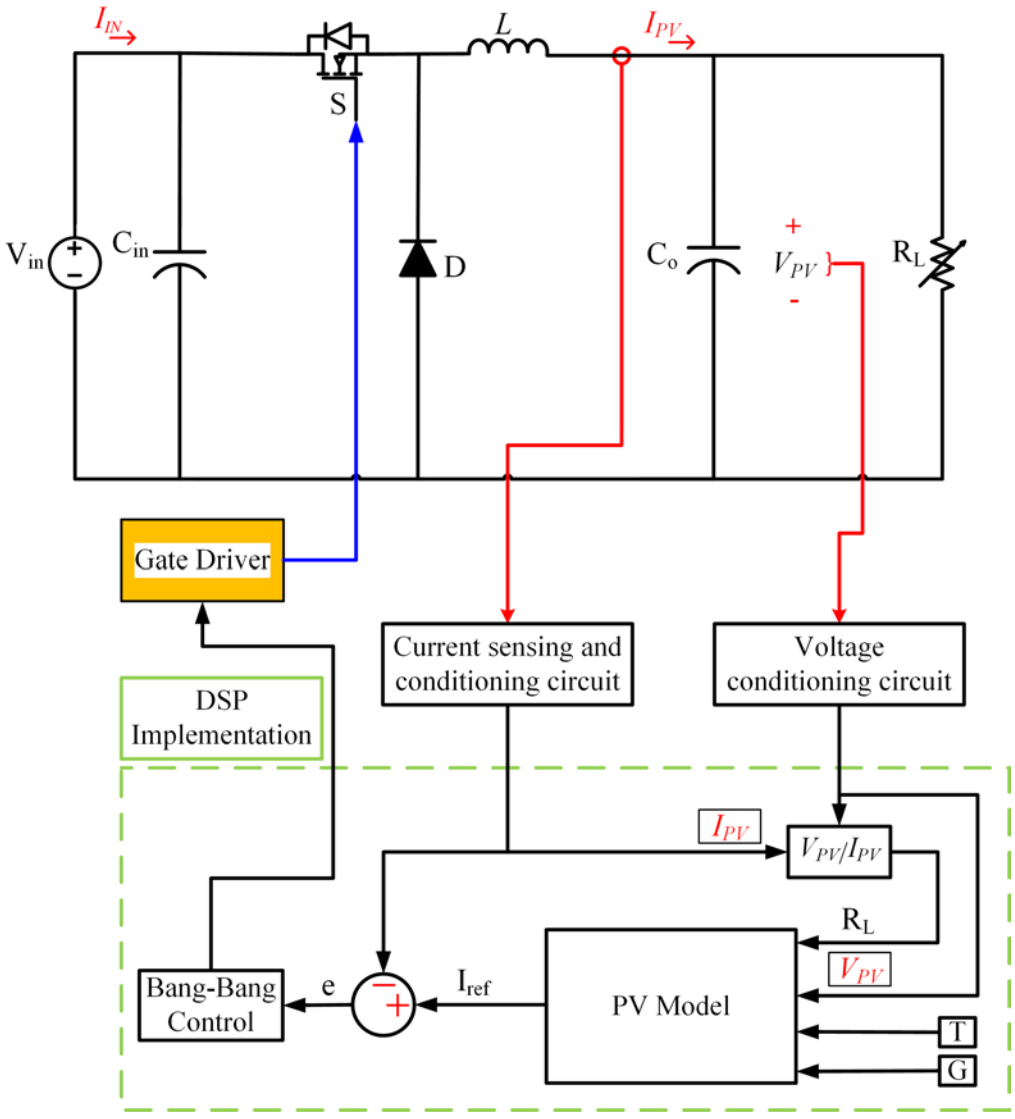


Figure 2.9: The resistance comparison technique for the PVE using the current-mode method.

of the advantages of this method is its ability to handle the dynamic variation in the irradiance or temperature. Nevertheless, it requires a large number of iterations to reach the operating point of the emulator.

Based on the complexity of the control, the non-zero initial method is more complex than the zero initial input method [64]. The iteration procedure is established at the point of the V_{PV} equal to V_o. The photovoltaic output voltage increases from the open circuit value by a constant step size. In addition, the R_{PV} is found for each iteration. Two conditions confirm every iteration. The first one is the resistance error. This error is found by calculating the variation through R_{PV} and R_o. The reference current value is generated if the resistance error is lower than the tolerance value. The second condition is a variation decision of V_{PV}. The range of R_{PV} is varied based on the location of the operation point on the I-V characteristic curve, and the range is small at the I_{sc} region (constant current region) and large at the V_{oc} point (constant voltage point). If the R_{PV} value is lower than the output resistance value (R_o), then the V_{PV} value will be increased. However, if the R_{PV} is greater than the R_o, then the V_{PV} decreases.

The resistance line control method is known as one of the resistance comparison control methods. This method uses the PV graphical curve or characteristic curve to locate the value of the output resistance (R_o) instead of mathematically analyzing the method [16]. The characteristic curve at a certain irradiation and temperature represents the PV model. This PV datum is drawn with the inverse R_o line, and the crossing among these two lines is used to determine the PVE operating point. The resistance line method is divided into two types, namely static resistance line method [16,86] and the dynamic resistance line method [88]. Both of them are implemented in the emulator. The static resistance line method only remembers the I-V data at specific irradiance and temperature values. This method is not appropriate for studying the PVE dynamic behaviour (under any variation of the irradiance or temperature). On the other hand, this method requires a large amount of I-V information data to build on the controller at different irradiance and temperature values. The dynamic resistance line method includes the PV model in the resistance

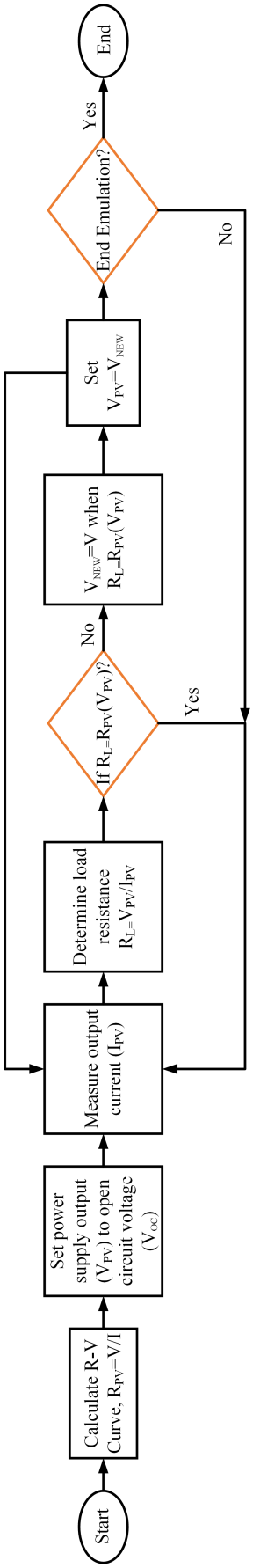


Figure 2.10: The iteration-based method together with the resistance comparing strategies in every iteration according to the input gives the PV module output voltage.

line method. When any variation of the irradiation or temperature occurs, the PV model is removed to obtain the I-V data. The variation in the irradiation and temperature values requires a fixed comprehensive process that loads the controller.

2.3.1.5 Analog-based Technique

Generally, the direct referencing and resistance comparison control methods are the common control techniques applied to the PVE design. However, the analog-based method is another method used to mimic the characteristics curve of the PVE module. One of the disadvantages of this method is its inability to emulate the PV model into a digital form because it is based on the behaviour of the analog circuit.

a) Photovoltaic Amplifier Strategy

The photovoltaic amplifier method of the PVE is fulfilled by the PV amplifier techniques [65, 89]. A single PV cell is coupled with a linear amplifier that contains the Darlington pair circuit [90], as shown in Fig. 2.11. To reach the high accuracy of the PV emulator characteristic curve, this method uses the feedback current-controlled loop. The designer emulates the different irradiation effects by using a halogen lamp. It is controlled by a variable DC voltage power supply. However, this method is usually not used because it requires a real solar cell to mimic the PV panel. The PV cell researchers have overcome this issue by exchanging the real PV cell with a photo-sensor or photo-diode [65, 91]. The different types of PV cells are simulated by tuning the specific internal resistor of the PVE itself [91]. The light from the light emitting diode (LED) linked to the fibre optic is used to control the irradiance exposed to the photo-sensor. The light intensity generated by the LED is controlled by using a computer that is connected to the digital to analog (DAC) converter [91] or the analog PWM creator [92]. The actual PV panel temperature is mimicked by connecting a small ceramic heater to the photosensor [91].

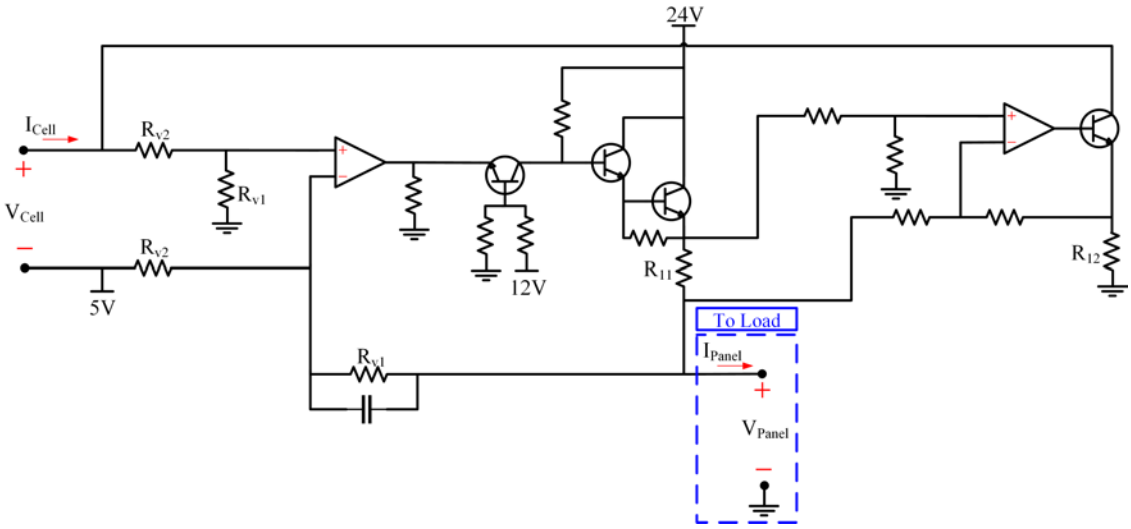


Figure 2.11: The linear amplifier by using a Darlington pair circuit.

b) Resistance Manipulation Strategy

The resistance manipulation method is the second type of analog-based control method used for the PVE [93, 94]. The resistance manipulation method is classified as a simple method compared with the other analog based control strategies, because it only needs a DC supply and a changeable load (resistor). In this method, the irradiance level is adjusted by controlling the current limiter of the DC power source. The resistance manipulation is one of the methods that uses the maximum power transfer theorem to check the MPPT and power conditioning system [93, 94]. The maximum power transfer theorem demonstrates that the PVE reaches the maximum power (MP) at the point of the series resistance equal to the load resistance. This method is a simple mimic method used to emulate the PVE, although the output characteristic of this method is not accurate compared with the real PV characteristic curve.

The resistance manipulation control method is situated at the MPP voltage at half the value of the open-circuit (OC) voltage. The resistance manipulation control method is not accurate enough to generate the I-V characteristic curve; however, this method is used to test the MPPT system and power conditioning system if

the designer's goal is to mimic the capability of the system to find the MPP. The PWM switch resistor is another technique used with the resistance manipulation control method. The characteristic curve generated by the PWM switch resistor is more accurate than the curve produced by the variable series resistance method. The PWM switch resistor performs the switch at the parallel and series resistance to create the characteristic curve identical to that generated by an actual PV. As a result, the output ripple generated by switching the resistance is very small because the output is adjusted by the DC power supply. On the other hand, this method has slow dynamic behaviour because it uses a large output capacitor of the DC source [94].

c) Unilluminated Photovoltaic Strategy

The electrical PV model has a current source, diodes, and resistors, as seen in Figs. 2.3 (c) and 2.3 (d). The current power source linearly follows the irradiance and module temperature, as seen in Fig. 2.3 (a), and the electrical model uses a diode to emulate real PV behaviour. However, the diode has a complex character and is difficult to mimic in a simple equation. Thus, the PV designer proposed unilluminated photovoltaic control strategies to overcome this issue [6,95]. The unilluminated photovoltaic is completed by preventing solar irradiance from damaging the PV model surface. Then, the designer removed the current source to mimic the electrical circuit model. The classical current source is replaced by the external current source, which is able to work under different operation parameters (under different variations of the irradiance or module temperature). The unilluminated photovoltaic control method consists of two types. The first one uses a PV cell(s) to create a closed loop converter reference point [6]. The second type uses a real PV module linked to the outer current source [95]. The second method does not have a control or power converter. As a result, this method does not have the bandwidth problem because it is linked with the power conditioning system, as with MPPT devices. In addition, the unilluminated photovoltaic is classified as a simple PVE method. This method has a fast dynamic response because it does not have a complex diode

calculation driving the controller. However, this method is not adaptable since it needs the real PV panel to run.

In summary, Table 2.4 shows a comparison between different types of feedback control system strategies, including the direct referencing technique, the hill climbing technique, the analog-based method, the resistance comparison (iteration-based) method, the resistance comparison (resistance line) method, and the hybrid-mode controlled method used for the PVE application. These methods are evaluated through various parameters, including accuracy, the need for an additional algorithm, computational time, software limitations, output stability, reference value calculation speed, complexity, computational cost, the convergence of the reference signal, input change detection, transient response, step size, dual reference, and independency.

Table 2.4: The comparison between the different types of feedback control system strategies used for the PVE [19–29]

Parameter	Direct referencing	Hill climbing	Analog based	Resistance comparison (Iteration based)	Resistance comparison (Resistance line)	Hybrid-mode
Accuracy	Accurate in steady state	Based on the step value	Based on the way used	Based on the step value	High	High
Additional algorithm	None	Needed	Based on the analog circuit	Needed	Needed	Needed
Computational time	High	Less than direct referencing	Depends on the analog circuit	Depends on the method used	-	High
Software limitation	There is no limitation	There is no limitation	Based on the analog circuit	There is no limitation	Needs line intercept detection	There is no limitation
Output stability	Unstable at some points of I-V curve	If the step size is large then it is unstable	-	If the step size is large then it is unstable	Steady	Steady
Reference value calculation speed	Slow due to convergence	Based on the speed of the controller	-	Based on the speed of the controller	-	Slow due to convergence
Complexity	Simple	Simple	Complex	Complex	Simple	Complex
Computational cost	High	Less than direct referencing	High	High	Less than Iteration based	High
Convergence of the reference signal	Depends on the closed-loop system	Based on the step size	-	Based on the step size	Inable	Depends on the closed-loop system
Input change detection	Unusable	Unusable	Unusable	Usable	Usable	Unusable
Transient response	Based on the controller	Based on by the step value	-	Based on by the step value	-	Based on the controller
Step size	Controller automatically adjusts	Constant value	Inapplicable	Constant value	Constant value	Controller automatically adjusts
Dual reference	Unable	Unable	-	Able	-	Able
Independency	Based on the external factor	Based on the external factor	-	Not affected by the external factor	Not affected by the external factor	Based on the external factor

2.3.2 Partial Shading (PS) Implementation Method

The partial shading implementation method is classified into two types, hardware-based and calculation-based or program-based, as shown in Fig. 2.12 [3,31,85]. The hardware-based type does not include any computation to generate an I-V characteristic curve over the partial shading operating condition. The many connections of the PVE or the common point of several PV cells are used to generate the PV characteristic during partial shading. In addition, the PV partial shading using the program-based approach is accomplished by using a complex mathematical representation to create the PV characteristic curve through the partial shading effect.

The PV cells can be connected in a series to increase the output voltage, as with a battery and connected in parallel to boost the output current. The sum of the PV cells connected on a series or parallel is called a PV module. However, the PV module has an issue with partial shading phenomena. If one or more PV cells is shaded, the power production from the string is reduced and the MPP transfers into the unexpected new point [67, 92]. The shaded problem creates a loss of power as heat, and the increase in PV temperature may damage the cell [96]. In order to solve this problem, the author of [96] proposed a new design that uses the bypass diode. The main aim of using the bypass diode is to protect the PV module from thermal harm and maintain the output power during the partial shading effect. As an example, the output characteristic curves of the PV system contain a 3 PV panel connected in series (model: SunPower SPR-X20-250-BLK), as shown in Fig. 2.13. The figure reveals that the PV system under partial shading using bypass diodes has more power than the one without bypass diodes. In addition, the figure shows that with bypass diodes, there are three MPPs, i.e., local (B and D) and global (C). Dirt and clouds are factors that cause PV partial shading [92]. PV researchers have used the field factor (FF) to represent the partial shading effect in the PV module. The FF is defined as the maximum power (MP) divided by the product of the short circuit current and open circuit voltage. The FF value decreases if partial shading occurs [92].

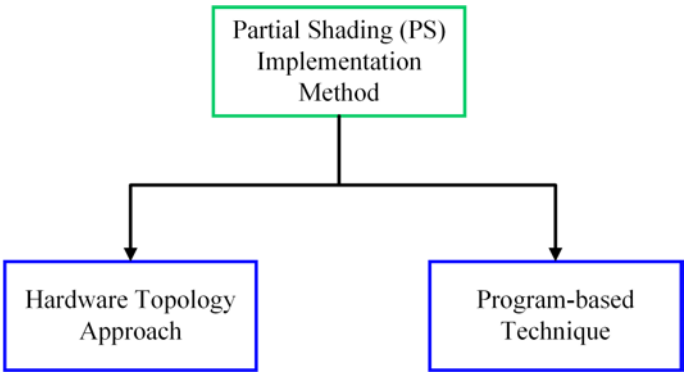
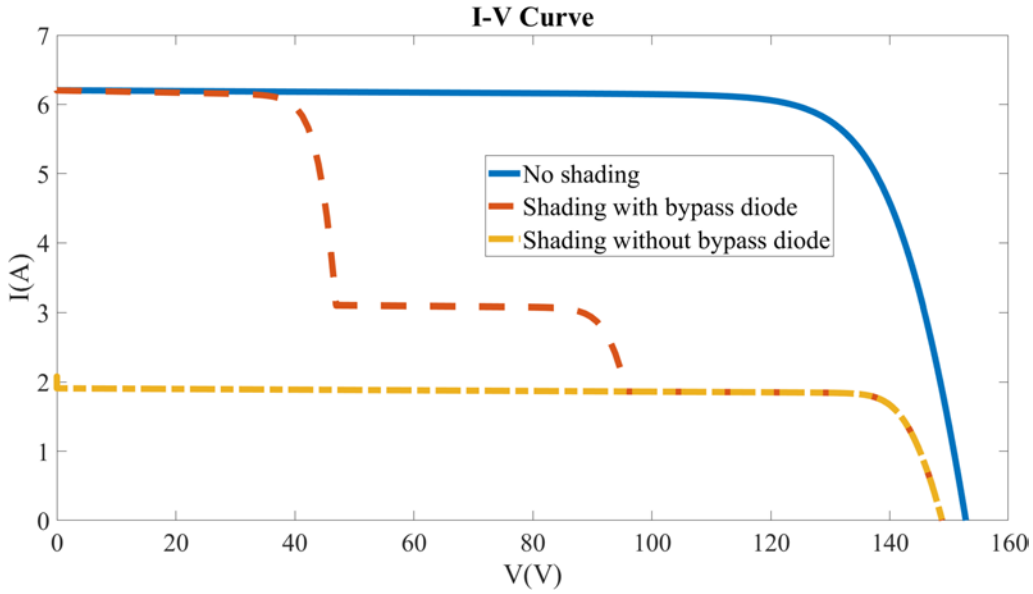


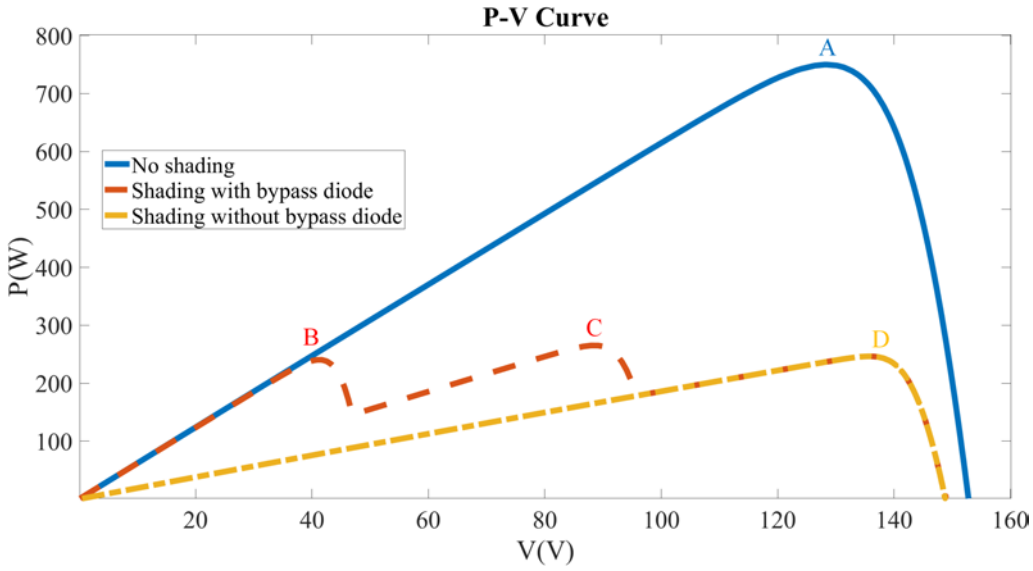
Figure 2.12: The partial shading implementation method for the PVE.

2.3.2.1 Hardware Topology Approach

The hardware-based application requires several elements. This approach is therefore a costly PV emulator method. In addition, this method does not include the calculation of the PV model in the controller unit through the partial shading effect. As a result, the controller complexity is minimized. The PV model is emulated by linking some of the programmable power sources in a series [86]. The resistance line strategy is used to locate the reference point. However, the data for the two *I-V* characteristics is sent to the two programmable power sources out of the serial data connection. Based on the two reference signals of the programmable power supplies, the power-voltage curve generates two maximum points for the series connection of the programmable power sources. As a result, the PV module characteristic curve is generated due to partial shading. The author of [31] presents the transistor-based control method as another form of the hardware-based partial shading emulation method. Comparing this method with the programmable power supply method reveals that fewer components are required to mimic the partial shading effect. In other words, the cost of the transistor is lower than the programmable supply method. However, the transistor-based method is inefficient because of the high power dissipated into the transistor body. To minimize the cost of the partial shading effect, the designer suggests implementing the hardware-based method into controller stage, not into the hardware design.



(a)



(b)

Figure 2.13: The PV system characteristic curve based on the partial shading effect with or without a bypass diode (a) I-V curve and (b) P-V curve.

The author of [92] proposed the PVE using series-connected small PV cells to solve this problem. The operational amplifier is used to control the V_{PV} of the series-connected PV cells while the I_{PV} becomes the reference signal for the PVE. Furthermore, the output voltage and current can be amplified to mimic a high-power PV system. This method generates a different value of irradiance based on the analog PWM generator. To achieve the shading effect, the photo-diode is covered by a piece of cardboard. However, the bypass diode is linked in parallel with the photodiode to generate several maximum points on the P-V curves. This method's low-efficiency is its main disadvantage because the PV amplifier only operates in the constant voltage region.

2.3.2.2 Program-Based Technique

The authors of [85, 88] presented a PV cell emulation based on the mathematical equation including the partial shading effect. The current is equal throughout the series-connected PV cells and the voltage is the sum of the voltage of all of the PV cells combined. On the other side, the voltage is equal across the parallel connection and the total current is the sum of the current of all of the PV cells combined. This method is implemented into the PV module's controller unit; thus, the design needs only one power converter. The buck converter [85] or the programmable power source [88] can be used. The electrical PV model uses a nonlinear equation [3, 42]. An iterative solution method such as the Newton-Raphson is used to solve this implicit equation [29, 81, 88]. Implementing partial shading via calculation requires some PV modules to be connected under different irradiance and temperature values. As a result, the complex equation of the PV model requires a large amount of time, which loads the controller and minimizes the sampling time. However, it is reasonable to directly calculate several PV models for the PVE [81, 85]. Researchers have proposed many techniques to solve this problem. In [85], the authors presented the curve segmentation method as a way to simplify the PV module. The authors of [97] proposed a matrix equation method to minimize the load in the controller. However, this method works in a certain way that varies the equivalent circuit PV model with a matrix equation. The interpolation implementation model is defined

as another method used to exchange the electrical complex model [88].

2.3.3 Controller for Photovoltaic Emulator or Hardware Platform

The hardware platform can be implemented through an analog approach, a digital approach or a combination of both, as shown in Fig. 2.14 [6, 24]. The controller of the PVE is classified into two main parts; the first is responsible for calculating the PV model parameters and creating the common point for the emulator, and the second enhances the power converter control system.

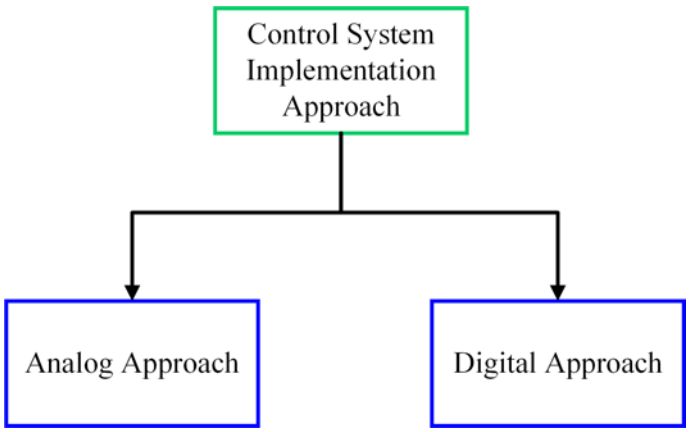


Figure 2.14: The method for implementing the control system into the controller unit in the PVE.

2.3.3.1 Analog Hardware Platform

In [98], the author proposed using the analog hardware platform to mimic the PV model. This method minimizes the computational delay related to the digital hardware method. The authors of [6, 99] used the resistance network and the series of diode heaps to create the reference point for the closed loop converter. The resistance network emulates the series and parallel resistance of the PV model; however, the diode stack requires the identification of the PV characteristic curves. In addition, the authors of [78, 98] proposed the operational amplifier method to generate the PV model characteristic curve. The authors of [12, 31], meanwhile, presented a collection of transistors and resistors as a proposed method used to mimic the PVE.

The main advantage of using a transistor over the diode is to minimize the number of the element needed to emulate the PVE [31]. Manually changing the irradiance or temperature value is one of the drawbacks of using passive elements to mimic the PV characteristic curve [78].

The authors of [4, 6] proposed the single PV cell as one of the analog hardware controllers used to implement the PV model. In this method, the operational amplifier is used to control the photovoltaic output voltage, and the current generated is used as a common value for the emulator [4]. In general, the closed loop controller has a PI compensator and uses a pulse width modulator (PWM) technique [65]. Due to the simplicity of the digital hardware method, the designer usually implements the PI compensator and PWM into a digital controller. The digital hardware controller is not sensitive to noise, and it suffers from a slow calculation. The hardware platform requires a fast response, especially during the transient period of the converter because the compensator feedback control is very sensitive. In [100], the authors suggested using the operational amplifier to emulate the compensator in the control system. The analog hardware for the PWM can be incorporated into an integrated circuit (IC) [94]. The switching frequency (f_s) of the power converter is controlled by variating the value of the resistance and capacitor linked to the integrated circuit (IC). The duty cycle product from the compensator is created from the analog or digital hardware control method [100]. One of the advantages of the PWM IC is that it allows the PVE to work at a high switching frequency of up to 500kHz; as a result, the PVE's LC filter size is reduced, resulting in a faster dynamic response [101].

2.3.3.2 Digital Hardware Platform

Two types of digital hardware platforms can be used to make the PVE: the single digital hardware platform and the cascade digital hardware platform. The single digital hardware platform uses several components to mimic the PVE, such as the dSPACE rapid prototyping [23, 24], the field-programmable gate array (FPGA) [25, 53], the digital signal processor (DSP) [21, 22], the computer [29] and the microcontroller [26–28]. However, using the digital hardware platform to make the PVE requires a large amount of time. This produces an incorrect control behaviour sym-

metrical to the power converter output signal. In other words, the PVE accuracy and stability are affected. However, the large sample time requires the SMPS to have a low switching frequency. Due to the low switching frequency, the size of the filter is increased, meaning the dynamic response of the emulator slows. The goal of using the cascade digital hardware is to minimize the load generated by single digital hardware. Generally, the processing load has two parts. The first one is the digital hardware and finds the PV model parameter required to build the PVE. The analog hardware method has a faster dynamic response compared with the digital hardware method. However, it is affected by noise. In addition, installing the analog hardware is more complex than implementing the digital hardware platform. If any change occurs, the analog hardware method requires a reimplementation. The digital hardware is more flexible than the analog hardware and less subject to noise associated with the analog hardware platform.

2.4 Power Stage

The PVE is used to produce the nonlinear electrical characteristics of PV cells or panels [74, 102]. The majority of the reported PVEs use a power supply, either a switching power converter or a linear regulator. Many studies have been done on PV source emulators, and most of them are based on the switched-mode power supply because the SMPS is more effective than a linear regulator [103, 104], as to be seen in Fig. 2.15.

2.4.1 Linear Regulator

The linear regulator converter is used to minimize the input voltage and adjust the output (voltage or current). The linear regulator uses two methods used to operate the PVE. The first is the linear regulator integrated circuit [17, 78]. There are two types, the voltage regulator and the current regulator; however, the voltage regulator is more frequently used in the PVE [17]. The linear regulator converter is controlled by the closed-loop PID or PI controller [17, 78]. The PVE controller is mimicked in either the analog circuit by using the operational amplifier method or the digital circuit through the microcontroller [105]. However, the linear regulator

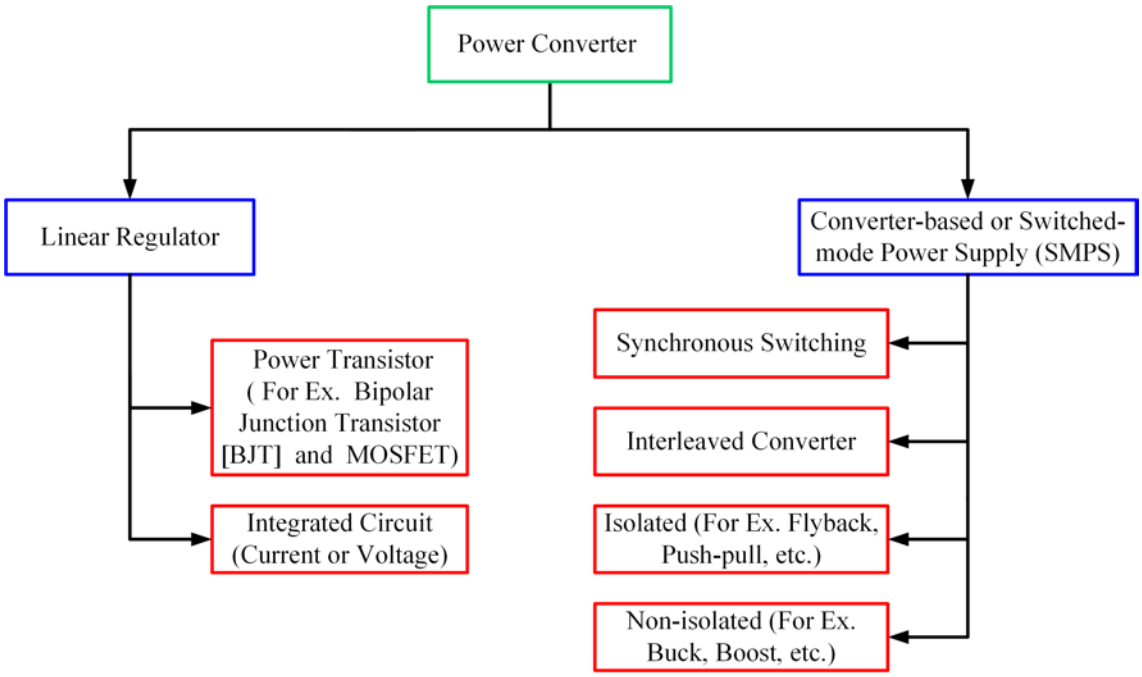


Figure 2.15: The power converter classification for PVE application.

IC generates a current with small value. Thus, the current booster design is used to increase the PVE output current value [105]. The power transistor implementation method, like the bipolar junction transistor (BJT) [12, 106] and the MOSFET [107], is classified as one of the linear regulator implementation techniques. In particular, the power transistor is connected in series with the load and DC power source. It does such a changing resistor controlled by the gate-source voltage, V_{gs} (MOSFET) or the base current (BJT) [108]. Based on the voltage divider rule, the variation in the resistor, which is mimicked by the power transistor, allows the voltage to be adjusted at the load. The BJT base current is controlled by using a complex design of resistors and diodes [12] or an operational amplifier [106]. The base current limitation value is defined by the common-emitter current gain [109]. When the converter gain is small, the BJT requires a high base current to control the current passing through it. The designer used a low base current value as a control signal. However, a high common-emitter current gain is required to maintain the simplicity of the control circuit. In [12], the author proposed the Darlington pair circuit in

order to increase the gain value. In summary, the MOSFET is more easily controlled than the BJT, in which it uses voltage control instead of current control in the BJT case. In addition, the MOSFET provides high switching frequency capabilities that help reduce output filter size and make the dynamic behaviour of the PVE fast. Furthermore, the switching speed of the MOSFET is higher than the switching speed of the BJT.

The diode in the PV model has a complex characteristic equation, and this complexity loads the digital controller. The diode equation has an implicit equation that needs a numerical iterative solution, for example, the Newton-Raphson method. The Newton-Raphson method requires multiple iterations based on the steady-state error value. As a result, this creates delays in the computation of the operating point of the PVE. A PV designer proposed unilluminated photovoltaic control strategies to overcome this issue [6]. The unilluminated photovoltaic was achieved by preventing solar irradiance from reaching the PV model surface. A network of diodes was proposed to emulate the diode characteristic used in the PV model [6]. In fact, the number of diodes required depends on the number of PV cells into the PV module.

2.4.2 Switched-mode Power Supply

Different approaches to converter-based PVEs have been reported, as shown in Fig. 2.15. The isolated and the non-isolated are two kinds of converter design used for the PVE. In terms of simplicity and the number of elements needed to mimic the PVE, the non-isolated method is more popular than the isolated method. The main aim of using the isolated converter is to separate the power source and the load. The separation is created by using the electrical transformer. The isolation method is very important if the output voltage is very similar to the input voltage. There are two types of electrical transformer: the step up and the step down. The forward converter is classified as a step-down isolation converter and is normally used PV emulator assembly [29,42]. In [110,111], the authors presented the flyback converter as a step-up and step-down isolation converter. One of the advantages of the flyback converter is its flexibility for changing the emulator output. In addition, the flyback converter requires only a few components, and the increase of the power rating

requires a large transformer core [108, 112]. The flyback converter is suitable for applications requiring less than 150W; on the other hand, the forward converter is usually used for the emulator applications of up to 500W [108]. The high voltage stress while the switch is turned off is the main disadvantage for both the flyback or forward converter.

The authors of [6, 65] presented the buck converter as a more appropriate converter for mimicking the PVE characteristic curve with a wide range of variations, especially when the input voltage of the buck is greater than the open circuit voltage (V_{oc}). In [74], the authors used a two-switch non-inverting buck-boost DC/DC converter to mimic actual PV behaviour. The key idea is to use multiple linear equations to perform the curve-fitting of the actual I-V curve, where the input voltage is less than the V_{oc}. The dual-mode controller was also introduced in [102], which works in both the current source and voltage source regions. However, it needs additional electronic hardware in addition to the basic converter and associated circuitry.

The authors of [4] proposed the interleaved buck converter for the emulator application. In [108], the author explains the advantages the multi-phase or interleaved buck converter has over the classical buck converter, such as its low inductor current ripple and small capacitor size. As a result, the low capacitance value enhances the dynamic behaviour of the power converter [113]. In other words, the interleaved buck converter has a faster dynamic performance response and a higher efficiency than the buck converter. In term of the voltage stress and power loss, the interleaved buck converter is more efficient and has less power loss than a buck converter because the interleaved converter uses MOSFET and inductor elements with a low internal resistance, meaning the power loss is decreased, the voltage stress is lower and the total system efficiency is increased. The interleaved buck converter requires a complex controller and a high number of elements [113]. The input power rating is one of the most important aspects when selecting the power converter for the PVE. However, the designer needs a high input of power for the design-build to mimic some of the PV modules, whereas for the single and double module, the single-phase power supply is enough [114, 115]. The DC power supply is used as the

converter's input in the PVE design.

In [102], the synchronous buck converter is used to mimic the PVE characteristic curves, and the power loss in this converter is lower than the conventional buck. However, the synchronous buck converter requires a more complex controller compared with the buck converter and needs a time delay among the two switch (dead time) to block a short circuit problem. In [15, 116], the authors proposed the zero-voltage-zero-current (ZVZC) switching or soft switching technique to minimize the power loss and enhance the power converter's efficiency. In the conventional converter, the hard switching technique is used. As a result, this method increased the switching loss and generated electromagnetic interference (EMI). These problems can be minimized by using soft switching techniques, such as zero-voltage switching (ZVS) and zero-current switching (ZCS) [116].

PVEs on the market are generally costly due to the complex hardware designs and implementation costs to reach a high level of accuracy, a high power level, and high efficiency and mimic different environmental conditions [42]. In [86], the authors presented an emulator that uses a programmable power supply; this converter requires 120ms to reply to the response after the new voltage value is set. The authors of [63] presented a programmable power supply using the LabVIEW program. The LabVIEW takes 400ms to do the algorithm loop, which requires 233ms to set up the programmable power supply. The author of [99] shows another type of programmable power supply that uses the analog control method with a reply time of 3.8ms.

In summary, Table 2.5 shows a comparison between the linear regulator and converter-based or switched-mode power supply (SMPS) used for the PVE application. The table compares the dynamic performance, controller requirements, electrical isolation, output ripple, and efficiency. Hence, the SMPS shows high overall efficiency and more flexibility than the linear regulator.

Table 2.5: A comparison between the linear regulator and converter-based emulator used for the PVE application [8, 20, 23, 28–32]

Parameter	Linear regulator	Converter-based
Dynamic performance	Fast	Slower than linear regulator
Converter controller	Needed	Needed
Electrical isolation	No need	Based on the type
Output ripple	No output ripple	Has output ripple
Efficiency	Low	High

2.5 Summary

Owing to the rapid increase in research and development in renewable energy systems in recent decades and the intermittent nature of most renewable energy sources, energy emulators have become a critical tool in the development and testing of these energy systems. A PVE is a power conditioning system used to emulate the static and dynamic behaviours of the real solar cell, panel, or array. The PVE consists of three main parts: the PV model system, the power stage, and the feedback control system. According to the literature, there are two types of PV model systems: analog or digital representations. In terms of the power stage, the majority of existing PVEs reported in the literature are based on switching mode power supply (SMPS) topologies such as the buck, boost, and buck-boost converters because they are more efficient than linear regulators. The switching converter based approach is reliable and ideal for a steady-state operation, but the controller bandwidth restricts its dynamic response. Hence, the converters are usually slower than a real PV panel. The third part of the emulator is the control system, which links the PV model system with the power stage to turn on the emulator. The control system impacts the accuracy, dynamic response, and steady-state response of the PVE.

Chapter 3

A Simple and Fast Dynamic Photovoltaic Emulator Based on a Physical Equivalent PV-cell Model

3.1 Overview

According to the literature review in Chapter 2, the existing PVEs are difficult to implement and require a high-performance control unit or a simple structure with inaccurate performance and slow dynamic response compared with existing PV systems. Many researchers have mathematically implemented the PV model into the control unit based on the single-diode model [3, 8, 30]. Unfortunately, the diode in the PV model has a complex characteristic equation. This complexity loads the digital controller. The diode equation has an implicit equation that needs a numerical iterative solution, for example, the Newton-Raphson method, which requires multiple iterations based on the steady-state error value. As a result, this creates unwanted delays in the computation of the operating or reference point of the PVE [3, 8].

The authors of [52] briefly described the circuit-based PVE, which can be classified as a linear power converter, as shown in Fig. 3.1. However, it is unclear how the diode string is designed to mimic the electrical characteristics of a commercial PV panel. Since the electro-thermal property of the diode is similar to the actual PV cell, the PVE based on this type of circuit is expected to achieve better performance, both in the steady-state and dynamic responses, although this has not been confirmed in [52]. In addition, the potential and practicality of the PVE based on the PV equivalent circuit model have not been fully explored, including the design of DC constant current source dedicated to this application, partial shading conditions, and electro-thermal behaviour. Due to these reasons, therefore, this work presents a simple, reliable, and effective circuit-based PVE based on the equivalent PV stacked cells considering different design aspects.

This chapter first describes the PV emulator's construction using the physical PV-cell model and based on the key design equations. Secondly, in addition to the work presented in [52], the thermal issue related to the diode string has been investigated and solved by adding a cooling system (variable speed fan). Thirdly, the study examines the partial shading (PS) effects on a series of combinations of PV cells and compares their maximum power points (MPPs). A boost DC/DC converter

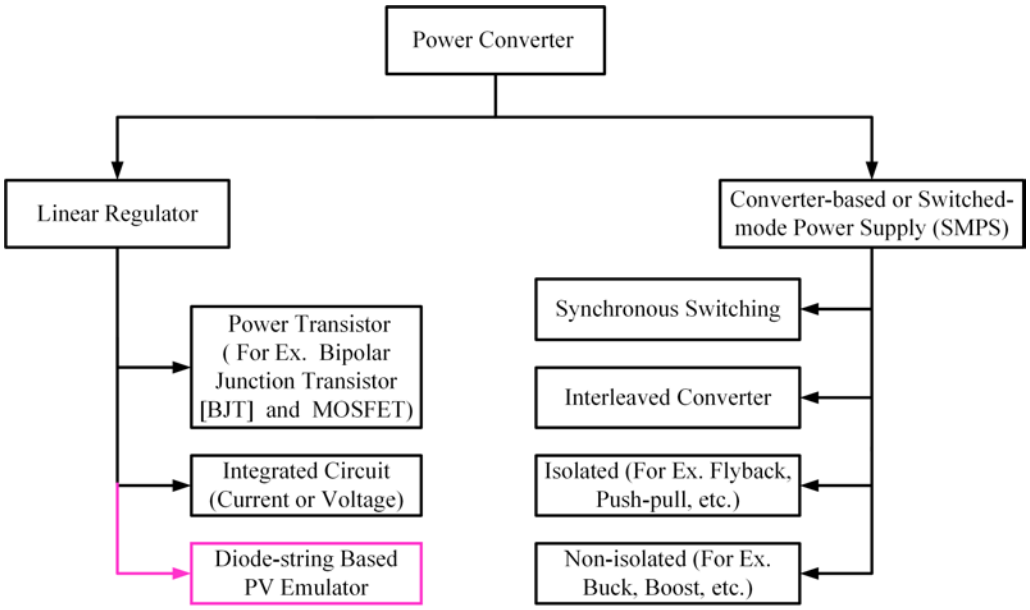


Figure 3.1: The power converter classification for PVE application, including the proposed approach.

loaded with a perturbing and observe (P&O) algorithm is used to evaluate the proposed PVE platform [37, 38]. The performance of the proposed emulator is also compared with a commercial 10W PV panel and several commercial PVE products.

The chapter is organized as follows: The photovoltaic mathematical model and equivalent circuit design based on a one-diode photovoltaic representation are presented in Section 3.2. Section 3.3 illustrates and discusses the simulation and experimental results, followed by the conclusion in Section 3.4.

3.2 Photovoltaic Mathematical Model and Equivalent Circuit Design Based on a One-diode Photovoltaic Representation

For the sake of simplicity and acceptable accuracy, the one-diode PV model, as shown in Fig. 3.2 [44, 117], is used in this work. The PV model is built by using a DC current source, diode, series resistance (R_s), and parallel resistance (R_p). The DC current source I_{ph} is used to represent the cell photo-current generated by the PV cell. I_{ph} is a function of both solar radiation and cell temperature. The

series resistances (R_s) is used to represent the sum of several structural and contact resistance in the PV model. Lastly, the equivalent parallel resistance (R_p) is used to represent the leakage current in the p-n junction that depends on the fabrication technology of the PV cell itself.

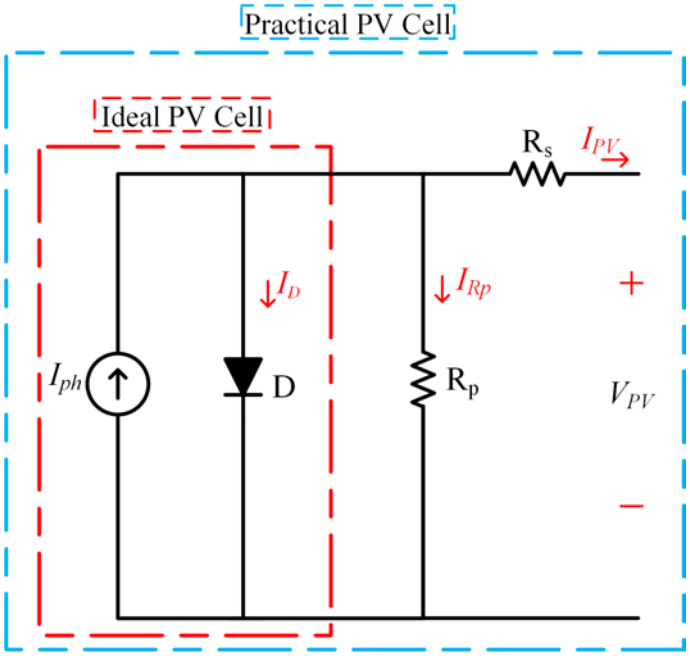


Figure 3.2: One-diode model of the theoretical PV cell and equivalent circuit of a practical PV system, including both the series and parallel resistors.

Depending on the reverse recovery characteristics, speed of operation, current, and voltage handling capability, the power diodes can be classified into three main categories: normal or general-purpose diodes, fast/ultrafast recovery diodes, and Schottky diodes [118, 119]. Unlike a conventional p-n junction diode (normal and fast/ultrafast), the Schottky diode is formed from a metal-semiconductor (N-type) junction. It is also not available with high reverse blocking voltages, and its reverse leakage current is relatively high. In addition, it is more expensive than the normal and fast recovery diodes. Furthermore, the PV cell built using the p-n junction, the Schottky diode, is not suitable for mimicking the actual PV cell because of the fabrication material.

According to the thermo-electrical characteristics given in the datasheet, the normal

(1N5400) and ultrafast recovery diode (UF5400) share additional similarities when comparing suitable diode types for building a PV emulator for a chosen PV panel. The chosen criteria are forwarding voltage, the average rectified output current, typical thermal resistance junction to ambient, operating and storage temperature range, typical junction, capacitance, reverse and forward recovery time, and cost. The 1N5400 and UF5400 have almost the same characteristics except for the price and the recovery time. However, this study uses the 1N5400, as it is less expensive than the UF5400. It also has an acceptable dynamic response concerning the actual PV panel.

The mathematical representation for the series-connected PV cells shown in Fig. 3.3 can be derived as follows [38, 120]:

$$I_{PV} = I_{ph} - \frac{V_D}{R_{peq}} - I_D \tag{3.1}$$

where V_D is the forward diode voltage (V), and I_D is the diode forward current (A).

$$I_D = I_s \times [exp(\frac{V_D}{a \times V_t}) - 1] = I_s \times [exp(\frac{(V_{PV} + I_{PV} \times R_{seq})}{a \times V_t}) - 1] \tag{3.2}$$

$$I_{PV} = I_{ph} - I_s \times [exp(\frac{(V_{PV} + I_{PV} \times R_{seq})}{a \times V_t}) - 1] - \frac{(V_{PV} + I_{PV} \times R_{seq})}{R_{peq}} \tag{3.3}$$

where I_{PV} is the output current of the PV system (A). I_{ph} and I_s are the photovoltaic and saturation currents of the PV system, respectively. V_{PV} is the output voltage of the PV system (V). V_t is the thermal voltage of the PV system with several cells connected in series. R_{seq} is the equivalent series resistance (Ω), and R_{peq} is the equivalent parallel resistance (Ω). a is the diode ideality factor.

$$V_t = \frac{NKT}{q} \tag{3.4}$$

where K is the Boltzmann constant, and it is equal to $1.3806503 \times 10^{-}23$ ($\frac{J}{K}$). T is the actual temperature of the p-n junction (Kelvin). q is the electron charge, and it is equal to $1.60217646 \times 10^{-}19$ C. N is the number of cells connected in series to

increase the output voltage of the PV panel.

In this experiment, a p-n junction power diodes, resistors, and a constant current source are used to build a simple PV panel emulator as an equivalent physical PV cell/panel model, as shown in Fig. 3.3. The I_{ph} of the PVE is represented by using a DC voltage source which operates at constant current mode. In order to clarify the proposed circuit clearly, Equation (3.1) is presented graphically in Fig. 3.4.

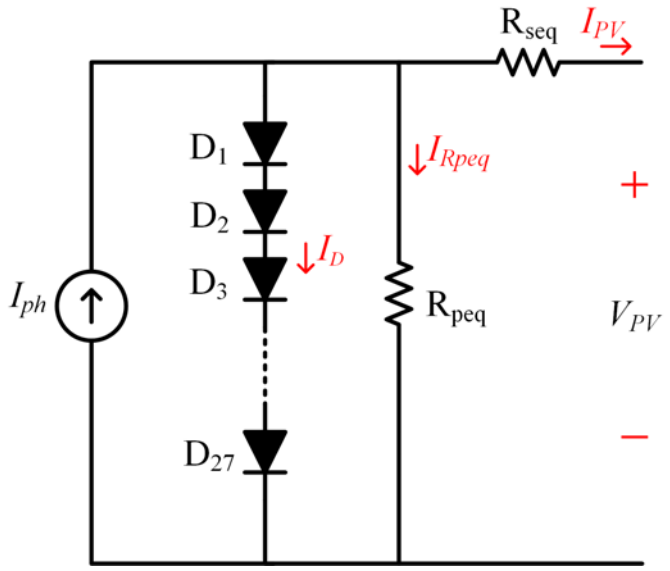


Figure 3.3: A simple PVE using the idea of the one-diode equivalent circuit of a PV cell with series resistance and shunt resistance. A diode string is used to create an effect similar to stacking multiple PV cells to develop a PV panel.

In general, the manufacturers of PV panels supply limited information about electrical and thermal behaviour at the STC. Usually, the photovoltaic datasheet contains details about the open-circuit voltage (V_{oc}), short-circuit current (I_{sc}), and the current and voltage at the MPP (I_{mpp} and V_{mpp}) [121]. This work uses the datasheet of a commercially available PV panel to work out the circuit parameters for the emulator. By using three operating points, namely short-circuit, maximum power point, and open-circuit, we are able to develop the model with four boundary conditions [122]. However, mathematically it is not sufficient to find the values of the five parameters of the PVE (R_{seq}, R_{peq}, N, I_{ph}, and diode ideality factor a) based on the four boundary conditions.

According to the semiconductor material used to fabricate diodes, the ideality factor is between 1 and 2 [122,123]. The diode ideality factor is estimated at 1.85, according to the diode datasheet (1n5400) and (V_{oc}-I_{sc}) curve method [124]. Equations (3.5) to (3.9) can be produced using boundary conditions [125].

By considering the value at the short circuit operating condition and substituting the value of the voltage and current (0, I_{sc}), Equation (3.3) can be expressed as (3.5).

$$I_{sc} = I_{ph} - I_s \times [exp(\frac{q \times (I_{sc} \times R_{seq})}{a \times N \times K \times T}) - 1] - \frac{(I_{sc} \times R_{seq})}{R_{peq}} \tag{3.5}$$

By substituting the voltage and the current values at open-circuit condition (V_{oc}, 0) in Equation (3.3), the Equation can be re-written as follows:

$$0 = I_{ph} - I_s \times [exp(\frac{(q \times V_{oc})}{a \times N \times K \times T}) - 1] - \frac{V_{oc}}{R_{peq}} \tag{3.6}$$

By considering the value at the maximum power point operating condition and

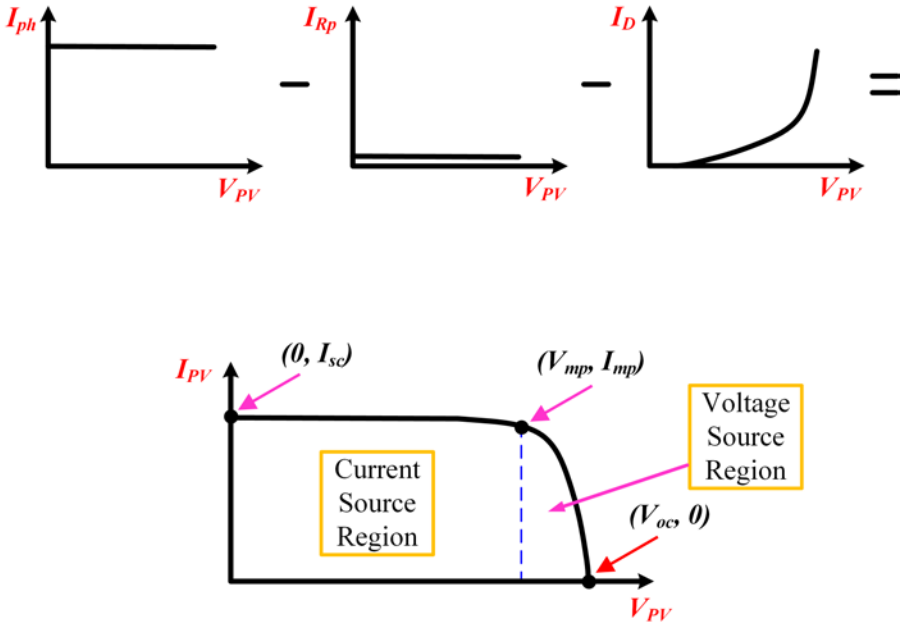


Figure 3.4: The characteristic I-V curve of the photovoltaic cell. The net cell current I_{PV} is composed of the light-generated current I_{ph}, I_{Rpeq} and the diode current I_D.

substituting the value of the voltage and current (V_{mpp}, I_{mpp}), Equation (3.3) can be expressed as (3.7).

$$I_{mpp} = I_{ph} - I_s \times [exp(\frac{q \times (V_{mpp} + I_{mpp} \times R_{seq})}{a \times N \times K \times T}) - 1] - \frac{(V_{mpp} + I_{mpp} \times R_{seq})}{R_{peq}} \tag{3.7}$$

The derivative of (3.7) with respect to V_{mpp} at MPP is given by:

$$\frac{-I_{mpp}}{V_{mpp}} = (\frac{-I_s}{a \times V_t}) \times (1 - \frac{I_{mpp}}{V_{mpp}} \times R_{seq}) \times [exp(\frac{(V_{mpp} + I_{mpp} \times R_{seq})}{a \times V_t})] - \frac{1}{R_{peq}} \times (1 - \frac{I_{mpp}}{V_{mpp}} \times R_{seq}) \tag{3.8}$$

Equation (3.8) can be simplified to find the values of the four parameters, as shown below:

$$N = \frac{(q \times V_{oc})}{(a \times K \times T \times ln(\frac{I_{sc}}{I_s} + 1))} \tag{3.9}$$

where N is the number of series cells or power diodes required to build a PVE.

$$R_{seq} = A \times (W_{-1}(B \times exp(C)) - (D + C)) \tag{3.10}$$

where:

$$A = \frac{a \times V_t}{I_{mpp}} \tag{3.11}$$

$$B = -\frac{V_{mpp} \times (2 \times I_{mpp} - I_{sc})}{(V_{mpp} \times I_{sc} + V_{oc} \times (I_{mpp} - I_{sc}))} \tag{3.12}$$

$$C = \frac{-(2 \times V_{mpp} - V_{oc})}{a \times V_t} + \frac{(V_{mpp} \times I_{sc} - V_{oc} \times I_{mpp})}{(V_{mpp} \times I_{sc} + V_{oc} \times (I_{mpp} - I_{sc}))} \tag{3.13}$$

$$D = \frac{(V_{mpp} - V_{oc})}{a \times V_t} \tag{3.14}$$

and W_{-1} is the negative branch of the lambert W function.

$$R_{peq} = \frac{(V_{mpp} - I_{mpp}R_{seq})(V_{mpp} - R_{seq}(I_{sc} - I_{mpp}) - aV_t)}{((V_{mpp} - I_{mpp} \times R_{seq}) \times (I_{sc} - I_{mpp}) - aV_t I_{mpp})} \tag{3.15}$$

$$I_{ph} = \frac{(R_{peq} + R_{seq})}{R_{peq}} \times I_{sc} \tag{3.16}$$

3.3 Simulation And Experimental Results

3.3.1 Experimental Circuit Setup

In this study, the PV panel (model: Powertech-ZM9054) is selected as the reference PV panel to be mimicked. The PVE consists of a DC voltage source (operating at constant current mode), a diode string, and two of the electrical resistors, as shown in Fig. 3.3. The PVE components, such as R_{seq}, R_{peq}, N, and I_{ph}, are selected based on the MATLAB calculation of the mentioned mathematical equations of the real PV panel. The design component values are shown in Table 3.1. Equations (3.9), (3.10), (3.15), and (3.16) are used to calculate the parameters required to build the emulator circuit. A selected power diode (1n5400), with reverse saturation current (5×10^{-6}A), is used with I_{sc}, V_{oc}, I_{mpp}, and V_{mpp} values from the commercial datasheet, as shown in Table 3.2.

The number of power diodes (N) needed to mimic the real PV panel differs from one PV panel to another, and it can be calculated by using (3.9). The number of diodes for the proposed PVE is found below by considering the maximum operating temperature of the selected diode, which is equal to 150°C based on its datasheet.

$$N = \frac{((1.60217646\times10^{-19})\times(21.5))}{((1.85)\times(1.3806503\times10^{-23})\times(273+150)\times ln(\frac{0.65}{(5\times10^{-6})}+1))} = 27, \text{ where T equals (273+150)°C.}$$

The PVE circuit has been built and tested, as shown in Fig. 3.5. There are twenty-seven power diodes, and a DC voltage source (constant current mode) has been adjusted based on the open-circuit voltage and short circuit current of the mimicked PV panel, as well as the voltage and current of the DC voltage source (constant current mode). A programmable DC load (model: B&K Precision 8500, 300W) is

used to vary the output resistor to generate the I-V and P-V characteristics curves.

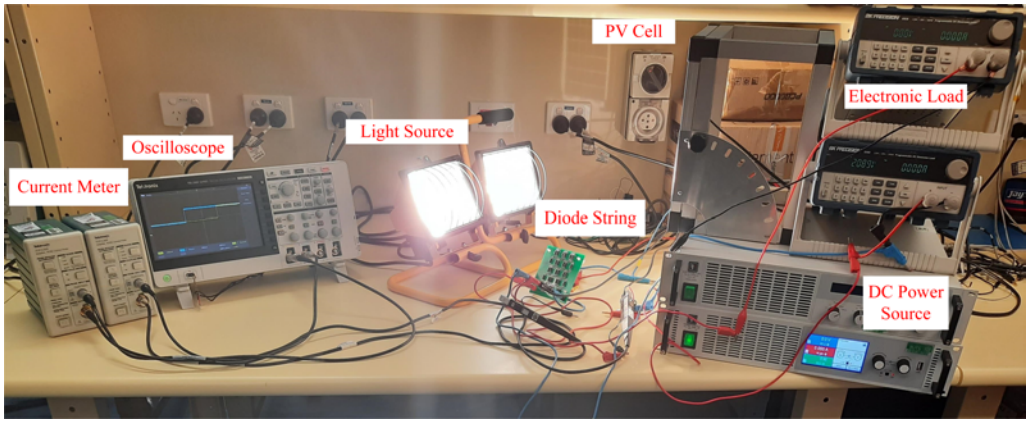


Figure 3.5: Experimental PVE in the lab.

Table 3.1: PVE parameters calculated by MATLAB

Parameter Name	MATLAB simulation value
R_{seq}	1.870488 (Ω)
R_{peq}	362.1797 (Ω)
N	27
I_{ph}	0.6533569 (A)

Table 3.2: Product information of the selected PV panel

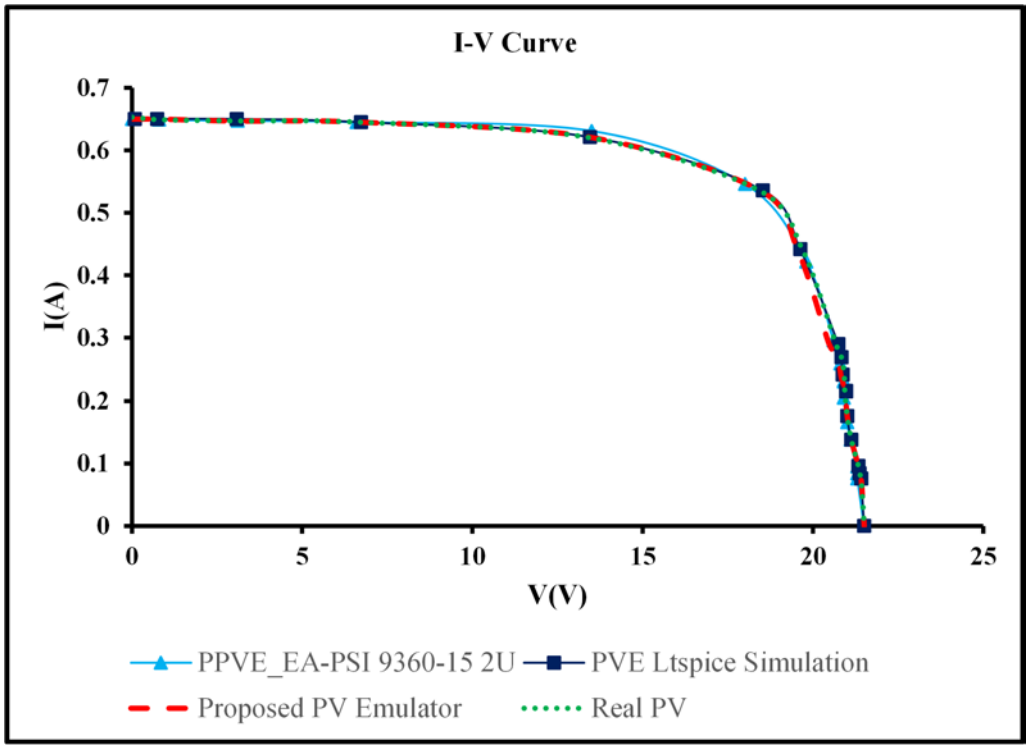
POWERTECH	
Model	ZM9054
Maximum Power (P_{mpp})	10W($\pm$5%)
Open Circuit Voltage (V_{oc})	21.5V
Short Circuit Current (I_{sc})	0.65A
Rated Voltage (V_{mpp})	17.5V
Rated Current (I_{mpp})	0.57A
Maximum System Voltage	1000V
Test Condition	AM1.5, 1000W/m^2, 25°C

3.3.2 Steady-state Response

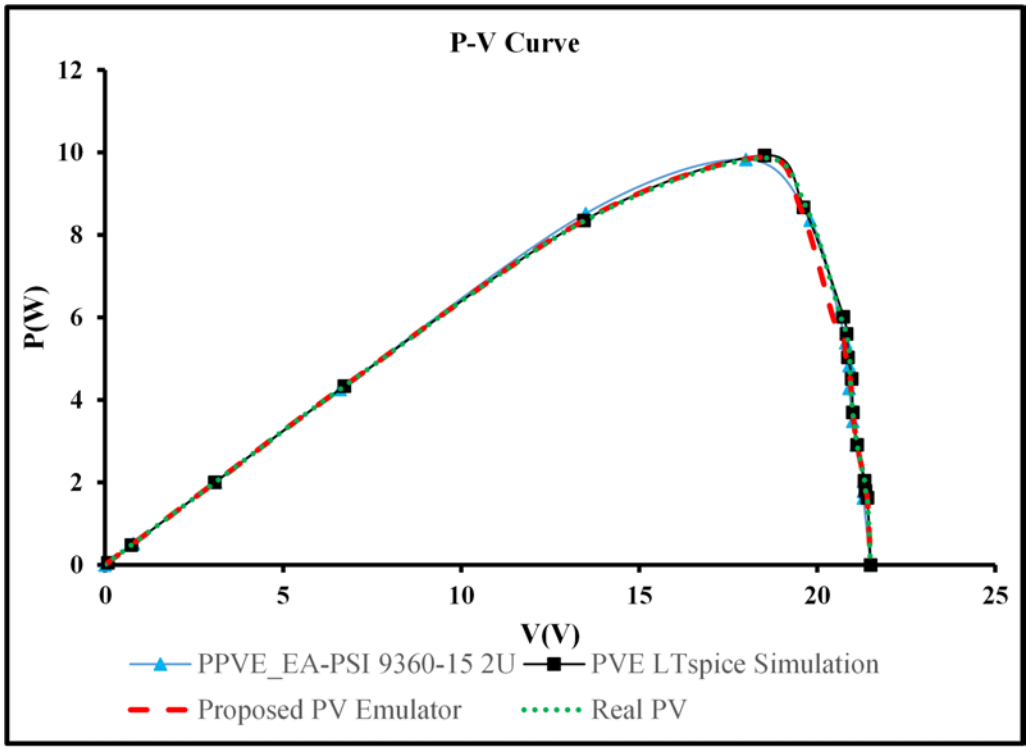
The experiment results agree with the simulation results, as shown in Fig. 3.6. Fig. 3.6 (a) shows the experimental I-V curve of the commercial programmable PVE device (PPVE, model: EA-PSI 9360-15 2U), PVE LTspice simulation, proposed PVE (based on diode string), and real PV panel (model: Powertech-ZM9054). Fig. 3.6 (b) shows the P-V curve for the same setup. It is clear from the real PV panel curve that the I_{sc} equals 0.65A and the open-circuit voltage equals 21.5V at $990W/m^2$ and 26°C. To simulate the same electrical characteristic, the DC power supply (constant current mode) is limited to 0.65A and the voltage set to 21.5V. The actual PV panel voltage and current are measured again at different irradiation levels ($760W/m^2$ at 27°C). The short circuit current drops to 0.513A, and the open-circuit voltage reduces to 21.2V. The voltage and current values are used as the input for the PVE. The I-V and P-V curves for the commercial programmable PVE, PVE LTspice simulation, proposed PVE, and real PV panel are plotted in Fig. 3.7. The proposed PVE shows high performance, where the output voltage and current match that generated by the real PV panel and commercial programmable PVE device.

The absolute deviation value (error) between the I-V curve of the actual PV panel and the one produced by the proposed PVE based on a diode string is used to indicate the inaccuracy. The results shown in Fig. 3.8 are according to (3.17), and by using a DC fan on full speed, as shown in Fig. 3.9. Fig. 3.8 (a) give the absolute error at the I_{sc} = 0.513A. The figure shows that the variation for a large part of the characteristic curve is less than 1% and is below 1.8% overall. In addition, Fig. 3.8 (b) presents the absolute error at I_{sc} = 0.65A, where the deviation for a large part of the I-V curve is less than 1.7% and is below 2.8% overall. In summary, the accuracy of the proposed PVE compared to the real PV system demonstrates the successfulness of the proposed PVE in regenerating the I–V characteristic curve at different irradiation levels.

$$Abs(Error)\% = Abs(I_{load_{realPV}} - I_{load_{PVE}}) \times 100 \tag{3.17}$$

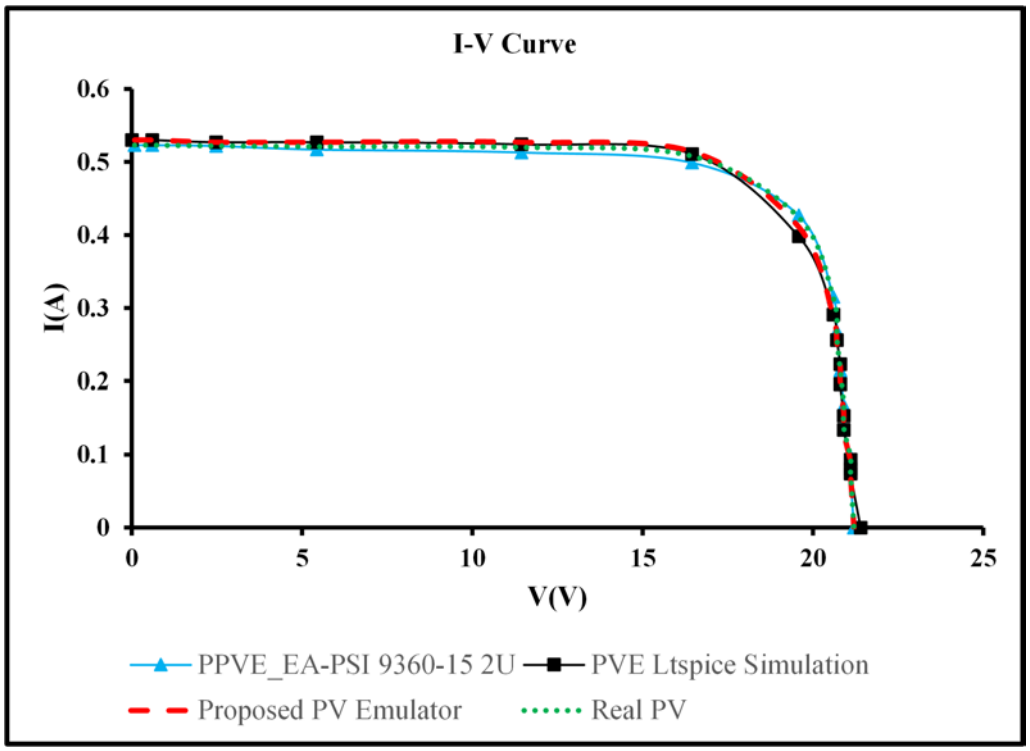


(a)

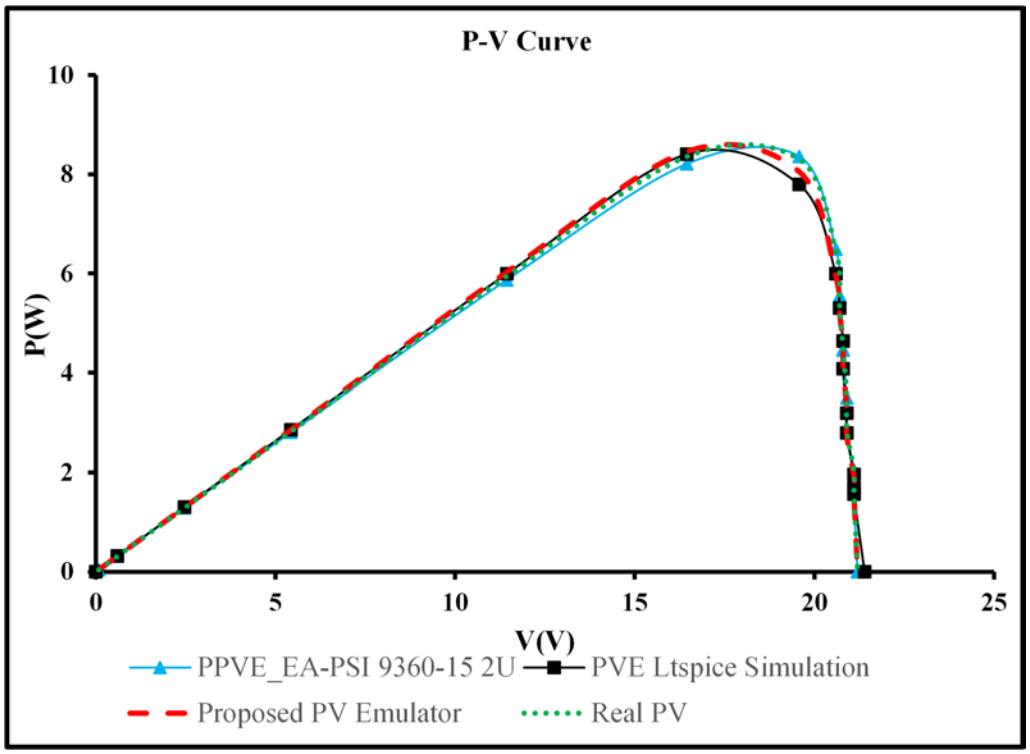


(b)

Figure 3.6: Experimental and simulation results at $I_{sc} = 0.65$A and $V_{oc} = 21.5$V: (a) I-V and (b) P-V characteristic curves.

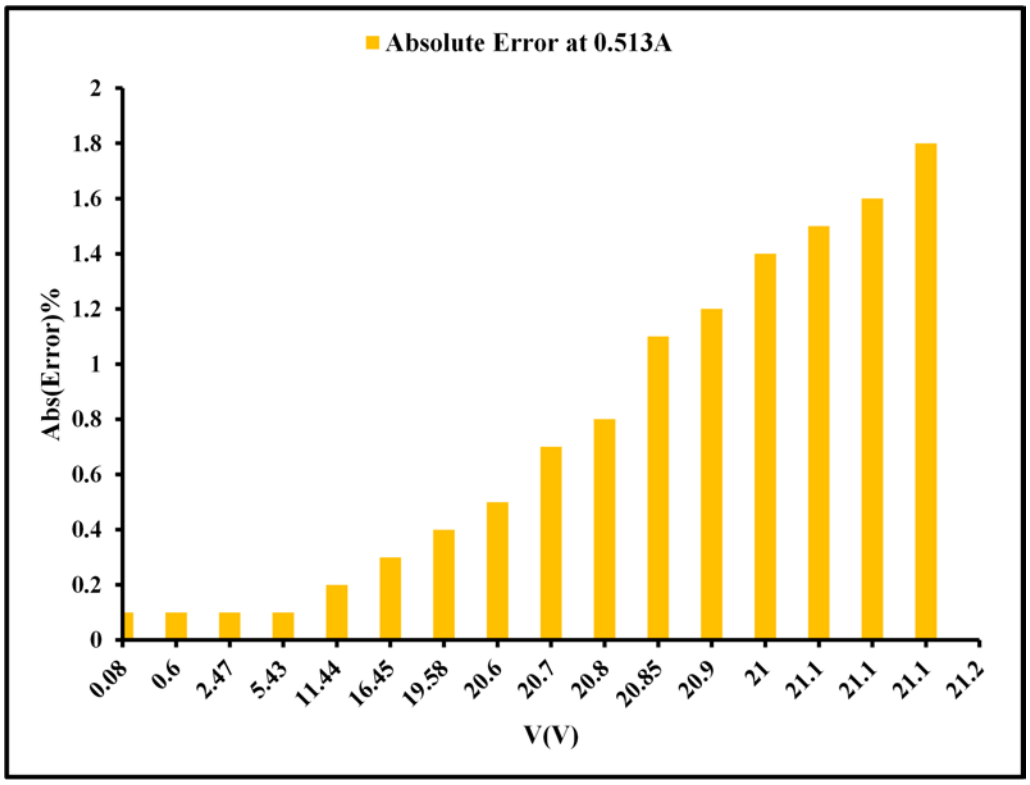


(a)



(b)

Figure 3.7: Experimental and simulation results at I_{sc} = 0.513A and V_{oc} = 21.2V: (a) I-V and (b) P-V characteristic curves.



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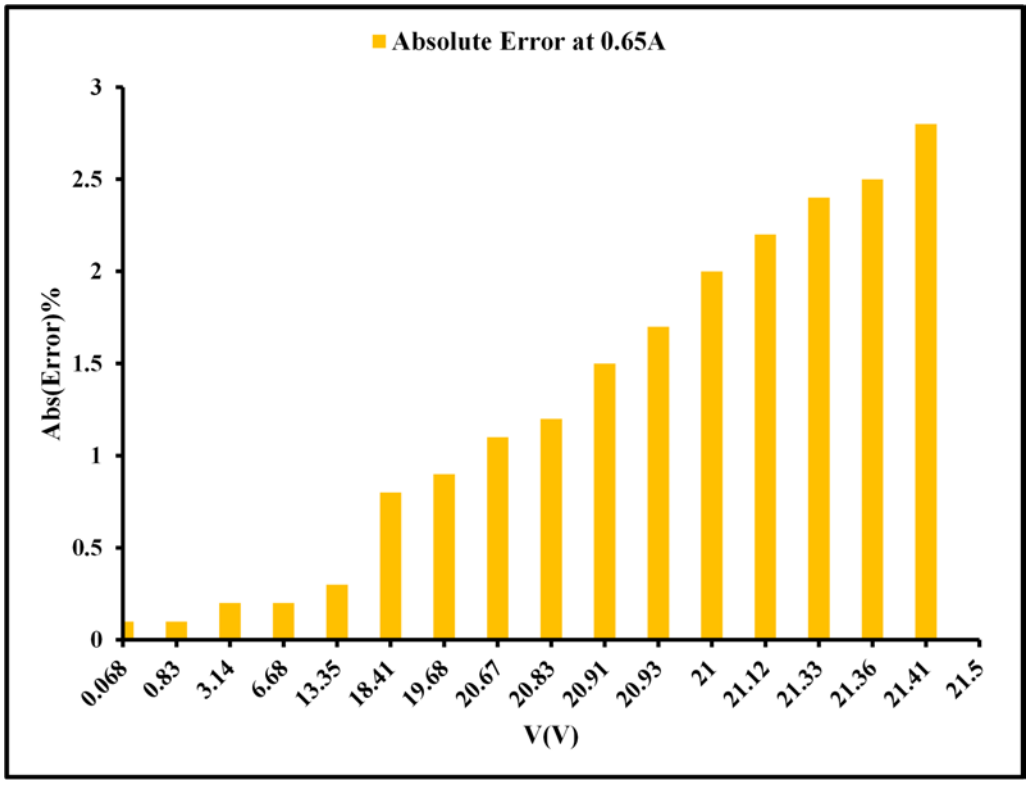


(b)

Figure 3.8: The maximum absolute deviation between the real PV panel I–V characteristic curve and the one generated by the PVE based on the diode string: (a) at I_{sc} = 0.513A and (b) at I_{sc} = 0.65A.

3.3.3 Thermal Behaviour Based on the Cooling System

In order to evaluate the impact of using a variable speed cooling system (12VDC, 0.24A, and 3 pin cooling fan PVA092G12M, in which the rated speed is 2500rpm and the airflow is 45CFM), different speed conditions starting from 0 up to full speed have been used. The fan speed is controlled by using a simple switching circuit and variable duty cycle.

Fig. 3.9 shows the thermal behaviour and the issues associated with using a single diode model to mimic the PV panel. The x-axis represents the duty cycle that controls the speed of the fan, whereas the y-axis shows the output resistive load connected with the PVE. In Fig. 3.9, when moving from the left to the right-hand side, the speed of the fan increases by increasing the duty cycle. When moving from bottom to top, the resistive load increases up to the point that the emulator reaches the open circuit operating condition. A thermal imaging camera (FLIR TG167) is used to capture the temperature change once the current increases.

In the figure, it is notable that the diode string temperature increases from 29.2°C to 98.3°C, without any cooling system (first column on the left). Subsequently, the cooling system (fan) is used at duty cycle D=0.25, and the diode string temperature increases from 29°C to 85.5°C. At D=0.5, the diode string temperature increases from 28.1°C to 76.5°C. At D=0.75, the diode string temperature increases from 27.2°C to 68.9°C, and finally, at D=1.0, the diode string temperature increases from 26.4°C to 56.7°C. The cooling system is used to keep the diode string temperature at an acceptable value to minimize the effects of high temperatures on the PVE characteristics.

3.3.4 Partial Shading Response

The series connection of the two groups of diode string using a bypass diode (1n5400) to mimic the electrical characteristics of the real PV panel (model: Powertech-ZM9054) under the PS condition is shown in Fig. 3.10. Each diode string has its own current source (irradiation level), and the two current sources have different values. The first current source value is I_{pha} at irradiation level a, and the second

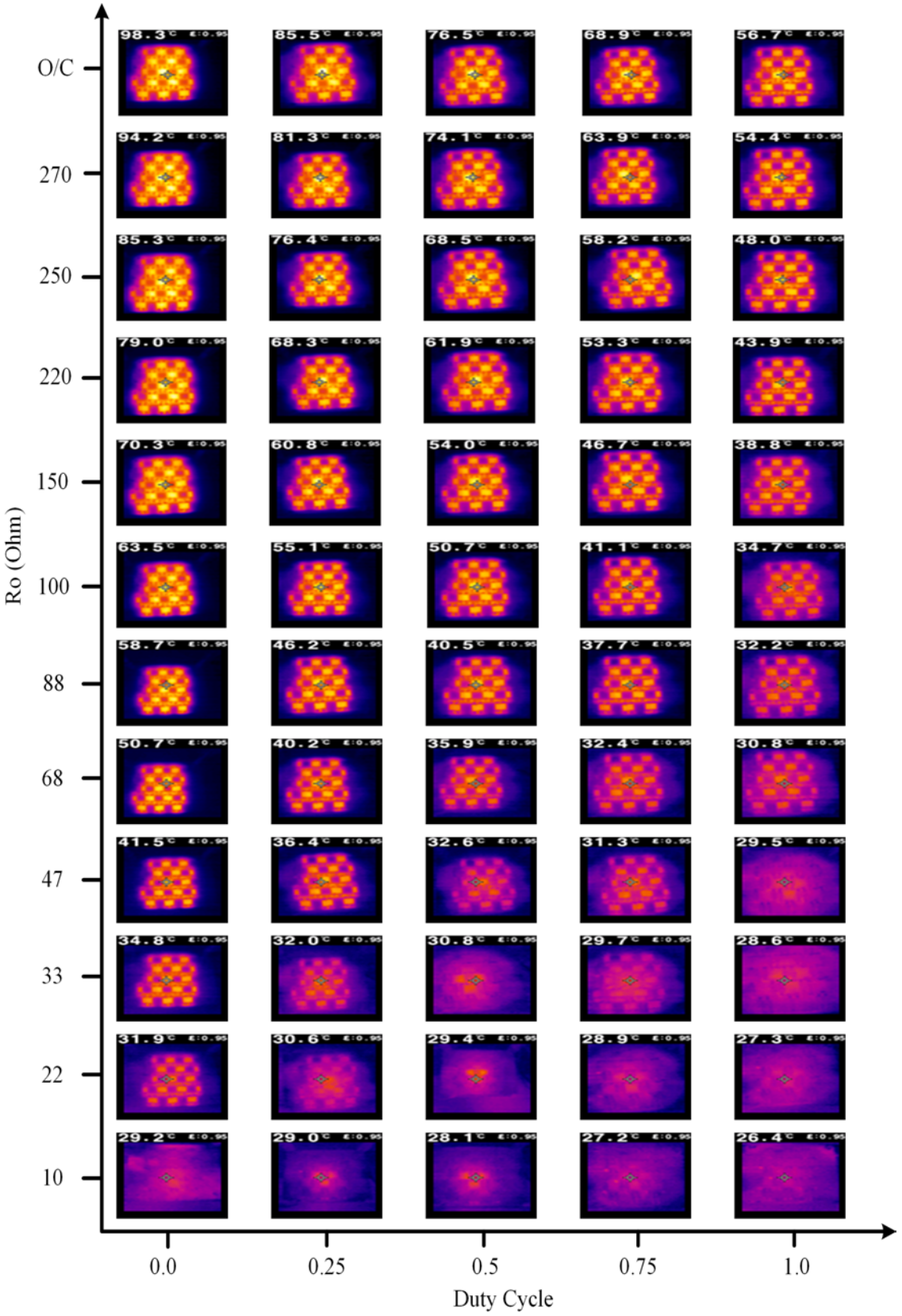


Figure 3.9: Thermal behaviour of the diode string at different operating conditions.

current source value is I_{phb} at irradiation level b, as shown in Fig. 3.10.

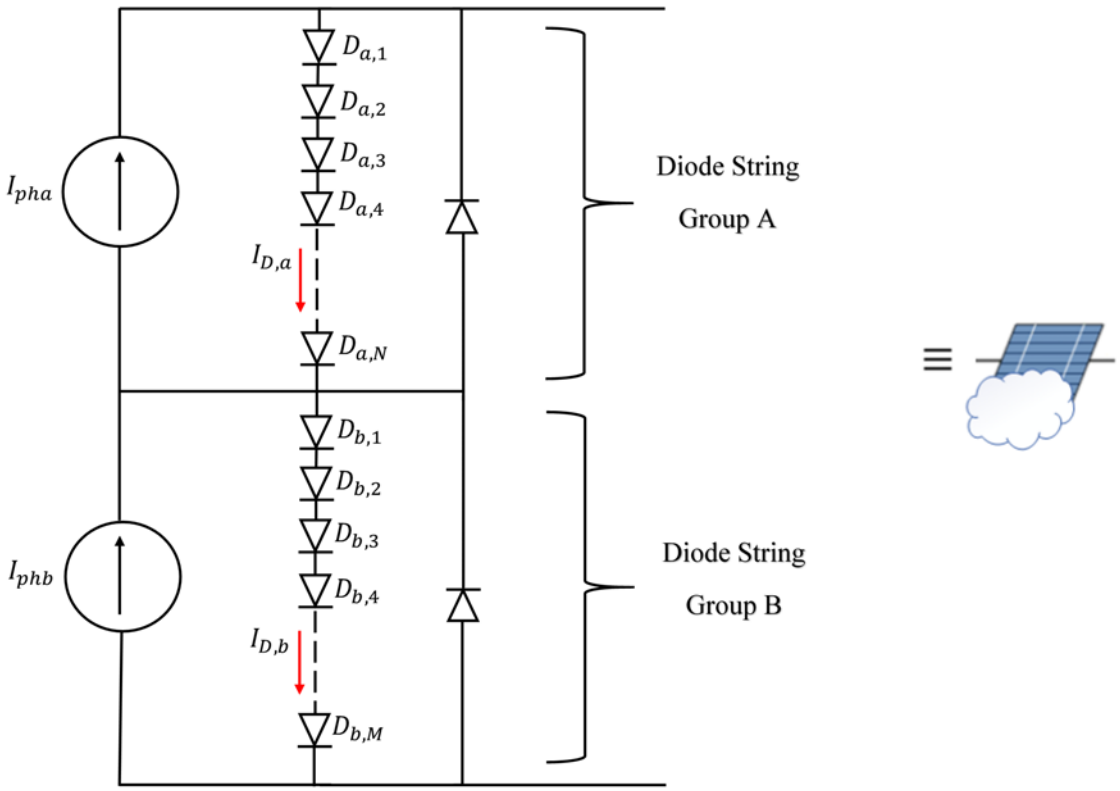


Figure 3.10: The series connection of the two groups of diode strings with different irradiation values (various currents) in order to mimic real PV panel behaviour in the PS and PVE under the PS condition by using bypass diodes, where $I_{D,a} \neq I_{D,b}$.

Figs. 3.11 and 3.12 show a comparison between the I-V and P-V characteristic curves based on experimental and simulation results for the real PV panel, proposed PVE, and LTspice simulation under the PS effect, respectively. Fig. 3.11 (a) shows the I-V curve under PS based on the same setup, as shown in Fig. 3.10. It is clear from the beginning of the real PV panel curve (i.e., the constant current region) that the I_{sc} equals 0.65A and the open-circuit voltage equals 21.5V at $990W/m^2$ and 26°C without any shading scenarios. After that, the real PV panel is affected by the partial shading, in which the output current drops to 0.42A at $646W/m^2$ and 26.5°C. To

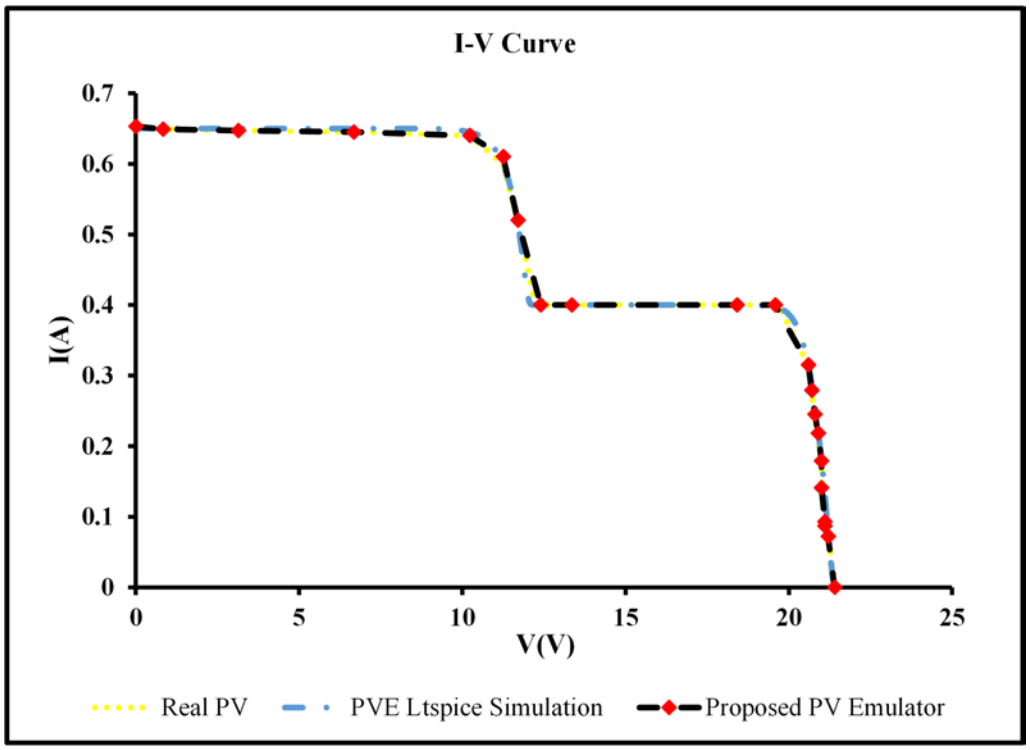
simulate the same electrical characteristic, the DC power supply (constant current mode) is limited to 0.65A for the first group of series-connected power diodes (I_{pha}). Furthermore, the current of the second group of series-connected power diodes (I_{phb}) is limited to 0.42A. In two cases, the limitation voltage is set to 21.5V.

The actual PV panel is affected by two levels of the PS, the first one when the irradiation level drops to $760W/m^2$ at 27°C, as shown in Fig. 3.12. After that, the second PS occurs, in which the irradiation level drops to $460W/m^2$ at 27.3°C. To simulate the same electrical characteristic, the DC power supply (constant current mode) is limited to 0.513A for the I_{pha} and to 0.42A for the I_{phb}, for the same experimental setup. In two cases, the limitation voltage is set to 21.2V. It is clear from the two figures that the proposed PVE mimics the actual PV panel perfectly, even under the PS effect.

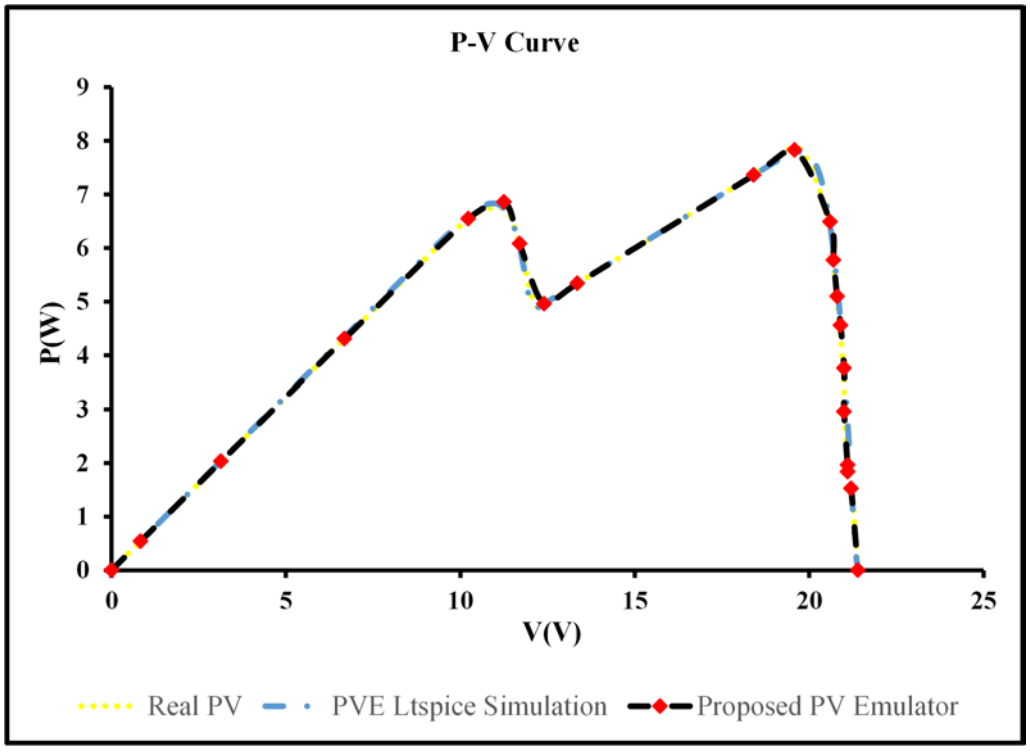
3.3.5 MPPT Test Using a Boost DC/DC Converter

In this section, another experiment is conducted to test and validate the proposed PVE during the dynamic MPPT test. Fig. 3.13 shows the P-V curves for the proposed PVE and the real PV panel under two different irradiation levels, where the performance of the proposed emulator and real PV panel are identical. The figure clearly shows that the PVE has two MPPs (point A and B). The voltage and current at the first MPP (point A) equal 17.6V and 0.55A, respectively. Meanwhile, the voltage and current at the second MPP (point B) equal 17.3V and 0.36A, respectively.

A boost DC/DC converter with a P&O algorithm is used to test the proposed PVE. The experimental setup is shown in Fig. 3.14. Fig. 3.15 shows the performance of the proposed PVE during the MPPT test. The top waveform represents the output voltage of the PVE side, followed by the output voltage of the boost converter side, followed by the output power, then the current of the PVE side. It is clear from the figure that the performance of the proposed PVE is not effected by the MPPT system used. On the other hand, the tracking system is able to track the MPPs, and the tracked current and voltage match the one shown in Fig. 3.13 at the same

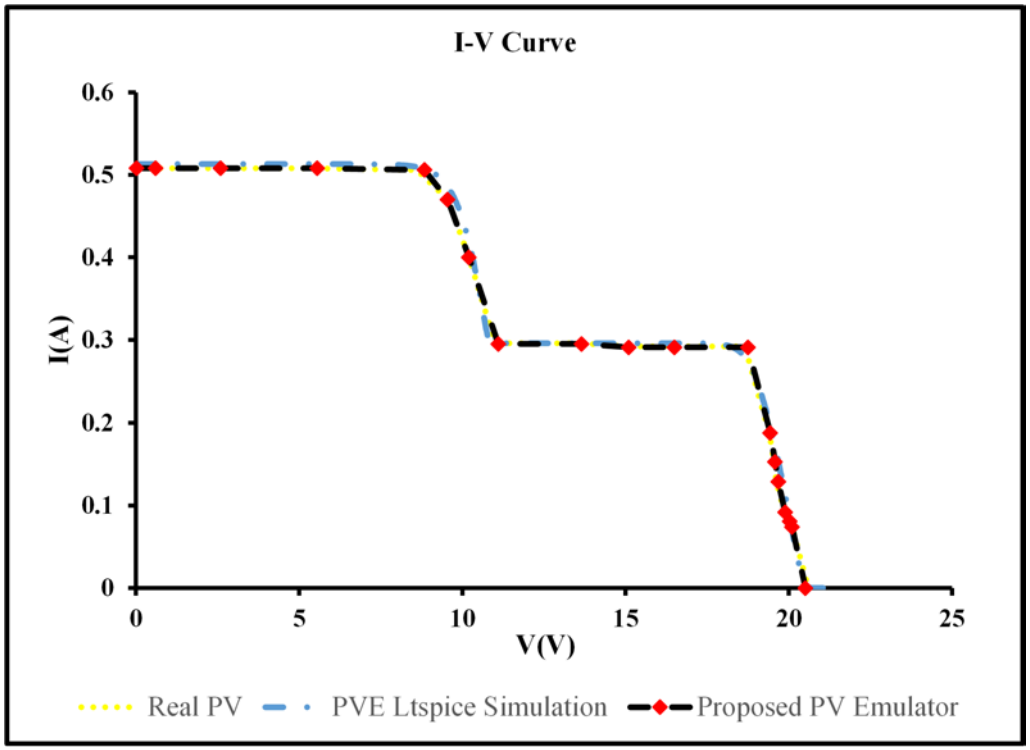


(a)

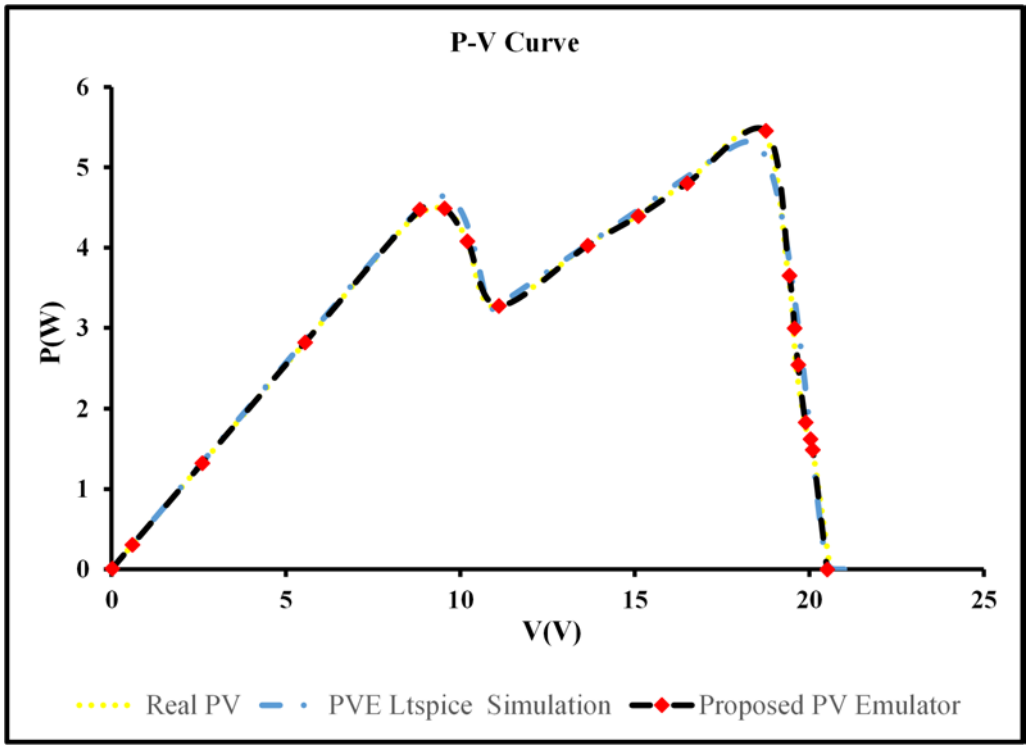


(b)

Figure 3.11: Experimental and simulation characteristic curves under the PS effect: (a) *I-V* curve and (b) *P-V* curve. Scenario 1.



(a)



(b)

Figure 3.12: Experimental and simulation characteristic curves under the PS effect: (a) I-V curve and (b) P-V curve. Scenario 2.

irradiation levels.

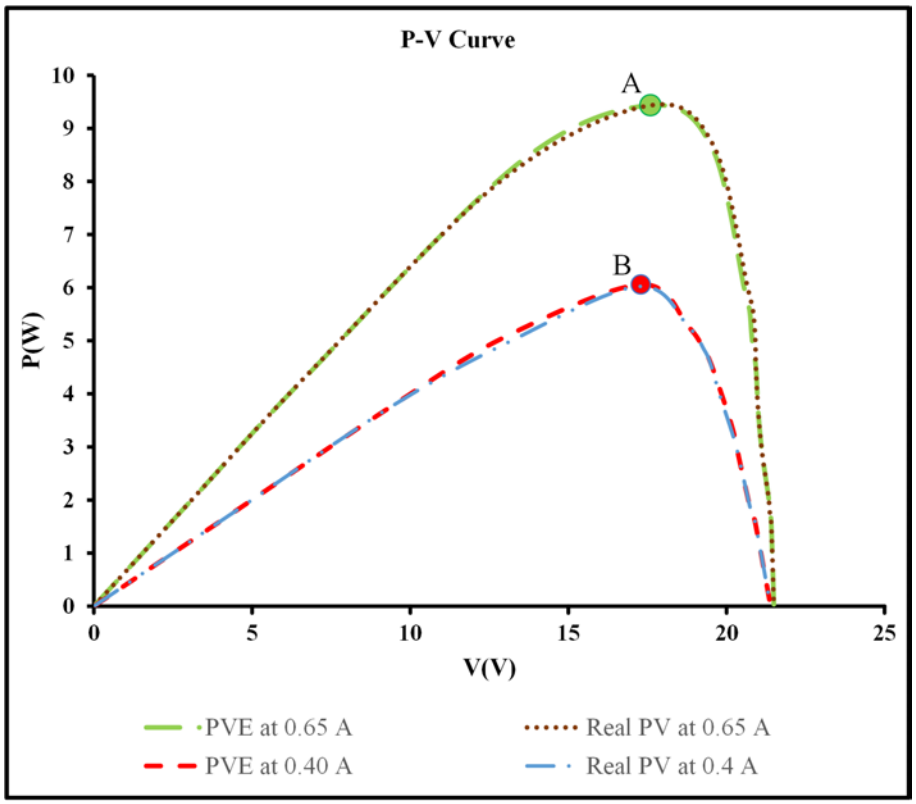


Figure 3.13: MPPT points based on a boost DC/DC converter.

3.3.6 Dynamic Characteristics

Fig. 3.16 shows a comparison of the dynamic behaviour between the PV panel (model: Powertech-ZM9054), the PVE based on diode string, and the programmable PVE device (PPVE, model: EA-PSI 9360-15 2U). The programmable electronic load is used to change the load resistance where the current changes from 0.185A to 0.385A. According to Fig. 3.16 (b), the PVE dynamic response lags around $3ms$ with respect to the real PV panel (model: Powertech-ZM9054). In addition, the programmable PVE (PPVE, model: EA-PSI 9360-15 2U) lags around $120ms$ with respect to the real PV panel (model: Powertech-ZM9054), as shown in Fig. 3.16 (a). The PVE based on the diode string is simple, but it is very effective, and it exhibits fast dynamic behaviour compared to both the real PV panel and the commercial PVE. The dynamic response of the proposed PVE also compares to some of the

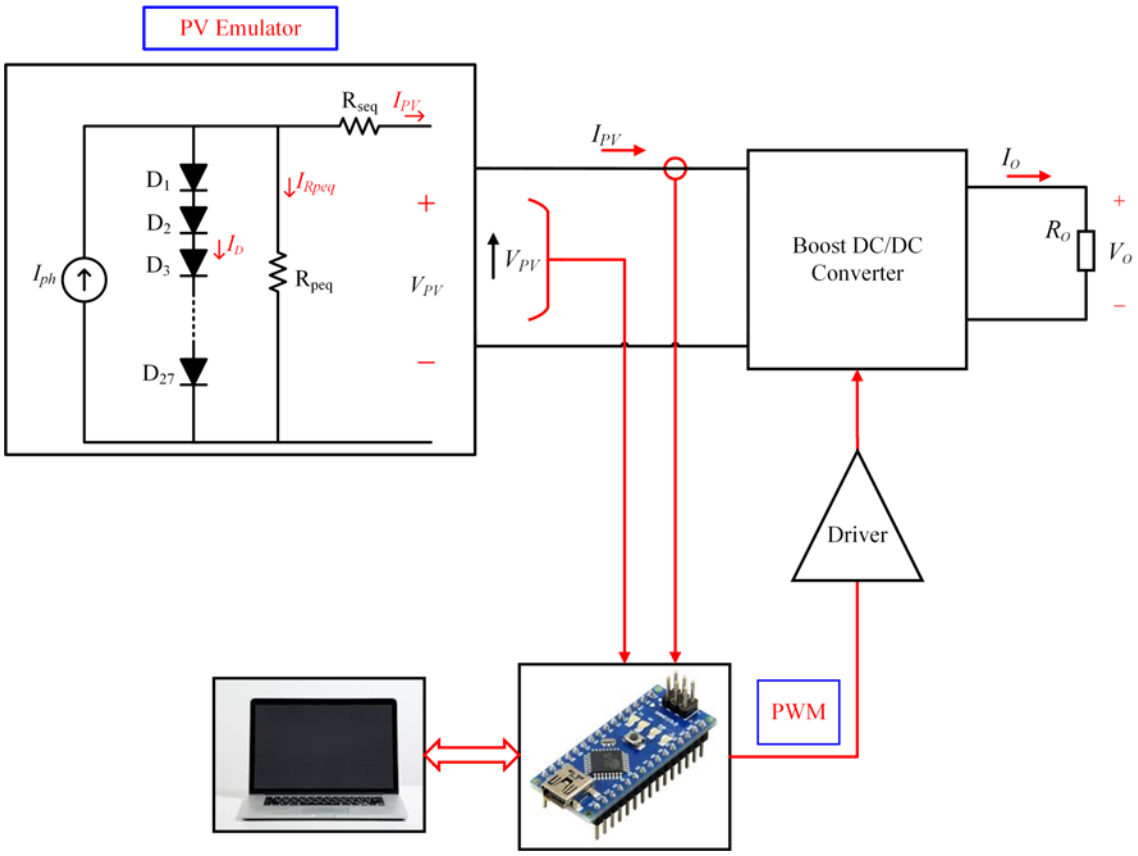


Figure 3.14: MPPT experiment setup.

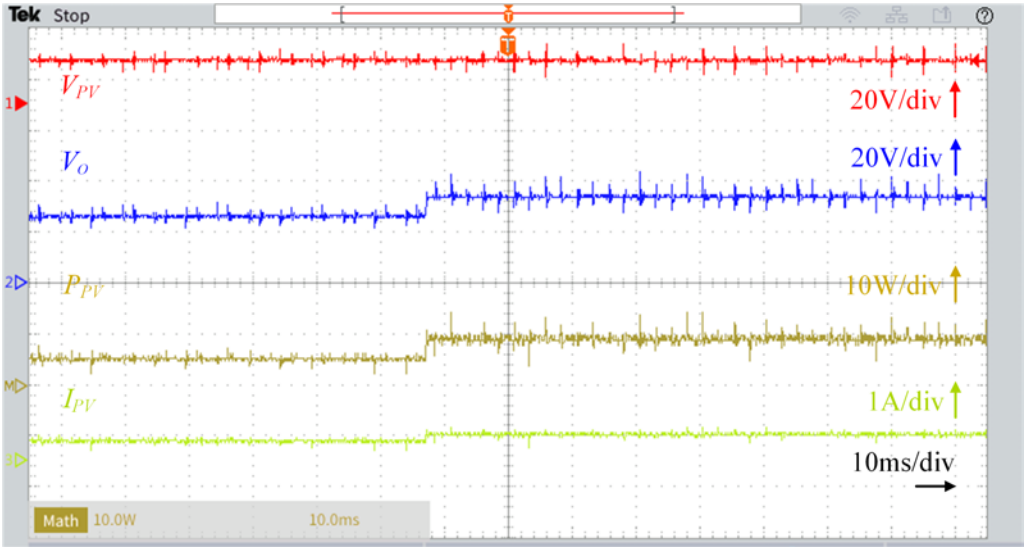
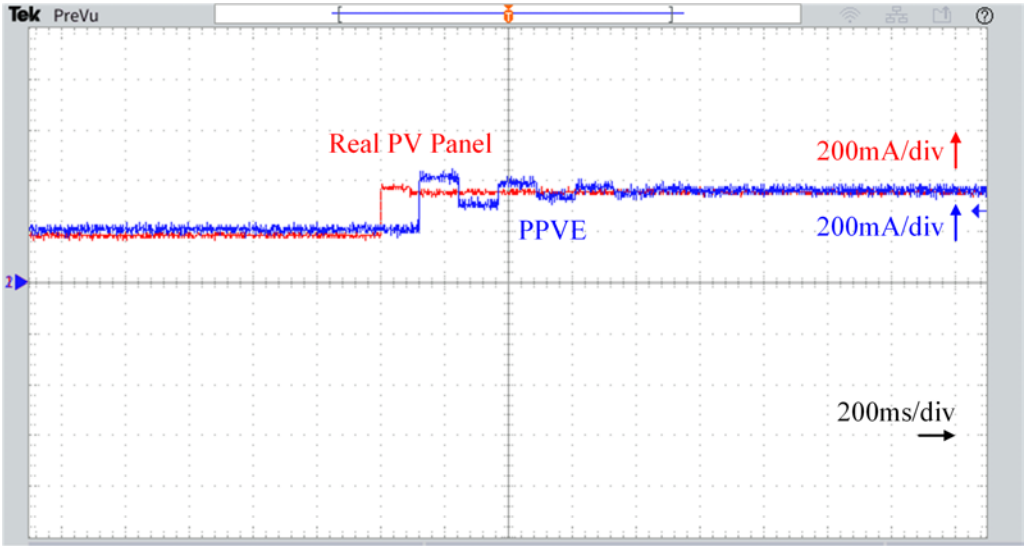
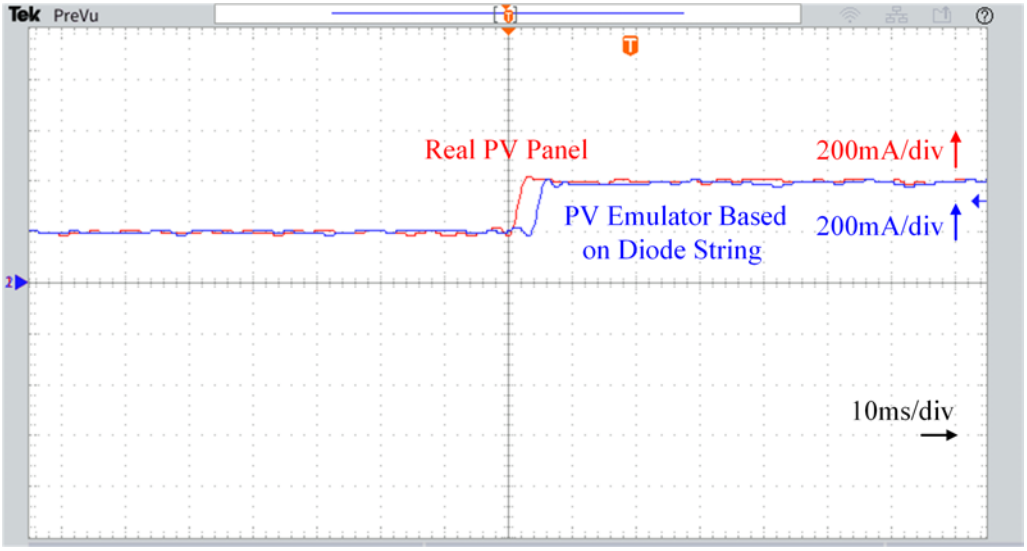


Figure 3.15: The dynamic response of the output power. Time base: 10ms/div. Ch1 (red): 20V/div. Ch2 (blue): 20V/div. Ch3 (green): 1A/div. ChM (yellow +1): 10W/div.



(a)



(b)

Figure 3.16: The dynamic PV characteristic when I_{PV} is converted from 0.185A to 0.385A based on load variation: (a) Real PV compared with the programmable PVE device (PPVE, model: EA-PSI 9360-15 2U), (b) Real PV compared with the PVE based on a diode string. Time base (a): 200ms/div. Time base (b): 10ms/div. I_{PV}: 200mA/div.

existing PVE platforms under the sudden output load change, in which the output current reaches a twice value, as shown in Table 3.3. The proposed emulator shows the best response time compared with the existing solutions.

Table 3.3: Dynamic response comparison between an existing platform and the proposed PVE

No.	Author\s (Ref.)	Converter used	Structural and control complexity	Dynamic response (ms)	Efficiency at MPP (%)
1	Cirrincione et al. [126]	Buck	Complex	160	≤ 93.5
2	EA-PSI 9360-15 2U [127]	SMPSU	Complex	120	≤ 93
3	Ayop and Tan [23]	Buck	Complex	21.25	93
4	Remache et al. [9]	Boost	Complex	18	≈ 90
5	Koran et al. [6]	Buck	Complex	3.8	≤ 90.2
6	Proposed PVE	Diode String	Simple	3	94.25

3.4 Summary

In this chapter, a new simple structure and cost-effective method for developing a PVE that can mimic a real PV system has been proposed and thoroughly described. It uses a number of power diodes and two resistors. The electro-thermal performances of series-connected PV cells have been studied. The LTspice simulation program is used to build the electrical model of the solar panel. In addition to simulation work, a thermal camera is used to investigate and capture the effect of temperature on the diode string. Unfortunately, the main problem of this design is the increase in the diode string temperature, specifically at the open circuit condition (i.e., the maximum power dissipation), where the diode string temperature increases from 29.2°C to 98.3°C with no cooling system. In this work, this problem has been considered and solved by adding a variable speed fan.

The proposed PVE exhibits high performance, where the generated power is identical to an actual PV panel and a commercial PVE. Furthermore, the dynamic response of the proposed PVE shows an improvement of 117ms compared to the commercial PVE device. In addition, the proposed emulator has been tested by using one of the well-known MPPT methods (P&O), and the result was close to the result obtained when the actual PV panel is used.

Chapter 4

Design of a Constant Current Source Converter for a PV-cell Equivalent Circuit-based Photovoltaic Emulator

4.1 Overview

In Chapter 3, a simple PVE based on the physical PV-cell model is proposed [40, 44]. It consists of a DC voltage source operating in constant current source mode (I_{ph}), a diode string, and two resistors. However, a DC voltage source operating in current limiting mode has been used to mimic the photocurrent (I_{ph}), including the temperature and solar irradiation effects. The DC voltage source has some limitations, such as limiting the maximum value of the DC current by using a simple DC power supply and the need for more than one DC power supply if simulating a multi-string of solar cells or panels. As a result, there is an increased need to design a constant current source converter (CCSC) for PVE applications.

The DC constant current source (CCS) can be implemented using a linear regulator or a switch-mode power supply (SMPS) [128]. The linear CCS has limited outputs, limited flexibility, poor efficiency, and high implementation costs for high-power applications. It is usually suitable for applications with a forwarding current of less than 100mA [129]. The SMPS is smaller, more efficient, and more flexible in its applications than linear power supplies [128]. The isolated SMPS can provide different output voltages independent of the input voltage [130]. This type suits applications with a forwarding current of a hundred milliamperes up to several amperes [128, 129]. Existing non-isolated DC/DC CCSCs can be implemented and are based on different types such as buck, buck-boost, half-bridge, SEPIC, and Ćuk converters, with the buck converter most commonly used [131]. Based on the previous comparison, the SMPS method is used in this study to design a CCS for the PVE application.

The authors of [128] presented a single inductor multiple-output (SIMO) buck-boost DC/DC converter as a constant current source converter for light-emitting diodes (LEDs) applications. The multi-output DC/DC flyback converter for the multi-channel LED is proposed in [132]. The operating principle is based on a load balancing capacitor, which is applied to multi-output systems. Every LED string is linked to a separate secondary winding of a flyback transformer since each LED string is wired to the other by a current balancing capacitor. The LED string current is

sensed and used as feedback to control the duty cycle of the power switch for the flyback converter. In [133] and [129], the authors proposed a single-stage multiple-output LED driver based on a DC/DC buck converter using a time-multiplexing (TM) control system, meaning that only one string is used in the closed-loop at any given time.

In this chapter, a PVE is first built using the physical PV cell model based on the key design equations shown in Chapter 3. In addition to the work presented in [40, 44, 52], the constant current source converter is proposed for PVE applications. Secondly, the CCSC is designed and tested to mimic the practical behaviour of the DC voltage source (operating at constant current mode). Based on the above literature review, the flyback DC/DC converter can be used for low-power applications. The power is less than 200W because of its electrical isolation, circuit simplicity, low cost, wide input voltage range, and high reliability [130, 134]. The buck DC/DC converter is known as one of the simplest and non-isolated current-type converters [128, 134, 135]. The single input single output (SISO) flyback-buck DC/DC converter is selected to design a constant current source converter (CCSC) for the PVE application, as shown in Fig. 4.2. Moreover, the flyback and the buck converters are controlled independently, as described in the following sections. The PVE using the proposed CCSC is studied and compared with a commercial 10W PV panel (model: Powertech-ZM9054) and the programmable PVE product (PPVE, model: EA-PSI 9360-15 2U).

The chapter is organized as follows: The system overview and converter selection are presented in Section 4.2. Section 4.3 illustrates the design by providing an example of the proposed PVE. The experimental results and discussion are presented in Section 4.4. Finally, Section 4.5 concludes the chapter.

4.2 System Overview and Converter Selection

4.2.1 Description of the PVE

The PVE system is shown in Fig. 4.1. It contains a DC voltage source (V_{in}), a DC/DC converter with a constant current output and wide output voltage range, a

string of diodes, a TMS320F28335-controller for sensing and controlling the output current (I_{ph}), and series or parallel resistors. A variable electronic load (model: BK8500), R_L, is used to test and verify the performance of the PVE, including the steady-state and dynamic behaviours.

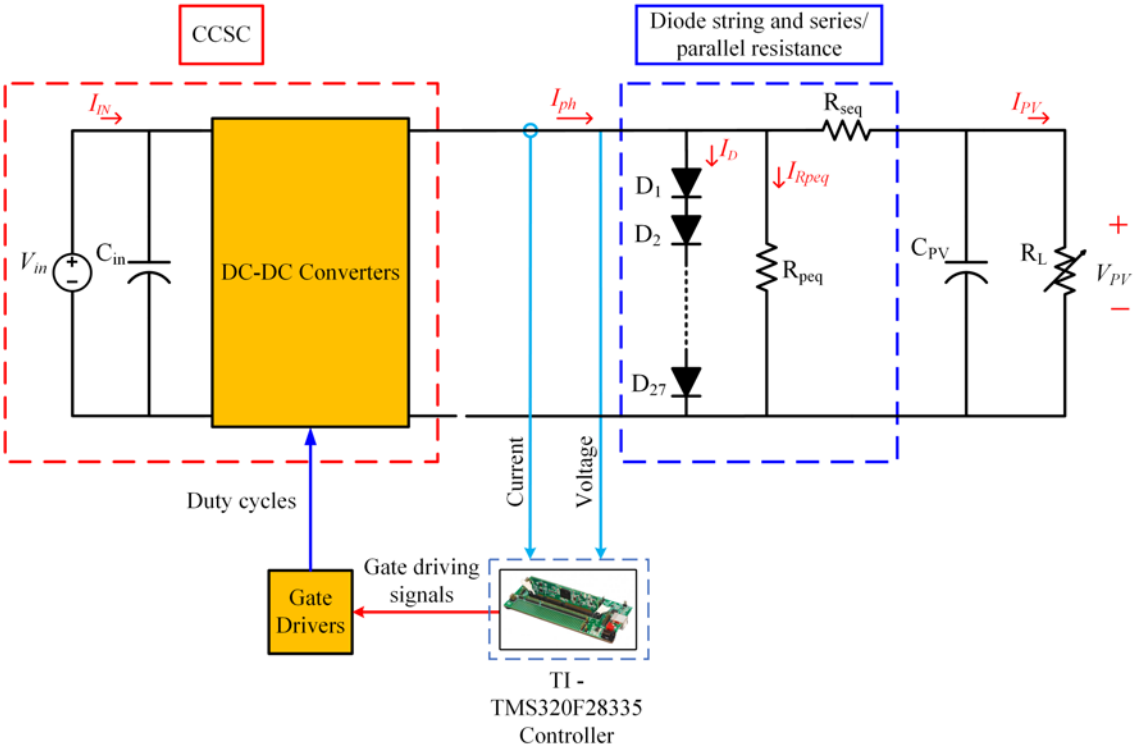


Figure 4.1: Block diagram of the proposed PVE.

4.2.2 Constant Current Source and Converter Selection

The selection criteria for the constant current source converter are simplicity, effectiveness, and ease of expansion. To mimic low power PV panels (<200W), types such as the buck, boost, and flyback converter can be used [128]. For high-power PV panels, half-bridge and full-bridge converters are popular options [130, 135]. Although a single power-stage design is straightforward, there are few options that provide both broad input and output operating ranges and a smooth output current. In this work, a two-stage flyback-buck converter is selected for implementing a low-power PVE. The flyback-buck converter combines the advantages of a wide op-

erating range and a smooth output current. Moreover, adding more outputs to the flyback converter and cascaded buck converters is straightforward should one want to scale up the emulator for other applications, such as multi-string and half-cell technologies.

4.3 Design Considerations of the Proposed PVE

The simplified circuit and connection diagram of the proposed PVE is shown in Fig. 4.2. A PVE was built and implemented based on a single diode PV model. The photovoltaic current (I_{ph}) is mimicked based on a series combination of flyback and buck DC/DC converter.

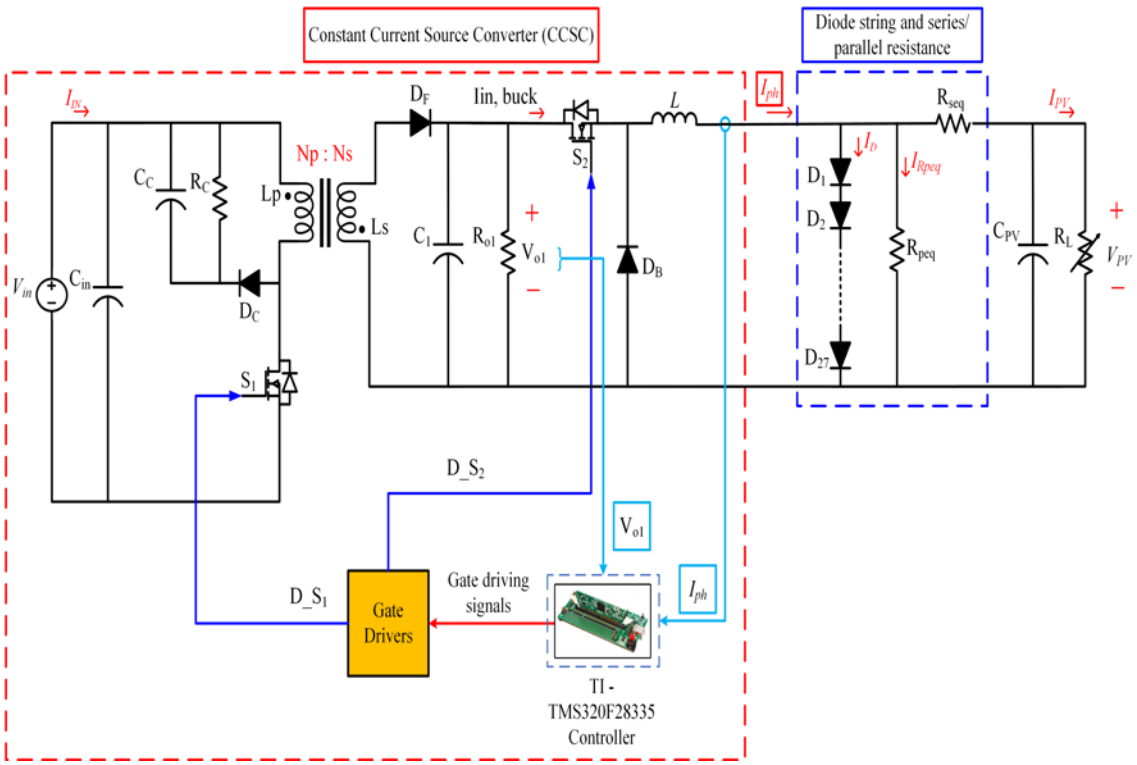


Figure 4.2: The flyback-buck DC/DC converter used to mimic a constant current source.

4.3.1 Power Stage

The converter parameters are designed based on the selected PV system (model: Powertech-ZM9054). The input voltage source of the flyback converter equals 21.5V,

and the output voltage (V_{o1}) is fixed at 43V based on the discrete proportional-integral (PI) controller. In addition, the buck output current is kept at a constant value, such as 0.65A (I_{sc} of selected PV panel), based on the hysteresis current control.

4.3.1.1 Design of Flyback Stage

The flyback DC/DC converter first-order model is used for its simplicity. The converter operates in discontinuous conduction mode (DCM) to avoid the right half-plane zero (RHPZ). The following assumptions are made to facilitate steady-state analysis [136, 137].

1. The input capacitor C_{in} is large enough to accept the input voltage (V_{in}) constant.
2. The output capacitors C_1 and C_{PV} are large enough to smooth the output voltage.
3. The leakage inductance is ignored.
4. All semiconductors are ideal.

According to the above assumptions, the voltage gain of the flyback converter in DCM is determined from the average volt-second balance of the inductor during the switching time under steady-state conditions and is expressed as [136–138]:

$$\frac{1}{T_s}(V_{in} \times D_1 \times T_s - \frac{V_{o1}}{n} \times D_2 \times T_s) = 0 \tag{4.1}$$

where $D_1 \times T_s$ is the on-time period of the primary switch and $D_2 \times T_s$ is the on-time period of the diode in the secondary winding. V_{o1} is the output voltage of the flyback converter. V_{in} is the input voltage of the flyback converter and n is the turn ratio of the flyback transformer.

$$\frac{V_{o1}}{V_{in}} = \frac{n \times D_1}{D_2} \tag{4.2}$$

According to the capacitor charge balance equation,

$$\frac{V_{o1}}{R_{o1}} = \frac{V_{in} \times D_1 \times D_2 \times T_s}{2 \times L_s} \tag{4.3}$$

substituting for D_2 from (4.2) in (4.3) yields the voltage ratio. The voltage ratio is given by the following expression:

$$V_{o1} = \frac{D_1}{\sqrt{K}} \times V_{in} \tag{4.4}$$

where,

$$K = \frac{2 \times L_s}{R_{o1} \times T_s} \tag{4.5}$$

where R_{o1} is the load resistance, L_s is the secondary winding inductance, and T_s is the switching period.

The turns ratio (n) of the flyback converter equals 0.5 based on the design specifications, the L_s is set to 2mH, and the L_p is calculated by using the equation below:

$$L_p = n^2 \times L_s \tag{4.6}$$

where n is the transformer turns ratio, L_p is the primary winding inductor value, and L_s is the secondary winding inductor value. Then, L_p is equal to 500uH.

4.3.1.2 Buck Stage Design

The buck inductor (L) is chosen to keep the converter operating in continuous conduction mode (CCM), as it generates less conduction loss. A $\pm$ 10% maximum current ripple in the inductor is selected at a 100kHz switching frequency. The minimum inductance, L_{min}, to meet this requirement is given by [84, 139]:

$$L_{min} = \frac{(1 - D) \times R_L}{2 \times f_s} \tag{4.7}$$

where D is the duty cycle of the power switches (S_2), f_s is the switching frequency, and R_L is the output load.

L_{min}= 80.27uH, and the inductor value is set at 15 times the L_{min} to keep converter in CCM and reduce the output current ripple. Table 3.2 shows the key parameters of the chosen PV panel (model: Powertech-ZM9054), where the maximum open-circuit voltage (OCV) is 21.5V and the minimum short-circuit voltage is 0V. The components used in this design are selected based on the datasheet of the selected PV panel (as seen in Table 3.2) and the flyback-buck components' power stress.

4.3.1.3 Design of the Diode String

The PVE is based on a physical single-diode PV model and can be divided into two parts. The first part is the diode string and series or parallel resistors, which are studied in-depth in [40, 44]. These studies include PV model equations, which consider $Rseq$, $Rpeq$, N, and I_{ph} to select the design parameters of the PV simulator to mimic an actual solar panel (model: Powertech-ZM9054). The second part is the DC constant current source converter, which is the main contribution of this work, as shown in Fig. 4.1.

4.3.2 Control Stage

The microcontroller used in this work is the 32-bit TMS320F28335 by Texas Instruments [140]. Analog to digital converters (ADCs) are used to sense the flyback output voltage (V_{o1}) and the output buck converter current, I_{ph}. The PWM signals for both the flyback and buck switches must be generated to keep the flyback output voltage (V_{o1}) at 43V and the output buck current (I_{ph}) at a specific value based on (2.9).

4.3.2.1 Voltage Controller Design for Flyback DC/DC Converter

The feedback loop compensation of a DC/DC converter is relatively simple in discontinuous conduction mode compared to continuous conduction mode. The converter output voltage is compared with the reference voltage, and the error generated is fed to the PI controller. This signal is then passed to the duty cycle modulator,

resulting in a suitable duty cycle to drive the power switch. The estimation of the controller parameters is given below.

The duty cycle to output transfer function based on the state-space first-order average model of the flyback DC/DC converter works at DCM and is presented by,

$$\frac{V_{o1}(s)}{d(s)} = \frac{V_{in}}{\sqrt{K}}\left(\frac{1}{1+\frac{sR_{o1}C_1}{2}}\right) \tag{4.8}$$

The transfer function in s domain of the PI controller is defined by,

$$\frac{d(s)}{e(s)} = K_p + \frac{K_i}{s} \tag{4.9}$$

where K_p is the proportional constant and K_i is the integral constant.

The transfer function of the PI controller and converter in the discrete-time domain is obtained by the backward Euler transformation method, where

$$s = \frac{1 - Z^{-1}}{T_s} \tag{4.10}$$

The PI controller transfer function is given by,

$$\frac{d(z)}{e(z)} = \frac{K_p(1 - Z^{-1}) + K_i T_s}{(1 - Z^{-1})} \tag{4.11}$$

The transfer function of the converter in the z domain is given by,

$$\frac{V_{o1}(z)}{d(z)} = \frac{V_{in}}{\sqrt{K}}\left(\frac{1}{1+\frac{(1-Z^{-1})R_{o1}C_1}{2T_s}}\right) \tag{4.12}$$

by pole-zero matching,

$$K_p = \frac{\sqrt{K}R_{o1}C_1}{2T_s} \tag{4.13}$$

and,

$$K_i = \frac{\sqrt{K}}{T_s} \tag{4.14}$$

The inverse of the z-transform of (4.11) represents the PI controller on a processor, provided by,

$$d[n] = d[n-1] + ae[n] + be[n-1] \tag{4.15}$$

where $d[n]$ represents the value of the duty ratio, $e[n]$ and $e[n\text{-}1]$ represent the present and the previous value of the errors. $a = K_p + K_i T_s$, and $b = K_p$. The a and b values are chosen after considering the L_s, R_{o1}, C_1, and T_s values.

4.3.2.2 Current Mode Digital Controller Design for the Buck Converter

The constant current control method is classified into three major types based on the control platform, namely sine triangle pulse width modulation (PWM), hysteresis, and predictive dead-beat. Hysteresis control is selected for this study due to its simple implementation. As mentioned in [141], the hysteresis control method has a quick dynamic response and does not require any data on the system parameters, which increases its robustness. The classical hysteresis current control (HCC) generates the control signal by comparing the current error $e(t)$ against fixed hysteresis bands. This current error is the difference between the desired current, I_{ref}(t), and the actual current, I_{actual}(t). If the error current exceeds the upper limit of the hysteresis band, the buck converter switch is turned OFF. If the error current crosses the lower boundary of the hysteresis band, the switch is turned ON, and if the current error value is between the upper and lower limit, then the previous switch state is maintained [142]. This work uses a constant frequency hysteresis current control method. In addition, the current reference value, the current density of the PV panel (I_{ph}), is proportional to the radiation level. It is also affected by the temperature, based on (2.9) [84].

4.3.3 Power Device Voltage and Current Stress Analysis

Assuming that the output voltage on the capacitor C_1 is constant and the power MOSFET and the diode are ideal switches, the maximum flyback voltage and current

stresses of the switch (S_1) and the diode (D_F) in discontinuous conduction mode (DCM) for a steady-state operation are:

$$V_{D_F} = \frac{V_{in,max}}{n} + V_{o1max} \tag{4.16}$$

$$I_{D_F} = \frac{nV_{in,max}D_{S_1}}{f_s L_P} \tag{4.17}$$

$$V_{S_1} = V_{in,max} + nV_{o1max} \tag{4.18}$$

$$I_{S_1} = I_{Lp,max} = \frac{V_{in,max}D_{S_1}}{f_s L_P} \tag{4.19}$$

The buck maximum voltage and current stresses of the switch (S_2) and the diode (D_B) in continuous conduction mode (CCM) for a steady-state operation are:

$$V_{S_2} = V_{D_B} = V_{o1max} \tag{4.20}$$

$$I_{S_2} = I_{D_B} = I_{ph,max} + \frac{\Delta I_{Lmax}}{2} \tag{4.21}$$

where ΔI_{Lmax} is the maximum current ripple in the inductor of the buck converter. Table 4.1 shows the chosen power diode and MOSFET switches. The current, voltage, and power ratings are selected based on the voltage and current stresses of the proposed design specifications.

4.3.4 Capacitor Design

To achieve a PV panel use with 98% efficiency, the voltage ripple at the input source should be below 8.5% of the MPP voltage [143, 144]. According to the above result, the lowest value of the PV panel filtering capacitor can be set as,

$$C_{PV} = I\frac{dt}{dv} = I_{mpp}\frac{1}{0.085V_{mpp}f_s} \tag{4.22}$$

The output and input capacitors of the DC/DC converter are designed based on the consideration given to the hold-up time requirement for the step-load. The minimum output voltage ripple shall remain below the required value, usually 1% of the output voltage. A nonzero time is needed to return the load voltage to the steady state, and this period is typically approximated as $1/(0.1f_s)$ [143, 144].

$$C_1 = I\frac{dt}{dv} = \frac{I_{o1}}{0.01V_{o1}(0.1f_s)} \tag{4.23}$$

4.4 Experimental Results and Discussion

The proposed CCSC for the PVE system application is tested and verified, and an experimental prototype is implemented, as shown in Fig. 4.3. The proposed emulator is tested on a 10W power module. The maximum OCV is 21.5V, and the I_{sc} is equal to 0.65A at standard operating conditions, as seen in Table 3.2. The performance of the PVE system based on the proposed CCSC is compared with a MATLAB/SIMULINK program, commercial programmable PVE (PPVE, model: EA-PSI 9360-15 2U), and a real PV panel. The experimental results show that the PV emulator performance is comparable with the simulation, commercial PVE, and actual PV panel. The steady-state and dynamic behaviour have been considered for the proposed approach.

Fig. 4.4 shows the experimental steady-state results for the proposed CCSC, with the output current (I_{ph}) fixed at 0.65A. In Fig. 4.4 (a), the top waveform represents the output current (I_{ph}), followed by the PWM signal generated from the TI-TMS320F28335 controller, then the high side driver (IR2184) PWM signal at 22Ω resistive load. Fig. 4.4 (b) has the same setup and shows the previous waveform at 47Ω resistive load. It is clear from the figure that the duty cycle changes to keep the output current constant at various load values. The experimental steady-state results for the proposed CCSC are shown in Fig. 4.5, with the output current (I_{ph}) fixed at 0.424A. In Fig. 4.5 (a), the top waveform represents the output current (I_{ph}), followed by the ePWM signal generated from the TI-TMS320F28335 controller, then the high side driver (IR2184) PWM signal at 22Ω resistive load. Fig.

Table 4.1: Circuit parameters component selection

Component	Model/Value
Digital Controller	TMS320F28335
Switching Frequency	100kHz
MOSFET	IRF540N
MOSFET Driver for S_1 (Flyback converter)	TC4428
MOSFET Driver for S_2 (Buck converter)	IR2184PBF
Diode (Flyback & buck)	MBR20200CT
D_1,...D_{27}	1N5400
Current Sensor	ACS712-5A
Inductor Core (Buck)	RM14/I-3C95
Coupled Inductor Core (Flyback)	RM10/I-3C95
N_P/N_S (Flyback)	1/2
Buck Inductor (L)	1mH
L_P	500uH
L_S	2mH
C_{in}, C_1 & C_{PV}	470uF
C_C	0.1uF
D_C	UF4004
R_C	40KΩ
Programmable PVE Device	EA-PSI 9360-15 2U
Programmable DC Electronic Load	BK8500
Electronic Load	EA-EL 9750-25

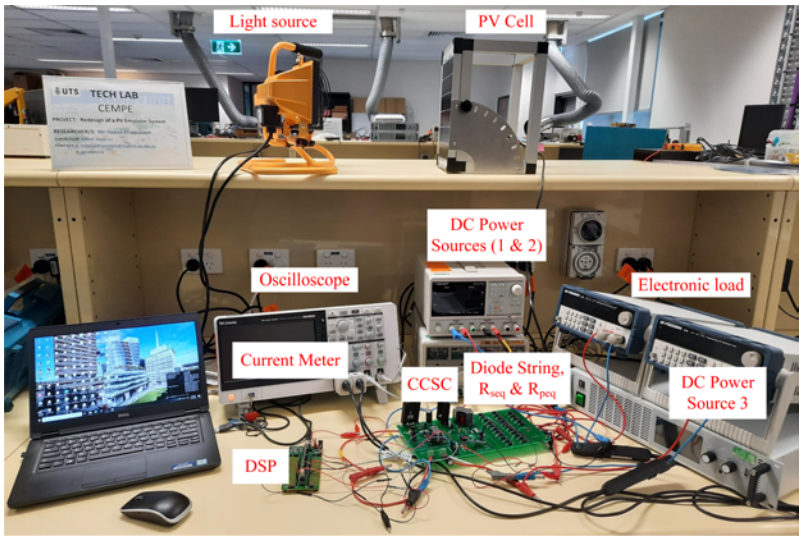
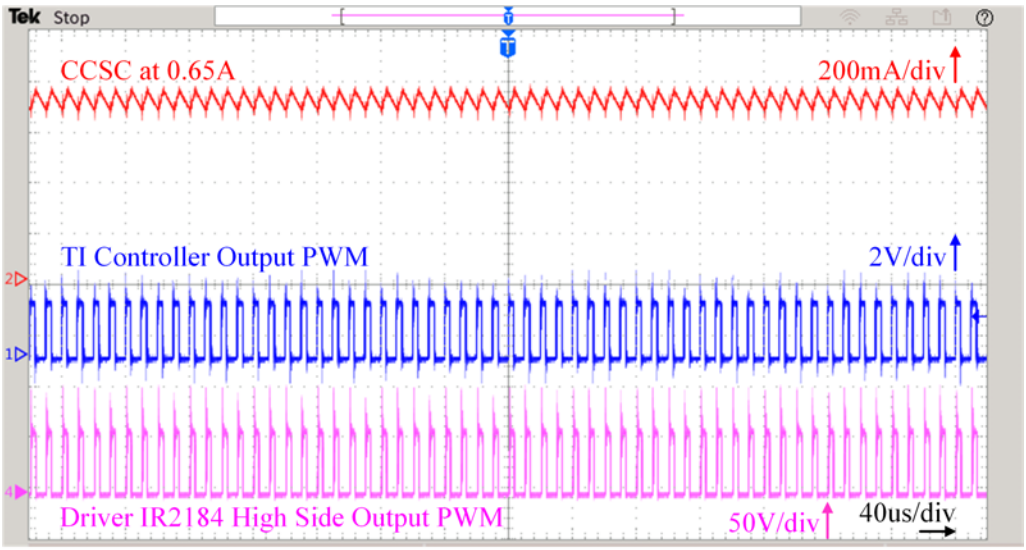


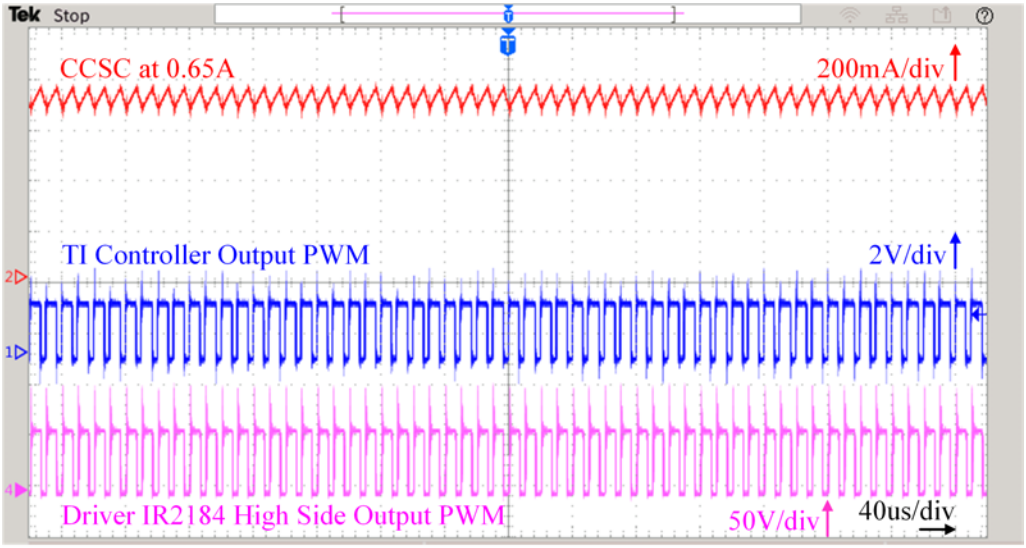
Figure 4.3: Laboratory prototype.

4.5 (b) has the same setup, showing the previous waveform at 33Ω resistive load.

Figs. 4.6 and 4.7 show a comparison between the I-V and P-V curves based on the experimental and simulation results for the proposed PVE, the PVE MATLAB simulation based on the CCSC, the commercial programmable PVE device (PPVE, model: EA-PSI 9360-15 2U), and the real PV panel (model: Powertech-ZM9054). Fig. 4.6 (a) shows the I-V curve, and Fig. 4.6 (b) shows the P-V curve for the same setup. From Fig. 4.6, it is clear that the actual PV panel short circuit current (I_{sc}) equals 0.65A and the OCV equals 21.5V at $990W/m^2$ and 26°C. To simulate the same electrical characteristic, the CCSC is controlled to keep the I_{ph} equal to 0.65A, with the current reference value calculated based on (2.9) considering the effects of solar radiation and temperature. The real PV panel current and voltage are measured again at another irradiation and temperature level ($655W/m^2$ at 26.5°C), at which the short circuit current drops to 0.424A and the OCV decreases to 21.3V. The current and voltage values are used as input for the PVE, where the CCSC is controlled to keep the I_{ph} equal to 0.424A, and the current reference value can be calculated based on (2.9) by including the effects of solar radiation and temperature. The I-V and P-V curves for the commercial PPVE, PVE MATLAB simulation, proposed PVE, and actual PV panel are plotted in Fig. 4.7. The proposed PVE exhibits

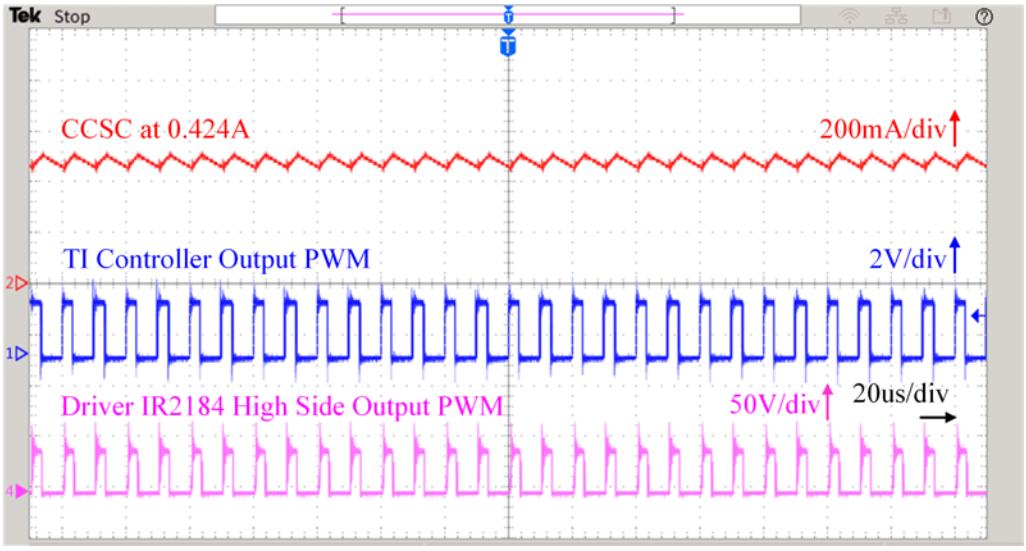


(a)

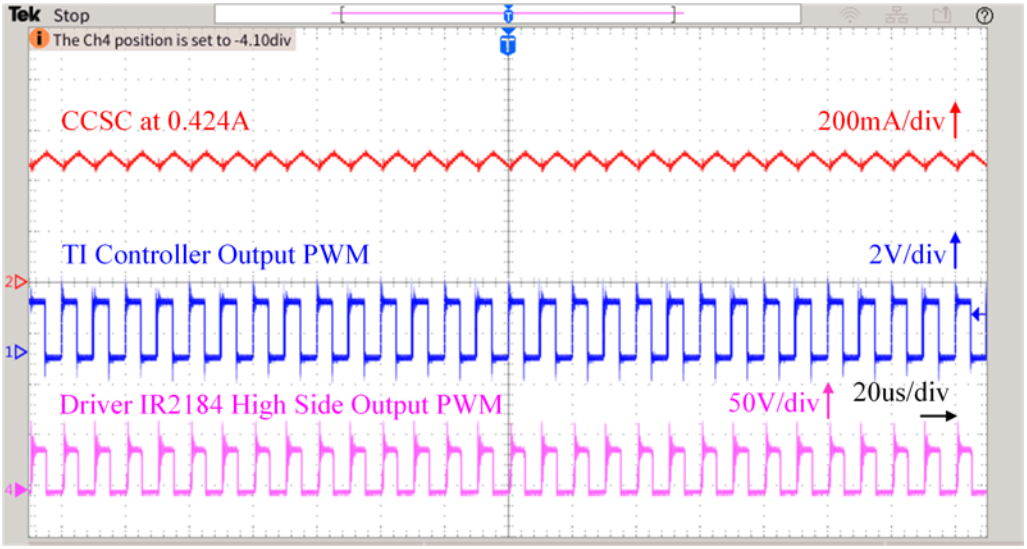


(b)

Figure 4.4: The output current of the proposed CCSC at different loads and constant output currents, I_{ph} = 0.65A: (a) At 22Ω and (b) At 47Ω. Time base: 40us/div. Ch1 (blue): 2V/div. Ch2 (red): 200mA/div. Ch4 (pink): 50V/div.

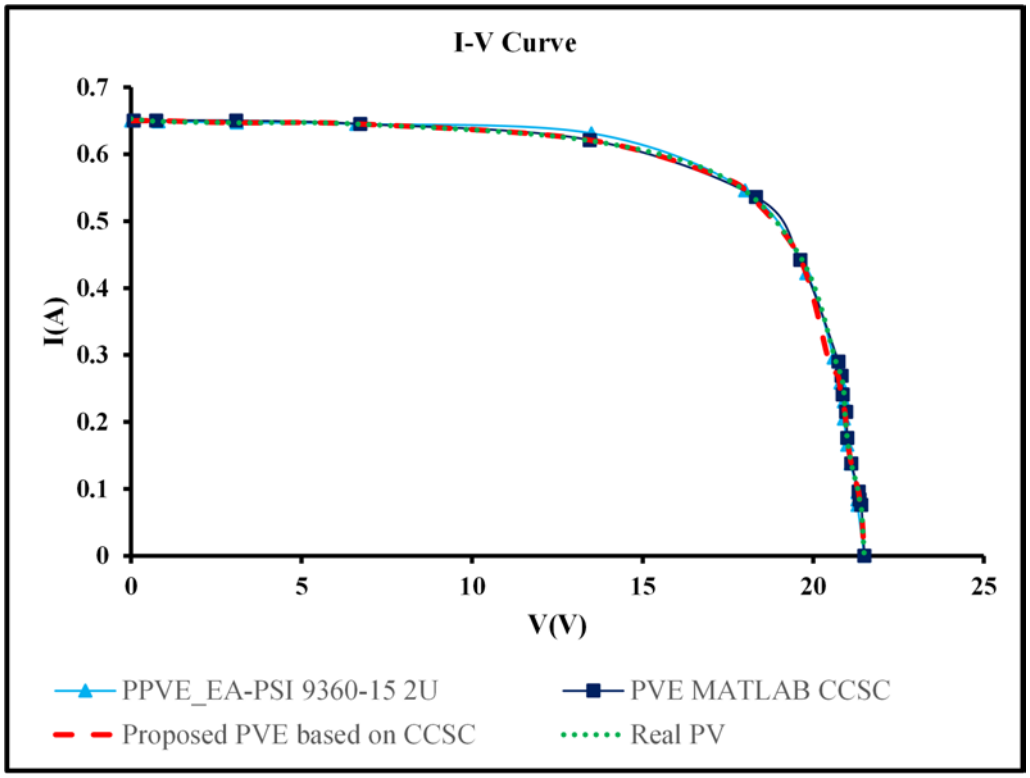


(a)



(b)

Figure 4.5: The output current of the proposed CCSC at different loads and constant output currents, I_{ph} = 0.424A: (a) At 22Ω and (b) At 33Ω. Time base: 20us/div. Ch1 (blue): 2V/div. Ch2 (red): 200mA/div. Ch4 (pink): 50V/div.



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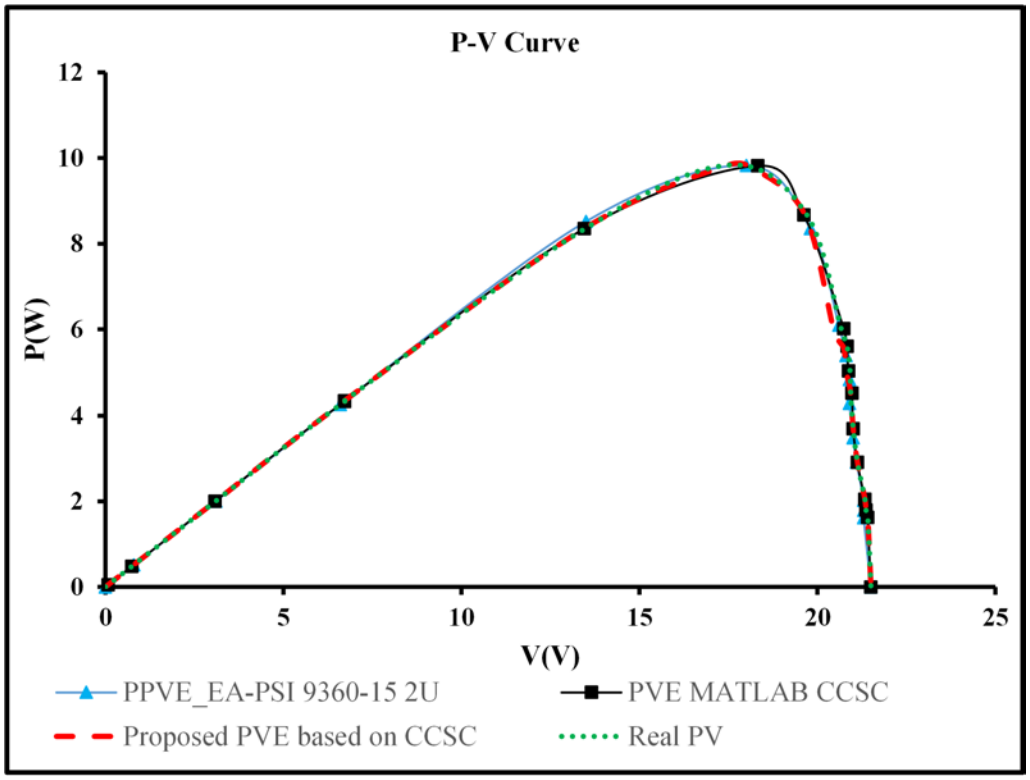


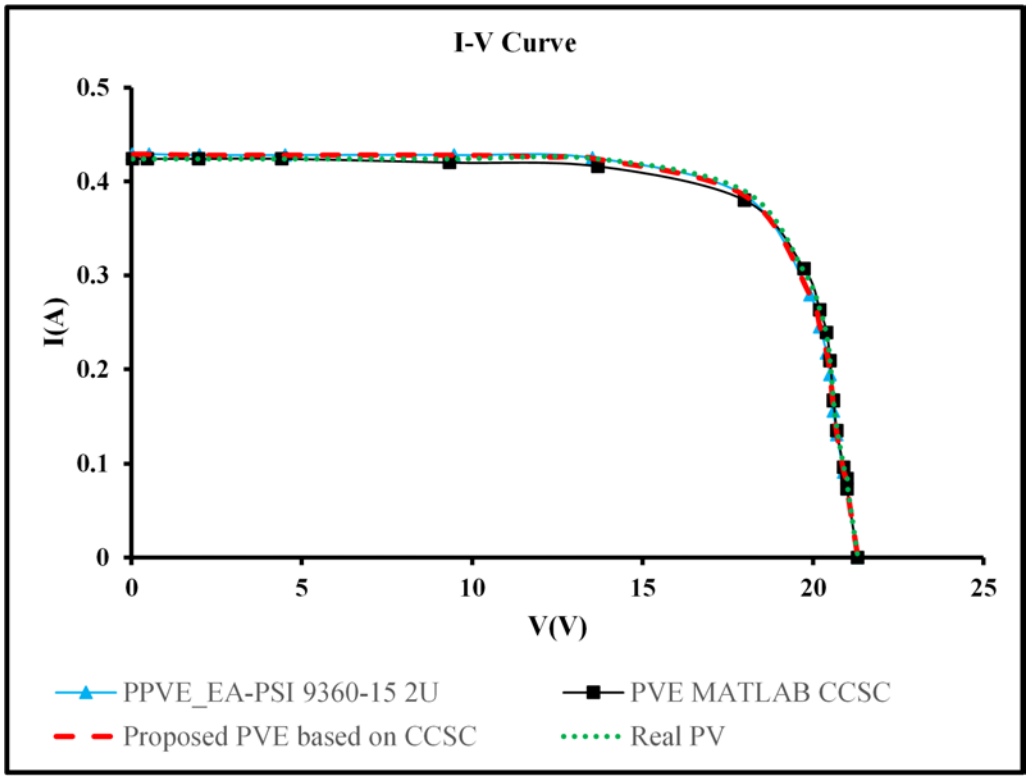
(b)

Figure 4.6: The characteristic curve of the PVE compared with the actual PV panel, MATLAB simulation, and commercial PVE at $I_{sc} = 0.65$A: (a) I-V curve and (b) P-V curve.

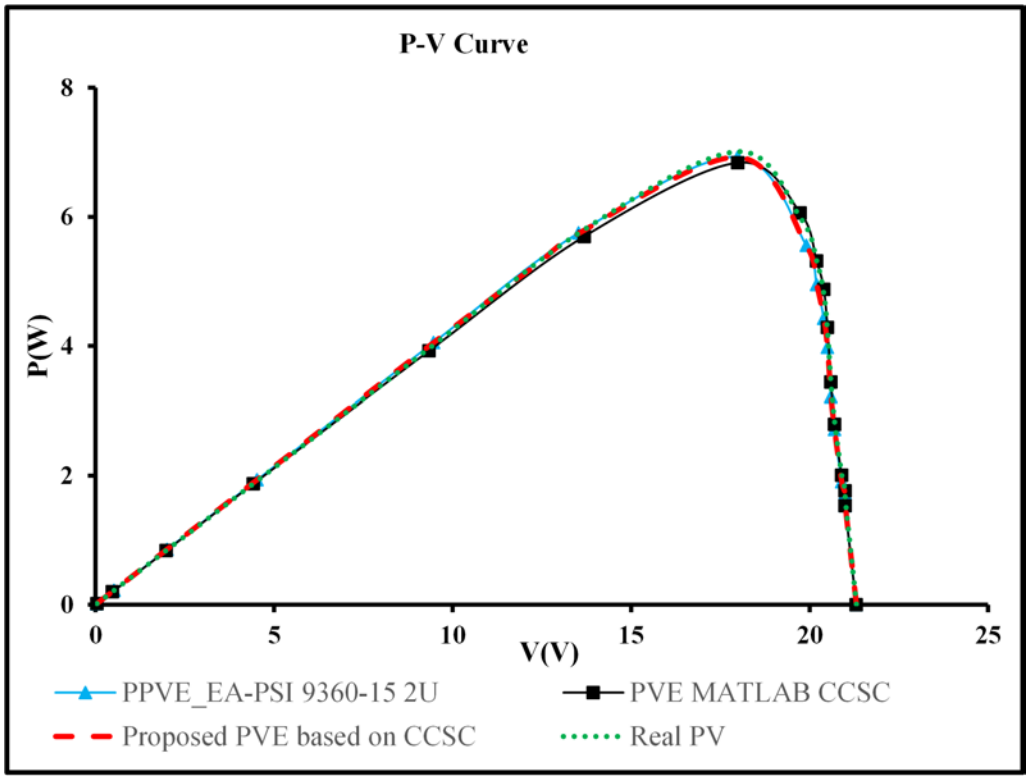
high performance, with the output voltage and current matching that generated by the real PV panel and commercial programmable PVE device.

Fig. 4.8 presents the dynamic behaviour of the proposed constant current source converter based on the weather conditions (irradiation and temperature conditions). As an example, the reference value is changed from 0.424A ($655W/m^2$ at 26.5°C) to 0.65A ($990W/m^2$ at 26°C). From the figure, it is clear that the proposed CCSC is able to track the new reference value during varying weather conditions. Fig. 4.8 (a) shows the dynamic response when the time scale is equal to 200ms/div. However, to measure the time needed to swap between two reference values, the time scale extended to 10ms/div, as seen in Fig. 4.8 (b). The proposed CCSC requires approximately 1.7ms to reach a new reference value.

The dynamic response of the actual PV panel, PVE, and programmable PVE device (PPVE, model: EA-PSI 9360-15 2U) are shown in Fig. 4.9. It showed a comparison when I_{PV} varied from 0.185A to 0.385A according to the programmable electronic load (model: BK8500). From Fig. 4.9 (a), the PVE based on the CCSC shows a dynamic response that lags around 10ms compared with the actual PV panel. Nevertheless, the programmable PVE lags around 120ms with respect to the real PV panel, as shown in Fig. 4.9 (b). The PVE based on the CCSC is very effective, and its dynamic behaviour is acceptable compared to both the actual PV panel and commercial PVE, with an increased time response of 110ms. This increase comes from the fast dynamic response of the power diode.

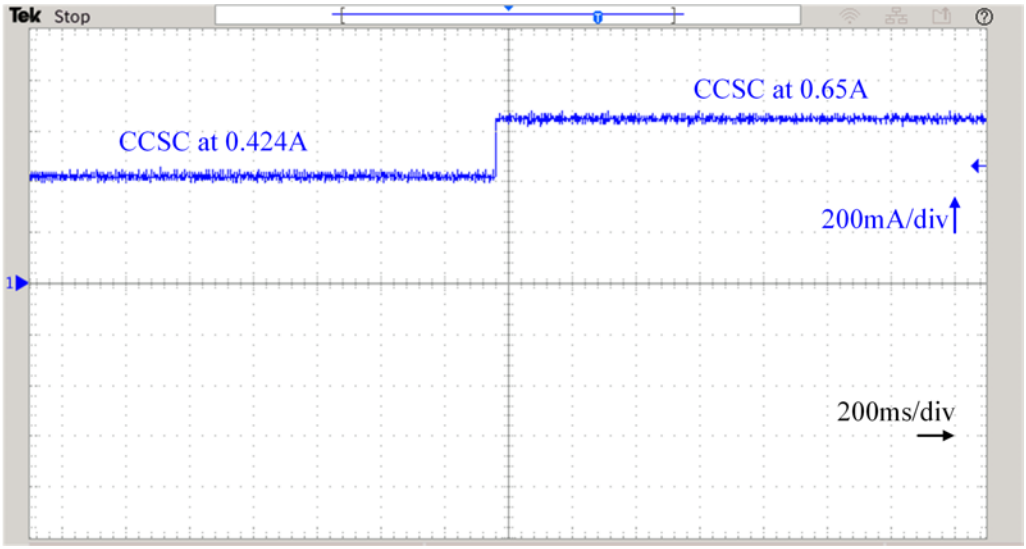


(a)



(b)

Figure 4.7: The characteristic curve of the PVE compared with the real PV panel, MATLAB simulation, and commercial PVE at $I_{sc} = 0.424$A: (a) I-V curve and (b) P-V curve.



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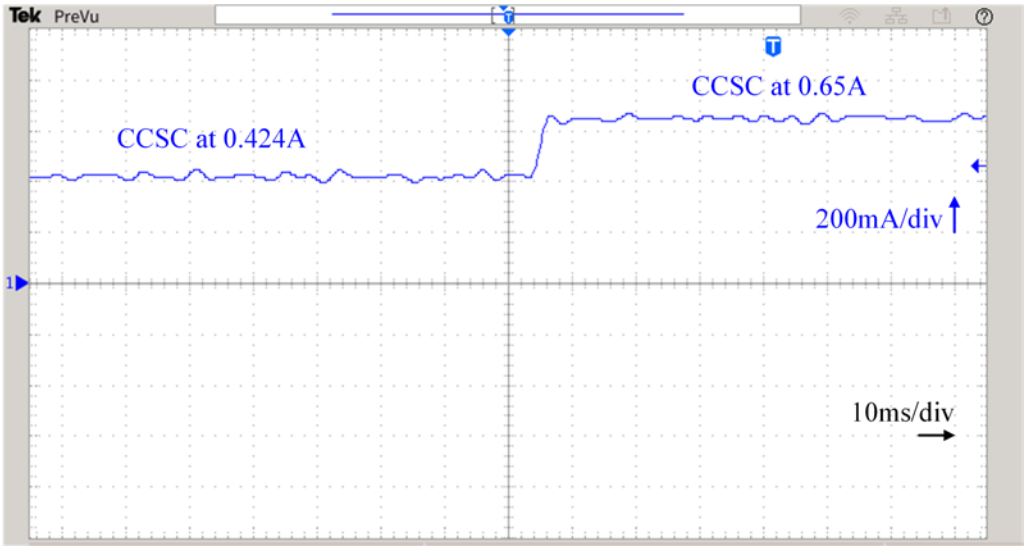
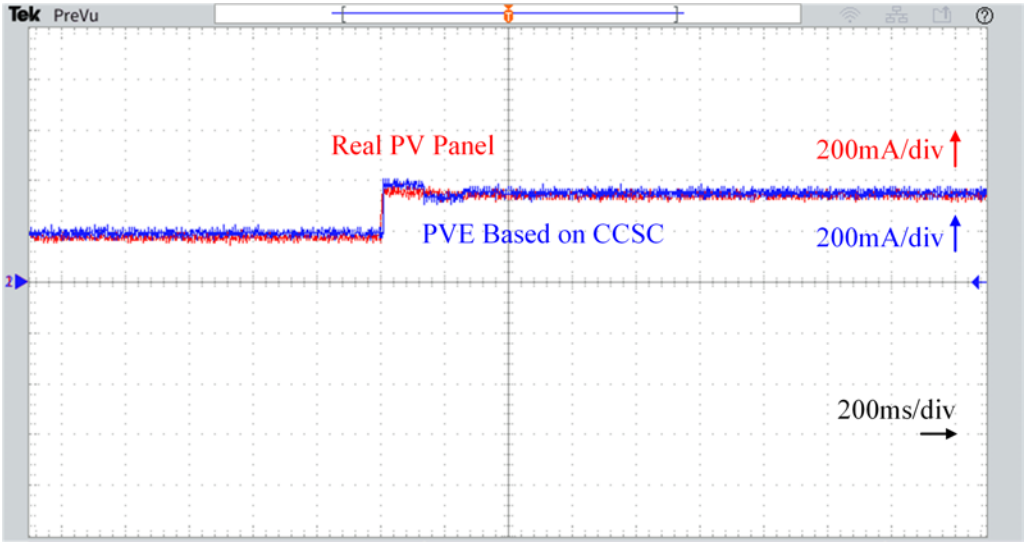


(b)

Figure 4.8: The dynamic response of the CCSC during changes to the irradiation and temperature conditions. Time base (a): 200ms/div. Time base (b): 10ms/div. I_{ph}: 200mA/div.



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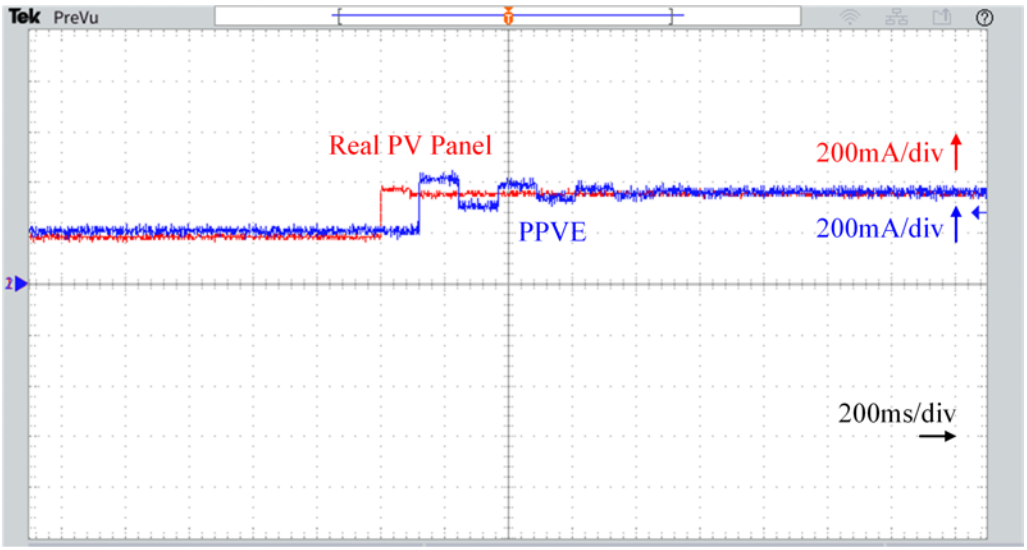


(b)

Figure 4.9: The dynamic PV characteristic when I_{PV} is converted from 0.185A to 0.385A based on load variation: (a) Real PV panel compared with the PVE based on the proposed CCSC, (b) Real PV panel compared with the programmable PVE. Time base: 200ms/div and I_{PV}: 200mA/div.

4.5 Summary

A simple but effective PVE consists of a DC constant current source, a diode string, and two resistors. This chapter presents a cost-effective and straightforward method for designing a constant current source for PVE applications based on a single input single output (SISO) flyback-buck DC/DC converter. The feedback control system

for the flyback-buck DC/DC converter is implemented using a digital signal processing (DSP) controller. Experimental results have demonstrated the usefulness and the effectiveness of the proposed PVE based on the CCSC. The output results show a good match between the proposed PVE and the actual PV panel and the commercial PVE device. The dynamic response of the PVE based on the proposed CCSC is considered. Then, it is compared to the existing PV panel and programmable PV simulator. The proposed PV simulator shows significant improvement compared to the commercial PVE device in terms of dynamic response.

Chapter 5

An Accurate, Fast and Power-efficient PV Emulator Based on Hybrid Passive and Active Circuits

5.1 Overview

Recently, the authors of [40], [44], and [52] proposed a PVE based on a physically equivalent PV cell model. It consists of a DC current source in parallel with a power diode string and a few resistors. It has a fast dynamic response, and its accurate performance is compatible with that of a real PV system. The main problem with making a PVE using a physically equivalent single diode PV cell is the thermal behaviour, as the diode string temperature increases rapidly with an increasing current [40, 44]. In other words, the single diode module has a high power efficiency at the MPP because most of the current flows to the output instead of the diode string. However, the emulator suffers from high power loss beyond the MPP, i.e., the voltage source region, and the power loss is highest in the open-circuit condition, in which the entire current flows to the diode string. Even at high temperatures, the diodes are still functional, but the output voltage (V_{PV}) decreases with respect to time based on the power diode characteristics at high operating temperatures. In addition, running a power semiconductor device at a high temperature shortens its lifetime compared with a low-temperature operating condition [145, 146]. This issue is raised and studied in [40], and solved using a classical solution (variable speed fan), but the overall system efficiency is still low.

This chapter presents two new hybrid solutions, i.e., topologies A and B, that consist of a switching circuit (SC) inserted in parallel with the diode string, as shown in Fig. 5.1, to avoid the high temperature of the diode string when it operates at the voltage source region, minimize the aforementioned power loss while retaining the fast dynamics of the physically equivalent PV cell model, and keep the operating temperature at an acceptable value, at which the output voltage value is kept constant with respect to time at each load value. The first SC consists of a two-switch non-inverting buck-boost (NIBB) DC/DC converter, and the second approach uses an additional bypass switch. The diode string operates in the current source region of the I-V curve with low power loss. In the voltage source region, the converter switches on to replace the diode string to minimize the power loss of the diode string to seamlessly maintain the circuit operation of the emulator. Hardware prototypes

are built and tested to verify the new structures of the enhanced PVE. In addition, a boost DC/DC converter loaded with a perturb and observe (P&O) method is used to test and evaluate the proposed PVEs. The chapter is organized as follows: In Section 5.2, the system overview and description of the proposed PVE are presented. Section 5.3 illustrates the design as an example of the proposed PVE. The experimental results and discussion are presented in Section 5.4, followed by the conclusion in Section 5.5.

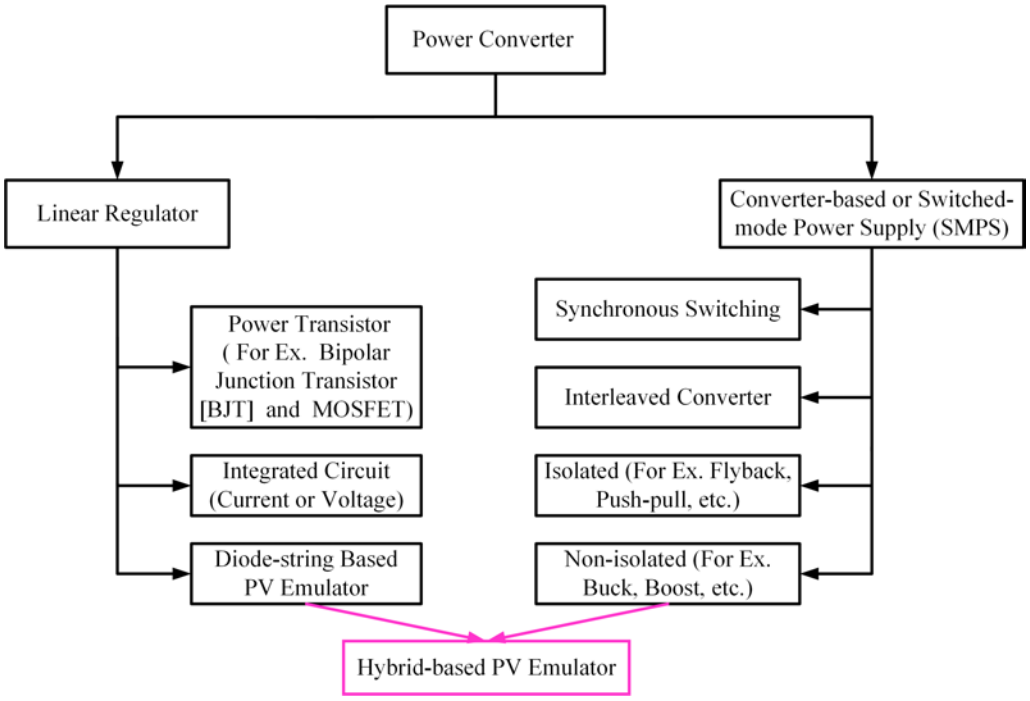


Figure 5.1: The power converter classification for the PVE application including a proposed hybrid-based PVE solution.

5.2 System Overview

5.2.1 Operation Principle of the PVE

The PV panel has two operating regions, as shown in Fig. 3.4. In the first operating region, the output voltage is less than the voltage at MPP. In this region, the PV panel works as a current source, where the relationship between the current and the voltage is almost linear when the voltage increases from the voltage at the short

circuit current (0V) to the voltage around the MPP. The diode string of the PVE will shape this portion of the I-V curve naturally (see the box of red dashes in Figs. 5.2 (a) and (b)). For the voltage source area, which is defined as the operating point from the MPP towards the open-circuit voltage, the proposed switching circuit (see the box of blue dashes in Figs. 5.2 (a) and (b)) operates in place of the diode string to minimize the power loss on the diode while achieving a good PVE performance, as shown in Section 5.4.

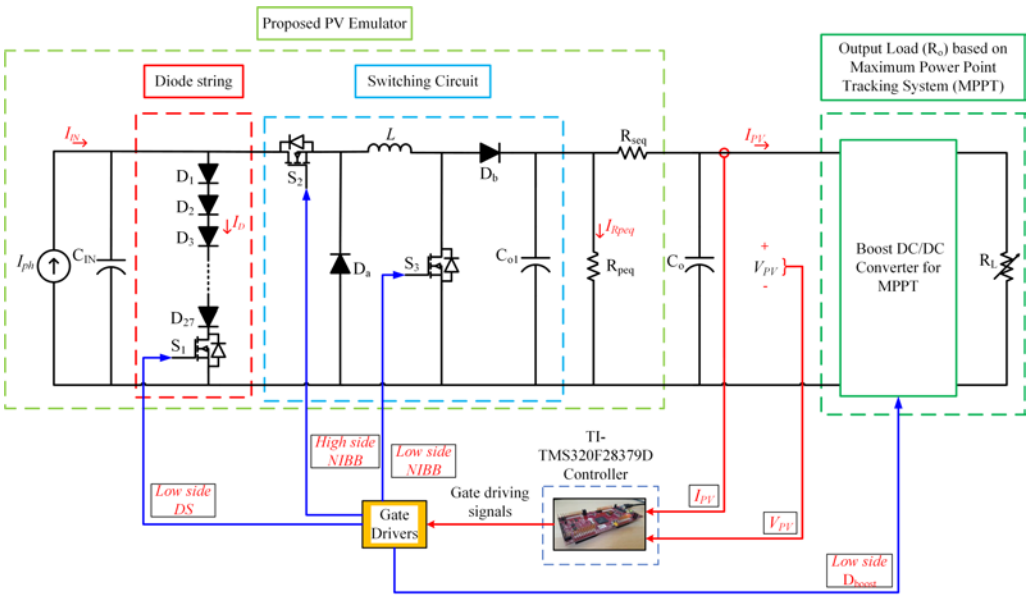
5.2.2 Description of the Proposed PVE

To achieve both simplicity and acceptable accuracy, a PVE based on the physical single-diode PV model is used in this study, as shown in Fig. 5.2 [9, 22, 23, 44]. It consists of a DC input source, operating in constant current source mode, (I_{ph}), a string of diodes inserted in parallel with the NIBB DC/DC converter with a wide output voltage range for shaping the current/voltage curves of the selected PV source in the voltage source region, a TI-TMS320F28379D controller for sensing and controlling the output voltage (V_{PV}) and current (I_{PV}), the computation and dispatch of the duty cycle command, a MOSFET gate driver, and a pair of series and parallel resistors. The output load R_o changes based on the MPPT system using a boost DC/DC converter to test the performance of the PVE, including both steady-state and dynamic behaviours, where a variable electronic load (model: BK8500), R_L, is used.

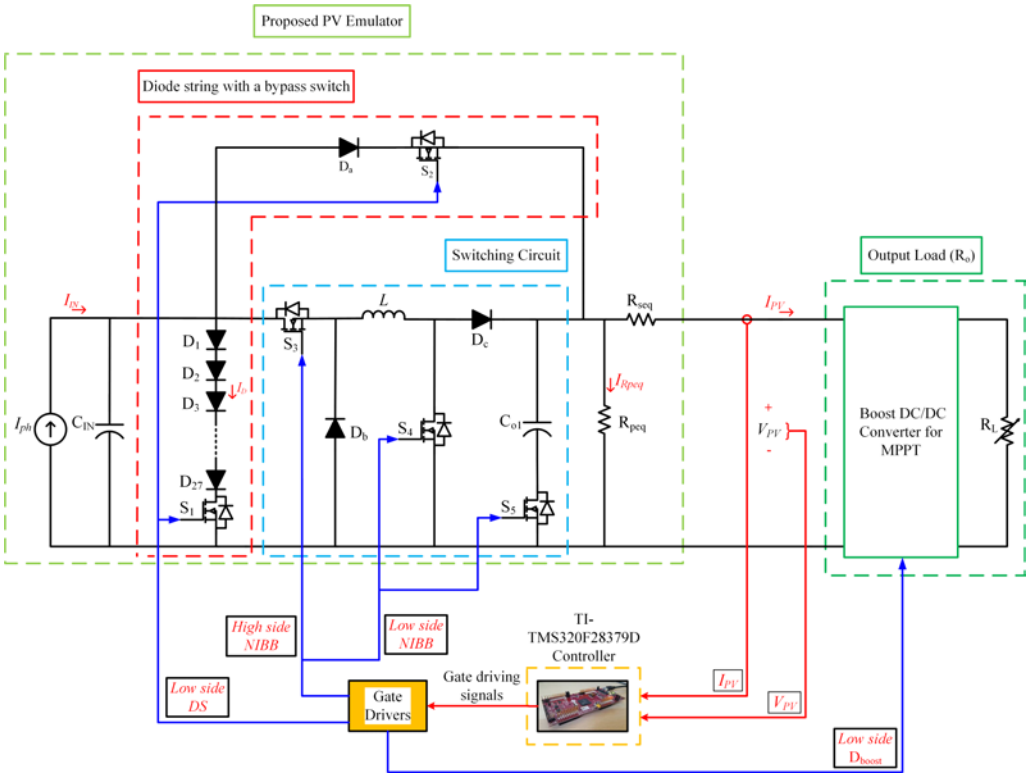
5.3 Example Design of the Proposed PVE

5.3.1 Design of the Diode String

The diode string design is studied in-depth in [44]. Basically, it uses the PV model equations, which consider R_{seq}, R_{peq}, N, and I_{ph}, to design the circuit parameters of the PVE to mimic a selected PV panel (model: Powertech-ZM0954). The design challenge is how to extract real PV parameters and solve the thermal issue of the PVE based on the physical single-diode PV model.



(a)



(b)

Figure 5.2: Block diagram of the proposed hybrid PVE solutions and control scheme with a boost DC/DC converter for the MPPT system: (a) The first topology (A), (b) The second topology (B).

5.3.2 DC/DC Converter Selection and Design

The second part of the PVE is the proposed switching circuit; as shown in Fig. 5.2, this study uses a switching power converter. The selection criteria for the parallel DC/DC converter are simplicity, effectiveness and the ability to sweep through the entire voltage range of the selected PV panel. In order to mimic a low power PV system (<100W), converters such as the buck, boost, buck-boost and non-inverting buck-boost converter can be used [147–150]. The NIBB DC/DC converter is chosen for this work because of its voltage step-up and step-down capability. It can also work with a input voltage less than the OCV of the real PV panel, which reduces the device power stress. Moreover, it simplifies the hardware design due to its common ground feature. The NIBB DC/DC converter consists of two power MOSFETs, two diodes, and an inductor L, as shown in Fig. 5.2. The inductor L is chosen to keep the converter operating in CCM to reduce the conduction losses. A ±10% maximum current ripple in the inductor is selected, at 100kHz switching frequency, and the minimum inductance L_{min} is calculated as shown in (5.1) [74, 150]:

$$L_{min} = \frac{D \times V_{in}}{f_s \times \Delta I} \tag{5.1}$$

where the V_{in} is the maximum input voltage coming from the external DC power supply. It equals the V_{oc} plus the forward voltage of the active components (the diode and switch), where these values are constant, D is the duty cycle of the power switches, f_s is the switching frequency and ΔI is the maximum current ripple.

Table 3.2 shows the key parameters of the chosen PV panel (model: Powertech-ZM9054), where the maximum OCV is 21.5V and the minimum short-circuit voltage is 0V. Two different input DC voltage source ranges are used to feed the proposed PVE circuit in this study. The first is used when the maximum input voltage is less than the OCV (19V), where the NIBB works in buck/boost mode, and the second is used when the maximum input voltage is greater than the OCV (23V), where the NIBB works only in buck mode. The output PVE voltage based on the NIBB converter varies from 17V to 21.5V, where the hysteresis output voltage control is applied to the converter.

The minimum critical inductance is chosen when the input source equals 23V and 0.65A. By setting the maximum duty cycle at 0.5 and using (5.1), L_{min} is 575μH. The inductor value is chosen as 1mH to keep the converter in CCM and reduce the current ripple. The MOSFET used in this work is the IRF540N, in which the selection criteria are based on the voltage and current stress of the switch(s) and loss due to on-resistance (R_{on}). In order to provide at least 15V for both the floating and non-floating gate drives for the MOSFETs, both low- and high-side drivers are used. In this work, the TC4428 gate driver is used as a low-side driver, and the IR2184PBF is used as a high-side driver. The selection criteria of the low and high-side drivers are based on the gate drive supply range from (10V to 20V) and the high-speed operation (turn-on and turn-off time). The components used in this design are shown in Table 5.1 and are based on the datasheet of the selected PV panel (as seen in Table 3.2) and the NIBB component power stress.

Table 5.1: Components details of the proposed PVE

Component	Model/Value
Digital Controller	TMS320F28379D
Switching Frequency	100kHz
MOSFET	IRF540N
Low-side Driver	TC4428
High-side Driver	IR2184PBF
D_a, D_b & D_c	MBR20200CT
D_1,.....D_{27} (Diode String)	1N5400
Current Sensor	LEM-LTS-6-NP
Boost Converter Inductor	1mH
L (NIBB Converter)	1mH
C_{IN}, C_{o1} & C_o	470uF
Programmable PVE Device	EA-PSI 9360-15
Programmable DC Electronic Load	BK8500

5.3.3 Operation Principle of the Proposed PVE

The proposed topologies A and B have two operating modes, as shown in Figs. 5.3 and 5.4. The first mode, where the V_{PV} is less than the MPP voltage (i.e., the current source region). In this mode, the switches in Mode-I are active (as seen in Table 5.2), where the current will flow through the diode string and the output current will be complementary to the diode string current, and the NIBB converter is bypassed. In the second mode, the NIBB DC/DC converter starts to operate once the voltage reaches the MPP voltage and operates up to the OCV (i.e., the voltage source region). In this mode, the switches in Mode-II are active (as seen in Table 5.2) to charge the inductor (Figs. 5.3 (b) & 5.4 (b)). Then, both switches are OFF to discharge the inductor through the diodes (Figs. 5.3 (c) & 5.4 (c)). In addition to the two switches in Mode-II, i.e., topology B, the switch S_5 is used to control the output capacitor when it is not used in Mode-I, as it causes a slow dynamic response. In Mode-II, S_5 turns ON because it is required as part of the NIBB converter operation. The diode string is not engaged in this mode to reduce power loss. In fact, the NIBB converter is used to limit and control the current rate on the diode string to enhance its thermal behaviour. The diode string in this circuit will help achieve a fast dynamic response based on the similar electrothermal characteristics between a power diode and a real PV panel. The use of an NIBB converter is not essential in the first operation mode because the current is almost linear when the voltage increases from the voltage at the short circuit current (0V) to the voltage around the maximum power point (MPP). Afterwards, the current starts to change exponentially.

Table 5.2: Switching look-up table for various operating modes of the proposed PVE based on the hardware platforms A and B

Topology	Operating Mode	State	Active Elements	Switch State		Duty Condition	Fig.
				ON	OFF		
A	1	I	C_{IN}, C_o, DS, S_1, S_2, L & D_b	S_1^o & S_2^o	S_3	—	Fig. 5.3 (a)
	2	I	C_{IN}, C_o, S_2, L & S_3	S_2^* & S_3^*	S_1	Buck- or Boost-based on Maximum	Fig. 5.3 (b)
		II	C_{IN}, C_o, D_a, L & D_b	—	S_1, S_2 & S_3	V_{in} Compared with V_{oc}	Fig. 5.3 (c)
B	1	I	C_{IN}, DS, S_1, D_a & S_2	S_1^o & S_2^o	S_3, S_4 & S_5	—	Fig. 5.4 (a)
	2	I	C_{IN}, C_o, S_3, L, S_4 & S_5	S_3^*, S_4^* & S_5^o	S_1 & S_2	Buck- or Boost-based on Maximum	Fig. 5.4 (b)
		II	C_{IN}, C_o, D_b, L, D_c & S_5	S_5^o	S_1, S_2, S_3 & S_4	V_{in} Compared with V_{oc}	Fig. 5.4 (c)

* Switch works in PWM, ^{o} Switch is fully ON and diode string is active (DS)

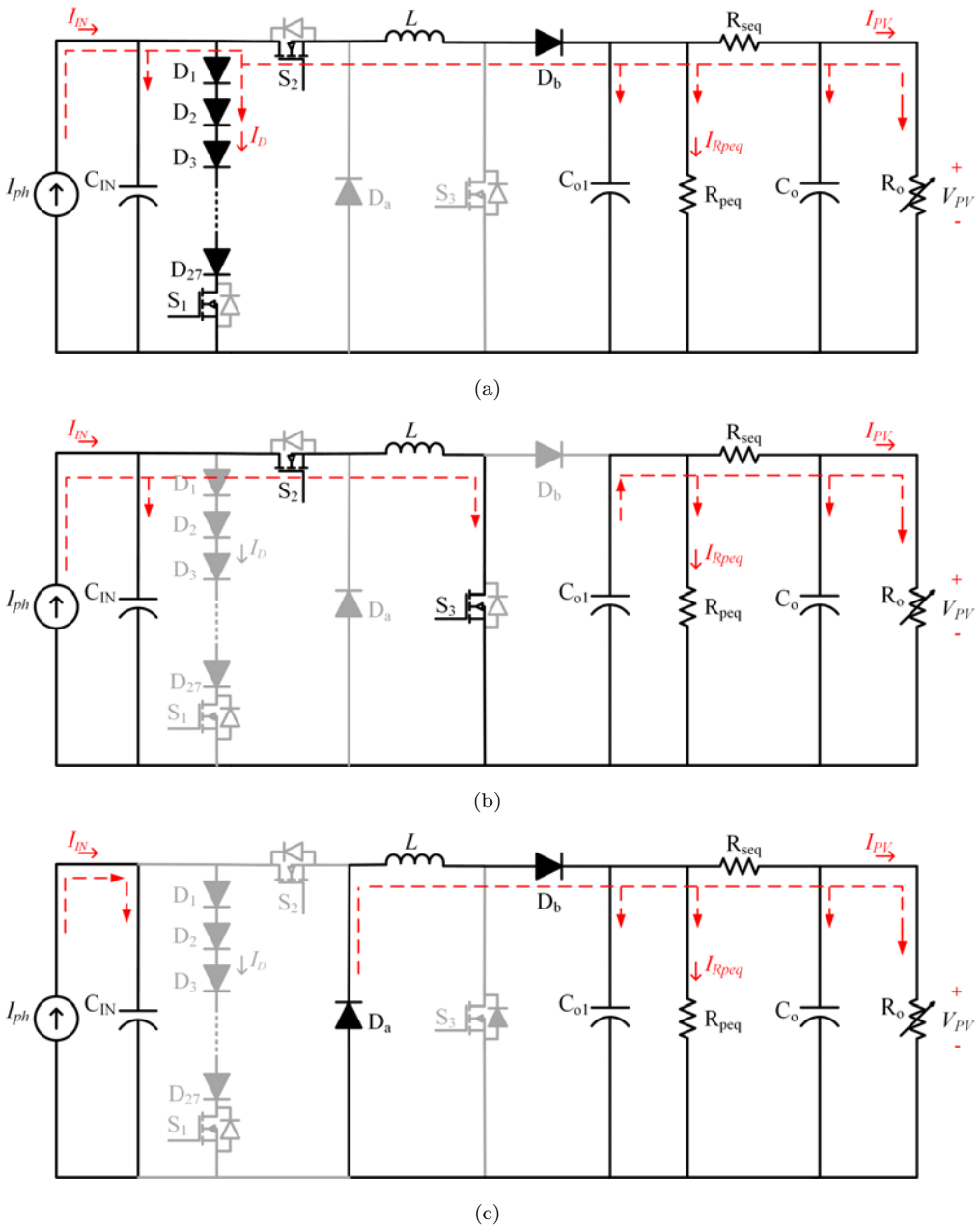


Figure 5.3: Operation principle of the proposed PVE topology A: (a) Mode-I when S_1 and S_2 are ON and (b) and (c) Mode-II when the NIBB works.

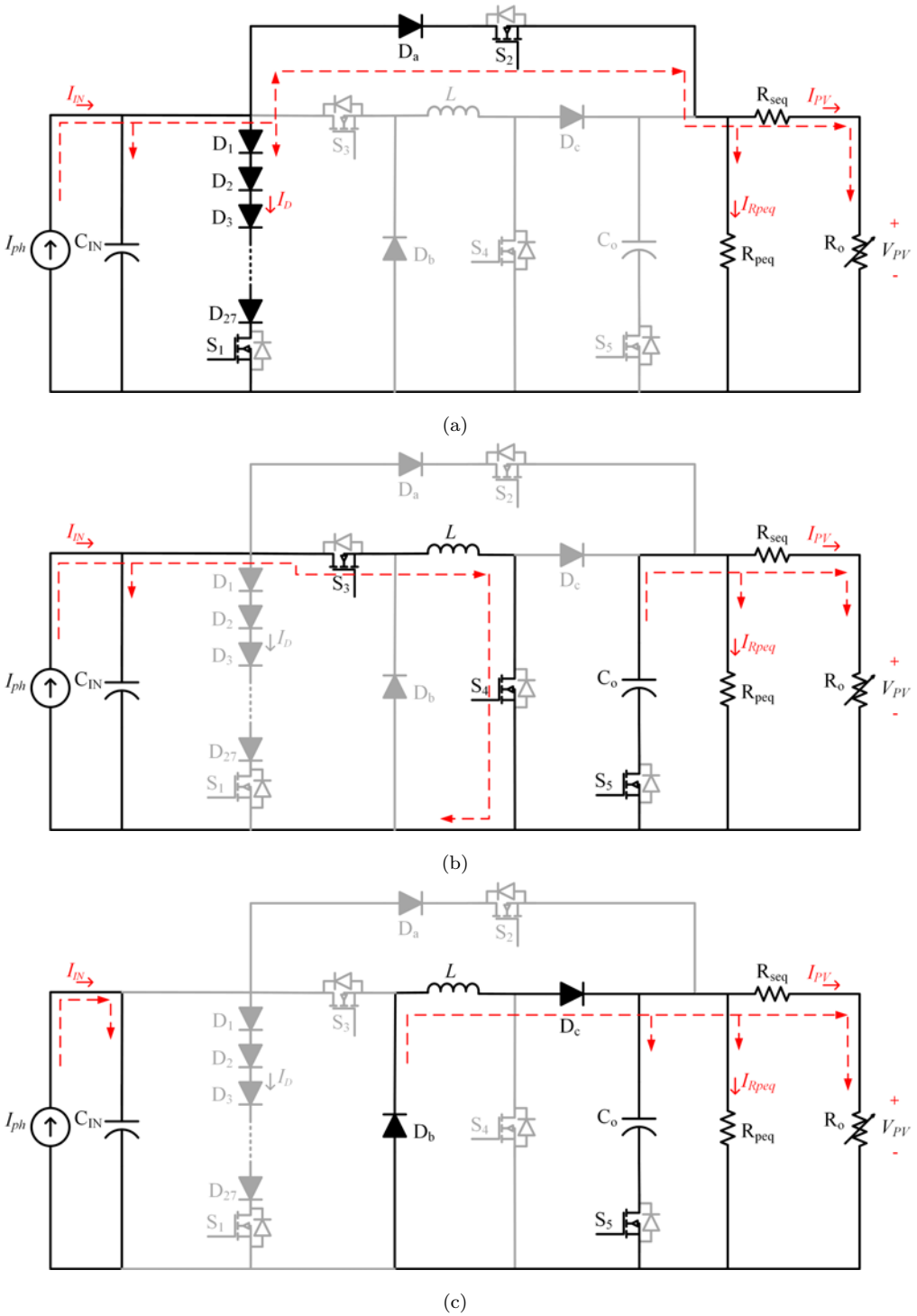


Figure 5.4: Operation principle of the proposed PVE topology B: (a) Mode-I when S_1 and S_2 are ON and (b) and (c) Mode-II when the NIBB works.

5.3.4 Controller and Control Strategy for Both Topologies A and B

The microcontroller used in this work is the LAUNCHXL-F28379D from TI [151, 152]. The closed-loop control system and MPPT algorithm are implemented based on the control block diagram, as shown in Fig. 5.5, and the mode selection algorithm is designed based on the control flow chart shown in Fig. 5.6.

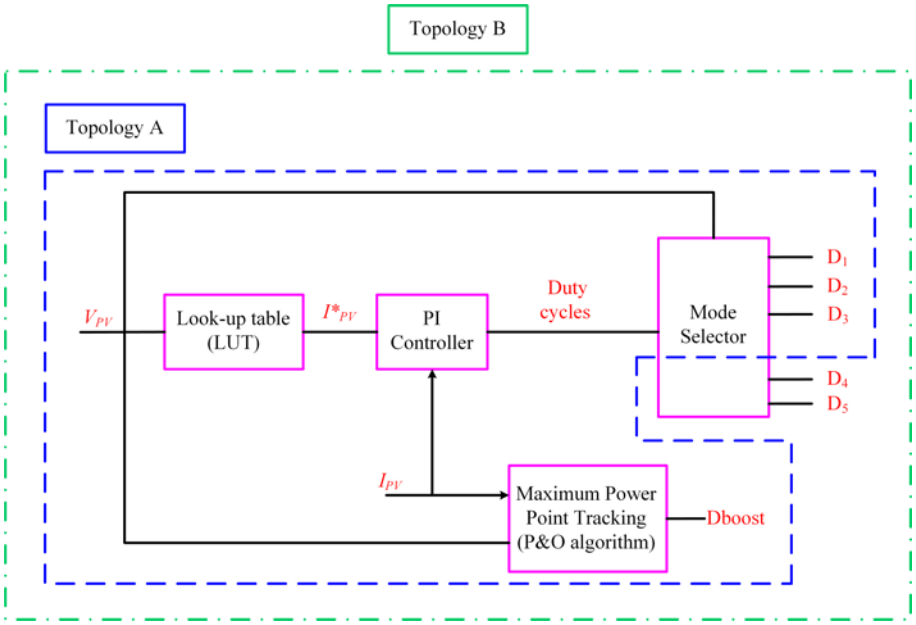


Figure 5.5: Block diagram of the closed-loop control for both topologies A and B.

The program starts by specifying the symbols for the duty cycles. Since the initial current sensor output value may not be precisely zero due to the residual magnetization in the current sensor used (model: LEM-LTS-6-NP), an initial zero calibration has to be performed by measuring the I_{PV} value and setting it as a reference to cancel this offset. Suppose V_{PV} is less than 16.5V. In that case, the PVE works in the linear operating region (the relationship between the current and voltage is almost linear before the MPP) or diode string mode, where the switches in Mode-I are active for both topologies A and B as seen in Table 5.2. Next, the output voltage (V_{PV}) is measured. If the V_{PV} is still less than 16.5V, the emulator remains in the same mode (i.e., Mode-I). On the other hand, if the V_{PV} is larger than 16.5V and smaller than 17.5V, the controller will wait for 1ms and recheck the V_{PV} status to

decide if the mode should be changed. The voltage range from 16.5V to 17.5V, a 1V window, is used as the hysteresis band control. Lastly, if V_{PV} is larger than 17.5V and less than 21.5V (the OCV for the selected PV panel), the PVE has now entered the voltage source region or NIBB DC/DC converter mode, where the NIBB begins to operate, i.e., Mode-II. The active components in this mode can be found in the switching look-up table as shown in Table 5.2. The control strategy used in Mode-II is based on the look-up table (LUT) [153,154]. These two methods are popular control methods used to obtain the I-V curves of real PV panels using power electronics converters [74, 155]. A boost DC/DC converter with a P&O algorithm is used to test the proposed PVE at different irradiation levels. Table 5.2 shows the switching look-up table for both topologies A and B in different operating modes and presents the active components in each mode.

5.4 Experimental Results and Discussion

A hardware prototype is built and tested in the laboratory, as shown in Fig. 5.7. The maximum OCV (V_{oc}) is 21.5V, and the short-circuit current (I_{sc}) is 0.65A. The performance of the proposed close-loop PVE is compared with both the real PV panel and a commercial programmable PVE (PPVE, model: EA-PSI 9360-15 2U). The experimental results show similar electrical characteristics among the proposed emulator, the selected PV panel and the commercial PVE.

Fig. 5.8 shows the measured steady-state results for the proposed PVE, i.e., topology A, in Mode-I where only the diode string is active. The top waveform shows the gate control signal for S_1, followed by the control signal for S_2, then the control signal for S_3 and the output voltage, when the output load equals 4.7Ω, and 22Ω, respectively. It is clear from the figure that S_1 and S_2 are ON, and S_3 is OFF.

As mentioned above, there are two control scenarios depending on the input voltage of the DC source value. The first one occurs when a 23V DC input source is used, in which the NIBB converter works as a buck converter in Mode-II, as shown in Fig. 5.9. Based on the figure, it is notable that the duty cycle value of S_2, and S_3 is less than 0.5 at the OCV. In the second control scenario, a 19V DC input source is used

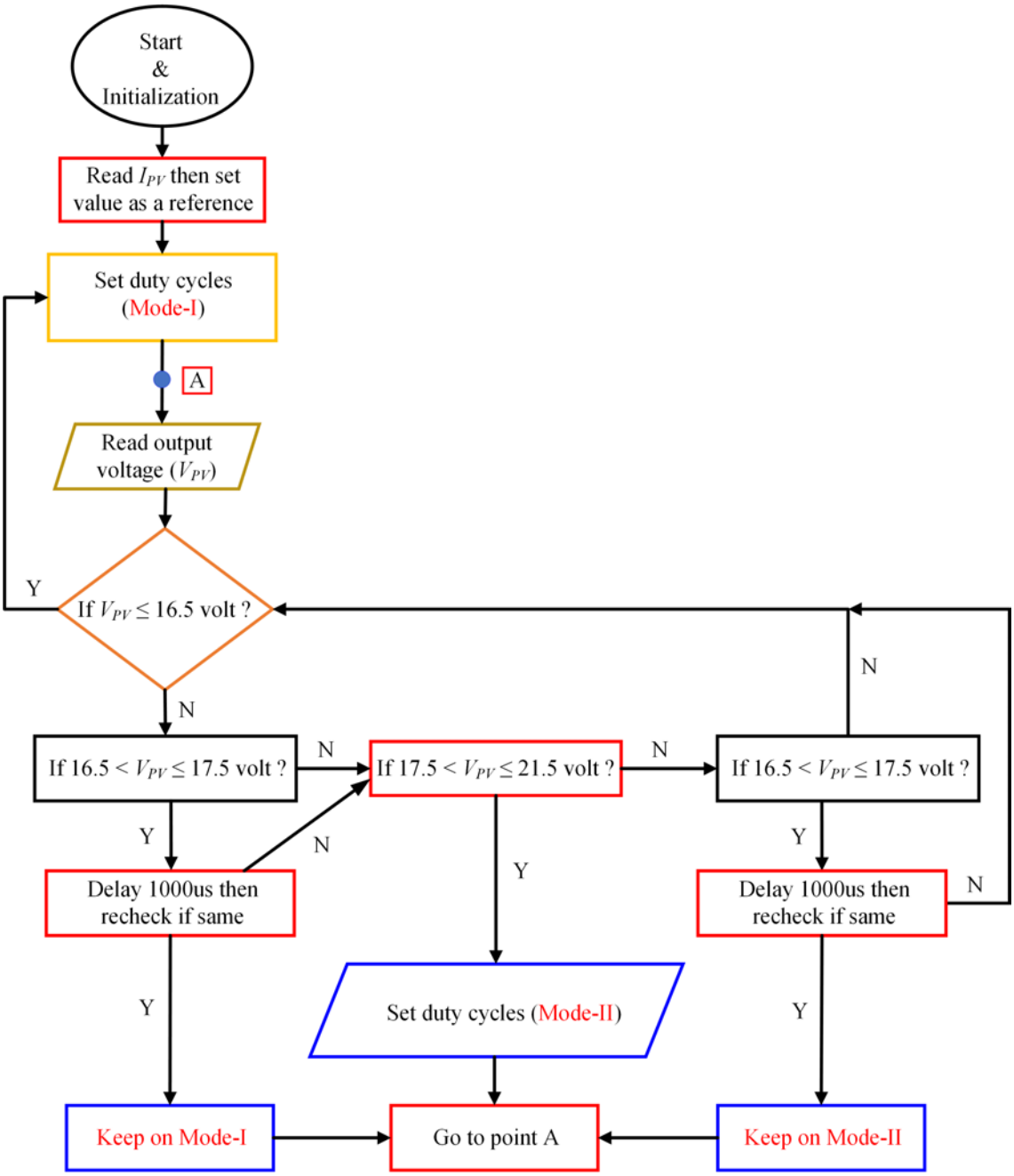


Figure 5.6: Flowchart of the operating mode selection algorithm for both topologies A and B.

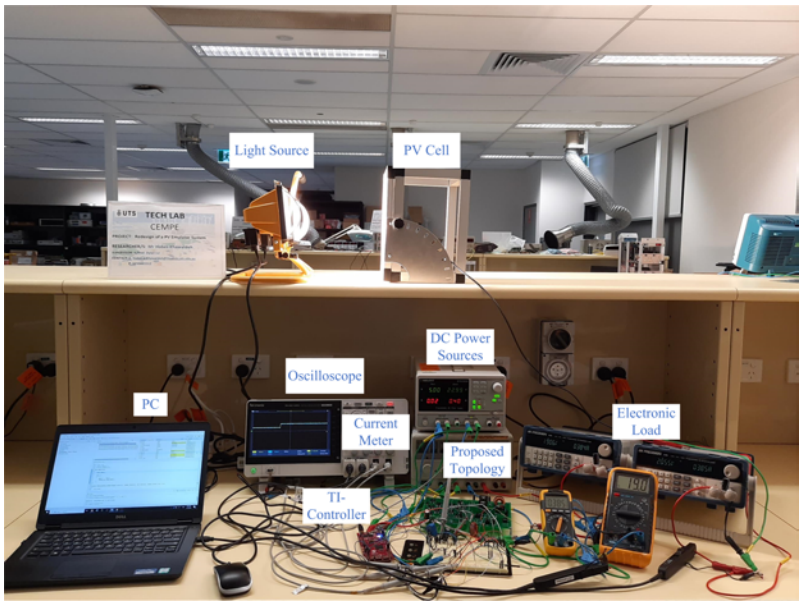
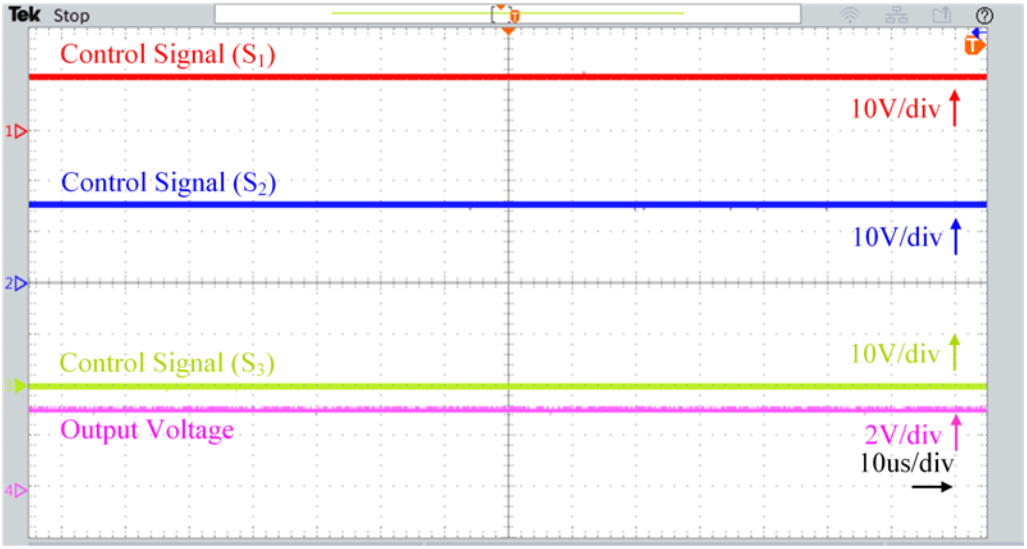


Figure 5.7: Experimental setup for the proposed PVE.

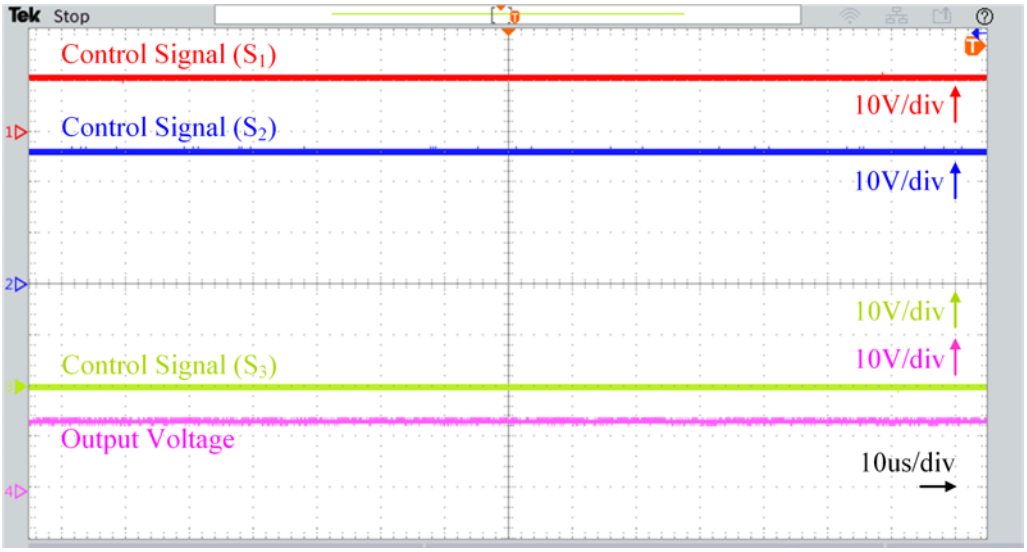
as a DC supply, and the NIBB converter works as a boost converter in Mode-II, as shown in Fig. 5.9. Notably, the duty cycle values of S_2 and S_3 are greater than 0.5. The efficiency and dynamic response are studied based on the boost mode control scenario.

The experimental steady-state results for the proposed PVE, i.e., topology A, in Mode-II is based on the first and second control scenarios, where only the NIBB DC/DC converter is active, are shown in Figs. 5.9 and 5.10, respectively. The top waveform represents the PWM control signal for S_1, followed by the control signal for S_2, then the control signal for S_3 and the output voltage of the proposed PVE when the output load equals 47Ω, and 270Ω, respectively. It is clear that the NIBB converter is operating where S_2 and S_3 are switching, and S_1 is OFF.

Fig. 5.11 (a) shows the measured steady-state results for the proposed PVE, i.e., topology B, in Mode-I, where only the diode string is active. The top waveform represents the gate control signal for S_1, followed by the control signal for S_2, then the control signal for S_3, S_4, and S_5, and the output voltage when the output load equals 22Ω. It is clear from the figure that the diode string is working when S_1

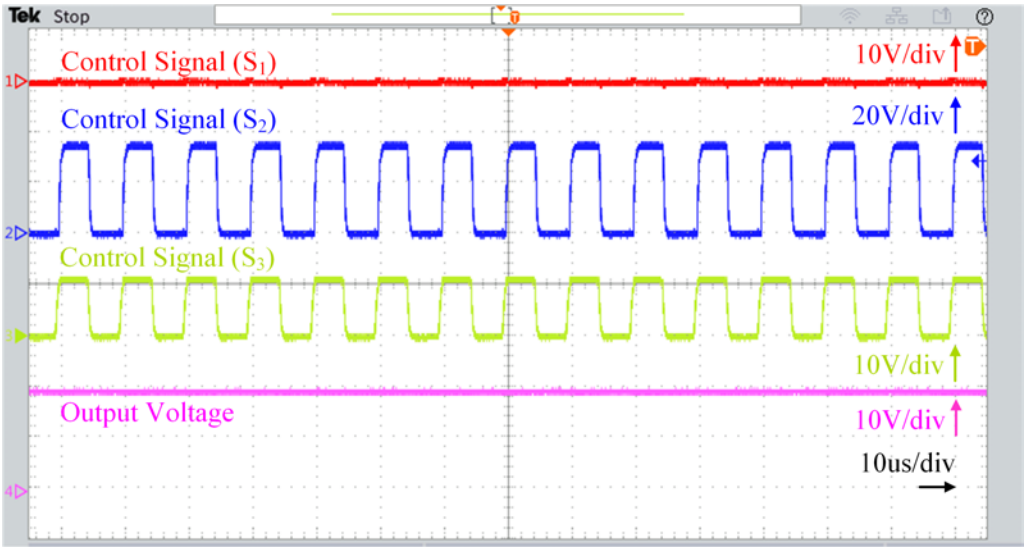


(a)

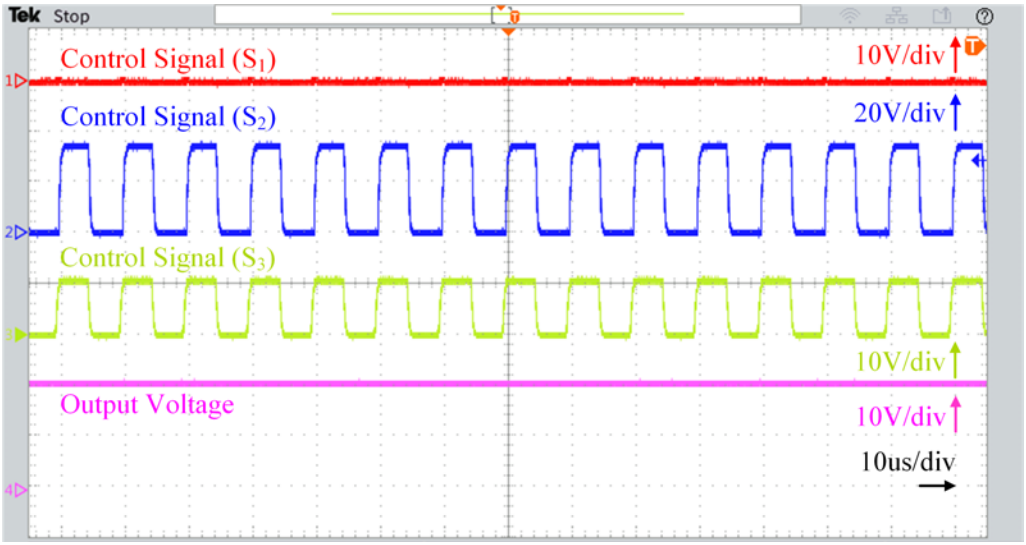


(b)

Figure 5.8: The gate control signals and output voltage of the proposed PVE: (a) at 4.7Ω and (b) at 22Ω resistive load. Time base: 10us/div. Ch1 (red): 10V/div. Ch2 (blue): 10V/div. Ch3 (green): 10V/div. Ch4 (a-pink): 2V/div. Ch4 (b-pink): 10V/div. Diode string mode (first control scenario).

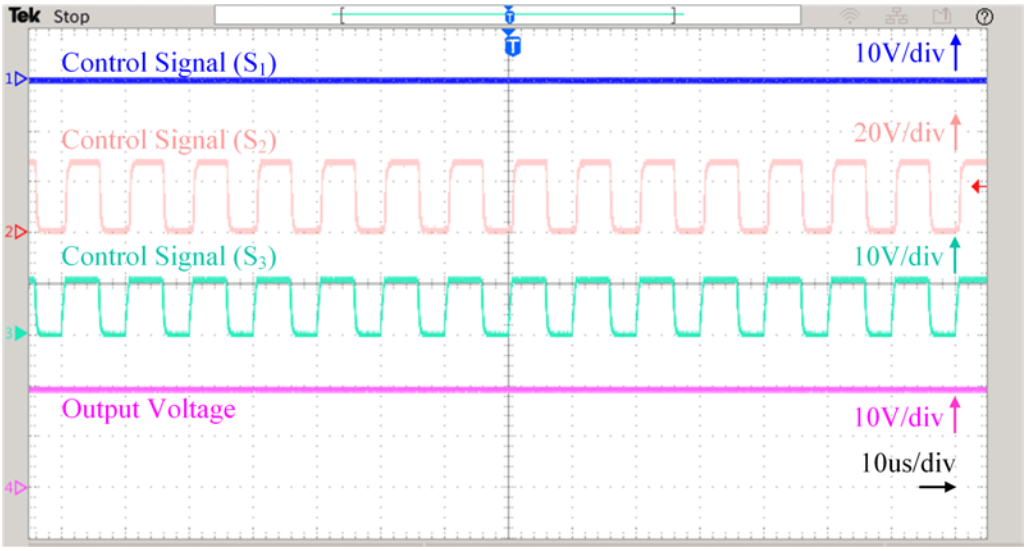


(a)

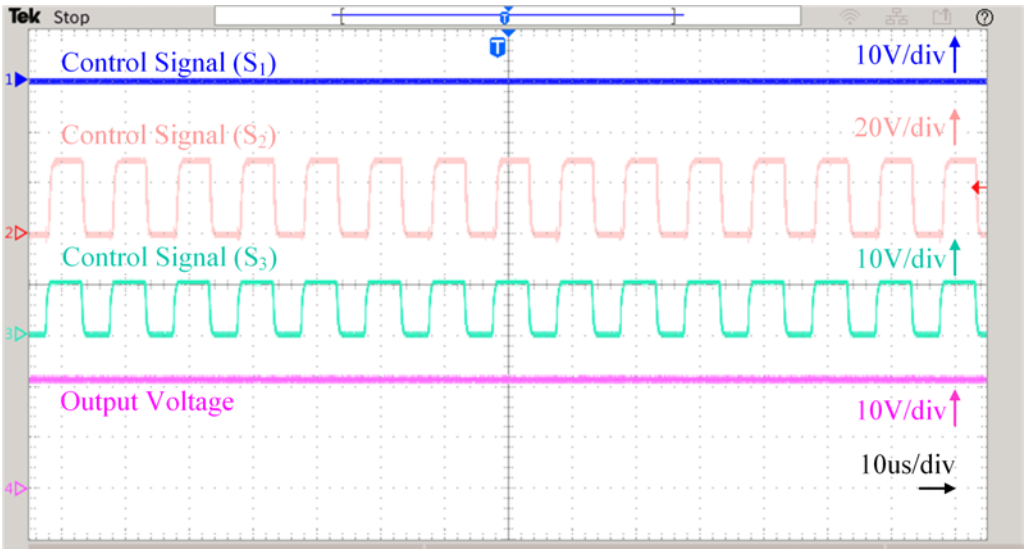


(b)

Figure 5.9: The PWM control signals and output voltage of the proposed PVE: (a) at 47Ω and (b) at 270Ω resistive load. Time base: 10us/div. Ch1 (red): 10V/div. Ch2 (blue): 20V/div. Ch3 (green): 10V/div. Ch4 (pink): 10V/div. NIBB converter (buck mode).



(a)



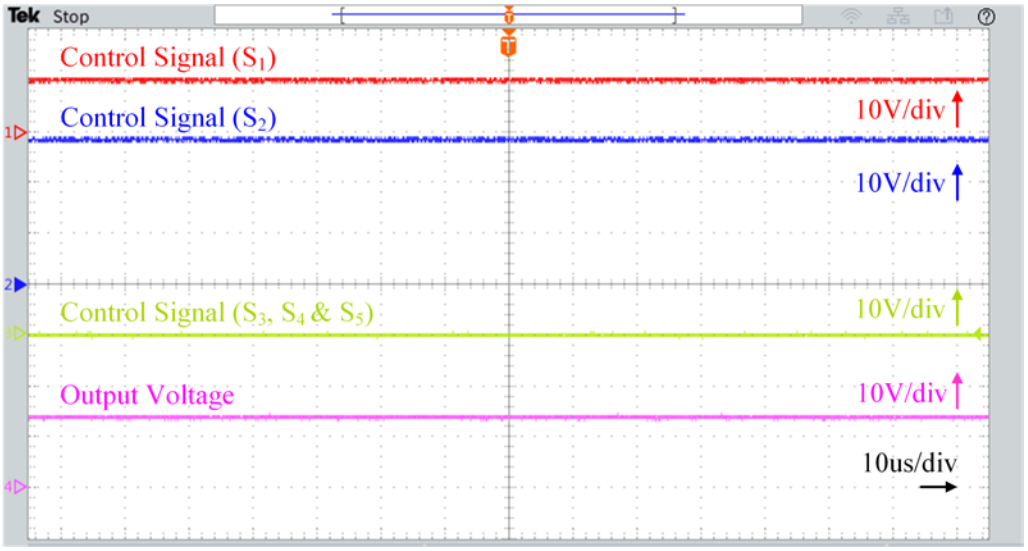
(b)

Figure 5.10: The PWM control signals and output voltage of the proposed PVE: (a) at 47Ω and (b) at 270Ω resistive load. Time base: 10us/div. Ch1 (blue): 10V/div. Ch2 (red): 20V/div. Ch3 (green): 10V/div. Ch4 (pink): 10V/div. NIBB converter (boost mode).

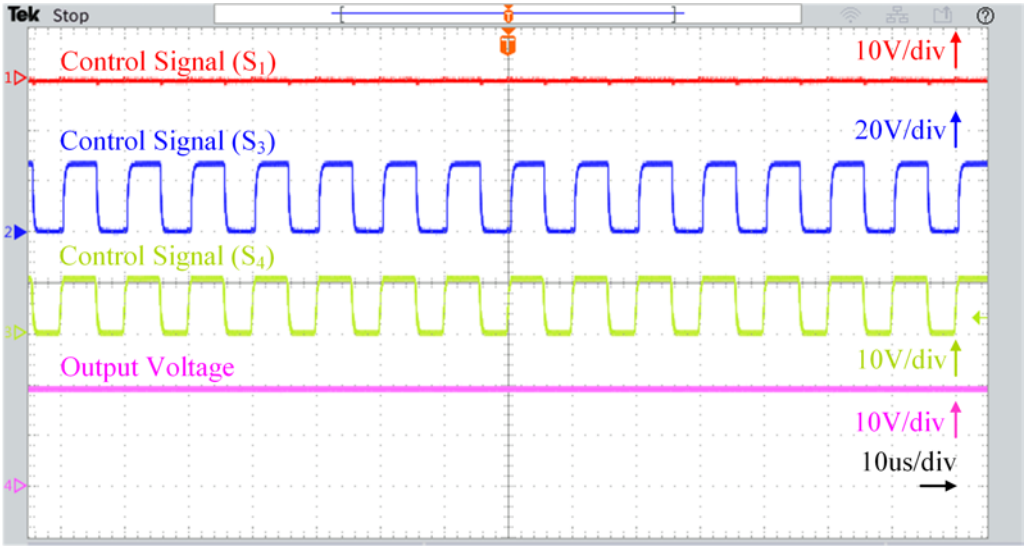
and S_2 are ON and S_3, S_4, and S_5 are OFF. Based on the DC supply voltage value (19V), the NIBB converter works as a boost converter in Mode-II, as shown in Fig. 5.11 (b). In Fig. 5.11 (b), it is notable that the duty cycle values of S_3 and S_4 are greater than 0.5 at 47Ω. The top waveform represents the gate control signal for S_1, followed by the control signal for S_3, then the control signal for S_4 and the output voltage of the proposed PVE when the output load is 47Ω. It is clear that the NIBB converter is operating where S_3 and S_4 are switching, and S_1 and S_2 are OFF.

Fig. 5.12 shows the dynamic behaviour of the proposed PVE when the operating mode changes between Mode-I and Mode-II based on the output load variation. V_{PV} equals 13.5V and 18.7V when the load is 22Ω and 47Ω, respectively. As the figure reveals, in Mode-I, in which the only diode string is working, it is clear that the diode string operates when S_1 and S_2 are ON, and S_3 is OFF. In Mode-II, in which the NIBB DC/DC converter is active, the NIBB converter operates where S_2 and S_3 are switching based on the shared PWM, and S_1 is OFF. Notably, the proposed emulator can switch between the modes smoothly, where the output power equals 8.28W (at 13.5V & 0.614A) in Mode-I and 7.44W (at 18.7V & 0.398A) in Mode-II in this example.

Figs. 5.13 and 5.14 show a comparison between the I-V and P-V characteristic curves based on the experimental and simulation results for the commercial programmable PVE device (PPVE, model: EA-PSI 9360-15 2U), proposed PVE, PVE MATLAB simulation, and the actual PV panel (model: Powertech-ZM0954). Fig. 5.13 (a) shows the I-V curve and Fig. 5.13 (b) shows the P-V curve for the same setup. According to Fig. 5.13, it is clear that the actual PV panel short circuit current (I_{sc}) is equal to 0.65A and the OCV equals 21.5V at $990W/m^2$ and 26°C. To simulate the same electrical characteristics, the DC power source operates at the constant current mode and is limited to 0.65A based on (2.9) and the voltage is set to 23V or 19V based on the control scenario. The real PV panel current and voltage are measured again at another irradiation level ($795W/m^2$ at 26.5°C), where the short circuit current drops to 0.52A and the OCV decreases to 21.3V. The current and voltage values are used as inputs for the PVE, where the DC power source is



(a)



(b)

Figure 5.11: The gate control signals and output voltage of the proposed PVE: (a) at 22Ω and (b) at 47Ω resistive load. Time base: 10us/div. Ch1 (red): 10V/div. Ch2 (a-blue): 10V/div. Ch2 (b-blue): 20V/div. Ch3 (green): 10V/div. Ch4 (pink): 10V/div.

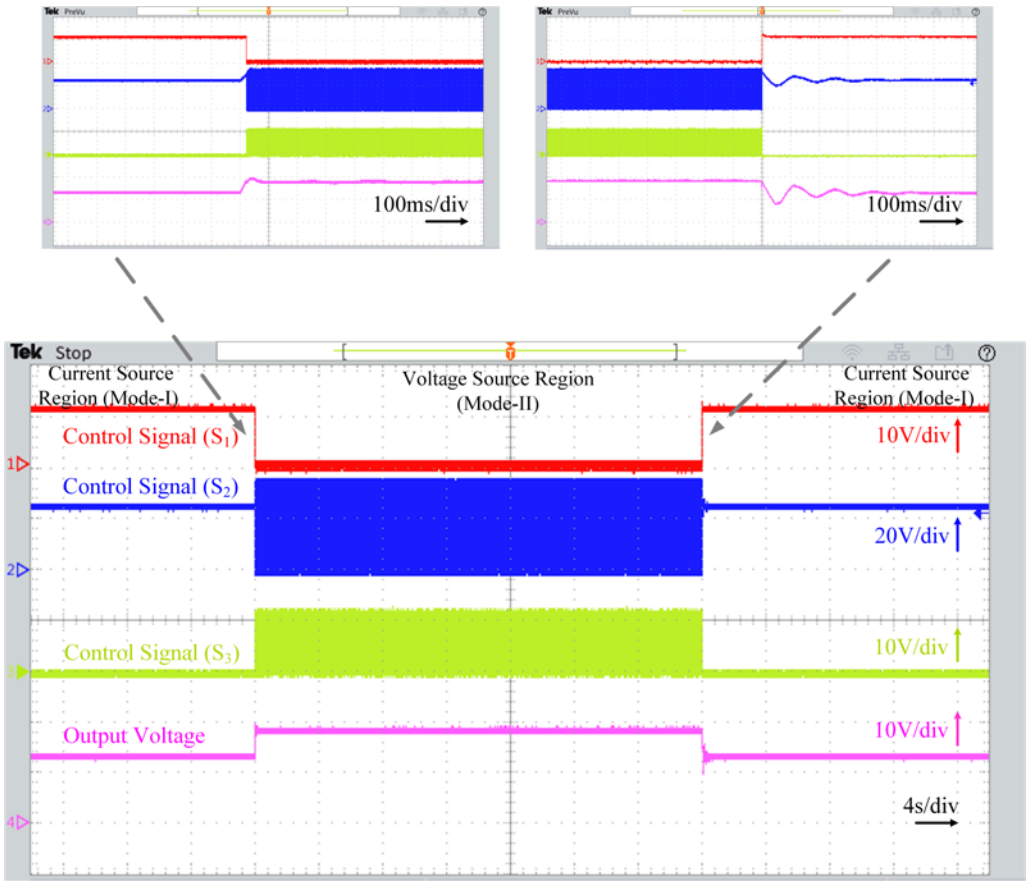


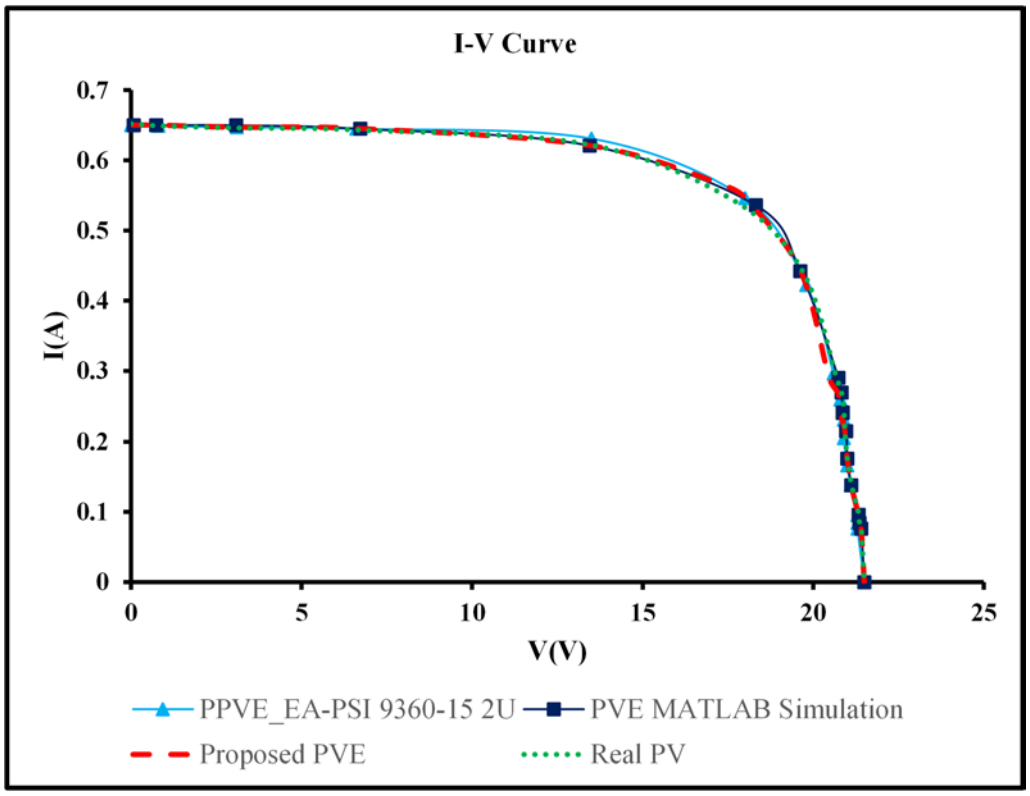
Figure 5.12: The PWM control signals for S_1, S_2 and S_3, respectively and the output voltage of the proposed PVE when the operation is mode changed. Time base: 4s/div. Ch1 (red): 10V/div. Ch2 (blue): 20V/div. Ch3 (green): 10V/div. Ch4 (pink): 10V/div.

limited to 0.52A based on (2.9) and the voltage set to 23V or 19V based on the control scenario. The I-V and P-V curves for the commercial PPVE, PVE MATLAB simulation, proposed PVE, and actual PV panel are plotted in Fig. 5.14. The enhanced PVE shows a high performance, and the current and voltage match that generated by the commercial PPVE and the actual PV panel.

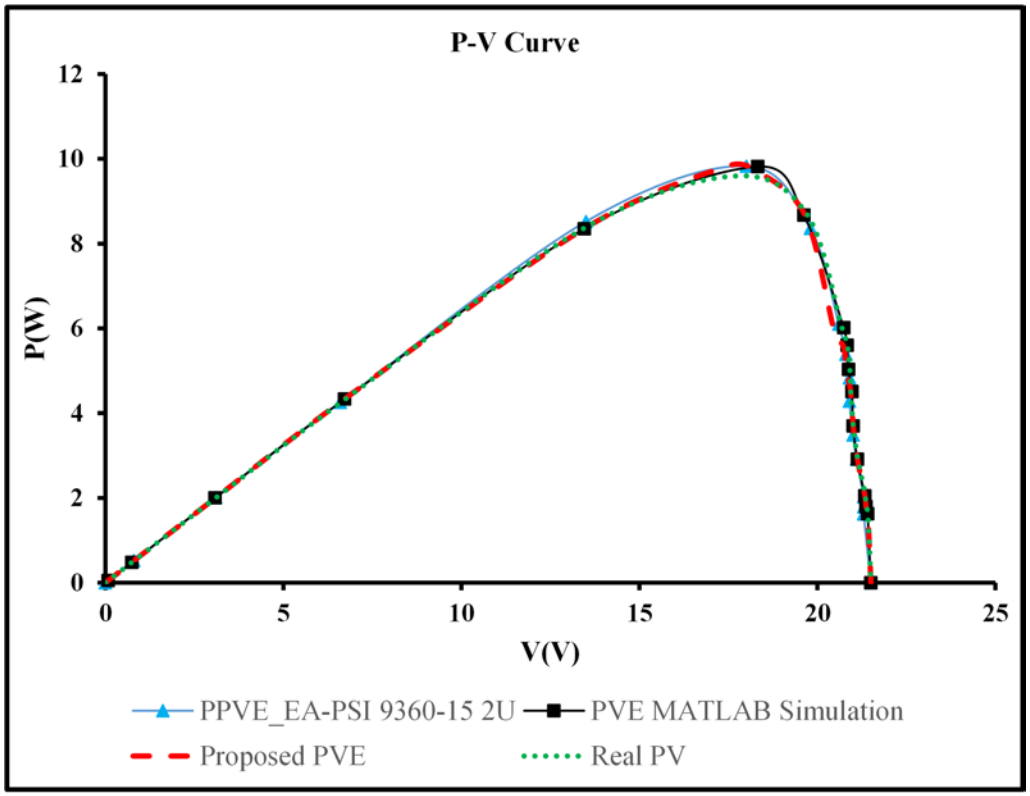
Using the proposed topology enhanced the accuracy of the PVE, which was confirmed by applying the concept of the absolute deviation value (error) between the I-V curve of the real PV panel and the proposed PVE. The results using (3.17) are shown in Fig. 5.15. The figure shows that the variation for a large part of the I-V curve is less than 0.25%, and worst-case scenario is equal to 0.4% and 0.5% for the I_{sc} equal 0.52A and 0.65A, respectively. It is thus confirmed that the proposed structure enhances the overall system efficiency and accuracy compared with the diode string-based solution.

The MPPT test has been conducted to validate and evaluate the proposed PVE at different irradiation levels. Figs. 5.16 (a) and (b) depicts a drawing of the I-V curve, the duty cycle of the boost DC/DC converter (D_{boost}) is changed from 10% to 90%. The experimental setup is shown in Fig. 5.7. The MPP at different irradiation levels is shown in Figs. 13 (d) and (e), by using the MPPT method (P&O), respectively. Figs. 5.16 (c) and (f) show the I-V and P-V curves for the actual PV system and the proposed PVE under two different irradiation levels, and the performance of the proposed emulator behaves identically to the real PV system. It is notable from Fig. 5.16 (f) that the PVE will have two MPPs (points A and B). The voltage and current at the first MPP (point A) equal 17.4V and 0.562A, respectively, whereas the voltage and current at the second MPP (point B) equal 17.3V and 0.485A, respectively. In addition, it is clear from the figure that the performance of the proposed PVE is not affected by the MPPT system used. In summary, the tracking system is able to track the MPPs at the same irradiation levels, and the tracked current and voltage match with the one in Fig. 5.16 (f).

Fig. 5.17 shows a comparison between the PVE built by using diode string and the proposed PVE, i.e., topologies A and B, in terms of temperature and efficiency. A

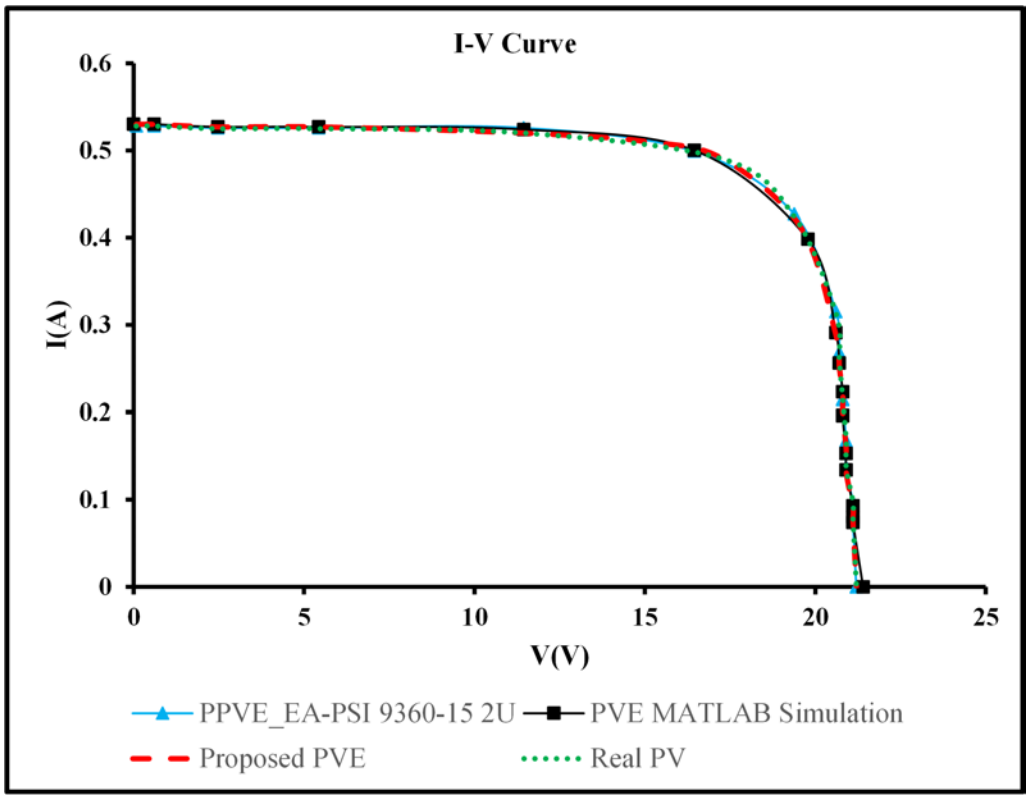


(a)

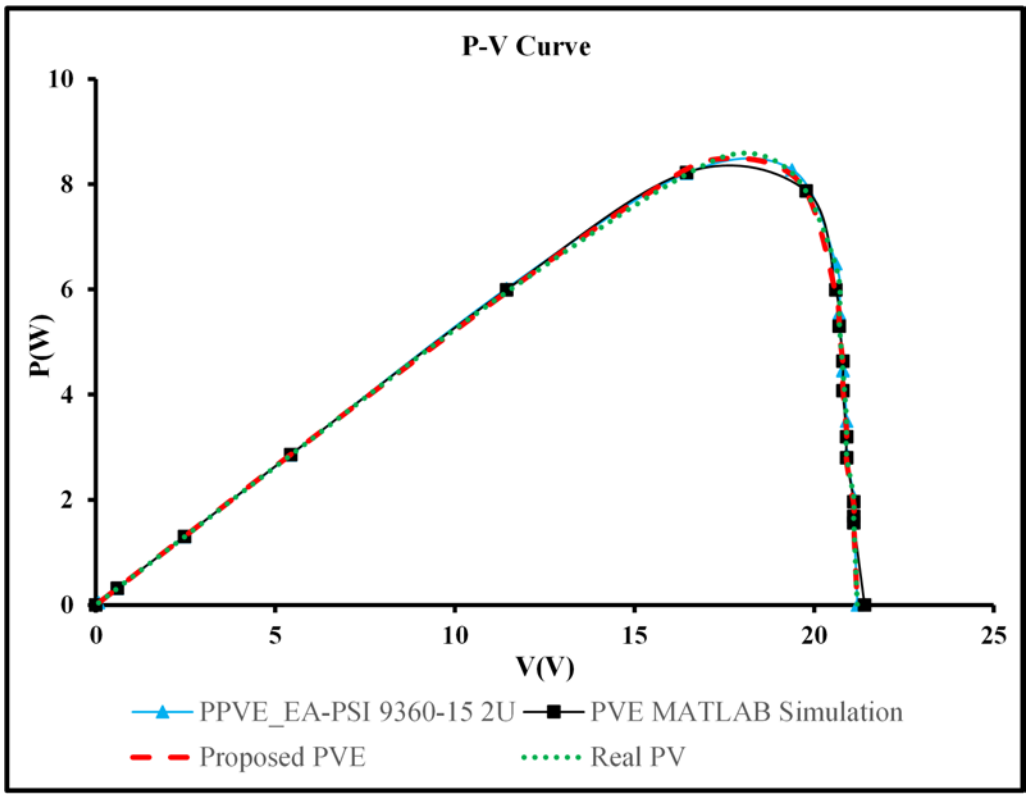


(b)

Figure 5.13: The comparison of characteristic curves of the real photovoltaic panel, proposed PVE and commercial PVE device at I_{sc} = 0.65A and V_{oc} =21.5V: (a) I-V curve and (b) P-V curve.

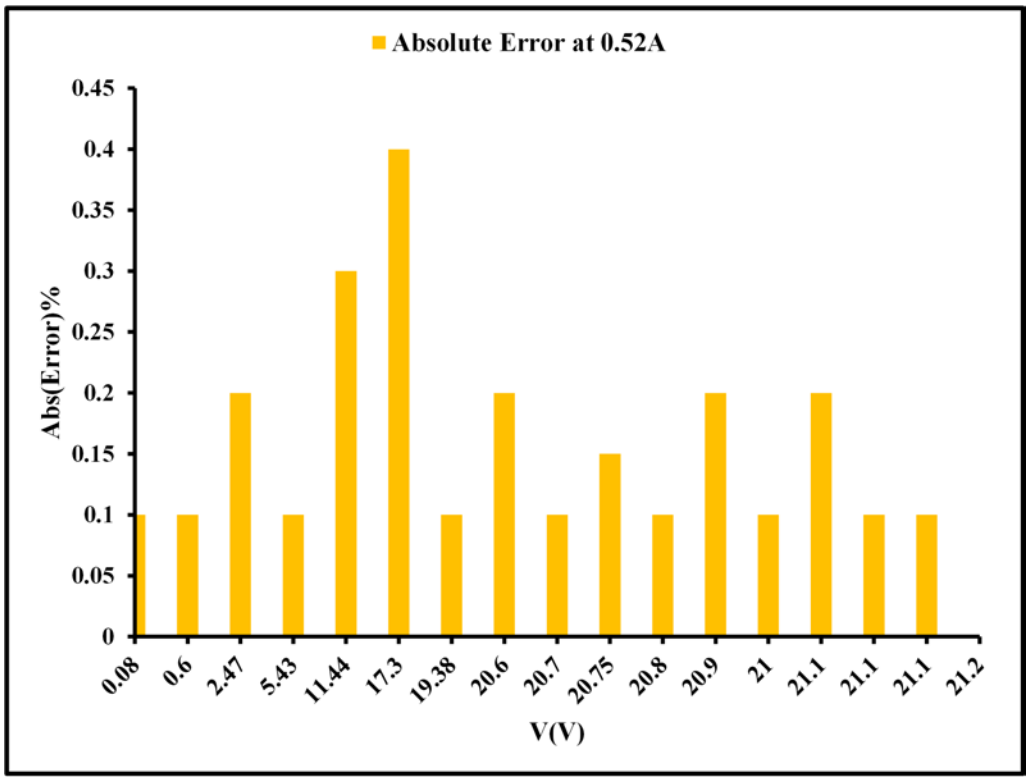


(a)

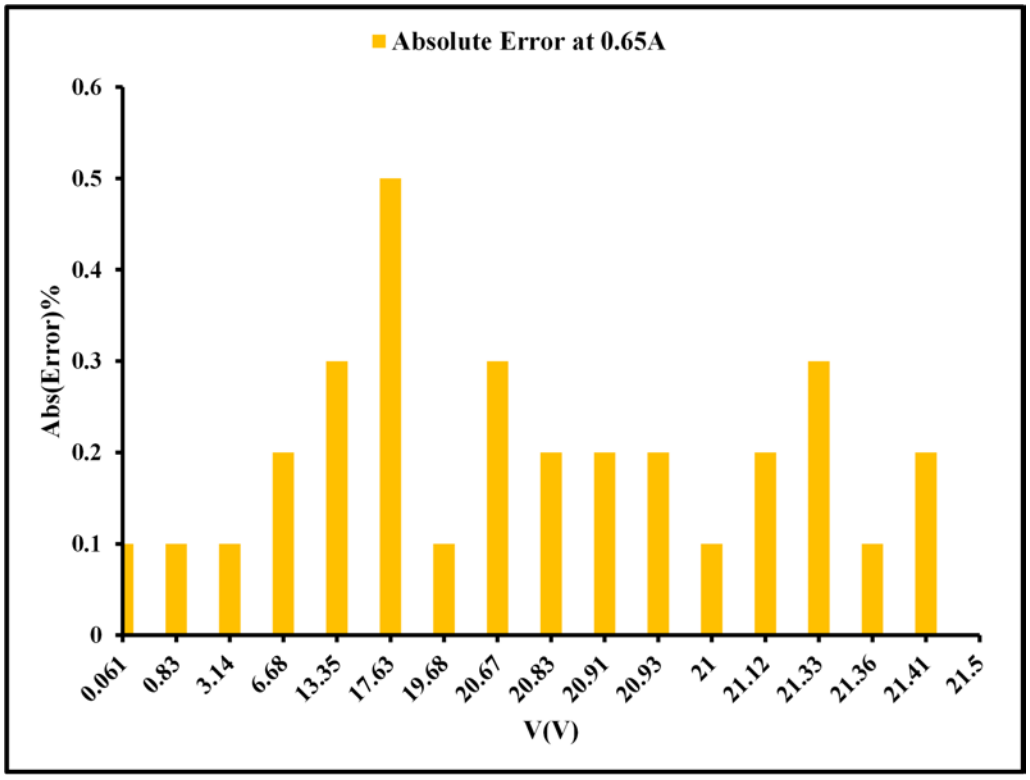


(b)

Figure 5.14: The comparison of characteristic curves of the real photovoltaic panel, proposed PVE and commercial PVE device at I_{sc} = 0.52A and V_{oc} =21.3V: (a) I-V curve and (b) P-V curve.



(a)



(b)

Figure 5.15: The maximum absolute deviation between the real PV panel I–V characteristic curve and the one generated by the PVE based on the diode string: (a) at $I_{sc} = 0.52$A and (b) at $I_{sc} = 0.65$A.

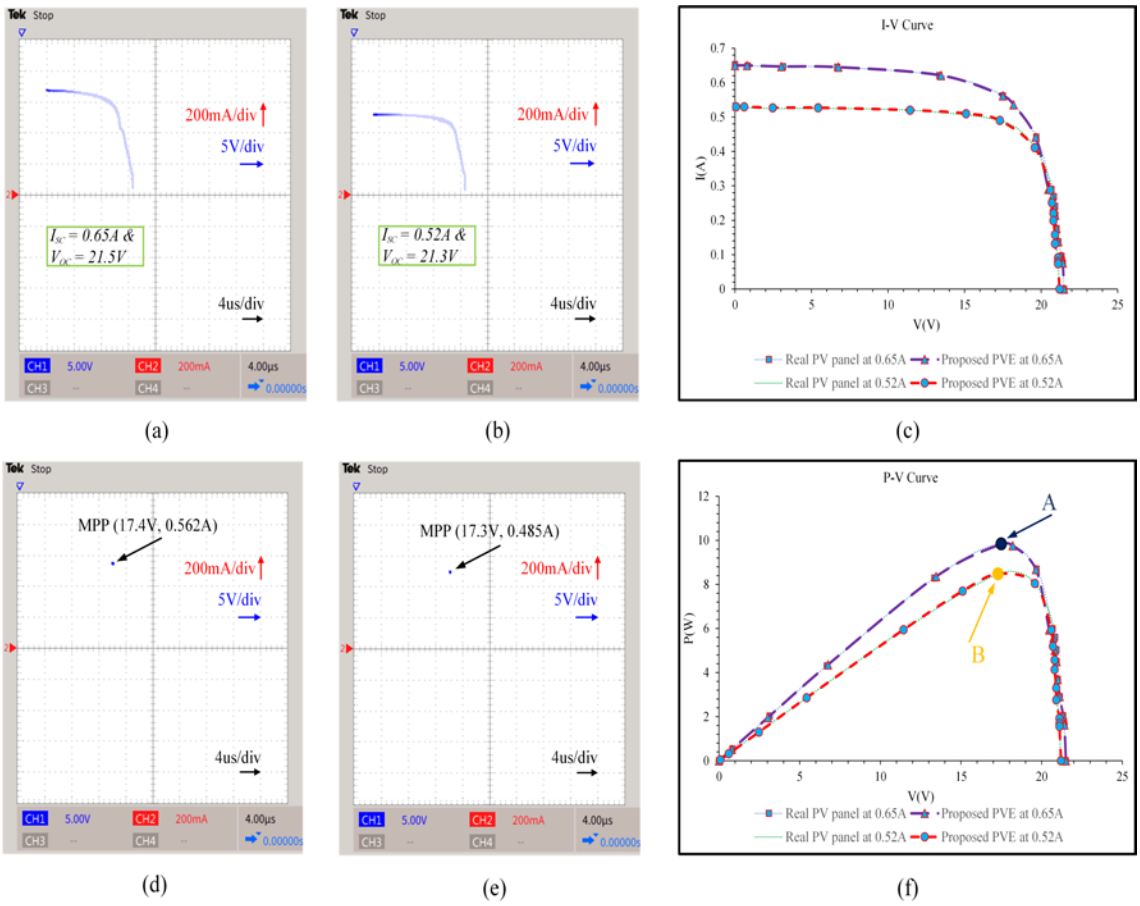


Figure 5.16: Experimental results showing the following: (a & b) drawing of the I-V curve based on the MPPT (boost DC/DC converter), when the I_{sc} equals 0.65A ($990W/m^2$) and 0.52A ($795W/m^2$), respectively, (d & e) MPP at the different irradiation levels, and (c & f) I-V and P-V curves, respectively.

thermal imaging camera (FLIR TG167) is used to show the change of temperature against the output current. It can be seen that the diode string temperature increases from 29.5°C to 94.2°C, which indicates a rapid increase in the power loss. After using the proposed switching circuit, the temperature only increases from 27.5°C to 35.1°C on the diode string in Mode-I. In Mode-II, the diode string is switched OFF, and the diode string temperature drops back to room temperature. Meanwhile, the NIBB DC/DC converter begins to work in this mode. The temperature increases from 24.8°C to a maximum of 30.1°C in the NIBB branch based on topology A, and by using topology B, it increases from 23.6°C to 26.5°C. It is also

shown in Fig. 5.17 that the power efficiency of the PVE based on the diode string decreases from 98.8% to 2.8% at the output loads of 10Ω and 270Ω, respectively. In addition, the proposed emulator based on both topologies A and B show significant improvement in overall conversion efficiency, with the efficiency varying from 98.8% to 81.48% and 85.98% based on topologies A and B, respectively, using the same experiment setup. The power efficiency is calculated based on Equation (5.2) [137], as follows:

$$Efficiency(\%) = \frac{P_{out}}{P_{in}} \times 100 \tag{5.2}$$

where the P_{out} is the output power, and the P_{in} is the input power.

The mean time to failure (MTTF) is used to compare the PVE based on the diode string and the proposed approachs [145, 146]. The lifetime of the PVE based on the diode string approach in the worst-case scenario, the OCV operate condition with an operating temperature of 94.2°C, is 15000 hours. Furthermore, the lifetime of the PVE based on topologies A and B is 147000 and 154000 hours, respectively. Hence, the maximum operating temperature for the proposed PVEs is equal to 30.1°C and 26.5°C, respectively. Furthermore, the mathematical model of the MTTF under thermal and electrical stresses is expressed as [145, 146]:

$$MTTF = (I^{-0.1699}) \times exp(\frac{4197.9}{T_m} - 2.5774) \tag{5.3}$$

where the I is the maximum operating current that goes through the power device at the worst-case scenario, and the T_m is the measured operating temperature in Kelvin.

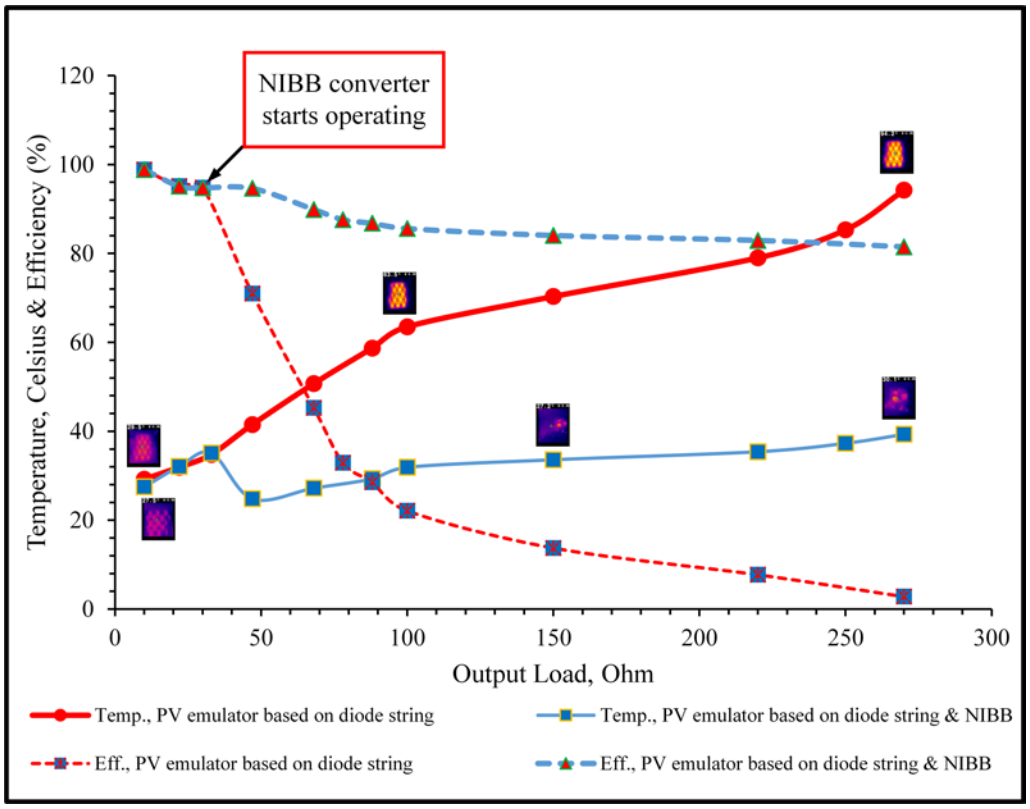
The power loss analysis for the PVE based on the diode string compared with the proposed topology is shown in Fig. 5.18. It is clear from the figure that the power loss for the emulator design using only the diode string increases rapidly, especially at the voltage source region, where it reaches the maximum power dissipation at the OCV operating condition. In addition, the proposed topologies, i.e., A and B, exhibit good behaviour compared to the diode string solution in terms of power

loss. This comparison can be used to explain the increase in cost of the presented solution. Furthermore, the power losses of each semiconductor device at different output loads or various power levels based on the NIBB converter are depicted in Fig. 5.19. In addition, in the diode string case, the power loss value at different power levels is shown in Fig. 5.18.

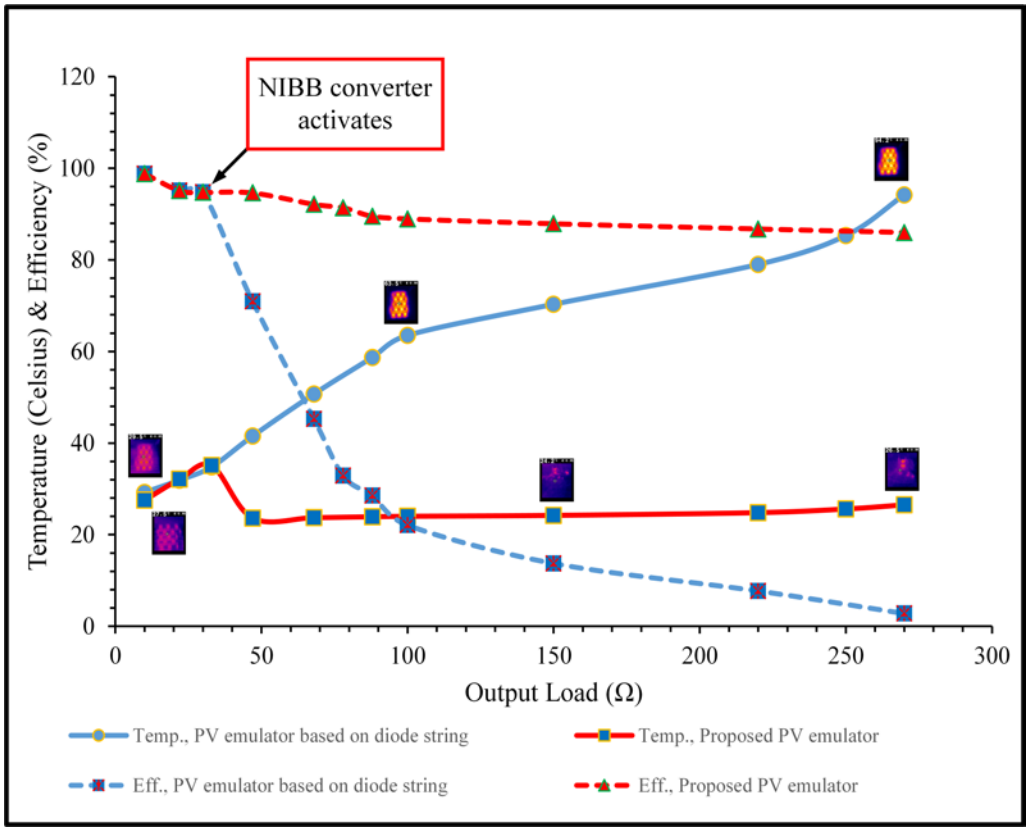
The dynamic response of the PVE based on the diode string, proposed PVE, i.e., topologies A and B, programmable PVE device (PPVE, model: EA-PSI 9360-15 2U), and actual PV panel are shown in Fig. 5.20, where the I_{PV} varies from 0.185A to 0.385A based on the programmable electronic load (model: BK8500). The dynamic behaviour of the PVE based on the diode string lags by 3ms compared with the real PV panel, as shown in Fig. 5.20 (a). In Fig. 5.20 (b), it is notable that the dynamic behaviour of the PVE based on topology A lags by 3.5ms compared with the real PV panel. In Fig. 5.20 (c) (i.e., topology B), it is notable that the dynamic behaviour of the proposed PVE lags by 3.2ms compared with the real PV panel. Nevertheless, the PPVE lags by 120ms compared with the real PV panel, as shown in Fig. 5.20 (d). The enhanced PVE is very effective, and it has an acceptable dynamic response when compared with both the actual PV panel and PPVE. The dynamic response of the proposed PVE also compares with some of the existing PVE platforms, as shown in Table 5.3. The proposed emulator shows the best response time compared with the existing solutions.

Table 5.3: Comparison of different aspects of existing platforms with the proposed PVE

No.	Author\s (Ref.)	Converter used	Control complexity	Cost	Dynamic response (ms)	Efficiency at MPP (%)
1	Cirrincione et al. [126]	Buck	Complex	Moderate	160	$\leq$ 93.5
2	EA-PSI 9360-15 2U [127]	SMPSU	Complex	High	120	$\leq$ 93
3	Ayop and Tan [23]	Buck	Complex	Moderate	21.25	93
4	Remache et al. [9]	Boost	Complex	High	18	$\approx$ 90
5	Koran et al. [6]	Buck	Complex	High	3.8	$\leq$ 90.2
6	Proposed PVE (i.e., topology A)	Diode String & NIBB	Moderate	Moderate	3.5	94.75
7	Proposed PVE (i.e., topology B)	Diode String & NIBB	Moderate	Moderate	3.2	95.7
8	Proposed PVE	Diode String	Not needed	Low	3	94.25



(a)



(b)

Figure 5.17: Thermal behaviour based on the output load variation for the PVE based on the diode string and the proposed PVE using both the diode string and NIBB converter: (a) topology A and (b) topology B.

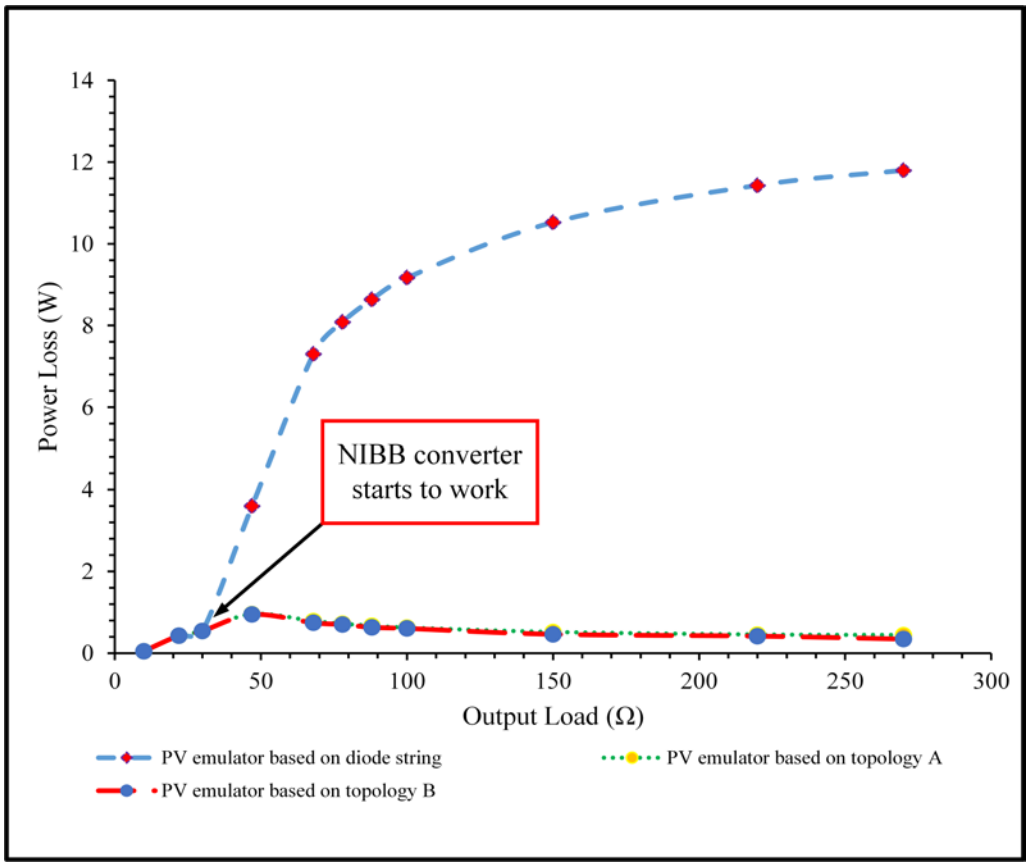


Figure 5.18: Power loss comparison between the PVE based on diode string and the proposed topologies A and B.

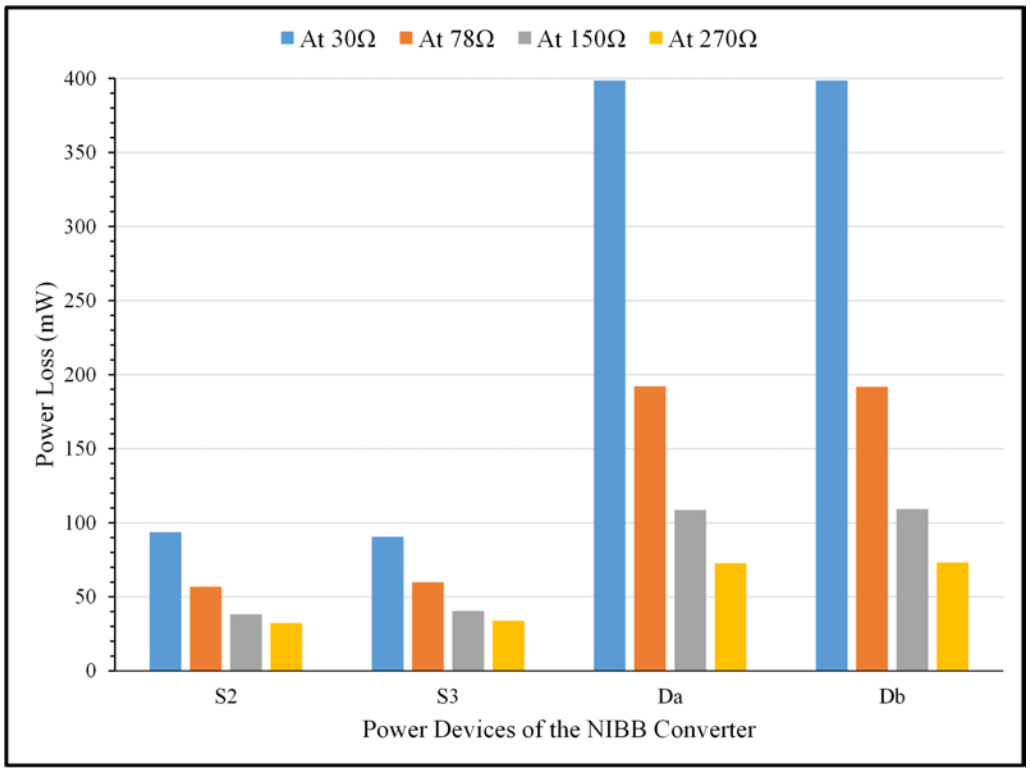


Figure 5.19: The power losses of the NIBB converter at different output loads.

5.5 Summary

This chapter proposes a PVE based on two new hybrid solutions that consist of a switching circuit (SC) in parallel with the diode string to minimize the power loss and improve the thermal performance of the emulator. The first switching circuit consists of a two-switch NIBB DC/DC converter, and the second SC uses an additional bypass switch. When the operating point of the PVE moves from the current source region to the voltage source region, the more efficient converter switches on to replace the diode string to continuously maintain the circuit operation of the emulator. The proposed PVE can mimic a PV panel with highly accurate results compared with the actual PV panel and commercial PVE under steady-state and dynamic operating conditions. The system performance has been studied from both thermal and electrical perspectives.

The main problem of the PVE based on the physically equivalent single-diode PV-

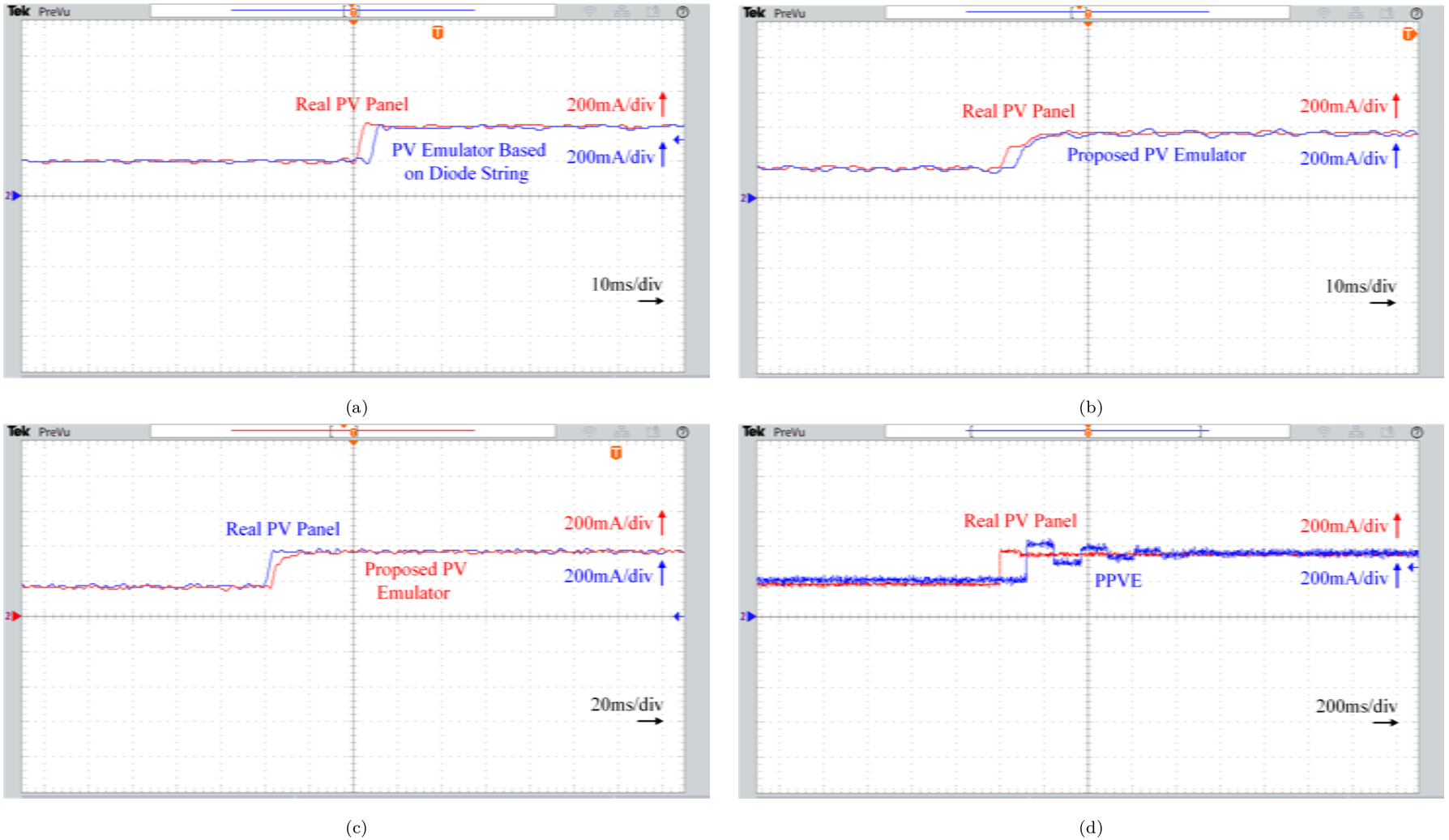


Figure 5.20: The dynamic PV characteristics when I_{PV} is converted from 0.185A to 0.385A based on load variation: (a) Real PV panel compared with the PVE based on the diode string, (b) Real PV panel compared with the proposed PVE, i.e., topology A, (c) Real PV panel compared with the proposed PVE, i.e., topology B, and (d) Real PV panel compared with the programmable PVE device. Time base (a & b): 10ms/div. Time base (c): 20ms/div. Time base (d): 200ms/div and I_{PV}: 200mA/div.

cell module is the increase in the diode string temperature, specifically at the open circuit condition (i.e., the maximum power dissipation). The diode string temperature increases from 29.5°C to 94.2°C from the short-circuit condition to the open-circuit condition, respectively, without any cooling system, and the power efficiency decreases from 98.8% to 2.8%. With the presence of hybrid solutions, which start to work in the voltage-source region of the PVE, the overall power efficiency and thermal behaviour are improved, varying between 81.47% and 30.1°C and 85.98% and 26.5°C for the first and second proposed hybrid solutions, respectively, under the same operating conditions.

In addition, the proposed solutions show that the new emulator structures have a comparable dynamic response to the selected PV panel. It is also faster than the commercial PVE under the same working conditions, in which the proposed PVE lags behind the actual PV panel by only 3.5ms and 3.2ms for the first and second proposed hybrid solutions, respectively, as compared with a lag of 120ms by a commercial emulator under the 30% to 60% insolation change test. In addition, the proposed PVEs have been tested and verified by using a well-known MPPT techniques (P&O), and the results are similar to the results when the actual PV system is used.

Chapter 6

The Modeling, Design, and Control of a High-Efficiency PV Emulator Using a Combination of a Transistor-based PV Model and a Switching Circuit

6.1 Overview

Over the past decade, the authors of [52], [44], and [40] made a PVE that depends on the physically equivalent PV-cell model. It is consists of a DC voltage source operating in constant current mode and is associated in parallel with a diode string and two resistors. The authors of [31] used a transistor string instead of a diode string to construct a similar PVE with a greatly reduced number of components. However, both the diode and transistor-based methods have a common high power loss issue. Along with the power loss, its temperature rises rapidly as the current rate increases, and the worst-case scenario occurs at the OCV operating condition [31, 40, 44]. During the maximum power point (MPP), the main part of the current flows to the output load rather than the transistor string path (i.e., a current source region (CSR)). In this case, the power loss on the transistor string is low. In addition, the power loss rises when the emulator works at the voltage source region (VSR), i.e., beyond the MPP. Hence, the highest value of the power loss happens at the OCV operating condition, in which the main part of the current flows through the transistor string path. This issue is mentioned in [31], but a solution has not been provided yet. In addition, it has been noted that, it is unclear how the transistor string is designed to emulate the electrical characteristics of a selected PV system with high accuracy. Furthermore, the usefulness and capability of using the transistor-based PVE have not been thoroughly investigated, including the electro-thermal property, circuit parameters design, and the dynamic response.

This chapter firstly discusses the design and construction of a PV emulator that is based on a physical PV-cell model and the key design equations. In addition to the work shown in [31], the thermal problem related to the transistor string has been studied and investigated. This problem was solved by adding a DC variable speed fan that works as a cooling system, and while this approach reduces the total temperature of the proposed PV emulator, the system efficiency remains low. Secondly, therefore, this chapter also proposes a new solution using a switching circuit (SC) composed of a bypass path and a non-inverting buck-boost (NIBB) DC/DC converter, as shown in Fig. 6.1. It is combined into and parallels the

transistor string to reduce the total power loss while maintaining a fast dynamic response. In addition, a boost DC/DC converter loaded with a perturbing and observe (P&O) maximum power point tracking (MPPT) technique is applied to test and verify the proposed PVE [30, 40, 156]. The chapter is organized as follows: A system overview and description of the proposed PVE are presented in Section 6.2. Section 6.3 illustrates the design of the proposed PVE. The experimental results and discussion are given in Section 6.4. Finally, Section 6.5 concludes the chapter.

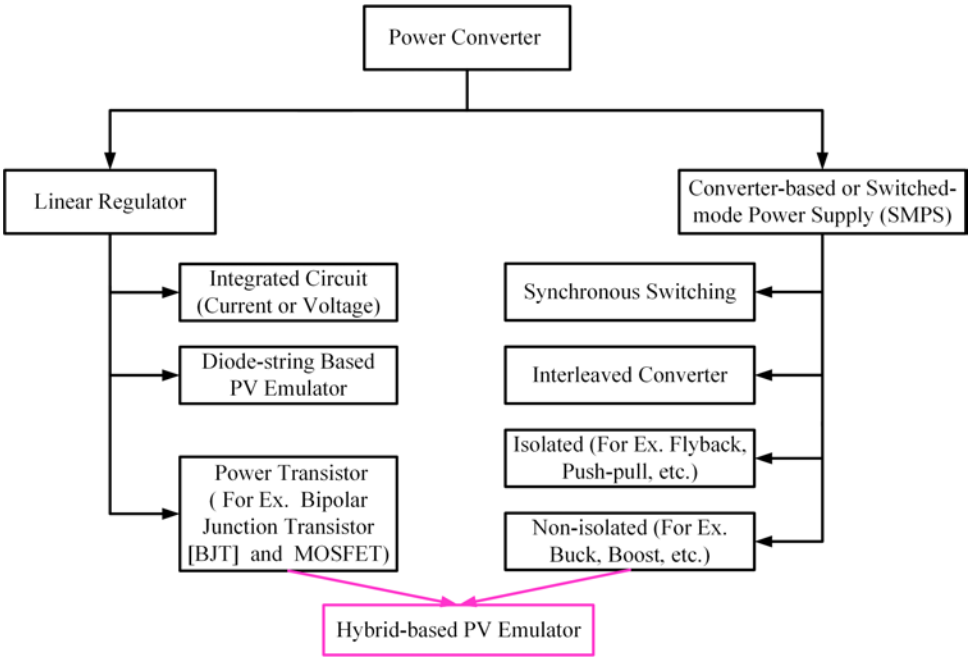


Figure 6.1: The power stage classification for the PVE application, including a proposed solution.

6.2 System Overview

6.2.1 Operation Principle of the PV Emulator

As illustrated in Fig. 3.4, the real PV panel has two working regions. In the first region, the PV voltage (V_{PV}) is lower than the voltage at MPP. In this state, the PV system operates as a constant current source, where the relationship between current and voltage is nearly linear. In contrast, the voltage rises from zero volts at the short circuit current to the voltage around the MPP, as seen in Fig. 3.4. In this region, the transistor string and bypass path are used to mimic this part of the

I-V curve. Then the current starts to change exponentially in the second region, where the PV panel works as a voltage source. However, in the second region, the PV voltage is larger than the voltage at the MPP, up to the OCV of the real PV system (i.e., the voltage source region). The NIBB converter begins to operate to emulate the rest of the I-V curve and also to minimize the total power loss on the transistor string while achieving an accurate emulation performance.

6.2.2 Description of the Proposed PV Emulator

To keep the design simple and accurate, this study relies on a PVE based on the physical single-diode PV model [22, 44]. It consists of a DC input source running in constant current source mode (I_{ph}), a transistor string with a bypass path to avoid the NIBB converter in Mode-I, an NIBB DC/DC converter arranged in parallel, a TI-TMS320F28379D controller, a MOSFET gate driver, an output load R_o, which varies by using the MPPT system based on the boost DC/DC converter to test and verify the realistic behaviour of the proposed PVE, and a variable electronic load (model: BK8500), R_L.

6.3 Example Design of the Proposed PVE

6.3.1 Design of the Transistor String

Generally, the modeling PV system in real conditions uses three strings of PV cells; however, for a low power PV system, one string is enough based on the load requirements. Fig. 6.2 shows the topology derivation of the PVE starting from the single-diode model for a single cell, a string of series cells, a Darlington pair to mimic a PV panel, a string of high power PV systems in a traditional series combination, and a modified diagonal topology, which uses at least one Darlington pair to feed a power transistor. The Darlington pair in this design amplifies and controls the base current of the power transistor, which has a reduced number of components compared with the diode-based PVE. A diagonal approach is selected for this work because the power level is not too high and this approach simplifies the design and control.

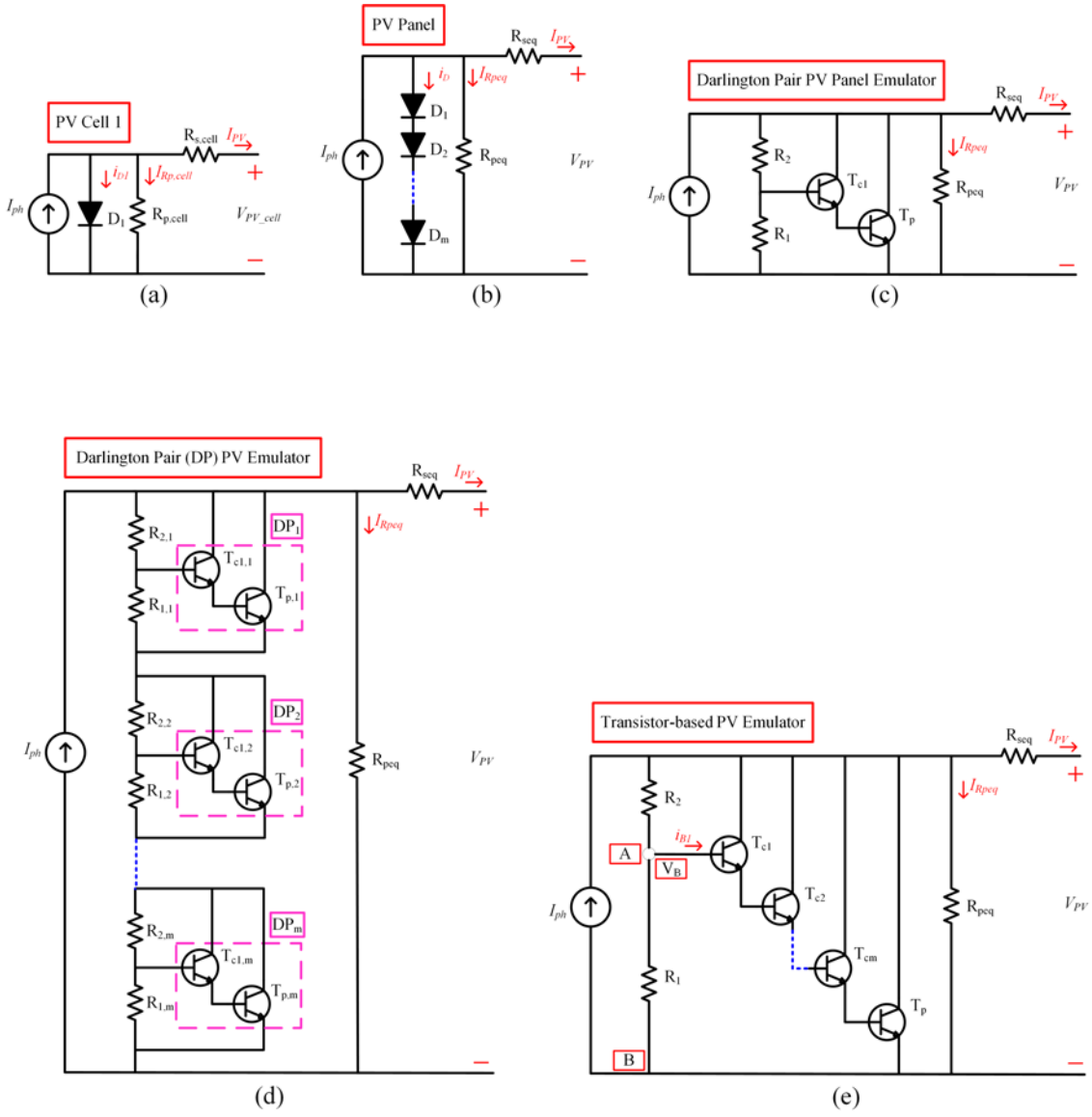


Figure 6.2: Representation of a PV system composed of the following: (a) One-diode model including both the series and parallel resistors, (b) One string of series connected PV cells (N) by using the one diode model, (c) One string of series connected PV cells (N) by using the Darlington pair (DP) model, (d) Multi-string of series connected PV cells or panels by using the DP model, and (e) One string of series connected PV systems by using the transistor-based model, where T_p is a power transistor, and is driven by a cascade of transistors T_{c1},.... m, amplifying the base current of T_p.

The proposed PVE model can be divided into two main parts, as shown in Fig. 6.3. The first part is the transistor string, which will be studied in-depth in this work, which uses the PV model equations to select the design parameters (R_1, R_2, number of required transistors) of the PVE to mimic a specific PV system (model: Powertech-ZM9054), where the values of R_{seq} and R_{peq} are calculated in a previous work [44]. The second component of the proposed PVE is a switching circuit, as illustrated in Fig. 6.3, in which the selected criteria of the paralleled converter are closely investigated in [30], and the NIBB converter is selected and constructed for this study. In addition, the behaviour of the proposed topology is tested and evaluated from an electro-thermal perspective.

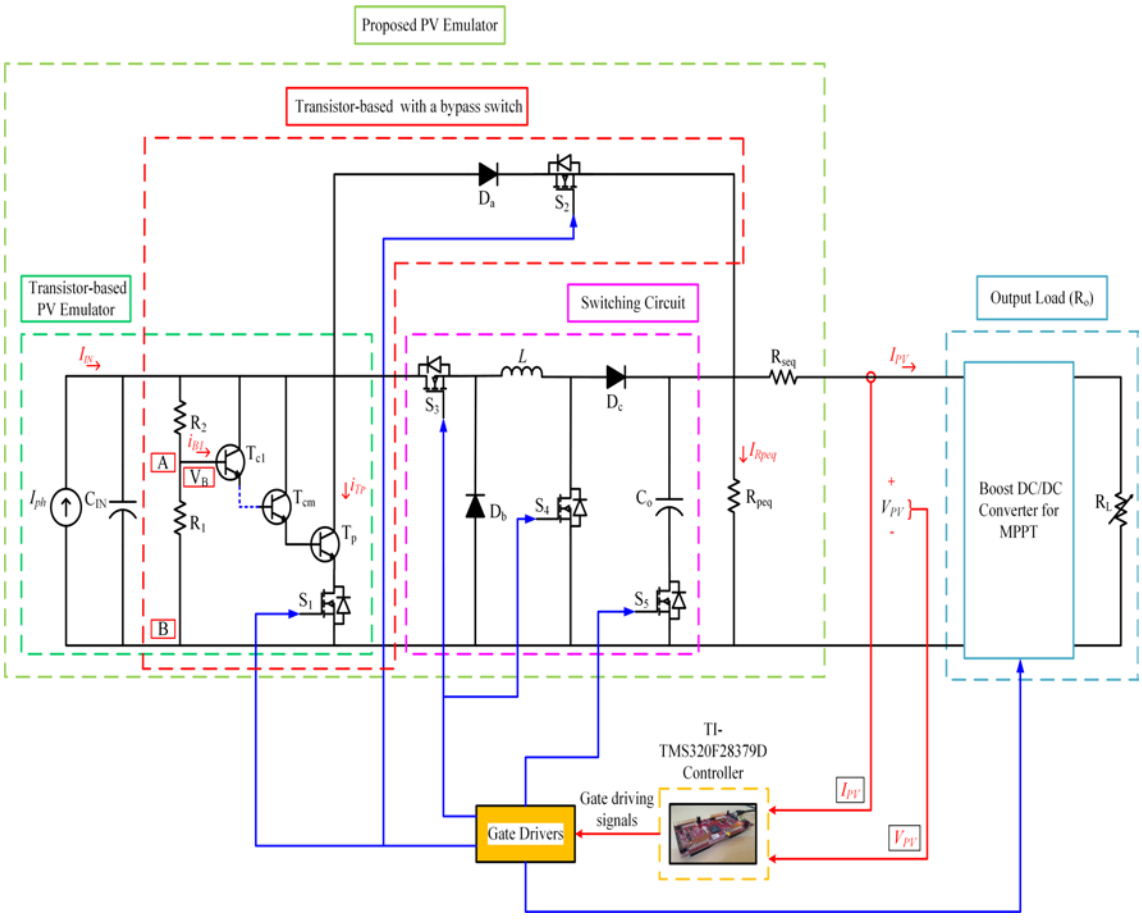


Figure 6.3: Block diagram and control scheme of the proposed PVE.

As shown in Fig. 6.3, the short circuit current of the real PV current is mimicked by

using a DC voltage source operating at constant current mode. The figure demonstrates that high power dissipation occurs at the OCV, where the main current goes through the power bipolar transistor (2N3055) branch and the rest of the current goes through the parallel resistor (R_{peq}), the collector of the control bipolar transistor (2N2219A & BC33725TA) and the voltage divider bridge (R_1 & R_2). Generally, in the PV system, the value of the R_{peq} is high, and the voltage divider bridge (R_1 & R_2) is used with a high resistor value. The current flowing through these resistors can be neglected. Thus, as a first approximation, the entire short circuit current I_{ph} is flowing through the power transistor (2N3055) at the OCV operation condition. This approximation gives rise to two design aspects, the first is to determine the worst operating condition and derive the current protection margin of the selected device.

Based on the datasheet of the power transistor (2N3055), it can be used to mimic a PV system with a maximum current and voltage up to 15A and 60V, respectively. In addition, it shows that the current gain is equal to 20, which means the base current should be equal the short circuit current divided by the current gain (20). It helps to select suitable lower power transistors (2N2219A & BC33725TA), whose datasheets can verify that this value is in conformity and is less than the maximum value of the collector current. The voltage of resistor R_1 is equal to the summation of the forward voltage of the series transistors, and by assuming R_1 is in range of kΩ, e.i., 5kΩ, it not difficult to deduce and find the current crossing through R_1. Next, the Thevenin equivalent circuit principle between points A and B (as shown in Fig. 6.3) is used to find and select the design parameters based on the equations below.

Eqs. (6.1) to (6.3) show the mathematical model of the proposed PVE based on the Thevenin equivalent circuit:

$$R_{th} = R_1 || R_2 = \frac{R_1 R_2}{R_1 + R_2} \tag{6.1}$$

$$V_{th} = \frac{R_1 V_{in}}{R_1 + R_2} \tag{6.2}$$

$$i_{B1} = \frac{V_{th} - V_B}{R_{th}}, V_{th} > V_B \tag{6.3}$$

where resistors R_1 and R_2 are used as a voltage divider to control the basing point (A), V_{in} is the input DC voltage source and is equal to the OCV (V_{oc}), V_B is the DC biasing voltage between points A and B, and i_{B_1} is the base current of the first transistor T_{c1}.

$$\begin{aligned} &i_{E_1} = i_{B_1} + i_{C_1} = i_{B_1} + \beta_1 i_{B_1} = (1+\beta_1) i_{B_1}, \\ &i_{E_2} = i_{B_2} + i_{C_2} = i_{E_1} + i_{C_2} = (1+\beta_1) i_{B_1} + \beta_2 i_{B_2}, then \\ &i_{E_2} = (1+\beta_1) i_{B_1} + \beta_2 (1+\beta_1) i_{B_1} = (1+\beta_1)(1+\beta_2) i_{B_1}, \end{aligned} \tag{6.4}$$

Then,

$$\begin{aligned} &i_{E_3} = (1+\beta_1)(1+\beta_2)(1+\beta_3) i_{B_1} = \beta i_{B_1}, where \\ &\beta = (1+\beta_1)(1+\beta_2)(1+\beta_3) \cong (\beta_1)(\beta_2)(\beta_3), then \\ &i_{E_p} = (1+\beta_1)(1+\beta_2).....(1+\beta_p) i_{B_1} = \beta i_{B_1} \end{aligned} \tag{6.5}$$

In addition, the base current of the first transistor of the cascade, T_{c1}, is expressed by the following:

$$i_{B_1} \cong \frac{I_{sc}}{\beta} \tag{6.6}$$

where i_{B_1} is the base current of the T_{c1}, I_{sc} is the short circuit current of the real PV system, and β is the multiplication of the cascade transistor current gain.

6.3.2 DC/DC Converter Selection and Design

The switching circuit is the second part of the proposed PVE, as shown in Fig. 6.3. The selected criteria of the paralleled DC/DC converter are studied in detail in [30, 147, 149]. The NIBB DC/DC converter is chosen and designed for this study [30].

Table 3.2 shows the important characteristics of the chosen PV panel, including the maximum open-circuit voltage of 21.5V and the lowest short circuit voltage of 0V, which are used to select the maximum current and voltage value for the DC input source that is needed to feed the proposed PVE. The components used in this design are listed in Table 6.1. The maximum input DC voltage source value is adjusted to 19V, which is less than the OCV, and the NIBB operates in boost mode (i.e., the voltage source region). Additionally, the NIBB may be used as a backup system in buck/boost mode to replicate the I-V curve in the event that the transistor string fails. Based on the NIBB converter, the V_{PV} ranges from 17V to 21.5V when the hysteresis voltage band control is applied. Based on the datasheet of the selected PV panel and the control strategy, the critical inductance value (525µH) is found when the input voltage source is at 19V and 0.65A, at which the NIBB converter operates in boost mode, and the maximum duty cycle is set to 0.55. However, the inductor value is chosen as 1mH to keep the converter working in CCM and reduce the current ripple [30].

6.3.3 Operation Principle of the Proposed PV Emulator

There are two operational modes for the proposed PVE topology, as indicated in Fig. 6.4. When the V_{PV} is less than the voltage at the MPP, the first mode occurs (i.e., the current source region). In this mode, i.e., Mode-I, S_1 and S_2 are turned on, allowing the current to flow through the transistor string and the output current to be complementary to the transistor string current to shape the desired I-V curve in this region, bypassing the NIBB converter. In the second mode, the NIBB DC/DC converter starts working after the voltage reaches the MPP level and rises to the OCV voltage (i.e., the voltage-source region). To charge the inductor, both S_3 and S_4 are turned on (Fig. 6.4 (b)). The switches are then turned off to discharge the inductor via D_b and D_c (Fig. 6.4 (c)). In addition to the two switches in Mode-II, switch S_5 is utilized to regulate the output capacitor, which is not used in Mode-I due to its sluggish dynamic response. The output voltage is formed according to the characteristics of the selected PV panel by adjusting the duty cycle of the MOSFETs depending on the values of the output resistive load. To reduce power

Table 6.1: Main specifications of the experimental prototype.

Component	Model/Value
Digital Controller	TMS320F28379D
Switching Frequency	100kHz
MOSFET	IRF540N
Transistor	2N3055, 2N2219A & BC33725TA
R_1	5kΩ
R_2	60kΩ
Low Side MOSFET Driver	TC4428
High Side MOSFET Driver	IR2184PBF
D_a, D_b & D_c	MBR20200CT
D_1,.....D_{27} (Diode String)	1N5400
Current Sensor	LEM-LTS-6-NP
Coupled Inductor Core	Toroidal Inductor
L (NIBB Converter)	1mH
PV Panel	Powertech-ZM9054
Programmable PVE Device	EA-PSI 9360-15
Programmable DC Electronic Load	BK8500
Thermal Imaging Camera	FLIR TG167
DC Fan	PVA092G12M

loss, the transistor string is turned off in this mode. This converter, i.e., the NIBB, limits and controls the current rate on the transistor string to improve its thermal performance. Depending on the transistor string electrothermal characteristics, this circuit will help produce a quick dynamic response. When operating in the first mode, it is not necessary to employ an NIBB converter since the current is practically linear as the voltage increases from zero volts at the short circuit current to the voltage at the MPP. Afterwards, the current begins to change exponentially.

6.3.4 Controller and Control Strategy

The LAUNCHXL-F28379D microcontroller from TI is used in this study [151, 152]. The feedback control system and the MPPT method are built based upon the schematic diagram presented in Fig. 6.5. The mode selection algorithm is selected based on the control diagram seen in Fig. 6.6.

The program begins by initializing the duty cycles by assuming that the proposed emulator works in Mode-I. Afterwards, during the residual magnetization of the current sensor, an initial zero calibration is required to make the reference value equal to zero. In Mode-I, i.e., the transistor string mode, the V_{PV} value is less than 16.5V. In this mode, i.e., CSR, the relationship between the output PVE current and voltage is nearly linear before the MPP, where S_1 and S_2 are ON and S_3, S_4, and S_5 are OFF. Then, the output voltage V_{PV} is measured again. If it remains less than 16.5V, the proposed emulator keeps working in Mode-I. In order to prevent chattering between the operating modes, a small hysteresis band, a 1V window, is used. However, if the V_{PV} is greater than 17.5V and lower than the OCV, the emulator works in Mode-II, i.e., VSR, where the NIBB begins to work. In this mode, S_1 and S_2 are OFF, S_5 is ON, and S_3 and S_4 are the control switches based on the look-up table (LUT) [153, 154].

In addition to the previous control strategy, Fig. 6.6 presents another control method in Mode-II that results in a tradeoff between the thermal and dynamic responses of the proposed PVE when the sudden load changes occur. In this study, a value of 100mA is used as an example to approve the model, at which point the emulator

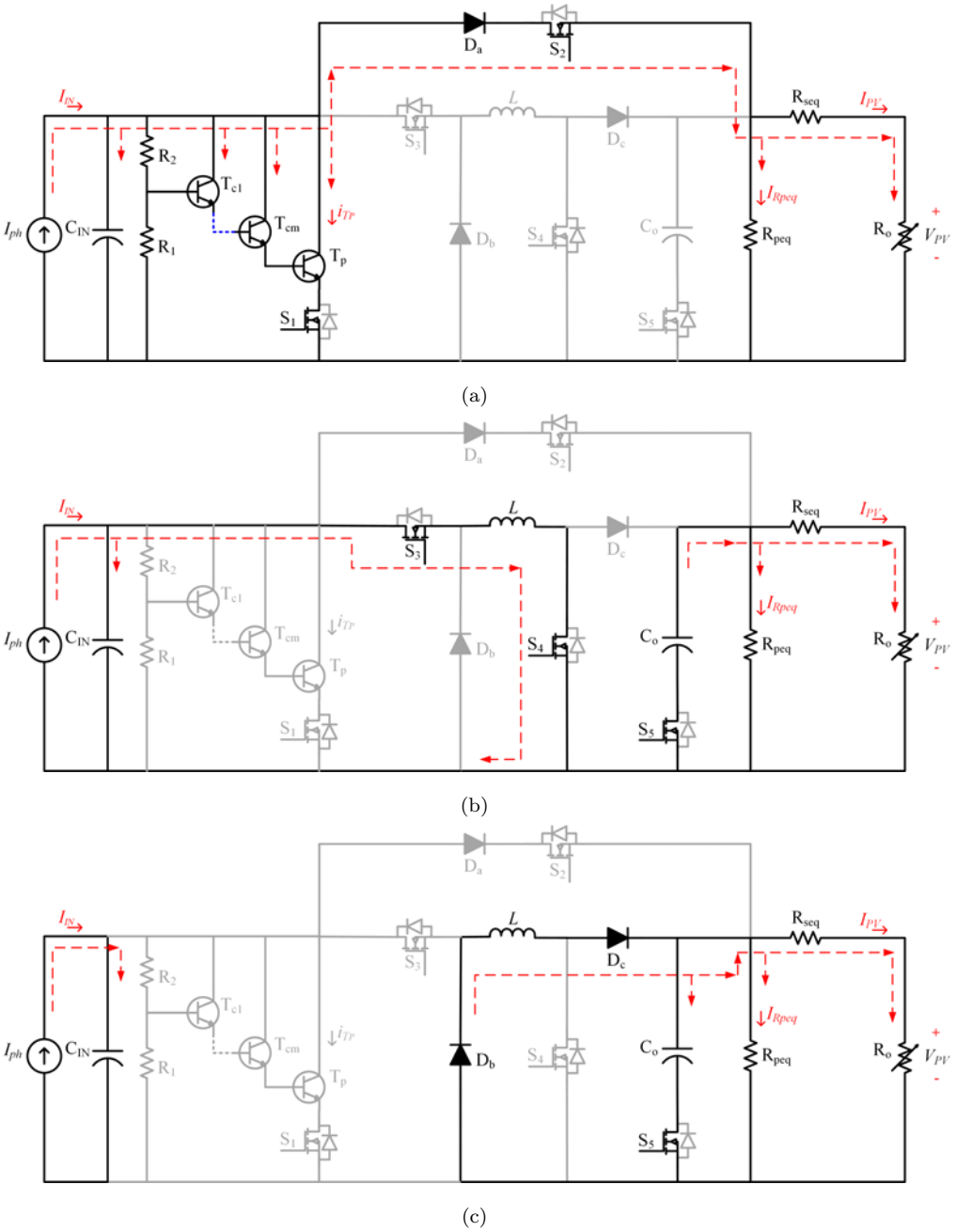


Figure 6.4: Operation principle of the proposed PVE: (a) Mode-I when S_1 and S_2 are ON and (b) and (c) Mode-II when NIBB works.

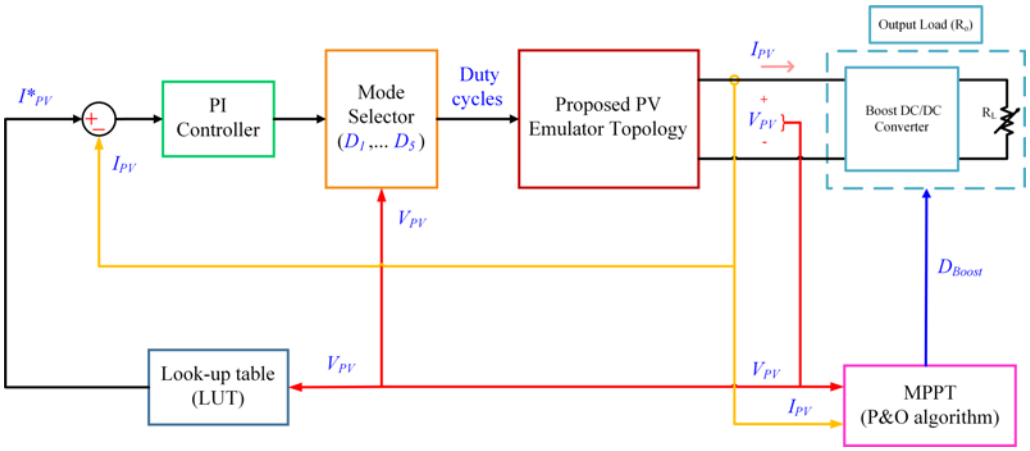


Figure 6.5: Block diagram of the closed-loop control.

mode changes from Mode-II to Mode-I for 100ms.Then, the I_{PV} is reread several times, and the standard deviation is calculated from this set of measurements to check the stability of the current reading. If the output current reaches and stays at a specific point, then V_{PV} is measured to select the suitable operation mode. However, if the I_{PV} value is still unstable, the emulator continues to work in Mode-I for another 100ms, and then the output emulator current is rechecked. The performance of the enhanced PVE is tested and verified at different irradiation levels, and the output load is mimicked by using a boost DC/DC converter loaded with a P&O algorithm.

6.4 Experimental Results and Discussion

6.4.1 Experimental Setup

Fig. 6.7 shows an experimental prototype that is used to test and evaluate the proposed PVE. The maximum open-circuit voltage (V_{oc}) of the selected PV panel (model: Powertech-ZM9054) is 21.5V, and the short-circuit current (I_{sc}) is 0.65A. Compared to an actual 10W PV panel, the recommended emulator has performed fast and accurate with the proposed control strategy. Another comparison is made with an available commercially available PVE (PPVE, model: EA-PSI 9360-15 2U). The experimental findings demonstrate that the proposed PVE, the selected PV panel, and the PPVE have similar electrical properties.

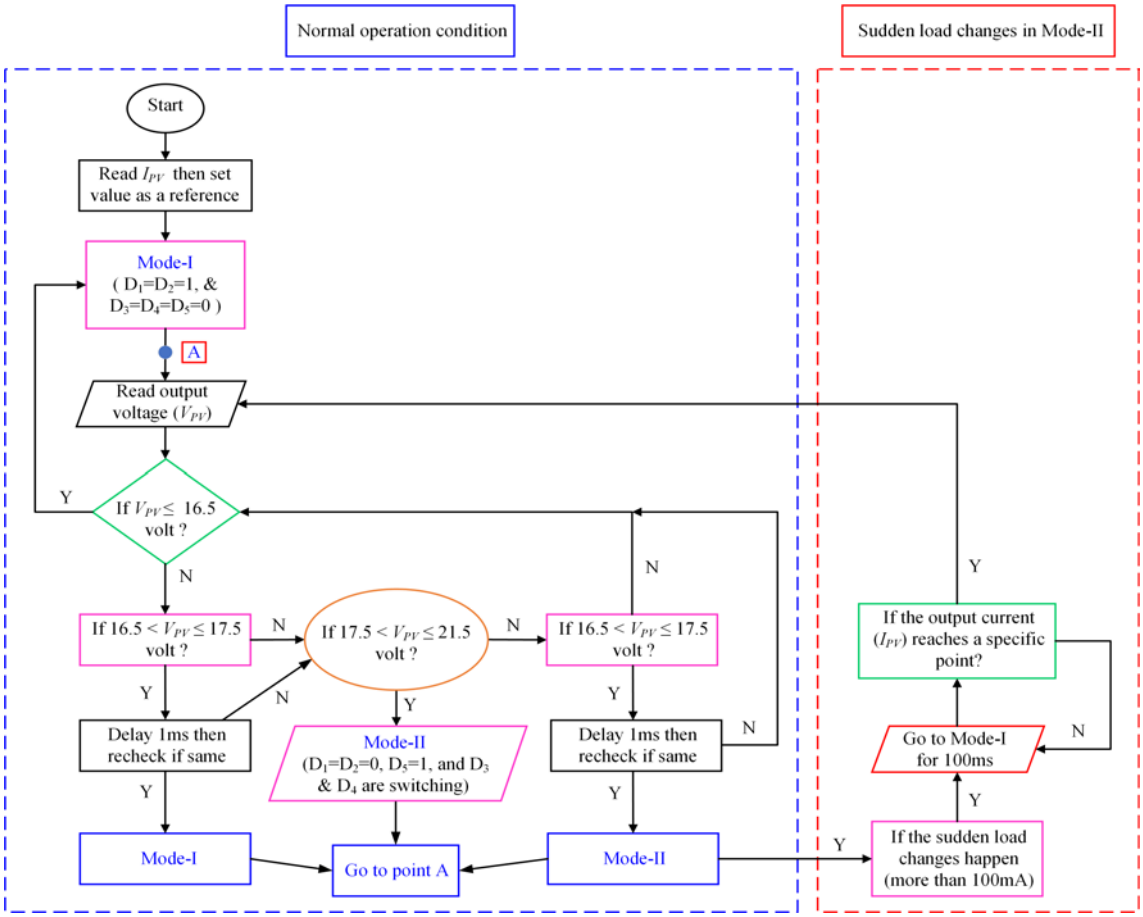


Figure 6.6: Flowchart of the operating mode selection algorithm.

6.4.2 Thermal Behaviour Based on the Cooling System

In this section, an experimental work has been conducted to test and validate the effect of a cooling system using an adjustable speed DC fan (model: PVA092G12M) on the thermal behaviour of the PVE based on the transistor string with the rotating speed varying from 0 up to full speed. It is controlled by using a simple switching circuit and variable duty cycle. This study concentrates on and highlights the thermal response of the main power transistor (model: 2N3055), as it is the main source of heating and power loss, as shown in Fig. 6.8.

Fig. 6.8 presents the thermal behaviour and the issues related to the main power transistor when using the transistor-based PVE model to simulate the PV panel. In the figure, the x-axis represents the duty cycle that is used to control the speed of

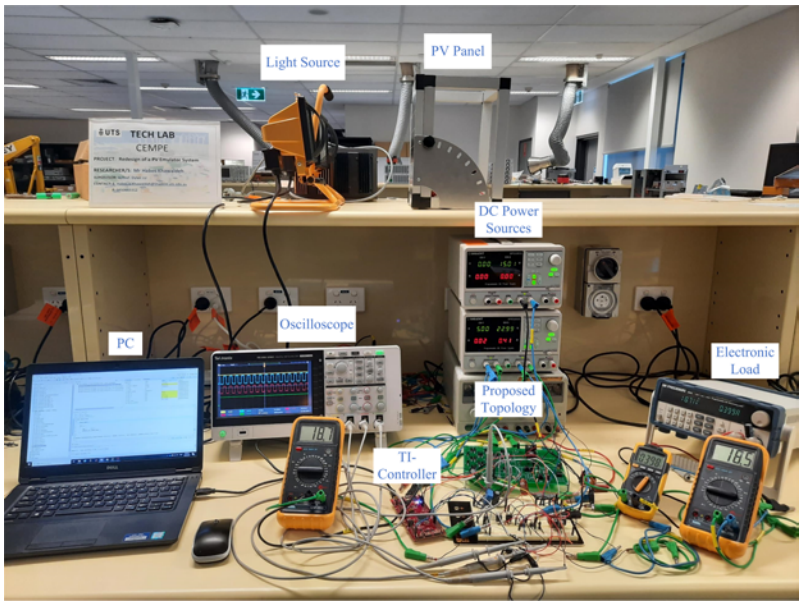


Figure 6.7: Experimental bench.

the DC fan, and the y-axis shows the output load of the PVE. In addition, Fig. 6.8 demonstrates that while going from the left- to the right-hand side, the fan speed increases with the duty cycle. The resistive load increases from bottom to top until the point when the emulator reaches the OCV condition. A thermal imaging camera (model: FLIR TG167) captures the temperature change as the current increases.

The figure shows that without the cooling system, the transistor temperature (model: 2N3055) rises from 29.4°C to 93.5°C, as seen in the first column on the left. Then, the DC fan (model: PVA092G12M) starts to work, and the duty cycle at the first control scenario operates at D=0.25. In this case, the power transistor temperature increases from 28.2°C to 84.3°C. The second control scenario occurs when the duty cycle is set to D=0.5, and the operating temperature increases from 27.4°C to 75.1°C. Next, the duty cycle is set to D=0.75. In this case, the power transistor temperature increases from 26.3°C to 66.8°C. A duty cycle of D=1.0 is used for the last control scenario, in which the operating temperature increases from 25.2°C to 53.6°C. The cooling system is used to keep the power transistor temperature at an acceptable value to minimize the effects of the high temperatures on the PVE characteristics.

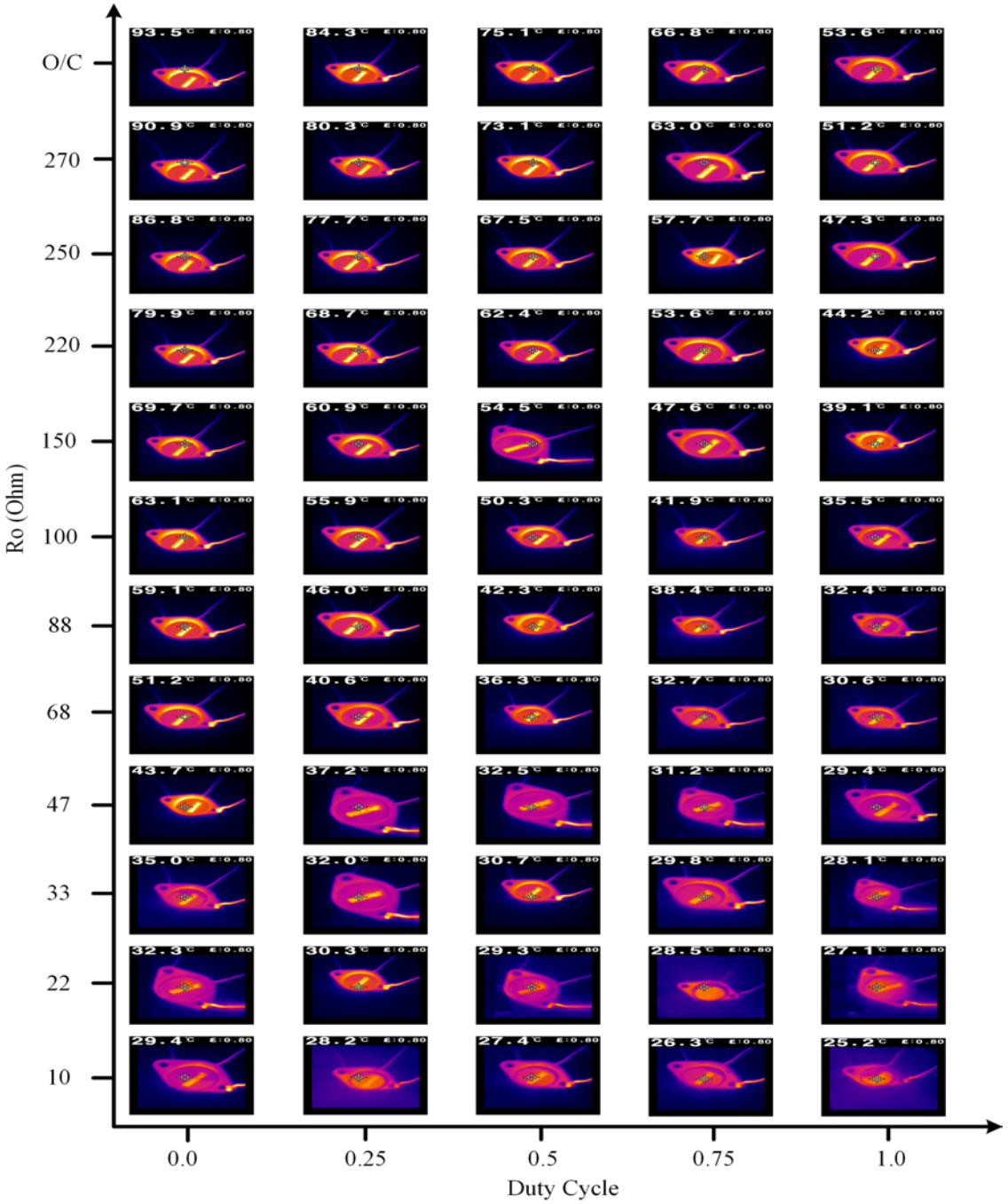
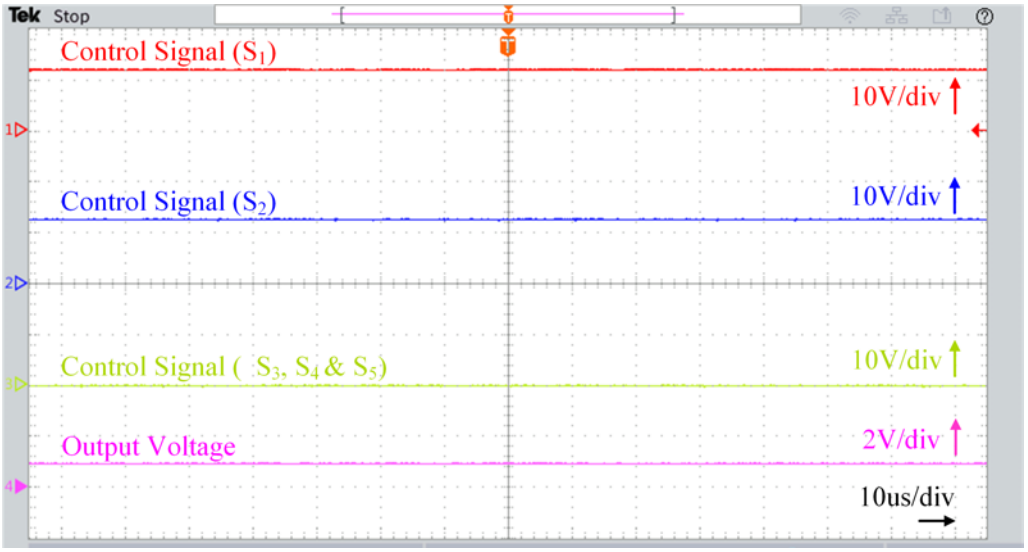


Figure 6.8: Thermal behaviour of the 10W transistor-based PVE at different operating conditions.

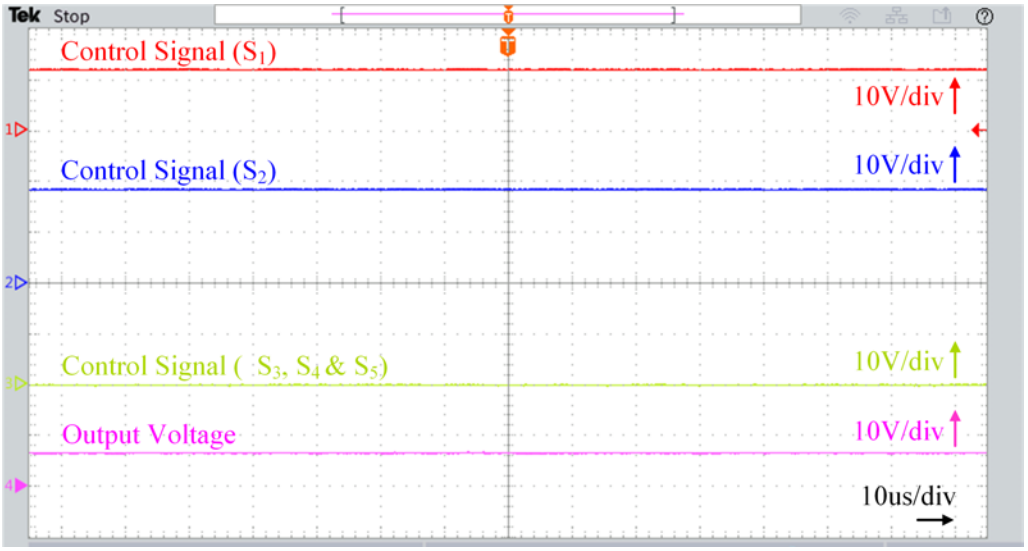
6.4.3 Steady-state Response

Figs. 6.9 (a & b) shows the measured steady-state results for the proposed PVE in Mode-I, in which only the transistor string is active. The top waveform represents the gate control signal for S_1, followed by the control signal for S_2, then the control signal for S_3, S_4, and S_5, and the output voltage, when the output load is at 1Ω and 10Ω, respectively. It is clear from the figure that the transistor string is working when S_1 and S_2 are ON and S_3, S_4, and S_5 are OFF. Based on the DC supply voltage value (19V), the NIBB converter works as a boost converter in Mode-II, as shown in Fig. 6.10. In Fig. 6.10, it is clear that the NIBB converter is operating. The experimental steady-state results for the proposed PVE in Mode-II, when only the NIBB DC/DC converter is active, are shown in Fig. 6.10. The top waveform represents the gate control signal for S_1, followed by the control signal for S_3, the control signal for S_4, and the output voltage of the proposed PVE when the output load is at 33Ω and 250Ω, respectively. It is clear that the NIBB converter is operating, where S_5 is ON, the S_3 and S_4 are switching, and S_1 and S_2 are OFF. Moreover, Fig. 6.10 (a & b) shows that the duty cycle values of S_3 and S_4 are greater than 0.5 at 33Ω and 250Ω, respectively. In addition, Fig. 6.10 (b) presents the output control signal of the high-side driver to ground for S_2 to show that S_2 is OFF in Mode-II.

Figs. 6.11 and 6.12 reveal a similarity between the I-V and P-V characteristic curves based on the simulation and experimental results for the commercial PVE (PPVE, model: EA-PSI 9360-15 2U), the proposed PVE, the PVE using the MATLAB program, and the real PV panel (model: Powertech-ZM0954). Fig. 6.11 (a) shows the I-V curve and Fig. 6.11 (b) shows the P-V curve for the same setup. From Fig. 6.11, it is clear that the actual PV panel short circuit current (I_{sc}) is equal to 0.65A and the OCV equals 21.5V at $990W/m^2$ and 26°C. To simulate the same electrical characteristics of the real PV panel, the DC power source works at constant current mode and is limited to 0.65A based on (2.9) with the maximum voltage value set to 19V. The actual PV panel voltage and current are read again at another irradiation level ($540W/m^2$ at 27°C), at which the OCV drops to 21.3V and the short circuit current decreases to 0.35A. The current and voltage values are used as input for

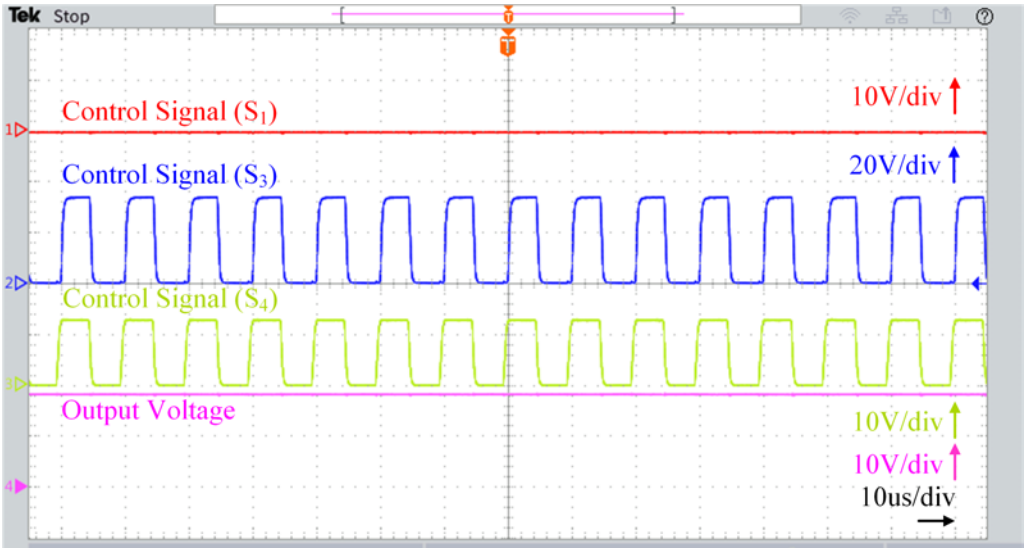


(a)

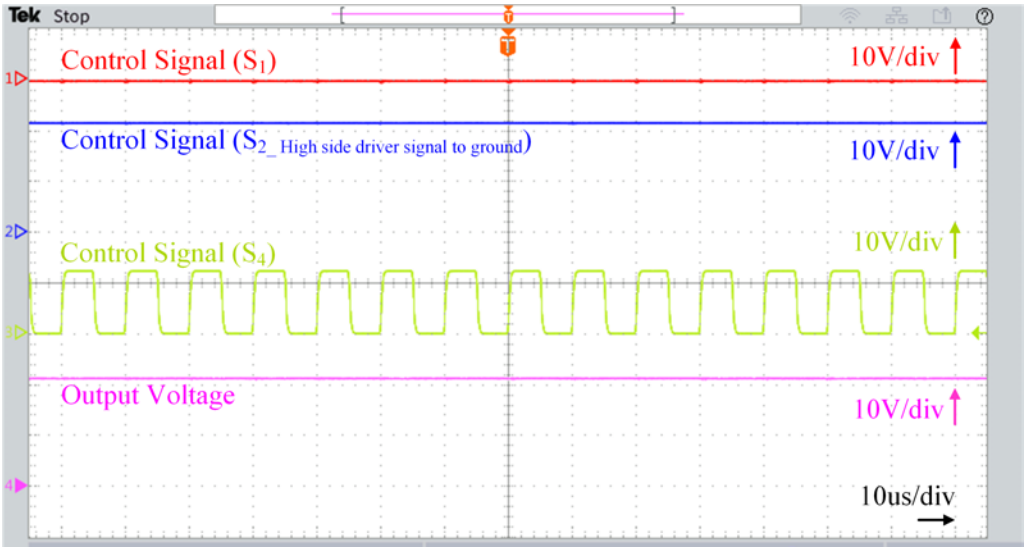


(b)

Figure 6.9: The gate control signals and output voltage of the proposed PVE: (a) at 1Ω and (b) at 10Ω resistive load. Time base: 10us/div. Ch1 (red): 10V/div. Ch2 (blue): 10V/div. Ch3 (green): 10V/div. Ch4 (a-pink): 2V/div. Ch4 (b-pink): 10V/div. Transistor string mode.



(a)



(b)

Figure 6.10: The gate control signals and output voltage of the proposed PVE: (a) at 33Ω and (b) at 250Ω resistive load. Time base: 10us/div. Ch1 (red): 10V/div. Ch2 (a-blue): 20V/div. Ch2 (b-blue): 10V/div. Ch3 (green): 10V/div. Ch4 (pink): 10V/div. NIBB mode.

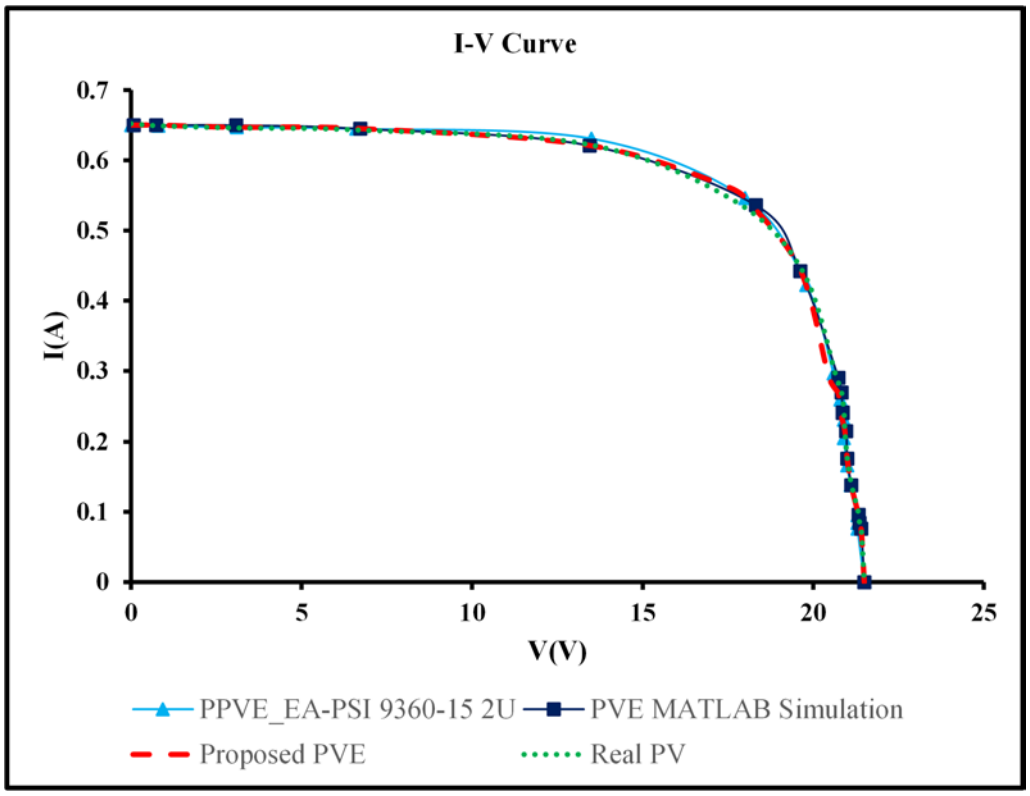
the proposed PVE, for which the DC power source is limited to 0.35A based on (2.9) and the voltage value is kept the same (19V). The enhanced PVE has a high performance, with the current and voltage matching that generated by commercial PPVE and the actual PV panel.

6.4.4 Accuracy Comparison

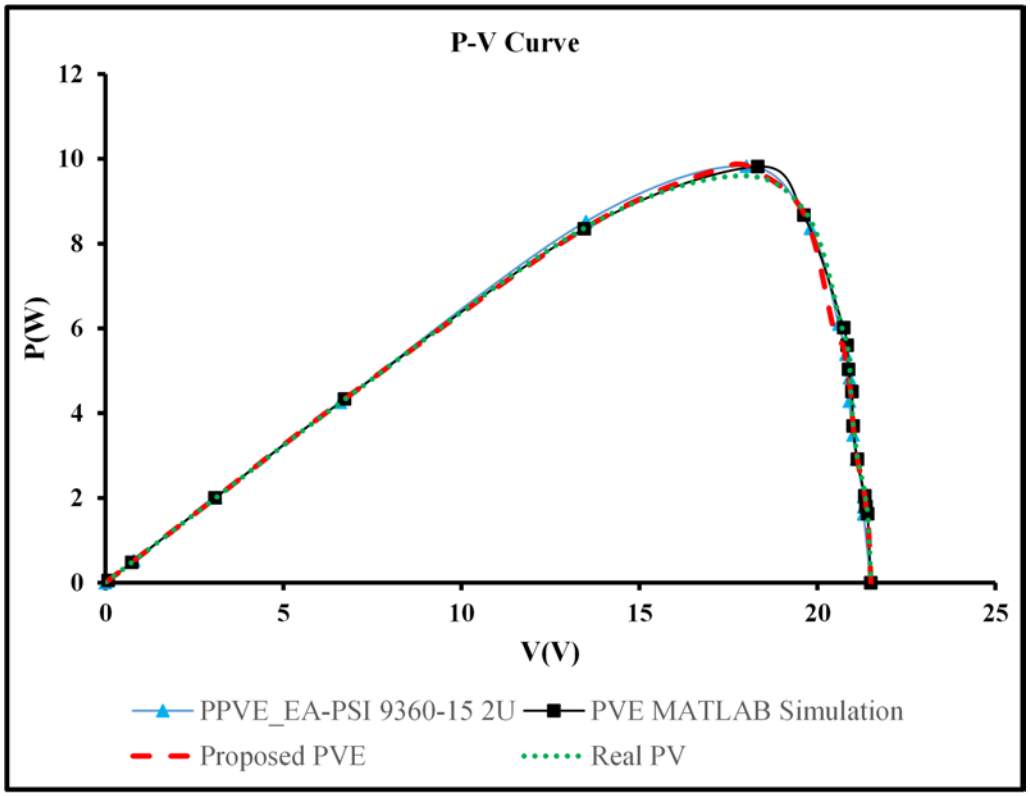
The absolute deviation value (error) is determined to indicate the inaccuracy, i.e., the I-V curve, of the proposed hybrid topology in relation to the real PV panel. The results using equation (3.17) are shown in Fig. 6.13, with Fig. 6.13 (a) showing the absolute error at $I_{sc} = 0.35$A and Fig. 6.13 (b) depicting the absolute error at $I_{sc} = 0.65$A. In both cases, the proposed solution shows a variation of less than 0.15% for a large part of the characteristic curve. In addition, the figure reveals that in the worst-case scenario, the deviation reaches 0.25% and 0.4% when the I_{sc} is equal to 0.35A and 0.65A, respectively.

6.4.5 MPPT Test Using a Boost DC/DC Converter

In this section, the MPPT test has been conducted to test and evaluate the proposed PVE at different irradiation levels. Figs. 6.14 (a) and (c) present the I-V curve drawing when the duty cycle of the boost DC/DC converter (D_{boost}) is changed from 5% to 95%. The MPP under two various irradiation levels has been shown in Fig. 6.14 using the MPPT method (P&O), and the proposed emulator performs identically to the real PV system. Figs. 6.14 (b) and (d) reveal that the PVE has two MPPs. The voltage and current at the first MPP equals 17.45V and 0.572A, respectively, while the voltage and current at the second MPP equals 17.2V and 0.305A, respectively. Moreover, from the figure, it is clear that the proposed PVE performance is not affected by the MPPT system used. In addition, the tracking system can track the MPPs at the same irradiation levels, and the tracked current and voltage match up with the one in Figs. 6.11 and 6.12.

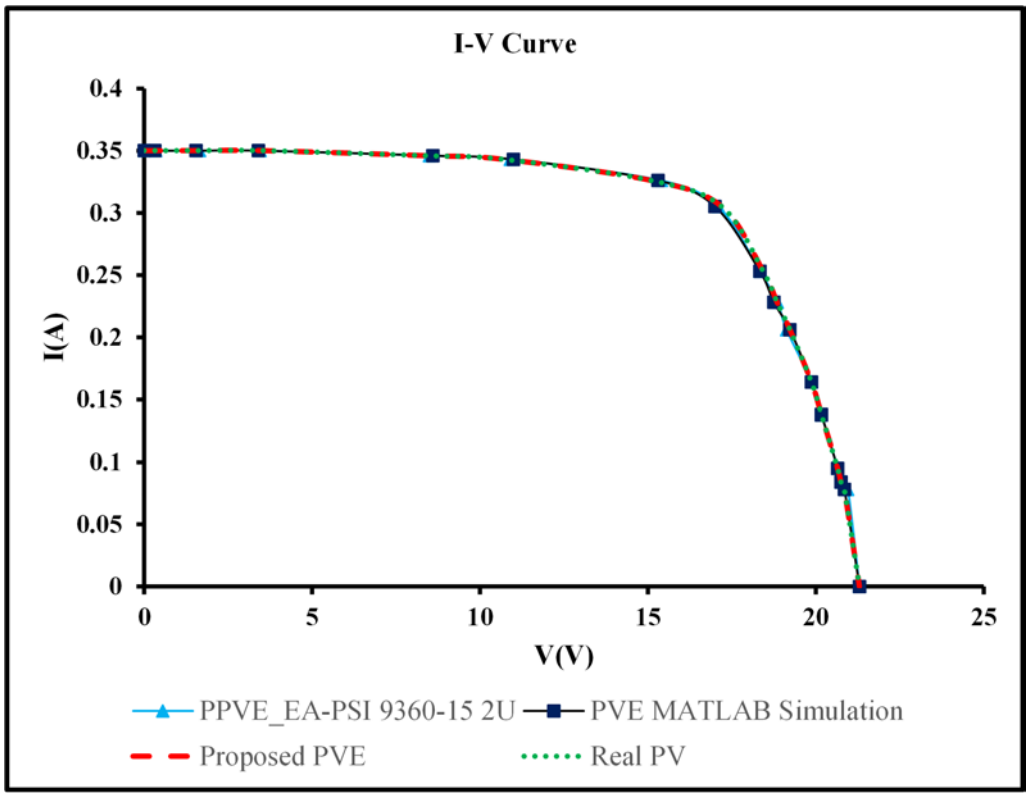


(a)

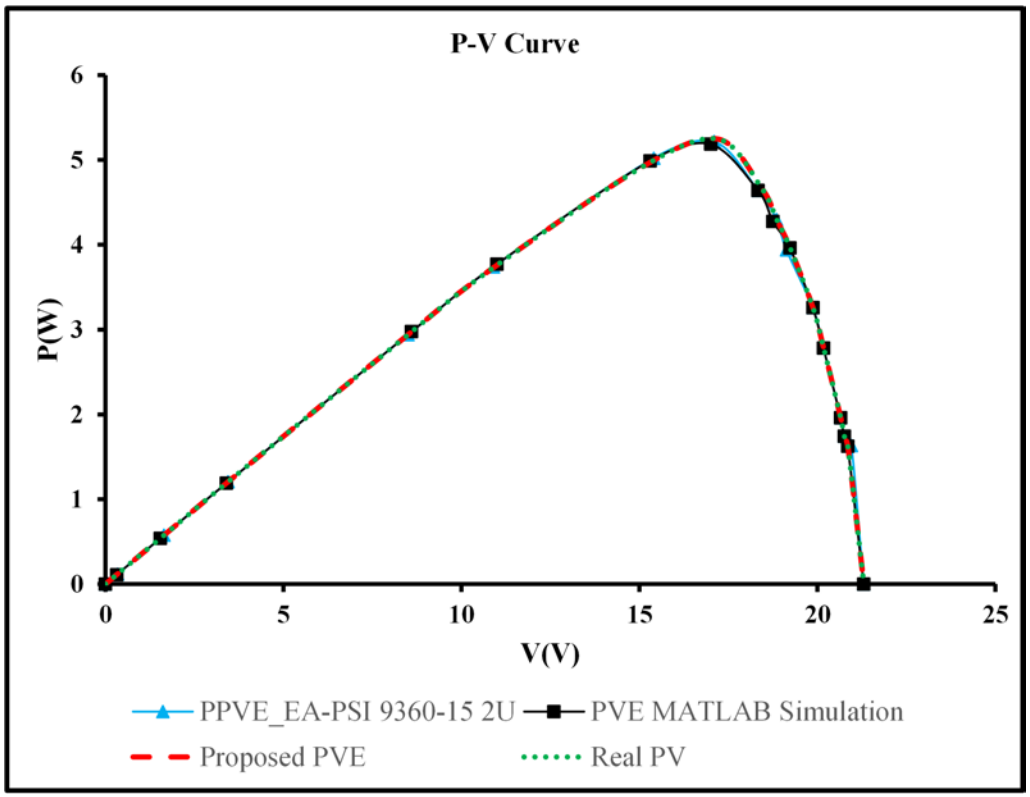


(b)

Figure 6.11: The comparison of the characteristic curves of the real PV panel, proposed PVE and PPVE at I_{sc}= 0.65A and V_{oc}= 21.5V: (a) I-V curve and (b) P-V curve.

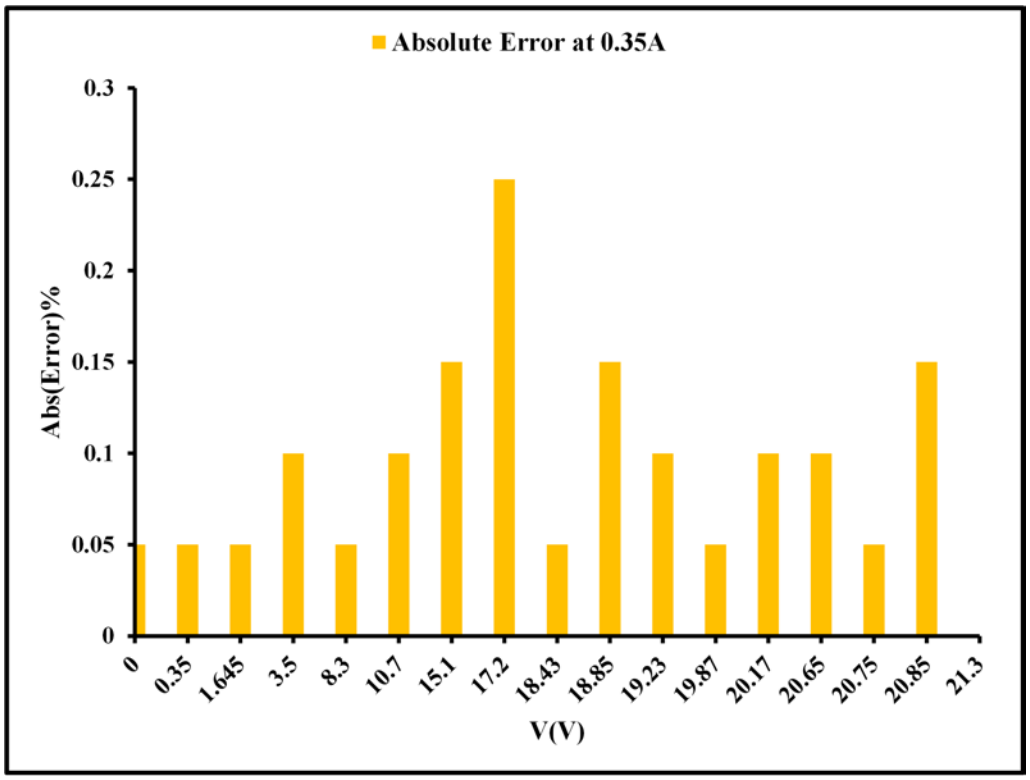


(a)

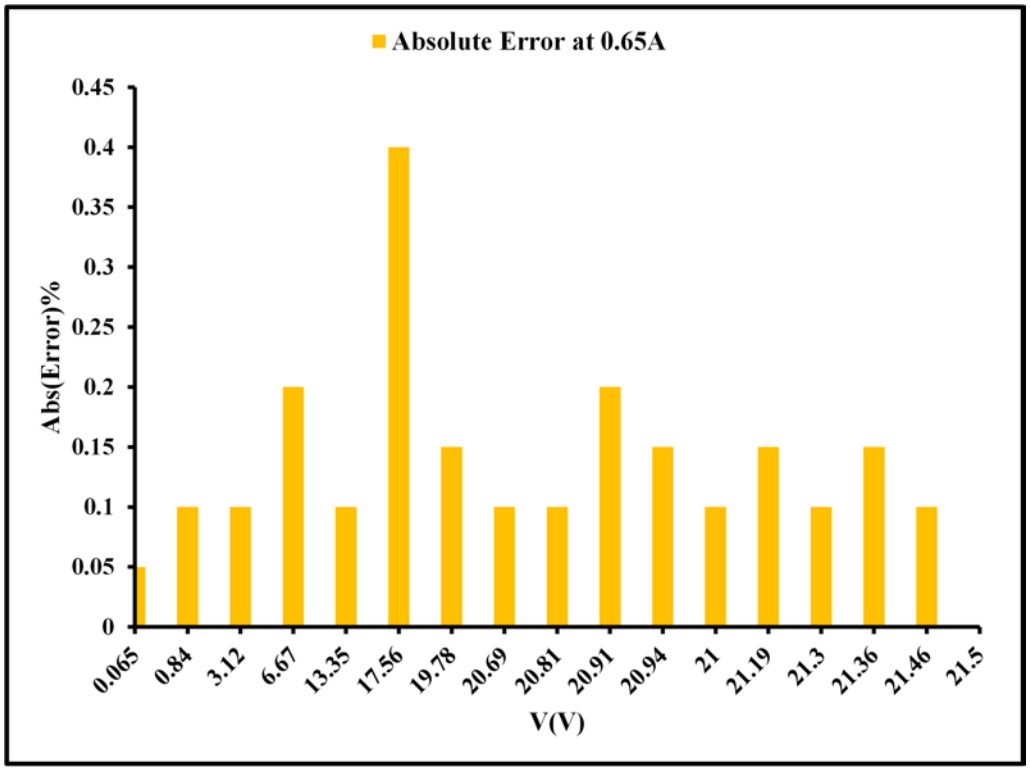


(b)

Figure 6.12: The comparison of the characteristic curves of the actual PV panel, proposed PVE, and PPVE at I_{sc}= 0.35A and V_{oc}= 21.3V: (a) I-V curve and (b) P-V curve.



(a)



(b)

Figure 6.13: The maximum absolute deviation between the real PV panel I–V characteristic curve and the one generated by the PVE based on the diode string: (a) at $I_{sc} = 0.35$A and (b) at $I_{sc} = 0.65$A.

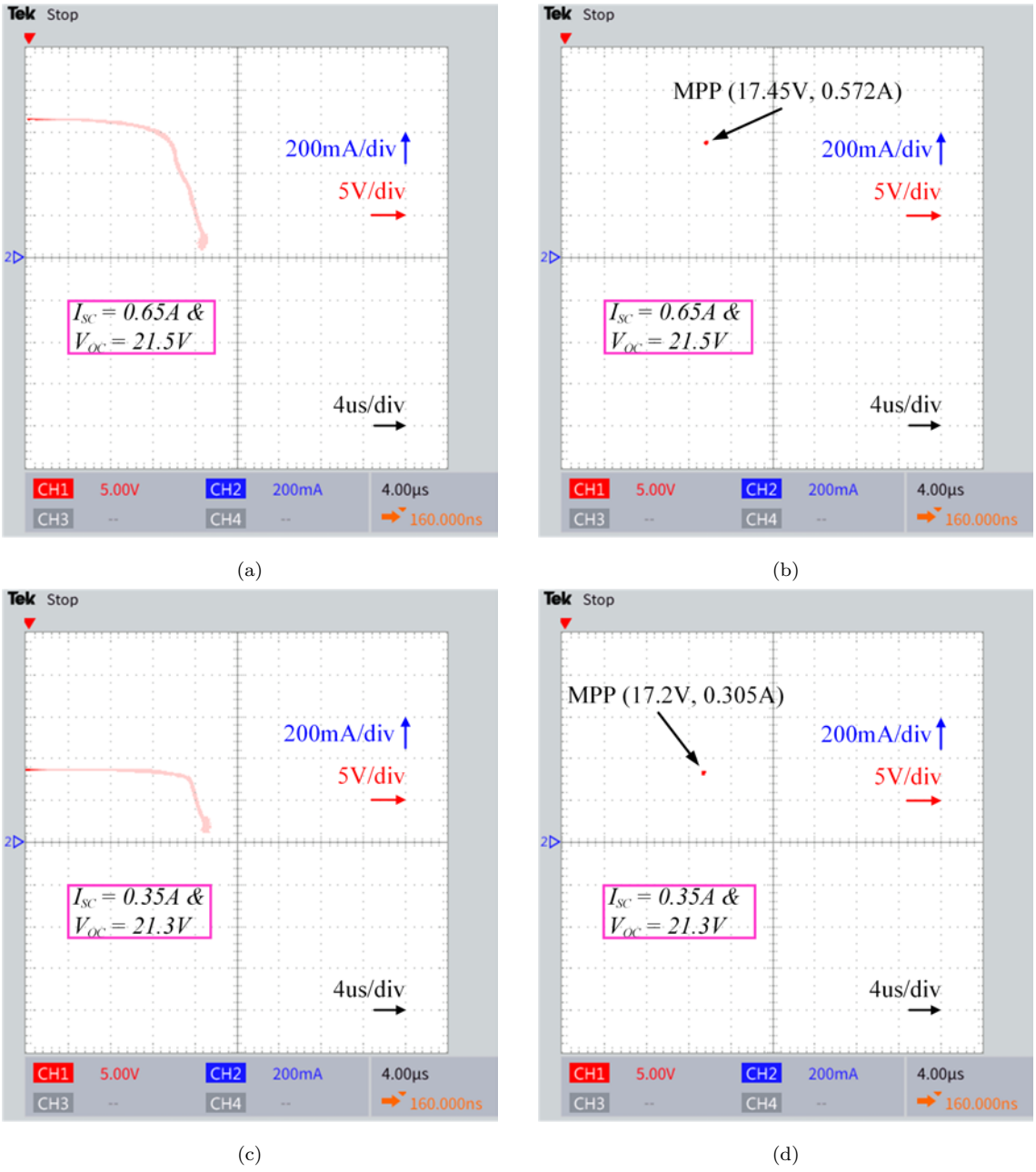


Figure 6.14: Experimental results showing the I-V curve drawing based on the MPPT (boost DC/DC converter), when the I_{sc} equals: (a) 0.65A ($990W/m^2$) and (b) 0.35A ($540W/m^2$), respectively.

6.4.6 Efficiency and Thermal Behaviour

Fig. 6.15 shows a comparison between the PV emulator based only on the transistor string and the modified PVE in terms of efficiency and temperature. According to Fig. 6.15, the temperature of the PVE created with only the transistor string rises from 29.4°C to 90.9°C, indicating an immediate increase in the power loss, as seen in Fig. 6.8. When using the enhanced structure, the operating temperature only increases from 27.4°C to 34.5°C on the transistor string in Mode-I, and from 23.1°C to 26.3°C in Mode-II, in which the NIBB DC/DC converter begins to operate. While this process occurs, the transistor string is turned off, allowing it to cool down until it reaches room temperature once again. It can also be seen from the figure that the power efficiency of the PVE built using only the transistor string decreases from 99.1% to 4.8% when the output load is set to 10Ω, and 270Ω, respectively. Furthermore, the modified PVE presents significant improvement in the overall system efficiency, which varies from 99.1% to 88.3% when using the same experimental setup. The power efficiency is calculated based on Equation (5.2).

6.4.7 Dynamic Response

The dynamic behaviour of the proposed PVE when the operating mode changes between Mode-I and Mode-II based on the output load variation is shown in Fig. 6.16. The V_{PV} equals 13.23V and 18.65V when the load is 20Ω and 47Ω, respectively. In Mode-I, only the transistor string is active, as shown in Fig. 6.16, and it is clear that the proposed PVE works in Mode-I, in which S_1 and S_2 are ON and S_3, S_4 and S_5 are OFF. In Mode-II, in which the NIBB DC/DC converter is operating, the figure shows that the NIBB converter operates when S_3 and S_4 are switching, S_5 is ON, and S_1 and S_2 are OFF. Fig. 6.16 also reveals that the proposed emulator can switch between the modes smoothly, with the output power equaling 8.31W (at 13.23V & 0.628A) in Mode-I and 7.22W (at 18.65V & 0.387A) in Mode-II in this study.

Fig. 6.17 shows the dynamic behaviour of the proposed PVE when the operating mode changes between Mode-I and Mode-II based on sudden load variation (more

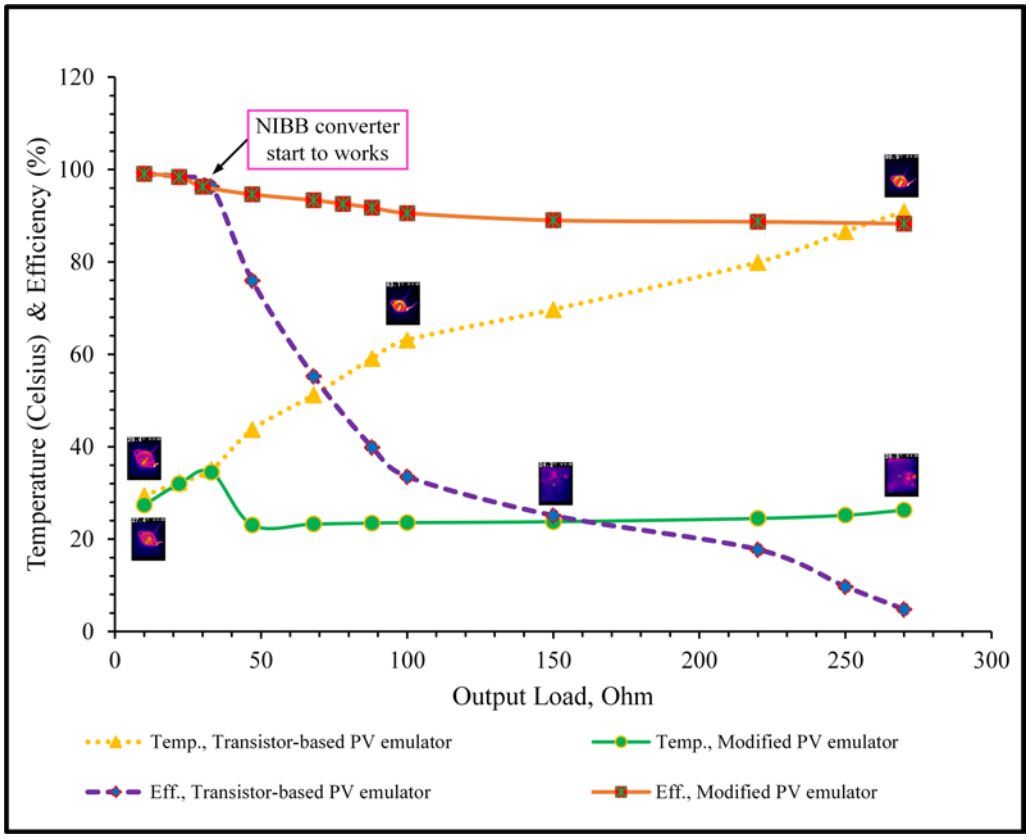


Figure 6.15: Thermal behaviour and efficiency of the transistor-based PVE compared with the modified PVE.

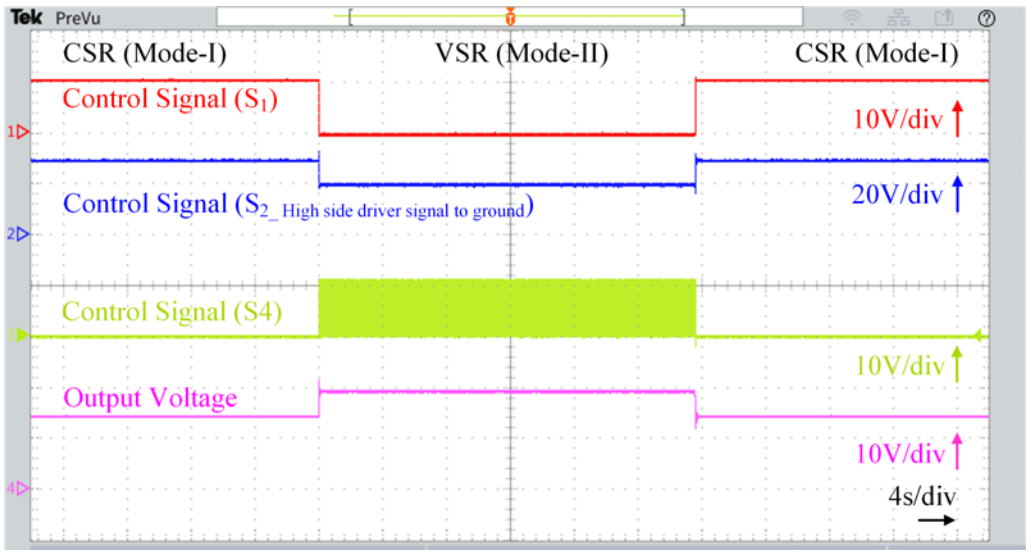


Figure 6.16: The gate control signals for S_1, S_2, and S_4, respectively, and output voltage of the proposed PVE when the operation mode is changed. Time base: 4s/div. Ch1 (red): 10V/div. Ch2 (blue): 20V/div. Ch3 (green): 10V/div. Ch4 (pink): 10V/div.

than 100mA in this example) in Mode-II. Based on the control strategy used, the proposed emulator works at 100ms in Mode-I. Then, the stability of the output current is rechecked, and the standard deviation is measured to test the stability of the output current readings. If the reading is stable, the output voltage (V_{PV}) determines the operation mode. The V_{PV} equals 20.22V, 19.54V, and 21.35V when the load is 100Ω, 50Ω, and 250Ω, respectively, as shown in Fig. 6.17. Notably, the proposed emulator can switch between the modes smoothly, with the output power equaling 4.35W (at 20.22V & 0.215A) in Mode-II and 7.66W (at 19.54V & 0.392A) in Mode-I and Mode-II when the load is set to 50Ω, then 1.82W (at 21.35V & 0.086A) in Mode-I in this example.

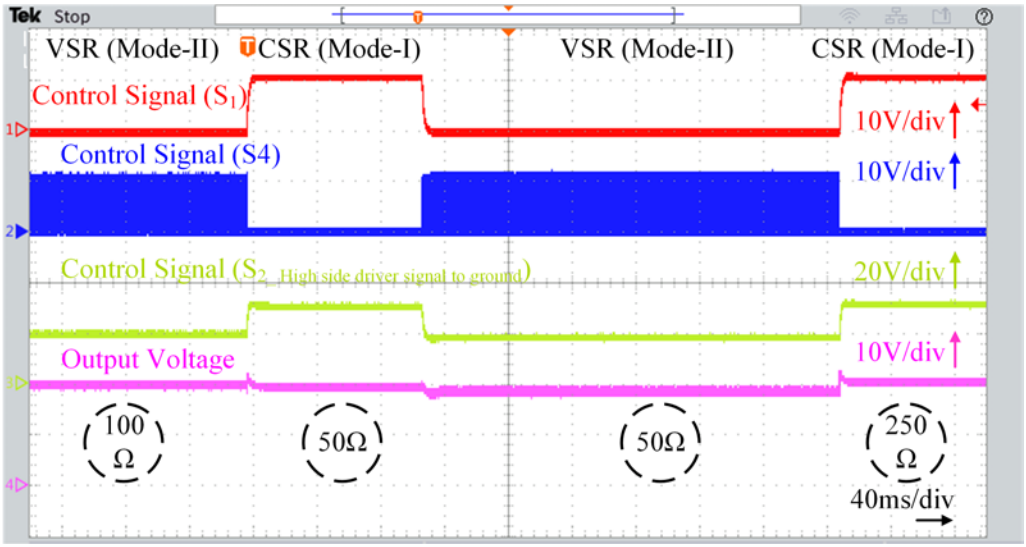


Figure 6.17: The gate control signals for S_1, S_4, and S_2, respectively, and the output voltage of the proposed PVE when the operation mode is changed based on sudden load changes in Mode-II. Time base: 40ms/div. Ch1 (red): 10V/div. Ch2 (blue): 10V/div. Ch3 (green): 20V/div. Ch4 (pink): 10V/div.

The dynamic response of the actual PV panel compared with the PVE based on the diode string, the transistor-based PVE, and the PPVE is shown in Fig. 6.18, where the I_{PV} changes from 0.185A to 0.385A based on the programmable electronic load (model: BK8500). The dynamic response of the PVE based on the diode string lags by 3ms compared with the actual PV panel, as shown in Fig. 6.18 (a). In addition,

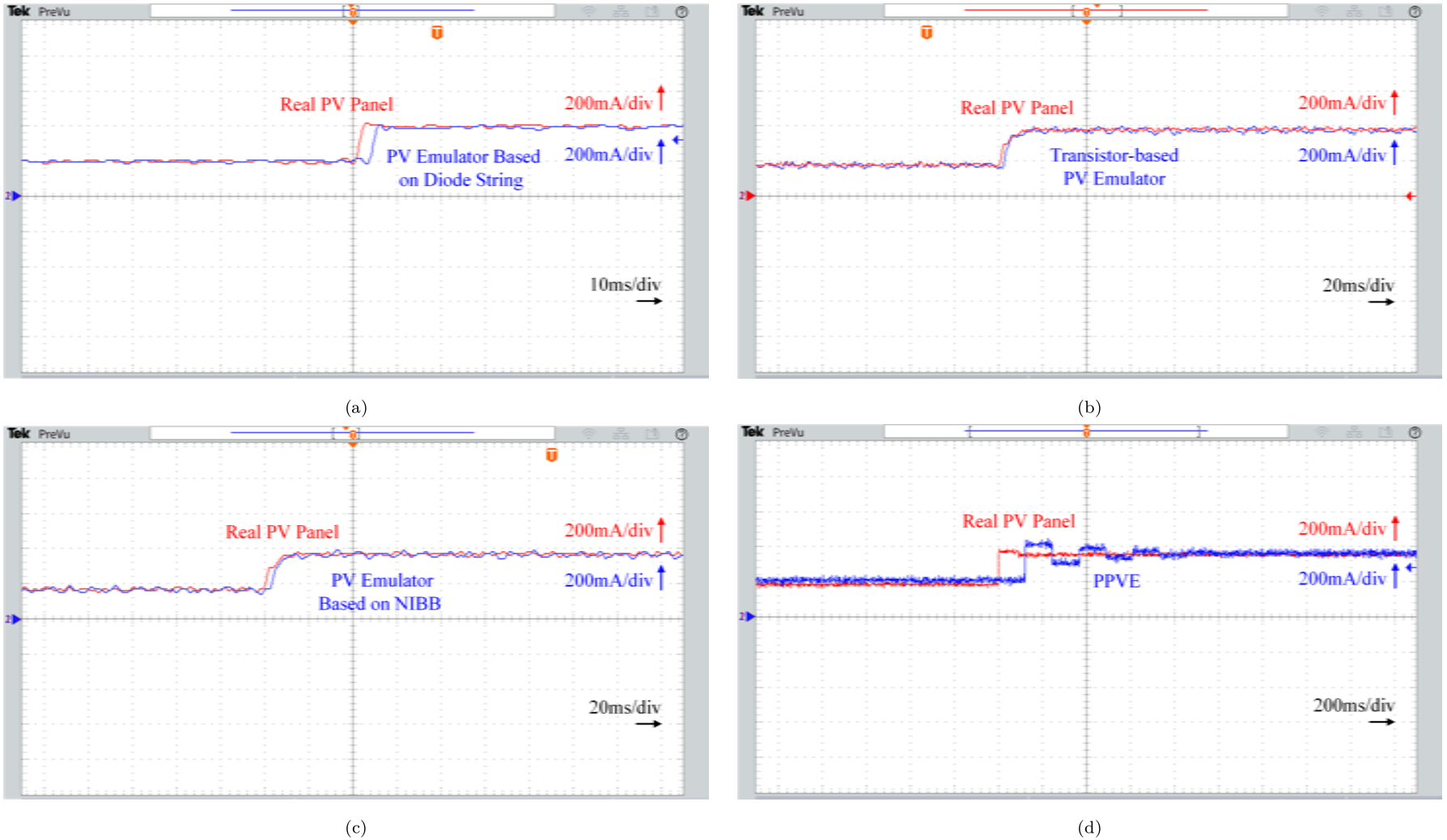


Figure 6.18: The dynamic PV characteristics when I_{PV} is converted from 0.185A to 0.385A based on load variation: (a) Real PV panel compared with the PVE based on the diode string, (b) Real PV panel compared with the transistor-based PVE, (c) Real PV panel compared with the PVE based on the NIBB converter, and (d) Real PV panel compared with the PPVE. Time base (a): 10ms/div. Time base (b & c): 20ms/div. Time base (d): 200ms/div and I_{PV}: 200mA/div.

Fig. 6.18 (b) reveals that the dynamic response of the transistor-based PV emulator lags by 1.8ms compared with the real PV panel. Fig. 6.18 (c) shows that the dynamic response of the PVE based on the NIBB converter lags 3.5ms behind the real PV panel. Nevertheless, the PPVE lags by 120ms compared with the real PV panel, as shown in Fig. 6.18 (d). In summary, the modified PVE is convenient and effective, as its dynamic behaviour is acceptable when compared with both the actual PV panel and the PPVE. The dynamic behaviour of the transistor-based PVE is also compared with some of the existing PVE solutions, as presented in Table 6.2. The table indicates that the proposed emulator shows the best response time compared with the existing solutions.

Table 6.2: Comparison of the different aspects of the existing platforms with the proposed PVE

No.	Author\s (Ref.)	Converter used	Control complexity	Cost	Dynamic response (ms)	Efficiency at MPP (%)
1	Cirrincione et al. [126]	Buck	Complex	Moderate	160	≤ 93.5
2	EA-PSI 9360-15 2U [127]	SMPSU	Complex	High	120	≤ 93
3	Ayop and Tan [23]	Buck	Complex	Moderate	21.25	93
4	Remache et al. [9]	Boost	Complex	High	18	≈ 90
5	Proposed PVE	Diode String	Not needed	Low	3	94.25
6	Proposed PVE	Transistor String	Not needed	Low	1.8	96.1

6.5 Summary

The PVE is based on a physically equivalent PV-cell model that has a high power loss, with the highest value occurring at OCV operating conditions. This chapter proposes two solutions to enhance the total system efficiency and improve the thermal response of the proposed emulator. The first one is based on a variable speed electric fan. Although this solution reduces the maximum temperature, the efficiency is still low. The second solution was developed to enhance the thermal behaviour and to increase the total system efficiency. Hence, it uses a hybrid-based PVE based on an SC method in parallel with the transistor-based emulator. The SC be constructed with a two-switch non-inverting buck-boost DC/DC converter and additional switches. Experimental results show the benefits and effectiveness of the enhanced PVE from both the thermal and electrical perspectives, as it can

mimic a real PV system with an accuracy comparable to an actual PV system and a PPVE under different operating conditions.

However, the main disadvantage of the transistor-based PVE is the increase in transistor temperature, particularly during the OCV scenario (i.e., the maximum power dissipation), where the transistor string temperature rises from 29.4°C to 93.5°C when no cooling method is used, from the short-circuit to the OCV condition. In addition, the power efficiency drops from 99.1% to 4.8%. By utilizing the suggested architecture for the hybrid-based PVE, the temperature in Mode-II when the SC is engaged increases from 23.1°C to 26.3°C, and the power efficiency of the whole module improves, reaching 88.3% at the OCV operation condition. The improved PVE exhibits an improvement of 118.2ms compared to the PPVE. A control strategy was implemented to handle the tradeoff between the thermal and dynamic performances in Mode-II of the proposed hybrid solution. In addition, one of the common MPPT approaches (P&O) was used to test the suggested PVE, and the results closely aligned to the results when the actual PV system is used.

Chapter 7

Conclusion and Future Work

7.1 Conclusions and Contribution

This thesis focuses on the development of a PVE based on the physical single-diode PV model to enhance system performance, and four different contributions are proposed, designed, and validated by the experimental results under different operating conditions. These include the following:

1. A simple and fast dynamic photovoltaic emulator based on a physically equivalent PV-cell model;
2. A design for a constant current source converter (CCSC) for PVE applications;
3. An efficiency improvement scheme for the PVE based on a physically equivalent PV-cell model;
4. A power loss reduction strategy for the PVE using the transistor-based PV model.

7.1.1 A Simple and Fast Dynamic Photovoltaic Emulator Based on a Physical Equivalent PV-cell Model

Existing solutions for PVEs usually require a sophisticated hardware design with a wide output range and fast computing. However, the controller bandwidth restricts the emulator response time, and it must stabilize the converter at many different operating points. Hence, pure power converter-based solutions generally have a slower response time than the real PV system. Chapter 3 presents a simple, reliable, and cost-effective circuit-based PVE based on the equivalent PV stacked cells. This study focuses on two aspects of the PVE design. Firstly, a detailed parametric design from model equations to the extraction of experimental PV parameters is explained to estimate the electrical performance of the PV simulator. Secondly, the electrothermal characteristics are studied and described. The proposed emulator has a high power loss. To enhance the emulator performance, a variable speed DC fan is used. However, it can be used for solar system testing and analysis, such as the MPPT and partial shading effect. The proposed PVE has a better dynamic response and shorter settling time than several benchmarked commercial products.

7.1.2 A Design for a Constant Current Source Converter (CCSC) for PVE Applications

The PVE based on a PV cell equivalent circuit model consists of a DC constant current source, a string of diodes, and two resistors. Chapter 4 proposes the second stage of the PVE design, focusing on the constant current source converter and controller designs for the PVE application. The CCSC simplifies the converter and controller designs. It operates at a constant point for each insolation level compared with a converter-based solution that needs a voltage source converter with wide output operating ranges. The response time of the proposed emulator system is comparable to both a benchmarked commercial product and a real PV system.

7.1.3 An Efficiency Improvement Scheme for the PVE Based on a Physically Equivalent PV-cell Model

The PVE based on a physical PV model has a high power loss around and at the OCV operating condition. Thus, there is a need for a new topology to enhance system performance, especially thermal behaviour, and minimize total power loss. Chapter 5 presents two new hybrid solutions, i.e., topologies A and B, that are based on a diode string and a switching circuit that is placed in parallel with the diode string to minimize the power loss. The switching circuit consists of a two-switch non-inverting buck-boost DC/DC converter. When the operating point of the PVE moves from the current source region to the voltage source region, the converter, which is more efficient, switches in to replace the diode string to seamlessly maintain the circuit operation of the emulator. Experimental results show that in the worst-case scenario, i.e., the OCV condition, the efficiency and temperature of the proposed solutions reach 81.47% and 30.1°C and 85.98% and 26.5°C for the first and second proposed hybrid solutions, respectively, as compared with 2.8% and 94.2°C for the emulator based only on the diode string. In terms of dynamic response, the proposed PVE lags 3.5ms and 3.2ms behind the actual PV panel for the first and second proposed hybrid solutions, respectively, compared with a commercial emulator's lag of 120ms under the 30% to 60% insolation change test.

7.1.4 A Power Loss Reduction Strategy for the PVE Using a Transistor-based PV Model

Chapter 6 proposes a transistor-based PVE, which reduces the number of required components. However, the transistor-based emulator faces the same heat problem as the diode-based solution. Hence, in Chapter 6, two solutions to improve system efficiency and enhance the thermal behaviour of the proposed emulator are proposed. The first solution is based on an ajustable speed DC electric fan. This solution minimizes the maximum heat temperature, however; the system efficiency remains low. The second solution enhances the thermal response and increases the overall efficiency. It uses a hybrid-based PVE that depends on a switching circuit method in parallel with the transistor string. The SC can be constructed with a two-switch non-inverting buck-boost DC/DC converter and additional switches. Experimental results show the benefits and effectiveness of the enhanced PVE from both thermal and electrical perspectives, and it can accurately emulate an actual PV panel and a PPVE under different operating conditions. The main drawback of the transistor-based PVE is the increase in the transistor temperature, particularly during the OCV operating condition (i.e., the maximum power dissipation), where the transistor string temperature increases from 29.4°C to 93.5°C when no cooling method is applied and the power efficiency decreases from 99.1% to 4.8%. When using the proposed hybrid-based PVE, the temperature during Mode-II, when the SC is engaged, increases from 23.1°C to 26.3°C, and the power efficiency improves, reaching 88.3% at the OCV operating condition. The enhanced PVE exhibits an improvement of 118.2ms compared to the PPVE.

7.2 Future Work

This thesis has covered the fundamental design, electrothermal issues and potential solutions for using a physically equivalent cell model to develop a PVE. Below are some suggestions for further developing the PVE:

1. Develop an adaptive PVE algorithm to mimic different types of PV panels by including the real-time control (digital) of the temperature and irradiation

effects. In addition, add a real-time control to alter the bias of the transistor-based PVE.

2. Extend the power capability of the proposed PVE by using a series or parallel connection to emulate PV arrays.
3. Study thermal coupling and electromagnetic interference in the proposed PVE.
4. Examine the proposed PVE system in different applications, such as the multi-port DC-DC converter and microgrid, to study its dynamics further.

Bibliography

[1] L. Ranalder, H. Busch, T. Hansen, M. Brommer, T. Couture, D. Gibb, F. Guerra, J. Nana, Y. Reddy, J. Sawin *et al.*, "Renewables in cities 2021 global status report," 2020.

[2] Y. Li, T. Lee, F. Z. Peng, and D. Liu, "A hybrid control strategy for photovoltaic simulator," in *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, Feb 2009, pp. 899–903.

[3] R. Ayop and C. W. Tan, "A comprehensive review on photovoltaic emulator," *Renewable and Sustainable Energy Reviews*, vol. 80, pp. 430–452, 2017.

[4] A. Koran, T. LaBella, and J. Lai, "High efficiency photovoltaic source simulator with fast response time for solar power conditioning systems evaluation," *IEEE Transactions on Power Electronics*, vol. 29, no. 3, pp. 1285–1297, March 2014.

[5] K. Nguyen-Duy, A. Knott, and M. A. E. Andersen, "High dynamic performance nonlinear source emulator," *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 2562–2574, March 2016.

[6] A. Koran, K. Sano, R.-Y. Kim, and J.-S. Lai, "Design of a photovoltaic simulator with a novel reference signal generator and two-stage lc output filter," *IEEE Transactions on Power Electronics*, vol. 25, no. 5, pp. 1331–1338, 2009.

[7] H. Nagayoshi, S. Orio, Y. Kono, and H. Nakajima, "Novel pv array/module iv curve simulator circuit," in *Conference Record of the Twenty-Ninth IEEE Photovoltaic Specialists Conference, 2002.* IEEE, 2002, pp. 1535–1538.

[8] I. Moussa, A. Khedher, and A. Bouallegue, "Design of a low-cost pv emulator applied for pvecs," *Electronics*, vol. 8, no. 2, p. 232, 2019.

[9] S. E. I. Remache, A. Y. Cherif, and K. Barra, "Optimal cascaded predictive control for photovoltaic systems: application based on predictive emulator," *IET Renewable Power Generation*, vol. 13, no. 15, pp. 2740–2751, 2019.

[10] J. P. Ram, T. S. Babu, T. Dragicevic, and N. Rajasekar, "A new hybrid bee pollinator flower pollination algorithm for solar pv parameter estimation," *Energy conversion and management*, vol. 135, pp. 463–476, 2017.

[11] A. F. Ebrahim, S. Ahmed, S. Elmasry, and O. A. Mohammed, "Implementation of a pv emulator using programmable dc power supply," in *SoutheastCon 2015*. IEEE, 2015, pp. 1–7.

[12] K.-H. Tang, K.-H. Chao, Y.-W. Chao, and J.-P. Chen, "Design and implementation of a simulator for photovoltaic modules," *International Journal of Photoenergy*, vol. 2012, 2012.

[13] F. Gómez-Castañeda, G. M. Tornez-Xavier, L. M. Flores-Nava, O. Arellano-Cárdenas, and J. A. Moreno-Cadenas, "Photovoltaic panel emulator in fpga technology using anfis approach," in *Electrical Engineering, Computing Science and Automatic Control (CCE), 2014 11th International Conference on*. IEEE, 2014, pp. 1–6.

[14] M. C. D. Piazza, M. Pucci, A. Ragusa, and G. Vitale, "Analytical versus neural real-time simulation of a photovoltaic generator based on a dc–dc converter," *IEEE Transactions on Industry Applications*, vol. 46, no. 6, pp. 2501–2510, Nov 2010.

[15] Z. Ziming, Z. Jianwen, S. Haimeng, W. Gang, H. Xiwen, and Z. Shi, "Research on photovolta array emulator system based on a novel zero-voltage zero-current switching converterer."

[16] M. T. Iqbal, M. Tariq, and M. S. U. Khan, "Fuzzy logic control of buck converter for photo voltaic emulator," in *2016 4th International Conference*

on the Development in the in Renewable Energy Technology (ICDRET), Jan 2016, pp. 1–6.

[17] Y. Kim, W. Lee, M. Pedram, and N. Chang, "Dual-mode power regulator for photovoltaic module emulation," *Applied energy*, vol. 101, pp. 730–739, 2013.

[18] J. Chavarría, D. Biel, F. Guinjoan, A. Poveda, F. Masana, and E. Alarcón, "Fpga-based design of a step-up photovoltaic array emulator for the test of pv grid-connected inverters," in *2014 IEEE 23rd International Symposium on Industrial Electronics (ISIE)*, June 2014, pp. 485–490.

[19] S. Jin, D. Zhang, and C. Wang, "Ui-ri hybrid lookup table method with high linearity and high-speed convergence performance for fpga-based space solar array simulator," *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 7178–7192, 2017.

[20] L. Callegaro, M. Ciobotaru, D. J. Pagano, E. Turano, and J. E. Fletcher, "A simple smooth transition technique for the noninverting buck–boost converter," *IEEE Transactions on Power Electronics*, vol. 33, no. 6, pp. 4906–4915, 2017.

[21] S. Vavilapalli, U. Subramaniam, S. Padmanaban, and F. Blaabjerg, "Design and controller-in-loop simulations of a low cost two-stage pv-simulator," *Energies*, vol. 11, no. 10, p. 2774, 2018.

[22] M. Farahani, M. A. Shamsi-nejad, and H. R. Najafi, "Design and construction of a digital solar array simulator with fast dynamics and high performance," *Solar Energy*, vol. 196, pp. 319–326, 2020.

[23] R. Ayop and C. W. Tan, "Rapid prototyping of photovoltaic emulator using buck converter based on fast convergence resistance feedback method," *IEEE Transactions on Power Electronics*, vol. 34, no. 9, pp. 8715–8723, 2019.

[24] R. Ayop, C. W. Tan, and A. L. Bukar, "Simple and fast computation photovoltaic emulator using shift controller," *IET Renewable Power Generation*, vol. 14, no. 11, pp. 2017–2026, 2020.

[25] I. Moussa and A. Khedher, "Photovoltaic emulator based on pv simulator rt implementation using xsg tools for an fpga control: Theory and experimentation," *International Transactions on Electrical Energy Systems*, vol. 29, no. 8, p. e12024, 2019.

[26] E. Beser, "Design and application of a photovoltaic array simulator with partial shading capability," *Journal of Power Electronics*, vol. 19, no. 5, pp. 1259–1269, 2019.

[27] O. Oussalem, M. Kourchi, A. Rachdy, M. Ajaamoum, H. Idadoub, and S. Jenkal, "A low cost controller of pv system based on arduino board and inc algorithm," *Materials Today: Proceedings*, vol. 24, pp. 104–109, 2020.

[28] A. N. Ali, K. Premkumar, M. Vishnupriya, B. Manikandan, and T. Thamizhselvan, "Design and development of realistic pv emulator adaptable to the maximum power point tracking algorithm and battery charging controller," *Solar Energy*, vol. 220, pp. 473–490, 2021.

[29] A. C. Atoche, J. V. Castillo, J. Ortegon-Aguilar, R. Carrasco-Alvarez, J. S. Gío, and A. Colli-Menchi, "A high-accuracy photovoltaic emulator system using arm processors," *Solar Energy*, vol. 120, pp. 389–398, 2015.

[30] H. A. Khawaldeh, M. Al-soeidat, M. Farhangi, D. D.-C. Lu, and L. Li, "Efficiency improvement scheme for pv emulator based on a physical equivalent pv-cell model," *IEEE Access*, 2021.

[31] A. Zegaoui, M. Aillerie, P. Petit, and J.-P. Charles, "Universal transistor-based hardware simulator for real time simulation of photovoltaic generators," *Solar Energy*, vol. 134, pp. 193 – 201, 2016. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0038092X16300950

[32] S. Jin, D. Zhang, Z. Bao, and X. Liu, "High dynamic performance solar array simulator based on a sic mosfet linear power stage," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1682–1695, 2017.

[33] B. K. Bose, "Power electronics, smart grid, and renewable energy systems," *Proceedings of the IEEE*, vol. 105, no. 11, pp. 2011–2018, 2017.

[34] H. Bizhani, R. Noroozian, S. Muyeen, K. Techato, and F. Blaabjerg, "A grid-connected smart extendable structure for hybrid integration of distributed generations," *Ieee Access*, vol. 7, pp. 105 235–105 246, 2019.

[35] G. P. Office, *International Energy Outlook 2016, with Projections To 2040*. Government Printing Office, 2016.

[36] T. Mai, W. Cole, E. Lantz, C. Marcy, and B. Sigrin, "Impacts of federal tax credit extensions on renewable deployment and power sector emissions," National Renewable Energy Lab.(NREL), Golden, CO (United States), Tech. Rep., 2016.

[37] S. Padmanaban, N. Priyadarshi, J. B. Holm-Nielsen, M. S. Bhaskar, F. Azam, A. K. Sharma, and E. Hossain, "A novel modified sine-cosine optimized mppt algorithm for grid integrated pv system under real operating conditions," *Ieee Access*, vol. 7, pp. 10 467–10 477, 2019.

[38] N. Priyadarshi, S. Padmanaban, J. B. Holm-Nielsen, F. Blaabjerg, and M. S. Bhaskar, "An experimental estimation of hybrid anfis–pso-based mppt for pv grid integration under fluctuating sun irradiance," *IEEE Systems Journal*, vol. 14, no. 1, pp. 1218–1229, 2019.

[39] W. N. Shafarman, S. Siebentritt, and L. Stolt, "Cu (inga) se2 solar cells," *Handbook of photovoltaic science and engineering*, vol. 2, pp. 546–599, 2011.

[40] H. A. Khawaldeh, M. Al-soeidat, D. D.-C. Lu, and L. Li, "Simple and fast dynamic photovoltaic emulator based on a physical equivalent pv-cell model," *The Journal of Engineering*, vol. 2021, no. 5, pp. 276–285, 2021. [Online]. Available: https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/tje2.12032

[41] N. Priyadarshi, S. Padmanaban, P. K. Maroti, and A. Sharma, "An extensive practical investigation of fpso-based mppt for grid integrated pv system under

variable operating conditions with anti-islanding protection," *IEEE Systems Journal*, vol. 13, no. 2, pp. 1861–1871, 2018.

[42] J. P. Ram, H. Manghani, D. S. Pillai, T. S. Babu, M. Miyatake, and N. Rajasekar, "Analysis on solar pv emulators: A review," *Renewable and Sustainable Energy Reviews*, vol. 81, pp. 149–160, 2018.

[43] A. K. Panchal, "A per-unit-single-diode-model parameter extraction algorithm: A high-quality solution without reduced-dimensions search," *Solar Energy*, vol. 207, pp. 1070 – 1077, 2020. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0038092X20307830

[44] H. A. Khawaldeh, H. Aljarajreh, M. Al-Soeidat, D. D.-C. Lu, and L. Li, "Performance investigation of a pv emulator using current source and diode string," in *2018 26th International Conference on Systems Engineering (ICSEng)*. IEEE, 2018, pp. 1–5.

[45] S. Pindado, E. Roibas-Millan, J. Cubas, J. M. Alvarez, D. Alfonso-Corcuera, and A. M. Gomez-San-Juan, "On the performance of solar cells/panels and li-ion batteries: simplified models developed at the idr/upm institute," *IEEE Transactions on Industry Applications*, 2021.

[46] A. D. Dhass, R. Senthil Kumar, P. Lakshmi, E. Natarajan, and A. Arivarasan, "An investigation on performance analysis of different pv materials," *Materials Today: Proceedings*, vol. 22, pp. 330–334, 2020, international Conference on Materials Engineering and Characterization 2019. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S2214785319312283

[47] M. Farangi, E. A. Soleimani, M. Zahedifar, O. Amiri, and J. Poursafar, "The environmental and economic analysis of grid-connected photovoltaic power systems with silicon solar panels, in accord with the new energy policy in iran," *Energy*, vol. 202, p. 117771, 2020.

[48] A. P. Gonzalo, A. P. Marugán, and F. P. G. Márquez, "Survey of maintenance

management for photovoltaic power systems," *Renewable and Sustainable Energy Reviews*, vol. 134, p. 110347, 2020.

[49] R. Khezri and A. Mahmoudi, "Review on the state-of-the-art multi-objective optimisation of hybrid standalone/grid-connected energy systems," *IET Generation, Transmission & Distribution*, vol. 14, no. 20, pp. 4285–4300, 2020.

[50] Z. Bektas, M. O. Kayalıca, and G. Kayakutlu, "A hybrid heuristic algorithm for optimal energy scheduling of grid-connected micro grids," *Energy Systems*, pp. 1–17, 2020.

[51] H. A. Kazem, M. T. Chaichan, A. H. Al-Waeli, and K. Sopian, "Evaluation of aging and performance of grid-connected photovoltaic system northern oman: Seven years' experimental study," *Solar Energy*, vol. 207, pp. 1247–1258, 2020.

[52] M. Ünlü and S. Çamur, "A simple photovoltaic simulator based on a one-diode equivalent circuit model," in *2017 4th International Conference on Electrical and Electronic Engineering (ICEEE)*. IEEE, 2017, pp. 33–36.

[53] M. Balato, L. Costanzo, D. Gallo, C. Landi, M. Luiso, and M. Vitelli, "Design and implementation of a dynamic fpaa based photovoltaic emulator," *Solar Energy*, vol. 123, pp. 102–115, 2016.

[54] M. Abd Elaziz and D. Oliva, "Parameter estimation of solar cells diode models by an improved opposition-based whale optimization algorithm," *Energy conversion and management*, vol. 171, pp. 1843–1859, 2018.

[55] M. H. Qais, H. M. Hasanien, S. Alghuwainem, and A. S. Nouh, "Coyote optimization algorithm for parameters extraction of three-diode photovoltaic models of photovoltaic modules," *Energy*, vol. 187, p. 116001, 2019.

[56] X. Gao, Y. Cui, J. Hu, N. Tahir, and G. Xu, "Performance comparison of exponential, lambert w function and special trans function based single diode solar cell models," *Energy Conversion and Management*, vol. 171, pp. 1822–1842, 2018.

[57] M. Merchaoui, A. Sakly, and M. F. Mimouni, "Particle swarm optimisation with adaptive mutation strategy for photovoltaic solar cell/module parameter extraction," *Energy Conversion and Management*, vol. 175, pp. 151–163, 2018.

[58] N. Muangkote, K. Sunat, S. Chiewchanwattana, and S. Kaiwinit, "An advanced onlooker-ranking-based adaptive differential evolution to extract the parameters of solar cell models," *Renewable Energy*, vol. 134, pp. 1129–1147, 2019.

[59] A. M. Beigi and A. Maroosi, "Parameter identification for solar cells and module using a hybrid firefly and pattern search algorithms," *Solar Energy*, vol. 171, pp. 435–446, 2018.

[60] W. De Soto, S. A. Klein, and W. A. Beckman, "Improvement and validation of a model for photovoltaic array performance," *Solar energy*, vol. 80, no. 1, pp. 78–88, 2006.

[61] H. A. Khawaldeh, M. Al-soeidat, D. Dah-Chuan Lu, and L. Li, "Fast photovoltaic emulator based on pv-cell equivalent circuit model," in *2021 IEEE 12th Energy Conversion Congress Exposition - Asia (ECCE-Asia)*, 2021, pp. 2121–2126.

[62] K. Khouzam and K. Hoffman, "Real-time simulation of photovoltaic modules," *Solar Energy*, vol. 56, no. 6, pp. 521–526, 1996.

[63] J. G. Durago, "Photovoltaic emulator adaptable to irradiance, temperature and panel specific iv curves," 2011.

[64] A. V. Rana and H. H. Patel, "Current controlled buck converter based photovoltaic emulator," *Journal of Industrial and Intelligent Information Vol*, vol. 1, no. 2, 2013.

[65] C. Balakishan and S. Babu, "Development of a microcontroller based pv emulator with current controlled dc/dc buck converter," *International Journal of Renewable Energy Research (IJRER)*, vol. 4, no. 4, pp. 1049–1055, 2014.

[66] M. C. Di Piazza and G. Vitale, *Photovoltaic sources: modeling and emulation*. Springer Science & Business Media, 2012.

[67] K. Ishaque, Z. Salam *et al.*, "A comprehensive matlab simulink pv system simulator with partial shading capability based on two-diode model," *Solar energy*, vol. 85, no. 9, pp. 2217–2227, 2011.

[68] L. Sandrolini, M. Artioli, and U. Reggiani, "Numerical method for the extraction of photovoltaic module double-diode model parameters through cluster analysis," *Applied Energy*, vol. 87, no. 2, pp. 442–451, 2010.

[69] N. A. Kamarzaman and C. W. Tan, "A comprehensive review of maximum power point tracking algorithms for photovoltaic systems," *Renewable and Sustainable Energy Reviews*, vol. 37, pp. 585–598, 2014.

[70] B. D. Patel and A. Rana, "A pole-placement approach for buck converter based pv array emulator," in *2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES)*, July 2016, pp. 1–5.

[71] D. Abbes, A. Martinez, G. Champenois, and B. Robyns, "Real time supervision for a hybrid renewable power system emulator," *Simulation Modelling Practice and Theory*, vol. 42, pp. 53 – 72, 2014. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1569190X13001755

[72] A. Vijayakumari, A. Devarajan, and N. Devarajan, "Design and development of a model-based hardware simulator for photovoltaic array," *International Journal of Electrical Power & Energy Systems*, vol. 43, no. 1, pp. 40–46, 2012.

[73] D. Ickilli, H. Can, and K. S. Parlak, "Development of a fpga-based photovoltaic panel emulator based on a dc/dc converter," in *2012 38th IEEE Photovoltaic Specialists Conference*, June 2012, pp. 001 417–001 421.

[74] D. D. Lu and Q. N. Nguyen, "A photovoltaic panel emulator using a buck-boost dc/dc converter and a low cost micro-controller," *Solar Energy*, vol. 86, no. 5, pp. 1477–1484, 2012.

[75] H. Abidi, A. B. B. Abdelghani, and D. Montesinos-Miracle, "Mppt algorithm and photovoltaic array emulator using dc/dc converters," in *Electrotechnical Conference (MELECON), 2012 16th IEEE Mediterranean.* IEEE, 2012, pp. 567–572.

[76] S. Gadelovits, M. Sitbon, and A. Kuperman, "Rapid prototyping of a low-cost solar array simulator using an off-the-shelf dc power supply," *IEEE Transactions on Power Electronics*, vol. 10, no. 29, pp. 5278–5284, 2014.

[77] C. Roncero-Clemente, E. Romero-Cadaval, V. Minambres, M. Guerrero-Martinez, and J. Gallardo-Lozano, "Pv array emulator for testing commercial pv inverters," *Elektronika ir Elektrotechnika*, vol. 19, no. 10, pp. 71–75, 2013.

[78] P. J. Binduhewa and M. Barnes, "Photovoltaic emulator," in *2013 IEEE 8th International Conference on Industrial and Information Systems*, Dec 2013, pp. 519–524.

[79] A. C. Nanakos and E. C. Tatakis, "Static and dynamic response of a photovoltaic characteristics simulator," in *2008 13th International Power Electronics and Motion Control Conference*, Sep. 2008, pp. 1827–1833.

[80] R. Ayop and C. W. Tan, "An adaptive controller for photovoltaic emulator using artificial neural network," 2017.

[81] T. D. Mai, S. De Breucker, K. Baert, and J. Driesen, "Reconfigurable emulator for photovoltaic modules under static partial shading conditions," *Solar Energy*, vol. 141, pp. 256–265, 2017.

[82] Ö. Özden, Y. Duru, S. Zengin, and M. Boztepe, "Design and implementation of programmable pv simulator," in *2016 International Symposium on Fundamentals of Electrical Engineering (ISFEE).* IEEE, 2016, pp. 1–5.

[83] J. Gonzalez-Llorente, A. Rambal-Vecino, L. A. Garcia-Rodriguez, J. C. Balda, and E. I. Ortiz-Rivera, "Simple and efficient low power photovoltaic emulator for evaluation of power conditioning systems," in *Applied Power Electronics Conference and Exposition (APEC), 2016 IEEE.* IEEE, 2016, pp. 3712–3716.

[84] R. Ayop and C. W. Tan, "Rapid prototyping of photovoltaic emulator using buck converter based on fast convergence resistance feedback method," *IEEE Transactions on Power Electronics*, vol. 34, no. 9, pp. 8715–8723, 2018.

[85] C.-C. Chen, H.-C. Chang, C.-C. Kuo, and C.-C. Lin, "Programmable energy source emulator for photovoltaic panels considering partial shadow effect," *Energy*, vol. 54, pp. 174 – 183, 2013. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0360544213000911

[86] K. Bhise, N. Pragallapati, S. Thale, and V. Agarwal, "Labview based emulation of photovoltaic array to study maximum power point tracking algorithms," in *2012 38th IEEE Photovoltaic Specialists Conference*, June 2012, pp. 002 961–002 966.

[87] Q. Zeng, P. Song, and L. Chang, "A photovoltaic simulator based on dc chopper," in *IEEE CCECE2002. Canadian Conference on Electrical and Computer Engineering. Conference Proceedings (Cat. No. 02CH37373)*, vol. 1. IEEE, 2002, pp. 257–261.

[88] A. Xenophontos, J. Rarey, A. Trombetta, and A. M. Bazzi, "A flexible low-cost photovoltaic solar panel emulation platform," in *2014 Power and Energy Conference at Illinois (PECI)*, Feb 2014, pp. 1–6.

[89] H. Nagayoshi, "I–v curve simulation by multi-module simulator using i–v magnifier circuit," *Solar energy materials and solar cells*, vol. 82, no. 1-2, pp. 159–167, 2004.

[90] S. Armstrong, C. K. Lee, and W. G. Hurley, "Investigation of the harmonic response of a photovoltaic system with a solar emulator," in *2005 European Conference on Power Electronics and Applications*, Sep. 2005, pp. 8 pp.–P.8.

[91] H. Nagayoshi, "Characterization of the module/array simulator using i-v magnifier circuit of a pn photo-sensor," in *3rd World Conference onPhotovoltaic Energy Conversion, 2003. Proceedings of*, vol. 2, May 2003, pp. 2023–2026 Vol.2.

[92] O. Midtgard, "A simple photovoltaic simulator for testing of power electronics," in *2007 European Conference on Power Electronics and Applications*, Sep. 2007, pp. 1–10.

[93] W. Peiyu, T. Boxue, Z. Housheng, and Z. Yanlei, "Research on maximum power point tracker based on solar cells simulator," in *2010 2nd International Conference on Advanced Computer Control*, vol. 1. IEEE, 2010, pp. 319–323.

[94] A. Mukerjee and N. Dasgupta, "Dc power supply used as photovoltaic simulator for testing mppt algorithms," *Renewable Energy*, vol. 32, no. 4, pp. 587 – 592, 2007. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0960148106000644

[95] Z. Zhou, P. Holland, and P. Igic, "Mppt algorithm test on a photovoltaic emulating system constructed by a dc power supply and an indoor solar panel," *Energy Conversion and Management*, vol. 85, pp. 460 – 469, 2014. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0196890414005317

[96] N. Belhaouas, M. A. Cheikh, A. Malek, and C. Larbes, "Matlab-simulink of photovoltaic system based on a two-diode model simulator with shaded solar cells," *Revue des Energies Renouvelables*, vol. 16, no. 1, pp. 65–73, 2013.

[97] R. Kadri, H. Andrei, J.-P. Gaubert, T. Ivanovici, G. Champenois, and P. Andrei, "Modeling of the photovoltaic cell circuit parameters for optimum connection model and real-time emulator with partial shadow conditions," *Energy*, vol. 42, no. 1, pp. 57 – 67, 2012, 8th World Energy System Conference, WESC 2010. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0360544211006773

[98] A. Algaddafi, N. Brown, R. Gammon, and S. A. Altuwayjiri, "Effect of pv array emulator on power quality of pv inverter compared to a real pv array," in *2015 3rd International Renewable and Sustainable Energy Conference (IRSEC)*, Dec 2015, pp. 1–6.

[99] A. M. Koran, "Photovoltaic source simulators for solar power conditioning systems: design optimization, modeling, and control," Ph.D. dissertation, Virginia Tech, 2013.

[100] R. González-Medina, I. Patrao, G. Garcerá, and E. Figueres, "A low-cost photovoltaic emulator for static and dynamic evaluation of photovoltaic power converters and facilities," *Progress in Photovoltaics: Research and Applications*, vol. 22, no. 2, pp. 227–241, 2014.

[101] Y. Erkaya, P. Moses, I. Flory, and S. Marsillac, "Steady-state performance optimization of a 500 khz photovoltaic module emulator," in *2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC)*, June 2016, pp. 3205–3208.

[102] W. Zhang and J. W. Kimball, "Dc–dc converter based photovoltaic simulator with a double current mode controller," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 5860–5868, July 2018.

[103] M. Alaoui, H. Maker, A. Mouhsen, and H. Hihi, "Photovoltaic emulator of different solar array configurations under partial shading conditions using damping injection controller," *International Journal of Power Electronics and Drive Systems*, vol. 11, no. 2, p. 1019, 2020.

[104] J. Zhang, S. Wang, Z. Wang, and L. Tian, "Design and realization of a digital pv simulator with a push-pull forward circuit," *Journal of Power Electronics*, vol. 14, no. 3, pp. 444–457, 2014.

[105] A. Soetedjo, Y. I. Nakhoda, A. Lomi, and G. E. Hendroyono, "Development of pv simulator by integrating software and hardware for laboratory testing," in *2015 International Conference on Automation, Cognitive Science, Optics, Micro Electro-Mechanical System, and Information Technology (ICACOMIT)*, Oct 2015, pp. 96–100.

[106] D. M. K. Schofield, M. P. Foster, and D. A. Stone, "Low-cost solar emulator for evaluation of maximum power point tracking methods," *Electronics Letters*, vol. 47, no. 3, pp. 208–209, February 2011.

[107] S. Jin and D. Zhang, "A simple control method of open-circuit voltage for the fpga-based solar array simulator," in *2016 IEEE International Conference on Power and Renewable Energy (ICPRE)*. IEEE, 2016, pp. 209–216.

[108] D. W. Hart, *Power electronics*. Tata McGraw-Hill Education, 2011.

[109] T. L. Floyd, *Electronic devices: electron flow version*. Pearson Prentice Hall, 2008.

[110] S. Thale, R. Wandhare, and V. Agarwal, "A novel low cost portable integrated solar pv, fuel cell and battery emulator with fast tracking algorithm," in *2014 IEEE 40th Photovoltaic Specialist Conference (PVSC)*, June 2014, pp. 3138–3143.

[111] L. M. Barrera, R. A. Osorio, and C. L. Trujillo, "Design and implementation of electronic equipment that emulates photovoltaic panels," in *2015 IEEE 42nd Photovoltaic Specialist Conference (PVSC)*, June 2015, pp. 1–5.

[112] A. Pressman, *Switching power supply design*. McGraw-Hill, Inc., 1997.

[113] M. Bendali, C. Larouci, T. Azib, C. Marchand, and G. Coquery, "Design methodology with optimization of an interleaved buck converter for automotive application," in *Eurocon 2013*, July 2013, pp. 1066–1072.

[114] G. Martin-Segura, J. Lopez-Mestre, M. Teixido-Casas, and A. Sudria-Andreu, "Development of a photovoltaic array emulator system based on a full-bridge structure," in *2007 9th International Conference on Electrical Power Quality and Utilisation*, Oct 2007, pp. 1–6.

[115] D. Heredero-Peris, M. Capó-Lliteras, C. Miguel-Espinar, T. Lledó-Ponsati, and D. Montesinos-Miracle, "Development and implementation of a dynamic pv emulator with hmi interface for high power inverters," in *2014 16th European Conference on Power Electronics and Applications*, Aug 2014, pp. 1–10.

[116] M. K. Kazimierczuk, *Pulse-width modulated DC-DC power converters*. John Wiley & Sons, 2015.

[117] N. Priyadarshi, A. K. Sharma, and F. Azam, "A hybrid firefly-asymmetrical fuzzy logic controller based mppt for pv-wind-fuel grid integration," *International Journal of Renewable Energy Research (IJRER)*, vol. 7, no. 4, pp. 1546–1560, 2017.

[118] R. Muhammad, "Power electronics devices, circuits and applications," 2014.

[119] S. J. Gift and B. Maundy, "Semiconductor diode," in *Electronic Circuit Design and Application*. Springer, 2021, pp. 1–40.

[120] N. Priyadarshi, S. Padmanaban, M. S. Bhaskar, F. Blaabjerg, and A. Sharma, "Fuzzy svpwm-based inverter control realisation of grid integrated photovoltaic-wind system with fuzzy particle swarm optimisation maximum power point tracking algorithm for a grid-connected pv/wind power generation system: hardware implementation," *IET Electric Power Applications*, vol. 12, no. 7, pp. 962–971, 2018.

[121] M. G. Villalva, J. R. Gazoli, and E. Ruppert Filho, "Modeling and circuit-based simulation of photovoltaic arrays," in *2009 Brazilian Power Electronics Conference*. IEEE, 2009, pp. 1244–1254.

[122] A. Laudani, F. R. Fulginei, and A. Salvini, "High performing extraction procedure for the one-diode model of a photovoltaic panel from experimental i–v curves by using reduced forms," *Solar Energy*, vol. 103, pp. 316–326, 2014.

[123] M. G. Villalva, J. R. Gazoli, and E. Ruppert Filho, "Comprehensive approach to modeling and simulation of photovoltaic arrays," *IEEE Transactions on power electronics*, vol. 24, no. 5, pp. 1198–1208, 2009.

[124] C. Carrero, J. Amador, and S. Arnaltes, "A single procedure for helping pv designers to select silicon pv modules and evaluate the loss resistances," *Renewable Energy*, vol. 32, no. 15, pp. 2579–2589, 2007.

[125] J. Cubas, S. Pindado, and M. Victoria, "On the analytical approach for modeling photovoltaic systems behavior," *Journal of power sources*, vol. 247, pp. 467–474, 2014.

[126] M. Cirrincione, M. C. Di Piazza, M. Pucci, and G. Vitale, "Real-time simulation of photovoltaic arrays by growing neural gas controlled dc-dc converter," in *2008 IEEE Power Electronics Specialists Conference*. IEEE, 2008, pp. 2004–2010.

[127] EA-Elektro-AutomatikGmbH, "Ea-psi 9360-15 2u," shorturl.at/hlCMN, may, 2015.

[128] Z. Dong, K. T. Chi, and S. R. Hui, "Circuit theoretic considerations of led driving: Voltage-source versus current-source driving," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4689–4702, 2018.

[129] T. N. Gücin, B. Fincan, and M. Biberoğlu, "A series resonant converter-based multichannel led driver with inherent current balancing and dimming capability," *IEEE Transactions on Power Electronics*, vol. 34, no. 3, pp. 2693–2703, 2018.

[130] A. Zu, Q. Luo, J. Huang, Q. He, P. Sun, and X. Du, "Analysis and design of a multi-channel constant current led driver based on dc current bus distributed power system structure," *IET Power Electronics*, vol. 13, no. 4, pp. 627–635, 2019.

[131] M. F. Menke, Á. R. Seidel, and R. V. Tambara, "Llc led driver small-signal modeling and digital control design for active ripple compensation," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 1, pp. 387–396, 2018.

[132] R. Wang and J. Zhang, "A simple current balancing method for multi-output flyback led driver," in *2015 IEEE 2nd International Future Energy Electronics Conference (IFEEC)*. IEEE, 2015, pp. 1–5.

[133] K. H. Yi, "High voltage, low current high-power multichannel leds llc driver by stacking single-ended rectifiers with balancing capacitors," *Electronics*, vol. 9, no. 3, p. 529, 2020.

[134] S. Li, Y. Guo, S.-C. Tan, and S. R. Hui, "An off-line single-inductor multiple-output led driver with high dimming precision and full dimming range," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4716–4727, 2016.

[135] Z. Dong, K. T. Chi, and S. R. Hui, "Current-source-mode single-inductor multiple-output led driver with single closed-loop control achieving independent dimming function," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 3, pp. 1198–1209, 2018.

[136] M. A. Al Hilmi, "Desain dan implementasi flyback dc-dc konverter 48-12 volt 100 watt untuk supply auxiliary kendaraan listrik," Ph.D. dissertation, Institut Teknologi Sepuluh Nopember, 2018.

[137] R. Kumar, C.-C. Wu, C.-Y. Liu, Y.-L. Hsiao, W.-H. Chieng, and E.-Y. Chang, "Discontinuous current mode modeling and zero current switching of flyback converter," *Energies*, vol. 14, no. 18, p. 5996, 2021.

[138] A. M. Kamath, K. Anjana, and M. Barai, "Design and implementation of voltage mode digital controller for flyback converter operating in discontinuous conduction mode (dcm)," in *2016 7th India International Conference on Power Electronics (IICPE)*. IEEE, 2016, pp. 1–6.

[139] R. Ayop, C. W. Tan, S. N. S. Nasir, K. Y. Lau, and C. L. Toh, "Buck converter design for photovoltaic emulator application," in *2020 IEEE International Conference on Power and Energy (PECon)*. IEEE, 2020, pp. 293–298.

[140] F. Barbieri, R. P. Chandrasena, F. Shahnia, S. Rajakaruna, and A. Ghosh, "Application notes and recommendations on using tms320f28335 digital signal processor to control voltage source converters," in *2014 Australasian Universities Power Engineering Conference (AUPEC)*. IEEE, 2014, pp. 1–7.

[141] T. Nguyen-Van, R. Abe, and K. Tanaka, "A digital hysteresis current control for half-bridge inverters with constrained switching frequency," *Energies*, vol. 10, no. 10, p. 1610, 2017.

[142] H. Yi, F. Zhuo, F. Wang, and Z. Wang, "A digital hysteresis current controller for three-level neural-point-clamped inverter with mixed-levels and prediction-based sampling," *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3945–3957, 2015.

[143] B. Chandrasekar, C. Nallaperumal, S. Padmanaban, M. S. Bhaskar, J. B. Holm-Nielsen, Z. Leonowicz, and S. O. Masebinu, "Non-isolated high-gain triple port dc–dc buck-boost converter with positive output voltage for photovoltaic applications," *IEEE Access*, vol. 8, pp. 113 649–113 666, 2020.

[144] M. Al-Soeidat, H. Aljarajreh, H. Khawaldeh, D. D.-C. Lu, and J. Zhu, "A reconfigurable three-port dc-dc converter for integrated pv-battery system," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2019.

[145] X. Yang, B. Sun, Z. Wang, C. Qian, Y. Ren, D. Yang, and Q. Feng, "An alternative lifetime model for white light emitting diodes under thermal–electrical stresses," *Materials*, vol. 11, no. 5, p. 817, 2018.

[146] H. Givi, E. Farjah, and T. Ghanbari, "A comprehensive monitoring system for online fault diagnosis and aging detection of non-isolated dc–dc converters' components," *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6858–6875, 2018.

[147] S. Singh *et al.*, "Selection of non-isolated dc-dc converters for solar photovoltaic system," *Renewable and Sustainable Energy Reviews*, vol. 76, pp. 1230–1247, 2017.

[148] S. Sivakumar, M. J. Sathik, P. Manoj, and G. Sundararajan, "An assessment on performance of dc–dc converters for renewable energy applications," *Renewable and Sustainable Energy Reviews*, vol. 58, pp. 1475–1485, 2016.

[149] L. Jotham Jeremy, C. A. Ooi, and J. Teh, "Non-isolated conventional dc-dc converter comparison for a photovoltaic system: A review," *Journal of Renewable and Sustainable Energy*, vol. 12, no. 1, p. 013502, 2020.

[150] D.-H. Kim and B.-K. Lee, "An enhanced control algorithm for improving the light-load efficiency of noninverting synchronous buck–boost converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3395–3399, 2015.

[151] T. Instruments, "Tms320f2837xd dual-core delfino microcontrollers," *Data Manual, Texas Instruments Inc*, 2018.

[152] L. R. Merchan-Villalba, J. M. Lozano-Garcia, J. G. Avina-Cervantes, H. J. Estrada-Garcia, and J. Martinez-Patiño, "Matrix converter based on svd modulation using a microcontroller as unique controlling device," *IEEE Access*, vol. 7, pp. 164 815–164 824, 2019.

[153] L. Shen, F. Yang, X. Wang, and P. Comerford, "Functional curve fitting algorithm via multi-heterogeneous data curve," *IEEE Access*, vol. 5, pp. 470–479, 2017.

[154] J. Ren, "Digital predistorter for short-wave power amplifier with improving index accuracy of lookup table based on fpga," *IEEE Access*, vol. 7, pp. 182 881–182 885, 2019.

[155] J. Sa, H. Gu, Y. An, Y. Luo, and Z. Zhang, "Study on curved surface fitting of countersink based on point cloud," *IEEE Access*, vol. 8, pp. 106 464–106 470, 2020.

[156] M. Al-Soeidat, H. Khawaldeh, D. D.-C. Lu, and J. Zhu, "A novel high step-up three-port bidirectional dc/dc converter for pv-battery integrated system," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 3352–3357.

[157] E. Manuel Godinho Rodrigues, R. Godina, M. Marzband, and E. Pouresmaeil, "Simulation and comparison of mathematical models of pv cells with growing levels of complexity," *Energies*, vol. 11, no. 11, p. 2902, 2018.

[158] R. Semiconductor, "Efficiency of buck converter," *Appl. Note*, 2016.

[159] M. V. Morelli, "Modelling, design and control of a dc-dc converter for automotive thermoelectric generator," Ph.D. dissertation, Politecnico di Torino, 2018.

[160] L. An and D. D.-C. Lu, "Power loss analysis of a single-switch non-isolated dc/dc converter," in *2015 IEEE 11th International Conference on Power Electronics and Drive Systems*. IEEE, 2015, pp. 592–597.

[161] F. Saint-Eve, J.-P. Sawicki, P. Petit, F. Maufay, and M. Aillerie, "Comparison between two photovoltaic module models based on transistors," in *AIP Conference Proceedings*, vol. 1968, no. 1. AIP Publishing LLC, 2018, p. 030082.

Appendices

Appendix A

Power loss modelling and analysis of the proposed PVEs

The power loss modelling, analysis and simulation of the proposed PVEs using the LTspice program is shown in this Appendix.

A.1 The PV Emulator based on the Diode String

The mathematical power loss equation of the PV emulator based on the physical PV-cell model is written in (A.1). Furthermore, the total power loss of the PV emulator using the diode string is determined based on Equation (A.2) [44, 157]. The LTspice program is used to mimic the PV panel's I-V and P-V curves using the proposed diode string PV emulator. In addition, it is used to calculate the power losses at different power levels, as shown in Fig. A.1.

$$P_{D,Loss} = I_D \times V_D \tag{A.1}$$

where the I_D is the diode forward current (A), and V_D is the diode forward voltage (V).

$$P_{DS,Loss} = N \times I_D \times V_D \tag{A.2}$$

where the I_D is the diode forward current (A), V_D is the diode forward voltage (V), and N is the number of series-connected power diodes.

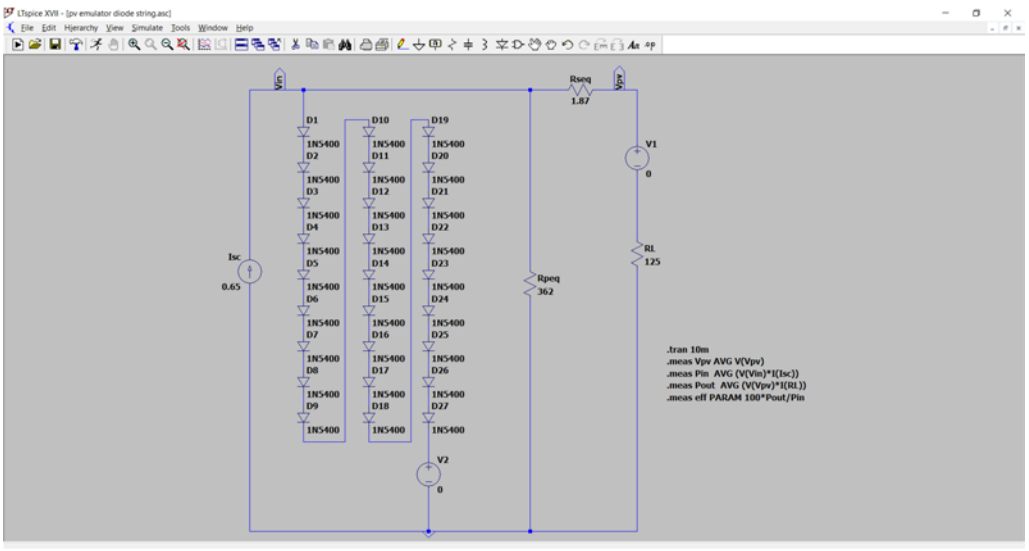


Figure A.1: The LTspice simulation file of the PVE is based on a diode string.

A.2 The Converter-based PV Emulator

This section deals with a number of calculations that can be used to get a general idea of the NIBB DC-DC converter's power dissipation and, thus, its efficiency. This converter can be worked into three different modes based on the control strategies, namely buck, boost, and buck-boost mode, of which this study depends on the buck-boost mode. The major losses, i.e., the conduction and switching losses, are calculated for each component. Using the converter-based PV emulator, the LTspice program is used to emulate the PV panel's characteristic curves. It also calculates power losses at different power levels, as shown in Fig. A.2.

1. Inductor

   Two types of power losses characterize the component: conduction loss and magnetic core loss. In this work, only conduction loss is considered, and it is determined by the equivalent resistance of the inductor (ESR) caused by the inductor's windings. The inductance has a direct relationship with

the ESR value. The inductor power loss is unaffected by the duty cycle. It means that the higher the inductor's average current, the higher the power dissipation [158–160].

$$P_L = (I_{in}^2 + \frac{\Delta I_L^2}{12}) \times R_L + (I_o^2 + \frac{\Delta I_L^2}{12}) \times R_L \tag{A.3}$$

where I_{in} is the input current, I_o is the output current and it equals to I_{PV} in this case, ΔI_L is the maximum current ripple in the inductor, and R_L is the equivalent resistance of the inductor (ESR).

2. Capacitors (C_{in} & C_o)

   Equations (A.4) and (A.5) define the general power dissipation model used for the input and output capacitors [158, 159].

$$P_{C_{in}} = I_{C_{in},rms}^2 \times R_{C_{in}} \tag{A.4}$$

where $I_{C_{in},rms}$ is the RMS current of capacitor C_{in}, and $R_{C_{in}}$ is the equivalent series resistance of capacitor C_{in}.

$$P_{C_o} = I_{C_o,rms}^2 \times R_{C_o} \tag{A.5}$$

where $I_{C_o,rms}$ is the RMS current of capacitor C_o, and R_{C_o} is the equivalent series resistance of capacitor C_o.

3. Diodes (D_a & D_b)

   For the sake of simplicity, only the forward voltage is considered during the power loss analysis for diodes. The power loss of the diode D_a is calculated in (A.6), and the loss of the diode D_b is found by (A.7) [158–160].

$$P_{D_a} = I_{D_a} \times V_{D_a} \tag{A.6}$$

where I_{D_a} is the average current of the diode D_a, and V_{D_a} is the forward voltage of the diode D_a .

$$P_{D_b} = I_{D_b} \times V_{D_b} \tag{A.7}$$

where I_{D_b} is the average current of the diode D_b, and V_{D_b} is the forward voltage of the diode D_b .

4. Switches (S_2 & S_3)

Switch losses are the essential dissipations, and they are primarily dependent on the duty cycle (D) and thus on the different DC-DC converter operation modes. The conduction ($D = 1$) and switching ($D =$ variable) conditions cause the most dissipation [158–160].

(a) Conduction loss The conduction loss of the switch S_2 is calculated in (A.8), and the conduction loss of the switch S_3 is found by (A.9).

$$P_{S_2,conduction} = (I_o^2 + \frac{\Delta I_L^2}{12}) \times R_{S_2,on} \times D \tag{A.8}$$

where I_o is the output current, ΔI_L is the maximum current ripple in the inductor, $R_{S_2,on}$ is the equivalent on-resistance of the S_2, and D is the duty cycle.

$$P_{S_3,conduction} = (I_{in}^2 + \frac{\Delta I_L^2}{12}) \times R_{S_3,on} \times D \tag{A.9}$$

where I_{in} is the input current, ΔI_L is the maximum current ripple in the inductor, $R_{S_3,on}$ is the equivalent on-resistance of the S_3, and D is the duty cycle.

(b) Switching loss

The switching loss of the switches S_2 and S_3 is calculated in Equations (A.10), and (A.11), respectively [158, 159].

$$P_{S_2,switching} = V_{in} \times I_o \times (t_{S_2,r} + t_{S_2,f}) \times \frac{f_s}{2} \tag{A.10}$$

where V_{in} is the input voltage, I_o is the output current, $t_{S_2,r}$ is the rise time of the S_2, $t_{S_2,f}$ is the fall time of the S_2, and f_s is the switching frequency.

$$P_{S_3,switching} = V_o \times I_{in} \times (t_{S_3,r} + t_{S_3,f}) \times \frac{f_s}{2} \tag{A.11}$$

where V_o is the output voltage, I_{in} is the input current, $t_{S_3,r}$ is the rise time of the S_3, $t_{S_3,f}$ is the fall time of the S_3, and f_s is the switching frequency.

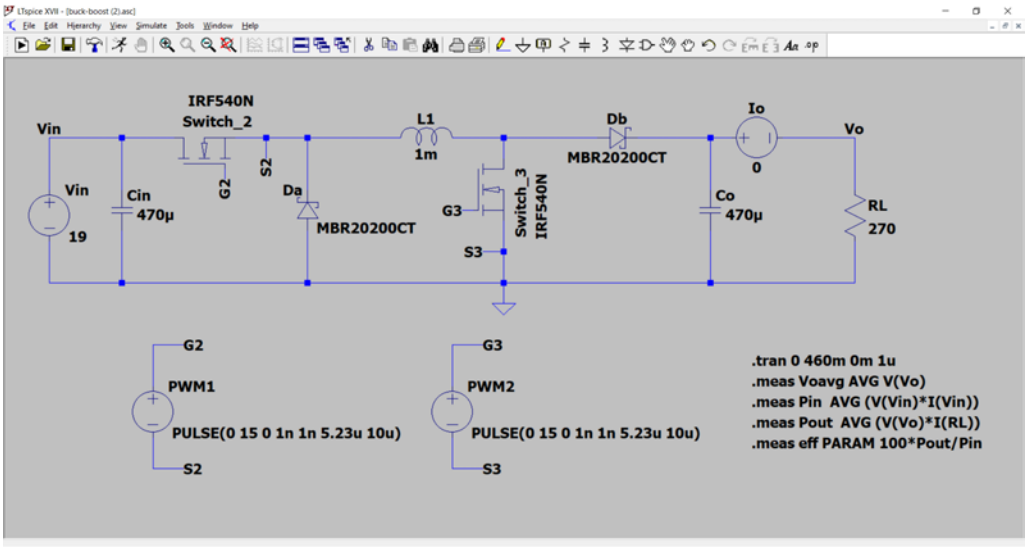


Figure A.2: The converter-based PVE using LTspice simulation.

A.3 The Transistor-based PV Emulator

The LTspice program mimics the PV panel's I-V and P-V curves of the proposed transistor-based PV emulator. Furthermore, it is used to calculate the power losses at different power levels, as shown in Fig. A.3. The current Ic_{T_p} passes through the collector of the power transistor (T_p), which varies from the current at short-circuit operating condition (0A) to a maximum value at open-circuit operating condition (I_{sc}). Based on Equation (6.6), in the worst-case scenario, i.e., the OCV, the base

current of the power transistor is delivered by the first transistor of the cascade, T_{c1}, and is expressed by [31, 161]:

$$i_{B_{T_p}} \cong \frac{I_{sc}}{\beta_p} \tag{A.12}$$

where the $i_{B_{T_p}}$ is the base current of the power transistor (T_p), I_{sc} is the short circuit current of the real PV system, and β_p is the power transistor current gain.

Using the same approach in Equation (A.12), the collector current for any control transistors can be generalized as follows:

$$i_{B_{T_{ci}}} \cong \frac{I_{sc}}{\beta_{ci}} \tag{A.13}$$

where the $i_{B_{T_{ci}}}$ is the base current of the control transistor (T_{ci}) and i can be equals any value from 1 to m, I_{sc} is the short circuit current of the real PV system, and β_{ci} is the multiplication of the cascade control transistor current gain.

The power loss in the power transistor (T_p) is calculated as follows:

$$P_{T_p} = V_{oc} \times Ic_{T_p} \cong V_{oc} \times I_{sc} \tag{A.14}$$

where the V_{oc} is the open-circuit voltage of the real PV system, and the Ic_{T_p} is the collector current of the power transistor (T_p).

The dissipated power in the mth control transistor is calculated as follows:

$$P_{T_{cm}} = (V_{oc} - m \times V_{FW}) \times Ic_{T_{cm}} \tag{A.15}$$

where the V_{oc} is the open-circuit voltage of the real PV system, m is the number of control transistors, V_{FW} is the forward voltage of the control transistor (V), and the $Ic_{T_{cm}}$ is the collector current of the control transistor (T_{cm}).

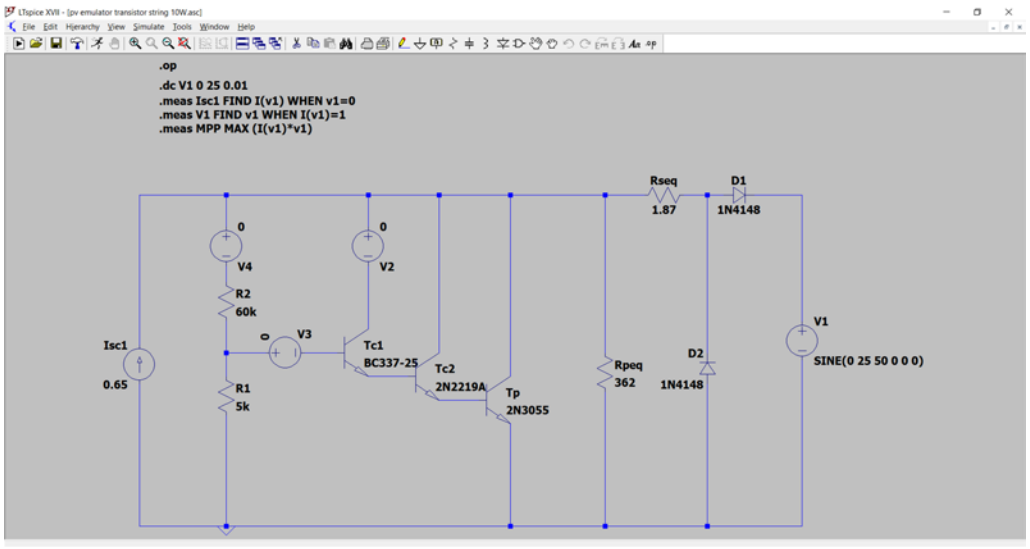


Figure A.3: The LTspice simulation file of the PVE is based on a transistor string.

Appendix B

The Components Datasheets of the Proposed PVEs

B.1 Power Diode (1N5400)

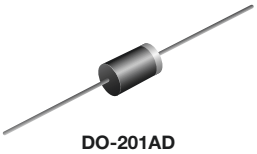
VISHAY

1N5400, 1N5401, 1N5402, 1N5403, 1N5404, 1N5405, 1N5406, 1N5407, 1N5408

www.vishay.com

Vishay General Semiconductor

General Purpose Plastic Rectifier



DO-201AD

FEATURES

- Low forward voltage drop
- Low leakage current
- High forward surge capability
- Solder dip 275 °C max. 10 s, per JESD 22-B106
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb e3 RoHS COMPLIANT

PRIMARY CHARACTERISTICS	
$I_{F(AV)}$	3.0 A
V_{RRM}	50 V, 100 V, 200 V, 300 V, 500 V, 600 V, 800 V, 1000 V
I_{FSM}	200 A
I_R	5.0 µA
V_F	1.2 V
T_J max.	150 °C
Package	DO-201AD
Diode variations	Single die

TYPICAL APPLICATIONS

For use in general purpose rectification of power supplies, inverters, converters and freewheeling diodes application.

Note

- These devices are not AEC-Q101 qualified.

MECHANICAL DATA

Case: DO-201AD, molded epoxy body
Molding compound meets UL 94 V-0 flammability rating
Base P/N-E3 - RoHS-compliant, commercial grade

Terminals: Matte tin plated leads, solderable per J-STD-002 and JESD 22-B102
E3 suffix meets JESD 201 class 1A whisker test

Polarity: Color band denotes cathode end

MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

PARAMETER	SYMBOL	1N5400	1N5401	1N5402	1N5403	1N5404	1N5405	1N5406	1N5407	1N5408	UNIT
Maximum repetitive peak reverse voltage	V_{RRM}	50	100	200	300	400	500	600	800	1000	V
Maximum RMS voltage	V_{RMS}	35	70	140	210	280	350	420	560	700	V
Maximum DC blocking voltage	V_{DC}	50	100	200	300	400	500	600	800	1000	V
Maximum average forward rectified current 0.5" (12.5 mm) lead length at T_L = 105 °C	$I_{F(AV)}$	3.0									A
Peak forward surge current 8.3 ms single half sine-wave superimposed on rated load	I_{FSM}	200									A
Maximum full load reverse current, full cycle average 0.5" (12.5 mm) lead length at T_L = 105 °C	$I_{R(AV)}$	500									µA
Operating junction and storage temperature range	T_J, T_{STG}	- 50 to + 150									°C

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)												
PARAMETER	**TEST CONDITIONS**	**SYMBOL**	**1N5400**	**1N5401**	**1N5402**	**1N5403**	**1N5404**	**1N5405**	**1N5406**	**1N5407**	**1N5408**	**UNIT**
Maximum instantaneous forward voltage	3.0 A	V_F	1.2									V
Maximum DC reverse current at rated DC blocking voltage	T_A = 25 °C	I_R	5.0									µA
	T_A = 150 °C		500									
Typical junction capacitance	4.0 V, 1 MHz	C_J	30									pF

THERMAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)											
PARAMETER	**SYMBOL**	**1N5400**	**1N5401**	**1N5402**	**1N5403**	**1N5404**	**1N5405**	**1N5406**	**1N5407**	**1N5408**	**UNIT**
Typical thermal resistance	$R_{\theta JA}$ (1)	20									°C/W

Note

(1) Thermal resistance from junction to ambient at 0.375" (9.5 mm) lead length, PCB mounted with 0.8" x 0.8" (20 mm x 20 mm) copper heatsinks

ORDERING INFORMATION (Example)				
PREFERRED P/N	**UNIT WEIGHT (g)**	**PREFERRED PACKAGE CODE**	**BASE QUANTITY**	**DELIVERY MODE**
1N5404-E3/54	1.1	54	1400	13" diameter paper tape and reel
1N5404-E3/73	1.1	73	1000	Ammo pack packaging

RATINGS AND CHARACTERISTICS CURVES (T_A = 25 °C unless otherwise noted)

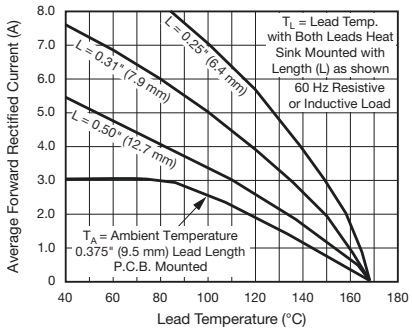


Fig. 1 - Forward Current Derating Curve

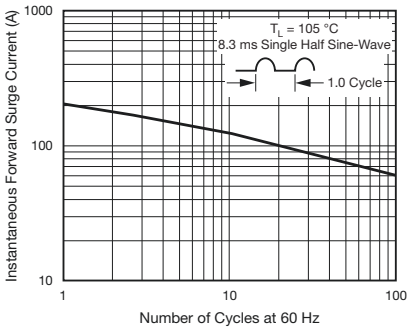


Fig. 2 - Maximum Non-Repetitive Peak Forward Surge Current

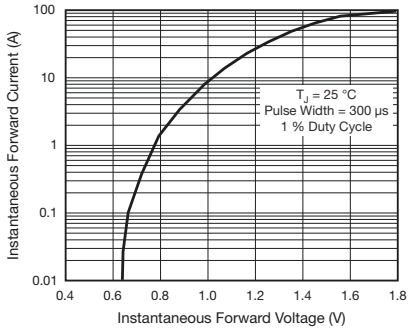


Fig. 3 - Typical Instantaneous Forward Characteristics

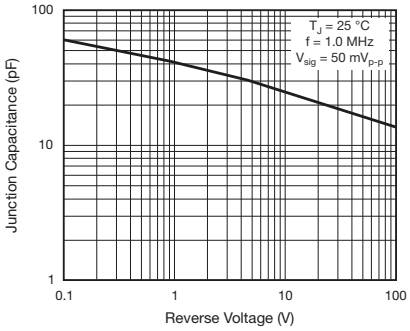


Fig. 5 - Typical Junction Capacitance

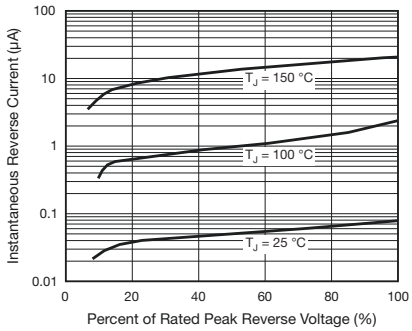


Fig. 4 - Typical Reverse Characteristics

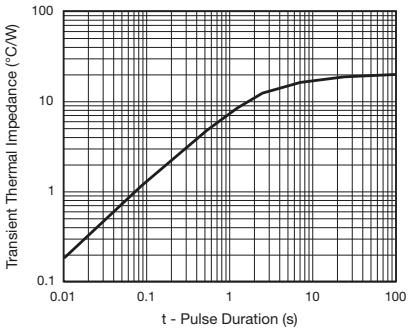
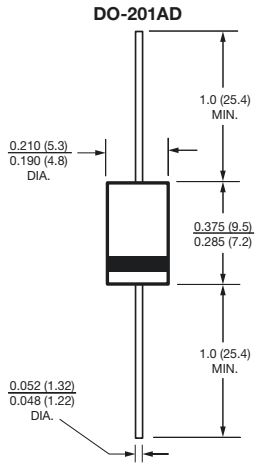


Fig. 6 - Typical Transient Thermal Impedance

PACKAGE OUTLINE DIMENSIONS in inches (millimeters)



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B.2 Cooling Fan (PVA092G12M)

https://www.elecok.com/sa/

FOXCONN PVA092G12M 12V 0.24A 3wires Cooling Fan

FOXCONN PVA092G12M 12V 0.24A 3wires Cooling Fan

Manufacturer	FOXCONN
Part number	PVA092G12M
other name	PVAO92G12M,
AC/DC	DC Fans
Fan Type	Axial
Voltage	12V
Current	0.24A
Termination	3 wires

B.3 Thermal Imaging Camera (FLIR TG167)

FLIR TG167

Spot Thermal Camera

The FLIR TG167 Spot Thermal Camera bridges the gap between single spot infrared thermometers and FLIR's legendary thermal cameras. Equipped with FLIR's exclusive Lepton® micro thermal sensor, the TG167 lets you see the heat so you know where to reliably measure it. Designed for indoor electrical inspection, the TG167 will help you easily find unseen hot and cold spots in electrical cabinets or switch boxes, giving you quality image detail on even small connectors and wires. Then you can store images and download data to show customers and include in reports.

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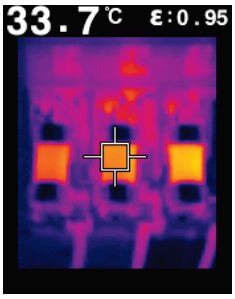

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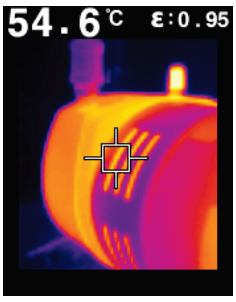

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Specifications

Imaging and optical data	
IR resolution	80 × 60 pixels
Thermal sensitivity/NETD	< 150 mK
Field of view (FOV)	25° × 19.6°
Minimum focus distance	0.1 m (4 in.)
Distance to spot ratio	24:01:00
Image frequency	9 Hz
Focus	Focus free
Detector type	Focal plane array (FPA), uncooled microbolometer
Spectral range	8–14 µm
Display	2.0 in. TFT LCD
Object temperature range	–25 to +380°C (–13 to +716°F)
Accuracy	±1.5% or 1.5°C (2.7°F)
Minimum measurement distance	26 cm (10 in.)
Center spot	Yes
Color palettes	Hot Iron, Rainbow, Grayscale
Memory type	Micro SD card
Image storage capacity	75 000 pictures with included 8 GB Micro SD card
Memory expansion	32 GB SD card maximum
Saved image format	Bitmap (BMP) image with temperature and emissivity
Laser	Dual diverging lasers indicate the temperature measurement area, activated by pulling the trigger
General	
Battery type	Rechargeable Li ion battery
Battery voltage	3.7 V
Battery operating time	>5 hours of continuous scanning with lasers
Battery charge life	30 days minimum
Camera weight, incl. battery	0.312 kg (11 oz.)
Camera size (L × W × H)	186 mm × 55 mm × 94 mm (7.3 in. × 2.2 in. × 3.7 in.)
Tripod mounting	1/4 in.-20 on handle bottom
Includes	Wrist strap lanyard, 8 GB Micro SD card, power supply with separate USB cable, printed documentation

Ordering Information	UPC	EAN
FLIR TG167 Spot Thermal Camera	845188011505	07332558010815
FLIR TA13 EVA Protective Case for TG165	793950377727	0793950377727
FLIR TA14 Belt Holster for TG165	793950377741	0793950377741

USA-NASHUA

FLIR Systems, Inc.
9 Townsend West
Nashua, NH 03063
USA
PH: +1 866.477.3687

USA-PORTLAND
Corporate Headquarters
FLIR Systems, Inc.
27700 SW Parkway Ave.
Wilsonville, OR 97070
USA
PH: +1 866.477.3687

EUROPE

FLIR Systems
Luxemburgstraat 2
2321 Meer
Belgium
PH : +32 (0) 3665 5100

UNITED KINGDOM

FLIR Systems UK
2 Kings Hill Av. - Kings Hill
West Malling
Kent
ME19 4AQ
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B.4 N-Channel, Power MOSFET (IRF540N)

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IOR Rectifier

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IRF540N

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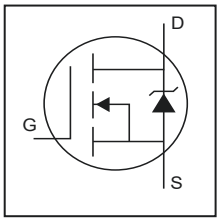
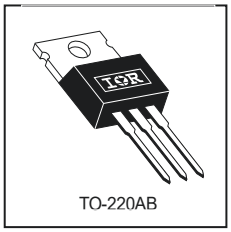
- Fully Avalanche Rated



V_{DSS} = 100V

$R_{DS(on)}$ = 0.052Ω

I_D = 33A



TO-220AB

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	33	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	23	
I_{DM}	Pulsed Drain Current ①	110	
P_D @T_C = 25°C	Power Dissipation	140	W
	Linear Derating Factor	0.91	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	300	mJ
I_{AR}	Avalanche Current①	16	A
E_{AR}	Repetitive Avalanche Energy①	14	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	1.1	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	62	

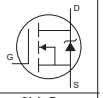
5/13/98

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.052	Ω	V_{GS} = 10V, I_D = 16A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	11	—	—	S	V_{DS} = 50V, I_D = 16A
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 100V, V_{GS} = 0V
		—	—	250		V_{DS} = 80V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	94	nC	I_D = 16A
Q_{gs}	Gate-to-Source Charge	—	—	15		V_{DS} = 80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	43		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	8.2	—	ns	V_{DD} = 50V
t_r	Rise Time	—	39	—		I_D = 16A
$t_{d(off)}$	Turn-Off Delay Time	—	44	—		R_G = 5.1Ω
t_f	Fall Time	—	33	—		R_D = 3.0Ω, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1400	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	330	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	170	—		f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	33	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑥	—	—	110		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 16A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	170	250	ns	T_J = 25°C, I_F = 16A
Q_{rr}	Reverse RecoveryCharge	—	1.1	1.6	µC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				



Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 2.0mH R_G = 25Ω, I_{AS} = 16A. (See Figure 12)

③ I_{SD} ≤ 16A, di/dt ≤ 210A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%

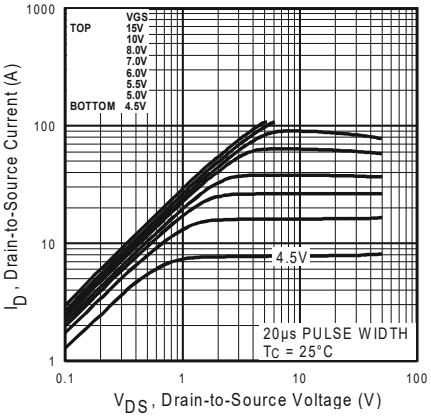


Fig 1. Typical Output Characteristics

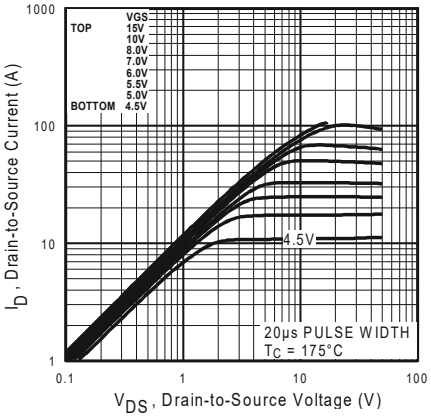


Fig 2. Typical Output Characteristics

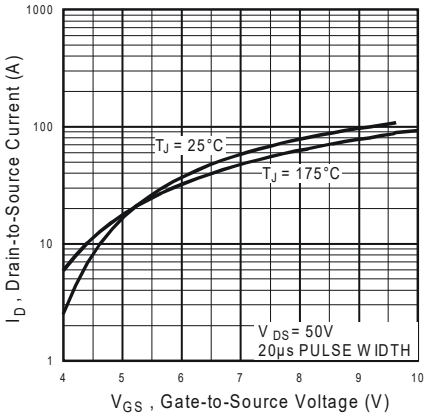


Fig 3. Typical Transfer Characteristics

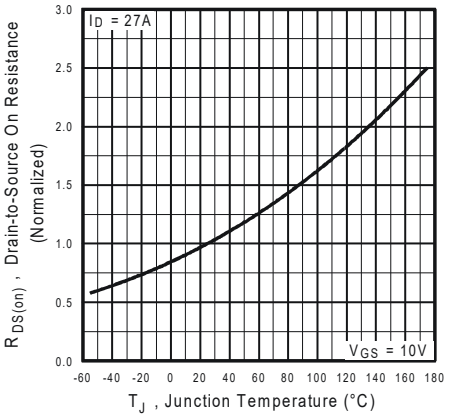


Fig 4. Normalized On-Resistance Vs. Temperature

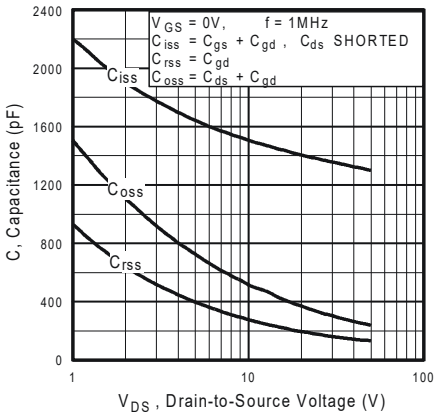


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

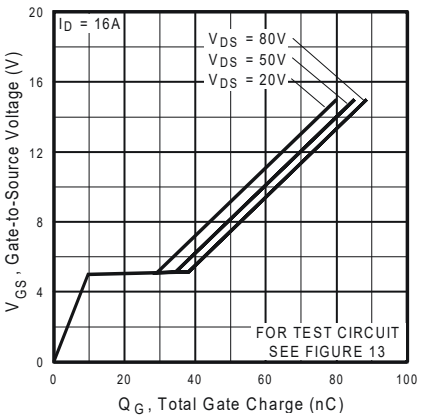


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

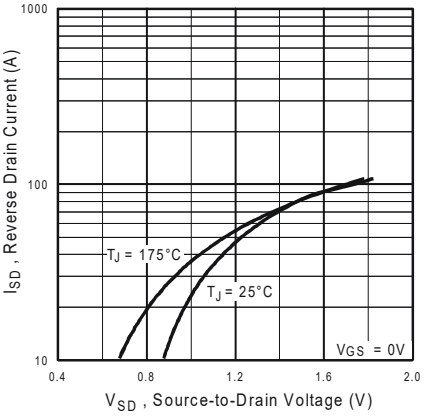


Fig 7. Typical Source-Drain Diode Forward Voltage

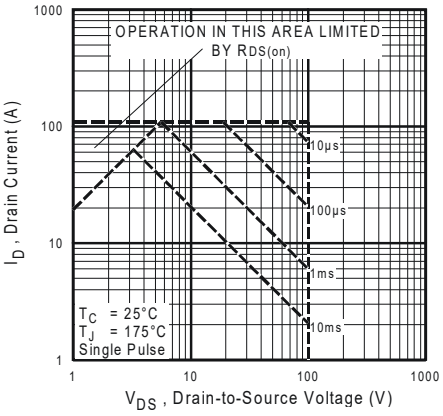


Fig 8. Maximum Safe Operating Area

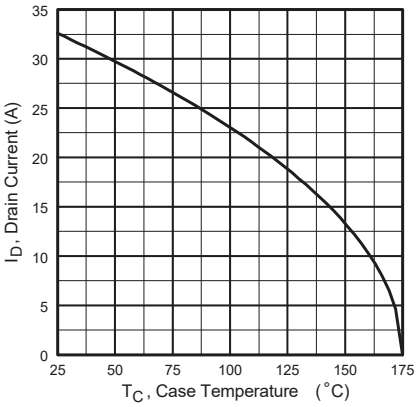


Fig 9. Maximum Drain Current Vs. Case Temperature

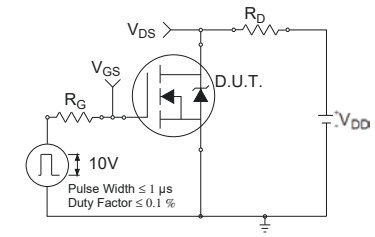


Fig 10a. Switching Time Test Circuit

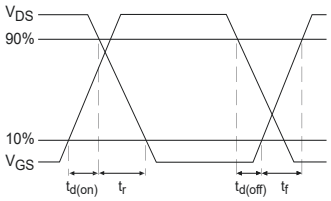


Fig 10b. Switching Time Waveforms

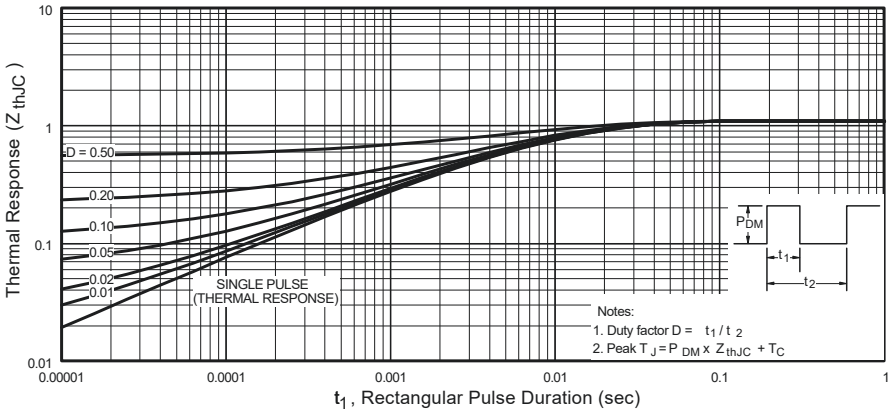


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

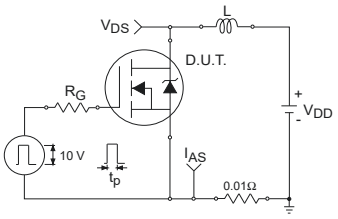


Fig 12a. Unclamped Inductive Test Circuit

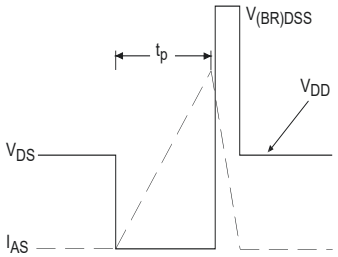


Fig 12b. Unclamped Inductive Waveforms

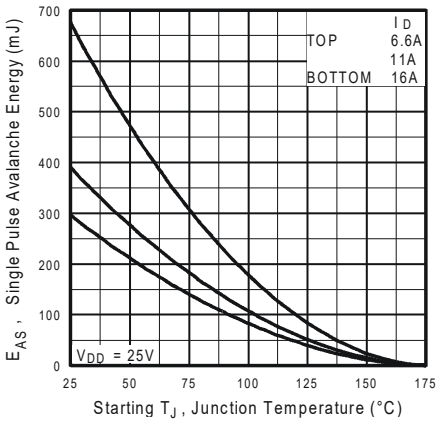


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

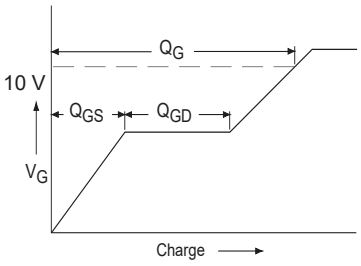


Fig 13a. Basic Gate Charge Waveform

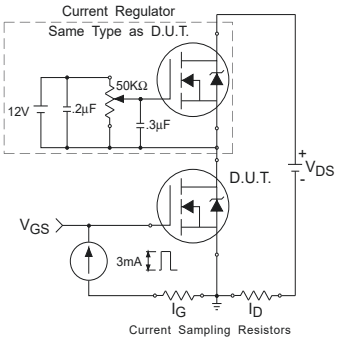


Fig 13b. Gate Charge Test Circuit

B.5 Low-side Power MOSFET driver (TC4428)

TelCom Semiconductor, Inc.

TC4426
TC4427
TC4428

1.5A DUAL HIGH-SPEED POWER MOSFET DRIVERS

FEATURES

- **High Peak Output Current 1.5A**
- **Wide Operating Range ..... 4.5V to 18V**
- **High Capacitive Load Drive Capability ..... 1000pF in 25nsec**
- **Short Delay Time ..... < 40nsec Typ.**
- **Consistent Delay Times With Changes in Supply Voltage**
- **Low Supply Current**
  - **— With Logic "1" Input 4mA**
  - **— With Logic "0" Input 400μA**
- **Low Output Impedance 7Ω**
- **Latch-Up Protected ..... Will Withstand >0.5A Reverse Current ..... Down to – 5V**
- **Input Will Withstand Negative Inputs**
- **ESD Protected 4kV**
- **Pinout Same as TC426/TC427/TC428**

ORDERING INFORMATION

Part No.	Package	Temperature Range
TC4426COA	8-Pin SOIC	0°C to +70°C
TC4426CPA	8-Pin Plastic DIP	0°C to +70°C
TC4426EOA	8-Pin SOIC	– 40°C to +85°C
TC4426EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC4426MJA	8-Pin CerDIP	– 55°C to +125°C
TC4427COA	8-Pin SOIC	0°C to +70°C
TC4427CPA	8-Pin Plastic DIP	0°C to +70°C
TC4427EOA	8-Pin SOIC	– 40°C to +85°C
TC4427EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC4427MJA	8-Pin CerDIP	– 55°C to +125°C
TC4428COA	8-Pin SOIC	0°C to +70°C
TC4428CPA	8-Pin Plastic DIP	0°C to +70°C
TC4428EOA	8-Pin SOIC	– 40°C to +85°C
TC4428EPA	8-Pin Plastic DIP	– 40°C to +85°C
TC4428MJA	8-Pin CerDIP	– 55°C to +125°C

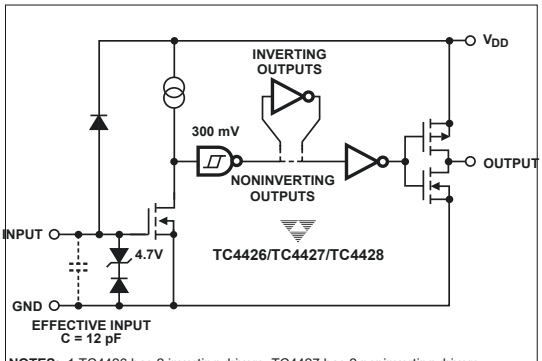
GENERAL DESCRIPTION

The TC4426/4427/4428 are improved versions of the earlier TC426/427/428 family of buffer/drivers (with which they are pin compatible). They will not latch up under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (of either polarity) occurs on the ground pin. They can accept, without damage or logic upset, up to 500 mA of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against up to 4kV of electrostatic discharge.

As MOSFET drivers, the TC4426/4427/4428 can easily switch 1000pF gate capacitances in under 30nsec, and provide low enough impedances in both the ON and OFF states to ensure the MOSFET's intended state will not be affected, even by large transients.

Other compatible drivers are the TC4426A/27A/28A. These drivers have matched input to output leading edge and falling edge delays, tD1 and tD2, for processing short duration pulses in the 25 nsec range. They are pin compatible with the TC4426/27/28.

FUNCTIONAL BLOCK DIAGRAM



NOTES: 1.TC4426 has 2 inverting drivers; TC4427 has 2 noninverting drivers.
2. TC4428 has one inverting and one noninverting driver.
3. Ground any unused driver input.

1.5A DUAL HIGH-SPEED POWER MOSFET DRIVERS

TC4426
TC4427
TC4428

ABSOLUTE MAXIMUM RATINGS*

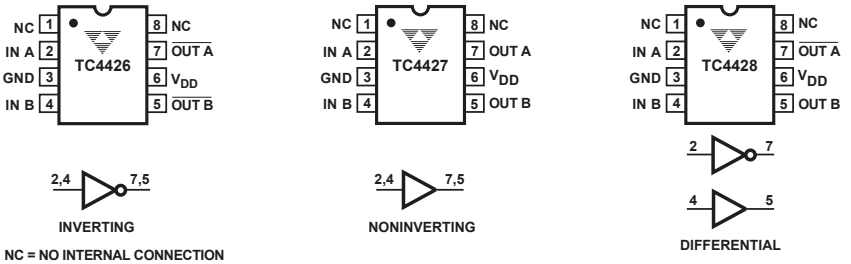
Supply Voltage ..... +22V
Input Voltage, IN A or IN B . (V_{DD} + 0.3V) to (GND – 5.0V)
Maximum Chip Temperature ..... +150°C
Storage Temperature Range ..... – 65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Thermal Resistance
- CerDIP $R_{\theta J-A}$ ..... 150°C/W
- CerDIP $R_{\theta J-C}$ ..... 50°C/W
- PDIP $R_{\theta J-A}$ ..... 125°C/W
- PDIP $R_{\theta J-C}$ ..... 42°C/W
- SOIC $R_{\theta J-A}$ ..... 155°C/W
- SOIC $R_{\theta J-C}$ ..... 45°C/W

Operating Temperature Range
- C Version ..... 0°C to +70°C
- E Version ..... – 40°C to +85°C
- M Version ..... – 55°C to +125°C

Package Power Dissipation ($T_A \leq 70°C$)
- Plastic 730mW
- CerDIP 800mW
- SOIC 470mW

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS



NC = NO INTERNAL CONNECTION
NOTE: SOIC pinout is identical to DIP.

ELECTRICAL CHARACTERISTICS: T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	– 1	—	1	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	V_{DD} = 18V, I_O = 10mA	—	7	10	Ω
I_{PK}	Peak Output Current	Duty Cycle ≤ 2%, t ≤ 30µsec	—	1.5	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 30 µsec	> 0.5	—	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1	—	19	30	nsec
t_F	Fall Time	Figure 1	—	19	30	nsec
t_{D1}	Delay Time	Figure 1	—	20	30	nsec
t_{D2}	Delay Time	Figure 1	—	40	50	nsec
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs) V_{IN} = 0V (Both Inputs)	— —	— —	4.5 0.4	mA mA

NOTE: 1. Switching times are guaranteed by design.

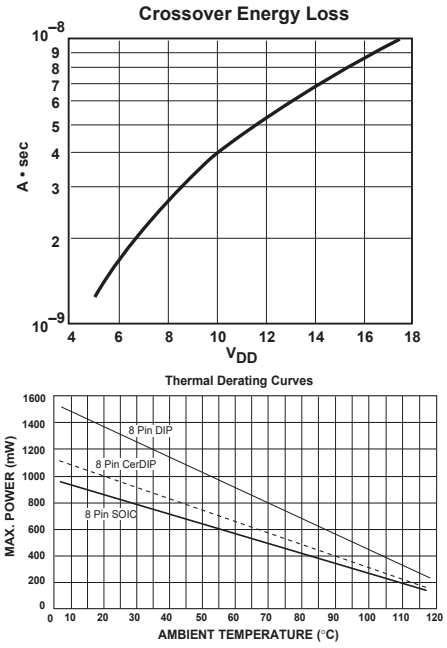
1.5A DUAL HIGH-SPEED POWER MOSFET DRIVERS

TC4426
TC4427
TC4428

ELECTRICAL CHARACTERISTICS: Specifications measured over operating temperature range with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	– 10	—	10	µA
Output						
V_{OH}	High Output Voltage		V_{DD} – 0.025	—	—	V
V_{OL}	Low Output Voltage		—	—	0.025	V
R_O	Output Resistance	V_{DD} = 18V, I_O = 10mA	—	9	12	Ω
I_{PK}	Peak Output Current	Duty Cycle ≤ 2%, t ≤ 300µsec	—	1.5	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle≤ 2% t ≤ 300µsec	> 0.5	—	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1	—	—	40	nsec
t_F	Fall Time	Figure 1	—	—	40	nsec
t_{D1}	Delay Time	Figure 1	—	—	40	nsec
t_{D2}	Delay Time	Figure 1	—	—	60	nsec
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V (Both Inputs) V_{IN} = 0V (Both Inputs)	— —	— —	8 0.6	mA mA

NOTE: 1. Switching times are guaranteed by design.



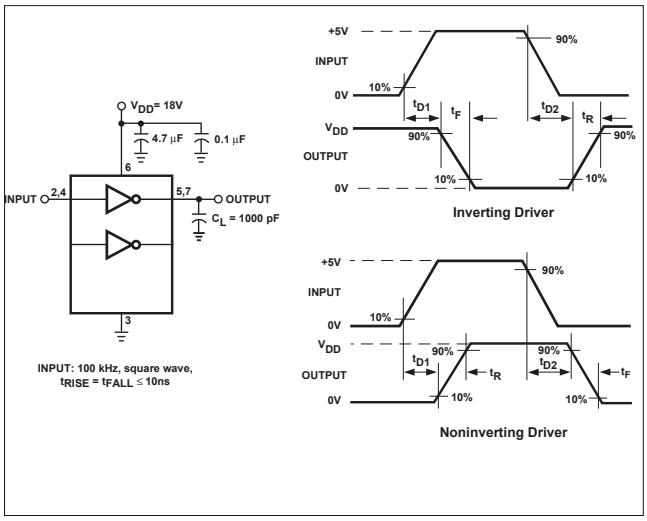
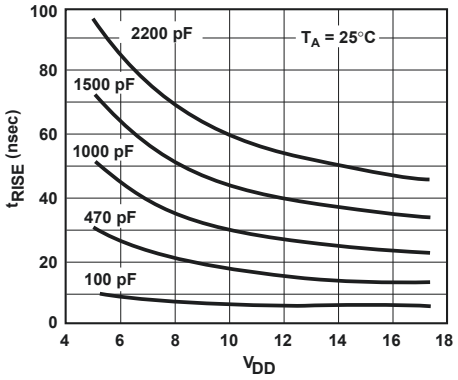


Figure 1. Switching Time Test Circuit

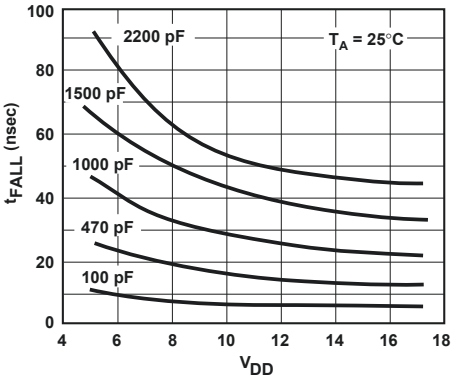
NOTE: The values on this graph represent the loss seen by both drivers in a package during one complete cycle. For a single driver, divide the stated values by 2. For a single transition of a single driver, divide the stated value by 4.

TYPICAL CHARACTERISTICS

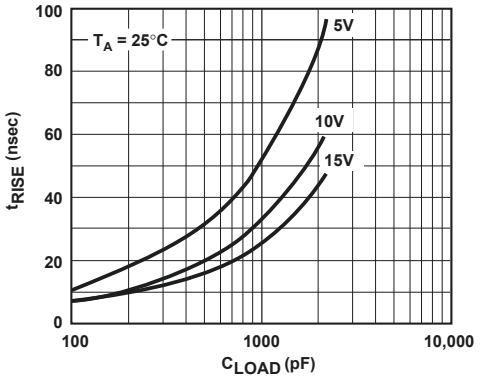
Rise Time vs. Supply Voltage



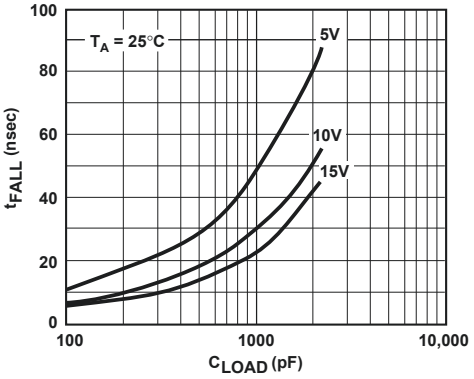
Fall Time vs. Supply Voltage



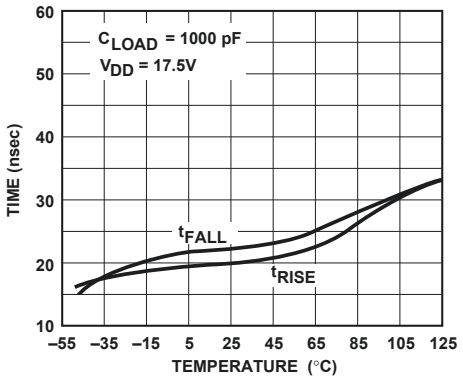
Rise TIme vs. Capacitive Load



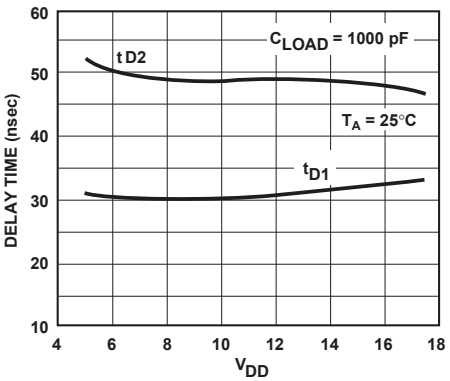
Fall TIme vs. Capacitive Load



Rise and Fall Times vs. Temperature

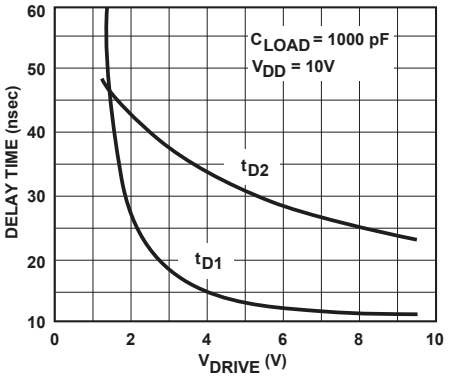


Propagation Delay vs. Supply Voltage

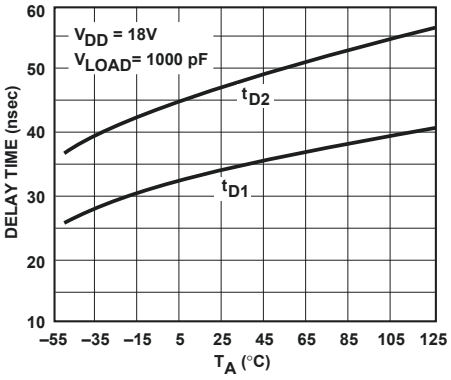


TYPICAL CHARACTERISTICS (Cont.)

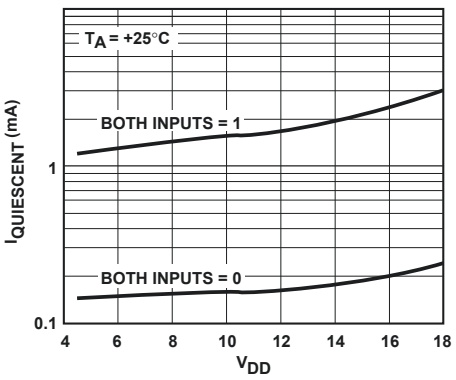
Effect of Input Amplitude on Delay Time



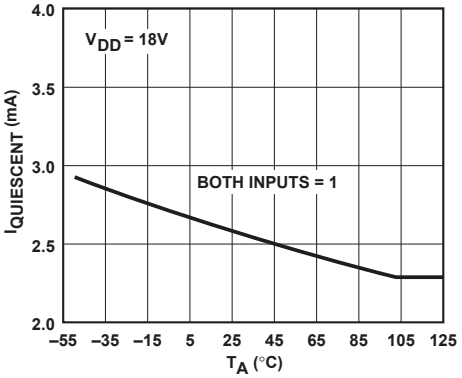
Propagation Delay Time vs. Temperature



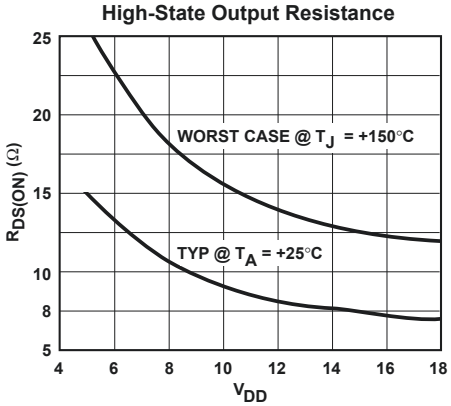
Quiescent Supply Current vs. Voltage



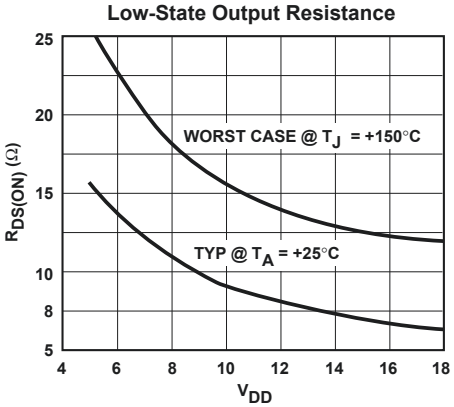
Quiescent Supply Current vs. Temperature



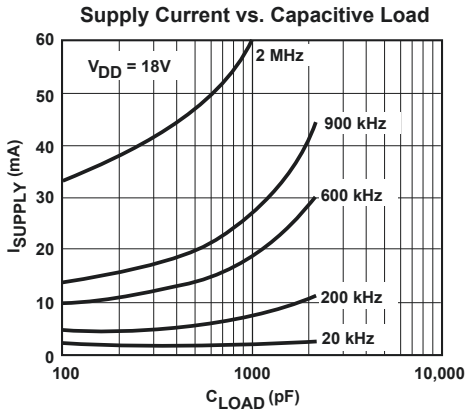
High-State Output Resistance

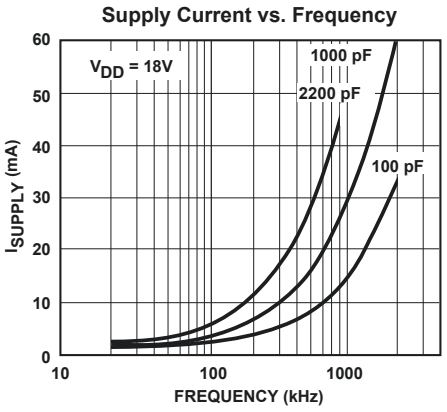


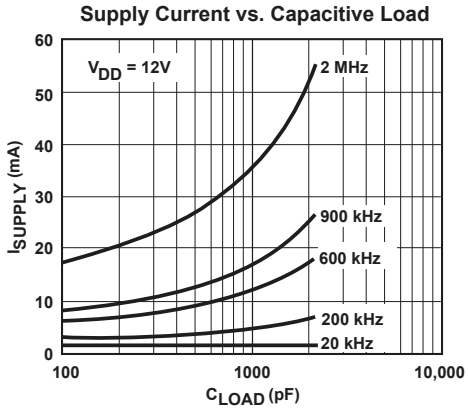
Low-State Output Resistance

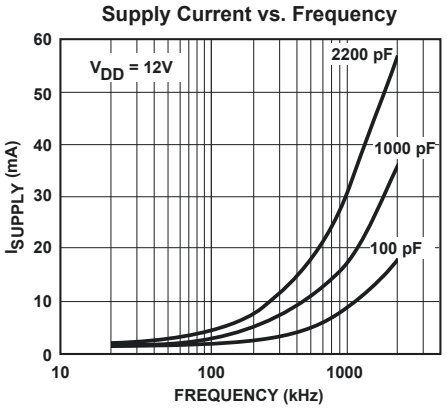


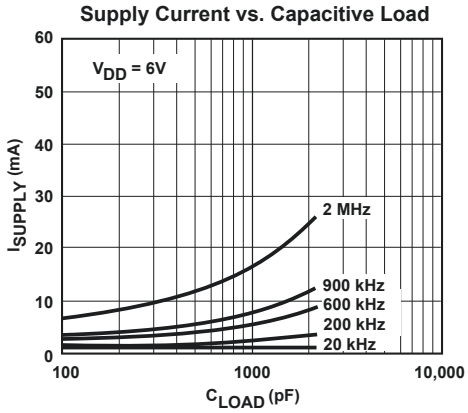
SUPPLY CURRENT CHARACTERISTICS (Load on Single Output Only)

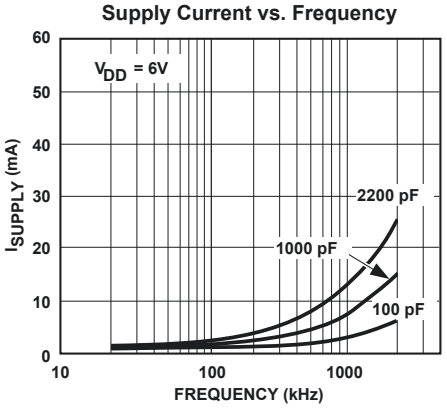










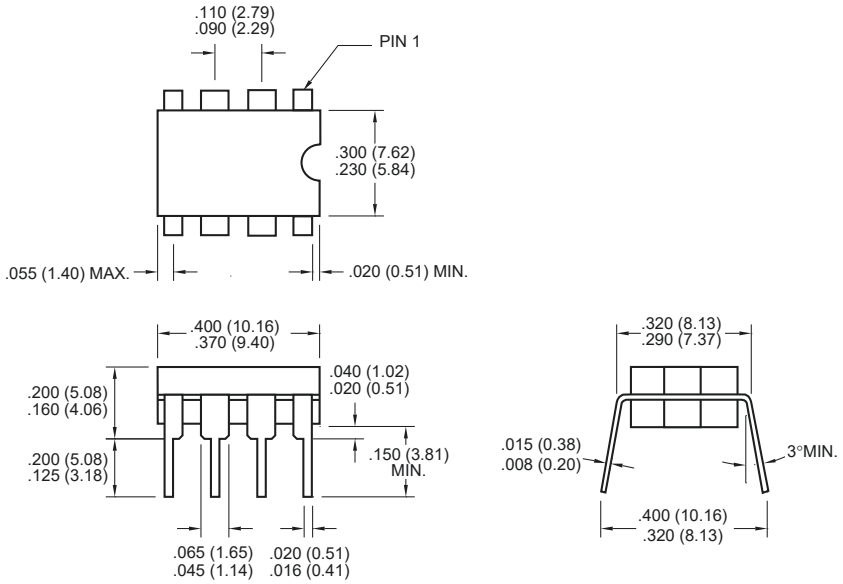


1.5A DUAL HIGH-SPEED POWER MOSFET DRIVERS

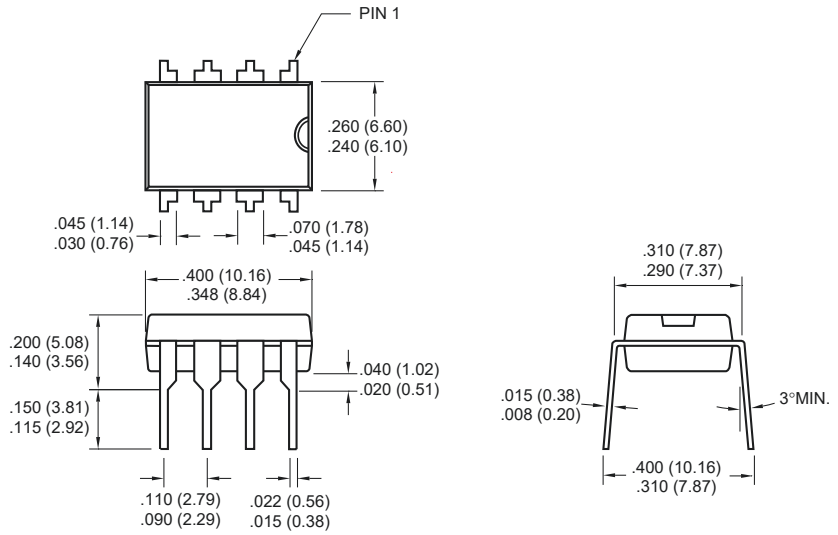
TC4426
TC4427
TC4428

PACKAGE DIMENSIONS

8-Pin CerDIP



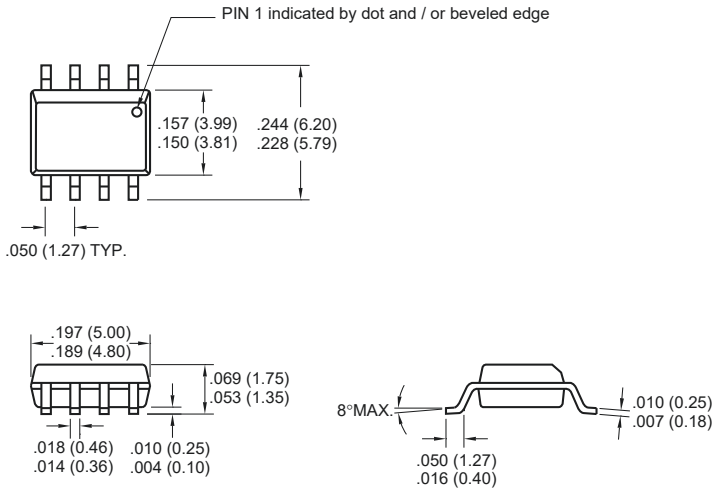
8-Pin Plastic DIP



Dimensions: inches (mm)

PACKAGE DIMENSIONS Cont.)

8-Pin SOIC



Dimensions: inches (mm)

Sales Offices

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Printed in the U.S.A.

B.6 High-side Power MOSFET driver (IR2184PBF)

International
IOR Rectifier

Data Sheet No. PD60174 revG

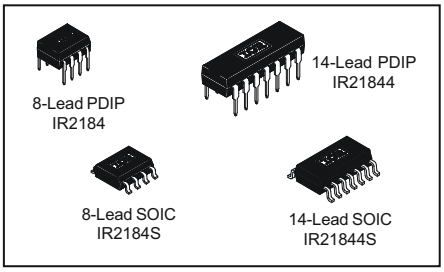
IR2184(4)(S)&(PbF)

HALF-BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V and 5V input logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5V offset.
- Lower di/dt gate driver for better noise immunity
- Output source/sink current capability 1.4A/1.8A
- Also available LEAD-FREE (PbF)

Packages



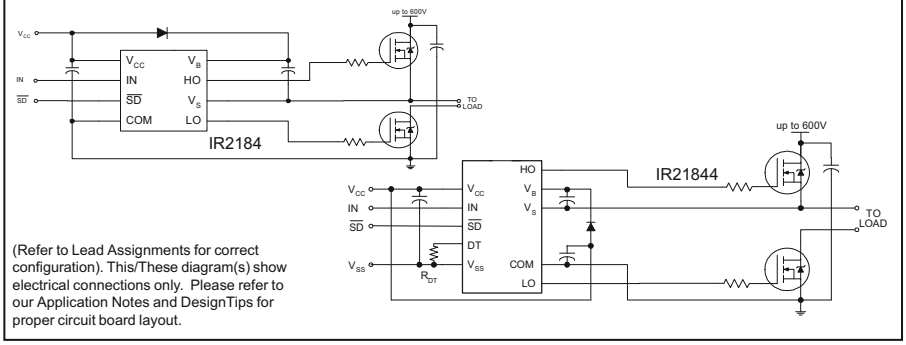
Description

The IR2184(4)(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

IR2181/IR2183/IR2184 Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Dead-Time	Ground Pins	Ton/Toff
2181	HIN/LIN	no	none	COM	180/220 ns
21814				VSS/COM	
2183	HIN/$\overline{\text{LIN}}$	yes	Internal 500ns	COM	180/220 ns
21834			Program 0.4 ~ 5 us	VSS/COM	
2184	IN/$\overline{\text{SD}}$	yes	Internal 500ns	COM	680/270 ns
21844			Program 0.4 ~ 5 us	VSS/COM	

Typical Connection



(Refer to Lead Assignments for correct configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating absolute voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
DT	Programmable dead-time pin voltage (IR21844 only)		V_{SS} - 0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)		V_{SS} - 0.3	V_{SS} + 10	
V_{SS}	Logic ground (IR21844 only)		V_{CC} - 25	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(8-lead PDIP)	—	1.0	W
		(8-lead SOIC)	—	0.625	
		(14-lead PDIP)	—	1.6	
		(14-lead SOIC)	—	1.0	
Rth_{JA}	Thermal resistance, junction to ambient	(8-lead PDIP)	—	125	°C/W
		(8-lead SOIC)	—	200	
		(14-lead PDIP)	—	75	
		(14-lead SOIC)	—	120	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
VB	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (IN & $\overline{SD}$)	V_{SS}	V_{SS} + 5	
DT	Programmable dead-time pin voltage (IR21844 only)	V_{SS}	V_{CC}	
V_{SS}	Logic ground (IR21844 only)	-5	5	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).
Note 2: IN and SD are internally clamped with a 5.2V zener diode.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, T_A = 25°C, DT = VSS unless otherwise specified.

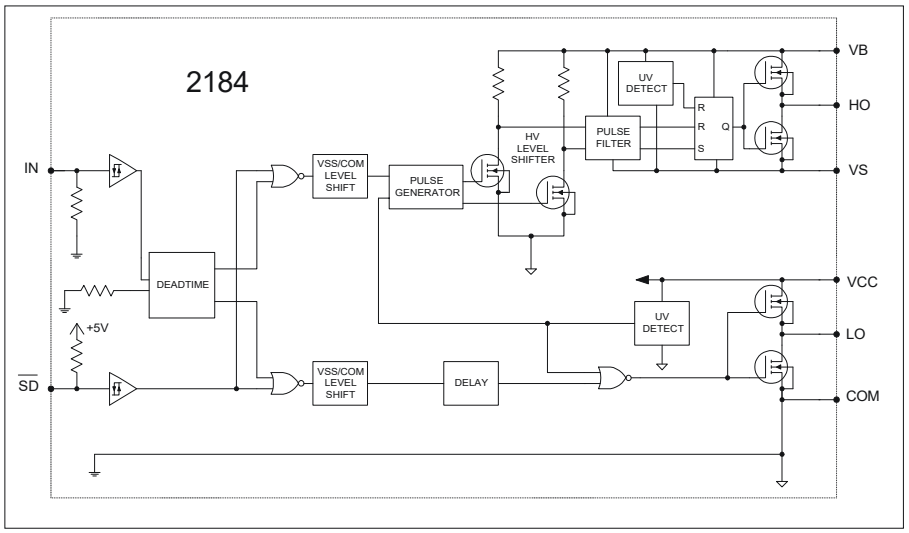
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	680	900	nsec	V_S = 0V
t_{off}	Turn-off propagation delay	—	270	400		V_S = 0V or 600V
t_{sd}	Shut-down propagation delay	—	180	270		
MTon	Delay matching, HS & LS turn-on	—	0	90		
MToff	Delay matching, HS & LS turn-off	—	0	40		
t_r	Turn-on rise time	—	40	60		V_S = 0V
t_f	Turn-off fall time	—	20	35		V_S = 0V
DT	Deadtime: LO turn-off to HO turn-on(DT_{LO-HO}) &	280	400	520		RDT= 0
	HO turn-off to LO turn-on (DT_{HO-LO})	4	5	6	µsec	RDT = 200k
MDT	Deadtime matching = $DT_{LO\ -\ HO}$ - DT_{HO-LO}	—	0	50	nsec	RDT=0
		—	0	600		RDT = 200k

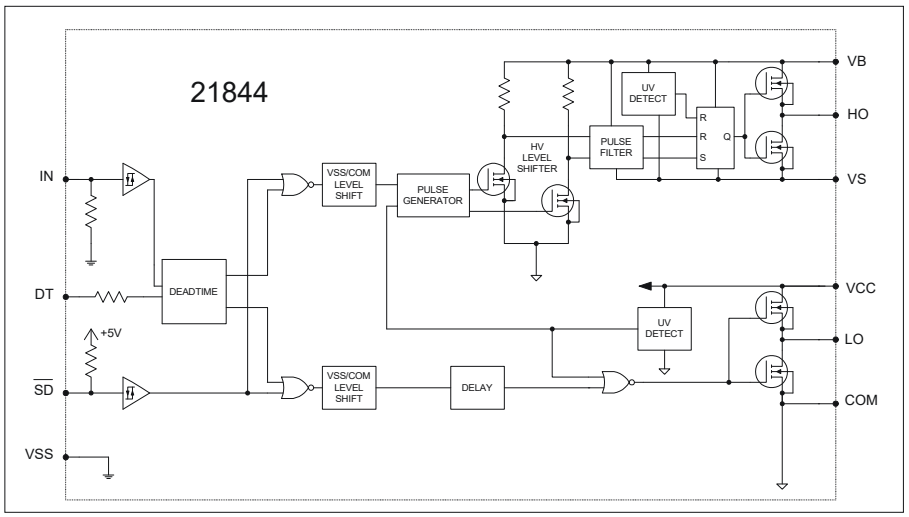
Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, DT= V_{SS} and T_A = 25°C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to V_{SS} /COM and are applicable to the respective input leads: IN and $\overline{SD}$. The V_O, I_O and Ron parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “1” input voltage for HO & logic “0” for LO	2.7	—	—	V	V_{CC} = 10V to 20V
V_{IL}	Logic “0” input voltage for HO & logic “1” for LO	—	—	0.8		V_{CC} = 10V to 20V
$V_{SD,TH+}$	$\overline{SD}$ input positive going threshold	2.7	—	—		V_{CC} = 10V to 20V
$V_{SD,TH-}$	$\overline{SD}$ input negative going threshold	—	—	0.8		V_{CC} = 10V to 20V
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	1.2		I_O = 0A
V_{OL}	Low level output voltage, V_O	—	—	0.1		I_O = 0A
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600V
I_{QBS}	Quiescent V_{BS} supply current	20	60	150		V_{IN} = 0V or 5V
I_{QCC}	Quiescent V_{CC} supply current	0.4	1.0	1.6	mA	V_{IN} = 0V or 5V
I_{IN+}	Logic “1” input bias current	—	25	60	µA	IN = 5V, $\overline{SD}$ = 0V
I_{IN-}	Logic “0” input bias current	—	—	1.0		IN = 0V, $\overline{SD}$ = 5V
V_{CCUV+} V_{BSUV+}	V_{CC} and V_{BS} supply undervoltage positive going threshold	8.0	8.9	9.8	V	
V_{CCUV-} V_{BSUV-}	V_{CC} and V_{BS} supply undervoltage negative going threshold	7.4	8.2	9.0		
V_{CCUVH} V_{BSUVH}	Hysteresis	0.3	0.7	—		
I_{O+}	Output high short circuit pulsed current	1.4	1.9	—	A	V_O = 0V, PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	1.8	2.3	—		V_O = 15V, PW ≤ 10 µs

Functional Block Diagrams

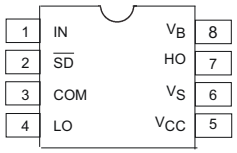




Lead Definitions

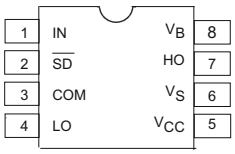
Symbol	Description
IN	Logic input for high and low side gate driver outputs (HO and LO), in phase with HO (referenced to COM for IR2184 and VSS for IR21844)
$\overline{SD}$	Logic input for shutdown (referenced to COM for IR2184 and VSS for IR21844)
DT	Programmable dead-time lead, referenced to VSS. (IR21844 only)
VSS	Logic Ground (21844 only)
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side and logic fixed supply
LO	Low side gate drive output
COM	Low side return

Lead Assignments



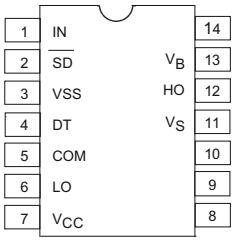
8-Lead PDIP

IR2184



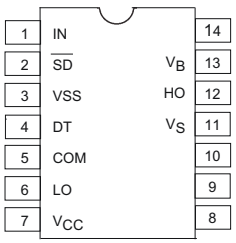
8-Lead SOIC

IR2184S



14-Lead PDIP

IR21844



14-Lead SOIC

IR21844S

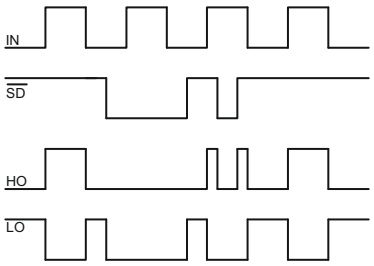


Figure 1. Input/Output Timing Diagram

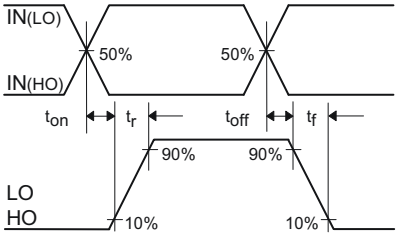


Figure 2. Switching Time Waveform Definitions

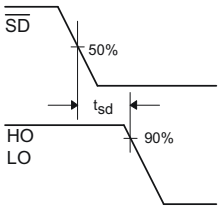


Figure 3. Shutdown Waveform Definitions

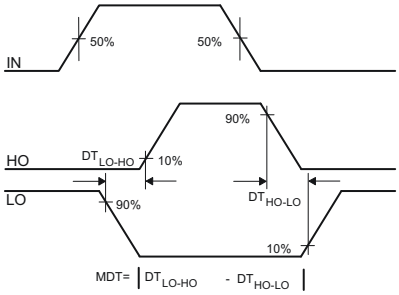


Figure 4. Deadtime Waveform Definitions

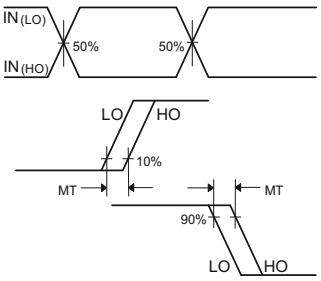


Figure 5. Delay Matching Waveform Definitions

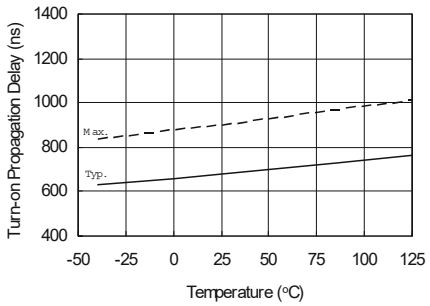


Figure 4A. Turn-on Propagation Delay vs. Temperature

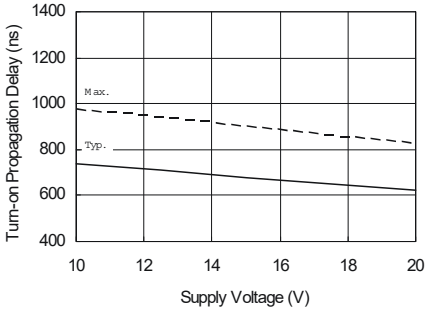


Figure4B. Turn-on Propagation Delay vs. Supply Voltage

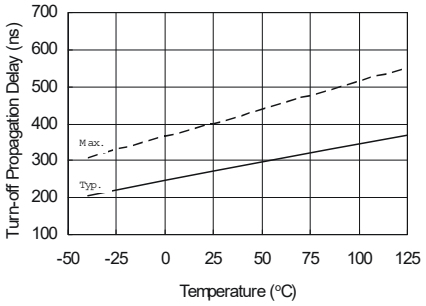


Figure 5A. Turn-off Propagation Delay vs. Temperature

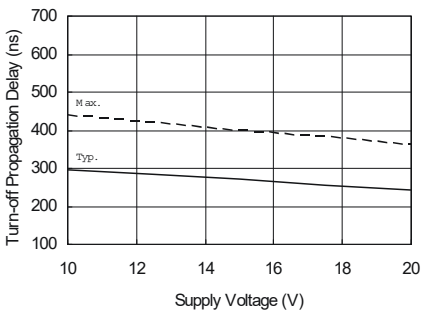


Figure 5B. Turn-off Propagation Delay vs. Supply Voltage

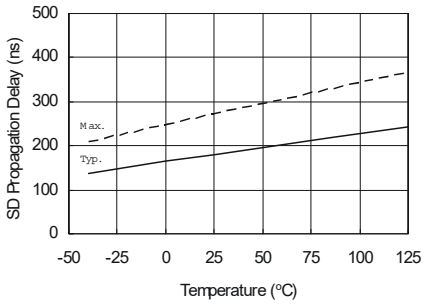


Figure 6A. SD Propagation Delay vs. Temperature

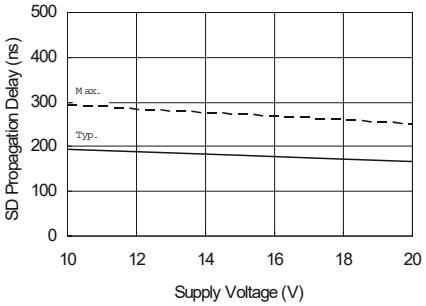


Figure 6B. SD Propagation Delay vs. Supply Voltage

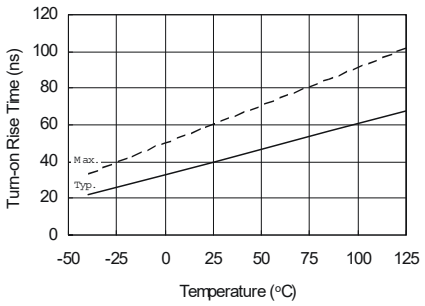


Figure 7A. Turn-on Rise Time vs. Temperature

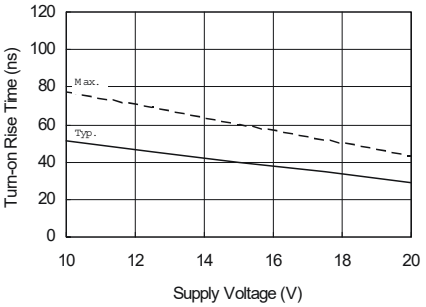


Figure 7B. Turn-on Rise Time vs. Supply Voltage

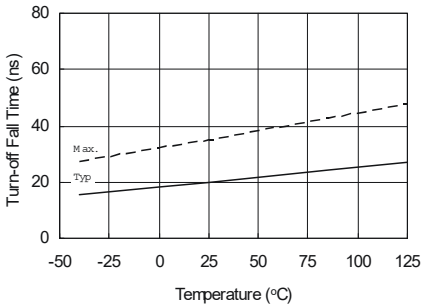


Figure 8A. Turn-off Fall Time vs. Temperature

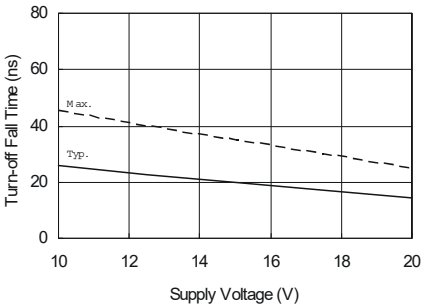


Figure 8B. Turn-off Fall Time vs. Supply Voltage

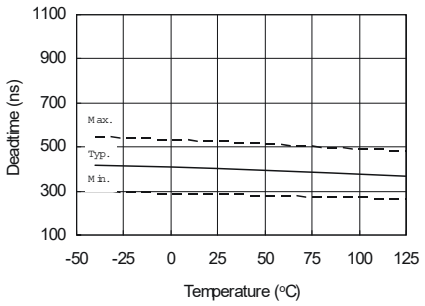


Figure 9A. Deadtime vs. Temperature

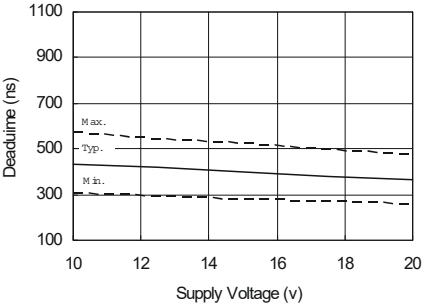


Figure 9B. Deadtime vs. Supply Voltage

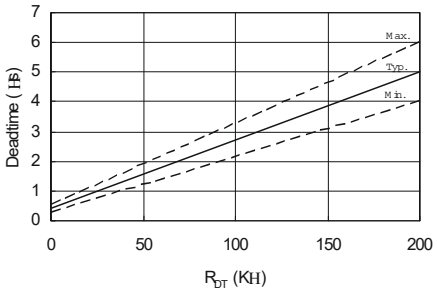


Figure 9C. Deadtime vs. R_{DT}

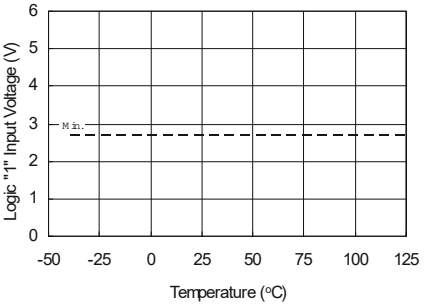


Figure 10A. Logic "1" Input Voltage
vs. Temperature

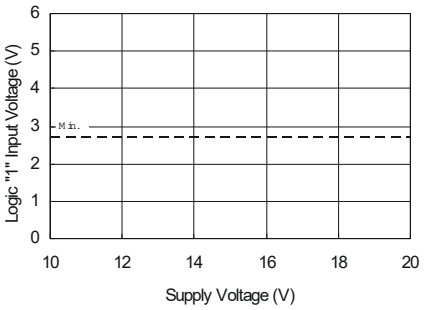


Figure 10B. Logic "1" Input Voltage
vs. Supply Voltage

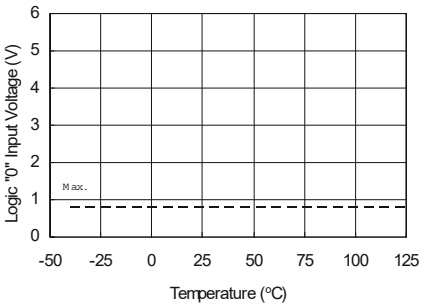


Figure 11A. Logic "0" Input Voltage
vs. Temperature

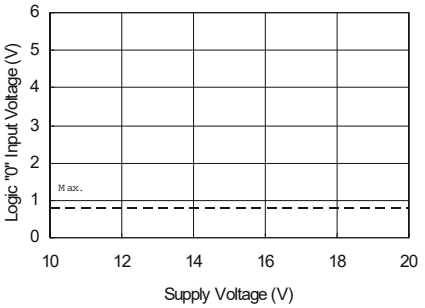


Figure 11B. Logic "0" Input Voltage vs. Supply Voltage

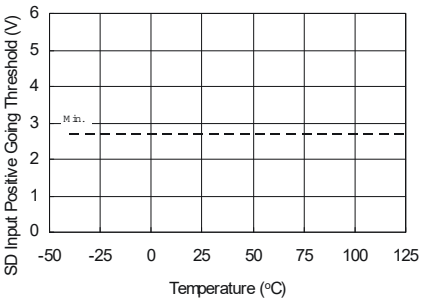


Figure 12A. SD Input Positive Going Threshold vs. Temperature

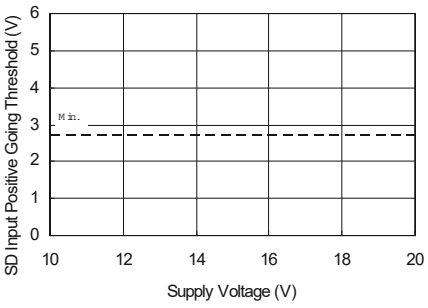


Figure 12B. SD Input Positive Going Threshold vs. Supply Voltage

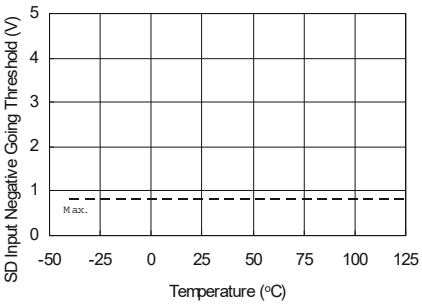


Figure 13A. SD Input Negative Going Threshold vs. Temperature

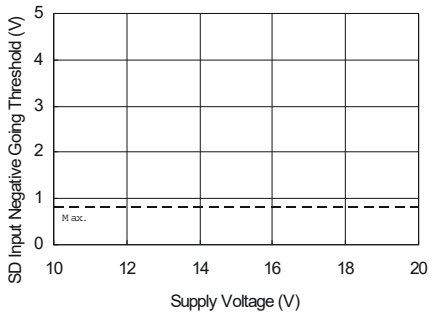


Figure 13B. SD Input Negative Going Threshold vs. Supply Voltage

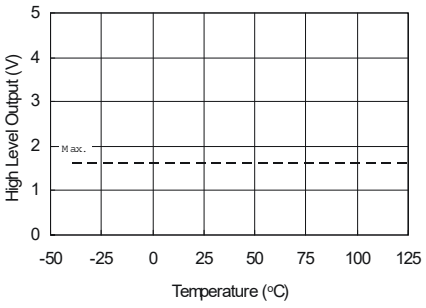


Figure 14A. High Level Output vs. Temperature

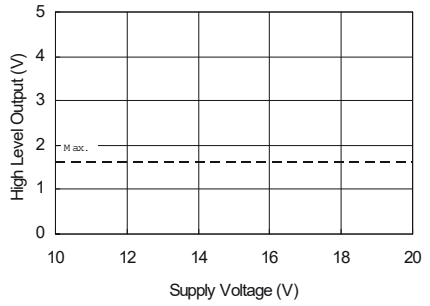


Figure 14B. High Level Output vs. Supply Voltage

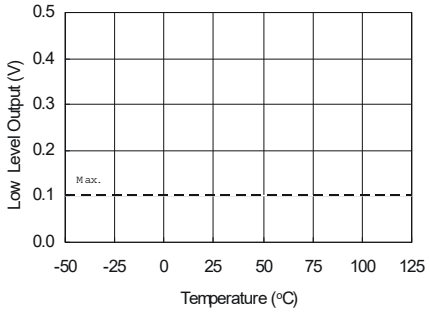


Figure 15A. Low Level Output vs. Temperature

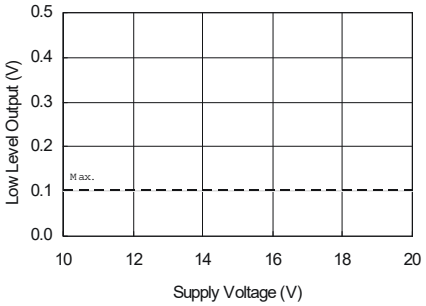


Figure 15B. Low Level Output vs. Supply Voltage

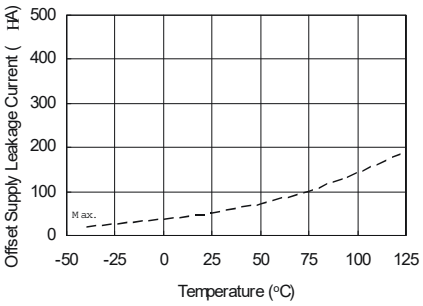


Figure 16A. Offset Supply Leakage Current vs. Temperature

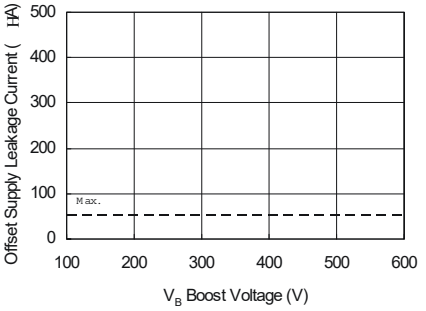


Figure 16B. Offset Supply Leakage Current vs. V_B Boost Voltage

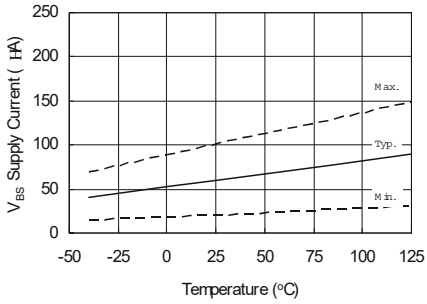


Figure 17A. V_{BS} Supply Current vs. Temperature

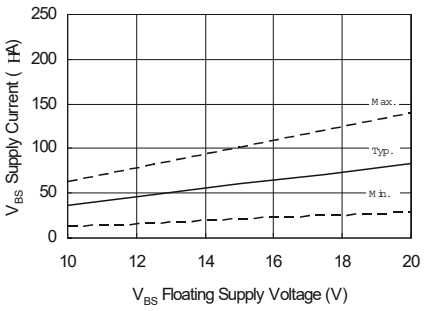


Figure 17B. V_{BS} Supply Current vs. V_{BS} Floating Supply Voltage

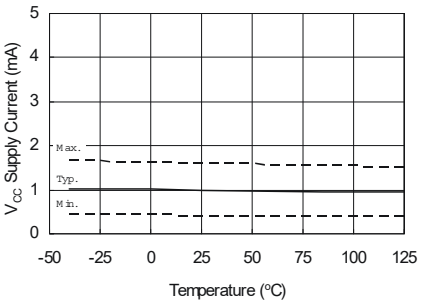


Figure 18A. V_{CC} Supply Current vs. Temperature

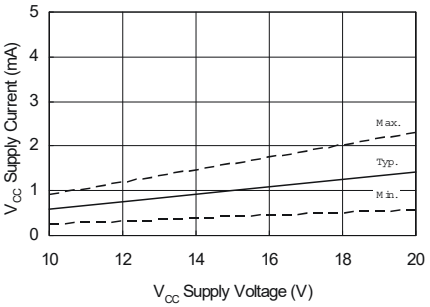


Figure 18B. V_{CC} Supply Current vs. V_{CC} Supply Voltage

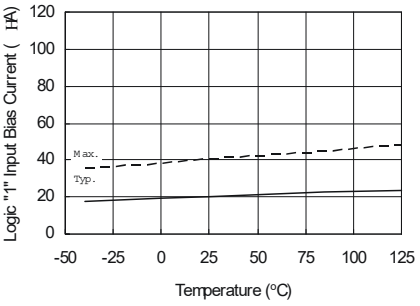


Figure 19A. Logic "1" Input Bias Current vs. Temperature

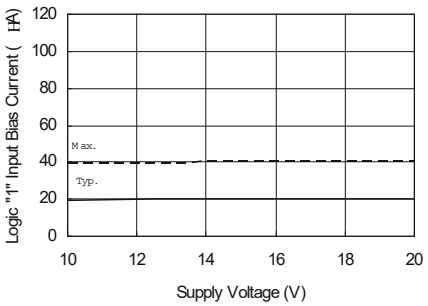


Figure 19B. Logic "1" Input Bias Current vs. Supply Voltage

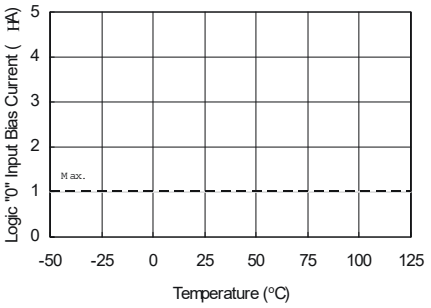


Figure 20A. Logic "0" Input Bias Current vs. Temperature

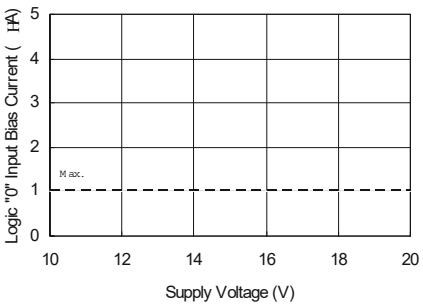


Figure 20B. Logic "0" Input Bias Current vs. Supply Voltage

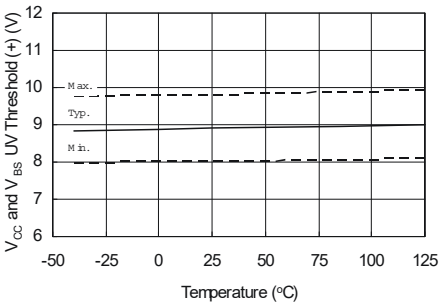


Figure 21. V_{CC} and V_{BS} Undervoltage Threshold (+) vs. Temperature

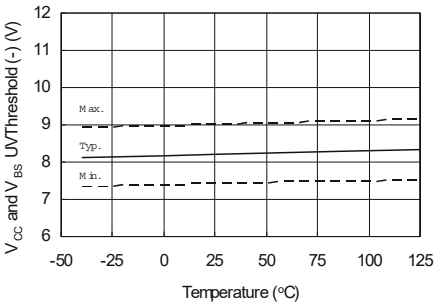


Figure 22. V_{CC} and V_{BS} Undervoltage Threshold (-) vs. Temperature

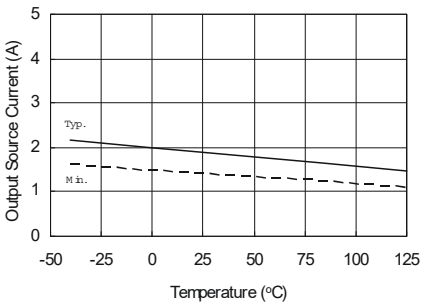


Figure 23A. Output Source Current vs. Temperature

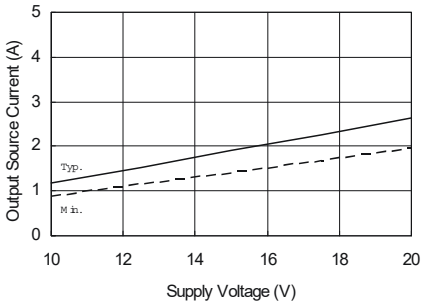


Figure 23B. Output Source Current vs. Supply Voltage

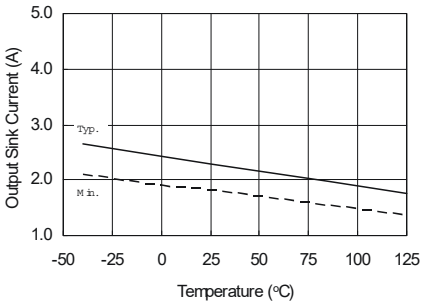


Figure 24A. Output Sink Current vs. Temperature

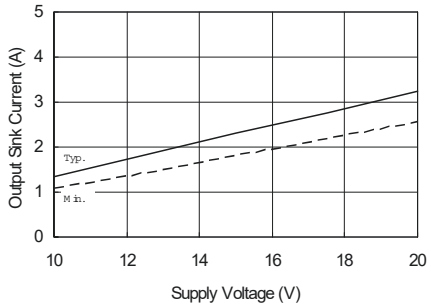


Figure 24B. Output Sink Current vs. Supply Voltage

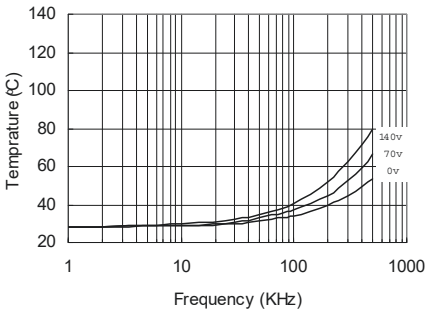


Figure 21. IR2181 vs. Frequency (IRFBC20), $R_{gate}=33\Omega, V_{CC}=15V$

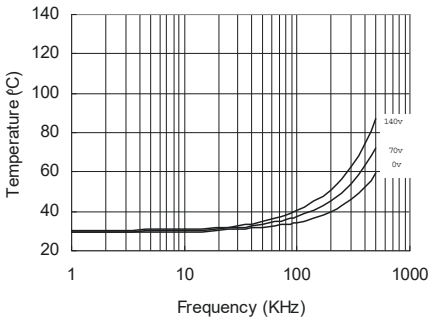


Figure 22. IR2181 vs. Frequency (IRFBC30), $R_{gate}=22\Omega, V_{CC}=15V$

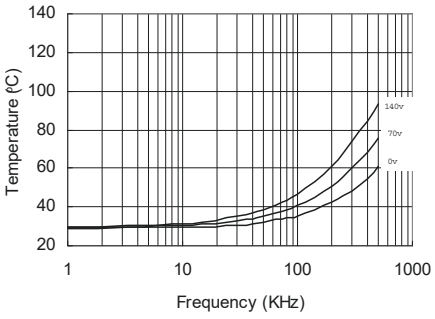


Figure 23. IR2181 vs. Frequency (IRFBC40), $R_{gate}=15\Omega, V_{CC}=15V$

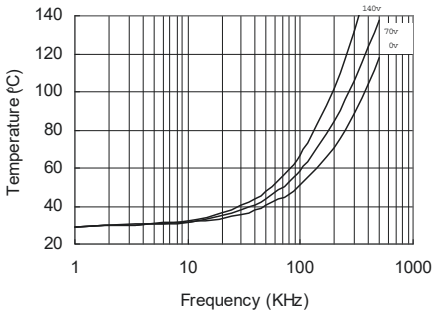


Figure 24. IR2181 vs. Frequency (IRFPE50), $R_{gate}=10\Omega, V_{CC}=15V$

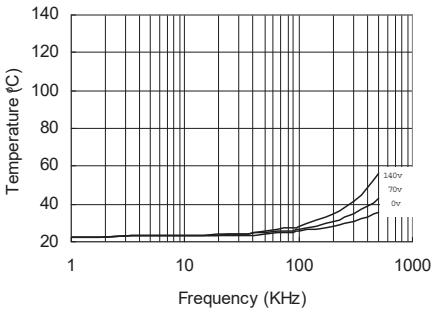


Figure 25. IR21814 vs. Frequency (IRFBC20), $R_{gate}=33\Omega, V_{CC}=15V$

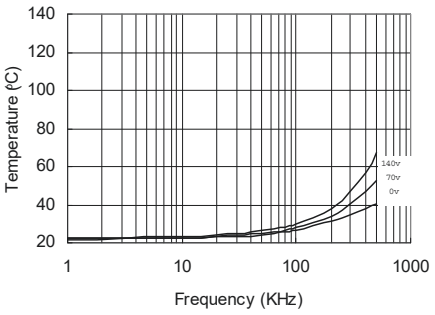


Figure 26. IR21814 vs. Frequency (IRFBC30), $R_{gate}=22\Omega, V_{CC}=15V$

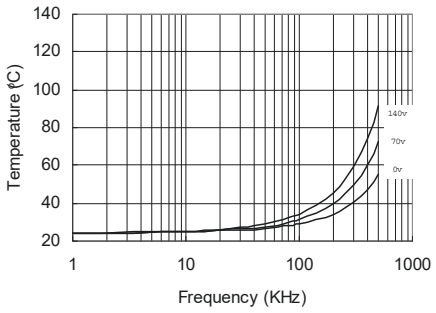


Figure 27. IR21814 vs. Frequency (IRFBC40), $R_{gate}=15\Omega, V_{CC}=15V$

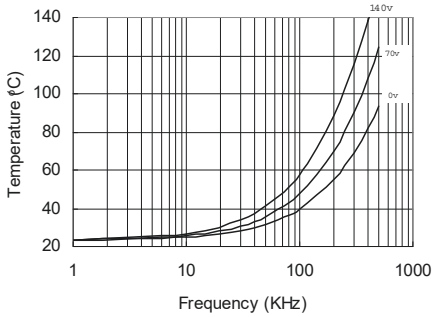


Figure 28. IR21814 vs. Frequency (IRFPE50), $R_{gate}=10\Omega, V_{CC}=15V$

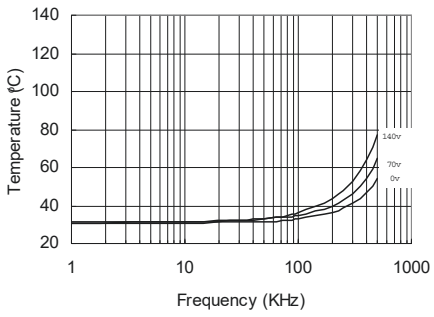


Figure 29. IR2181s vs. Frequency (IRFBC20), $R_{gate}=33\Omega, V_{CC}=15V$

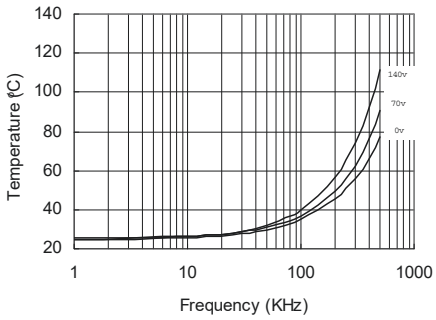


Figure 30. IR2181s vs. Frequency (IRFBC30), $R_{gate}=22\Omega, V_{CC}=15V$

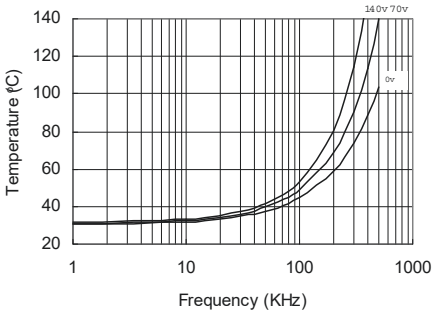


Figure 31. IR2181s vs. Frequency (IRFBC40), $R_{gate}=15\Omega, V_{CC}=15V$

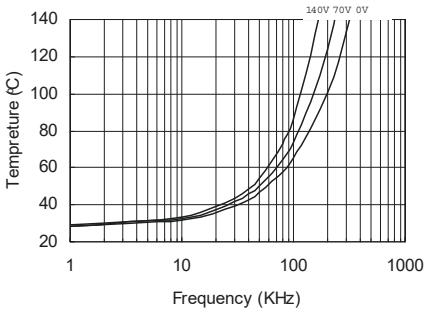


Figure 32. IR2181s vs. Frequency (IRFPE50), R_{gate}=10Ω, V_{CC}=15V

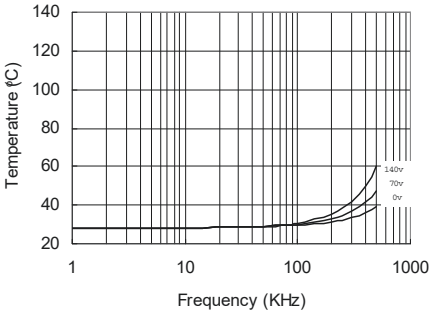


Figure 33. IR21814s vs. Frequency (IRFBC20), R_{gate}=33Ω, V_{CC}=15V

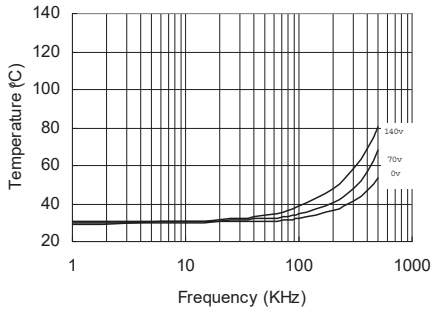


Figure 34. IR21814s vs. Frequency (IRFBC30), R_{gate}=22Ω, V_{CC}=15V

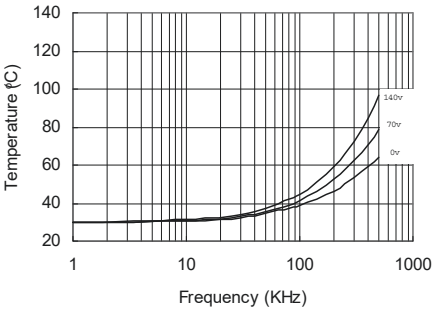


Figure 35. IR21814s vs. Frequency (IRFBC40), R_{gate}=15Ω, V_{CC}=15V

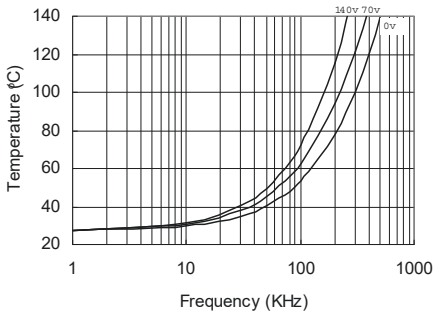
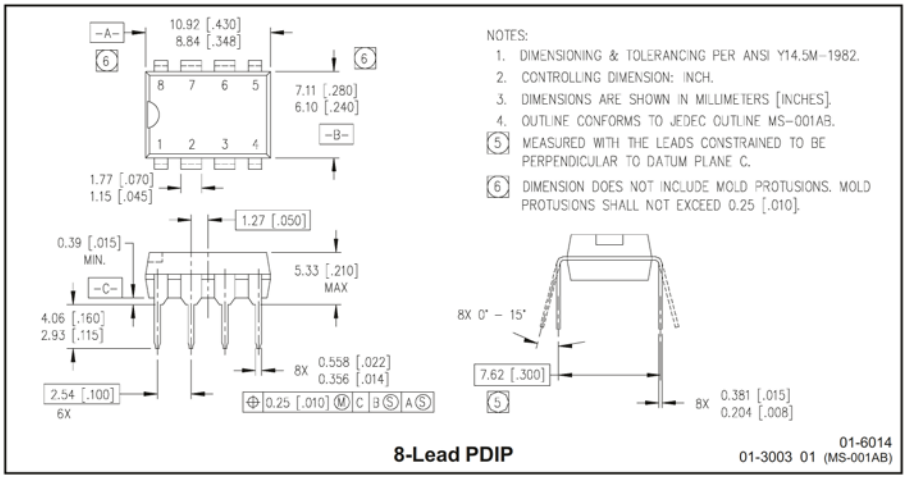
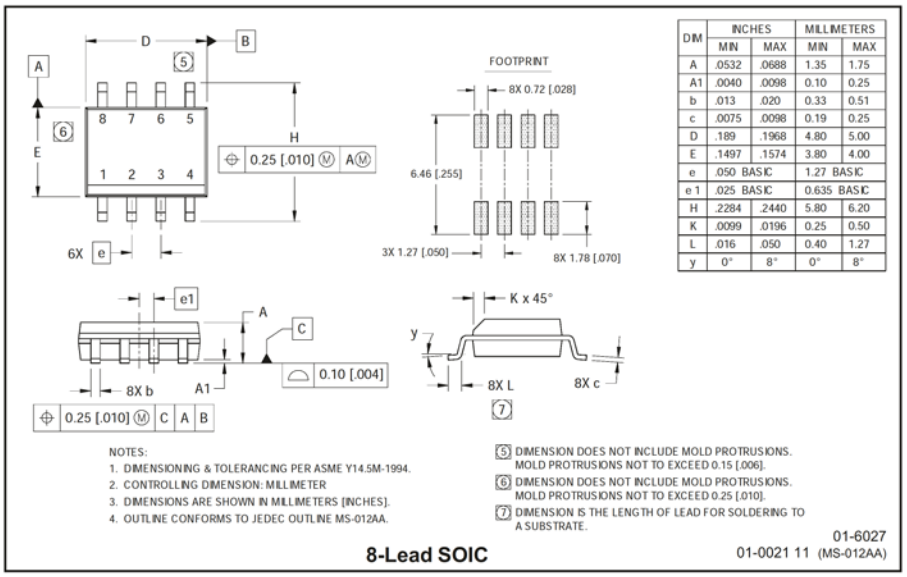


Figure 36. IR21814s vs. Frequency (IRFPE50), R_{gate}=10Ω, V_{CC}=15V



8-Lead PDIP

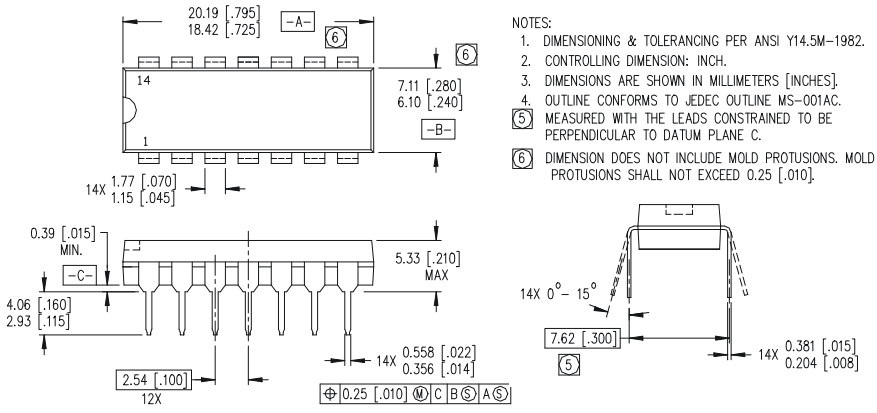
01-6014
01-3003 01 (MS-001AB)



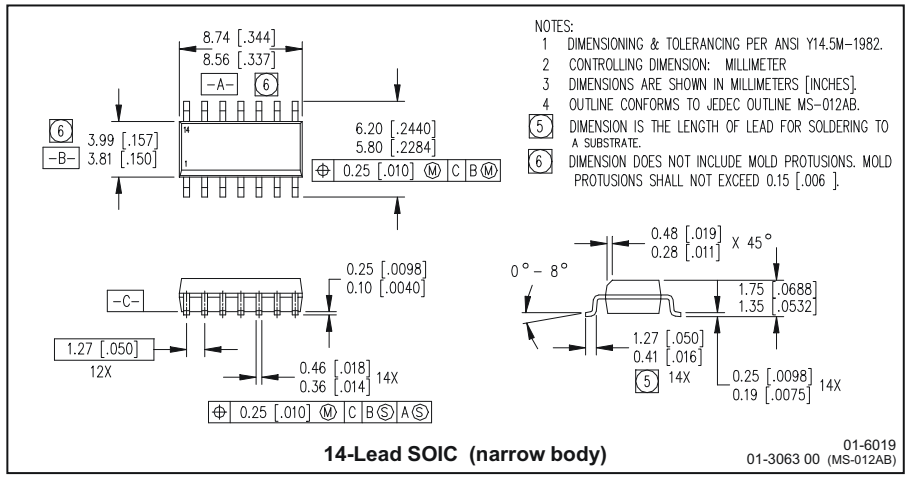
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

8-Lead SOIC

01-6027
01-0021 11 (MS-012AA)

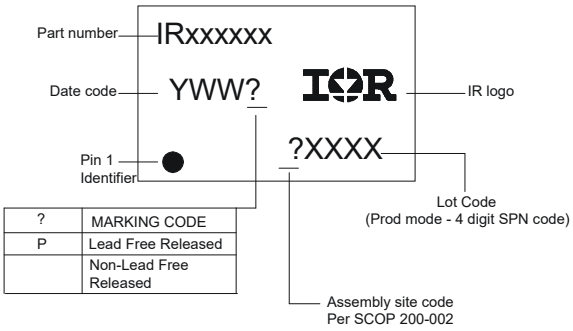


14-Lead PDIP



14-Lead SOIC (narrow body)

LEADFREE PART MARKING INFORMATION



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

ORDER INFORMATION

Basic Part (Non-Lead Free)
8-Lead PDIP IR2184 order IR2184
8-Lead SOIC IR2184S order IR2184S
14-Lead PDIP IR21844 order IR21844
14-Lead SOIC IR21844 order IR21844S

Leadfree Part
8-Lead PDIP IR2184 order IR2184PbF
8-Lead SOIC IR2184S order IR2184SPbF
14-Lead PDIP IR21844 order IR21844PbF
14-Lead SOIC IR21844 order IR21844SPbF

B.7 Power Diode (MBR20200CT)

MBR20200CT

Switch-mode Power Rectifier

Dual Schottky Rectifier

Features and Benefits

- Low Forward Voltage
- Low Power Loss/High Efficiency
- High Surge Capacity
- 175°C Operating Junction Temperature
- 20 A Total (10 A Per Diode Leg)
- This is a Pb-Free Device*

Applications

- Power Supply − Output Rectification
- Power Management
- Instrumentation

Mechanical Characteristics

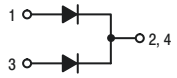
- Case: Epoxy, Molded
- Epoxy Meets UL 94, V−0 @ 0.125 in
- Weight: 1.9 Grams (Approximately)
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads are Readily Solderable
- Lead Temperatures for Soldering Purposes: 260°C Max. for 10 Seconds
- ESD Rating: Human Body Model 3B
  Machine Model C

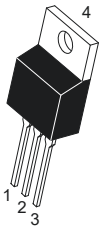
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

http://onsemi.com

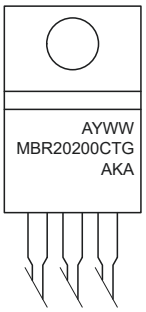
SCHOTTKY BARRIER RECTIFIER 20 AMPERES, 200 VOLTS





TO−220 CASE 221A PLASTIC STYLE 6

MARKING DIAGRAM



A	= Assembly Location
Y	= Year
WW	= Work Week
G	= Pb−Free Package
AKA	= Diode Polarity

ORDERING INFORMATION

Device	Package	Shipping
MBR20200CTG	TO−220 (Pb−Free)	50 Units / Rail

MBR20200CT

MAXIMUM RATINGS (Per Leg)

Rating		Symbol	Value	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage		V_{RRM} V_{RWM} V_R	200	V
Average Rectified Forward Current (T_C = 161°C)	Per Leg Per Package	$I_{F(AV)}$	10 20	A
Peak Repetitive Forward Current per Leg (Square Wave, 20 kHz, T_C = 158°C)		I_{FRM}	20	A
Non-Repetitive Peak Surge Current (Surge Applied at Rated Load Conditions Halfwave, Single Phase, 60 Hz)		I_{FSM}	150	A
Peak Repetitive Reverse Surge Current (2.0 μs, 1.0 kHz)		I_{RRM}	1.0	A
Storage Temperature Range		T_{stg}	−65 to +175	°C
Operating Junction Temperature		T_J	−65 to +175	°C
Voltage Rate of Change (Rated V_R)		dv/dt	10,000	V/μs

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Condition	Symbol	Value	Unit
Maximum Thermal Resistance, Junction-to-Case	Minimum Pad	$R_{\theta JC}$	2.0	°C/W
Maximum Thermal Resistance, Junction-to-Ambient	Minimum Pad	$R_{\theta JA}$	60.0	°C/W

ELECTRICAL CHARACTERISTICS (Per Leg)

Characteristic	Symbol	Min	Typical	Max	Unit
Maximum Instantaneous Forward Voltage (Note 1) (I_F = 10 A, T_J = 25°C) (I_F = 10 A, T_J = 125°C) (I_F = 20 A, T_J = 25°C) (I_F = 20 A, T_J = 125°C)	V_F	 − − − −	 0.80 0.66 0.89 0.76	 0.90 0.80 1.00 0.90	V
Maximum Instantaneous Reverse Current (Note 1) (Rated dc Voltage, T_J = 25°C) (Rated dc Voltage, T_J = 125°C)	I_R	 − −	 0.0002 0.4	 1.0 50	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

DYNAMIC CHARACTERISTICS (Per Leg)

Characteristic	Symbol	Value	Unit
Capacitance (V_R = −5.0 V, T_C = 25°C, Frequency = 1.0 MHz)	C_T	500	pF

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

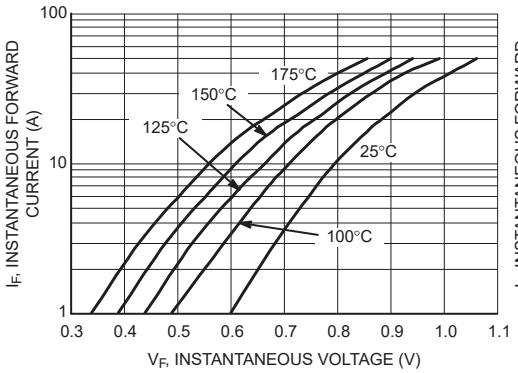


Figure 1. Typical Forward Voltage

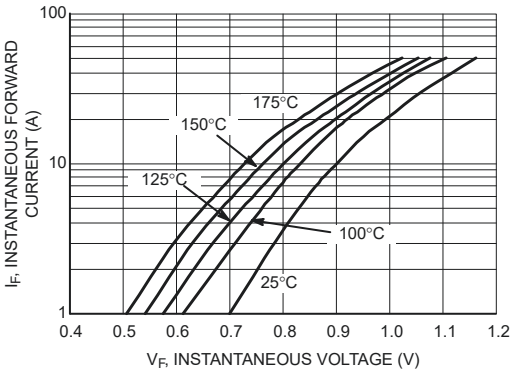


Figure 2. Maximum Forward Voltage

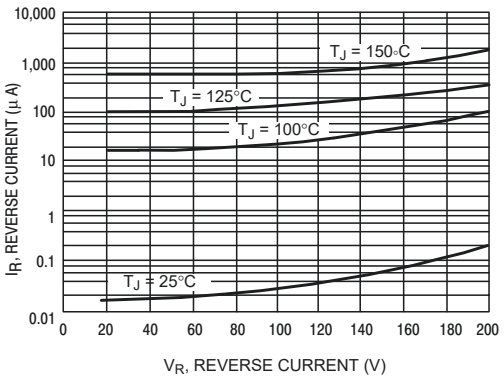


Figure 3. Typical Reverse Current (Per Leg)

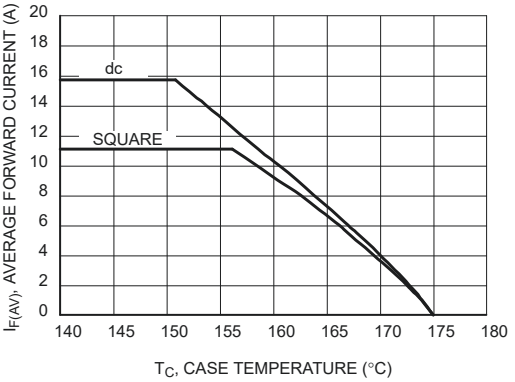


Figure 4. Current Derating, Case, Per Leg

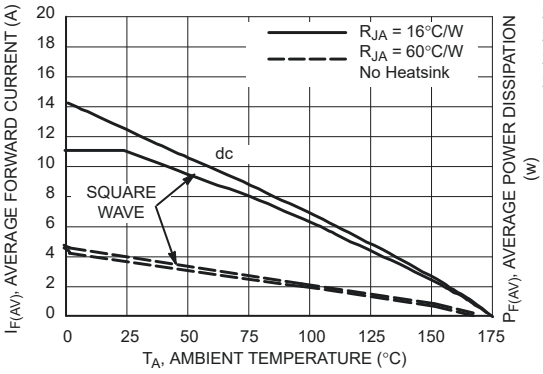


Figure 5. Current Derating, Ambient, Per Leg

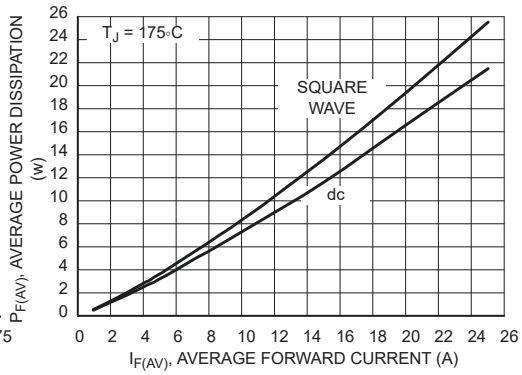


Figure 6. Forward Power Dissipation

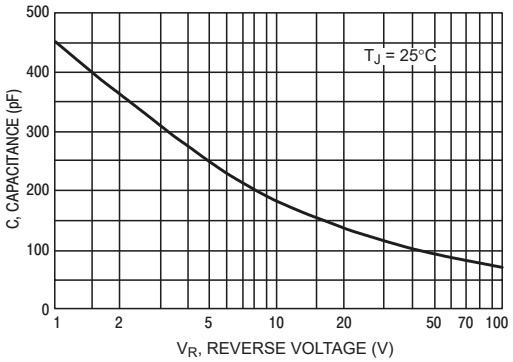


Figure 7. Typical Capacitance (Per Leg)

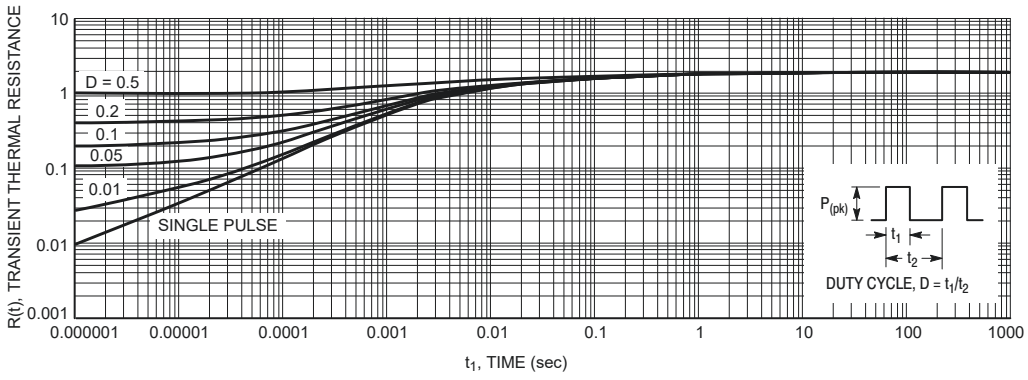
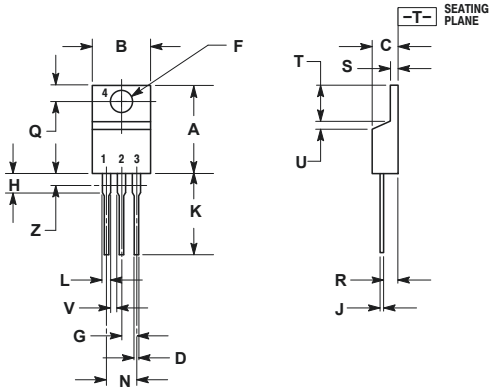


Figure 8. Thermal Response Junction-to-Case

MBR20200CT

PACKAGE DIMENSIONS

TO−220
CASE 221A−09
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

MBR20200CT/D

B.8 Current Sensor (ACS712-5A)

ACS712 Current Sensor

Basic Overview

The ACS712 Current Sensors offered on the internet are designed to be easily used with micro controllers like the Arduino.

These sensors are based on the Allegro ACS712ELC chip.

These current sensors are offered with full scale values of 5A, 20A and 30A.

The basic functional operation of each of these devices is identical. The only difference is with the scale factor at the output as detailed below.

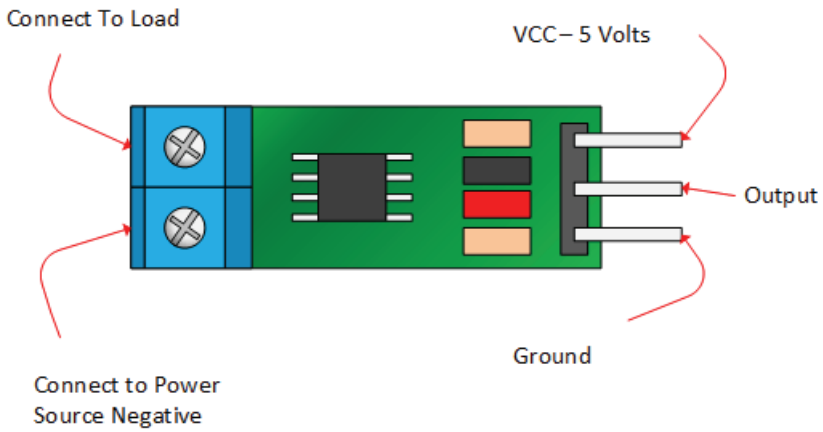
Sensor Specifications

	5A Module	20A Module	30A Module
Supply Voltage (VCC)	5Vdc Nominal	5Vdc Nominal	5Vdc Nominal
Measurement Range	-5 to +5 Amps	-20 to +20 Amps	-30 to +30 Amps
Voltage at 0A	VCC/2 (nominally 2.5Vdc)	VCC/2 (nominally 2.5Vdc)	VCC/2 (nominally 2.5VDC)
Scale Factor	185 mV per Amp	100 mV per Amp	66 mV per Amp
Chip	ACS712ELC-05A	ACS712ELC-10A	ACS712ELC-30A

ACS712 Module Pin Outs and Connections

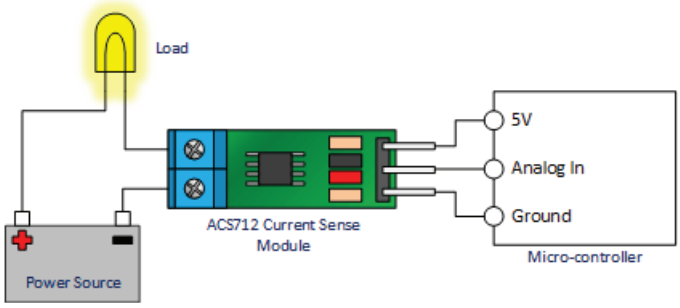
The picture below identifies the pin outs for the ACS172 Modules.

Pay attention to the polarity at the load end of the device. If you are connected as illustrated below, the output will raise. If you connect it opposite of this picture, the output will decrease from the 2.5 volt offset.



Basic Hook Up and Functional Description

As mentioned before, these modules are primarily designed for use with micro-controllers like the Arduino. In those applications, the connections would be as picture below:



If the light bulb shown in the picture above were disconnected, the output of the ACS712 module would be 2.500 volts.

Once connected, the output would be scaled to the current drawn through the bulb. If this were a 5 Amp module and the light bulb pulled 1 Amp, the output of the module would be 2.685 volts.

Now imagine the battery polarity reversed. Using the same 5A module, the output would be 2.315 volts.

IMPORTANT NOTE – This device is a Hall Effect transducer. It should not be used near significant magnetic fields.

B.9 Inductor Core (RM14/I-3C95)

FERROXCUBE

DATA SHEET

RM14/I
RM, RM/I, RM/ILP cores and accessories

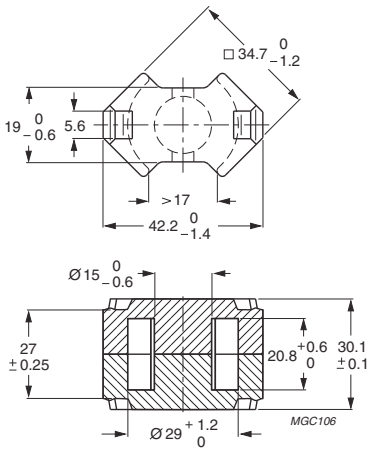
Supersedes data of September 2004 2008 Sep 01

FERROXCUBE
A YAGEO COMPANY

CORE SETS

Effective core parameters

SYMBOL	PARAMETER	VALUE	UNIT
Σ(l/A)	core factor (C1)	0.353	mm^{-1}
V_e	effective volume	13900	mm^3
l_e	effective length	70.0	mm
A_e	effective area	198	mm^2
A_{min}	minimum area	168	mm^2
m	mass of set	≈ 69	g



Dimensions in mm.

Fig.1 RM14/I core set.

Core sets for general purpose transformers and power applications

Clamping force for A_L measurements, 80 ±20 N.

GRADE	A_L (nH)	μ_e	AIR GAP (μm)	TYPE NUMBER
3C90	250 ±3%	≈ 70	≈ 1270	RM14/I-3C90-A250
	315 ±3%	≈ 89	≈ 950	RM14/I-3C90-A315
	400 ±3%	≈ 113	≈ 710	RM14/I-3C90-A400
	630 ±5%	≈ 177	≈ 410	RM14/I-3C90-A630
	1000 ±5%	≈ 281	≈ 240	RM14/I-3C90-A1000
	6600 ±25%	≈ 1850	≈ 0	RM14/I-3C90
3C94	250 ±3%	≈ 70	≈ 1270	RM14/I-3C94-A250
	315 ±3%	≈ 89	≈ 950	RM14/I-3C94-A315
	400 ±3%	≈ 113	≈ 710	RM14/I-3C94-A400
	630 ±5%	≈ 177	≈ 410	RM14/I-3C94-A630
	1000 ±5%	≈ 281	≈ 240	RM14/I-3C94-A1000
	6600 ±25%	≈ 1850	≈ 0	RM14/I-3C94
3C95 des	8130 ±25%	≈ 2290	≈ 0	RM14/I-3C95
3C96 des	5700 ±25%	≈ 1600	≈ 0	RM14/I-3C96
3F3	250 ±3%	≈ 70	≈ 1270	RM14/I-3F3-A250
	315 ±3%	≈ 89	≈ 950	RM14/I-3F3-A315
	400 ±3%	≈ 113	≈ 710	RM14/I-3F3-A400
	630 ±5%	≈ 177	≈ 410	RM14/I-3F3-A630
	1000 ±5%	≈ 281	≈ 240	RM14/I-3F3-A1000
	5700 ±25%	≈ 1600	≈ 0	RM14/I-3F3

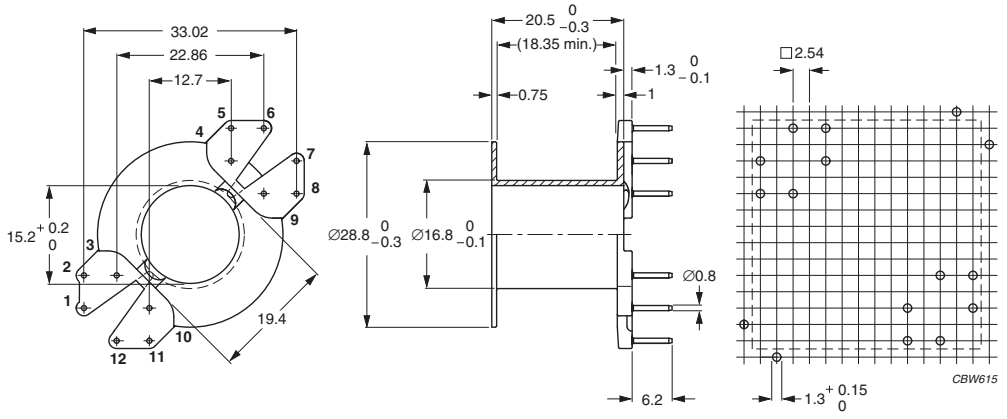
Properties of core sets under power conditions

GRADE	B (mT) at	CORE LOSS (W) at					
	H = 250 A/m; f = 25 kHz; T = 100 °C	f = 25 kHz; B = 200 mT; T = 100 °C	f = 100 kHz; B = 100 mT; T = 100 °C	f = 100 kHz; B = 200 mT; T = 25 °C	f = 100 kHz; B = 200 mT; T = 100 °C	f = 400 kHz; B = 50 mT; T = 100 °C	f = 500 kHz; B = 50 mT; T = 100 °C
3C90	≥315	≤ 1.67	≤ 1.76	–	–	–	–
3C94	≥315	–	≤ 1.4	–	≤ 7.4	–	–
3C95	≥315	–	–	≤ 8.76	≤ 8.34	–	–
3C96	≥340	–	≤ 1.1	–	≤ 5.6	≤ 2.6	≤ 5.2
3F3	≥315	–	≤ 1.55	–	–	≤ 2.65	–

COIL FORMERS

General data

PARAMETER	SPECIFICATION
Coil former material	phenolformaldehyde (PF), glass reinforced, flame retardant in accordance with *"UL 94V-0"*; UL file number E167521(M)
Pin material	copper-tin alloy (CuSn), tin (Sn) plated
Maximum operating temperature	180 °C, *"IEC 60085"*, class H
Resistance to soldering heat	*"IEC 60068-2-20"*, Part 2, Test Tb, method 1B, 350 °C, 3.5 s
Solderability	*"IEC 60068-2-20"*, Part 2, Test Ta, method 1



Dimensions in mm.

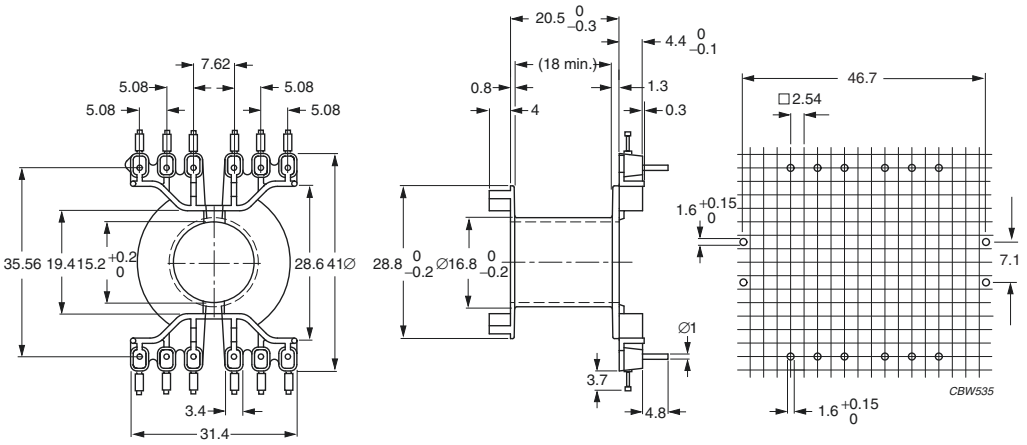
Fig.2 RM14/I coil former; 12-pins.

Winding data and area product for 12-pins RM14/I coil former

NUMBER OF SECTIONS	NUMBER OF PINS	PIN POSITIONS USED	AVERAGE LENGTH OF TURN (mm)	WINDING AREA (mm^2)	WINDING WIDTH (mm)	AREA PRODUCT Ae x Aw (mm^4)	TYPE NUMBER
1	10	1, 2, 3, 4, 6, 7, 9, 10, 11, 12	71	112	18.4	22200	CSV-RM14-1S-10P
1	12	all	71	112	18.4	22200	CSV-RM14-1S-12P

General data

PARAMETER	SPECIFICATION
Coil former material	polybutyleneterephtalate (PBT), glass-reinforced, flame retardent in accordance with *"UL 94V-0"*; UL file number E45329(R)
Pin material	copper-tin alloy (CuSn), tin (Sn) plated
Maximum operating temperature	155 °C, *"IEC 60085"*, class F
Resistance to soldering heat	*"IEC 60068-2-20"*, Part 2, Test Tb, method 1B, 350 °C, 3.5 s
Solderability	*"IEC 60068-2-20"*, Part 2, Test Ta, method 1



Dimensions in mm.

Fig.3 RM14/I coil former; 12-pins (DIL).

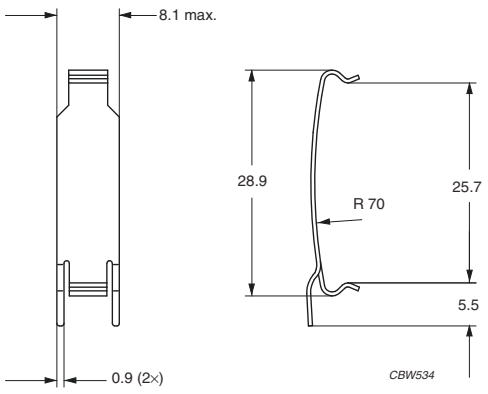
Winding data and area product for 12-pins RM14/I coil former (DIL)

NUMBER OF SECTIONS	AVERAGE LENGTH OF TURN (mm)	WINDING AREA (mm^2)	WINDING WIDTH (mm)	AREA PRODUCT Ae x Aw (mm^4)	TYPE NUMBER
1	71	111	18.0	22000	CPV-RM14/I-1S-12PD

MOUNTING PARTS

General data mounting clip with earth pin

ITEM	SPECIFICATION
Clamping force	≈40 N
Clip material	stainless steel
Clip plating	tin (Sn)
Solderability	*"IEC 60068-2-20"*, Part 2, Test Ta, method 1
Type number	CLI/P-RM14/I



Dimensions in mm.

Fig.4 Mounting clip for RM14/I.

DATA SHEET STATUS DEFINITIONS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS
Preliminary specification	Development	This data sheet contains preliminary data. Ferroxcube reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Ferroxcube reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

DISCLAIMER

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Ferroxcube customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Ferroxcube for any damages resulting from such application.

PRODUCT STATUS DEFINITIONS

STATUS	INDICATION	DEFINITION
Prototype	prot	These are products that have been made as development samples for the purposes of technical evaluation only. The data for these types is provisional and is subject to change.
Design-in	des	These products are recommended for new designs.
Preferred		These products are recommended for use in current designs and are available via our sales channels.
Support	sup	These products are **not** recommended for new designs and may not be available through all of our sales channels. Customers are advised to check for availability.

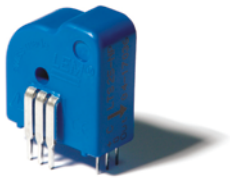
B.10 Current Sensor (LEM-LTS-6-NP)

LEM

Current Transducer LTS 6-NP

For the electronic measurement of currents: DC, AC, pulsed..., with galvanic separation between the primary circuit and the secondary circuit.

I_{PN} = 6 At



Electrical data

I_{PN}	Primary nominal RMS current		6	At
I_{PM}	Primary current, measuring range		0 … ±19.2	At
I_P	Overload capability		250	At
V_{out}	Output voltage (analog) @ I_P		2.5 ±(0.625 × I_P/ I_{PN})	V
	@ I_P = 0		2.5 [1]	V
G	Sensitivity		104.16	mV/A
N_S	Number of secondary turns (±0.1 %)		2000	
R_L	Load resistance		≥ 2	kΩ
R_{IM}	Internal measuring resistance (±0.5 %)		208.33	Ω
TCR_{IM}	Temperature coefficient of R_{IM}		< 50	ppm/K
U_C	Supply voltage (±5 %)		5	V
I_C	Current consumption @ U_C = 5 V	Typical	28 + I_S [2] (V_{out}/R_L)	mA

Accuracy - Dynamic performance data

X	Accuracy @ I_{PN}, T_A = 25 °C		±0.2		%
	Accuracy with R_{IM},@ I_{PN}, T_A = 25 °C		±0.7		%
ε_L	Linearity error		< 0.1		%
			Typ	Max	
TCV_{out}	Temperature coefficient of V_{out} @ I_P = 0	−10 ... +85 °C	80	200	ppm/K
		−40 ... −10 °C		250	ppm/K
TCG	Temperature coefficient of G	−40 ... +85 °C		50 [3]	ppm/K
V_{OM}	Magnetic offset voltage @ I_P = 0,				
	after an overload of 3 × I_{PN}			±0.5	mV
	after an overload of 5 × I_{PN}			±2.0	mV
	after an overload of 10 × I_{PN}			±2.0	mV
t_{ra}	Reaction time @ 10 % of I_{PN}		< 100		ns
t_r	Step response time to 90 % of I_{PN} [4]		< 400		ns
BW	Frequency bandwidth	(0 ... −0.5 dB)	DC … 100		kHz
		(−0.5 ... 1 dB)	DC … 200		kHz

General data

T_A	Ambient operating temperature	−40 … +85	°C
T_S	Ambient storage temperature	−40 … +100	°C
m	Mass	10	g
	Standards	EN 50178: 1997 IEC 60950-1: 2001	

Notes: [1] Absolute value @ T_A = 25 °C, 2.475 < V_{out} < 2.525

[2] I_S = I_P/ N_S

[3] Only due to TCR_{IM}

[4] For a di/dt = 15 A/µs.

Features

- Closed loop (compensated) current transducer using the Hall effect
- Unipolar supply voltage
- Insulating plastic case recognized according to UL 94-V0
- Compact design for PCB mounting
- Incorporated measuring resistance
- Extended measuring resistance.

Advantages

- Excellent accuracy
- Very good linearity
- Low temperature drift
- Optimized response time
- Wide frequency bandwidth
- No insertion losses
- High immunity to external interference
- Current overload capability.

Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Switched Mode Power Supplies (SMPS)
- Power supplies for welding applications.

Application domain

- Industrial.

UL 508: Ratings and assumptions of certification

File # E189713 Volume: 2 Section: 1

Standards

- CSA C22.2 NO. 14-10 INDUSTRIAL CONTROL EQUIPMENT - Edition 11
- UL 508 STANDARD FOR INDUSTRIAL CONTROL EQUIPMENT - Edition 17

Ratings

Parameter	Symbol	Unit	Value
Primary involved potential		V AC/DC	600
Max surrounding air temperature	T_A	°C	85
Primary current	I_P	A	According to series primary currents
Output voltage	V_{out}	V	0 to 5

Conditions of acceptability

When installed in the end-use equipment, consideration shall be given to the following:

1 - These devices must be mounted in a suitable end-use enclosure.
2 - The terminals have not been evaluated for field wiring.
3 - The LTS, LTSR, LTSP Series are intended to be mounted on the printed wiring board of the end-use equipment (with a minimum CTI of 100).
4 - The LTS, LTSR, LTSP Series shall be used in a pollution degree 2 environment.
5 - Low voltage circuits are intended to be powered by a circuit derived from an isolating source (such as a transformer, optical isolator, limiting impedance or electro-mechanical relay) and having no direct connection back to the primary circuit (other than through the grounding means).
6 - The LTS, LTSR, LTSP Series: based on results of temperature tests, in the end-use application, a maximum of 100°C cannot be exceeded at soldering point between primary coil pin and soldering point or on primary bus bar (corrected to the appropriate evaluated max, surrounding air).
7 - For LTS, LTSR, LTSP Series, the secondary sensing circuit was evaluated as the circuit intended to be supplied from a Limited Voltage/Current circuit defined in UL 508 standard.

Marking

Only those products bearing the UL or UR Mark should be considered to be Listed or Recognized and covered under UL's Follow-Up Service. Always look for the Mark on the product.

Current Transducer LTS 6-NP

Insulation coordination

U_d	RMS voltage for AC insulation test, 50 Hz, 1 min	3	kV
$\hat{U}_W$	Impulse withstand voltage 1.2/50 µs	> 8	kV
U_e	Partial discharge extinction RMS voltage @ 10 pC	1.5 Min	kV
d_{Cp}	Creepage distance [1]	15.5	mm
d_{Cl}	Clearance [2]	6.35	mm
CTI	Comparative tracking index (group IIIa)	175	

Notes: [1] On housing
[2] On PCB with soldering pattern UTEC93-703.

Applications examples

According to EN 50178 and IEC 61010-1 standards and following conditions:
- Over voltage category OV 3
- Pollution degree PD2
- Non-uniform field

	EN 50178	IEC 61010-1
d_{Cp}, d_{Cl}, $\hat{U}_W$	Rated insulation voltage	Nominal voltage
Basic insulation	600 V	600 V
Reinforced insulation	300 V	300 V

Safety

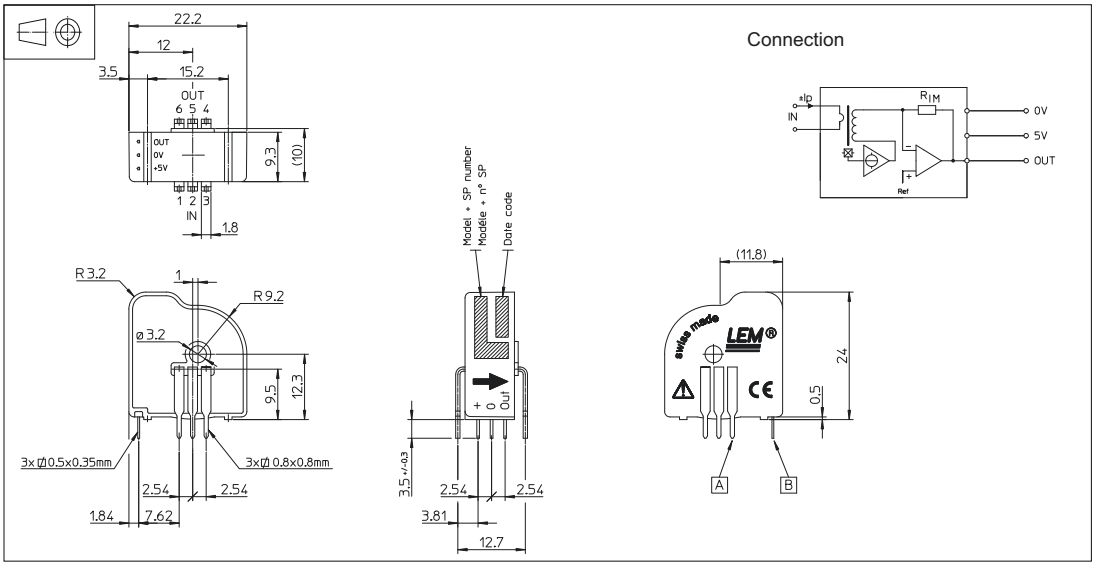
This transducer must be used in limited-energy secondary circuits according to IEC 61010-1.

This transducer must be used in electric/electronic equipment with respect to applicable standards and safety requirements in accordance with the manufacturer's operating instructions.

Caution, risk of electrical shock

When operating the transducer, certain parts of the module can carry hazardous voltage (e.g. primary busbar, power supply). Ignoring this warning can lead to injury and/or cause serious damage.
This transducer is a build-in device, whose conducting parts must be inaccessible after installation. A protective housing or additional shield could be used.
Main supply must be able to be disconnected.

Dimensions LTS 6-NP (in mm)



Number of primary turns	Primary nominal RMS current	Nominal output voltage V_{out}	Primary resistance R_P [mΩ]	Primary insertion inductance L_P [µH]	Recommended connections
1	±6	2.5 ±0.625	0.18	0.013	6 5 4 OUT IN 1 2 3
2	±3	2.5 ±0.625	0.81	0.05	6 5 4 OUT IN 1 2 3
3	±2	2.5 ±0.625	1.62	0.12	6 5 4 OUT IN 1 2 3

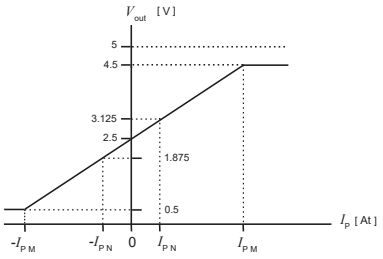
Mechanical characteristics

- General tolerance ±0.2 mm
- Transducer fastening of primary 6 pins 0.8 × 0.8 mm
  Recommended PCB hole 1.3 mm
- Transducer fastening of secondary 3 pins 0.5 × 0.35 mm
  Recommended PCB hole 0.8 mm
- Primary through-hole ⌀ 3.2 mm

Remarks

- V_{out} swings above 2.5 V when I_P flows from terminals 1, 2, 3 to terminals 6, 5, 4 (with the arrow).
- Temperature of the primary conductor should not exceed 100 °C.
- Installation of the transducer must be done unless otherwise specified on the datasheet, according to LEM Transducer Generic Mounting Rules. Please refer to LEM document N°ANE120504 available on our Web site: **Products/Product Documentation.**
- This is a standard model. For different versions (supply voltages, turns ratios, unidirectional measurements...), please contact us.

Output voltage - Primary current



B.11 Power Transistor (2N3055)

NPN Silicon Planar Power Transistor

100V_{CBO}, 15A I_C, TO-3

multicomp PRO

RoHS Compliant

General Purpose Switching and Amplifier Applications

Absolute Maximum Ratings

Description	Symbol	Value	Units
Collector Base Voltage	V_{CBO}	100	V
Collector Emitter Voltage	V_{CEO}	60	
Collector Emitter Voltage(RBE=100W)	V_{CER}	70	
Emitter Base Voltage	V_{EBO}	7	
Collector Current Continuous	I_C	15	A
Base Current	I_B	7	
Power Dissipation @ Tc=25ºC Derate Above 25ºC	P_{TOT}	115 0.657	W W/ºC
Operating and Storage Junction Temperature Range	T_J, T_{STG}	- 65 to +200	ºC

Thermal Resistance

Junction to Case	$R_{th(j-c)}$	1.52	ºC/W

Electrical Characteristics (TC=25ºC unless specified otherwise)

Description	Symbol	Test Condition	Min	Max	Units
Collector Emitter Sustaining Voltage	$V_{CEO(sus)}$*	I_C=200mA, I_B=0	60		
Collector Emitter Sustaining Voltage	$V_{CER(sus)}$*	I_C=200mA, R_{BE}=100Ω	70		
Collector Cut off Current	I_{CEX}	V_{CE}=100V, V_{BE}=(off)=1.5V Tc=150ºC V_{CE}=100V, V_{BE}=(off)=1.5V		1 5	mA
Collector Cut off Current	I_{CEO}	V_{CE}=30V, I_B=0		0.7	mA
Emitter Cut off Current	I_{EBO}	V_{BE}=7V, I_C=0		5	mA
Collector Emitter Saturation Voltage	$V_{CE(Sat)}$ *	I_C=4A, I_B=400mA I_C=10A, I_B=3.3A		1.1 3	V
Base Emitter on Voltage	$V_{BE(on)}$ *	I_C=4A, V_{CE}=4V		1.5	V
DC Current Gain	h_{FE}*	I_C=4A, V_{CE}=4V I_C=10A, V_{CE}=4V	20 5	80	

*Pulse Test: Pulse Width <300ms, Duty Cycle <2%

NPN Silicon Planar Power Transistor
100V_{CBO}, 15A I_C, TO-3

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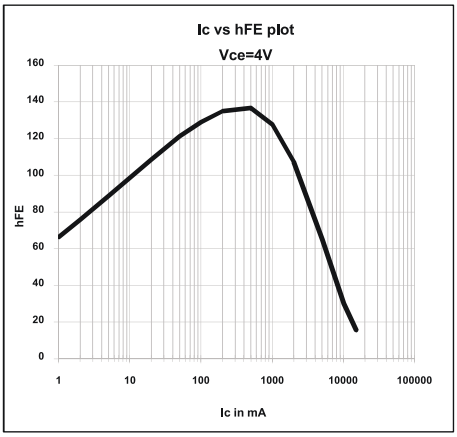
Second Breakdown

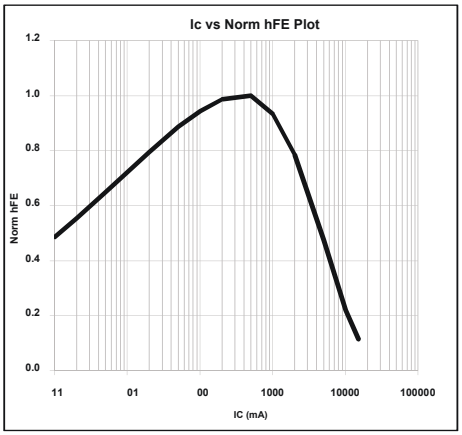
Description	Symbol	Test Condition	Min	Max	Units
Second Breakdown Collector Current with Base Forward Biased	Is/b	V_{CE}=40V, t=1 s, Nonrepetitive	2.87		A

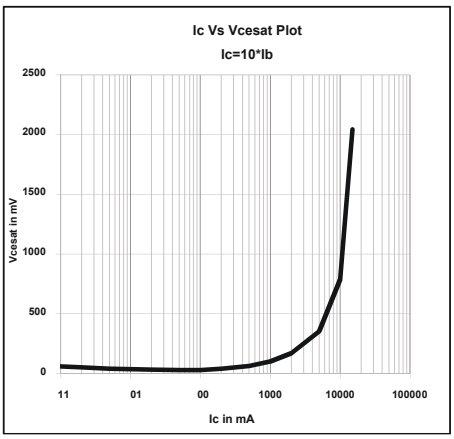
Dynamic Characteristics

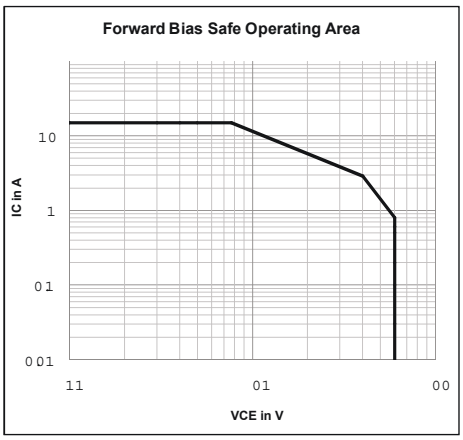
Current Gain - Bandwidth Product	f_T	I_C=0.5A, V_{CE}=10V, f=1MHz	2.5		MHz
Small Signal Current Gain	h_{FE}	I_C=1A, V_{CE}=4V, f=1kHz	15	120	
Small Signal Current Gain Cutoff Frequency	f_{HFE}	I_C=1A, V_{CE}=4V, f=1kHz	10		kHz

Characteristics Plots









NPN Silicon Planar Power Transistor

100V_{CBO}, 15A I_C, TO-3

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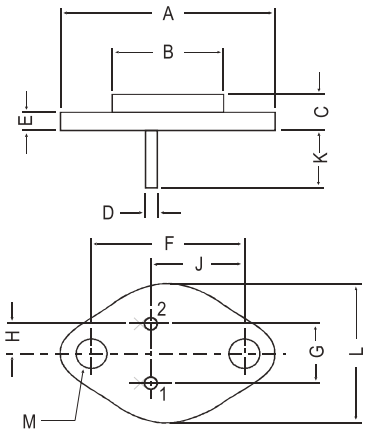
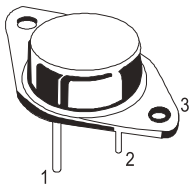
TO-3 Metal Can Package



Dim	Min.	Max.
A	—	39.37
B	—	22.22
C	6.35	8.5
D	0.96	1.09
E	—	1.77
F	29.9	30.4
G	10.69	11.18
H	5.2	5.72
J	16.64	17.15
K	11.15	12.25
L	—	26.67
M	3.84	4.19

Dimensions : Millimetres



Pin Configuration
1. Base
2. Emitter
3. Collector

Part Number Table

Description	Part Number
NPN Silicon Planar Power Transistor, 100 V_{CBO}, 15A I_C, TO-3	2N3055

B.12 Switching Transistor (2N2219A)

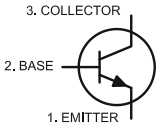
NPN Silicon Planar Switching Transistor
40V_{CEO}, 800mA I_C

multicomp PRO

TO-39

RoHS Compliant

NPN



Absolute Maximum Ratings

Description	Symbol	Value	Unit
Collector Emitter Voltage	V_{CEO}	40	V
Collector Base Voltage	V_{CBO}	75	V
Emitter Base Voltage	V_{EBO}	6	V
Collector Current Continuous	I_C	800	mA
Power Dissipation at T_A = 25°C Derate above 25°C	P_D	800 4.57	mW mW/°C
Power Dissipation at T_C = 25°C Derate Above 25°C	P_D	3 17.15	W mW/°C
Operating and Storage Junction Temperature Range	Tj, Tstg	- 65 to +200	°C

Electrical Characteristics: (T_A = +25°C Unless otherwise specified)

Description	Symbol	Test Conditions	Min	Max	Unit
Collector -Emitter Voltage	V_{CEO}	I_C = 10mA, I_B = 0	40	-	V
Collector Base Voltage	V_{CBO}	I_C = 100µA, I_E = 0	75	-	V
Emitter Base Voltage	V_{EBO}	I_E = 100µA, I_C = 0	6	-	V
Collector Cutoff Current	I_{CBO} I_{CEX}	V_{CB} = 60V, I_E = 0 V_{CB} = 60V, I_E = 0, T_A = 150°C V_{CE} = 60V, V_{EB} = 3V	- - -	10 10 10	nA µA nA
Emitter-Cut off Current	I_{EBO}	V_{EB} = 3V, I_C = 0	-	10	nA
Base-Cut off Current	I_{BL}	V_{CE} = 60V, V_{EB} = 3V	-	20	nA
Collector Emitter Saturation Voltage	$V_{CE(Sat)}$*	I_C = 150mA, I_B = 15mA I_C = 500mA, I_B = 50mA	-	0.3 1	V
Base Emitter Saturation Voltage	$V_{BE(Sat)}$*	I_C = 150mA, I_B = 15mA I_C = 500mA, I_B = 50mA	-	0.6-1.2 2	V

Description	Symbol	Test Conditions	Values	Unit
DC Current Gain	h_{FE}	I_C = 0.1mA, V_{CE} = 10V I_C = 1mA, V_{CE} = 10V I_C = 10mA, V_{CE} = 10V T_A = 55°C I_C = 10mA, V_{CE} = 10V I_C = 150mA, V_{CE} = 10V I_C = 150mA, V_{CE} = 1V I_C = 500mA, V_{CE} = 10V	>35 >50 >75 >35 100-300 >50 >40	

NPN Silicon Planar Switching Transistor
40V_{CEO}, 800mA I_C

multicomp PRO

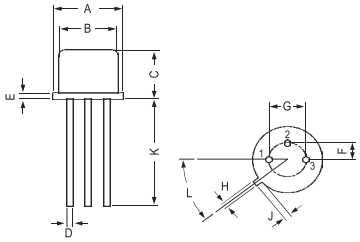
Description	Symbol	Test Conditions	Values	Unit
Dynamic Characteristics				
Small Signal Current Gain	hfe	ALL f = 1kHz I_C = 1mA, V_{CE} = 10V I_C = 10mA, V_{CE} = 10V	 50 - 300 75-375	
Input Impedance	hie	I_C = 1mA, V_{CE} = 10V I_C = 10mA, V_{CE} = 10V	2 - 8 0.25-1.25	kΩ
Voltage Feedback Ratio	hre	I_C = 1mA, V_{CE} = 10V I_C = 10mA, V_{CE} = 10V	<8 <4	x10-4
Out put Admittance	hoe	I_C = 1mA, V_{CE} = 10V I_C = 10mA, V_{CE} = 10V	5 - 35 25 - 200	umhos
Collector Base Time Constant	rb'Cc	I_E = 20mA, V_{CB} = 20V f = 31.8MHz	<150	ps
Real Part Common-Emitter High Frequency Input Impedance	Re(hie)	I_C = 20mA, V_{CE} = 20V f=300MHz	<60	Ω
Noise Figure	NF	I_C = 100μA, V_{CE} = 10V Rs = 1kohms, f = 1kHz	<4	dB
Dynamic Characteristics				
Transistors Frequency	ft	I_C = 20mA, V_{CE} = 20V f = 100MHz	>300	MHz
Out-Put Capacitance	Cob	V_{CB} = 10V, I_E = 0 f = 100kHz	<8	pF
Input Capacitance	Cib	V_{EB} = 0.5V, I_C = 0 f = 100kHz	<25	pF
Switching Time				
Delay time	td	I_C = 150mA, I_{B1} = 15mA	<10	ns
Rise time	tr	V_{CC} = 30V, V_{BE} = 0.5V	<25	ns
Storage time	ts	I_C = 150mA	<225	ns
Fall time	tf	I_{B2} = 15mA, V_{CC} = 30V	<60	ns

*Pulse Condition: Pulse Width=300μs, Duty Cycle=2%

NPN Silicon Planar Switching Transistor
40V$_{CEO}$, 800mA I_C

multicomp PRO

TO-39 Metal Can Package



Dim.	Min.	Max.
A	8.5	9.39
B	7.74	8.5
C	6.09	6.6
D	0.4	0.53
E	-	0.88
F	2.41	2.66

Dim.	Min.	Max.
G	4.82	5.33
H	0.71	0.86
J	0.73	1.02
K	12.7	-
L	42 Deg.	48 Deg.

Dimensions : Millimetres

Part Number Table

Description	Part Number
NPN Silicon Planar Switching Transistor, 40V, 800mA, TO-39	2N2219A

B.13 Switching Transistor (BC33725TA)

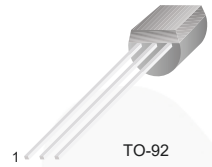
FAIRCHILD

October 2014

BC337 / BC338
NPN Epitaxial Silicon Transistor

Features

- Switching and Amplifier Applications
- Suitable for AF-Driver Stages and Low-Power Output Stages
- Complement to BC327 / BC328



TO-92

1. Collector 2. Base 3. Emitter

Ordering Information

Part Number	Top Mark	Package	Packing Method
BC33716BU	BC33716	TO-92 3L	Bulk
BC33716TA	BC33716	TO-92 3L	Ammo
BC33716TFR	BC33716	TO-92 3L	Tape and Reel
BC33725BU	BC33725	TO-92 3L	Bulk
BC33725TA	BC33725	TO-92 3L	Ammo
BC33725TAR	BC33725	TO-92 3L	Ammo
BC33725TF	BC33725	TO-92 3L	Tape and Reel
BC33725TFR	BC33725	TO-92 3L	Tape and Reel
BC33740BU	BC33740	TO-92 3L	Bulk
BC33740TA	BC33740	TO-92 3L	Ammo
BC33825TA	BC33825	TO-92 3L	Ammo

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter		Value	Unit
V_{CES}	Collector-Emitter Voltage	BC337	50	V
		BC338	30	
V_{CEO}	Collector-Emitter Voltage	BC337	45	V
		BC338	25	
V_{EBO}	Emitter-Base Voltage		5	V
I_C	Collector Current (DC)		800	mA
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		-55 to 150	°C

Thermal Characteristics[1]

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
P_D	Power Dissipation	625	mW
	Derate Above 25°C	5.0	mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	200	°C/W

Note:

1. PCB size: FR-4, 76 mm x 114 mm x 1.57 mm (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

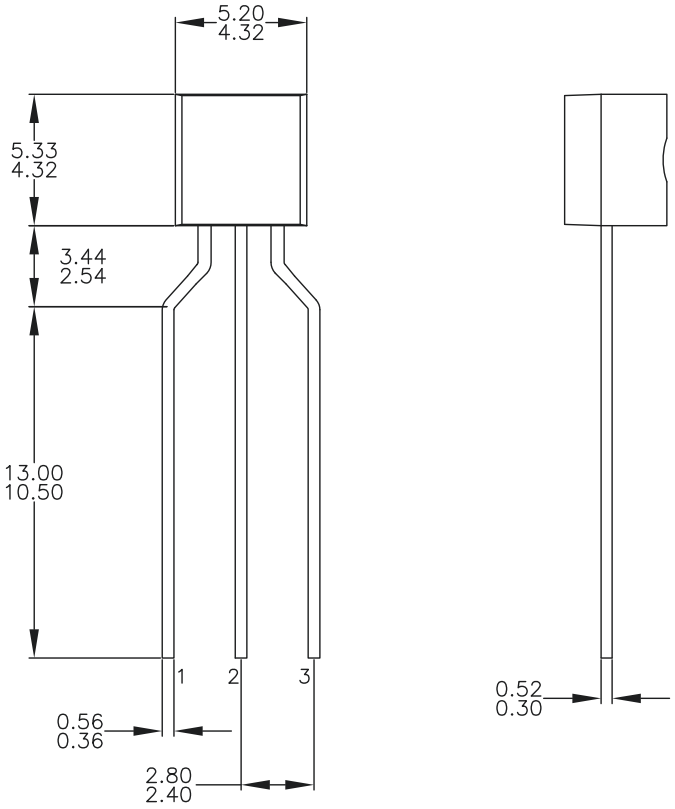
Electrical Characteristics

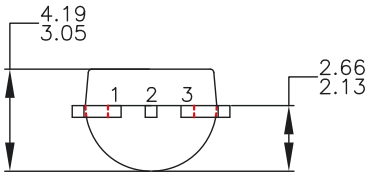
Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Unit
BV_{CEO}	Collector-Emitter Breakdown Voltage	BC337	I_C = 10 mA, I_B = 0	45			V
		BC338		25			
BV_{CES}	Collector-Emitter Breakdown Voltage	BC337	I_C = 0.1 mA, V_{BE} = 0	50			V
		BC338		30			
BV_{EBO}	Emitter-Base Breakdown Voltage		I_E = 0.1 mA, I_C = 0	5			V
I_{CES}	Collector Cut-Off Current	BC337	V_{CE} = 45 V, I_B = 0		2	100	nA
		BC338	V_{CE} = 25 V, I_B = 0		2	100	
h_{FE1}	DC Current Gain		V_{CE} = 1 V, I_C = 100 mA	100		630	
h_{FE2}			V_{CE} = 1 V, I_C = 300 mA	60			
V_{CE}(sat)	Collector-Emitter Saturation Voltage		I_C = 500 mA, I_B = 50 mA			0.7	V
V_{BE}(on)	Base-Emitter On Voltage		V_{CE} = 1 V, I_C = 300 mA			1.2	V
f_T	Current Gain Bandwidth Product		V_{CE} = 5 V, I_C = 10 mA, f = 50 MHz		100		MHz
C_{ob}	Output Capacitance		V_{CB} = 10 V, I_E = 0, f = 1 MHz		12		pF

h_{FE} Classification

Classification	16	25	40
h_{FE1}	100 ~ 250	160 ~ 400	250 ~ 630
h_{FE2}	60 ~	100 ~	170 ~





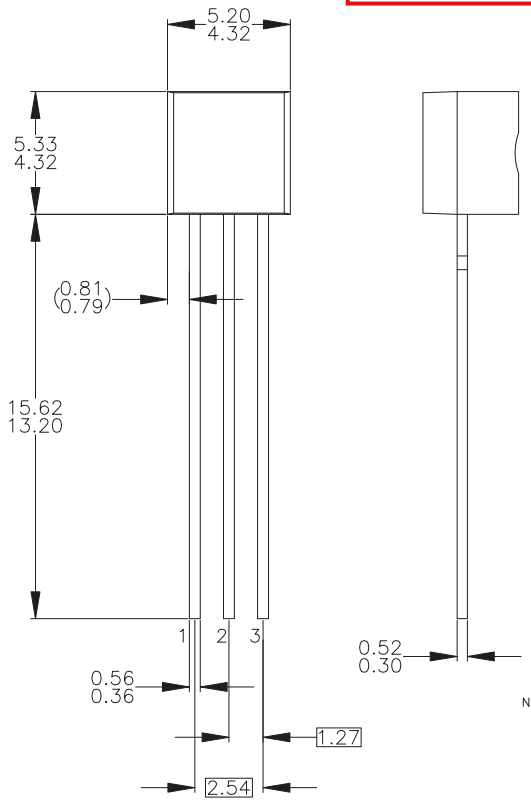
NOTES: UNLESS OTHERWISE SPECIFIED

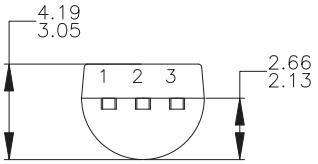
A. DRAWING CONFORMS TO JEDEC MS-013, VARIATION AC.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5M-2009.
D. DRAWING FILENAME: MKT-ZA03FREV3.
E. FAIRCHILD SEMICONDUCTOR.

APPROVED
July-14-2008

REVISIONS

NO.	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL.	MAR.4'96	RP
B	RDRW AS PER STD DWG TEMPLATE. CHG DIM REF FR DUAL DIM INCH[MM] TO SINGLE DIM MM. CHG LD PITCH DIM FR 1.14–1.40 TO 1.27 BSC. ADD DIM 2.54 BSC. CHG PKG WIDTH DIM FR 4.32– 4.70 TO 4.32–4.83; CHG PKG HEIGHT DIM FR 4.32–4.70 TO 4.32–4.78; CHG LD THICK DIM FR 0.30– 0.48 TO 0.30–0.52; DAMBAR–PKG DIM FR 1.27–1.65 TO 0.90–1.65; LD LGH DIM FR 14.47–15.64 TO 14.47–15.62; PKG DIM: 1.02–1.52 TO 0.92–1.52, 3.81–4.45 TO 3.40–4.80; NOTE 2: ADD DMOS "M" OPT'N AND LEGEND; NOTE B PKG 94 JFET OPT'N: CHG D TO S, CHG S TO D. ADD NOTE C; MOVE NOTE B INFO FR PKG 97&98 TO NEW NOTE D.	4OCT1999	RCM/MRG
3	CHG LD LEN FR $\frac{15.61}{15.37}$ TO $\frac{15.65}{15.39}$; CHG MOLD BODY HT FR $\frac{4.32}{4.06}$ TO $\frac{4.32}{4.83}$; CHG PKG EDGE TO LD EDGE DIST FR (0.81) TO $\frac{(0.84)}{(0.76)}$; CHG MOLD BODY WIDTH FR $\frac{4.32}{4.06}$ TO $\frac{4.32}{3.94}$; ADD PKG THICKNESS DIM 'E'; CHG 'S' DIM FR $\frac{2.41}{2.15}$ TO $\frac{2.41}{2.16}$; REMOVE DAMBAR & EJECTOR PIN LOCATOR FEATURES & DIMENSIONS; REMOVE MOLDED SURFACE & DRAFT ANGLE DIMS; ADD NOTE ON JEDEC REFERENCE; ADD NOTE ON ASME Y14.5M–1994; REMOVE NOTE ON L342 OPTION; ADD NOTE ON DWG FILENAME.	12FEB08	BMR/FSCP





NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO–92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M–1994.
D) TO–92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:
P – BIPOLAR
F – JFET
M – DMOS
E – EMITTER
B – BASE
C – COLLECTOR
D – DRAIN
S – SOURCE
G – GATE

E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT–ZA03DREV3.

APPROVALS	DATE
DRAWN: J.U. COMPARATIVO JR.	03APR2008
CHECKED: L. GALERA	
APPROVED: M.R. GESTOLE	
G.S. BAJE	

PROJECTION: INCH [MM]

FAIRCHILD SEMICONDUCTOR™

3LD,TO–92,MOLDED
STD STRAIGHT LD
(NO EOL CODE)

SCALE	SIZE	DRAWING NUMBER	REV
1:1	N/A	MKT–ZA03D	3

FORMERLY: N/A SHEET : 1 OF 1

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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