Electro-Thermal Modelling and Lifetime Evaluation of Power MOSFETs and Converters

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I would like to dedicate this thesis to my loving parents.

Declaration

I, Tian Cheng declare that this thesis, is submitted in fulfilment of the requirements for the award of Doctor of Philosophy, in the Faculty of Engineering and Information Technology at the University of Technology Sydney.

This thesis is wholly my own work unless otherwise referenced or acknowledged. In addition, I certify that all information sources and literature used are indicated in the thesis.

This document has not been submitted for qualifications at any other academic institution.

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Abstract

Due to the ongoing pursuit of high-density power supplies, thermal management has become one of the most critical issues to consider during the design phase for stable and efficient operation. Therefore, this thesis implements a series of thermally related investigations such as electro-thermal modelling techniques, device lifetime prediction, and reliability assessments on cascaded H-bridge (CHB) converter-based three-phase applications.

Firstly, two electro-thermal modelling techniques are proposed for a converter. Significant efforts and progress have been made in developing electro-thermal models (ETMs) for power semiconductors and passive components individually. However, very few have considered building an ETM for a whole converter to make it more realistic in terms of converter design. Hence, in this thesis, an ETM and an electro-thermal averaged model (ETAM) are proposed for a boost converter as examples. Both the simulation and experimental results are given and compared to verify the proposed solutions. An improved electrical performance estimation and fairly accurate temperature prediction can be achieved for both models.

Secondly, a comprehensive MOSFET model that enables electro-thermal modelling, aging, and lifetime estimation on an LTspice® circuit simulator is proposed. This model is also concise as it eliminates the need for multiple software platforms and is comprised of simple electrical circuits. This work is motivated by the fact that power MOSFETs have relatively low reliability as compared to other power components but have high penetration in current power systems. Therefore, it is essential to monitor their state of health to ensure system reliability. Additionally, the aging of a MOSFET is not considered in most reported

work but has an impact on device lifetime. Based on these concerns, the comprehensive MOSFET model is proposed. High-stress thermal cycling and long-term random mission profiles are applied to verify the correctness of the model. An accelerated aging trend can be observed in the long-term mission profile simulation, which is in agreement with the theory. Additionally, the fast simulation speed indicates that the proposed method is a good simulation/analytical tool to implement a long-term mission profile reliability assessment.

Thirdly, a circuit-based rainflow counting algorithm is elaborated aiming to improve the thermal cycle counting accuracy for the comprehensive MOSFET model proposed above. The rainflow counting algorithm is gaining popularity for its low relative error in fatigue analysis and device lifetime estimation. Nevertheless, the offline operation limits the device in considering other parameters, such as aging and the current state of health in the lifetime estimation, as it requires a complete loading profile to run recursive comparisons. This work proposes to tackle the issue and integrate it into a circuit simulator. Results show that the proposed method improves the counting accuracy, with an averaged error of 3.5% over that of the half-cycle counting which is 24.4% under different load stresses and length conditions, and it can be improved still further.

Finally, with the ETM and the lifetime assessment methodology outlined above, Wye (Y)- and Delta (Δ)-connected 5-level CHB converter-based three-phase systems are compared. The comparisons are from electrical, thermal, and lifespan aspects, particularly when the two systems deal with unbalanced power generation among phases. Recent studies have pointed out the superior power balancing capability of Δ- over Y-connection with zero sequence injection (ZSI). However, few studies have considered this from the reliability point of view, as ZSI has different influences on the two configurations. Reported results have verified that even though the Δ-connection can handle more severely unbalanced power, it will not only lead to an unequalled stress distribution among phases but may also overstress devices in some cases. However, the Y-configuration does not have this issue. Consequently, there is a

trade-off between electrical and thermal operation which requires careful consideration when selecting the best configuration to deal with power imbalances.

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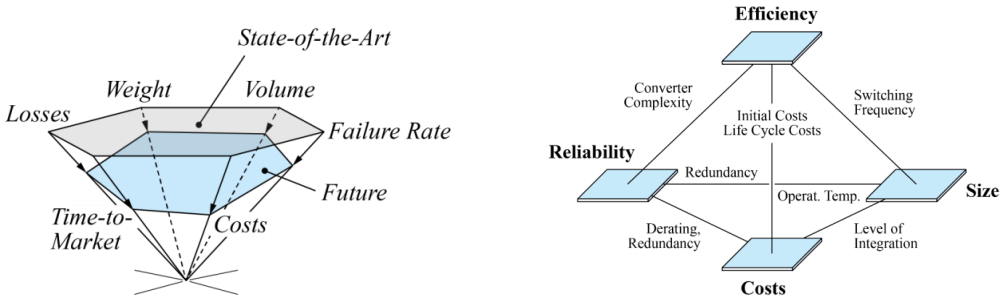
Chapter 1

Introduction

1.1 Background

Thermal management is one of the most critical concerns in power converter design. Future power converters are desired to have a high power density, which is defined as the ratio of the converter output power with respect to its volume. The power density has doubled every decade since 1970 with the progress in power semiconductor devices and packaging technologies, such as the introduction of wide bandgap (WBG) materials [1].However, it is suggested that cooling concepts, passive components and the interconnection technologies could be the limiting factors in power density's future development. A recent talk on discussing the power electronics design 4.0 is presented in [2]. State-of-the-art performance of the current power electronics has been analyzed and shown in Fig. 1.1a, together with indicators on areas that need to be put effort into to improve the future designs, including the reduction of power losses, weight, volume, failure rate, cost, and time-to-market. Additionally, the challenge of optimizing the future design by making trade-offs among efficiency, reliability, costs, and size are discussed and evaluated is also highlighted in Fig. 1.1b.

In addition, thermal management is an important consideration for stable and efficient power supply operation. This is partly due to renewable energy-related applications such



(a) (b)

Fig. 1.1 Power electronics design 4.0 from [2] (a) State-of-the-art of current power electronics and the desired future design. (b) Challenges in optimizing converter/inverter design.

as power converters/inverters in photovoltaic (PV) and wind farms, which have to handle sophisticated loading profiles (e.g. wind speed related long-term profiles, turbine mechanical system related medium-term profiles and load current alternating related short-term profiles [3]), making safe operation a great concern. Moreover, from an economic point of view, it is essential to know the state of health of power devices to properly schedule maintenance, and to avoid the downtime of power supplies and any catastrophic failures. With these concerns in mind, reliability assessment and lifetime prediction of power supplies have gained great attention and are being widely explored. Other related work, such as active thermal control, is also of interest [4]-[7] to facilitate manipulating device temperatures to not only push the power electronics systems to a higher power density level, but also to ensure or enhance their lifespan and reliability. Actions to reduce power losses, lower the temperature cycles, or redistribute the losses and etc. of power devices, for example, can be taken to addresses these goals.

To sum up, the main thermal-related areas and applications can be summarized into three categories, namely, active thermal control [4]-[7], high power density converter/inverter design and optimization [8]-[10], and lifetime estimation and reliability assessment [11]-[15]. This research focuses on the first two applications, and conducts a series of investigations. To study these issues, it is essential to understand the impacts of temperature on the electrical

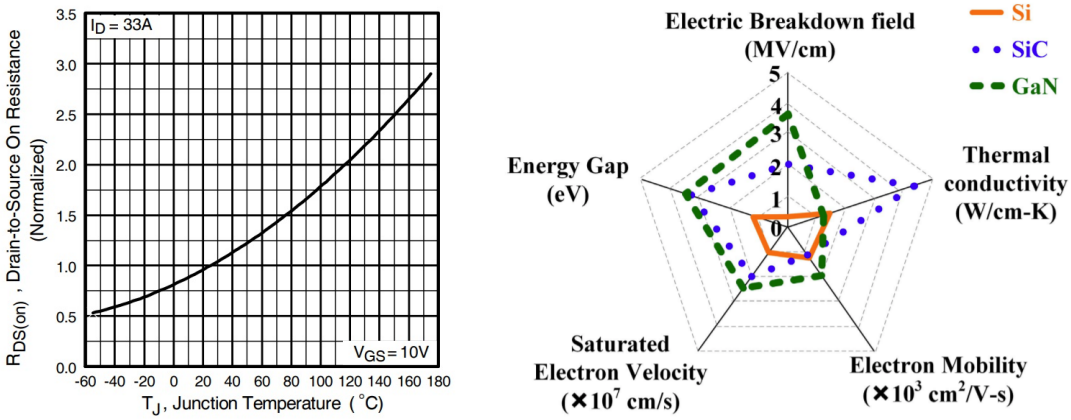
characteristics of both active and passive power components, and are discussed in Section 1.2. The principle of power device lifetime estimation is introduced in Section 1.3, including the power semiconductor failure mechanism, lifetime analytical model, and lifetime estimation methodology.

1.2 Characteristics of Active and Passive power Components

1.2.1 Power semiconductors

Power semiconductor devices, such as MOSFETs and diodes are highly sensitive to temperature changes. An increase in temperature would degrade their electrical performances. Take MOSFET on-state resistance $R_{ds,on}$ and diode forward voltage V_F as examples. Fig. 1.2a shows the normalised on-state resistance with respect to the temperature of an IRF540N power MOSFET from Infineon Technologies [16]. The normalised resistance at 25°C is 1, and the value is almost doubled at 125°C. With the actual resistance at 25°C, which is 44 mΩ, it is expected that the $R_{ds,on}$ is increased to 90 mΩ at 125°C. The corresponding conduction losses of this MOSFET operated in a boost converter with a 10A input current and 0.5 duty cycle at these two temperatures are 2.2W and 4.5W, respectively. Thus, the conclusion can be made that, the losses caused by $R_{ds,on}$ lead to the rise of device temperature, which will in turn incur a further increase in power losses. In contrast to Si devices, WBG devices, such as Silicon Carbide (SiC) and Gallium Nitride (GaN) are more promising. Summarized comparison of Si, SiC, and GaN device properties from [17] is shown in Fig. 1.2b. As can be observed, WBG devices are beneficial due to their material properties, especially the ON-resistance is reduced due to the higher breakdown field and electron mobility as compared to the conventional Silicon (Si) devices. These allow a higher current conducting capability with a smaller die size. The SiC device shows a superior thermal conductivity

performance, which makes it attractive in high-temperature applications. On the contrary, even though the GaN devices have advantages in high frequency and efficiency, the thermal management is more challenging than for SiC devices.



(a) (b)

Fig. 1.2 (a) Normalized drain-to-source on-resistance versus junction temperature of an IRF540N silicon MOSFET. From [16]. (b) Comparison of Si, SiC, and GaN power semiconductors. From [17].

Similarly, the electrical parameters of diodes, such as the forward voltage V_F and series resistance, are also temperature-dependent. The forward voltage characteristics vs temperature of MBR20100CT from ON Semiconductor is shown in Fig. 1.3. A negative correlation of V_F with regards to temperature can be observed. For example, at 25°C and 10 A forward current, the forward voltage V_F is about 0.72 V, while at 125°C, the value drops to 0.55 V. Although the forward voltage drops with the increase in temperature, the diode series resistance increases accordingly, which still results in increased losses at high current [18].

1.2.2 Inductors

Temperature also has an impact on inductors' electrical characteristics, particularly on the inductance and the copper winding wires. The influence is usually represented by the variation in the core permeability μ in the device datasheet. The inductance L is therefore

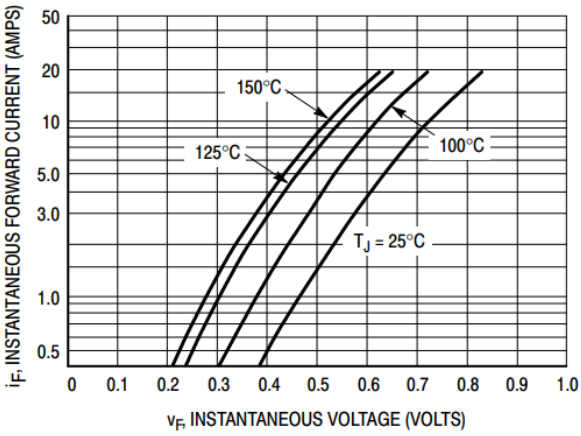


Fig. 1.3 Typical forward voltage per diode of MBR20100CT. From [19].

changed as these two parameters are directly linked. The relationship between μ and L is determined by

$$L = \frac{N^2 \mu A_e}{l_e} \tag{1.1}$$

where N, l_e and A_e represent the number of turns, mean path and cross-section area of the inductor core, respectively. The permeability versus temperature waveform is highly dependent on the core material, and varies significantly from one to another, as shown in Figs. 1.4 and 1.5a. For instance, in Fig. 1.4, an increasingly growing trend of the permeability of an F material can be observed between -50 °C to 65 °C and 125 °C to 210 °C. On the contrary, a negative correlation between permeability with temperature can be found in the remaining temperature ranges. The variation is about 750 μ from 3000 μ at 25 °C room temperature to 3750 μ at 100 °C, with a peak value of 4250 μ at 65 °C. Regarding the permeability of a magnetics molypermalloy powder (MPP) core, it increases less than 1% as shown in Fig. 1.5a. Hence, the temperature has a significant impact on the electrical performance of a ferrite core, while only a slight impact on a powder core. Parameters such as DC bias and frequency also have a great influences on the permeability, as can be observed

in Figs. 1.5b and 1.5c, respectively. The DC bias can be calculated with the help of

$$H = \frac{NI}{l_e} \tag{1.2}$$

where H and I are the magnetizing field and current, respectively. Based on the device datasheet, the rolloff percentage of the initial permeability with the current DC bias can be determined. Although inductors in power converters/inverters are pre-designed, when coping with varying loads the impact of DC bias should still be considered. Regarding the frequency, its relationship with permeability can also be easily traced from the datasheet.

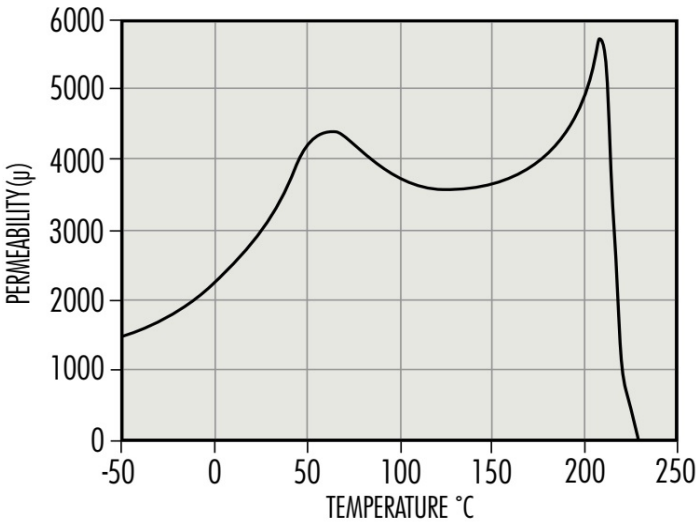
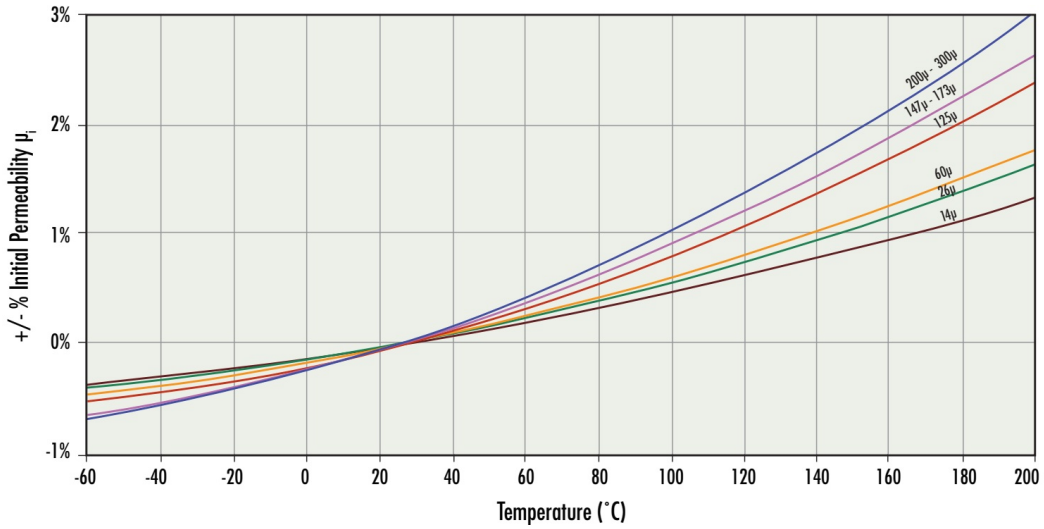
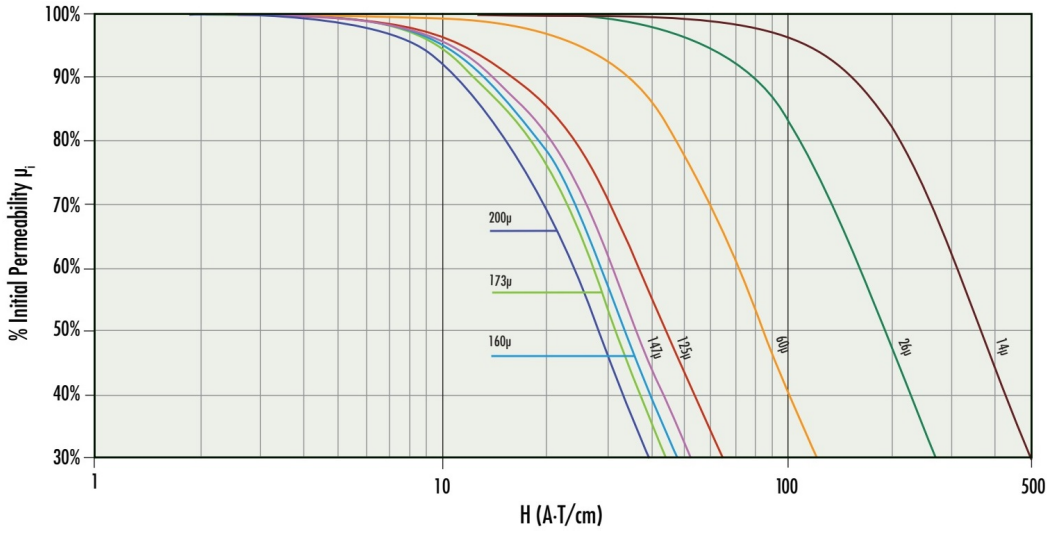


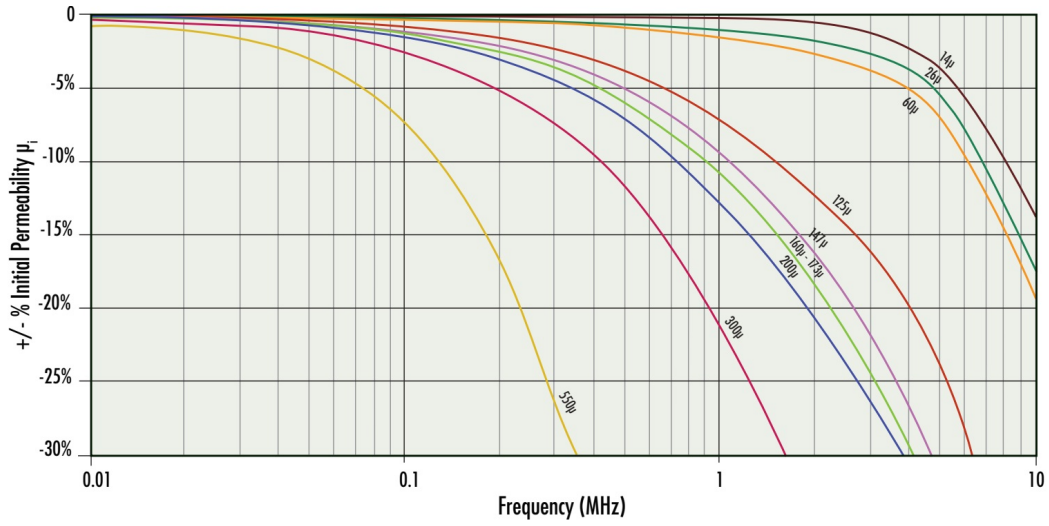
Fig. 1.4 Permeability versus temperature curves of an F material ferrite core from manufacturer Magnetics. From [20].



(a) Permeability versus temperature curve.



(b) Permeability versus DC bias.



(c) Permeability versus frequency curve.

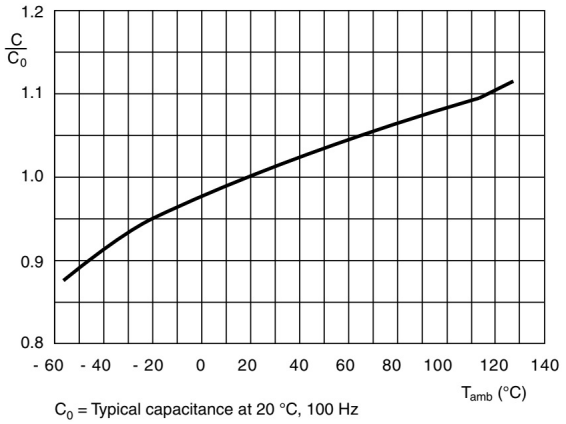
Fig. 1.5 Typical electrical characteristics of an MPP core from manufacturer Magnetics. From [21].

1.2.3 Capacitors

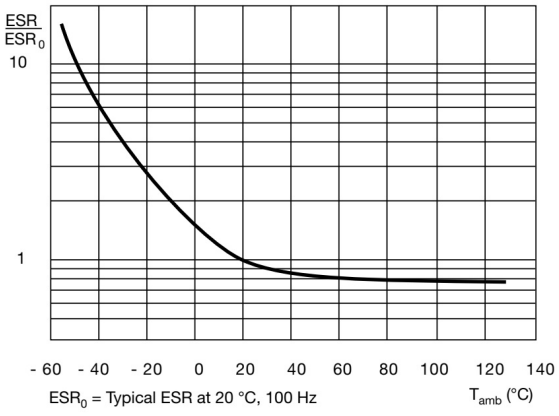
For capacitors, temperature has a direct impact on the capacitor equivalent circuit, particularly for the equivalent series resistance (ESR) and the capacitance. For instance, in the datasheet for VISHAY 150 RMI series low impedance aluminum electrolytic capacitors [22], an increase in temperature causes an almost linear increase in capacitance and exponential decrease in ESR, as can be observed in Figs. 1.6a and 1.6b. Frequency is another factor influencing these two parameters, and has even more significant impacts as shown in Figs. 1.6c and 1.6d. Taking as an illustration curve 2 with capacitor case diameter $\geq$ 16 mm and rated voltage $\geq$ 50 V. The capacitance and ESR require a multiplier of about 0.75 and 0.6, respectively, when the operation frequency increases to 10 kHz, as compared to their initial values tested at 20°C and 100 Hz. The capacitance reduces dramatically if frequency increases further, to 0.6 of the initial value even from 10 kHz to 20 kHz. For switching power supplies, especially for those that adopt variable frequency techniques, the ESR value should be carefully considered. Since electrolytic capacitors are also very critical as summarized in [23] based on the military handbook MIL-HDBK 217F [24], in which ESR is usually considered as an indicator of a faulty capacitor state, to predict its real-time value in operation is of great importance from a system safety point of view.

1.2.4 Summary

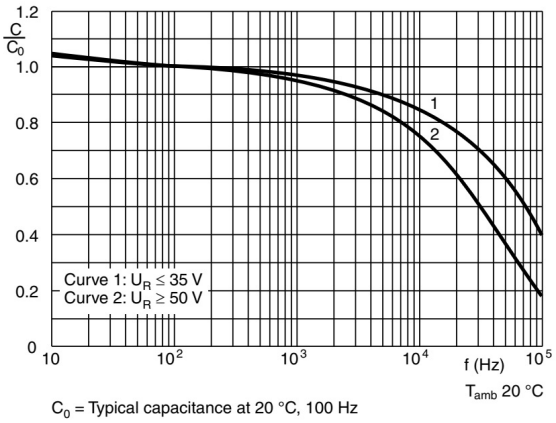
As discussed above, the temperature has direct impacts not only on semiconductors but also on passive components. An increase in temperature will result in variation of the electrical performances of these devices accordingly. Therefore, instead of considering a pure electrical model, electro-thermal models are preferred when simulating a converter to make more realistic estimations. Moreover, for passive components, additional considerations by introducing other affecting parameters should also be taken into account to further improve the simulation accuracy.



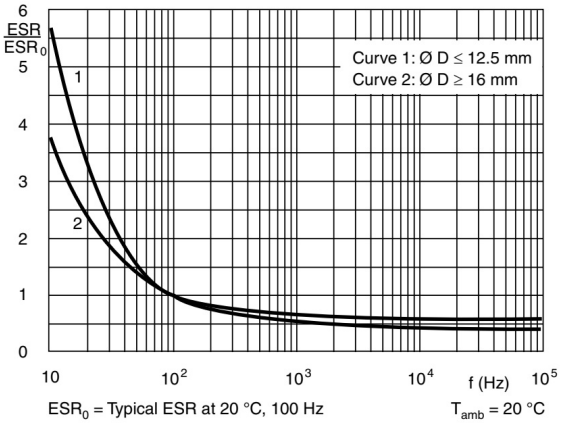
(a) Capacitance vs ambient temperature.



(b) ESR vs ambient temperature.



(c) Capacitance vs frequency.



(d) ESR vs frequency.

Fig. 1.6 Typical electrical characteristics of 150 RMI series aluminum electrolytic capacitors from VISHAY [22] with respect to temperature and frequency.

1.3 Power MOSFET Lifetime Estimation

Another highly thermally relevant consideration is the device lifetime evaluation or reliability assessment. In this section, the power device failure mechanism, the analytical model which depicts the device lifetime, and the lifetime estimation methodology are explained.

1.3.1 Failure mechanism of power MOSFETs

Thermally related failures fall into two main categories, namely solder fatigue and bond wire failure. Considerable work has been developed to investigate these two failures through device temperature cycling capability tests. They include power cycling and thermal cycling tests [25]-[30].

- **Power cycling** is a short-term (in a time frame of seconds) and chip-junction related failure test. The main failure parts in this test are the bond wires on the Silicon chips and also the soldered joints below the chips, due to the increased stress caused by the quick rising and falling of the junction temperature. A comprehensive comparison of various power cycling testings, considering test circuits, failures, and turn-on duration etc. are investigated [29].

- **Thermal cycling** is a relatively long-term (duration of minutes) failure test and is the solder joint and case temperature related. The failure is mainly due to the mismatch in the coefficients of thermal expansion of the composite materials (e.g. silicon chip, solder and copper base plate), and also the thermal stress-generated mechanical strain on the solder. The resultant defects are solder cracks which increase the thermal impedance between chip and solder plate.

Note that these two failure types are both package (e.g. module, discrete) and material (e.g. Si, SiC, copper) relevant. In addition, the two failure mechanisms are independent, both

of them should be considered, and the worse case scenario lifespan should be taken as the final result.

1.3.2 Lifetime model

To describe the aforementioned two temperature cycling capability, lifetime models are utilised. Two typical types, namely physics-of-failure (PoF) model and analytical model are introduced. The former depicts the physical failure mechanism and is dependent on the materials and structure of the device. Due to the difficulty of accessing these parameters, the utilization of this method is limited.

In contrast, the analytical model which is based on aging- accelerated testing data is more popular. This model is depicted by the term N_f, which represents the number of cycles before a device generates a fault under certain thermal stress. Different equations can be adopted to represent the device temperature cycling capability, with different parameters included. Three widely accepted failure models are presented below, where the coefficients A, δ, β_{1-5} can be extracted from datasheet provided by manufacturers.

- **Coffin-Manson model.** The model considers the temperature swing ΔT_j as the key affecting parameter.

$$N_f = A\Delta T_j^{\delta} \tag{1.3}$$

- **Modified Coffin-Manson model.** Based on (1.3), additional information about device mean temperature T_m is added. E_a and K denote activation energy and the Boltzmann constant, respectively:

$$N_f = A\Delta T_j^{\delta} e^{\frac{E_a}{kT_m}} \tag{1.4}$$

- **Bayerer's model [31].** Based on (1.3), extra information about the device turn-on period is considered. The typical turn-on and turn-off time in the power cycling test

is 1.5 s [25], and a weighting factor should be added if different durations of tests are carried out:

$$N_f = A(\Delta T_j)^{\delta} t_{on}^{\beta_3} I^{\beta_4} V^{\beta_5} D^{\beta_6} \tag{1.5}$$

Other lifetime analytical models, by making modification to (1.3)-(1.5) or introducing other parameters such as the elastic region, can also be found and enjoy popularity. It has been reported in [32] that inclusion of absolute temperature and/or the elastic region have significant effects on the accuracy of estimations, while the selection of Bayerer's model should be carefully considered as the term turn-on time may becomes ineffective if it is too long. Further discussions on lifetime model selections can also be found in [32].

1.3.3 Lifetime estimation methodology

This section depicts the essential steps in device and power supply lifetime estimation. A useful demonstration graph from [33, 34] proposed for the evaluation of the lifetime of PV inverter systems is shown in Fig. 1.7 for illustration. The detailed evaluation steps can be summarized as follows:

- **Step 1: Generate loss profile.** Apply environment profile and typical load mission profile to the electrical model (alternatively, to the loss model) of a device/power supply that needs to be evaluated, and generate the corresponding loss profile.
- **Step 2: Generate thermal profile.** Input the loss profile from step 1 to the thermal model of a device/power supply to produce the thermal profile. The detailed explanation of thermal models will be given in Section 1.3.4. Note that with the development of the electro-thermal model (ETM) of a device, steps 1 and 2 can be effectively merged.
- **Step 3: Thermal cycle counting.** Apply the thermal cycle counting method to translate complicated and irregular loading profiles into a set of organized cycles to facilitate the

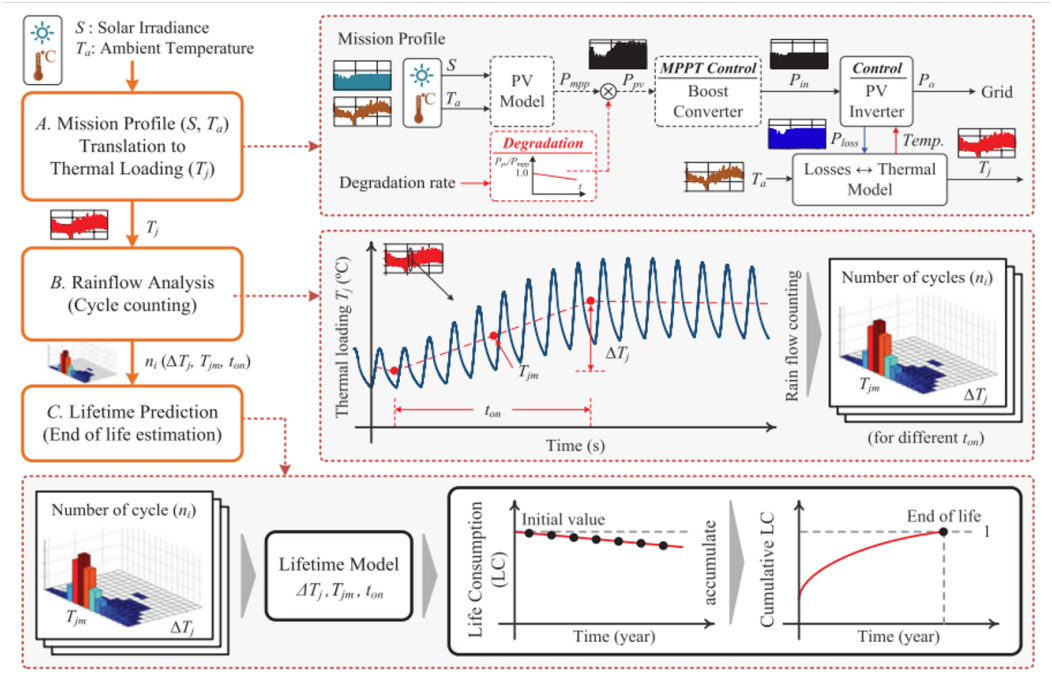


Fig. 1.7 Mission profile based analysis method of power devices of single-phase transformerless PV inverters proposed from [34].

stress accumulation calculation. More detailed discussions on the counting algorithms will be given in Section 1.3.5.

- **Step 4: Lifetime calculation.** With the information in step 3, use the so-called Miner's rule (1.6) to evaluate the stress that a device has undertaken after a number of thermal cycles. N_i and N_f in the equation are the cycles that a device has performed, and the corresponding number of cycles to fail under certain stress as described in Section 1.3.2, respectively. The stresses accumulate and once the Q value reaches one, the threshold of the end-of-useful lifetime of a device is reached.

$$Q = \sum_{i=1}^{n} \frac{N_i}{N_f} \tag{1.6}$$

- **Additional Step: Monte Carlo analysis.** Use this analysis to get the probability density distribution of failure to mimic a more realistic real-world operation by consid-

ering impacts such as variations of parameters due to manufacturing or uncertainty of the system.

1.3.4 Thermal model

A thermal model is necessary to evaluate the thermal performance of a device. Two types of thermal equivalent circuit models which describe the thermal impedance between the junction to case of a device, explained in [35], are revisited below.

- **Cauer model (Fig. 1.8):** A model based on the real physical structure of the semiconductor and heat flow paths. The thermal resistance and capacitance (R-C) elements are extracted based on the material characteristics, and following the layer sequence [36]. Hence, this representation allows users to monitor the internal temperatures of each layer (e.g. chip, solder layer, and lead frame) as can be seen in Fig. 1.9, which shows a simplified packaging structure of a device [18], [36]-[37]. However, the main difficulty lies in the parameter value extraction and also correct mapping.

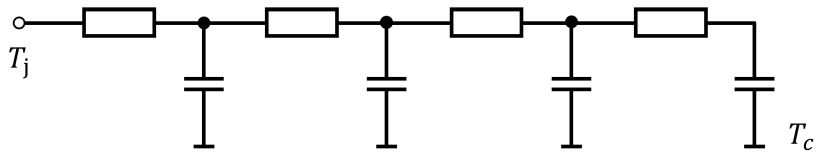


Fig. 1.8 Cauer model.

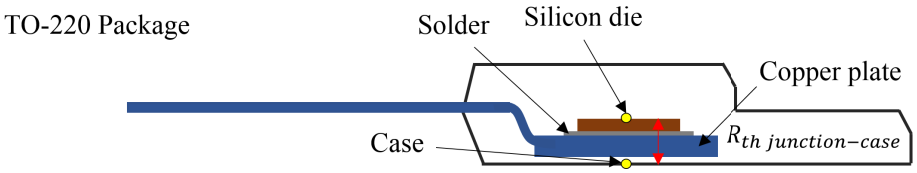


Fig. 1.9 An overview of the structure of a power MOSFET in TO-220 package.

- **Foster model (Fig. 1.10):** In contrast to the Cauer model, the individual R-C elements of the Foster model do not contain physical meaning, but act more like a behaviour

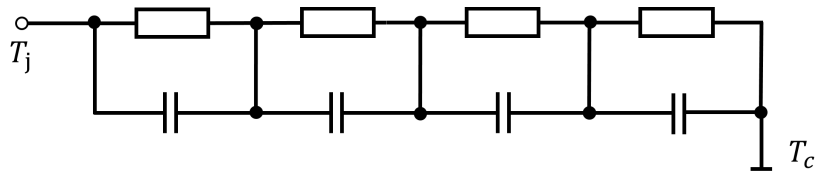


Fig. 1.10 Foster model.

model. The coefficients can be extracted from datasheets, or alternatively from the measured cooling curve of a device. The orders of the R-C pairs are user defined, usually, four orders are quick and accurate enough to describe the junction temperate variations.

The representation of the thermal impedance in equation form can be summarized as in (1.7), where R_i and C_i are the thermal resistance and capacitance of the corresponding number of order. Regarding the determination of those R_i and C_i values in the equation, there are two approaches. First, they can be obtained from manufacturers' websites, as some of them have already started providing thermal information of devices. Alternatively, they can be derived by users. The derivation steps can be summarized as follows: 1. Extract data points of the transient thermal impedance curve from a component's datasheet; 2. Import the extracted points to MATLAB or Excel and use the curve-fitting toolbox to produce a new curve to meet the points. Since the curve is governed by the known equation (1.7), the parameter values will be generated automatically. More information can be found in [38], which provides detailed derivation steps and validation of an Excel-generated thermal model example. Note that, different devices may present different transient thermal impedance performances, therefore, the R-C values are nonidentical.

$$Z_{thjc}(t) = \sum_{i=1}^{n} R_i \cdot [1 - e^{(\frac{t}{C_i R_i})}] \tag{1.7}$$

Both the Foster and Cauer models indicate the thermal impedance between the junction and the case of a device. In other words, the temperature between junction to case can be

determined. However, to estimate the junction temperature T_j, the case temperature T_c also should be known. This value can be identified by (1.8), depending on whether a heat sink is equipped with the power device or not. Z_{ca} and Z_{hs} are the thermal impedance from case to ambient, and heat sink to ambient, respectively. P_{loss} and T_a, namely the power losses generated by the device and the ambient temperature.

$$T_c = \begin{cases} P_{loss} \cdot Z_{ca} + T_a & \text{with heat sink} \\ P_{loss} \cdot Z_{hs} + T_a & \text{without heat sink} \end{cases} \tag{1.8}$$

Therefore the junction temperature can be calculated by the summation of junction to case and case temperature (1.9) below.

$$T_j = Z_{thjc}(t) \cdot P_{loss} + T_c \tag{1.9}$$

1.3.5 Thermal cycle counting algorithm

As described above, a thermal cycle counting algorithm is required to depict the stresses in reliability assessment and lifetime prediction of power devices, especially when they operate with critical and varying loads. Commonly used counting methods such as half-cycle peak through, rising-edge, and rainflow counting are introduced in [39]. Among them, rainflow counting is the most widely adopted counting method currently due to its relatively low relative error compared to other counting methods [40]. It is a method first proposed by Matsuishi and Endo in fatigue analysis in 1968 [41]. A strain fluctuation with time diagram rotated by 90° can be found in Fig. 1.11a. When applied to count thermal cycles, the strain is replaced by the temperature information. The method pictures the reversals (peaks and valleys) as rain drops and drips off pagoda roofs. The termination of the waterflow follows either when it meets with a drop dripping from an earlier source, the opposite peak has larger or equal magnitude, or it drips off the roof. The terminated flow is counted as a full

cycle which represents material energy dissipation. The actual physical meaning behind this methodology from a mechanical point of view is that the method filters out the small stress cycle interruptions from the original cycles, which mimics the effect of material memory observed in the strain and stress ε hysteresis diagram in Fig. 1.11b. By doing so, the material can resume its original cycle path which has more significant impacts on fatigue damage, and the calculation will not be underestimated.

Different methodologies are proposed to achieve rainflow counting in [39] and [42]. Here, the principle of the three reversal approach adopted by MATLAB is briefly explained.

The load profile is turned into a sequence of reversals first, a simplified example from [43] is shown in Fig. 1.12. The reversals denote the local minima and maxima with change of sign, e.g. points A-L. The three reversal approach replies on a pointer Z and comparison of the amplitude of two ranges to determine the counting actions, where the range is described as the difference between two reversals. Three points are read following the time sequence, e.g. points A, B and C are the 1st, 2nd and 3rd points respectively. The range of points 1 to 2, and 2 to 3 are represented as $r(Y)$ and $r(X)$. A moving pointer Z starting from the 1st point is set. The cycles are counted following the conditions below:

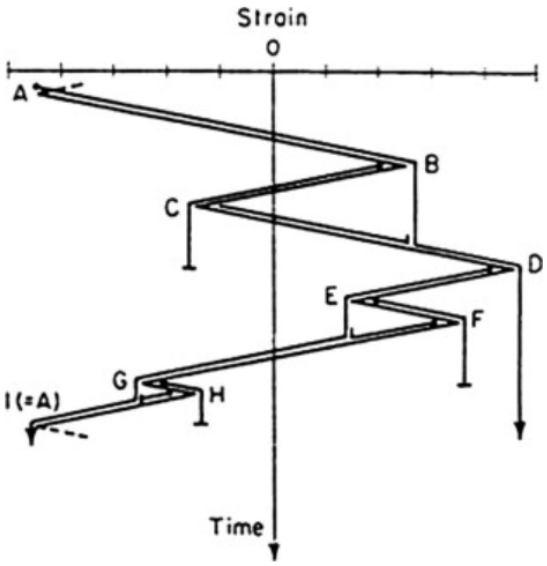
1. If $r(X) > r(Y)$, and the pointer Z is in Y, then count Y as half cycle, discard the 1st point, and set pointer to the 2nd point.

2. If $r(X) > r(Y)$, and the pointer Z is not in Y, then count Y as half cycle, discard the 1st and 2nd point.

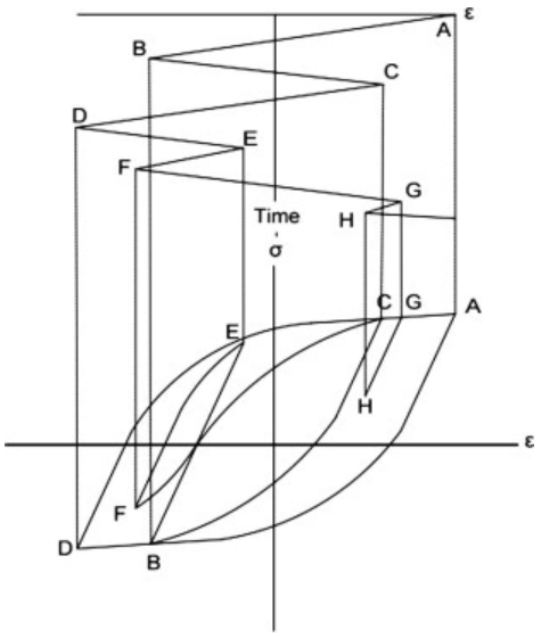
3. If out of data, count last two points as half cycle.

4. Else, read the next point/reversal.

Here, the detailed counting steps from point A to G in Fig. 1.12 are listed and explained as an example. More references as to the implementation of this algorithm can be found in [43]:



(a)



(b)

Fig. 1.11 Demonstration of the rainflow counting method based on stress-strain fatigue analysis. (a) The application of the rainflow method for a random loading from [44]. (b) The strain fluctuation diagram and the corresponding hysteresis curve from [44].

1. Pointer Z = A, reversals A, B, C. Satisfy the condition (1) that $r(BC) > r(AB)$ and Z in r(AB). Hence, count AB as half cycle, discard A and set Z=B.

2. Pointer Z = B, reversal, B, C. Satisfy the condition (4), read next point.

3. Pointer Z = B, reversals B, C, D. Satisfy the condition (1). Hence, count BC as half cycle, discard B and set Z = C.

4. Pointer Z = C, reversal, C, D. Satisfy the condition (4), read next point.

5. Pointer Z = C, reversal, C, D, E. Satisfy the condition (4), read next point.

6. Pointer Z = C, reversal, C, D, E, F. Satisfy the condition (4), read next point.

7. Pointer Z = C, reversal, C, D, E, F, G. Satisfy the condition (2), $r(FG) > r(EF)$. count EF as 1 cycle, and discard E and F.

8. Pointer Z = C, reversal, C, D, G. Satisfy the condition (1), count CD as half cycle, and discard C, set Z = D.

This method allows users to discard counted points to form a new reversal, and to compare two non-adjacent ranges. The pointer Z and the range values can be easily stored in and read from a stack or an array, hence, it is a programming friendly approach.

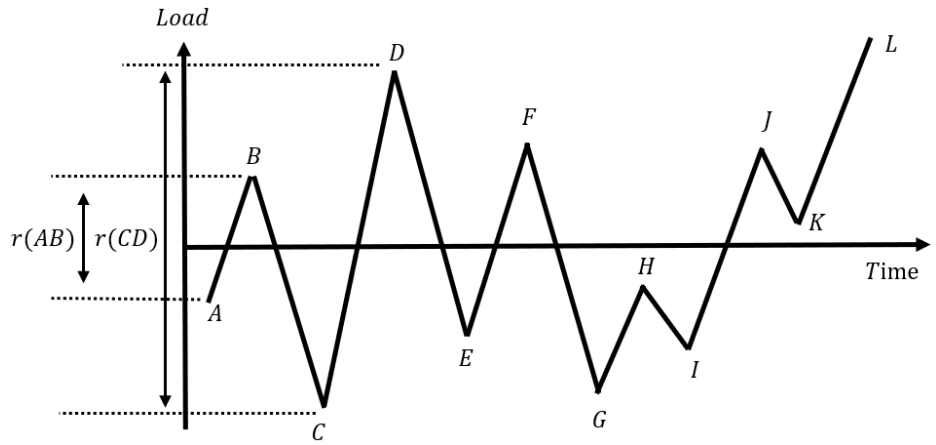


Fig. 1.12 Example of a reversal sequence in [43].

1.4 Research Gap

To fulfil the need for reliable and efficient operation of future power supplies as discussed in Section 1.1, some of the research gaps that can be filled in these fields are listed and discussed as follows:

- Characteristics of active and passive power components are discussed in Section 1.2. Investigations on constructing ETMs for the components have also been developed currently. However, in the most of works, ETMs are built for individual devices, particularly for those power semiconductors but not for a converter with all active and passive components. It is reasonable as power semiconductors are highly penetrated and are one of the most prone to failure parts in configurations such as modular multi-level converters. Therefore, it is widely accepted to utilize the thermal performance of a single MOSFET or IGBT module in those topologies to predict their lifetimes. Nevertheless, there still exists plenty of topologies that contain all active and passive components, to facilitate their design, optimization, and lifetime evaluation, there is also a need of a model which considers electrical and thermal aspects of all devices in a converter. Besides, this model also strengthens the connections among components and is more reasonable and realistic for a running converter. As a device will not only be affected by its electrical and thermal characteristics but also impacted by other components due to the interaction among them.

- Lifetime evaluation of power electronics systems has drawn great attention recently to ensure safe operation. The basic evaluation procedures have been introduced in Section 1.3, in which the electrical/thermal simulation and lifetime estimation are usually carried out on different simulators/platforms. Besides, the aging effect is not considered in the evaluation process. Hence, there is an absence of a method, which

allows simulating electrical, thermal, aging and lifetime of a device simultaneously in one software platform.

- The rainflow counting algorithm has gained popularity for its low relative error in device lifetime prediction. Nevertheless, the method requires a complete loading profile to run recursive comparisons to count the cycles. This, on one hand, prevents most simulation software from considering other parameters for the device under study, such as aging and current state of health in the estimation, On the other hand, it also brings difficulties in realization in circuit simulators like SPICE. Therefore, there is a lack of solution to address this issue.

- Zero-sequence voltage (ZSV) and current (ZSC) injection are frequently adopted in Y- and Δ-connected CHB converter-based three-phase systems, respectively, to cope with the unbalanced power generation among phases. The power balancing capability of these two configurations has been studied extensively, however the impacts of ZSI on the thermal performance and lifespans of the two configurations have not been evaluated before.

1.5 Thesis Objectives

With reference to the discussion in Section 1.4, this thesis has developed a series of research work to facilitate the achievement of the requirements. The main objectives can be summarized as follows:

1. Based on investigations of the different characteristics of power components, to propose models of a boost converter which are capable of describing electrical performance and also considering self-heating phenomenon of all devices. The proposed research work is required to have the following features: allows users to observe the drifts or variations of electrical parameters caused by temperature (e.g. on-state resistance of

MOSFETs, ESR of inductor/capacitor), DC current (e.g. inductance of inductor), and etc.; fairly accurate temperature prediction; and ease of implementation.

2. According to the study of lifetime evaluation, to propose a concise but comprehensive MOSFET model that enables electro-thermal modeling, aging and lifetime estimation on only one simulator, such that, multi-discipline modelling is integrated and co-simulation can be achieved. With this model, users should be able to monitor the aging process of the MOSFETs, and based on its state of health, strategies can be applied to prolong the lifetime of the device, or the reliability of the converter/inverter.

3. With the knowledge of lifetime evaluation, to realize the rainflow thermal cycle counting algorithm in SPICE, to improve the counting accuracy as compared to other counting methods on one hand, and to achieve the online counting on the other hand.

4. Rely on the electro-thermal modelling techniques and study of lifetime estimation, to assess and evaluate the reliability of Δ- and Y-connected CHB converter-based three-phase systems. The evaluation particularly emphasizes and analyzes these two systems when dealing with the unbalanced three-phase power, and to figure out the corresponding impacts on the device and system lifetime.

1.6 Thesis Structure

This thesis is organised as follows. Chapter 2 presents two electro-thermal derivation methods of a boost converter considering power semiconductors, and also passive components. Moreover, other affecting parameters on the electrical performances of inductor and capacitor, e.g. frequency, are also considered to form a more comprehensive study. The principle, mathematical models, and detailed derivation method of each component are described step by step. Fairly accurate temperature prediction is obtained and the experimental outcomes are illustrated to verify effectiveness. Key electrical performances are highlighted, indicating the

influence of other parameters affecting passive components. Discussions and comparisons in terms of simulation accuracy and speed are also presented.

Chapter 3 presents an integrated electro-thermal, aging and lifetime estimation model of power MOSFETs, which allows multi-discipline simulation in a single simulator. The idea comes from the fact that the MOSFET on-state resistance is not only temperature dependent, but is also widely identified as a failure precursor. Hence, based on the ETAM proposed in Chapter 2, the impact of aging is induced, facilitated by a lifetime analytical model, and also a thermal cycle counting method. Fast simulation speed is reported, making this model a promising candidate in device reliability assessment.

In Chapter 4, a rainflow counting algorithm realized by circuitries is proposed to facilitate a better estimation of consumed lifetime of the MOSFET proposed in Chapter 3 with an improved counting accuracy. The performance is validated by a comparative analysis in terms of counting accuracy and simulation speed between the proposed method, MATLAB and also a well-accepted half-cycle peak-through counting method carried out under different load stresses and length conditions.

In Chapter 5, an investigation into Y- and Δ-connected CHB-converter basede three-phase systems in terms of the unbalanced power ratio, thermal performance, and the impact on the device lifetime is presented. Device thermal performance evaluated by ETM provided by the PLECS® software is discussed. Both the simulation and experimental results have verified that even though the Δ-connection has better power balancing capability, it also leads to unbalanced stress distribution among the three phases, which will potentially lead to one phase aging faster.

Finally, in Chapter 6, the key achievements presented in this thesis, together with some future prospects are summarized.

1.7 Summary of Device Ratings

This thesis focuses on investigating the electrical and thermal characteristics, and lifetime estimation of power devices and converters, to facilitate the study, a summary of ratings of devices adopted in this thesis is presented in Table. 1.1.

Table 1.1 Component and Device Specification

Chapter	Parameter	Model/Manufacture	Typical Values
2	MOSFET	IRF540N Infineon	V_{DS} = 100 V, I_D = 33 A $R_{ds,on}$= 40 mΩ at V_{gs} = 15 V R_{jc} = 1.15 °C/W
2	Diode	MBR20100CT Vishay	I_F = 20 A, V_F at I_F = 0.57 V R_{jc}= 2 °C/W
2	Inductor L	MCAP115018047A Multicomp	250 uH, R_i= 60 mΩ
2	Inductor core	Iron Powder-75-TAF200 Curie	l_e = 9.38 cm, A_e = 0.887 cm^2
2	Capacitor C	MAL215050472E3-35V Vishay	C = 4700 uF, ESR = 61 mΩ
2, 5	Thermal coupler	Z2-K Series LABFACILITY	-
2, 5	Data logger	DT80 DataTaker	-
3, 4, 5	MOSFET	IRFP340 Vishay	V_{DS} = 400 V, I_D = 10 A $R_{ds,on}$ = 423 mΩ at V_{gs} = 15 V R_{jc} = 0.83 °C/W

Chapter 2

Electro-Thermal Modeling of a Boost Converter Considering Device Self-heating

2.1 Introduction

Based on the discussion in Chapter 1, it is known that the thermal performance of a device has great effects on its electrical characteristics. Recently, significant efforts and progress have been made in developing ETMs for power semiconductor devices as they are highly sensitive to temperature changes [18],[36],[45]-[46]. Passive components such as inductors and capacitors are also investigated, since they too are temperature-dependent [47]-[52]. To obtain actual values not only helps in estimating power losses more accurately, but also helps designers choose a proper component when optimising a converter [8]. However, most published work focuses on ETMs for a single power device or a module only as summarized in Table 2.1, instead of considering a whole converter which is more realistic in terms of converter design. Hence, in this work, a datasheet-informed ETM is proposed for a boost converter. It is achieved by adding additional behaviour models to the existing electrical

model of each power device to reflect the temperature-incurred electrical behavioural change. A loss model and R-C thermal network are used to estimate the temperature change. By doing so, the power loss and temperature feedback loop are formed. The advantages of this work are ease of integration with existing electrical models in the SPICE library, and elimination of the complicated physical properties of the power devices, but fully utilizes the device datasheet information and mathematical method.

However, a potential issue of the ETM is that with the increase of the operation frequency, the simulation time increases accordingly as it is derived based on a switching converter model. To address this issue, a modified ETAM which follows similar derivation steps employed in the ETM but adopts an averaged converter model is also developed. Modifications are made to tackle the problem that the averaged model is neither frequency nor temperature-dependent. The key merits of the proposed ETAM work are fast simulation speed, fairly accurate temperature prediction, and ease of implementation.

For both ETM and ETAM, simulation and experimental results are given and compared to verify the proposed solutions. The key voltage/current waveform and temperature data for the boost converter with different frequency and input power are captured, and comparisons from both the electrical and thermal aspects are given. In addition, a comparison of the simulation speed of both the ETM and ETAM is also given. This chapter addresses the first objective of the thesis, and part of its content contribution is published in [53, 54].

2.2 Related Works and Research Gap

2.2.1 Review of existing ETMs

Extensive studies on power MOSFETs and diodes have been undertaken from both the academic and industry sides, because they are highly sensitive to temperature changes [18],[36],[45]-[46]. In [18], ETMs for a SiC Schottky diode and a SiC MOSFET are devel-

oped based on their physical models. Polynomial equations are used to solve the convergence problems caused by some parameters in the physical model which are represented by exponential equations. Foster thermal models are built to predict the junction temperature of the diode and MOSFET. In [36], Infineon Technologies introduced a method by adding extra behaviour models to modify the threshold voltage V_{th}, drain current I_D and on-state resistance $R_{ds,on}$ changes caused by temperature. In [45], an ETM is derived for GaN FETs by adding an R-C network to estimate the junction temperature while by adding a modification circuit to change the gate voltage, and hence to reflect the FETs' electrical performance as it relates to the temperature.

Passive components such as inductors and capacitors are not only affected by temperature, but also greatly affected by the DC bias current (for inductance, e.g. ferrite core [20] or iron powder core [21]), and frequency (for both capacitance and ESR [22]). To obtain their actual values not only helps in estimating the power losses more accurately, but also helps designers choose a proper component when optimising a converter [8]. Hence, more comprehensive models of passive components are needed. In [47], a SPICE model is proposed for a ferrite core inductor to estimate the core losses and corresponding hot-spot temperature based on the datasheet. The temperature estimation is directly related to the operation conditions of the inductor, however, no feedback from the thermal model to the electrical model can be found. In [48], a LabVIEW-based experimental platform which allows users to set measurement parameters and collect the experiment data automatically is built to investigate the current and temperature-dependent behaviour of an inductor. In [49], by curve-fitting the results presented in [48], a polynomial equation of inductance with respect to the DC current and temperature is obtained to calculated the dynamic inductance. MATLAB simulation results and experimental results for a partially saturated inductor working in a boost converter are given. In [50], a method for estimating the hottest internal temperature of running power capacitors is introduced using heat transfer equations. A conduction equation is used to

calculate the internal hot spot to the capacitor shell, while radiation and convection equations are used to estimate the shell to ambient heat transfer. In [51], an improved physics-based model for aluminum capacitors is presented. To sum up, the temperature of the device has been estimated in [45], [47], [50] and [51], however, they have not considered the impacts of temperature on the device. Characteristics of inductors and capacitors have been investigated based on experimental and physical construction respectively in [48] and [51], however, efforts to build the experimental platform in [48] and deeper understanding of capacitor models to reflect the interaction with temperature change in [51] are required.

2.2.2 Review of existing ETAMs

The benefits of adopting ETMs owes to their capability of providing instantaneous change of temperature and device electrical performances. However, one significant drawback of ETMs is their long simulation time, especially when a converter operates at a high frequency, as it is based on a switching model. To solve this problem, ETAM of converters are proposed in [46],[52], [55]-[57]. In [46], a novel ETAM of a MOSFET-diode pair is proposed and applied to a boost converter with the capability of calculating its characteristics when operating in both continuous conduction mode and discontinuous condition mode. However, the switching losses of MOSFETs are not considered. In [52], an ETAM is proposed for a boost converter with a more precise inductor model based on its magnetic characteristics. In [55], a method that adds an extra resistor to represent the losses caused by switching is included into a boost converter average model. However, this work has not taken the thermal part into account. In [56], a state-space ETAM for a bi-directional converter in hybrid electric vehicles (HEVs) is proposed. Temperature-dependent loss models of MOSFETs and diodes are calculated and used to estimate the junction temperatures of devices. In [57], a fast FPGA real time electro-thermal modelling method of a boost converter, especially for IGBT and diode, is proposed. The algorithm determines the conduction/switching losses, sends them into the

thermal model, and updates the electrical model continuously. Hence, An electro-thermal model is formed. However, in the above ETAMs of power converters, MOSFET switching losses are usually not considered, while the parameters of passive components are usually kept fixed.

Table 2.1 A summary of the existing electro-thermal modelling techniques of power components and converters.

References	Components	Platform	Methodology		
			Electrical model	Temperature-dependent Parameters	Thermal model
[18]	SiC MOSFET	PSpice®	Behaviour models	V_F,I_D,V_{th},C_{gs},C_{ds},C_{gd}	Foster model
	SiC Diode	PSpice®	Behaviour models	V_F	Foster model
[36]	MOSFET	Pspice®, SABER®	Add behaviour model	V_{th}, I_D, $R_{ds,on}$	Cauer model
[45]	MOSFET	LTspice®	Add gate modification circuit	V_{gs}	R-C circuits
[46]	MOSFET, Diode	SPICE	Behaviour models	$R_{ds,on}$, V_F	Behaviour models
[47]	Inductor	PSpice®	Behaviour models	Power losses	Behaviour model
[48]-[49]	Inductor	Experiment	Equation: Polynomial-fitting	L	Equations
		LabVIEW, MATLAB	Experimental results		
[50]	Capacitor	Experiments	-	-	Heat transfer Equations
[51]	Capacitor	Pspice®	-	C, ESR	Modify R-C circuits
[52]	Inductor	SPICE	Behaviour models	ESR, L	Behaviour models
[55]	Boost converter	-	Modified averaged model	Switching losses	-
[56]-[57]	Converter	Simulink/PLECS®	State space averaged model	Power losses	Foster model

2.2.3 Research gaps

To sum up, in the review of ETMs in Section 2.2.1, ETMs for individual components or for semiconductor pairs have been introduced in the most of the research work. However, very few have considered building a comprehensive ETM for a converter. In other words, they fail to take electrical and thermal aspects of all components into consideration. To fill the gap, a complete ETM is derived for a boost converter for illustration in Section 2.3. ETMs are built for MOSFETs and diodes following the existing derivation methods, and are integrated with the datasheet-informed ETMs for inductors and capacitors to enable a more comprehensive study. Experiments are also conducted to validate and improve the derived model. The key voltage/current waveform and temperature data of the boost converter with different frequency and input power are captured. The advantage of this methodology is that it is easy to integrate with existing electrical models, since basic equations are used, and behaviour models and look-up tables are add-ons. In addition, the presented methodology is very generic and can be adopted to derive the ETMs of any active/passive components and converters.

At the meantime, in the ETAMs of power converters mentioned in Section 2.2.2, MOSFET switching losses are usually not considered as the average model is frequency independent. In addition, for passive components, their inductance, capacitance, and ESR are kept at fixed values in most cases. Hence, to solve these problems while providing a fast simulation speed, a temperature-dependent average model considering self-heating of all components in a boost converter is proposed in Section 2.5. Similarly, experiments are carried out to verify the proposed model, and comparisons from both the electrical and thermal aspects are given. In addition, a comparison of the simulation time between ETM and ETAM is presented.

2.3 Method 1: Electro-Thermal Modeling

The aim of this work is to build a more comprehensive model for converters which combines the electrical and thermal domains. In this section, an electro-thermal model for a boost converter is derived as an example. However, the methodology is universal and can be applied to other converters. LTspice®, which is a free, high-performance and user-friendly simulation tool, is used in evaluating the performance of the circuit. Since it can only simulate electrical circuits, analogies between the thermal domain and electrical domain are required to estimate the device temperature, in which the temperature (°C) and power loss (W) in the thermal domain are represented by a voltage source (V) and a behaviour current source (A) in the electrical domain.

The model is obtained by adding behaviour models or look-up tables to the existing electrical model of the device, and hence to reflect the temperature-caused variation of electrical parameters. Behaviour current sources are adopted to calculate the instantaneous power losses of each component. The temperature estimation circuit of each component is represented by a thermal network. Since the heat transfer speeds of inductors and capacitors are relatively low, only thermal resistance R is used in the circuit to represent the steady state temperature. It is also for the sake of mitigating the simulation time. Although it allows users to capture the actual thermal response of a device as in the experiment if considering their thermal capacitances, it will also lead to a long simulation time especially when a converter operates at high frequency. For the same reason, only R values are considered for heat sinks which are equipped on MOSFET and diode. However, both the thermal resistance and capacitance (R-C) circuits are needed for semiconductors as their junction temperatures change instantaneously with losses. The specific R-C thermal resistance values can be obtain by adopting approaches explained in Section 1.3.4. Regarding the R values, they can either be obtained from their datasheets or from experiments. In this simulation, R values are set

the same as adopted in the verification experiments and they are achieved by calculating power losses of devices and measuring their corresponding temperature rises.

A diagram of the proposed electro-thermal model is shown in Fig. 2.1. The detailed analysis of the proposed ETMs for each component in a boost converter is given in the following section, namely MOSFET, diode, inductor and capacitor.

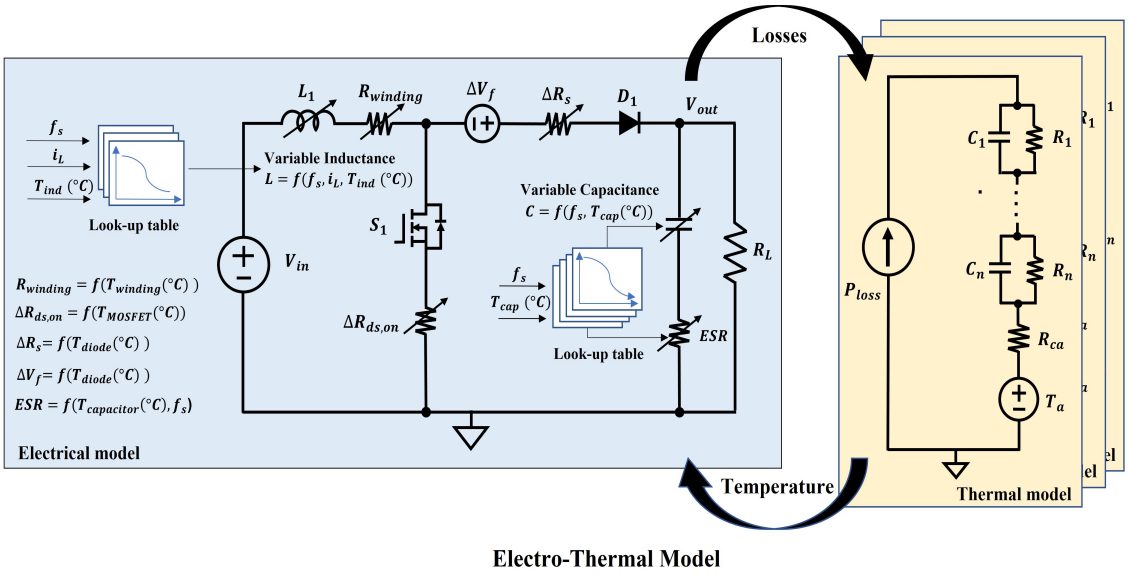


Fig. 2.1 An overview of the working principle of the electro-thermal model in this work.

2.3.1 MOSFET

A well-established ETM for MOSFETs [36] is adopted here to construct the model as shown in Fig. 2.2. Switching and conduction losses are two main contributors that cause an increase in the MOSFET temperature. The instantaneous losses of a MOSFET can be represented by $V_{DS} \cdot i_{DS}$, which are the device drain-to-source voltage and current respectively. The temperature rise affects the on-state resistance $R_{ds,on}$, the threshold voltage V_{th} and the allowed i_D. Among them, $R_{ds,on}$ is the dominant parameter that causes the losses. Hence, only $R_{ds,on}$ is considered in this work to estimate the MOSFET temperature in (3.1) below. The parameter α_M, which is a coefficient, can be determined by using the similar curve

fitting method presented in Section 1.3.4. To sum up, the MOSFET electrical model contains a MOSFET and an extra series connected temperature-dependent resistor. The R-C foster thermal model is built to monitor the instantaneous junction to case temperature changes following the construction method presented in Section 1.3.4, while the 23 V voltage source represents the ambient temperature. A low pass filter is used to calculate the average power loss. Hence, the MOSFET junction temperature Tj_MOS is the summation of the room temperature, the case to heat sink temperature (average power loss times the heat sink thermal resistance), and the instantaneous junction to case temperature Tj_Ins.

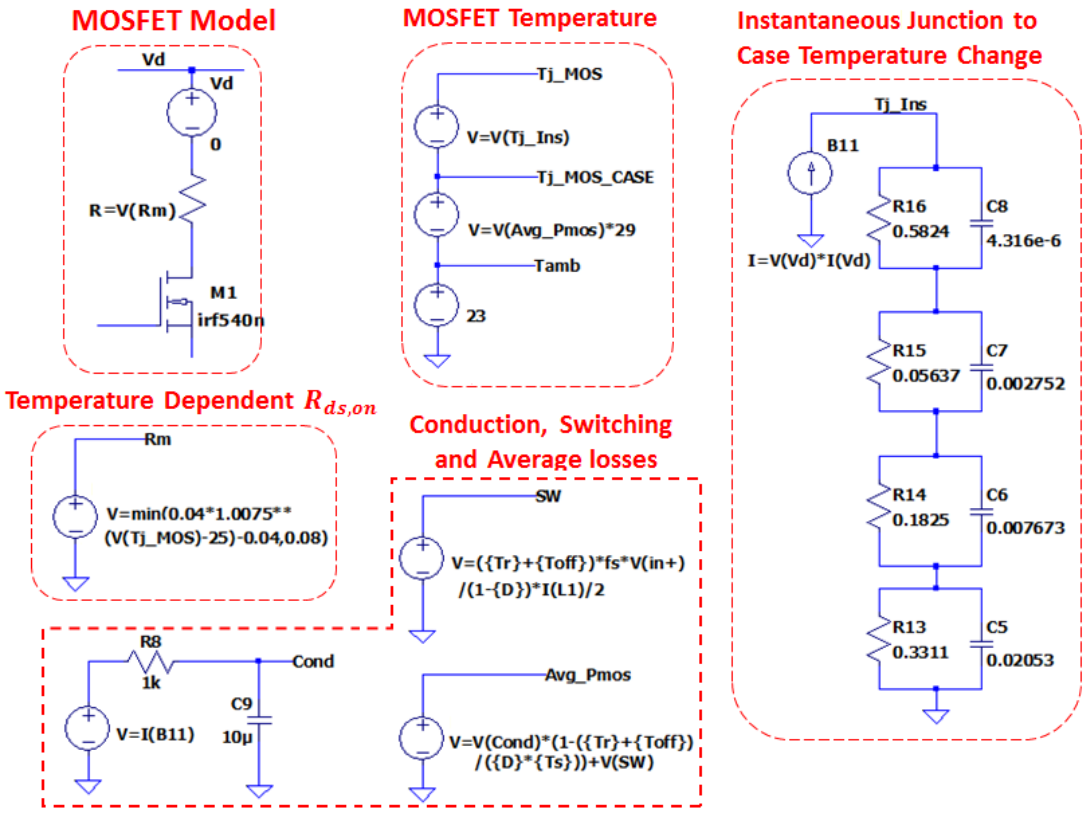


Fig. 2.2 Electro-thermal model of a MOSFET.

$$R_{ds,on}(T_j) = R_{ds,on}(25^{\circ}C) \cdot (1 + \frac{\alpha_M}{100})^{T_j - 25^{\circ}C} \tag{2.1}$$

2.3.2 Diode

Similarly, the diode ETM is derived by adopting the same method as in [36], as shown in Fig. 2.3. The main losses of the diode are the conduction losses, which can be calculated by multiplying instantaneous voltage on the diode and the current flow through it by $V_D \cdot i_D$. Two key temperature-related parameters in a diode are the series resistance and the forward voltage. They can be calculated using (2.2) and (2.3) below [46], and the coefficient can be calculated from the datasheet. The constructed average and instantaneous losses models and temperature estimation circuits are similar to the MOSFET mentioned above.

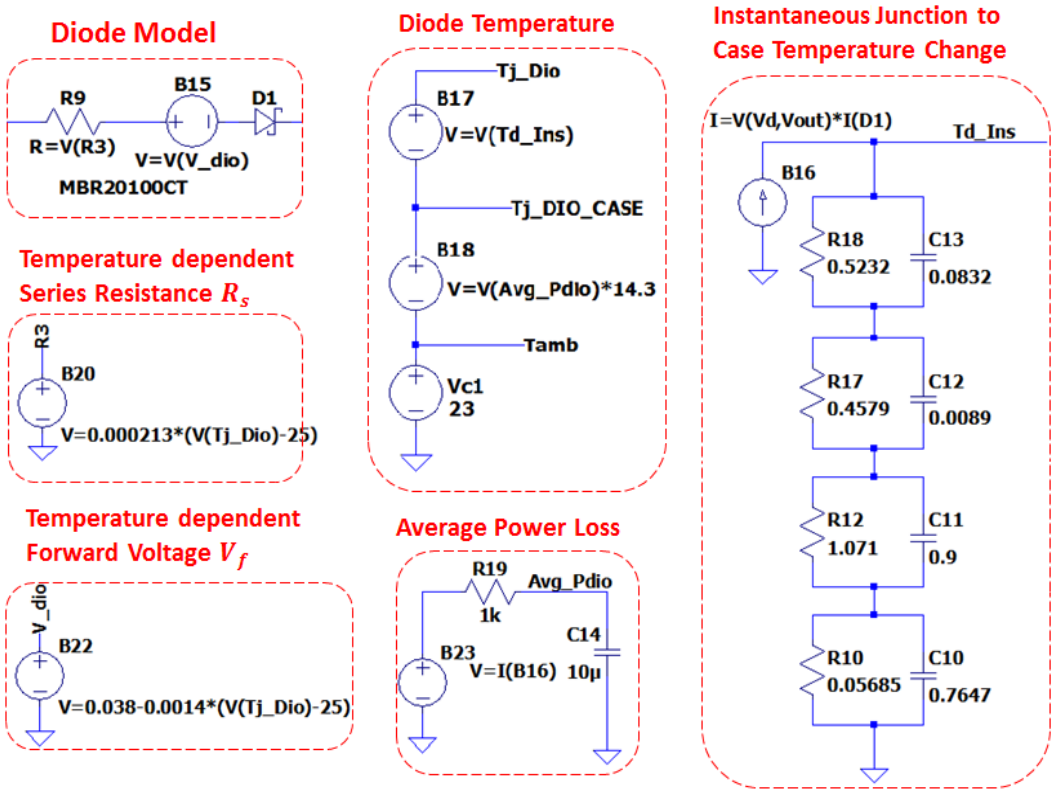


Fig. 2.3 Electro-thermal model of a diode.

$$R_s(T_D) = R_{s0}(25^\circ C) \cdot (1 + \alpha_{R_s} \cdot (T_D - 25^\circ C)) \tag{2.2}$$

$$V_f(T_D) = V_{f0}(25^\circ C) + (1 + \alpha_{V_f} \cdot (T_D - 25^\circ C)) \tag{2.3}$$

2.3.3 Inductor

The proposed ETM with variable inductance is shown in Fig. 2.4. The conventional inductor model is represented by a fixed inductance with its ESR. Since, in a real-world scenario, the inductance is not only temperature-dependent but also impacted by DC bias current and frequency, an ETM of an inductor with variable inductance in series with its temperature-dependent series resistance is introduced here. The variable inductor can be built either by employing a reluctance model [58] or by using the proposed model based on (2.4) below. Both of them are constructed with the help of behaviour models. With the variable reluctance model, it is possible to observe both the electric and magnetic behaviours of an inductor with any structures and materials. Brauer's model is adopted to depict the non-linear characteristic of the permeability of a magnetic device. The key limitation of this model is that it does not contain any information on temperature and frequency. On the contrary, the proposed model is data-driven, it does not allow the users to study the magnetic behaviour but has the capability of considering various impacting factors in a simple manner. As the focus of this thesis is to link a device's electrical performance with its thermal performance, the proposed model is selected.

The inductance L is set as a fixed value, for instance 1 H in this model. To add impacts of DC bias current, frequency, and temperature on inductance, three look-up tables are extracted from the datasheet, represented as L_vs_I, L_vs_Fre, and L_vs_Temp, which indicate the impacts of temperature, frequency and DC bias current on the change of inductance in percentage, respectively. A coefficient $V(L)$, calculated by a behaviour model, is the product of outputs of the look-up tables and initial inductance, and reflects the real inductance value.

$$\frac{V_L}{V(L)} = L\frac{di(t)}{dt} \tag{2.4}$$

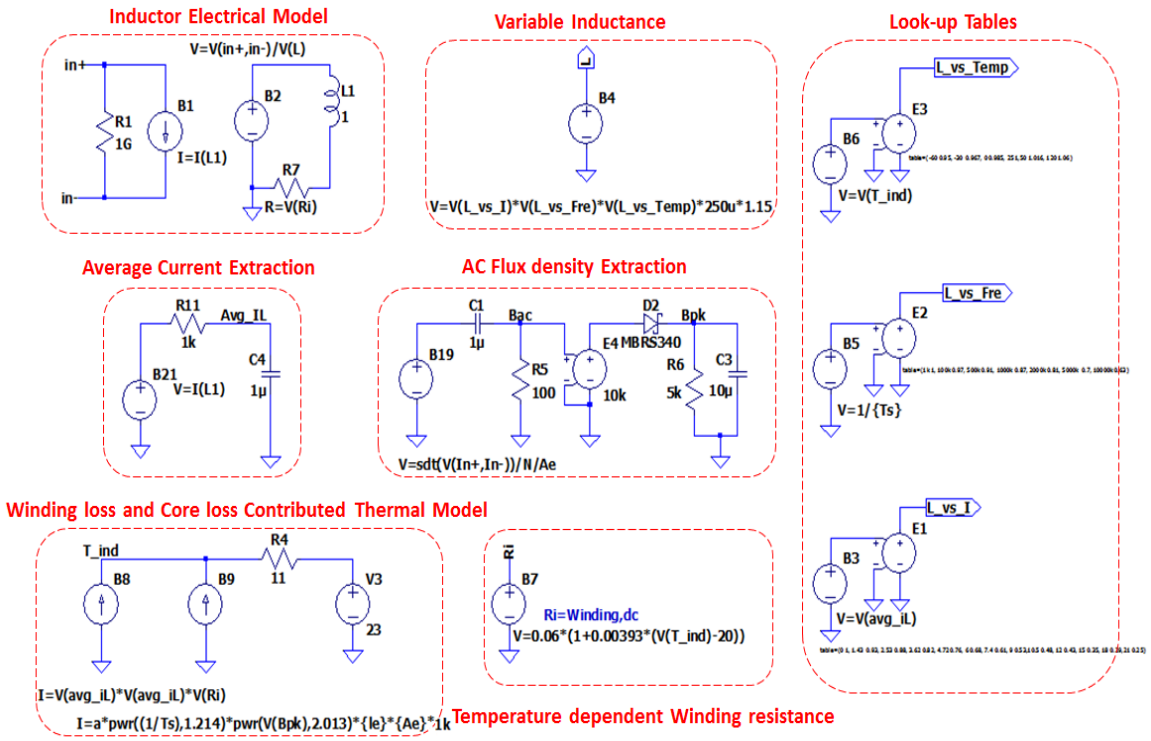


Fig. 2.4 Proposed electro-thermal model of an inductor with variable inductance.

The variable winding resistance R_i with an initial resistance R_{dc} at 20°C is represented by a behaviour model based on (2.5), in which α_i is the temperature coefficient of copper, valued at 0.00393, and $T_{winding}$ is the inductor winding temperature.

$$R_i = R_{dc}(20^\circ C) \cdot (1 + \alpha_i \cdot ((T_{winding})^\circ C - 20^\circ C)) \tag{2.5}$$

Both the winding loss and core loss are considered to predict the overall inductor temperature T_{ind}. The winding loss is calculated in (2.6) below, where $i_{L,rms}$ is the inductor root mean square (RMS) current, while for the core loss, [47] has proposed an approach to estimate the core loss and the hot-spot temperature for a ferrite core using the SPICE model. The most common Steinmetz equation which gives core power density losses (2.7) below, is used to calculate the core loss, in which, P_v ,B_{pk} and f are core loss density, peak value of the flux density and the operation frequency respectively. The coefficients k, a, b can be determined

from curve fitting the core loss chart in the datasheet. Regarding B_{pk}, it can be obtained by several approaches as discussed in [21]. The method adopted here is by employing a behaviour model to rewrite the Faraday's equation (2.8), where N and A_e are the inductor number of turns and cross-section area. By doing this the flux swing B_{ac} and its peak value B_{pk} can be determined.

Therefore, the core loss is calculated by multiplying the core loss density and its core volume in (2.9) below, where l_e is mean magnetic path length of the inductor core.

$$P_{winding} = i_{L,rms}^2 \cdot R_i(T_{ind}) \tag{2.6}$$

$$P_v = k f^a B_{pk}^b \tag{2.7}$$

$$V_L = N A_e \frac{dB}{dt} \tag{2.8}$$

$$P_{core} = k f^a B_{pk}^b \cdot l_e \cdot A_e \tag{2.9}$$

A low pass filter is built to extract the average DC inductor current, while a high pass filter is used to extract the AC flux density as explained in [47]. Alternatively, behaviour models can be used to calculate the average current and peak flux density.

The loss models contain both the core loss and winding loss, and are represented by current sources. The losses will go to the inductor thermal resistance, and hence generate a voltage T_{ind} which represents the actual temperature of the device. The 23 V voltage source represents the room temperature which is at 23 °C.

2.3.4 Capacitor

Similarly, the ETM of a variable capacitor (2.10) and ESR can be established as can be seen in Fig. 2.5.

$$\frac{i_C}{V(C)} = C \frac{dV(t)}{dt} \tag{2.10}$$

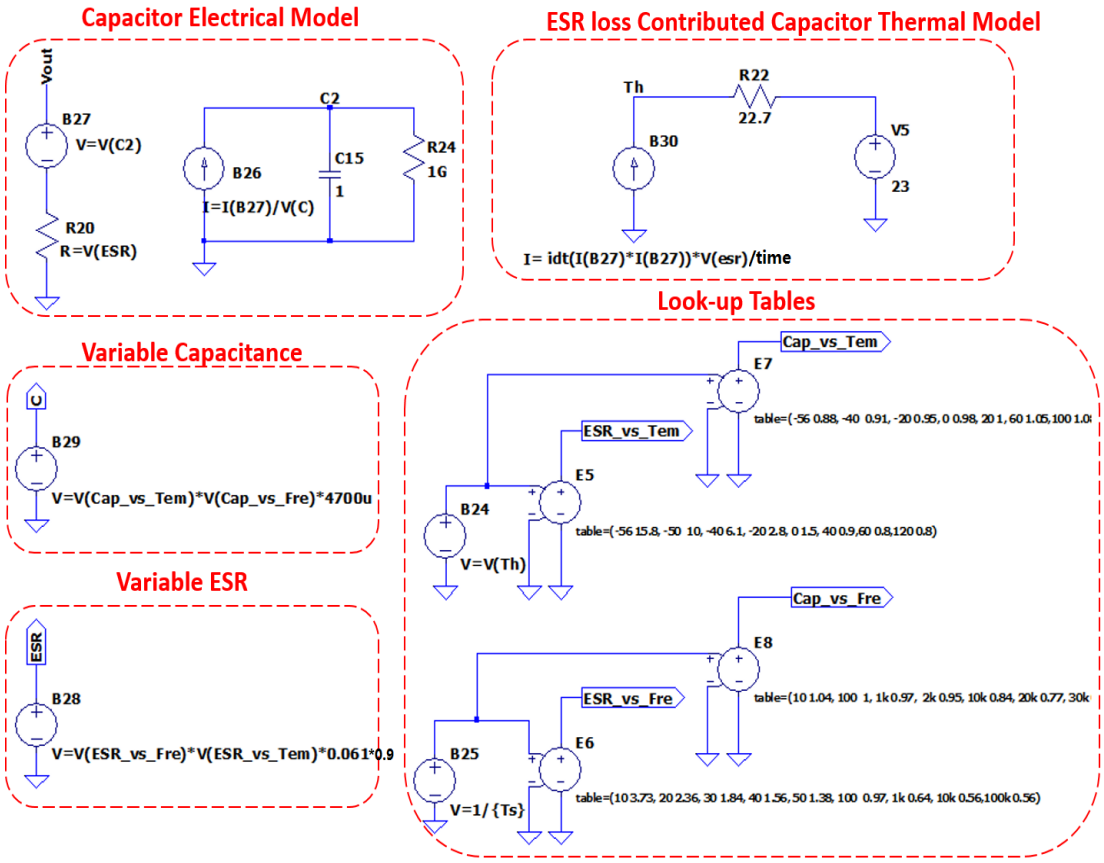


Fig. 2.5 Proposed electro-thermal model of a capacitor with variable capacitance and ESR.

Look-up tables, Cap_vs_Tem, Cap_vs_Fre, ESR_vs_Tem and ESR_vs_Fre, where they indicate the impacts of temperature and frequency on the change of capacitance and ESR in percentage respectively are extracted from the datasheet. The dominant losses of the capacitor are due to the ESR, which is calculated using (2.11) below. Due to the difficulty to measure and verify the capacitor internal hot-spot temperature, the capacitor shell temperature is estimated and measured. V_{th} represents the capacitor shell temperature.

$$P_{c,loss} = R_{ESR}(f_s, T_{cap}) \cdot i^2_{c,RMS} \tag{2.11}$$

Unlike the inductors which usually have detailed information in the datasheet, capacitors are usually only provided with limited information, such as dissipation factors (DF). DF

represents the ratio of the resistance to the reactance tan δ of a capacitor at 100 or 120 Hz, and is treated as an indicator to evaluate the capacitor quality. Since both the capacitance and the ESR are frequency and temperature dependent, DF at a fixed value can hardly reflect the real status of a capacitor. Hence, efforts are needed to construct look-up tables. Simple experimental methods, for example, are proposed in [59].

2.4 ETM Simulation and Experimental Results

To validate the correctness of the ETMs proposed for the components, experiments are implemented. These include the converter operating with different loads and frequencies. Since the temperature fluctuations of a device are directly related to its key parameter, for instance, MOSFET $R_{ds,on}$, if the estimation on this value is inaccurate, nonidentical simulated and experimental results will be found at different power conditions. Therefore, the accuracy of $R_{ds,on}$ can be confirmed. This, on the other hand, has also validated the accuracy of data-driven ETMs, as the key parameter is datasheet-informed. The verification method is also applicable to verify ETMs of other components. Fig. 2.6 shows the basic set-up of the experimental platform. The specifications of components and devices used in the prototype and testing are listed in Table 1.1. Due to the difficulty of measuring the real junction or hot-spot temperature of semiconductors and passive components, the inductor winding, capacitor top shell, and the case of MOSFET and diode are measured. In addition, as the temperature of the inductor core and winding are closely coupled, the winding temperature is collected. Both the electrical and thermal results from experiments are compared with the simulation results.

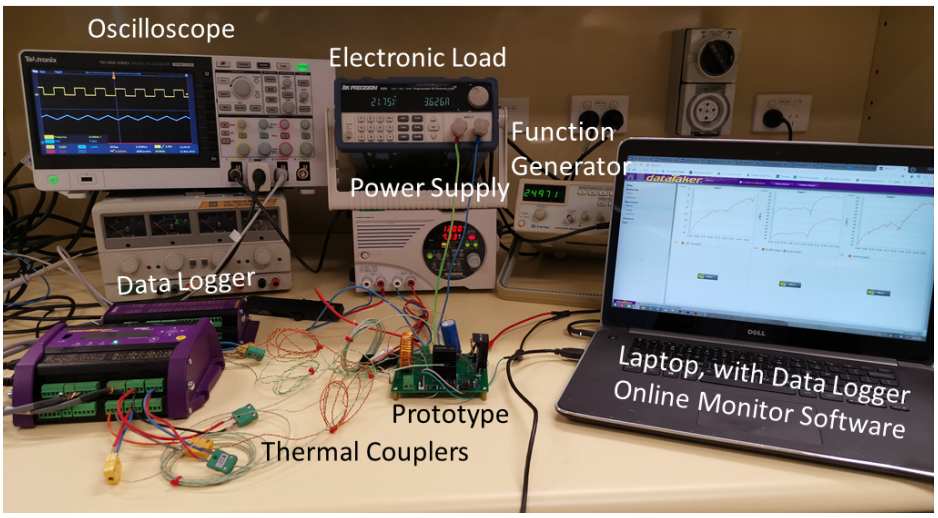


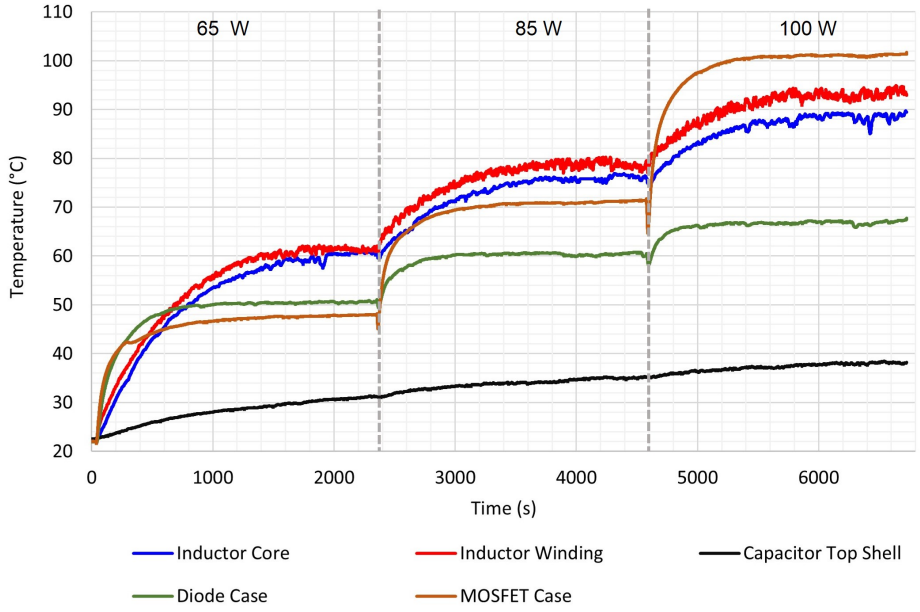
Fig. 2.6 Experiment platform used to evaluate the performance of the proposed ETM and ETAM of a boost converter.

2.4.1 Temperature estimation of each component

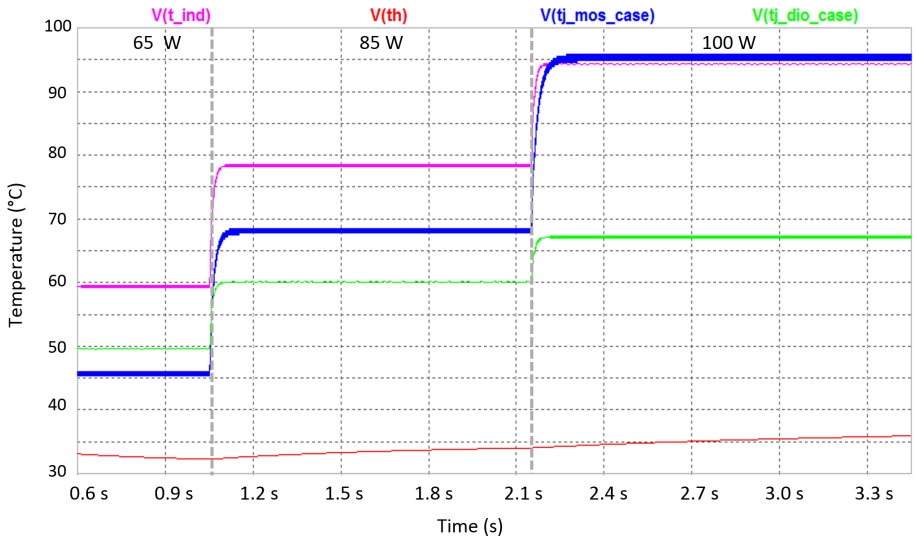
To verify the thermal performance of the proposed ETMs for the inductor and capacitor, simulation results are compared with experimental results. Selected experimental and simulation temperature waveforms are shown below for the boost converter under a 12 V input voltage, 0.5 duty cycle and 100 W input power operation conditions with 10 kHz and 25 kHz operation frequency. The 10 kHz experimental and simulation results are shown in Figs. 2.7a and 2.7b, respectively. Table 2.2 gives a comparison of the two results.

In addition, the 25 kHz boost converter temperature is added as a further validation. The simulation and experimental results are shown in Figs. 2.8a and 2.8b, respectively. A comparison of the two results is given in Table 2.3.

Good agreement can be observed by comparing the two results at two different frequencies and small mismatches exist may due to the measurement errors and a lack of considering the thermal coupling issue. More discussions on the results are summarized in Section 2.7.



(a) Experimental results of the measured MOSFET case, diode case, inductor core, inductor winding and capacitor top shell temperatures.



(b) Simulation results, where V(t_ind), V(th), V(tj_dio_case) and V(tj_mos_case) represent the estimated inductor surface, capacitor surface, diode case, and MOSFET case temperature, respectively.

Fig. 2.7 Experimental and simulated temperature results of power components in a boost converter with 10 kHz operation frequency, 0.5 duty cycle and 65/85/100 W input powers.

Table 2.2 Comparison between experiment and simulation results of a boost converter with 0.5 duty cycle, 10kHz operation frequency and 65W/85W/100W input power.

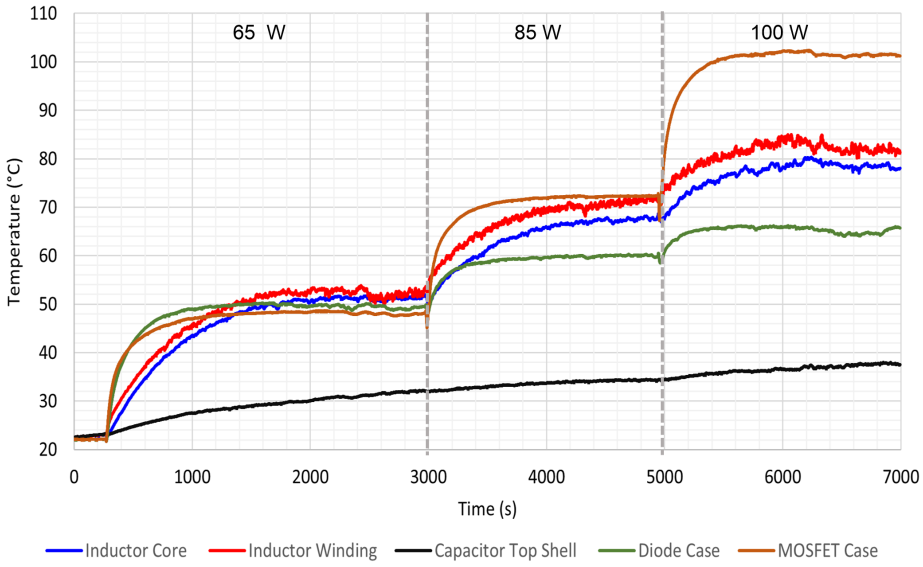
Input Power 65 W	**MOSFET**	**Diode**	**Inductor**	**Capacitor**
Experiment	47°C	50°C	60°C	30°C
Simulation	46°C	50°C	59°C	32°C
Input Power 85 W	**MOSFET**	**Diode**	**Inductor**	**Capacitor**
Experiment	70°C	60°C	76°C	35°C
Simulation	68°C	60°C	78°C	34°C
Input Power 100 W	**MOSFET**	**Diode**	**Inductor**	**Capacitor**
Experiment	101°C	68°C	90°C	38°C
Simulation	96°C	67°C	94°C	36°C

Table 2.3 Comparison between experiment and simulation results of a boost converter with 0.5 duty cycle, 25 kHz operation frequency and 65W/85W/100W input power.

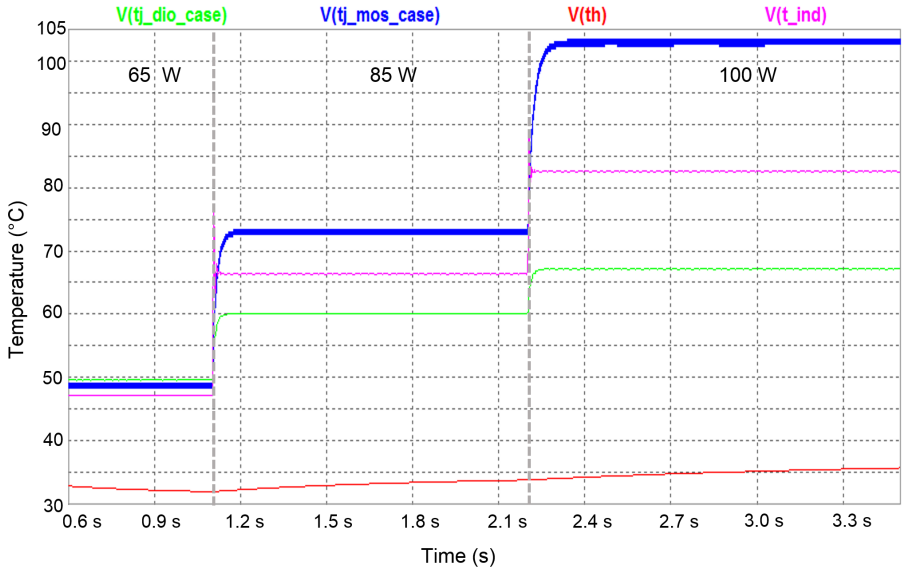
Input Power 65 W	**MOSFET**	**Diode**	**Inductor**	**Capacitor**
Experiment	48°C	50°C	50°C	30°C
Simulation	49°C	50°C	47°C	32°C
Input Power 85 W	**MOSFET**	**Diode**	**Inductor**	**Capacitor**
Experiment	72°C	60°C	68°C	34°C
Simulation	73°C	60°C	66°C	34°C
Input Power 100 W	**MOSFET**	**Diode**	**Inductor**	**Capacitor**
Experiment	101°C	67°C	80°C	38°C
Simulation	103°C	67°C	82°C	36°C

2.4.2 Comparison with conventional electrical model and experiment

To verify the ETM for the inductor with variable inductance, three inductor current waveforms driven by electro-thermal model i_{L1}, a normal SPICE inductor model with fixed 250uH inductance i_{L2}, and experiment i_{L3} are compared. Fig. 2.9a shows the comparison for a 10 kHz /100 W boost converter with 8.5 A average inductor current. As can be seen, the inductor current ripple in the experiment is higher than the constant inductance model i_{L2}. It is due to the high DC current induced; the inductance drops accordingly, and hence the



(a) Experimental results of the measured MOSFET case, diode case, inductor core, inductor winding and capacitor top shell temperatures.

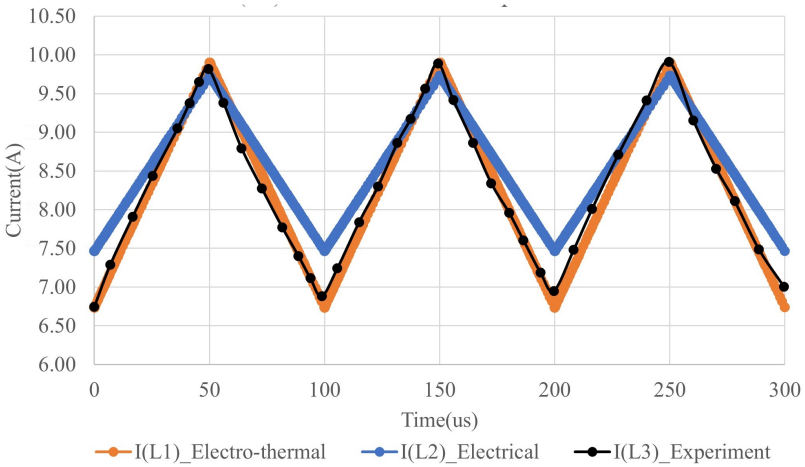


(b) Simulation results, where V(t_ind), V(th), V(tj_dio_case), and V(tj_mos_case) represent the estimated inductor surface, capacitor surface, diode case, and MOSFET case temperature, respectively.

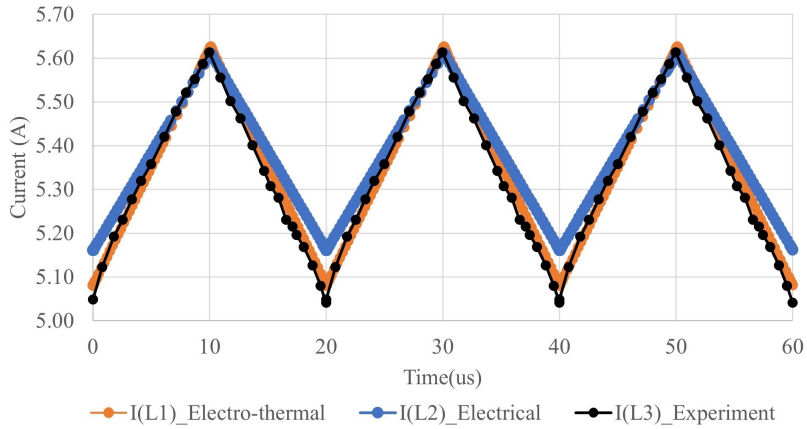
Fig. 2.8 Experimental and simulated temperature results of power components in a boost converter with 25 kHz operation frequency, 0.5 duty cycle and 65/85/100 W input power.

inductor current ripple is increased. In Fig. 2.9b, a 50 kHz/65 W boost converter with 5.3 A average inductor current is shown. Due to the increased operation frequency and lighter load

compared with Fig. 2.9a, the ripple increases a little. The ETM shows good agreement with the experimental results in both of the above two cases.



(a) 100 W boost converter with 10 kHz operation frequency.



(b) 65 W boost converter with 50 kHz operation frequency.

Fig. 2.9 A comparison of inductor current waveform generated by the proposed ETM i_{L1}, conventional electrical model i_{L2} and experiment result i_{L3} of (a) 100 W boost converter with 10 kHz operation frequency, and (b) 65 W boost converter with 50 kHz operation frequency.

To verify the ETM for the capacitor with variable capacitance and ESR, the output ripple voltages driven by the ETM, a normal SPICE capacitor model with fixed 4700 uF capacitance and 0.061 Ω ESR, and the experiment are compared in Fig. 2.10. As can be seen, the ESR drops by nearly half from the original value; the peak to peak value of the output ripple decreases, which is mainly contributed by the ESR. Similarly, the capacitance also drops as

can be seen from the capacitor charging rate. The proposed ETM matches the experiments compared to conventional models, however with small errors.

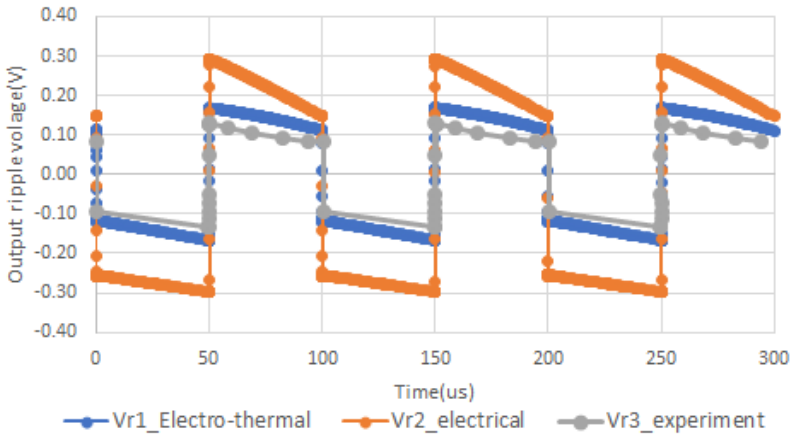


Fig. 2.10 A comparison of output voltage ripple waveforms generated by the proposed ETM Vr1, conventional electrical model Vr2 and experiment result Vr3 of a 100 W boost converter with 10 kHz operation frequency.

2.5 Method 2: Electro-Thermal Averaged Modelling

The aim of this section is to construct an ETAM of a converter to overcome the simulation time issue that occurs with an ETM, which with the increase of the switching frequency for higher power density design increases the simulation time accordingly. Simultaneously, fairly precise electrical and thermal performance estimations are also desired. The issue can be effectively solved by adopting an averaged model of the converter. As the conventional average model is neither frequency nor temperature dependent, which are the two key parameters in the ETM, modification is needed. Therefore, a modified electro-thermal averaged model (ETAM) of a boost converter considering self-heating of all devices is proposed. This is achieved by: a) adding additional behaviour models to calculate the device losses; b) replacing the fixed resistance of each component with a temperature dependent one; c) using variable inductor and capacitor instead of a fixed value counterpart to obtain an accurate electrical model and precise losses estimation, and d) forming electrical and temperature feedback loops for each component. The advantages of the proposed research are fast simulation speed, fairly accurate temperature prediction, ease of implementation, and the derivation method is universal and can be applied to any other converters or inverters.

Fig. 2.11 gives an overview of the proposed boost converter ETAM. The average model of a converter is employed to improve simulation speed. The electrical model and thermal model for each component are built, and then losses calculated from the electrical model and temperature from the thermal model are used to link the two. Therefore, an electro-thermal feedback loop is formed. The methodologies for constructing electrical models of semiconductors and passive components are different, and the details are explained in the following sections. However, the approaches to building thermal models are similar for all four components. The basic formula used in the thermal domain to estimate device temperature is by multiplying the losses and thermal resistance, and then add the room temperature $P_{loss} \cdot R_{th} + T_a$. To transfer this equation into the electrical domain, P_{loss} is represented by a

behaviour current source i_{Ploss}, thermal resistors are simply represented by electrical resistors, while the room temperature is expressed by a voltage source V_a. The thermal resistances of semiconductors usually include R_{jc} and R_{ca}, which represent the junction to case, and case to ambient thermal resistances respectively. For passive components, only R_{ca} is considered due to the difficulty of measuring their internal temperatures.

The main differences as compared to the conventional average model are: 1) the series resistance of each component is no longer a fixed value but temperature-dependent, 2) the model includes the MOSFET switching losses in the average model, 3) inductor and capacitor with variable inductance and capacitance are introduced respectively, and 4) the loss model and the thermal model are added to estimate the device thermal performance. The detailed derivation methodologies for MOSFET, diode, inductor and capacitor are explained as follows.

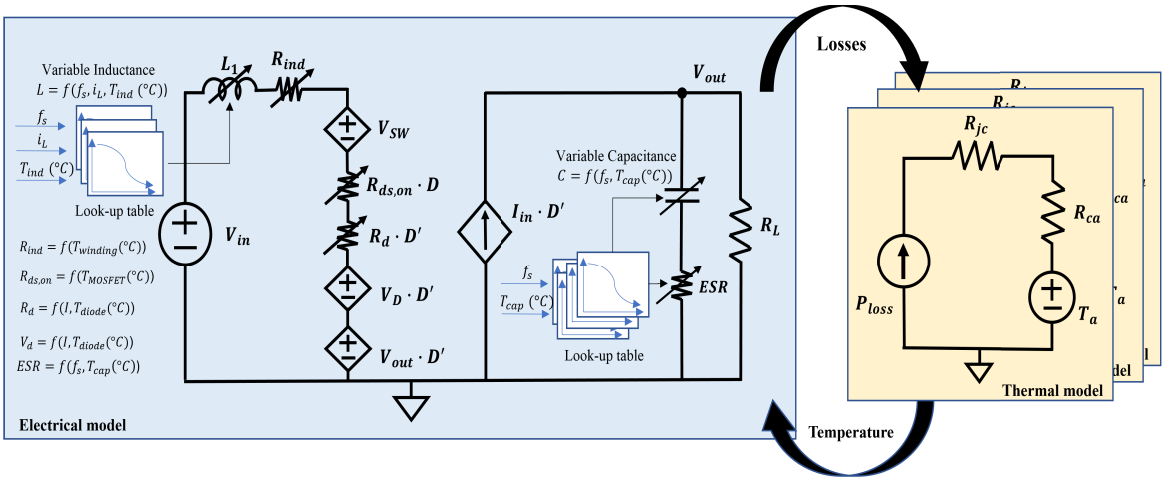


Fig. 2.11 An overview of the working principle of the proposed electro-thermal average model of a boost converter.

2.5.1 MOSFET

ETMs for semiconductors are well-developed by leading manufacturers and researchers [18], [36], [45]. Hence, this work, based on the framework in [36] applies the concept to develop the proposed average model. In the conventional average model, the MOSFET is replaced by its turn-on resistance $R_{ds,on}$. However, $R_{ds,on}$ is seriously affected by temperature in a real scenario. In addition, no switching losses are considered in an average model when calculating MOSFET losses, since the model is frequency independent. It is impractical to neglect it, especially when a MOSFET operates at high frequency. Besides this, high switching losses are also expected for SiC MOSFETs for their capability of handling high blocking voltage [61]. Hence, a variable resistor in series with an extra voltage source is used to indicate the temperature-related $R_{ds,on}$ and the extra voltage drop V_{sw} caused by switching losses. $R_{ds,on}$ is calculated using (3.1). Since the switching loss of a MOSFET can be estimated by (2.12) below, a behaviour voltage model is used to indicate the switching loss caused voltage drop. In addition, the averaged conduction loss resulted from the $R_{ds,on}$ during the MOSFET on-state in one switching cycle is calculated using (2.14) below. The quantities $i_{m_{rms}}$, D, f_s, T_r, T_f, I_{in}, V_{out} in (2.12)-(2.14) indicate the MOSFET RMS current, converter duty cycle, frequency, MOSFET turn-on rise time, MOSFET turn-off fall time, input current, and the drain-source voltage of the MOSFET when it switches off.

$$P_{sw} = 0.5 \cdot f_s \cdot (T_r + T_f) \cdot V_{out} \cdot I_{in} \tag{2.12}$$

$$V_{sw} = 0.5 \cdot f_s \cdot (T_r + T_f) \cdot V_{mid} \tag{2.13}$$

$$P_{cond} = i_{m_{rms}}^2 \cdot R_{ds,on}(T_{mj}) \cdot D \tag{2.14}$$

2.5.2 Diode

Similarly, the diode model proposed by STMicroelectronics in the application notes [60] is adopted. A voltage source V_d in series with a resistor R_d are adopted, and they are used to represent the temperature-dependent forward voltage drop (2.2) and the change of series resistance (2.3). For the diode loss model, only the dominant conduction losses are considered, and are calculated by using (2.15) below to estimate the diode junction temperature T_{dj}. The diode RMS current is i_{Drms}.

$$P_d(T_{dj}) = R_s(T_{dj}) \cdot i_{Drms}^2 + V_f(T_{dj}) \cdot i_{Drms} \tag{2.15}$$

2.5.3 Inductor and capacitor

The derivation principles of the variable inductor and capacitor are the same as in Section 2.3.3 and Section 2.3.4, respectively.

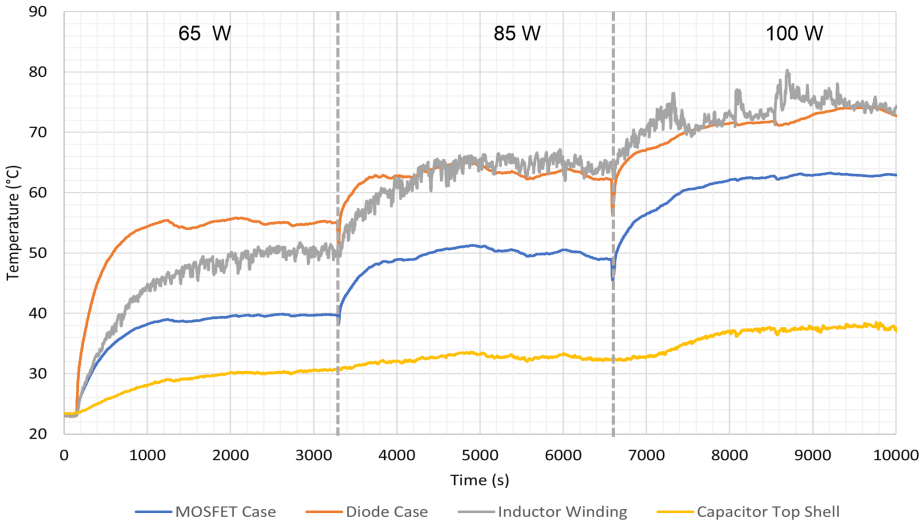
2.6 ETAM Simulation and Experiment Results

Experiments are implemented to verify the proposed modified ETAM of a boost converter, employing a similar experimental platform as shown in Fig. 2.6, and utilizing the same specifications of components listed in Table 1.1.

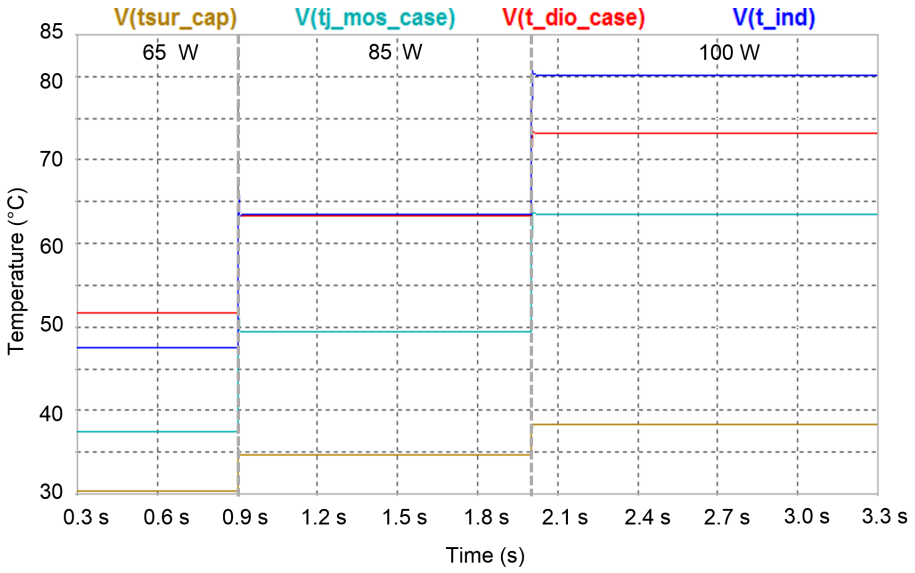
2.6.1 Temperature estimation for each component

To evaluate the thermal performances of the proposed ETAM, a boost converter operating at 25 kHz, with 12 V input voltage, 0.5 duty cycle, and 65 W/ 85 W/ 100 W input power levels is tested first. Due to the difficulty in measuring the real hottest point of components, inductor winding, capacitor top shell, and the case of MOSFET and diode are measured. In addition, as the temperature of the inductor core and winding are closely coupled, only the

winding temperature is collected. Experimental and simulation results are shown in Figs. 2.12a and 2.12b respectively. A summary of the two results is given in Table 2.4.



(a) Experimental results of the measured MOSFET case, diode case, inductor winding and capacitor top shell temperatures.



(b) Simulated temperature results, with V(t_ind), V(tsur_cap), V(tj_dio_case) and V(tj_mos_case) representing the estimated inductor surface, capacitor surface, diode case, and MOSFET case temperature, respectively.

Fig. 2.12 Experimental and simulation results of the temperature of power devices in a boost converter with 25 kHz operation frequency, 0.5 duty cycle and 65 W, 85 W and 100 W input power.

Table 2.4 Comparison between experiment and simulation results of a boost converter with 0.5 duty cycle, 25kHz operation frequency and 65W/85W/100W input power.

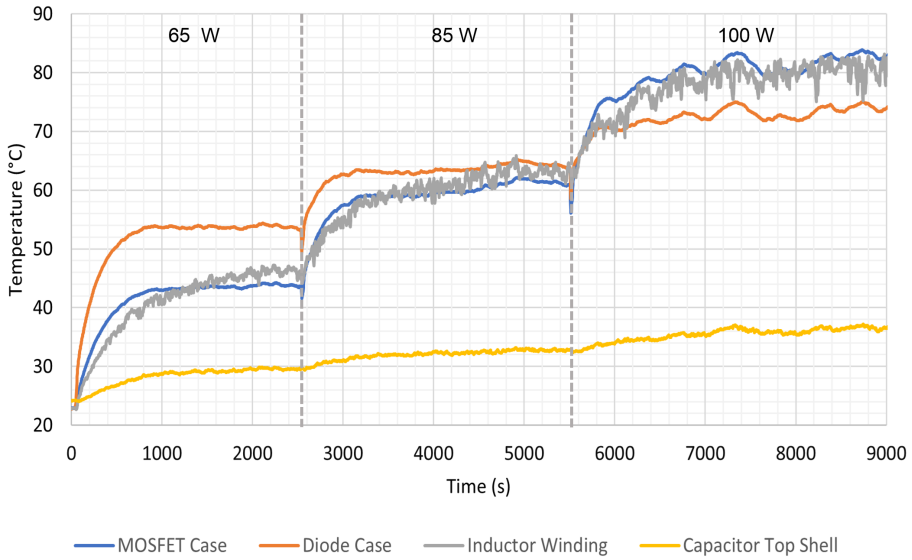
Input Power 65 W	**MOSFET**	**Diode**	**Inductor**	**Capacitor**
Experiment	40°C	55°C	50°C	30°C
Simulation	37°C	52°C	47°C	30°C
Input Power 85 W	**MOSFET**	**Diode**	**Inductor**	**Capacitor**
Experiment	50°C	63°C	65°C	33°C
Simulation	50°C	64°C	64°C	35°C
Input Power 85 W	**MOSFET**	**Diode**	**Inductor**	**Capacitor**
Experiment	63°C	72°C	75°C	38°C
Simulation	64°C	73°C	80°C	38°C

To further investigate the accuracy of the temperature estimation by the proposed model, experiments on a boost converter operating at 200 kHz with different loads are carried out. The simulation and experimental results are shown in Figs. 2.13a and 2.13b respectively. A summary of these two results is given in Table 2.5.

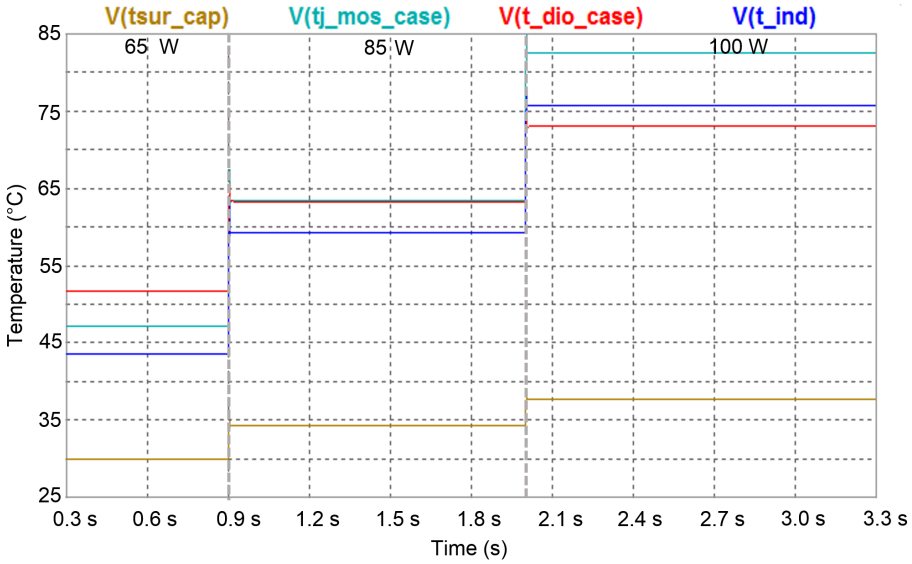
Table 2.5 Comparison between experiment and simulation results of a boost converter with 0.5 duty cycle, 200 kHz operation frequency and 65 W/85 W/100 W input power.

Input Power 65 W	**MOSFET**	**Diode**	**Inductor**	**Capacitor**
Experiment	47°C	54°C	46°C	30°C
Simulation	47°C	52°C	44°C	30°C
Input Power 85 W	**MOSFET**	**Diode**	**Inductor**	**Capacitor**
Experiment	64°C	64°C	63°C	33°C
Simulation	64°C	64°C	60°C	34°C
Input Power 85 W	**MOSFET**	**Diode**	**Inductor**	**Capacitor**
Experiment	82°C	73°C	80°C	37°C
Simulation	83°C	73°C	76°C	37°C

Comparing the results in Tables 2.4 and 2.5, good agreement between the predicted and measured temperatures can be observed. The temperature errors of the proposed model are within 5°C, and the maximum errors occur in the inductor prediction. The discrepancy may



(a) Experimental results of the measured MOSFET case, diode case, inductor winding and capacitor top shell temperatures.



(b) Simulated temperature results, with V(t_ind), V(tsur_cap), V(tj_dio_case) and V(tj_mos_case) representing the estimated inductor surface, capacitor surface, diode case and MOSFET case temperature respectively.

Fig. 2.13 Experimental and simulation results for the temperature of power devices in a boost converter with 200 kHz operation frequency at 23 °C room temperature, 0.5 duty cycle and 65 W, 85 W and 100 W input power.

be due to the lack of consideration of thermal conduction coupling among components and to measurement errors. Moreover, the accuracy of MOSFET switching loss model can also

be validated, since the operation frequency increases greatly from 25 kHz to 200 kHz while the estimated temperatures remain almost the same as to the experimental results.

2.6.2 Comparison with conventional electrical model and experiment

To validate the electrical performance of the proposed model, the inductor current and output voltage ripple are measured and compared with the simulation results.

Fig. 2.14 gives the measured inductor currents of a 100 W boost converter at 10 kHz and 25 kHz. As can be seen, the average input currents for both cases are around 8.5 A, while the current ripples are 3 A and 1.28 A, respectively. When comparing to the experimental results presented in Fig. 2.9a under the same operation condition at 10 kHz and 100 W power, the average current is almost the same, but the current ripple in Fig. 2.9a is slightly smaller from 6.8 A to 9.9 A. It is possibly due to the small mismatch of the power difference between these two experiments. Fig. 2.15 shows simulation results of the converter with 65 W, 85 W and 100 W input power (a) at 10 kHz, and (b) at 25 kHz. I(iL_ripple), I(Vin) and V(L) represent the inductor ripple current, average input current and inductance, respectively. As can be seen, the ripple currents in simulations are 3.15 A and 1.29 A for 10 kHz and 25 kHz, respectively. Small errors exist, however, compared with the case of constant 250 uH inductance which gives ripple currents at 2.1 A and 0.84 A for 10 kHz and 25 kHz operation frequency, respectively. The proposed variable inductor gives a much better and closer result because the proposed model is able to reflect the drop in inductance when DC bias current increases.

Fig. 2.16 shows the measured output voltage ripple of a 100 W boost converter operating at 10 kHz, valued at about 250 mV. Almost Identical experimental results can be found when comparing Figs. 2.10 and 2.16. Fig. 2.17 indicates the simulated output ripple V(vr), capacitance V(c), and the ESR of a 65 W/85 W/100 W boost converter at 10 kHz. The simulated output ripple is around 280 mV, which is slightly higher than the experimental

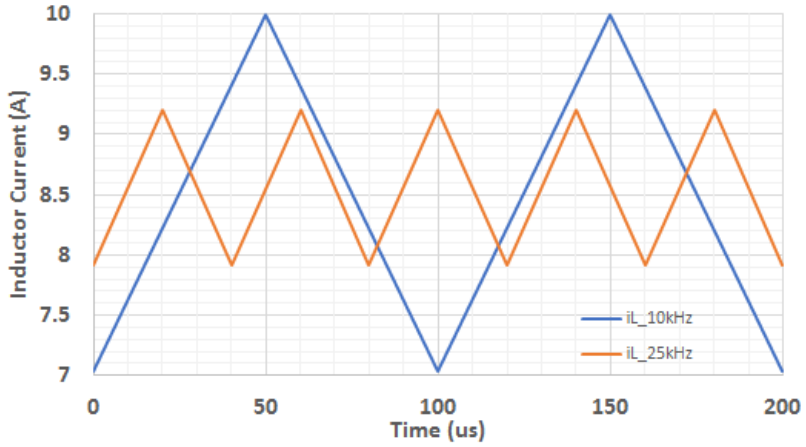


Fig. 2.14 Measured inductor current waveform of a boost converter operating at 12 V input voltage, 100 W input power, duty cycle 0.5, at 10 kHz and 25 kHz.

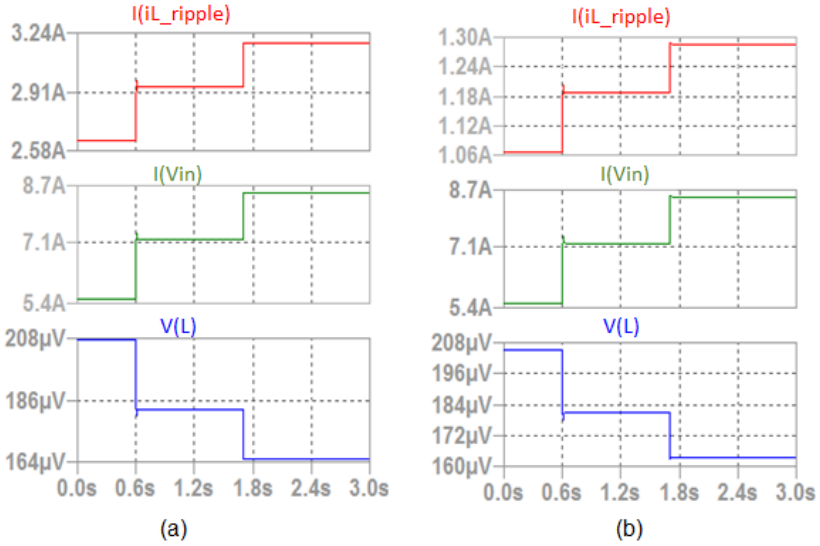


Fig. 2.15 Simulated inductor ripple current, input average current and inductance of a boost converter operating at 12 V input voltage, 65 W, 85 W and 100 W input power, duty cycle 0.5 (a) at 10 kHz, and (b) at 25 kHz.

result. In addition, both the simulated capacitance and ESR are much smaller than their initial values, which are 4700 uF and 0.061 Ω, respectively. The ESR drops to less than half of its initial value, mainly due to the influence of frequency. The change in capacitance can be seen from the charging rate. The simulation results show good agreement with the experimental results, and with reasonably small errors.

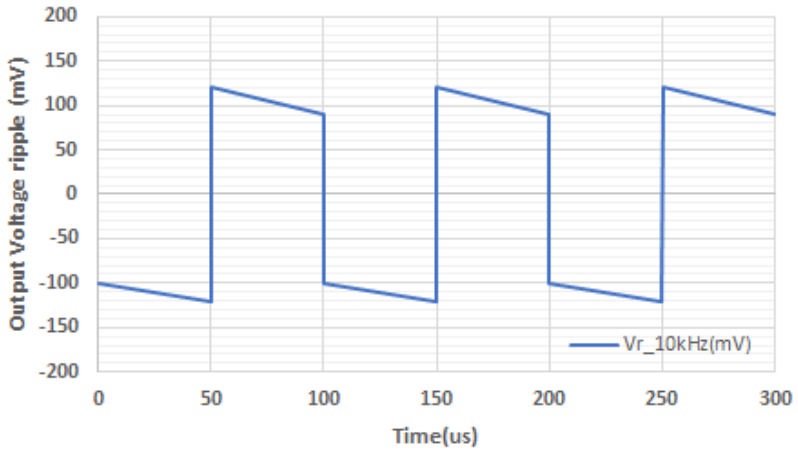


Fig. 2.16 Measured output voltage ripple waveforms of a boost converter operating at 12 V input voltage, 100 W input power, duty cycle 0.5, at 10 kHz.

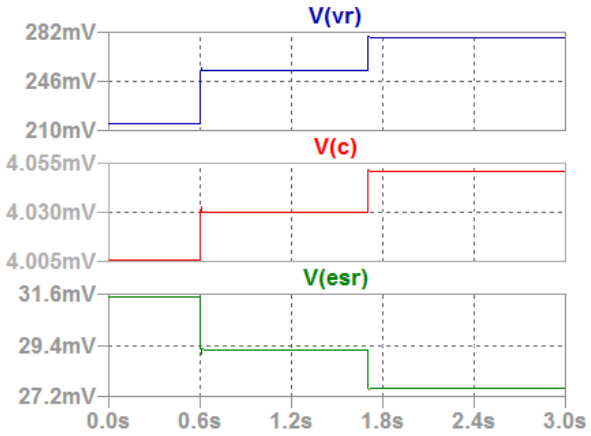


Fig. 2.17 Simulated output ripple voltage, capacitor capacitance and capacitor ESR of a boost converter operating at 12 V input voltage, 65 W, 85 W and 100 W input power, duty cycle 0.5 at 10 kHz.

2.7 Evaluation and Discussion of ETM and ETAM

2.7.1 Mismatches in temperature estimation

One common advantage of the two proposed models is that they are data-driven, and hence deep understanding of the magnetics or complex capacitor construction is not required. However, device datasheets do not cover all operating conditions and may contain errors. In this case, weighting coefficients can be added, as the data points reflect a genuine relationship

between two or more parameters under study. Similarly, additions can be made to indicate the impacts of internal hot spots of capacitor or inductor on parameteric drift. Small errors also exist between the experimental results and the simulation results partly due to the lack of consideration of thermal conduction coupling and measurement errors.

In addition, nonidentical thermal results can be observed when comparing experimental results of ETM and ETAM operated at the same frequency of 25 kHz and the same power references (65W, 85W and 100W). And it is particularly noticeable in the MOSFET results. The reason for causing this discrepancy is that different thermal resistances R_{ca} of the MOSFET are used in these two experiments. Although they share the same experimental platform, due to the loose of thermal coupler, which is attached to the center position of the MOSFET case by thermal adhesive, after many large temperature fluctuations cycles, there was a need of attaching them again in the second group of experiments. Therefore, different thermal resistances are applied in these two sets of experiments. The errors between these two thermal resistances are possibly due to the mismatch of the attached positions of thermal couplers, nonidentical amount of adhesive and thermal grease were used resulting different void spacing between MOSFET and heat sink and heat transfer capability respectively etc. All of these will result in a difference in thermal resistance. Nevertheless, these two models follow the same equations, and identical experimental results and simulation results can be found at these two sets of experiments respectively. Therefore, both the two models are accurate, and if identical thermal resistances are applied, they should provide the same simulation results.

Moreover, the proposed ETM and ETAM do not capture the actual thermal responses of the converter owing to a lack of considering the thermal capacitances of heat sinks, inductor and capacitor as discussed in Section 2.3. This can be found by comparing their transient performances and time scales of the simulated and experimental results.

2.7.2 Simulation speed

To evaluate the simulation speed, the elapsed time of running a 3.5 seconds simulation with different frequencies at 10 kHz, 25 kHz and 200 kHz of the established ETM and ETAM of a boost converter are compared and summarized in Table 2.6. The simulation is carried out in LTspice® XVII in a laptop computer, with Inter(R) Core(TM) i7-7600U CPU. As can be seen, the simulation speed is improved dramatically by utilizing the averaged model, being 2340 times faster at 10 kHz, and more than 7300 times at 25 kHz. It can be concluded that with the increase of frequency, the speed can be improved further. In addition, the simulation time of a switching model is increased accordingly and significantly with the operation frequency, while in the average model the increase is much smaller. Note that, the different thermal resistances applied to these two models will not affect the comparison of simulation time here. As the elapsed time is determined by the complexity of a simulated circuity instead of a specific thermal resistance value.

Table 2.6 Comparison of elapsed time to run a 3.5 second simulation of ETM and ETAM at different frequencies.

Frequency	10 kHz	25 kHz	200 kHz
ETM elapsed time	2246.9 s	7200 s +	-
ETAM elapsed time	0.96 s	0.985 s	2.067 s

2.8 Summary

In this chapter, two comprehensive electro-thermal modelling techniques are introduced for a boost converter.

An ETM is constructed firstly by adding extra behaviour models to the original power components to represent the variation of temperature-dependent parameters in the electrical domain, and to construct thermal R or R-C networks to estimate the temperature rise in the

thermal domain for all components. The advantages of this work are fairly accurate ETMs developed without the need for knowledge of complex device chemistry, together with ease of integration with existing electrical SPICE library software since they are constructed with basic behavioural models and circuits with values obtained from datasheet.

Secondly, an ETAM of a boost converter is derived to tackle the issue in the previous model that with the increase of operation frequency, the simulation speed decreases to a great extent. The model is obtained by employing variable parameters, such as variable inductor and capacitor, to represent the key power components, instead of using their fixed values. Modification is also undertaken to make the conventional averaged model frequency related. Due to the inclusion of the MOSFET switching losses and variable parameters, the simulation results are much closer to the experimental results compared to the conventional average model. The proposed model is time-efficient with reasonably accurate temperature and electrical performance estimations. The derivation methods are simple and universal, and hence allow users to develop their own models.

To evaluate the simulation accuracy, experiments are carried out on the performances of both electrical and thermal aspects. Discussions of the mismatches are depicted. In terms of simulation speed, the elapsed time of these two models implementing the same load are compared. A great improvement on the simulation speed of ETAM can be observed as compared to ETM.

Chapter 3

A MOSFET SPICE Model with Integrated Electro-Thermal Averaged modelling, Aging, and Lifetime Estimation

3.1 Introduction

Lifetime estimation of power semiconductor devices have been widely investigated to improve the reliability and reduce the cost of maintenance of power converters. However in most reported work, the aging effect is not considered in the lifetime evaluation process due to the omission or limitation of thermal cycle counting method. Additionally, the electrical/thermal simulation and lifetime estimation are usually implemented in different simulators/platforms, for the same reason. Thus, to tackle these problems, a concise but comprehensive MOSFET model that enables electro-thermal modelling, aging and lifetime estimation on LTspice® circuit simulator is proposed in this chapter. The idea comes from the fact that, MOSFET

on-state resistance $R_{ds,on}$ is not only temperature dependent, but also widely accepted as the device failure precursor. In other words, as it carries critical information about instantaneous temperature and aging progress. Hence, co-simulation can be achieved by constructing electrical, thermal, and aging and lifetime sub-modules exclusively first, and using $R_{ds,on}$, to build linkages among them. Averaged modelling technique, as developed in Chapter 2, is used and adopted here, due to the ease of establishing links among these three sub-modules, and fast simulation speed as compared to a switched converter model. Behavioral models are employed to realize the thermal cycles counting, stress accumulation and degradation evaluation. This chapter demonstrates that it is possible to use a single simulation software to monitor performances of devices and circuits, and their lifetime estimation simultaneously. High-stress thermal cycling and long-term random mission profiles are applied to verify the correctness of the model and to mimic a 10-year load respectively. An accelerated aging trend can be observed in the long-term mission profile simulation, which is in agreement with the theory. Facilitated by the employment of averaged circuits, the proposed method is a good simulation/analytical tool to implement a long-term mission profile that requires reliability assessment.

This chapter addresses the second objective of the thesis, and part of the contribution is published in [62].

3.2 Related Works and Research Gap

Reliability is one of the most challenging factors that needs thorough consideration when designing converters/inverters. It is especially critical for those devices which require to carry out challenging mission profiles while operating in severe environmental conditions. In addition, it has also attracted attention to future power supply design with increasing power density requirement. To avoid the downtime of power supplies and any catastrophic failures both electrically and economically, reliability assessment and prediction of useful lifetime

of power devices are widely investigated. By knowing the effective operation duration of devices, maintenance can be scheduled before the device fails. Hence, the reliability of the circuits and systems can be greatly improved, and the maintenance cost can be saved.

Recent research works focusing on device reliability and lifetime evaluation are reviewed. In [63], an experimental platform which allows concurrent execution of accelerated thermal cycling tests on multiple MOSFETs is built for reliability assessment. In [64], a MOSFET reliability model is proposed to predict $R_{ds,on}$ parametric drift through analyzing temperature distribution on the source metal so that the degree of degradation and lifetime of the MOSFET can be estimated. Experimental-based or endurance tests are traditional methods in assessing devices performance. They are reliable however the process is very time consuming. Long term and intensive tests are usually needed. Based on the device-level studies, lifetime descriptive model can be derived and they are widely employed in evaluating the lifetime of converters/inverters [3], [11]-[15], [34], [65]-[68]. In [11], a fast lifetime prediction simulation strategy based on conditions mapping (ambient temperature and load) and look-up tables (losses, junction temperature and load) is proposed for a SiC power module used in a PV inverter topology. In [12], an evaluation of bond wire fatigue of IGBTs in a PV inverter under a long-term operation are given. In [13], the lifetime of T-type and I-type power modules employed in 1500-V three-level PV inverters with different mission profiles and operation frequencies are evaluated respectively. In [14], the lifetime of a modular multilevel converter (MMC) with half-bridge as submodules operates in an offshore high voltage direct current offshore wind power system are studied. The impacts of comprehensive mission profiles on the lifetime of wind power converters are studied with an improved estimation method by considering different time scale thermal behaviors in [3]. Similarly, a comparative lifetime evaluation of several three-level converters with different modulation schemes are presented by simulating a 10-MW drivetrain [15]. In [34], the study investigates both impacts of installation sites and the PV panel degradation rate on the lifetime of the PV inverters.

In [65], a detailed wear-out failure probability analysis of a PV micro-inverter is presented aiming at identifying the weak point and improving the system reliability. In [66], the lifetime of a grid connected voltage source inverter is estimated, and a thermal resistance feedback system which reflects the device self-accelerating phenomenon is also introduced. In [67], an online evaluation of the consumed lifetime of a IGBT full bridge converter is presented through adopting the electro-thermal model, the physics-of-failure analysis and the real-time thermal counting algorithm. In [68], an online rainflow counting algorithm is also proposed to check the in-service operation of a three-level traction converter.

Although the aforementioned converters/inverters are applied to different applications in [11]-[15], [65]-[68], they follow a similar lifetime estimation procedure: 1. Apply environment profiles (e.g. ambient temperature, wind speed, etc.) and load profiles into inverter/converter in the circuit simulation tool (e.g. PLECS®, LTspice®, MATLAB, etc.), and get device junction temperature profile generated though ETM; 2. Input the temperature profile into a thermal cycle counting method to distribute the random cycles into different organized categories. The processed cycles information is utilized in the lifetime analytic model (e.g. Coffin-Manson law, etc.) and damage accumulation model to estimate the consumed and remaining lifetime. All the works in [11]-[15], [65]-[68] have considered the device damage phenomenon, however, only [66] - [68] have included this degradation into lifetime estimation. Nevertheless, instantaneous updating of thermal resistance caused by aging is not allowed in [66] due to the application of offline rainflow counting algorithm. While method used in [67] suits more for real-time estimation as it used real-time data which contains aging information already. The problem of offline counting in [66] is solved in [68], however, this method rely more on programming, but difficult to be adopted in circuit simulators as the proposed online rainflow counting algorithm is stack based.

As the device aging progress is in an accelerated trend, inclusion or exclusion of this process will cause a significant difference in estimation results. The estimated lifetime values

of IGBT which included and excluded aging process are 28.25 and 39.5 years respectively in [66]. In addition, it has also been pointed out that, the lifetime of an IGBT module not only is dependent on the stress level, but also on the current health state of a device [69]-[70]. Therefore, it will be of great benefit if the aging parameters can be monitored in the modelling process. Moreover, most of the studies above investigate the aging effects on the lifetime of IGBTs, however, few of them has taken discrete MOSFETs into account, which are also widely used in current power supplies. As these two devices are applied to different power rating applications, different packages are used. For instance, widely evaluated IGBTs are of the module design for its capability of high currents handling, while for the MOSFETs, discrete package (e.g. TO-220, TO-247, etc.) are more common. For this reason, aging impacts on different parameters of these two devices, for example, thermal resistance of IGBT modules, and $R_{ds,on}$ of MOSFETs are considered. Noted that, the aging does affect the thermal resistance R_{th} of a MOSFET, and R_{th} can be used as the failure precursor too. However, as compared to the R_{th}, the advantages of using $R_{ds,on}$ as healthy indicator are due to its higher sensitivity and ease of accessibility [71]. Hence, the aging of $R_{ds,on}$ should be considered.

To tackle this problem and to provide an alternative solution on an open-source or freeware platform particularly, a MOSFET model which contains three sub models, namely, electro-thermal averaged model, aging model, and lifetime analytic model is proposed in this chapter. Co-simulation of these three models and inclusion of aging effect can be achieved by forming feedback loops among MOSFET on-state resistance $R_{ds,on}$, junction temperature and accumulated stresses. While the lifetime of a device can be evaluated through assessing the degradation level or, in other words, the variation of the $R_{ds,on}$. Detailed derivation steps of this model are presented, and simulated results of both accelerated aging tests and long-term mission profile test are investigated and discussed.

3.3 Derivation principle of the proposed model

The aim of this work is to build a MOSFET SPICE model which can realize online simulation of electrical and thermal performances, degradation and lifetime estimation simultaneously.

An overview of the model operation principle is shown in Fig. 3.1. An averaged circuit of a power converter, i.e. a boost converter is taken as an example, is adopted to achieve time-effective electrical simulation, while the device temperature can be easily estimated by constructing a resistor thermal network. Combining these two models together, a complete ETAM is formed. The lifetime analytic model and MOSFET degradation model are added with the help of behavioral models. Instead of using a fixed $R_{ds,on}$ value in the electrical model, a variable which is a function of its initial electrical characteristic, temperature and aging effects is used. Through this approach, the feedback loops between any two models are formed. The complete circuitry of the proposed MOSFET SPICE model developed in LTspice® is shown in Fig. 3.2, while the derivation principles of sub-models contained in the model are discussed as follows.

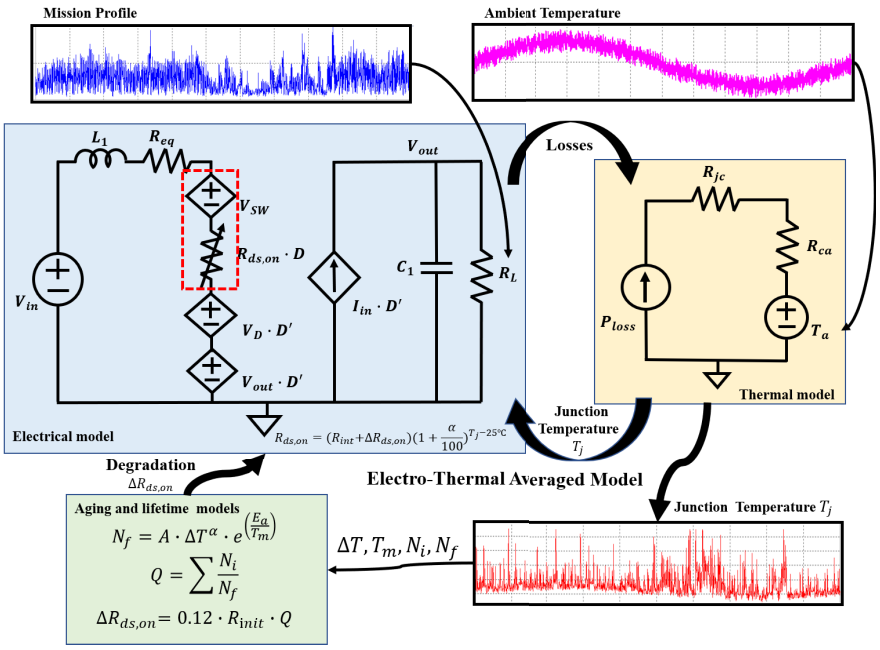


Fig. 3.1 An overview of the proposed integrated electro-thermal averaged modelling, aging and lifetime model.

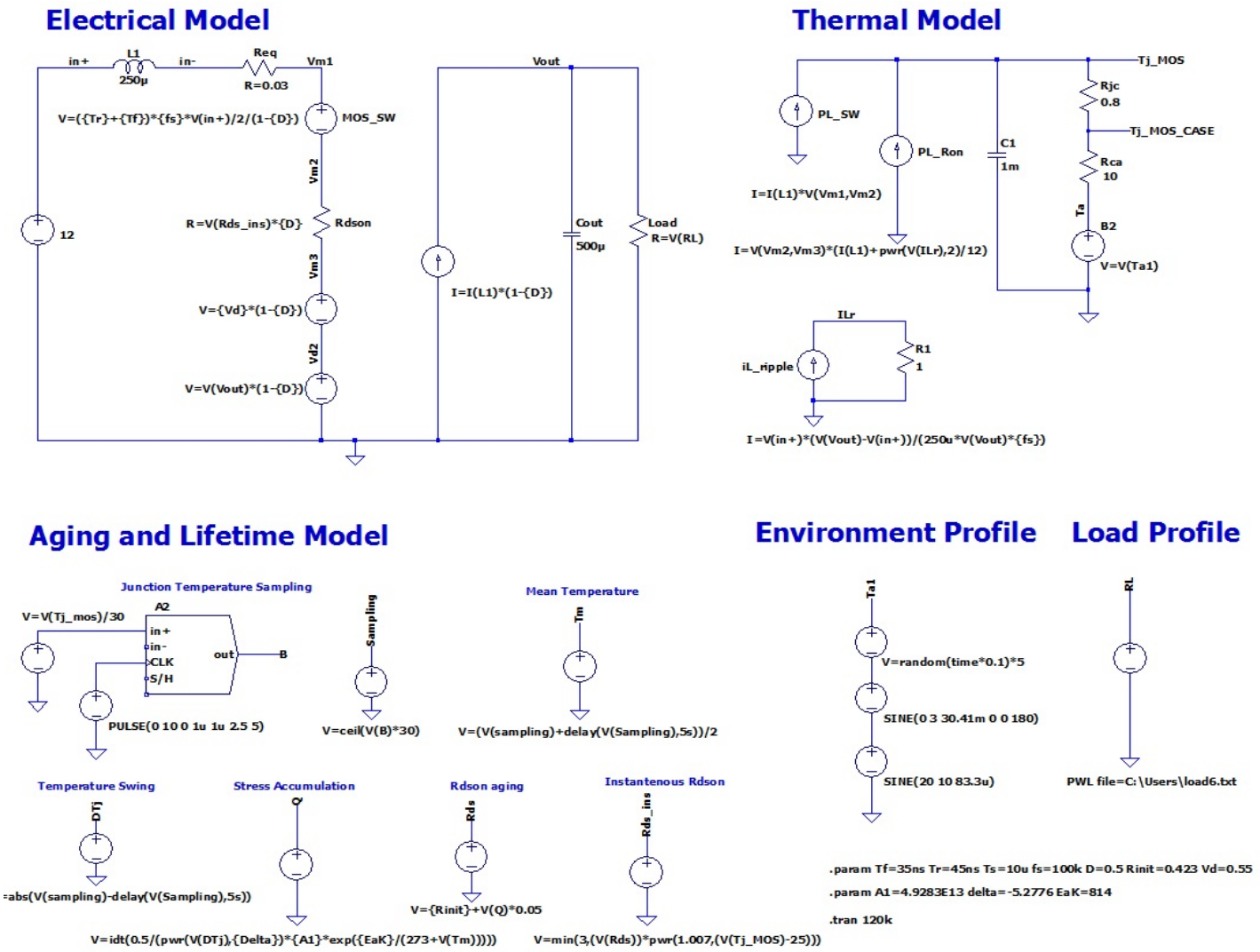


Fig. 3.2 The detailed circuitry of the proposed integrated electro-thermal average model, aging and lifetime model developed in LTspice®.

3.3.1 Derivation of the electro-thermal averaged model (ETAM)

The derivation and verification of the electro-thermal averaged model is based on the previous work developed in Section 2.5.1. This model mainly contains an electrical model and a thermal model, and they are linked by utilizing the characteristic that the MOSFET $R_{ds,on}$ is temperature dependent.

3.3.1.1 Electrical model

The derivation principle of the circuit is similar to the conventional averaged boost circuit. The inductor and diode series resistances are combined and represented by R_{eq}, V_D is the diode forward voltage drop, D and D' are namely the duty cycle and its inverse respectively. Additionally, two main modifications are made. First, the $R_{ds,on}$ is no longer a fixed value but is temperature and aging dependent. The value can be estimated by (3.1), in which, R_{init}, T_j, $\Delta R_{ds,on}$, and α indicate the initial $R_{ds,on}$ value, MOSFET junction temperature, degradation caused increment of resistance $\Delta R_{ds,on}$ and coefficient respectively. Two factors that contribute to the increase of T_j are conduction losses and switching losses. As the averaged model is switching frequency independent, while the switching losses play a significant role especially at a high frequency, the second modification is to induce the switching losses effects into the averaged model. The losses can be calculated by using (2.12), and can be represented by using an extra equivalent variable resistor ($R_{sw} = P_{sw}/I_{in}^2$) in the circuit. Alternatively, a simple extra voltage source V_{sw} by using (2.13) can be added as a result of (2.12). By doing so, the calculation steps can be saved. Regarding the conduction losses, it can be easily calculated from the RMS current, on-state duty cycle and the $R_{ds,on}$ of the MOSFET using (2.14). All of the losses will be input into the thermal model to calculate the corresponding temperature rise.

$$R_{ds,on} = (R_{init} + \Delta R_{ds,on}) \cdot (1 + \frac{\alpha}{100})^{T_j - 25°C} \tag{3.1}$$

3.3.1.2 Thermal model

A simple thermal model is formed by injecting power losses into a resistance network. Both switching and conduction losses represented by two behavioral current sources PL_SW and PL_Ron are considered in Fig. 3.2, and input into two thermal resistances, namely, junction to case R_{jc}, case to ambient R_{ca} of MOSFET. Noted that, since the averaged model considers the steady state operation, thus, instead of using conventional RC foster or cauer thermal network, only R is considered here. The T_a represented by a voltage source is the ambient temperature. In simulation, a constant temperature is used for the accelerated tests. While for the long-term mission profile simulation, T_a, which composed of daily and annually information with some noises is adopted, to mimic a more realistic environment profile. It is made by merging two sine waves with some randomly generated noises. Alternatively, it can be achieved by importing a real environment profile.

3.3.2 Derivation of lifetime analytical model and aging model

In addition to its temperature-dependent characteristic of MOSFET $R_{ds,on}$, it is also widely accepted as a device failure precursor. In other words, $R_{ds,on}$ contains device degradation information too. Thus, advantage can be taken by adding the degradation effects into the derived ETAM. Another benefit of employing the averaged circuit over the switching-mode circuit is that, it is well suited for simulating long-term mission profile due to its fast simulation speed.

3.3.2.1 Lifetime Analytical Model

In order to evaluate the lifetime of MOSFET, the widely accepted Modified Coffin-Manson law (1.4) is adopted to evaluate the device failure cycles, and Miner's rule (1.6) is employed to evaluate the stress that a device has undertaken after a number of thermal cycles as described in Sections 1.3.2 and 1.3.3.

To calculate the above two equations, it is necessary to count thermal cycles and to collect the ΔT_j and T_m data in each cycle. Counting algorithms, such as, half-cycle, maximum-edge, and the rainflow counting methods are widely adopted and compared [40]. The rainflow counting method is the most popular one with high accuracy. However, it usually needs to be applied offline as a complete thermal profile is required. Therefore it is not suitable to implement as an online algorithm in circuit simulation. In this chapter, the half-cycle peak through counting method which counts the cycle rising and falling slope as 2 half cycles is adopted. The detailed operation in simulation is to compare the T_j amplitude of the current thermal cycle to the previous one, and generate the difference ΔT_j and mean temperature T_m curves. The values are fed back to (1.4) and (1.6), and counted as half cycle.

3.3.2.2 Aging Model

An aging model is included in this work to compensate the Miner's rule, as the linear stress accumulation can hardly reflect the self-accelerating degradation process [66]. This can also be illustrated by interpreting the equation of Miner's rule in (1.6), where the total damage Q is the summation of every single stress that a device has suffered under each thermal cycle. Since this equation does not contain any aging factors, the stresses accumulated by a device at the early and end stages of its lifetime share the same value when operating with an identical mission profile. In other words, the accelerated degradation process is missing. A stress feedback model and a non-linear stress accumulation model are proposed in [66], [68] and [72] respectively to reflect the IGBT degradation performances. In this work, the feedback method is adopted, since the nonlinear method suits more for the IGBT thermal resistance failure mechanism which has a long crack initiation stages but will be propagated fast after reaching a certain limit. While for MOSFETs, although the aging is similarly in an exponential trend, the growing is not as steep as IGBT. Based on the study in [63] and [64],

the aging of MOSFETs can be observed through monitoring the increment of $R_{ds,on}$. Two different models are proposed by them to represent this phenomenon.

In [63], an exponential degradation model represented by (3.2) is proposed based on the experimental results, as shown in Fig. 3.3, where α and β are coefficients which can be obtained through using curve fitting tool, and R_{init} is the initial $R_{ds,on}$ value. Therefore, the incremental $\Delta R_{ds,on} = \alpha e^{\beta t}$.

$$R_{ds,on}(t) = \alpha e^{\beta t} + R_{init} \tag{3.2}$$

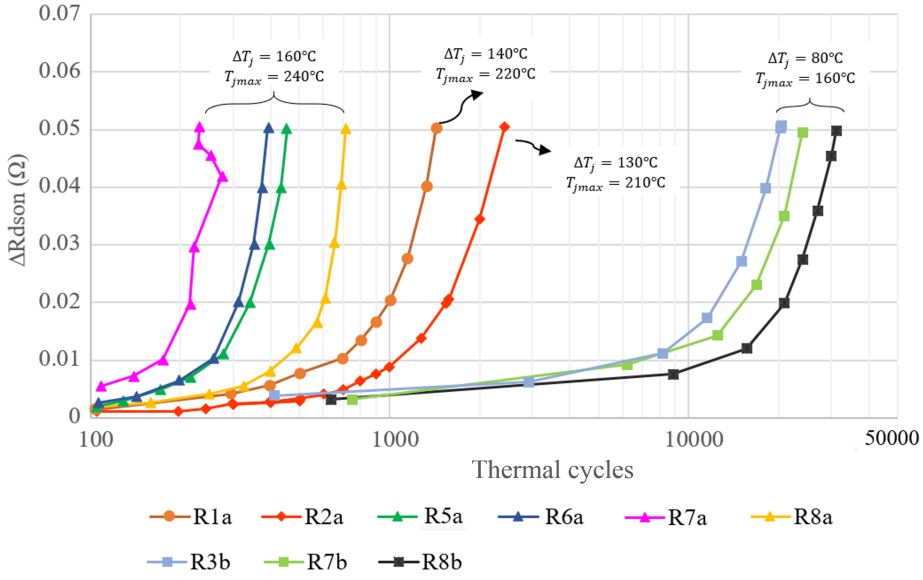


Fig. 3.3 Replotted experimental results from [73] of online $\Delta R_{ds,on}$ monitoring during thermal cycling under three different conditions: (A) $\Delta T_j = 160$ °C, $T_{max} = 240$°C (R5a-R8a) (B) $\Delta T_j = 140$°C, $T_{max} = 220$°C (R1a), (C) $\Delta T_j = 130$°C, $T_{max} = 210$°C (R2a), and (D) $\Delta T = 80$°C, $T_m = 120$°C (R3b, R7b and R8b).

Since this model is derived from experimental results, a direct deployment as such can effectively depict the degradation of the device. However, different stresses will give different degradation performances, which will result in different α and β values. In other words, one group of α and β values is only suitable for a certain stress operation. This will bring difficulties in calculating the accumulated stress when a practical mission profile is applied.

To solve this problem, a Remaining Useful Lifetime (RUL) estimation method is proposed in [73] through using Kalman filter and online computation to continuously update these two values. A random sample consensus (RANSAC) algorithm coupled with a sliding window method are proposed in [74] to delete outliers and to track some nonlinear samples in the experiment data respectively to improve the RUL estimation accuracy. These two methods focus on improving the accuracy of predicting the aging growing trend or failures on real data sets, as they are capable of dealing with sampling noises, hence, they are more suitable for real-time prognosis.

In this work, a straightforward approach to approximate α and β values is proposed to give a general estimation. By taking the natural logarithm of both sides of $\Delta R_{ds,on} = \alpha e^{\beta t}$, it produces (3.3). A linear equation can be obtained, where t represents N_i cycles, β is the slope and α is the initial value. To verify this, degradation data points of cases (A)-(C) in Fig. 3.3 are extracted, and the α and β values are obtained through curve fitting. Following (3.3), the sample points are replotted in Fig. 3.4, which all three cases show almost linear growing trend. Another thing that worth noticing is that, the initial increments of $\Delta R_{ds,on}$ remain small for all devices under different stress levels. This can be observed from both Figs. 3.3 and 3.4, where the $\ln(\Delta R_{ds,on})$ ranges from -7 to -6, which is equivalent to 0.00091 to 0.00245. The range may contain small mismatches as compared to the real experimental results due to extraction errors, however, it still gives an insight into the estimation. Hence, an assumption is made that a small and fixed α value 0.0015 which is when $\ln(\Delta R_{ds,on}) = -6.5$ is applied to all cycles, such that, the β can be easily calculated by taking the preset maximum allowed $\Delta R_{ds,on}$ value, N_f for a certain stress into the equation. Hence, offline calculation of the β parameter is achieved in this work, and it has the potential to be computed online by forming its feedback loop with $\Delta R_{ds,on}$ in the circuit. Both of the curve fitted α, β values and the calculated ones are shown in Table 3.2, together with its corresponding N_f cycles.

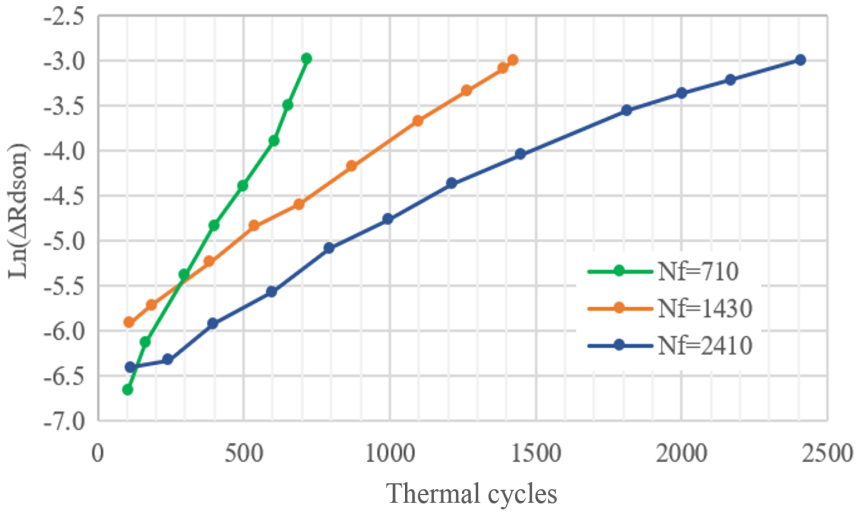


Fig. 3.4 Natural logarithm plot of $\Delta R_{ds,on} = \alpha e^{\beta t}$ with the N_f for cases: (A) $\Delta T_j = 160$ °C, $T_{max} = 240$°C, (B) $\Delta T_j = 140$°C, $T_{max} = 220$°C, and (C) $\Delta T_j = 130$°C, $T_{max} = 210$°C.

$$\ln(\Delta R_{ds,on}) = \ln(\alpha) + \beta t \tag{3.3}$$

In [64], the authors point out that the variation of $\Delta R_{ds,on}$ can be related to the accumulated stress Q. A maximum $\Delta R_{ds,on}$ of 0.2 p.u. of its initial $R_{ds,on}$ is set as the upper limit of a device before it is actually failed. Hence, the development of stress related aging model can be represented by (3.4).

$$\Delta R_{ds,on} = 0.2 \cdot R_{init} \cdot \sum_{i=1}^{n} \frac{N_i}{N_f} = 0.2 \cdot R_{init} \cdot Q \tag{3.4}$$

As discussed above, coefficients in the exponential equation may differ from one to another due to different stresses. In contrast, this approach gives a more simple and general solution as it is stress related.

All of these three aging models, namely, the exponential degradation model proposed by [63], the modified exponential model by authors, and the stress related model by [64] will be evaluated and discussed in Section 3.4.

3.3.3 Description of LTspice® Functions used in the circuit

A few functions employed in the behavioral current or voltage sources are explained in Table 3.1, and the description can be found from [75]. Another special symbol A2 adopted in the aging and lifetime model is the sample and hold function. Due to the maximum allowed sample voltage, which is 10 V, the MOSFET junction temperature needs to be scaled down before input to this function. It can be converted back to its original value by using the behavioral source.

3.4 Simulation Results

In this section, simulation results of the proposed MOSFET model with high stress thermal cycling mission profiles and a long-term random one are given. As the authors have provided very detailed experimental results and explanations in [73] based on the experimental platform built in [63], hence, in this work, the same MOSFET model IRFP340 with initial R_{init} at 0.423 ohm is used. Following this work, the degradation limit of $\Delta R_{ds,on}$ is set to 0.12 p.u. instead of 0.2 p.u., which is equivalent to 50 mΩ. Note that, the limit is user-defined and the

Table 3.1 Description and explanation of LTspice® functions used in the proposed model.

Function	**Description [75]**	**Purposes of these functions in the model**
ceil(x)	Integer equal or greater than x	filter out fraction for ease of calculation
idt(x)	Integrate x	accumulate stresses Q
delay(x,t)	x delayed by t	generate a waveform with t cycles delayed for comparison
abs(x)	Absolute value of x	calculate amplitude ΔT_j
random(x)	Random number between [0,1]	generate noises
min(x,y)	The smaller of x or y	limit $R_{ds,on}$

value does not necessary mean the device will be failed at that time, but indicate the device should be replaced soon. The values of parameters V_{in}, f_s, D, R_{eq}, and V_D in the open-loop converter operation are 12V, 100 kHz, 0.5, 0.03 ohm and 0.55V respectively.

3.4.1 High Stress Thermal Cycling Mission Profile

To verify the correctness of the proposed model, mission profiles which mimic the high stress thermal cycling experiments done in [73] is applied to the model first. Four cases are simulated here, A) $\Delta T = 160\ ^{\circ}$C, $T_m = 160^{\circ}$C, B) $\Delta T = 140^{\circ}$C, $T_m = 140^{\circ}$C, C) $\Delta T = 130^{\circ}$C, $T_m = 145^{\circ}$C, and D) $\Delta T = 80^{\circ}$C, $T_m = 120^{\circ}$C. Devices in this work are tested with extreme high temperatures that are above their specification limits, to accelerate devices' aging process and shorten the evaluation time. The testing follows techniques of accelerated accelerated life testing (ALT), which is frequently adopted in the reliability assessments. With ALT, the device failure mechanism, failure mode, mean time to failure, and design margin can be evaluated in a short term. Detailed information on ATL is presented in [76] and more examples of implementing and analyzing high temperature tests on power MOSFETs are presented in [30] and [77] respectively.

A simple electrical circuit is adopted here to achieve the thermal cycling simulation, by using a DC voltage source in series with the MOSFET $R_{ds,on}$ and a pulsating load. Only conduction losses need to be considered in this simulation and the pulsating load allows the device to reach the desired temperature swing ΔT and mean temperature T_m easily. The thermal and lifetime submodules remain unchanged. A constant ambient temperature $T_a = 25^{\circ}$C is assumed for all four cases in the simulation. Part of experimental results of cases (A) to (D) from [73] are replotted in Fig. 3.3, where multiple groups of testing results of cases (A) and (D) are given, while a single group of result of cases (B) and (C) is provided respectively. Noted that, due to the small discrepancies of devices in manufacture settings, degradation performances of devices differ from one to another. This can be observed from

the experimental results of both cases (A) and (D). Hence, selected experimental results are used to derive the coefficients δ and A_1 in (1.4), which are -5.2776 and 4.9283×10^{13} respectively given in [73]. Hence, the calculated N_f based on Coffin–Manson model (1.4) for above four cases are namely, 750, 1586, 2410, and 35200 cycles. Selected experimental results of cases (A)-(D) are R_{6a}, R_{1a}, R_{2a}, and R_{8b} from Fig. 3.3 respectively, as they match the calculated N_f better.

Table 3.2 Comparison of the N_f cycles among the experimental results, the calculated values and the proposed model with two different aging models respectively.

	ΔT_j	T_m	**Calculated** N_f	**Measured** N_f in [73]	**Experimental results**		**Proposed**		N_f **With Aging** $\Delta R_{ds,on} =$		
					$\alpha 1$	$\beta 1$	$\alpha 2$	β_2	$\alpha_1 e^{\beta_1 t}$	$\alpha_2 e^{\beta_2 t}$	0.05*Q
Case A	160	160	750	200-750	0.313E-3	6.93E-3	1.5E-3	4.67E-3	710	750	715
Case B	140	150	1586	1430	2.413E-3	2.124E-3	1.5E-3	2.21E-3	1430	1593	1480
Case C	130	145	2410	2410	2.696E-3	1.218E-3	1.5E-3	1.453E-3	2410	2390	2350
Case D	80	120	35.2k	20-35k	3.7E-3	8E-5	1.5E-3	9.95E-5	31.5k	35.5k	32k

To give an overview evaluation of the proposed model which embeds with the aforementioned three different aging models respectively, the N_f results of cases (A)-(D) of them are summarized and compared in Table 3.2. As can be observed, for the exponential model proposed by [63], since this model is based on the experimental results, where α_1 and β_1 values are extracted through curve fitting these devices aging waveforms, this method allows an effectively depiction of the aging of a device. For the exponential aging with the proposed α_2 and β_2 values, the simulated N_f fits the calculated N_f more for all cases as compared to the experimental results. It is because β_2 is obtained from the calculated N_f value. Hence, a conclusion can be made that, the accuracy of this method is in relation to the precision of N_f lifetime analytical models. While for the stress related model, it gives closer to the experimental results in most cases. However, a relatively bigger error in terms of the aging trend will occur in the high stress thermal cycling simulation as can be observed from Fig. 3.5, for example, maximum of 15 mΩ error can be found in case (A). The discrepancy is due to the intrinsic difference between using a linear or an exponential equation to represent the relationship between two parameters. Nevertheless, the error can be minimized in the long-term mission profile simulation, as to reach the maximum limit it needs hundreds of thousands of cycles. This conclusion can be found from observing case (A) to case (D). With the increase of N_f cycles, mismatches between simulation and experiments are reduced, from maximum of 15 mΩ to around 8 mΩ. Since, in relatively low stressed (e.g. case (D)) thermal cycling experiments, both the exponential and the stress related description models give flat growing trends. In other words, the stress related model will be more closer to the real exponential increasing trend, hence, less mismatches or errors when it is used to estimate the aging $\Delta R_{ds,on}$.

In addition, another experiment in [73] which investigates the $\Delta R_{ds,on}$ variation of a device under different stresses is also simulated. The operation is to keep T_m at 180°C, while changing the ΔT_j from 180°C to 140°C at 150 th cycle. The experimental result of

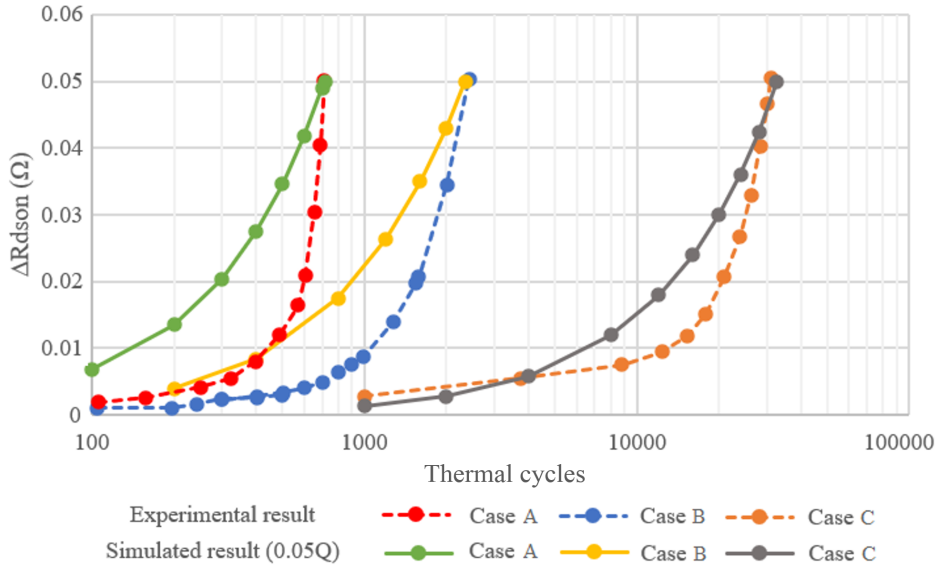


Fig. 3.5 A comparison of $\Delta R_{ds,on}$ aging performances between the simulated stress related model and the experimental results of cases (A), (C), and (D).

the $\Delta R_{ds,on}$ variation from [73] and the simulated results of both two models are shown in Fig. 3.6. As can be seen, to reach the 0.05 ohm limit of $\Delta R_{ds,on}$, the simulated N_f of both two models are close to the experimental result which is 914 cycles, with 930 and 950 cycles for the exponential method and the stress related model respectively. However, in terms of the growing trend, the exponential method gives a better performance. A steep increase occurs at 150th cycle due to the change of load, as the α value for the second load is no longer 0.0015, but will be the accumulated $\Delta R_{ds,on}$ caused by previous load which is around 0.05 in the graph. Since the degradation is irreversible, it is necessary to redefine the initial point. And it also verifies that, the degradation is not only based on the ΔT_j, but also on the device current health state in [69] - [70]. While for the stress related method, since it follows the Miner's rule, the $\Delta R_{ds,on}$ increases very fast when under high stresses. The calculated N_f is 371 cycles at $\Delta T_j = 180°C$, hence, at 150 th cycle, the accumulated Q is around 0.4, and the estimated $\Delta R_{ds,on}$ is 0.02 ohm. The growing trend slows down after the load is changed as the stress is lower. This simulation has also validate the point that, a relatively large mismatches can be obtained when use this model to depict high stress thermal cycling experimental results. To

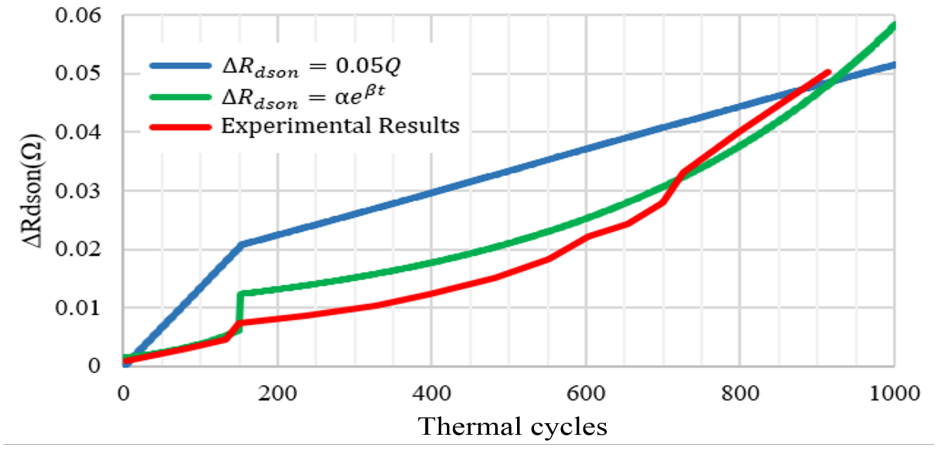


Fig. 3.6 Simulation results of the proposed model with exponential and stress related aging models, and experimental results from [73] of $\Delta R_{ds,on}$ resistance variation when ΔT_j is reduced from 180°C to 140°C at 150 cycles with the same $T_m = 180$°C.

sum up, the exponential model gives a better performance as compared to the stress related model when with high stress thermal cycling mission profiles. However, this advantage will be diminished in long-term lifetime simulation, as the $\Delta R_{ds,on}$ will give more flat aging trend. Both of these two methods can be used in long-term mission profile simulation. In terms of simplicity, the stress related method is adopted and discussed.

3.4.2 Random Mission Profile

Fig. 3.7 gives a complete simulation result of the proposed model with a random mission profile for 120000 seconds (120 Ks) which mimics 10 years load. Fig. 3.8 gives a close view of a 0.4 Ks simulation results from 11.6 Ks to 12 Ks. The load R_L changes every 5 seconds (5 s) which translates to a change in every 4.8 hours in real life. The ambient temperature profile T_a which includes both annually and daily information is adopted to reflect the device operation environment. Both of these two profiles are periodical and annually based. In the simulation, they are represented by voltage sources V(ta) and V(rl) respectively. The estimated T_j expressed by V(tj_mos) is within the range of 40 °C - 185 °C. As can be seen from Fig. 3.7, the Q value V(q) reaches 1.1 after 120 Ks, while at 12 Ks in Fig. 3.8, the

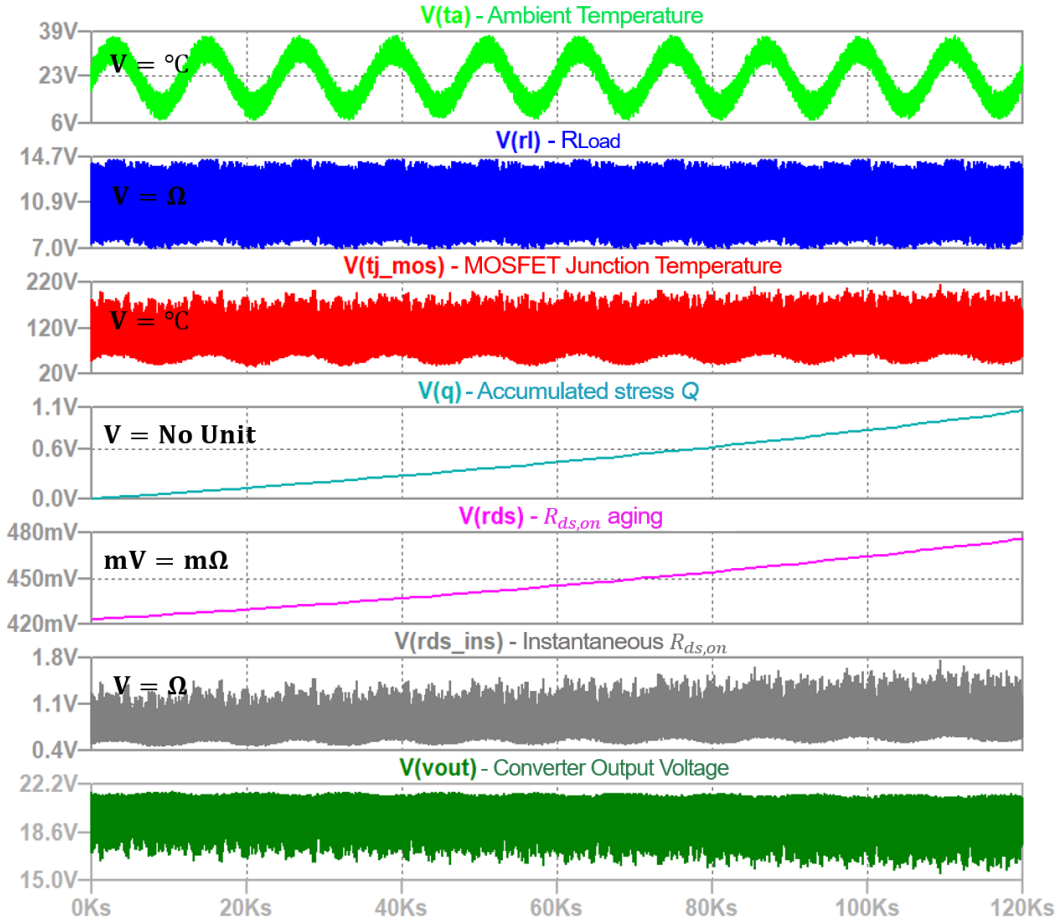


Fig. 3.7 An overview of simulation results of a 120 Ks random mission profile with varied ambient temperature to mimic a 10 years converter operation.

value is about 0.077. The lifetime of the device is around 13 years if no aging effects is considered. However, due to the induced degradation feedback loop which accelerates the aging progress, the lifetime is shorter than 13 years, which occurs at 116 Ks (equivalent to 9.67 years). V(rds), which indicates the $R_{ds,on}$ with aging ($R_{init} + \Delta R_{ds,on}$) grows in a similar trend with V(q). While for V(rds_ins), which reflects the aging and temperature dependent real-time $R_{ds,on}$, its values at later 60 Ks are clearly higher than the previous 60 Ks due to the increase of V(rds). V(out) indicates the converter output voltage, due to the open-loop operation, the value varies in the range of 17-21.6 V range. A low V(out) can be found when T_j is high, as the V(rds_ins) is high, more conduction losses are generated.

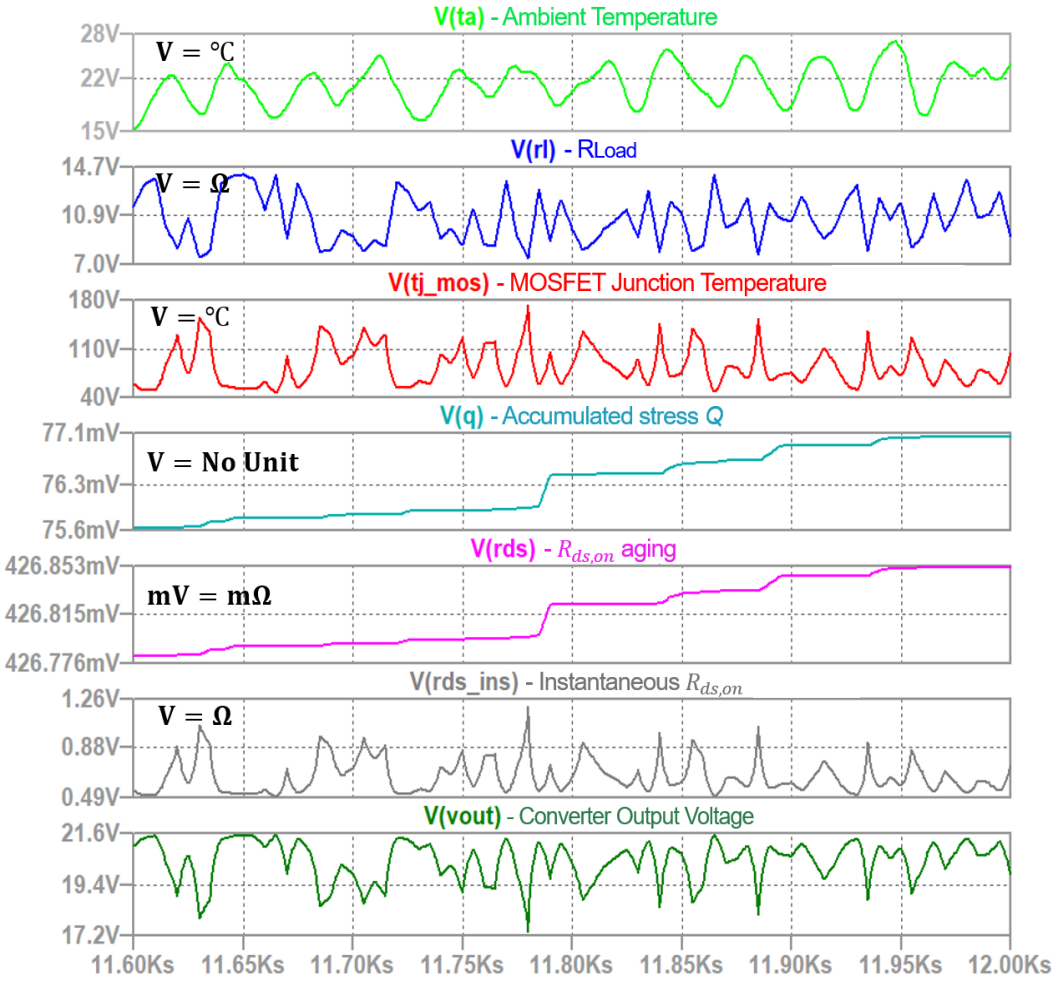


Fig. 3.8 A close look of Fig. 3.7, showing the last 0.4 Ks simulation results from 11.6 Ks to 12 Ks in the first periodical period (12 Ks).

Fig. 3.9 shows the detailed junction temperature data processing steps. Sample and hold function is used to extract the V(tj_mos) at each load, giving the V(sampling) waveform. Based on it, a continuous comparison between the current temperature value and previous one is made to calculate the difference ΔT_j and the mean temperature T_m and it is fed back to (1.4). As can be seen from the graph, the accumulation of V(q) remains flat when ΔT_j is low even T_m is high. Meanwhile a steep increase can be observed when ΔT_j is high. Due to the transformation between different domains and adoption of behavioral models, the real unit of each measured waveform has been clarified in Figs. 3.7-3.9.

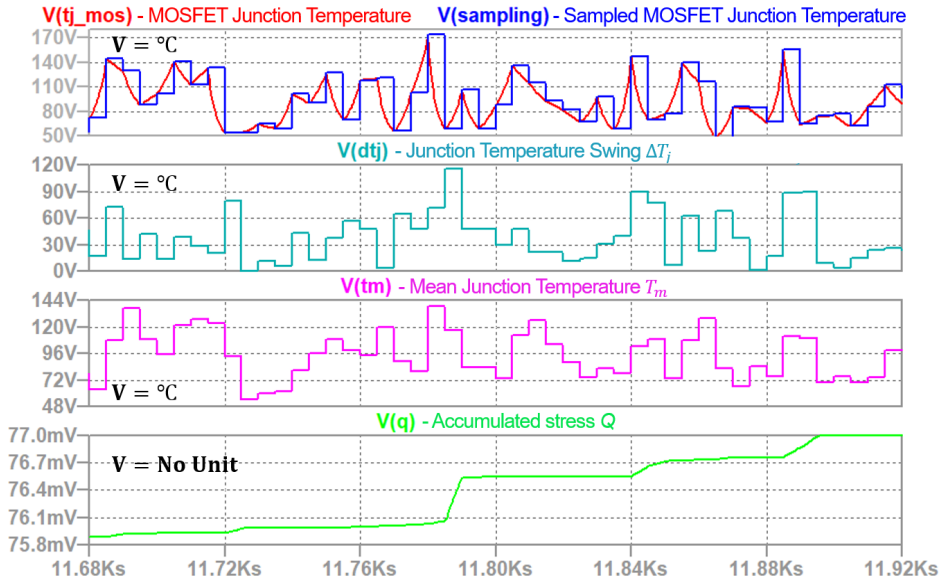


Fig. 3.9 T_j data processing stage, including sampling and extraction, T_m and ΔT_j calculation, and Q stress accumulation.

3.4.3 Simulation Speed

In this section, the running time of a thermal cycling profile and a long-term profile of the proposed model is compared with a modified MOSFET SPICE model. The simulation is completed in a laptop computer, with Inter(R) Core(TM) i7-7600U CPU. The modified MOSFET SPICE model has the same functionality as the proposed model, and the derivation follows similar procedures introduced in this chapter. Some minor modifications are made: 1. In the electrical model, an extra resistor is added and connected in series with a normal MOSFET SPICE model representing the increments of $R_{ds,on}$ caused by the temperature and aging; 2. In the thermal model, a foster RC network is used which enables users to see the instantaneous temperature changes. The construction of the electro-thermal model of the modified MOSFET SPICE model can be found in the previous work in [53]. Detailed evaluation and comparison of these two models are given in Table II.

As can be seen, in the 8 Ks high stress thermal cycling simulation, the proposed method does not show significant improvement of simulation speed over the switching model, due

Table 3.3 A comparison of elapsed time of running the thermal cycling simulation and long-term simulation between a switching model and the proposed model.

Simulation Tasks	**Thermal Cycling Profile (8 Ks)**	**Long-term Mission Profile (5 s)**		
Frequency (Hz)	0.1	10 k	20 k	50 k
Elapsed time of the switching-model	14.78	819.5	1312.7	3956
Elapsed time of the switching-model	12.266	0.145	0.119	0.148

to low operation frequency of this mission. However, in the long-term mission profile simulation, with the increase of the switching frequency, the simulation time of the switching model rises dramatically, with 819.5 s, 1312.7 s and 3955.7 s for 10 kHz, 20 kHz and 50 kHz respectively. Meanwhile, the proposed model achieves a relatively constant simulation speed for all three cases and is at least 5600 times faster than switched model. The gap further increases when the switching frequency increases.

3.5 Discussion

As the proposed model takes advantage of the ETAM which is independent of frequency, and the switching losses related terms are add-ons and are represented by equations, this model is well suited for assessing a device which deals with high switching frequency operation, long-term and complex mission profiles. In addition, the precision of the model can be improved by using more accurate equations of such as, switching losses, N_f, and etc. One may argue that this model has not taken parasitic parameters or manufacture settings of the device into consideration. Noted that, the dominant affected parameter in this device is $R_{ds,on}$ from both of the thermal and aging point of view. In addition, the manufacture settings are not easy to be reflected in modelling level, and this scenario happens on the normal MOSFET SPICE model as well. Since devices may differ from one to another, while modelling gives

a general information of a device, the common solution to solve it is to use Monte Carlo simulations to estimate the failure probability of converters/inverters. Alternatively, for an operating system, online monitoring or prognosis of $R_{ds,on}$ can be implemented to evaluate the device lifetime.

The proposed model allows an instantaneous calculation of the accumulated stress and aging at each half thermal cycle, thanks to the ease of construction of the half-cycle thermal counting algorithm in the circuit simulator. Although it is a widely accepted method, one drawback is that, the accuracy of this algorithm is not as good as rainflow counting method, especially when the device has large temperature fluctuations [40]. Hence, one potential future work is to develop a more accurate thermal counting method in the circuit simulator. Another limitation of this work is that, this model has not considered other failure modes like short circuit, etc. at this stage, which could be considered for future work.

3.6 Summary

In this chapter, a MOSFET model which merges electro-thermal averaged modelling, aging and lifetime evaluation is proposed in LTspice®, which is a powerful yet freeware circuit simulation tool. Derivation principle of the proposed model are discussed, and two aging descriptive models embedded in it are also investigated and compared. Key features of this work are that, it takes the device aging phenomenon into consideration when estimates its lifetime; secondly, online monitoring of electrical and thermal performances, stress accumulation, degradation and lifetime consumption can be realized simultaneously, which are achieved by using thermal-electrical analogy and behavioral models. High stress thermal cycling simulation is implemented for verification purpose. The results show an agreement with [73]. In long-term load simulation, an accelerated degradation progress can be observed due to the accumulated stress on device. The estimated lifetime with and without inducing aging effects are equivalent to 9.67 and 13 years respectively. Thus, it is important to consider

aging when evaluating device lifetime. Another benefit of the model is the fast simulation speed due to ETAM, allowing a 120 Ks simulation to be completed in around 46 s. Hence, the model has high potential for long-term lifetime evaluation of circuit device.

Chapter 4

Circuit-Based Rainflow Counting Algorithm in Application of Power Device Lifetime Estimation

4.1 Introduction

Software-assisted reliability assessment of power electronic converters is increasingly important due to its multi-domain nature and extensive parametric calculations. The rainflow counting algorithm is gaining popularity for its low relative error in device lifetime estimation. Nevertheless, the offline operation of the algorithm prevents most simulation software packages from considering other parameters for the device under study, such as aging and the current state of health in the estimation, as it requires a complete loading profile to run recursive comparison. This also brings difficulties in realization in circuit simulators such as SPICE. To tackle the issue, an in-the-loop circuit-based rainflow counting algorithm is proposed in this work and applied to estimate the consumed lifetime of the MOSFET in a boost converter for illustration. Instantaneous electrical and thermal performances, and accumulated stress of the device can be monitored. Not only does this assist in evaluating

the state of health of a device, but allows the possibility of integrating the aging into the lifetime evaluation. The method follows the four-point rainflow counting algorithm, which continuously compares three adjacent temperature fluctuations ΔT_j to select full cycles for two rounds, and the remaining cycles are counted as half cycles. To validate the performance, a comparative analysis in terms of counting accuracy and simulation speed among the proposed method, MATLAB and also with a well accepted half-cycle counting method is carried out. Reported results show that the proposed method has an improved counting accuracy compared to the half-cycle counting from 24% to 3.5% on average under different load stresses and length conditions. The accuracy can be effectively improved by a further 1.3-2% by adding an extra comparison round.

This chapter addresses the third objective of the thesis, and part of the contribution is published in [78].

4.2 Related Works and Research Gap

Stress cycle counting algorithms translate complicated and irregular loading profiles into a set of organized cycles to facilitate stress accumulative calculations, and are essential in reliability assessments and lifetime predictions for power devices, like power semiconductors or converters/inverters, especially when they operate with critical and varying loads.

Various counting approaches such as level-crossing, peak counting, rainflow and and so on are introduced in [25], [39]-[43], [79]. Comparative discussions on peak counting algorithms (e.g. half-cycle, maximum edge, rising edge, etc.) and rainflow counting are given in [40] through thermo-mechanical FEM analysis, and rainflow counting is reported to have the lowest relative error as summarized in Table 4.1. Rainflow counting was first introduced by Matsuishi and Endo in fatigue analysis in 1968 [41], by assuming the reversals as rain drops and drips off the pagoda roofs as explained in Section 1.3.5. It has also gained popularity in dealing with critical thermal profiles and calculating lifetimes. For example, the

lifetime of grid-connected PV inverters in [34] and [65], and multi-level converters utilized in wind turbine systems [3], [15] are evaluated with the help of this counting algorithm. In most of the studies, the counting is completed by inputting the thermal profile into the MATLAB rainflow counting command for ease of implementation and fast computation speed. To the best of our knowledge, there are very few existing solutions which realize rainflow counting in a circuit simulation platform. Possible reasons may be that the traditional rainflow method is applied offline, while the circuit simulator follows the time sequence, which brings difficulties in comparing different reversals, especially when they are far away from each other.

Table 4.1 Simulation results for certain mission profile - averaged relative error, reported in [40].

Place	Rising edge	half cycle	Max. Edge	Rainflow
Example case	19%	21%	27%	11%
Special case	32%	36%	20%	12%

There is a growing trend at preset for implementing multi-domain or multi-discipline simulations, for instance an increasing number of integrated ETMs of power MOSFETs, IGBTs, etc., are provided by leading manufacturers such as Infineon, and STMicroelectronics. It could be beneficial to include lifetime estimation into the simulation, such that users are allowed to monitor the device's electrical performance, thermal properties, accumulated damage, and lifetime simultaneously and only in one simulator. Apart from this, studies demonstrate the great impacts of aging and current health state of a device on lifetime estimation [66], [62], [69]-[70] and [80]. To take them into consideration, it is necessary to know the instantaneous accumulated stress. In other words, an online counting method is required. Although the MATLAB rainflow counting function provides a convenient implementation, it is an offline method, which means a complete loading profile is required. To tackle this, online rainflow counting methods are proposed in [81] and [82]. All are stack-based recursive algorithms, which allow users to easily select and discard counted

cycles in programming. These methods are well-suited to a real-time environment but have difficulty in applying in circuit simulator. As circuit simulators follow time sequence, and it is not possible to make any change on those already plotted points.

Therefore, this work proposes an easy-to-use and in-the-loop rainflow counting approach for power devices and power electronic circuits. This is to fill the gap of missing functionality and integrated approach in existing circuit simulators, and also to facilitate multi-discipline simulation in SPICE, which includes electrical, thermal, and lifetime consumption. Besides, since the rainflow counting has the smallest relative error, the estimated lifetime evaluation is more reliable with this method. Realization of this algorithm is assisted by sample-and-hold function blocks, buffers, logic gates, behavioural set-reset flipflop and behavioural models. Since it is not possible for the circuit simulator to run the recursive method like the stack-based implementation, simplification is made by only sorting full cycles for limited times. Although it cannot pick out all full cycles, it still has an improved counting accuracy as compared to other simple approaches, like the half-cycle counting method from the simulation result. Additional comparison rounds can be added to improve the counting accuracy further.

4.3 Principle of Rainflow Counting Algorithm

Different methodologies are proposed to achieve rainflow counting in [39] and [42]. The principle of the three reversal approach has been explained in Section 1.3.5. As discussed, the three reversal approach is well-suited to programming software, but it is hard to realize in a circuit simulator due to the difficulty of comparing and discarding reversals. For the sake of simplicity without losing effectiveness, its alternative, four-point algorithm is adopted and explained here.

4.3.1 Four-point algorithm

An equivalent four-point algorithm which compares three adjacent range amplitude can be adopted. Similarly, the load profile is turned into a sequence of reversals as depicted in Section 1.3.5. Then, three adjacent ranges are continuously compared to determine the counting action following the criteria that $X_2 \leq X_3$ and $X_2 \leq X_1$. If satisfied, a closed loop is formed, and the range X_2 is counted as a full cycle. Lastly, reversals involved in the counted range will be discarded, and a new range between uncounted reversals will be similarly formed, and the comparisons keeps on. For instance, $r(EF)$ in the loop of D-E-F-G in Fig. 1.12 is counted, as it satisfies the criteria $r(DE) \leq r(EF)$ and $r(FG) \leq r(EF)$. Both E and F will be discarded, the new range becomes $r(DG)$, and the new four-point becomes B-C-D-G. By doing so, it is possible to pick out all of the full cycles in the load profile, and only a few uncounted half cycles remain. Compared to the three reversal algorithm, it is easier to implement in a simulation as it does not require a pointer. Hence, the principle of the four-point rainflow counting algorithm is employed.

4.4 Implementation Method in SPICE

Following the four-point rainflow counting principle, and applying it in counting thermal cycles as shown in Fig. 4.1, the range X_1, X_2 and X_3 in the criteria represent the temperature

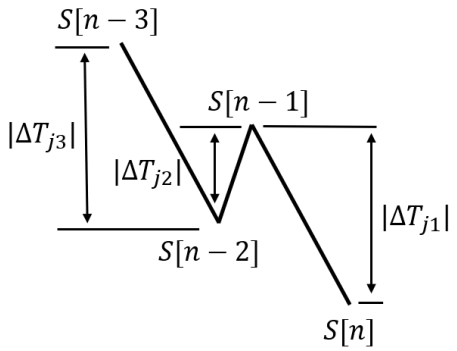


Fig. 4.1 An illustration of a thermal profile counted by four-point algorithm.

swings $|\Delta T_{j1}|$, $|\Delta T_{j2}|$ and $|\Delta T_{j3}|$, respectively. Although the principle is straightforward, when adopted in SPICE it still needs to address the recursive comparison issue. Here, the proposed method runs two comparison rounds to sort full cycles, and count all of the remaining cycles as half cycles. The detailed operation algorithm is shown in Fig. 4.2 and the derivation steps and explanation of implementing the method in SPICE are described below.

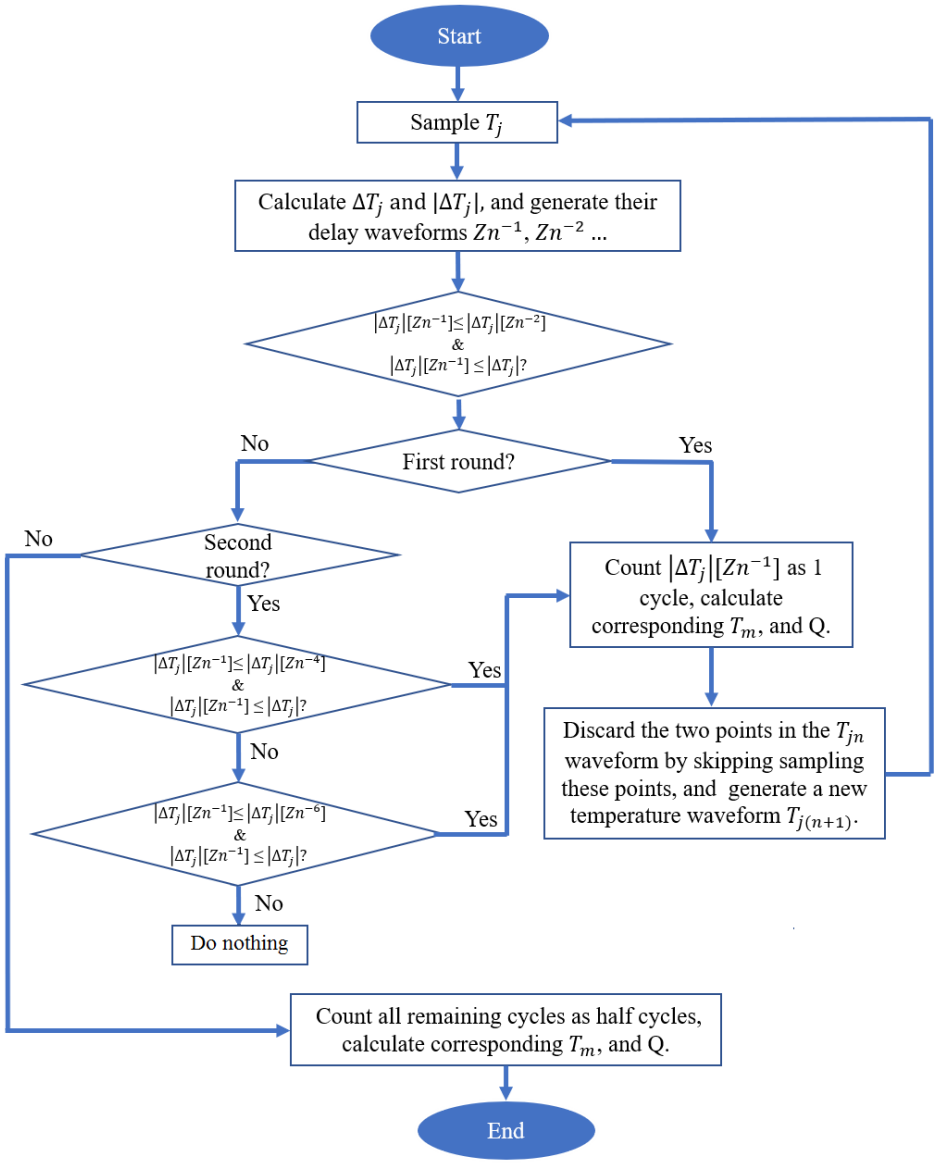


Fig. 4.2 Operation of the proposed rainflow counting algorithm in LTspice®.

1. 1st round starts here: Sample the data points T_j in the thermal profile, and get one sampling period T_s delay $T_j[Zn^{-1}]$ by using the delay function. Subtract these two values to generate the temperature swing waveform ΔT_j and calculate the swing amplitude $|\Delta T_j|$, in other words, the absolute value of ΔT_j. Generate required T_s delay waveforms for both of these values.

2. Compare the 1st T_s delay swing amplitude $|\Delta T_j[Zn^{-1}]|$ with the current value $|\Delta T_j[Zn]|$ and the 2nd T_s delay $|\Delta T_j[Zn^{-2}]|$. Convert the comparison into a Boolean expression, and if it satisfies the criteria that $X_2 \leq X_3$ and $X_2 \leq X_1$, then, the counting waveform $1st$ generates a pulse valued at 1 V, indicating that it counts the $|\Delta T_j[Zn^{-1}]|$ as 1 cycle. Calculate the corresponding T_m and Q of the counted cycles.

3. Generate a new sampling pulse which is made by inverting the $1st + 1st[Zn^{-1}]$, to sample T_j and construct a new waveform $T_{j(n+1)}$ waveform. This can effectively skip sampling the two points involved in the counted $|\Delta T_j[Zn^{-1}]|$, for example $S[n-2]$ and $S[n-1]$, while keeping and holding the uncounted values $S[n-3]$ and $S[n]$ in Fig. 4.1. Since the circuit simulator follows the time sequence, it is not possible to discard the already generated points like the stack-based implementation. In addition, waiting until the previous round to finish counting is also unwise. As the action is proceeding simultaneously with the load changing, the overall number of points that should be discarded, or in other words the delay time, is unknown until the simulation is completed. Hence, the proposed method is used to mimic the discard function.

4. 2nd round starts here: Same as step 1 with the newly generated $T_{j(n+1)}$.

5. At this time, $|\Delta T_{j(n+1)}[Zn]|$ is no longer consecutive, however, zeros appear due to the discarded points in the previous round. This results in difficulties by simply adopting the same method in step 2. Thus another solution is given here. Determine the growing trend of the temperature swing by comparing $|\Delta T_{j(n+1)}[Zn]|$ with

$|\Delta T_{j(n+1)}[Zn^{-1}]|$. A falling trend is indicated if the current $|\Delta T_{j(n+1)}[Zn]|$ is smaller or equal than $|\Delta T_{j(n+1)}[Zn^{-1}]|$. Else, it is in a rising trend. Based on the criteria that $X_2 \leq X_3$ and $X_2 \leq X_1$, X_2 must have the smallest range. Thus, there will always exist full cycles at the end of falling segments, and just next to the following rising segment. As the 1st round discards even numbers of points, for instance, two points for 1 counted cycle, four points for two consecutive counted cycles, etc., the full cycles are most likely to occur in odd delay T_s, e.g. $[Zn^{-1/-3/-5}]$. Therefore the solution is to pick out full cycles by shifting the $|\Delta T_{j(n+1)}|$ five times, from $[Zn^{-1}]$ to $[Zn^{-5}]$, to find out the first cycle that overlaps with the rising segment. Within 5 T_s periods, it is capable of filtering out most of the full cycles in this round.

6. Unify the counted cycles to the same delay T_s $[Zn^{-5}]$ and sum them up. Same as step 3 and generate with a new sampling pulse made by inverting the aforementioned pulses, and output a new $T_{j(n+2)}$ waveform.

7. 3rd round starts here: Same as step 1 with the newly generated $T_{j(n+2)}$.

8. Same as step 2, and loop stops here. The remaining $\Delta T_{j(n+2)}$ values are counted as half cycles. Calculate the corresponding T_m and Q of half cycles.

In summary, the proposed implementation of rainflow counting continuously compare the values of three adjacent temperature swings $|\Delta T_{jn(n=1,2,3)}|$ for the first two rounds. Counting pulses will be generated during the comparison, and its inverted waveform will be used as the sampling pulse for producing the next round $T_{j(n+1)(n=1,2)}$. By doing so, the counted points can skip sampling, and the next round $T_{j(n+1)(n=1,2)}$ waveforms are simplified. The remaining cycles in the 3rd round are all counted as half cycles.

Note that two rounds cannot filter out all full cycles. In fact, in theory, it requires numerous rounds to achieve. However, the difficulty, complexity and simulation time of running this are expected to increase rapidly. Hence, the proposed method inevitably will

have small errors. Nevertheless, it is possible to modularize the 2nd round operation and add it as additional rounds to improve the counting accuracy. As a trade-off, the simulation time will be increased. For illustration purposes, the three key steps of the proposed rainflow counting are explained. The detailed implementation of this algorithm in a circuit simulator will be introduced in the following section.

4.5 Circuitry Analysis

The implementation of the algorithm is carried out in LTspice®. In order to verify the effectiveness of the proposed model, it is applied to estimate the lifetime of the MOSFET in an operating boost converter. The complete circuity of the proposed counting method and the boost converter ETAM are shown in Fig. 4.3.

4.5.1 Electro-thermal averaged model

To count the thermal cycles, it is necessary to first have the thermal profile. An averaged boost converter is constructed first for its advantage of fast operation speed over the switching converter as can be found similarly in Fig. 3.2. Modification is made to replace the fixed MOSFET on-state resistance $R_{ds,on}$ in the conventional averaged model with a temperature dependent variable resistance using (3.1). In addition, since the averaged model is frequency independent, while the switching losses contribute significantly to the total power losses at high frequency, an extra voltage source V_{sw} which represents the voltage drop caused by the switching is added. A general estimation of switching losses is obtained by using (2.12). Thus, a simple method to represent V_{sw} is by using (2.13) as a result of (2.12). Regarding the conduction losses, it can be easily calculated using (2.14).

In the thermal model, a resistance network which comprised of two thermal resistances, namely junction to case R_{jc} and case to ambient R_{ca} thermal resistances, and a voltage source

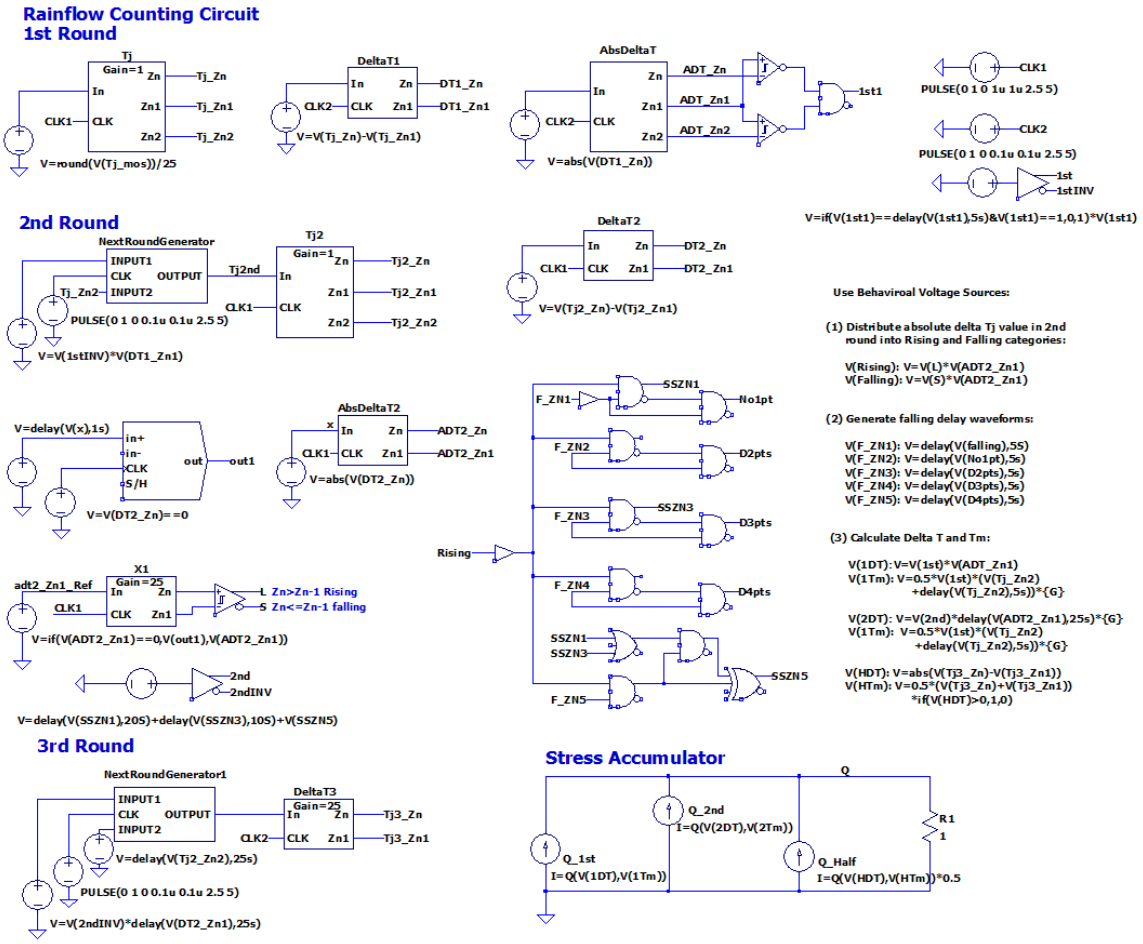


Fig. 4.3 Schematic of the implementation of the proposed rainflow counting algorithm in counting the thermal cycles of a MOSFET in a running averaged boost converter.

represented by ambient temperature T_a is constructed. Inputs of this model are conduction and switching losses described by behavioural current sources.

These two models are linked by feeding back the estimated MOSFET junction temperature T_j from thermal model to electrical model, while the calculated losses P_{loss} from electrical to the thermal model. The detailed derivation steps can be found in previous work in [54] and [62].

4.5.2 Rainflow counting circuits

Before explaining the counting circuities, sub-function blocks frequently employed in the circuitry, and purposes of using them are introduced first.

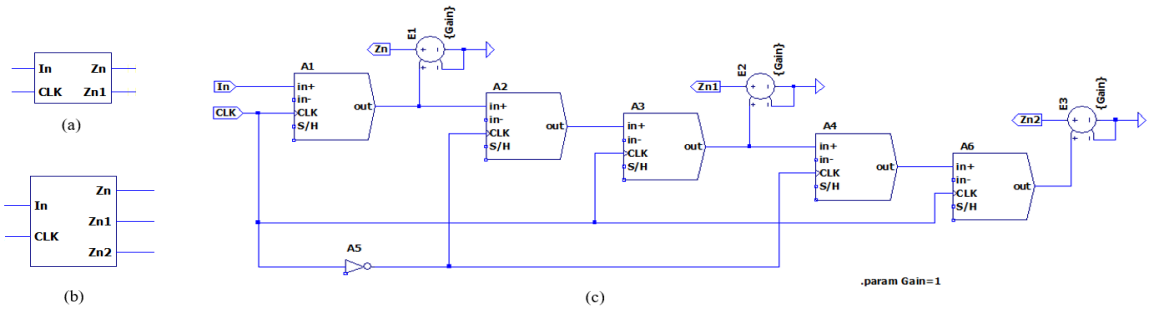


Fig. 4.4 Sample-and-hold with delay function block. (a) Symbol of the block with 1 T_s delay. (b) Symbol of the block with two T_s delay. (c) Schematic of (b).

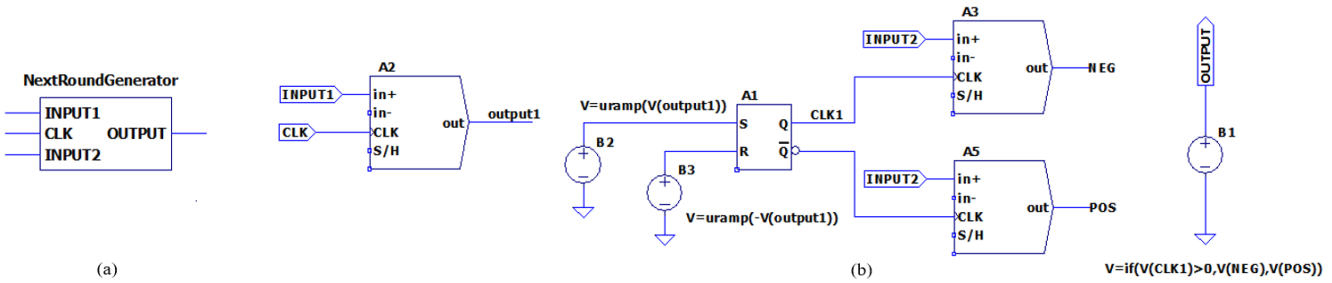
- Sample-and-hold with delay function block as shown in Fig. 4.4. This submodule comprises of several sample-and-hold function and logic gates, aiming at sampling the data, and generating the 1st and 2nd T_s delay. The input $in+$ and CLK are the data that needs to be sampled and the sampling frequency respectively. Due to the maximum allowed sample voltage being 10 V, the thermal profile needs to be scaled down before input to this function. It can be converted back to its original value by using a voltage dependent voltage source E to provide a gain. The pre-defined value is 1.

- Behavioural Schmitt-triggered buffer with differential inputs is utilized in comparing the input amplitudes, and output a Boolean result.

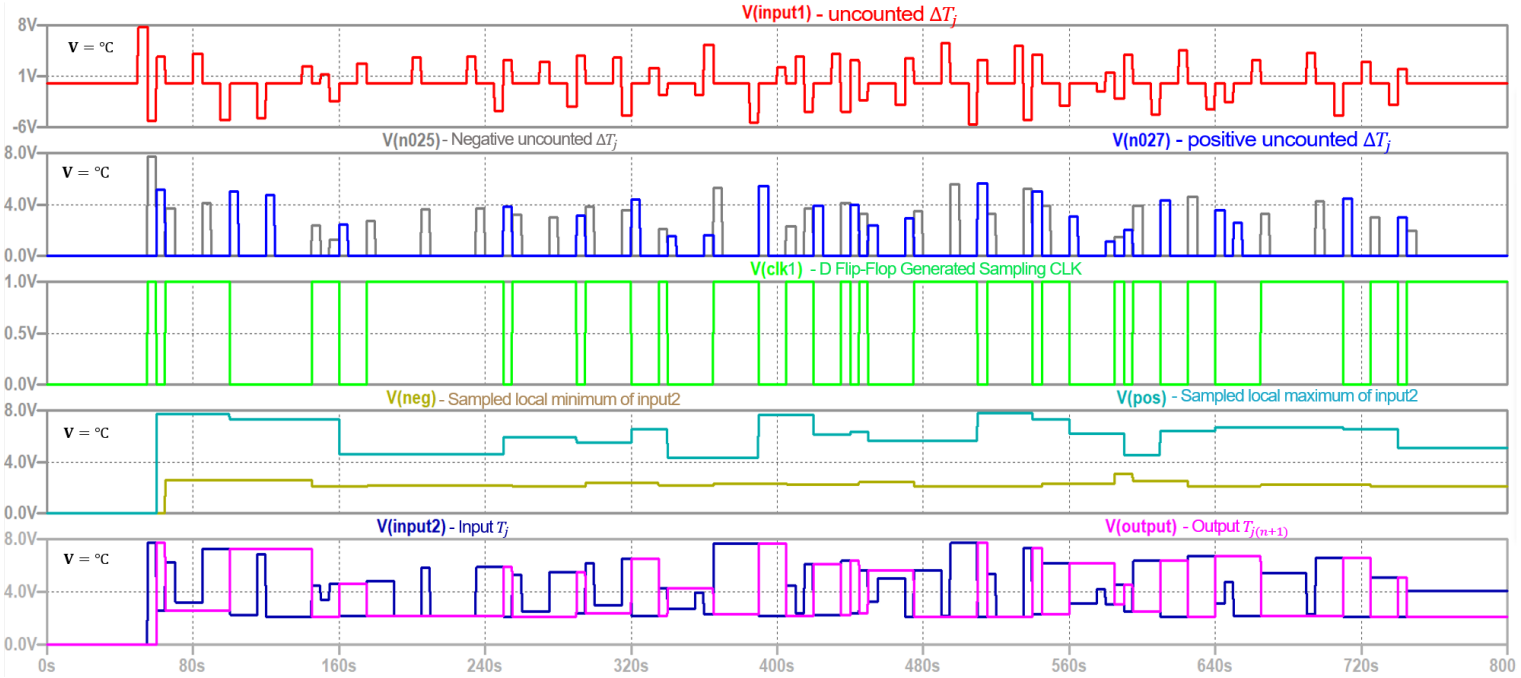
- Logic gates including AND, NOT and OR gates are used in making decisions if a cycle should be counted or not.

- Behavioural models, which include behavioural current or voltage sources, allow user to define the required functions. A few functions employed in this algorithm and also in the electrical circuits are explained in Table 4.2, and futher description can be found in [75].

- Next round $T_{j(n+1)}$ waveform generator, as shown in Fig. 4.5a, where, input 1, input 2 and CLK are the uncounted $\Delta T_{j(n)}$, $T_{j(n)}$ and sampling pulse respectively, while the output is the $T_{j(n+1)}$ waveform. After sampling the $\Delta T_{j(n)}$ values, it will be split into two groups which contain pure positive and negative values respectively as shown in Fig. 4.5b. Use the behavioural set-reset flipflop to extend the positive pulse until it meets the negative value, and vice versa. By doing so, the uncounted $T_{j(n)}$ will be kept and extended until meeting the next uncounted value. The achievement of the next round waveform is by adding the positive and negative outputs together through an if function. The key waveform of using this generator for illustration of the implementation is shown in Fig. 4.5b.



(a) Next round $T_{j(n+1)}$ waveform generator, symbol and schematic.



(b) Key simulation waveform of the module.

Fig. 4.5 Demonstration of next round generator.

Table 4.2 Description and explanation of LTspice® functions used in the proposed model.

Function	**Description [75]**	**Purposes of the functions in the model**
if(x,y,z)	If x is true, do y else z	conditional statement
idt(x)	Integrate x	accumulate stresses Q
delay(x,t)	x delayed by t	generate a waveform with t cycles delayed for comparison
abs(x)	Absolute value of x	calculate amplitude ΔT_j
uramp(x)	If $x > 0$, output x, else 0	Split positive and negative ΔT_j

As can be seen from the rainflow counting circuits in Fig. 4.3, the counting steps in 1st round is simple. It only contains sampling T_j, calculating the temperature swing and its amplitude, and generating their delays waveforms by employing sample-and-hold with delay function blocks and behavioural voltage sources. The determination of a full cycle is by using the behavioural Schmitt-triggered buffer with differential inputs. Since it can only output the true value when the positive side is larger than the negative side, an inverting comparison is thus made to achieve the $X_2 \leq X_3$ and $X_2 \leq X_1$ criteria.

The 2nd round is slightly complicated as zeros appear in $|\Delta T_{j2}|$, as explained in Section II. (B) step (5). A reference waveform $|\Delta T'_{j2}[Zn^{-1}]|$ is generated to facilitate the comparison between two non-zero adjacent values, as they may possibly separated and far away from each other in original $|\Delta T_{j2}|$. The reference waveform is achieved firstly by detecting all zeros in $|\Delta T_{j2}|$, and utilize it as the sampling pulse to sample the $|\Delta T_{j2}|$ again. By doing so, a new waveform, which samples the previous value of all zeros in $|\Delta T_{j2}|$ are constructed. This action will result 1 T_s delay from the $|\Delta T_{j2}|$. Hence, to sum the $|\Delta T_{j2}[Zn^{-1}]|$ and the aforementioned pulses together, the reference waveform $|\Delta T'_{j2}[Zn^{-1}]|$ is formed. For instance, the original $|\Delta T_{j2}[Zn^{-1}]|$ is $[X_3\ X_2\ 0\ 0\ X_1]$ while in the reference $|\Delta T'_{j2}[Zn^{-1}]|$, it becomes, $[X_3\ X_2\ X_2\ X_2\ X_1]$. With the help of the reference waveform, the falling and rising cycles

can be distinguished. Note that it is possible that a consecutive cycles $|\Delta T_{j(n+1)}[Zn^{-1/5}]|$ or $|\Delta T_{j(n+1)}[Zn^{-3/5}]|$ that should be counted, however, it requires extra efforts. Compared to the improved counting accuracy with respect to the required efforts, here does not consider this consecutive situation.

Shifting the falling cycles V(falling) by one T_s produces the V(F_ZN1), and use it to meet the rising cycles for five times. After each time, cycles that overlap with rising segment will be deleted, and a new truncated falling cycles waveform will be generated and employed in the next shifting step. Comparisons are mainly made in 1st, 3rd, 5th T_s, to search full cycles that when X_2 is 1, 3, 5 T_s away from X_1, indicating cases that, no cycles, one cycle, and two consecutive cycles are counted between X_2 and X_1 in previous round, respectively. Since one counted cycles contains two reversals, discard them will result 2 zeros in $|\Delta T_{j2}|$. Cycles in even numbers of shifting times, 2 or 4 T_s will be deleted straightly. As they will either be zeros or cycles X_3 before the full cycles X_2.

The third round is the simplest and counts all the remaining temperature swings cycles as half cycle. Therefore, only a next round generator and a sample-and-hold with delay function block to produce the T_{j3} and its one T_s delay $T_{j3}[Zn^{-1}]$ waveform are required, as they provide enough information to calculate the $|\Delta T_j|$ and T_m.

The corresponding $|\Delta T_j|$ and T_m of all cases above are calculated using (4.1) and (4.2), respectively. C and G indicate the counted cycles of each round, and the gain value, as the temperature is scaled down before inputting into the sample and hold function. For n and x, they are the corresponding round, and delay times.

$$\Delta T_j = C \cdot |\Delta T_{j(n)}| \cdot G \tag{4.1}$$

$$T_m = \frac{1}{2} \cdot C \cdot (T_{j(n)}[Zn^{-x}] + T_{j(n)}[Zn^{-x-1}]) \cdot G \tag{4.2}$$

The stress accumulator is utilized done to evaluate the accumulated damage of a device after a number of thermal cycles, in other words, the consumed lifetime. It is made by parallel connecting behavioural current sources which represent stresses from each round, and injecting into a 1 ohm resistor to sum the stresses. To calculate the accumulated stress of a device, a modified Coffin-Manson model (1.4) and Miner's rule (1.6) are employed, which are explained in Sections 1.3.2 and 1.3.3. The MOSFET model under consideration is the IRFP340, and coefficients δ and A_1 are -5.2776 and 4.9283×10^{13}, respectively, as given in [73] and are adopted in (1.4).

4.6 Simulation Results

4.6.1 Simulation waveform

The simulation results of applying the proposed method to a DC/DC boost converter with a 700 second random load are given in Figs. 4.6-4.8 as an illustrative example. An overview of the electrical performances of the MOSFET and the boost converter is given in Fig. 4.6, together with MOSFET output thermal profiles after each comparison round. The load V(load) changes every 5 s, and only contains reversal points. The V(tj_mos) and V(rds_ins), namely the simulated MOSFET junction temperature T_j, and the instantaneous $R_{ds,on}$, share the same varying trend. As they follow (3.1) that high operation temperature will result in a high on-state resistance, and it in turn will cause heavy power losses. V(tj_zn), V(tj2_zn), and V(tj3_zn) are the sampled waveforms of V(tj_mos), and the generated 2nd and 3rd round T_j after skipping sampling counted points. Due to V(tj_zn) and V(tj2_zn) being used in the next round sample-and-hold function, the gain is 1 for simplicity. The true value needs to be multiplied by a gain of 25. A fairly clear observation on the simplification of the latter round as compared to the previous one can be found.

Key waveforms utilized in 1st and 2nd rounds are shown in Fig. 4.7 to better explain the counting actions. V(tj_zn), V(adt_zn1) and V(1st) indicate the 1st round sampled T_j, the absolute value of the temperature swing $|\Delta T_{j(n+1)}[Zn^{-1}]|$ and the counting waveform. It is easy for this round to find out the full cycles due to its ease of comparison. The counted cycles can either appear at the middle value X_2 which corresponds to the $|\Delta T_{j(n+1)}[Zn^{-1}]|$. Alternatively, it can appear at the third point X_3, which is $|\Delta T_{j(n+1)}[Zn]|$. To facilitate the later stress calculation, the second point corresponding waveform is always selected.

While in the 2nd round, V(adt2_zn1) and V(adt2_zn1_ref) are the $|\Delta T_{j2}[Zn^{-1}]|$, and its corresponding reference waveform is $|\Delta T_{j2'}[Zn^{-1}]|$. With the help of the reference waveform, $|\Delta T_{j2}[Zn^{-1}]|$ can be divided into two groups, namely V(falling) and V(rising) with cycles only in a declining/increasing trend in it. The V(2nd) displays all of the counted cycles in 2nd round, with 5 T_s delay time away from the $|\Delta T_{j2}[Zn^{-1}]|$.

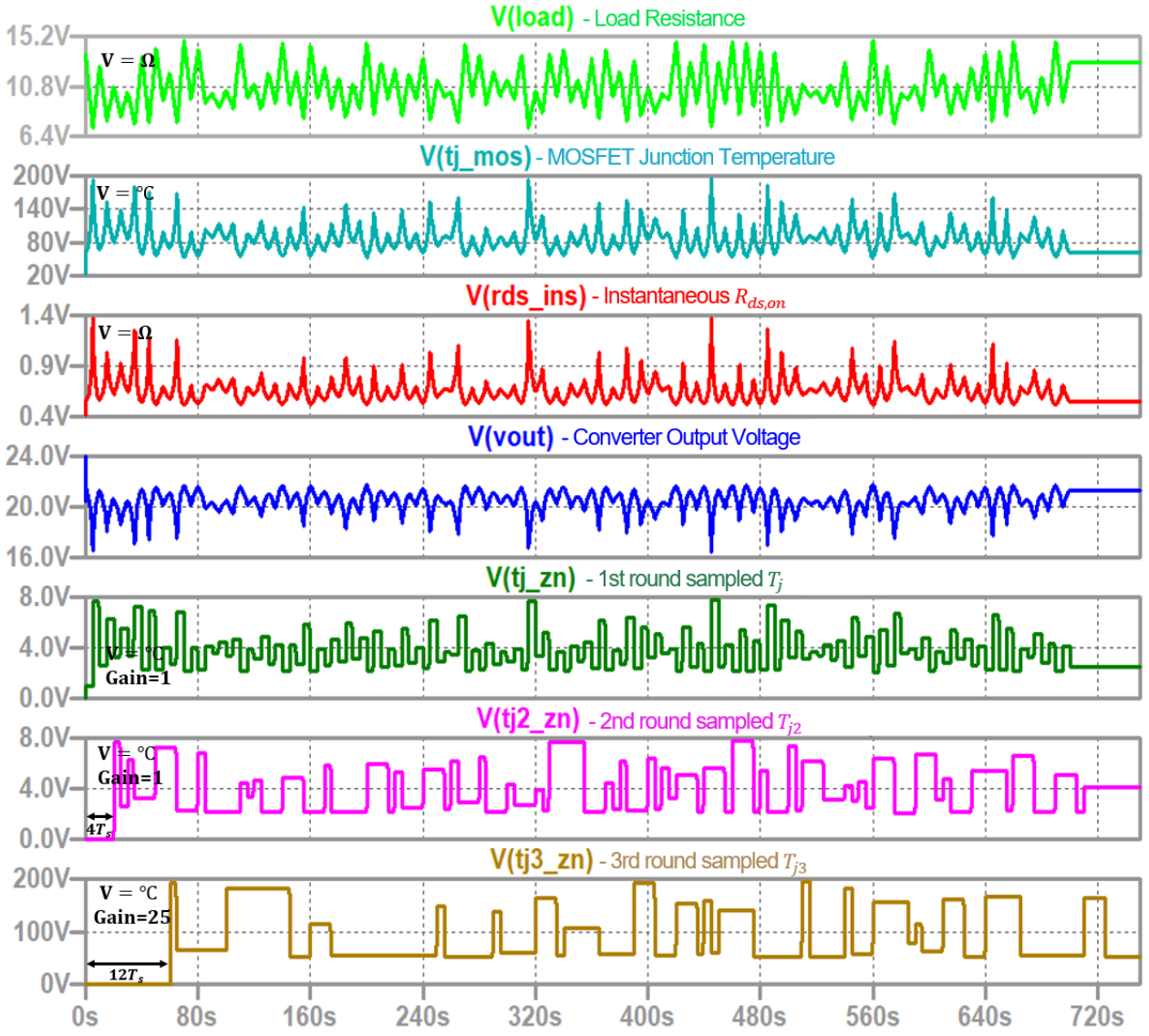


Fig. 4.6 Waveforms of the proposed method of running a 700 second randomly generated load as an illustrative example.

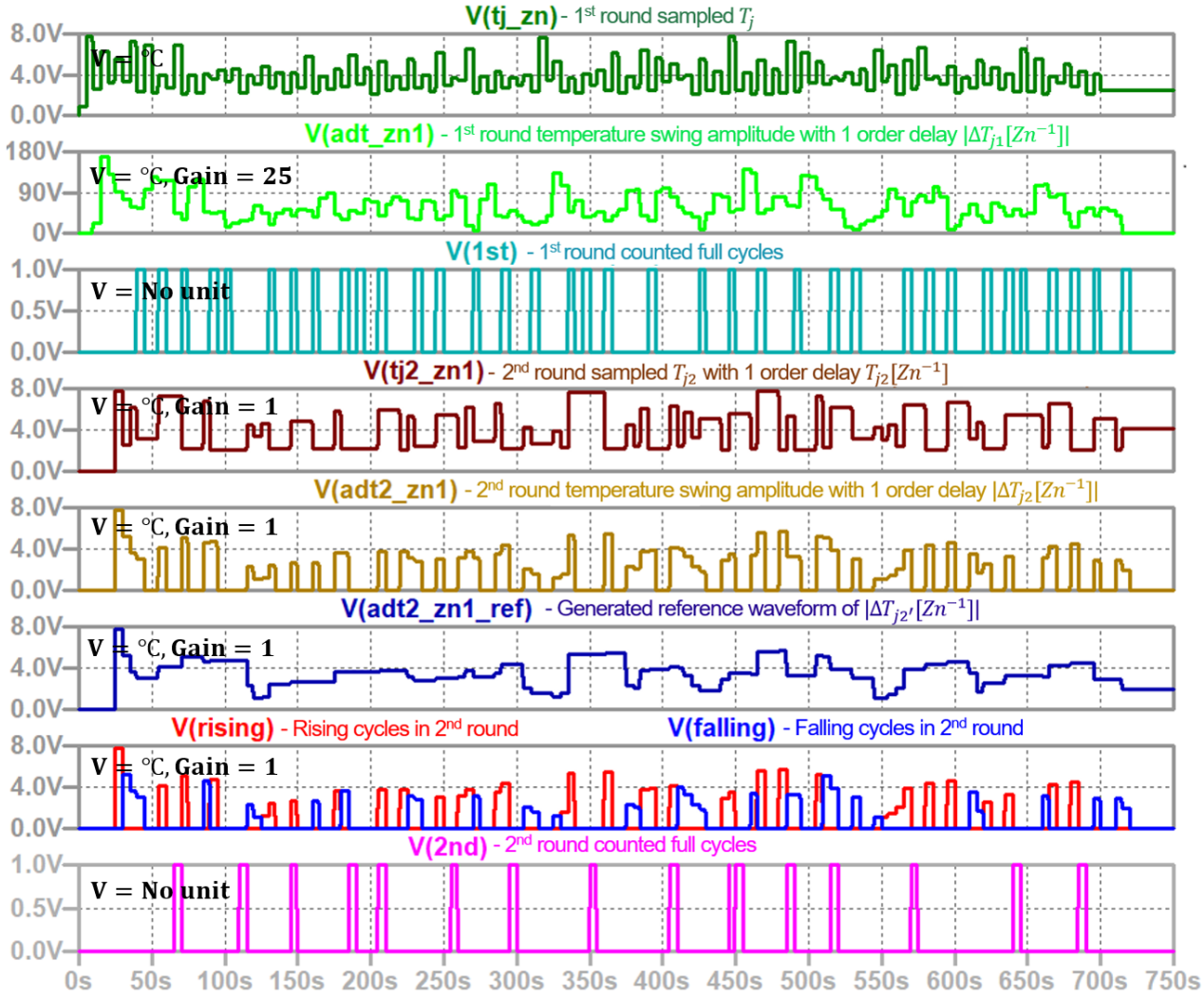


Fig. 4.7 Example waveforms depicting the counting actions of the 1st and 2nd rounds for explanation.

Stress accumulation performance is shown in Fig. 4.8. Since the proposed rainflow counting is an online method, a continuous accumulation of the stresses from the 1st, 2nd, and 3rd rounds with the simulation can be seen. Both steep and flat increases occur in all of the stresses. In addition, the stresses from half cycles take the highest portion in the overall accumulated one. The reason can be found from (1.4), where ΔT_j is the dominant term. Hence, the steepness is highly dependent on the temperature swing ΔT_j. As the first and second round filtered out small full cycles, while the large ΔT_j cycles are left, hence, the half cycles contribute the most.

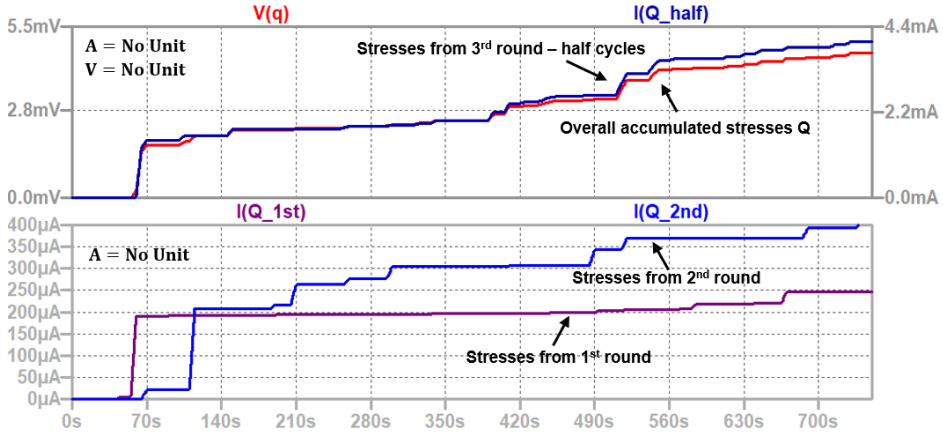


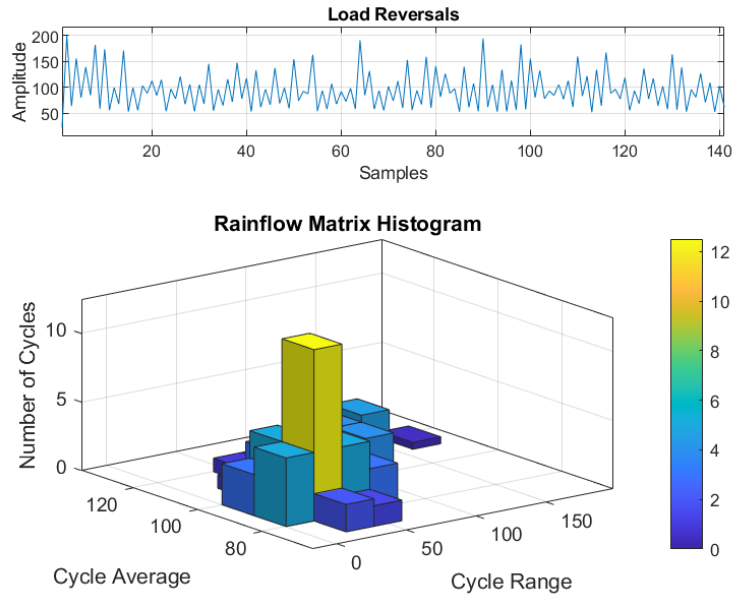
Fig. 4.8 Accumulated stress by the 1st, 2nd, and 3rd rounds.

4.7 Evaluation of the proposed method

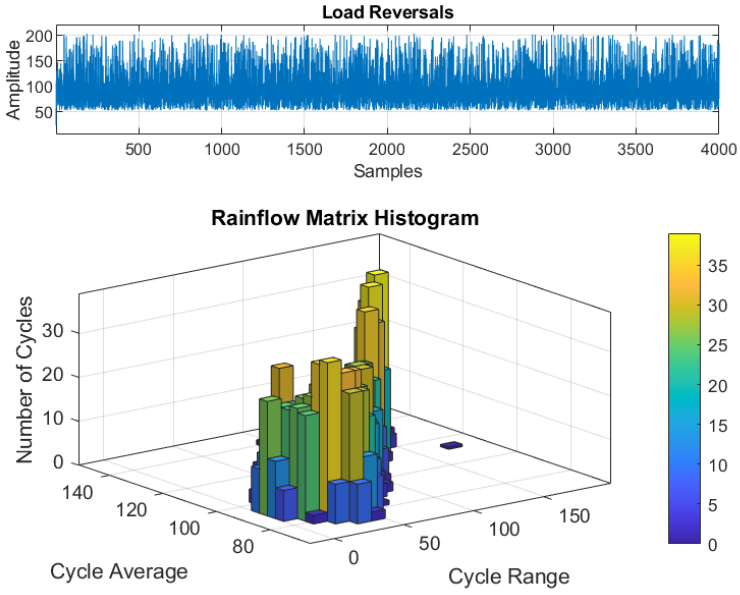
To evaluate the proposed method in terms of counting accuracy and simulation speed, several groups of long-term loads with different stresses and lengths are simulated. All of the loads change every 5 s, and only contain reversal points. The simulated accumulated stresses are compared with both MATLAB and half-cycle peak-through counting method simulation results for their wide acceptance in lifetime evaluation. Also, the operation principle of 3rd round in the proposed method is the same as the half-cycle counting approach. The detailed results are shown in Table 4.3, in which, the accumulated stress Q has a factor of 10^{-3}, while

the proposed (3) and (4) indicate the simulation results of the proposed method with 3 and 4 comparison rounds, respectively. An extra 2nd round is added in the proposed (4), to evaluate the improvement on counting accuracy as compare to the three rounds.

MATLAB results are adopted as the reference. MATLAB rainflow counting algorithm employs the three reversal approach as analyzed in Section 1.3.5. The simulation results of the 700 s demonstration load and 20 Ks High stress long-term load are shown in Figs. 4.9a and 4.9b, respectively. They are display in three-dimensional histograms for better visualizing and understanding the distribution of thermal cycles. The three dimensions are the necessary terms to calculate the accumulated stress, namely number of cycles, cycle average cycle and cycle range. They are equivalent to the number of cycles that a device has been implemented, average temperature and temperature swing used in the circuit. The accumulated stress can be calculated by extracting the data above.



(a)



(b)

Fig. 4.9 MATLAB rainflow counting histogram for illustration. (a) Simulation result of the 700 s demonstration load. (b) Simulation result of the 20 Ks high stress long-term load.

Table 4.3 Comparison of simulation accuracy and speed among half-cycle counting, proposed rainflow counting (three and four rounds), and MATLAB rainflow counting algorithm with different stresses long-term loads.

	High Stress (50-200 °C) 20 Ks Load			**Medium Stress Load (50-160 °C)**						**Small Stress Load (50-110 °C)**					
				20 Ks Load			**50 Ks Load**			**20 Ks Load**			**100 Ks Load**		
	Q	**Error**	**Time**	**Q**	**Error**	**Time**	**Q**	**Error**	**Time**	**Q**	**Error**	**Time**	**Q**	**Error**	**Time**
MATLAB	161	-	-	18.6	-	-	59.5	-	-	1.02	-	-	5.1	-	-
Half-cycle	122.5	23.7%	5 s	15.4	17.2%	5.7 s	49.8	16.3%	13 s	0.792	25.5%	7.2 s	3.49	31.6%	21 s
Proposed (3)	155.3	3.54%	91 s	17.85	4.03%	86 s	57.4	3.5%	198 s	0.99	3%	77 s	4.91	3.7%	376 s
Proposed (4)	158.3	1.7%	141 s	18.1	2.7%	137 s	58.17	2.2%	362 s	1.01	1%	144 s	5.01	1.8%	632 s

*Q has a factor of 10^{-3}. Proposed (3), (4) indicate result of the proposed method with 3 rounds and 4 rounds (run 2nd twice) respectively.

4.7.1 Accuracy

Three conclusions can obtained from Table. 4.3.

Firstly, the proposed method (result of 3 rounds operation for illustration) has higher counting accuracy than the half-cycle counting approach for all of the tested loads. The error in the former is between 3%-4%, while the latter is about 16.3%-31.6%. Since the rainflow counting takes large temperature swing cycles into account, while half-cycle counting does not, it is expected to obtain higher counting accuracy using the rainflow method.

Secondly, the counting method (result of 3 rounds operation for illustration) is effective regardless of the load stress and length. Two groups of simulations are carried out. (1) Three load profiles with the same 20 Ks length but different stress levels, namely high, medium and low stresses loads, with temperature swings of 50-200 °C, 50-160 °C and 50-110 °C tested. The calculated errors of these loads give similar results, between 3%-4%. Thus, the stress level has little impact on the counting accuracy is reported. (2) The impact of load length on counting accuracy is also tested, aiming at checking whether the errors will be accumulated with the increase in load length. Two cases are tested here: (a) Medium stress load profiles with 20 Ks and 50 Ks; and (b) Small stress load profiles with 20 Ks and 100 Ks length are simulated respectively. No significant accumulation of errors can be observed. Hence, the counting accuracy is independent of the load length.

Thirdly, it can also be observed that adding an extra round can effectively improve the accuracy by 1.3%-2%, generally from 3%-4% in three rounds to 1%-3%.

4.7.2 Simulation time

The simulation is carried out in a laptop computer, with Inter(R) Core(TM) i7-7600U CPU. The reported elapsed time of running the half-cycle algorithm with these 20 Ks - 100 Ks loads are between 5 s and 21 s, while for the proposed (3) are 77 s and 367 s. The half cycle counting has advantages in its fast simulation speed, as it does not require any comparison,

hence less circuitries are used. For the proposed method, as the trade-off for improved accuracy, the simulation speed is sacrificed as compared to the half-cycle counting method. Moreover, an increase of more than 50% in simulation time can be achieved by adding an additional round in proposed (4). Nevertheless, given the l00 Ks load profile which with 20,000 points, and finished both electro-thermal modelling and thermal cycle counting within less than 7 minutes is not unacceptable. A high performance computational system can also be used if high speed is required. Since the MATLAB rainflow counting is offline, its operation speed is not considered here.

4.8 Summary

This chapter presents an easy implementation of the rainflow counting algorithm in LTspice®, aiming at achieving an online and high accuracy counting, whilst realizing multi-domain simulation in the circuit simulator. The proposed method follows the principle of the four-point rainflow counting algorithm, which continuously compares adjacent temperature swings in a thermal profile to figure out full cycles for two rounds. Counting pulses will be generated during the comparison, and their inverse will be used as the sampling pulse for producing a simplified thermal profile $T_{j(n+1)}$ for the next round, where counted reversals are discarded. The remaining cycles will be counted as half cycles. Realization of this algorithm is facilitated by sample-and-hold function blocks, buffers, logic gates, behavioural set-reset flipflop and behavioural models. To verify the performance of the proposed method, it is applied to estimate the lifetime of an operating MOSFET in a boost converter. The simulated accumulated stress is compared with the MATLAB simulation results and also with the half-cycle peak-through counting method. Results show that the proposed method has an improved counting accuracy with 3%-4% errors as compared to the half-cycle counting method which is 16.3%-31.6% under different load conditions. It is also reported that, a further refinement of the accuracy of 1.3%-2% can be achieved by adding an extra comparison

round. Simulation speed will be inevitably increased as a trade-off for enhanced counting accuracy. Nevertheless, with 100 Ks load profile finished simulating in less than 7 minutes is still acceptable. High speed computing systems can also be utilized to compensate this effect if simulation speed is a requirement.

Chapter 5

Evaluation of Thermal Performance of Three-Phase Systems with Zero Sequence Injection

5.1 Introduction

ZSI techniques are widely adopted in Y- and Δ-connected CHB three-phase systems to cope with unbalanced power generation from each phase. Recent studies have shown that ZSI can allow a Δ-connected CHB converter to cope with a large range of power imbalances among phases when compared to a standard Y-connected CHB converter. The superiority in electrical performance under unbalanced input power has been well investigated, however the comparative thermal performance of each configuration under the same power imbalance conditions has been neglected. In this chapter, the thermal performance of a CHB converter connected in both the Δ-configuration and Y-configuration operating under an unbalanced power condition is studied. To this end, the ZSI for both Δ- and Y-connected CHB converters is firstly analyzed. Then, the impact of ZSI on the thermal performance and lifetime expectancy of the power switches in each phase is evaluated and compared for both

configurations. The thermal analysis shows that even though a Δ-connected CHB converter offers a wider power imbalance operation than its Y-connected counterpart from the electrical viewpoint, this is achieved by thermally stressing the power switches in each phase in an uneven manner, and in some cases overstressing them. Consequently, there is a trade-off between electrical performance and thermal stress when dealing with power imbalances in Δ-connected and Y-connected CHB converters.

This chapter addresses the fourth objective of the thesis, and part of the contribution is published in [83].

5.2 Related Works and Research Gap

The Cascaded H-bridge (CHB) multilevel converter is one of the most popular topologies for high power applications, mainly due to its capability to generate a high AC-voltage using lower power rated switches, modular design, and improved reliability. As a consequence, it has gained increased penetration in high power applications such as grid-tied PV power systems, static synchronous compensators (STATCOMs), and medium voltage drives. However, it is not uncommon for three-phase CHB systems to face the challenge of unbalanced power generation among phases. For instance, CHB converters in fault-tolerant operations, in grid-tied PV applications [84]-[86], in large-scale PV farms with unevenly distributed solar irradiance [87]-[92], or in motor drives operating with faulty HB cells [93]. Alternatively, applications, such as static var generator (SVG) or STATCOM which serve as the reactive power and imbalance compensator are also required to deal with this issue [94]-[95]. To cope with imbalances, the ZSI technique is widely adopted. The theory behind this principle is to shift the CHB converter's neutral point by injecting a ZSC or ZSV, depending on the converter configuration Δ or Y connection as shown Fig. 5.1, when the imbalance is encountered. By doing so, it is possible to extract different power levels per-phase from the converter size while delivering balanced power per-phase to the grid and/or load.

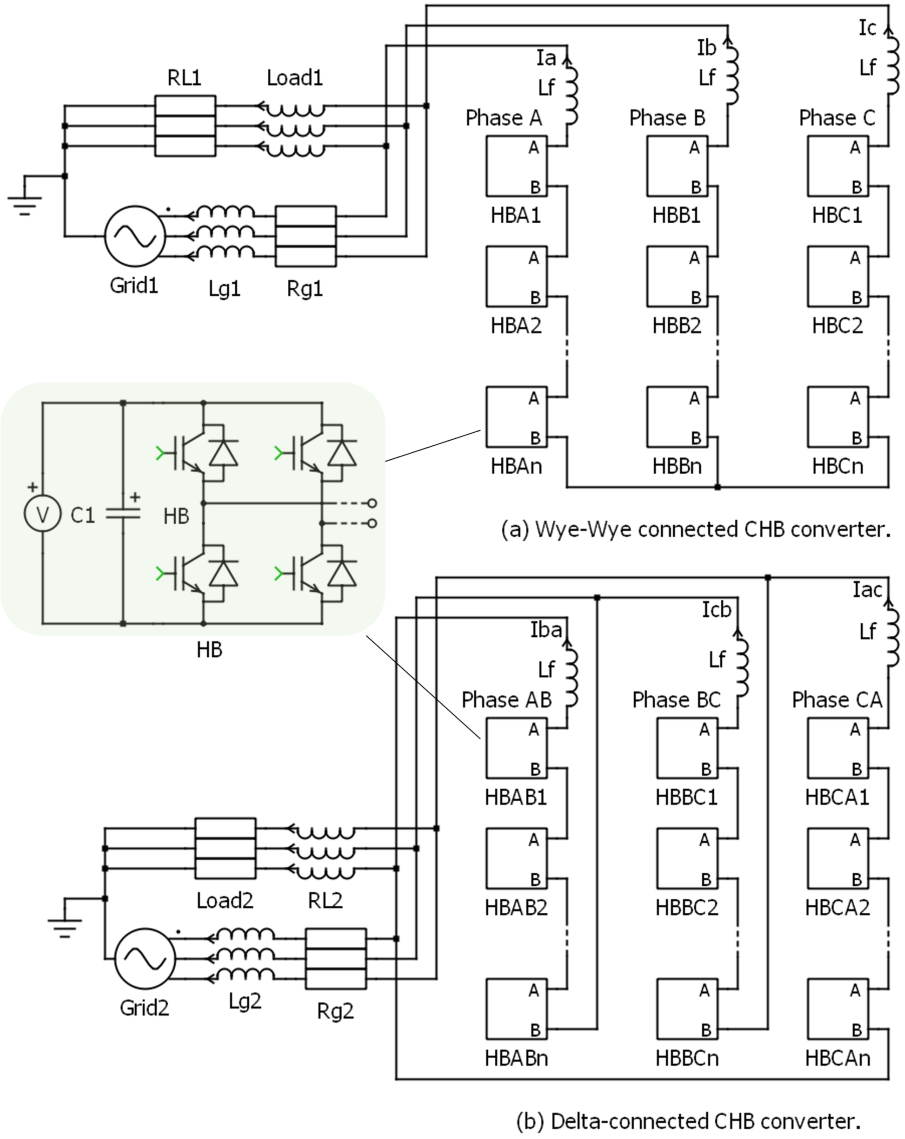


Fig. 5.1 Schematic of a CHB-based three-phase power system with (a) Y-Y (b) Δ-Y connection.

Reent studies have reported the superior power balancing capability (PBC) of Δ- over Y- connection three-phase systems [87]-[88] and [94]. The Δ-connected configuration is reported to be capable of handling 92.32% of all power imbalance cases as compared to the Y, which is 4.29%, for a CHB multilevel converter in grid connected PV systems [87]. The key limiting factor of delivering available power to compensate the imbalance in Y-configurations is the DC link capacitor voltage [88]. Efforts are being made to improve

the utilization of the DC link voltage to extend the balancing capability by proposing high-order harmonic injection methods, such as double third harmonic injection, optimal ZSI (OZSI) [89]-[90]. Quantitative evaluation of the aforementioned methods is presented in [88]. Additionally, investigations of their accuracy, complexity, and power balancing capability are also compared and summarized in [91], indicating OZSI is the most promising method to cope with the imbalanced Y-Y system.

In most of the aforementioned works, the emphasis is on improving the PBC of ZSV in Y-connected systems, alternatively on analysing and comparing the PBC of coping with the imbalance of Y- and Δ- configurations. However, to the best of our knowledge, PBC-related thermal issue have not been compared for the CHB Δ- and Y- configurations. Existing works which take thermal aspects into consideration are, for instance, ZSV injection to redistribute the losses in a three-phase neutral-point clamped (NPC) converter [96]-[97], or injecting the common mode voltage to a three-phase modular multilevel converter (MMC) to achieve the overall reduction in conduction losses [98]. The former considers device-level thermal performance of the converter to improve reliability, while the latter comes from the loss reduction point of view and aims to increase the converter efficiency. However, none have compared the thermal performances of different three-phase connections. Additionally, the existing investigations on lifetime evaluation of MMC in PV or wind power applications emphasize on studying the impacts of complicated loading mission profiles on the estimation [3], [14] [34], but very few of them have looked into the effects brought by three-phase power imbalance. Hence, to fill this gap, the aim of this work is to investigate the thermal performance and the corresponding impact on the lifetime of Y- and Δ- configurations operating with ZSI. In this study, Y-Y and Δ-Y configurations are investigated and analyzed for illustration, nevertheless, the methodology does not depend on the load end connection, and can be applied to other configurations, such as Y-Δ or Δ-Δ.

5.3 Review of Zero-Sequence Injection

In this section, the injection of fundamental frequency ZSV/ZSI into a three-phase Y- or Δ- grid-connected power system is revisited based on [87] and [90]. The representation of the instantaneous ZSV v_o and ZSC i_o required to be injected into the Y- and Δ-connected three-phase systems are revisited in Sections 5.3.1 and 5.3.2 respectively.

5.3.1 Zero-sequence voltage calculation

Based on [90], the representation of the zero-sequence voltage is defined by (5.1), which is composed of a voltage amplitude V_o and angle θ. Moreover, ω_g depicts the grid phase angle. Both are dependent on the power generation ratio $(\lambda_a, \lambda_b, \lambda_c)$ of each phase with respect to the nominal power P_{nom}. The detailed angle sector selection is displayed in Table. 5.1.

$$v_o = \sqrt{3} V_o \cos(\omega_g + \theta) \tag{5.1}$$

The amplitude V_o is defined as

$$V_o = \frac{\sqrt{6}\Delta_\lambda}{3(\lambda_a + \lambda_b + \lambda c)} V_g \tag{5.2}$$

where

$$\lambda_i = \frac{p_i}{P_{nom}/3}, \quad i = (a,b,c) \tag{5.3}$$

$$\Delta_\lambda = \sqrt{(\lambda_a - \lambda_b)^2 + (\lambda_b - \lambda_c)^2 + (\lambda_c - \lambda_a)^2} \tag{5.4}$$

The angle θ is defined as

$$\theta = \begin{cases} \sin^{-1}(\sqrt{6}\frac{\lambda_c - \lambda_b}{2\Delta_\lambda}) & \text{Section I, VI} \\ \sin^{-1}(\sqrt{6}\frac{\lambda_b - \lambda_a}{2\Delta_\lambda}) + \frac{2\pi}{3} & \text{Section II, III} \\ \sin^{-1}(\sqrt{6}\frac{\lambda_a - \lambda_c}{2\Delta_\lambda}) + \frac{4\pi}{3} & \text{Section IV, V} \end{cases} \tag{5.5}$$

Table 5.1 Zero-sequence voltage vector sectors.

Power Generation Ratio	Sector
$\lambda_b < \lambda_c < \lambda_a$	I
$\lambda_b < \lambda_a < \lambda_c$	II
$\lambda_a < \lambda_b < \lambda_c$	III
$\lambda_a < \lambda_c < \lambda_b$	IV
$\lambda_c < \lambda_a < \lambda_b$	V
$\lambda_c < \lambda_b < \lambda_a$	VI

5.3.2 Zero-sequence current calculation

Similarly, the representation of the ZSC can be calculated by (5.6) according to [87], which is composed of a current amplitude I_o and angle θ. Both are also dependent on the power generation ratio $(\lambda_{ab}, \lambda_{bc}, \lambda_{ca})$ of each phase with respect to the nominal power P_{nom}. The selection of the θ sector is depicted in Table. 5.2.

$$i_o = \sqrt{2} I_o \cos(\omega_g + \theta) \tag{5.6}$$

with the amplitude defined as

$$I_o = \frac{\sqrt{2}\Delta_\lambda P_{nom}}{9 V_g} \tag{5.7}$$

where

$$\lambda_i = \frac{p_i}{P_{nom}/3}, \quad i = (ab, bc, ca) \tag{5.8}$$

$$\Delta_\lambda = \sqrt{(\lambda_{ab} - \lambda_{bc})^2 + (\lambda_{bc} - \lambda_{ca})^2 + (\lambda_{ca} - \lambda_{ab})^2} \tag{5.9}$$

The angle θ is defined as

$$\theta = \begin{cases} \sin^{-1}(\sqrt{6}\frac{\lambda_{ca}-\lambda_{bc}}{2\Delta_\lambda}) + \frac{\pi}{6} & \text{Section I, VI} \\ \sin^{-1}(\sqrt{6}\frac{\lambda_{bc}-\lambda_{ab}}{2\Delta_\lambda}) + \frac{5\pi}{6} & \text{Section II, III} \\ \sin^{-1}(\sqrt{6}\frac{\lambda_{ab}-\lambda_{ca}}{2\Delta_\lambda}) + \frac{3\pi}{2} & \text{Section IV, V} \end{cases} \tag{5.10}$$

Table 5.2 Zero-sequence current vector sectors.

Power Generation Ratio	Sector
$\lambda_{bc} < \lambda_{ca} < \lambda_{ab}$	I
$\lambda_{bc} < \lambda_{ab} < \lambda_{ca}$	II
$\lambda_{ab} < \lambda_{bc} < \lambda_{ca}$	III
$\lambda_{ab} < \lambda_{ca} < \lambda_{bc}$	IV
$\lambda_{ca} < \lambda_{ab} < \lambda_{bc}$	V
$\lambda_{ca} < \lambda_{bc} < \lambda_{ab}$	VI

5.4 Control Implementation

5.4.1 Reference frame transformation

To inject the ZSC/ZSV, it is essential to change the actuation voltage of the three-phase system. To facilitate the analysis of the three-phase system and simplify the control procedure, the *abc* reference frame is translated into a two-axis frame, such as stationary $\alpha\beta$ or synchronous dq frame.

The Clarke transformation can help in transforming the *abc* frame to the $\alpha\beta$ frame as expressed in (5.11), which uses the current as an example. The current components along the α and β axes are sinusoidal, they feature as perpendicular and independent to each other.

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ 0 & \sqrt{3} & \sqrt{3} \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{5.11}$$

The Park transformation, also named the dq transformation, can be expressed as

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos\theta_s & \sin\theta_s \\ -\sin\theta_s & \cos\theta_s \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{5.12}$$

where θ_s is the rotating angle between $\alpha\beta$ and dq (5.12). Similarly, i_d and i_q are also perpendicular and independent to each other, however, instead of being sinusoidal, they are constant DC components.

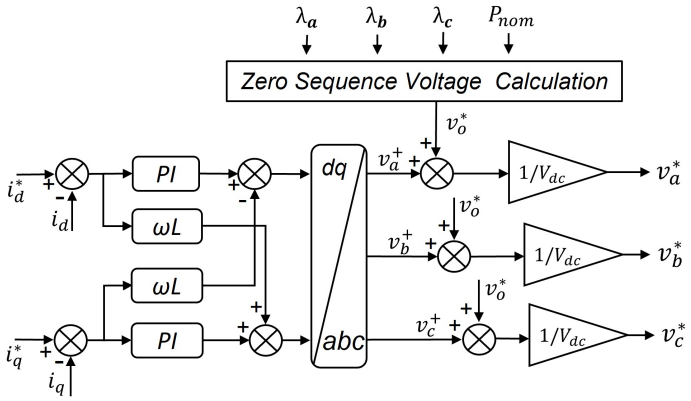
5.4.2 Control implementation

The control principles of injecting ZSV or ZSC to a Y- or Δ-connected CHB converter three-phase system are discussed in Sections 5.4.2.1 and 5.4.2.2, respectively. Moreover, the detailed procedure of employing PR controllers to regulate a Δ-connected CHB three-phase system in a digital controller is explained in Section 5.4.2.3.

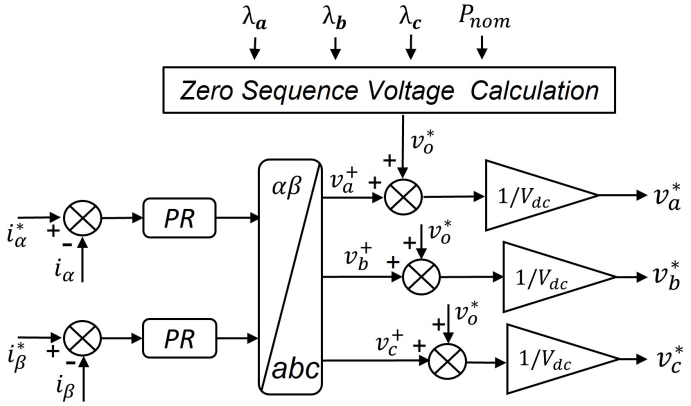
5.4.2.1 ZSV injection

The proportional-integral (PI) and proportional-resonant (PR) controllers adopted to inject the ZSV to cope with power imbalances are illustrated in Figs.5.2a and 5.3b, respectively. In Fig.5.2a, the three-phase balanced currents are firstly translated to a dq-framework, i.e., i_d and i_q. They are then compared to desired balanced dq-currents, i_d^* and i_q^*, which are regulated by a pair of PI controllers. Afterwards, these controllers provide a required dq-balanced inverter voltage, which is transformed to the original abc-framework, v_a^+, v_b^+, v_c^+. Then, based on the power generation ratio λ_i per-phase, the required ZSV, v_o^*, is directly added to each balanced phase voltage to obtain the final unbalanced voltage reference, v_a^*, v_b^*, v_c^*, to be synthesized at the modulation stage.

Regulation achieved by PR controllers as illustrated in Fig.5.2b follow similar procedures to the PI controllers, simply replacing the desired balanced currents into the $\alpha\beta$-framework, i.e., i^*_α and i^*_β, and employing a pair of PR controllers instead of PI ones.



(a)



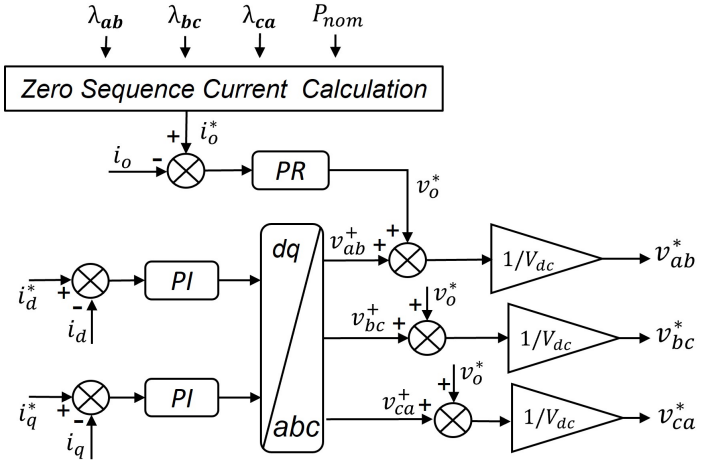
(b)

Fig. 5.2 Control diagrams of CHB-based three-phase Y-Y connected power systems using (a) PI controllers, and (b) PR controllers.

5.4.2.2 ZSC injection

Conversely, for the Δ-connection case, after being regulated by either PI or PR controllers as illustrated in Figs.5.3a and 5.3b, the output of the controllers are in fact the line-to-line balanced inverter voltages, $v^+_{ab}, v^+_{bc}, v^+_{ca}$. In addition, in this case the required ZSC, i^*_o,

is regulated by an extra resonant (PR) controller, which finally determines the required common-mode voltage, V_o, to be injected to each line-to-line branch.



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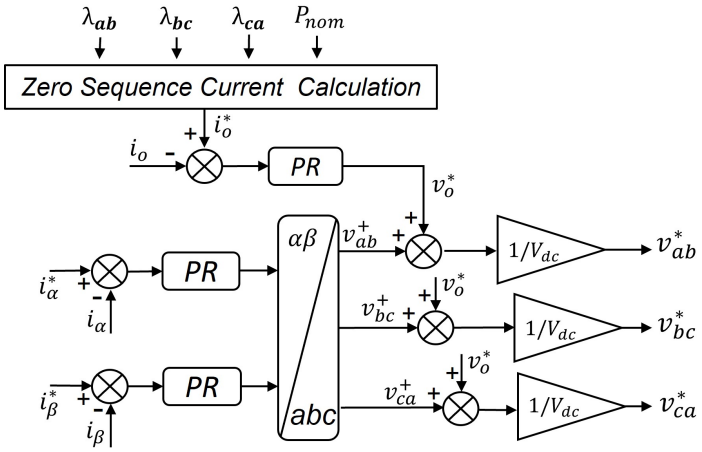


(b)

Fig. 5.3 Control diagrams of CHB-based three-phase Δ-Y connected power systems using (a) PI and PR controllers, and (b) PR controllers.

5.4.2.3 Implementation in digital controller

In this section, the detailed analysis of employing PR controllers to regulate the power of Δ-configurations and implementation in the digital controller is explained as an example.

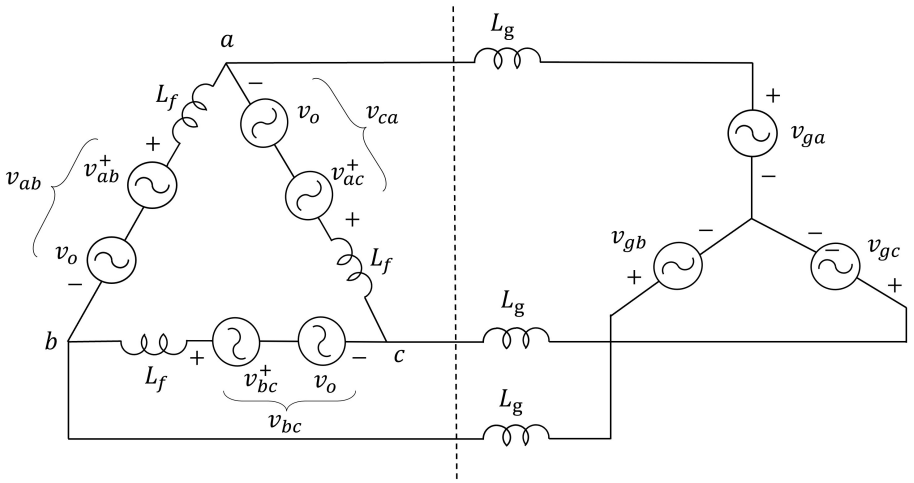


Fig. 5.4 A Δ-connected CHB-based three-phase power system consist of positive sequence, and zero sequence voltage which is for generating ZSC.

1. Consider a Δ-Y three-phase power system with unbalanced phase cluster power as shown in Fig. 5.4. The phase cluster voltage v_{ab}, v_{bc}, v_{ca} can be considered as a composite of positive sequence voltage v^+_{ab}, v^+_{bc}, v^+_{ca} and zero sequence voltage v_o.

2. Decouple the system and take only the positive sequence voltage into account, as illustrated in Fig. 5.5a. As in the Δ-Y configuration, positive sequence voltages are actually the line-to-line balanced inverter voltages, for ease of construction of the control system plant, it is converted into an equivalent Y-Y configuration as shown in Fig. 5.5b. The filter inductance L_g becomes $1/3$ of its original value. With the Clarke transformation, the plants of this system can be translated into an $\alpha\beta$ frame, and simplified as depicted in Fig. 5.5c. After being regulated by PR controllers, the actuation voltage for a balanced Y-Y three-phase system can be obtained as $v^+_{i,a}$, $v^+_{i,b}$, and $v^+_{i,c}$. By subtracting the two in (5.13), the line-to-line reference voltage for a Δ-Y

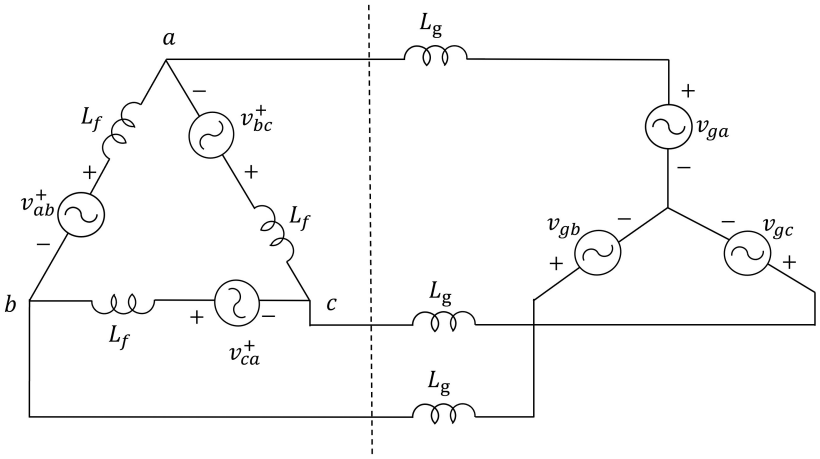
positive sequence system can be acquired.

$$\begin{cases} v_{ab}^{+} = v_{i,a}^{+} - v_{i,b}^{+} \\ v_{bc}^{+} = v_{i,b}^{+} - v_{i,c}^{+} \\ v_{ca}^{+} = v_{i,c}^{+} - v_{i,a}^{+} \end{cases} \tag{5.13}$$

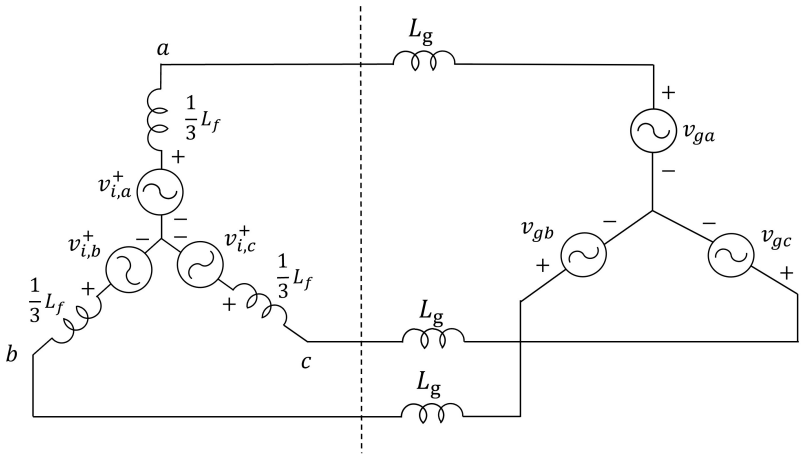
3. Zero-sequence voltage. When considering the internal loop of the three-phase cluster, the system can be further simplified as shown in Fig. 5.6a. The system only contains ZSV and the filter inductors, as the sum of the positive sequence components is zero. Hence, the plant of the system can be simplified as depicted in Fig. 5.6b. The ZSC, i_o^*, therefore can be sent to the PR controller, and finally determined the required common-mode voltage, V_o, to be injected into each line-to-line voltages.

5.5 Simulation of Balanced and Unbalanced 5-level Y-Y and Δ-Y Connected CHB Converter-based Three-Phase Systems

In this section, 5-level Y-Y and Δ-Y connected three-phase systems with balanced and unbalanced power generation of each phase are simulated, compared and discussed. The schematics of these two systems are the same as shown in Fig. 5.1. Two CHB modules are employed in each phase with a phase-shifted modulation scheme, and for simplicity purposes, an R-L load is used. Note that, due to the limitation of the employed power devices in [73], down scaled three-phase systems are simulated. Nevertheless, the ZSI introduced nonidentical stress distribution performances of the two configurations when three-phase power imbalance is encountered are generic and irrelevant to the power rating. To make a fair comparison, the same nominal power P_{nom} is applied. Two groups of different parameters



(a)



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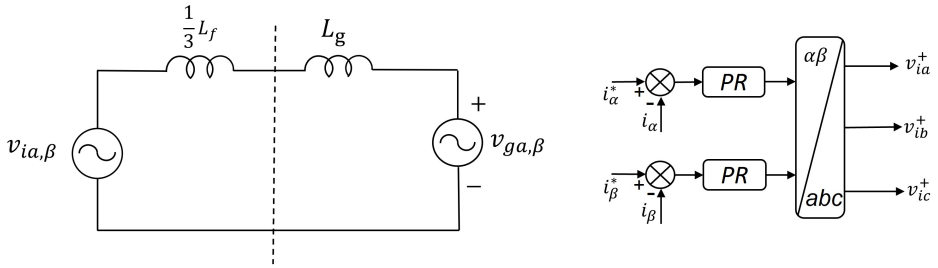
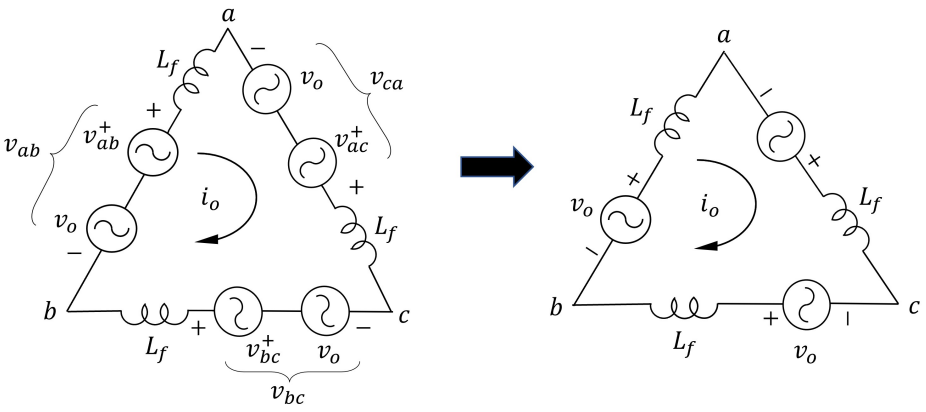
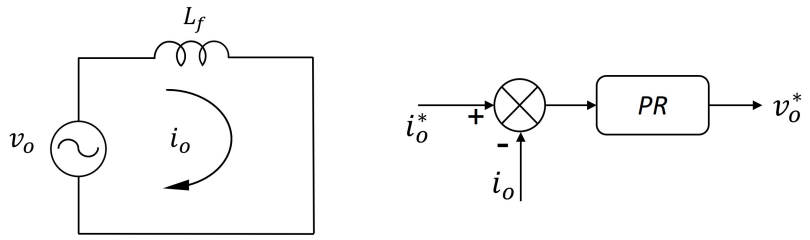


(c)

Fig. 5.5 Transformation of the PR control diagram of a Δ-Y connected CHB converter-based three-phase power system. (a) Balanced Δ-Y grid-tied system with positive sequence component. (b) Translation of the balanced Δ-Y system in (b) into a Y-Y configuration. (c) Plant of the system, and the control.



(a)



(b)

Fig. 5.6 Transformation of the PR control diagram of a Δ-connected CHB-based three-phase power system, (a) Zero sequence component. (b) Plant of PR controller for ZSC regulation.

are adopted in the Δ-Y configuration. Parameters adopted in group (A) have the same R-L value as used in the Y-Y configuration, giving the substantially comparison of Y-Y and Δ-Y comparison, in which the phase voltage and current of Δ-Y are $\sqrt{3}$ and $1/\sqrt{3}$ of those in the Y-Y configuration, respectively. In group (B), the load resistance is reduced to about $1/3$ of that employed in the Y-Y configuration, and therefore the same phase cluster current of Δ-Y and Y-Y can be achieved. Detailed circuit parameters used in the simulation are displayed in Tables. 1.1 and 5.3.

Note that in practical Δ- and Y-connected three-phase systems, different numbers of submodules or submodules with different power rating devices/heat sinks should be applied depending on their design requirements due to the characteristics of these two configurations and/or the costs. For instance, more submodules are adopted in the Δ-connections as compared to the Y-configurations when they are shared with the same line-to-line voltage

Table 5.3 Parameters in Simulation

Parameter	Y-Y	Δ-Y (A)	Δ-Y (B)
HB module input power V_{dc}	150 V	210 V	150 V
Numbers of HB modules per phase	2	2	2
Load line-to-line voltage V_L	247 V	247 V	143 V
Carrier frequency	1.5 kHz	1.5 kHz	1.5 kHz
Three-phase nominal power	1.8 kW	1.8 kW	1.8 kW
Load resistance	33.5 Ω	33.5 Ω	11 Ω
Load inductance	10 mH	10 mH	10 mH
Heat Sink Thermal resistance R_{th}	8 Ω	8 Ω	8 Ω

and different system power ratings [88]. The reason for using the same power MOSFET and heat sink is owing to the known lifetime information of the device, which can help users to estimate the lifetime and also gives a hint of the unevenly distributed lifetime of the Δ-system.

5.5.1 Y-Y three-phase system

5.5.1.1 Case 1: Balanced operation ($\lambda_a = \lambda_b = \lambda_c = 1$)

With equal power generation of each phase cluster, both the phase voltage $V_{a,b,c}$ and current $I_{a,b,c}$ are symmetric as illustrated in Fig. 5.7. Since in this configuration, the three-phase load currents $I_{la,lb,lc}$ share the same current flow with the phase currents, the same RMS value of 4.2 A can be obtained. The ZSV to deal with the power imbalance is almost 0 V. In addition, with phase-shifted modulation technique, the H-bridge submodules in a phase share the same losses. Hence, devices in a phase feature the same thermal performances, which is about 75 °C at 25 °C ambient temperature T_a.

5.5.1.2 Case 2: Unbalanced interphase power ($\lambda_a = 1,\ \lambda_b = 0.9,\ \lambda_c = 0.7$)

In an unbalanced situation, a clear nonidentical phase voltage can be observed in Fig. 5.8. Less output voltage of phase C can be found as compared to that in the balanced case due to

ZSV, which is a 50 Hz sinusoidal waveform with amplitude of 40 V to ensure equal power delivery to the load. Nevertheless, the phase current is regulated and still balanced due to ZSI. Since the total power generation is reduced, the phase cluster RMS drops from 4.2 A to 3.9 A, which leads to a reduction of junction temperature of all three-phase HB modules from the nominal 75 °C to 65 °C. Another finding is that, the injected ZSV has little impact on the thermal performance of H-bridge modules in each phase, as they are still identical. This comes from the fact that the power losses mainly depend on the current level rather than voltage.

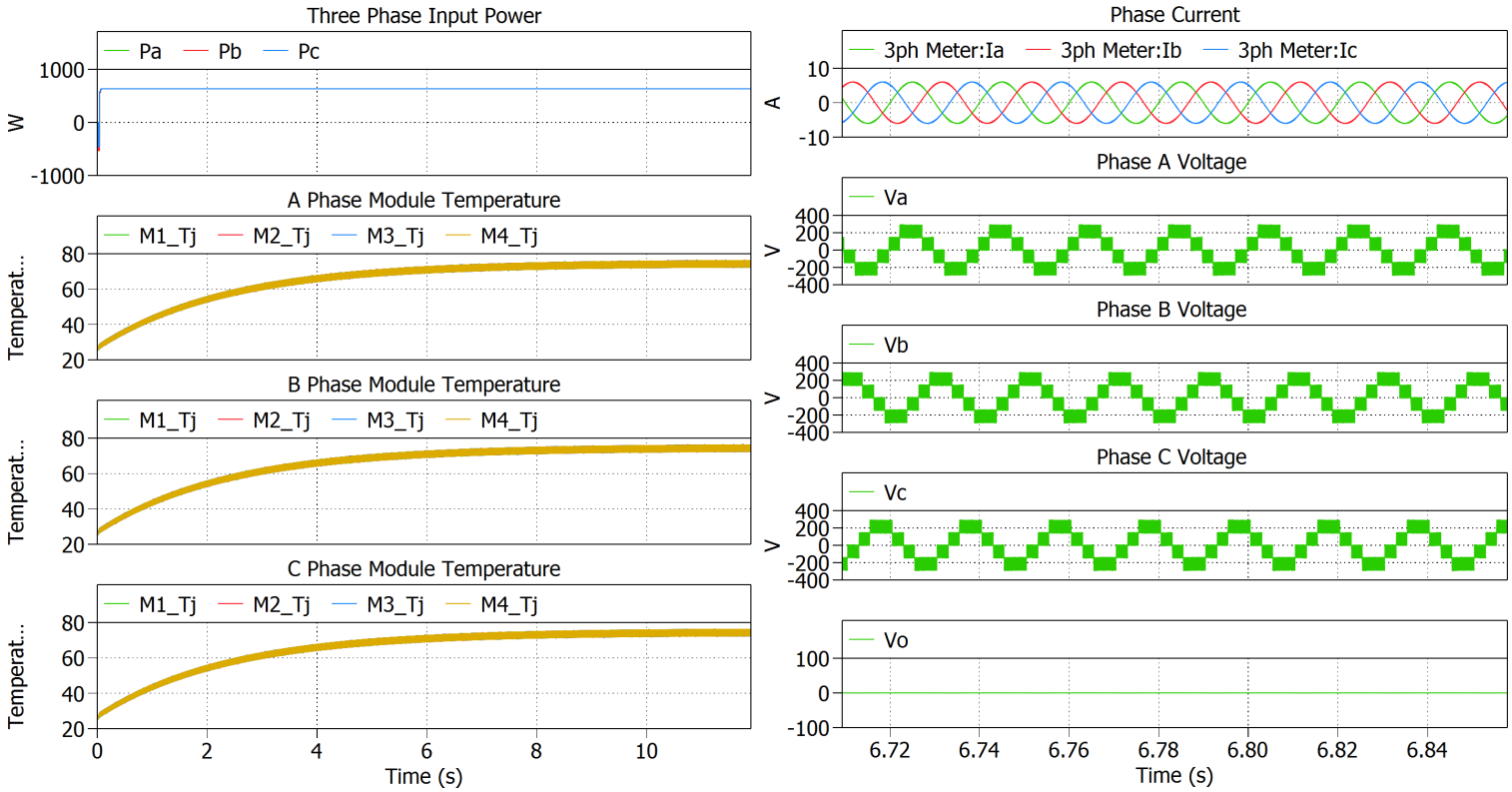


Fig. 5.7 Performance of a 5-level Y-Y connected three-phase power system with balanced power generation $P = P_{nom} = 1.8$ kW, $\lambda_a = \lambda_b = \lambda_c = 1$ and $R = 33.5\ \Omega$.

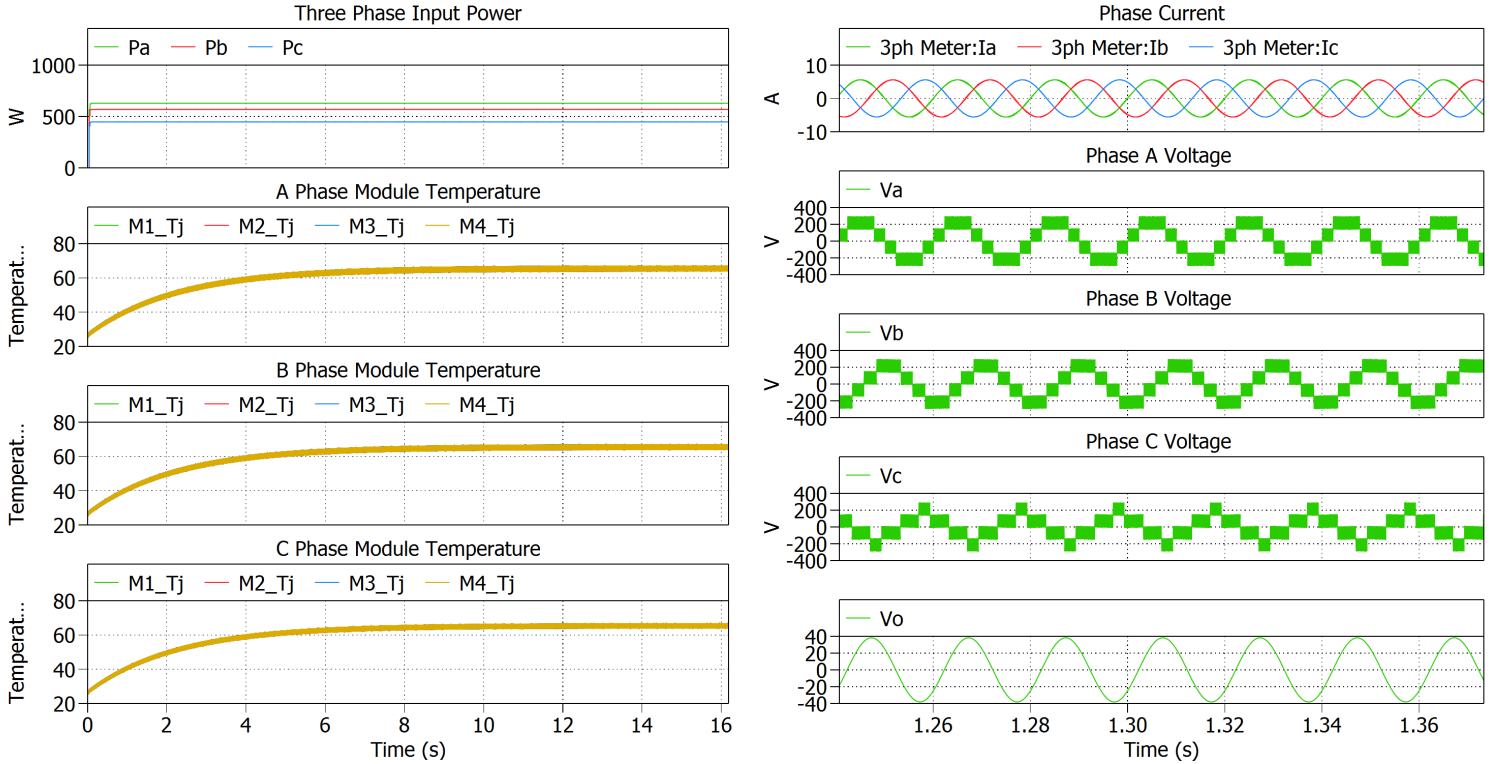


Fig. 5.8 Performance of a 5-level Y-Y connected three-phase power system with unbalanced power generation $P = 0.87P_{nom} = 1.56$ kW, $\lambda_a = 1,\ \lambda_b = 0.9,\ \lambda_c = 0.7$ and $R = 33.5\ \Omega$.

5.5.2 Δ-Y three-phase system with $R = 33.5\ \Omega$ (A)

In this case, the Δ-Y configuration with the same load ($R = 33.5\ \Omega$ and $L = 10\ mH$) as that in the Y-Y configuration is simulated.

5.5.2.1 Case 1: Balanced operation ($\lambda_{ba} = \lambda_{cb} = \lambda_{ac} = 1$)

In a balanced operation condition, the three-phase current $I_{ba,cb,ac}$, load current $I_{a,b,c}$ and phase voltage $V_{ab,bc,ca}$ are symmetric as depicted in Fig. 5.11. The approximate RMS value of phase and load currents are 2.4 A and 4.2 A, respectively. Almost 0 A ZSC I_o is injected due to the balanced operation condition. Moreover, identical thermal performance of the devices in three-phase can also be found with a value of 37.7 °C. The value is lower than that in the Y-Y configuration due to the characteristic of the Δ configuration that, the phase voltage and current are $\sqrt{3}$ and $1/\sqrt{3}$ of that in the Y configuration.

5.5.2.2 Case 2: Unbalanced three-phase power generation ($\lambda_{ba} = 1,\ \lambda_{cb} = 0.9,\ \lambda_{ac} = 0.7$)

In this case, the phase currents $I_{ba,cb,ac}$ are no longer identical, but deviate from one to another as a result of unequal power generation as shown in Fig. 5.9. The RMS values of I_{ba}, I_{cb}, and I_{ac} are 2.77 A, 2.35 A, and 1.8 A, respectively. The load per phase current $I_{a,b,c}$ is regulated and symmetric due to the injection of ZSC, with RMS values of 3.9 A and 0.48 A, respectively. On the other hand, the thermal performance of each module differs from one to another, from the minimum 31.8 °C in phase CA, medium 36.5 °C in phase BC, to the maximum 41.7 °C in phase AB. The decreased temperature of BC and CA phases are clearly caused by the decreased power generation of these two phases, while 4 °C more than the nominal temperature can also be seen in phase AB. In this scenario, although the positive sequence current is reduced due to the overall three-phase power reduction, with the injection of I_o, the current of the phase with the largest power (e.g., the AB phase) can be potentially

pushed to a higher degree. Therefore, an overstress in phase AB can be concluded. Moreover, this situation is worsened with the increase of the severity of the three-phase imbalance power ratio. For instance, with λ_{ba}=1, λ_{cb}=0.8, and λ_{ac}=0.6, the temperature difference can be from 32 °C to 54 °C, and the stress on the AB phase suffers thermal stress about 16.3 °C more than the nominal design.

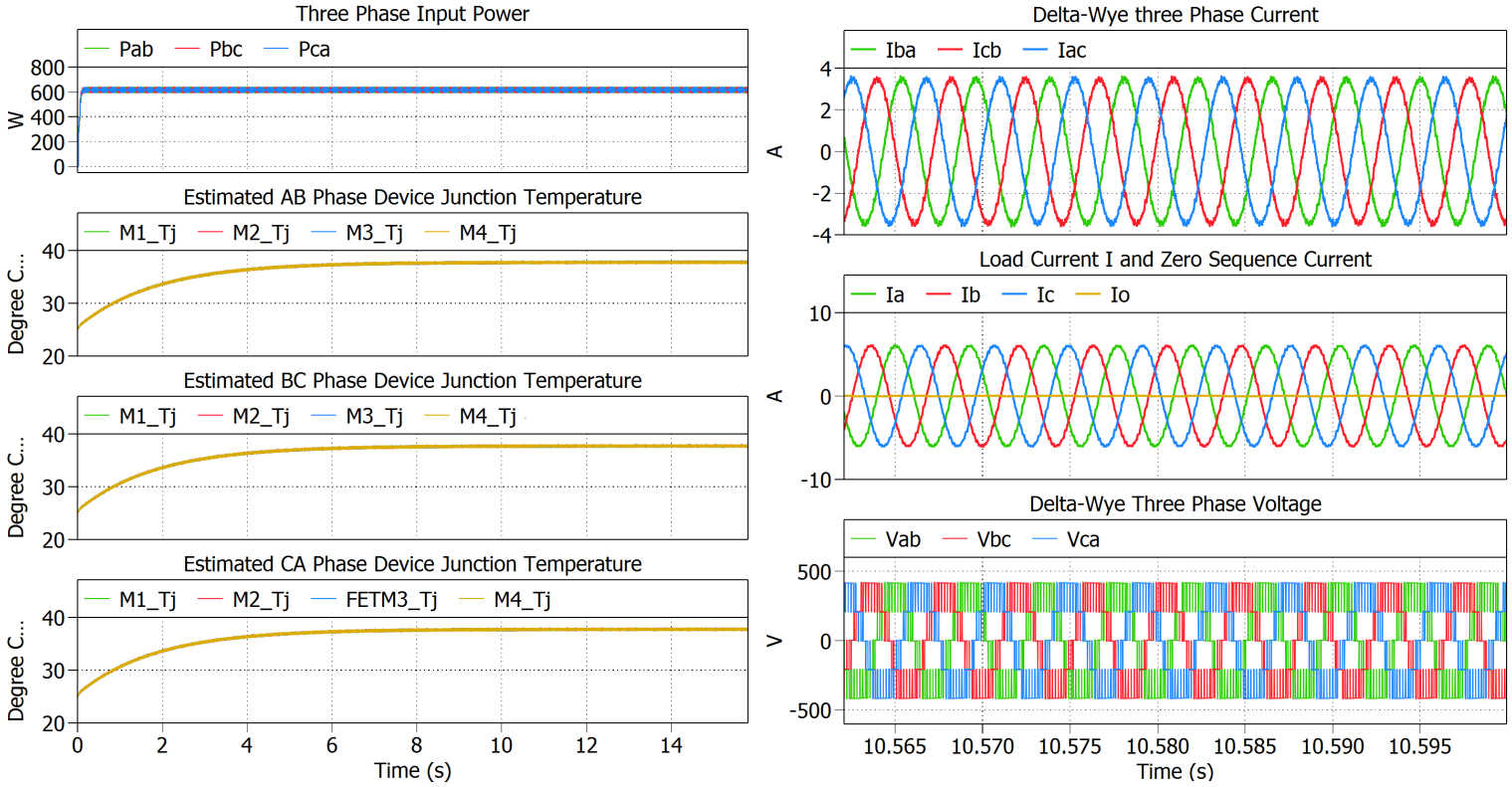


Fig. 5.9 Performance of a 5-level Δ-Y connected three-phase power system with balanced power generation $P = P_{nom} = 1.8$ kW, $\lambda_{ab} = \lambda_{bc} = \lambda_{ca} = 1$ and $R = 33.5\ \Omega$.

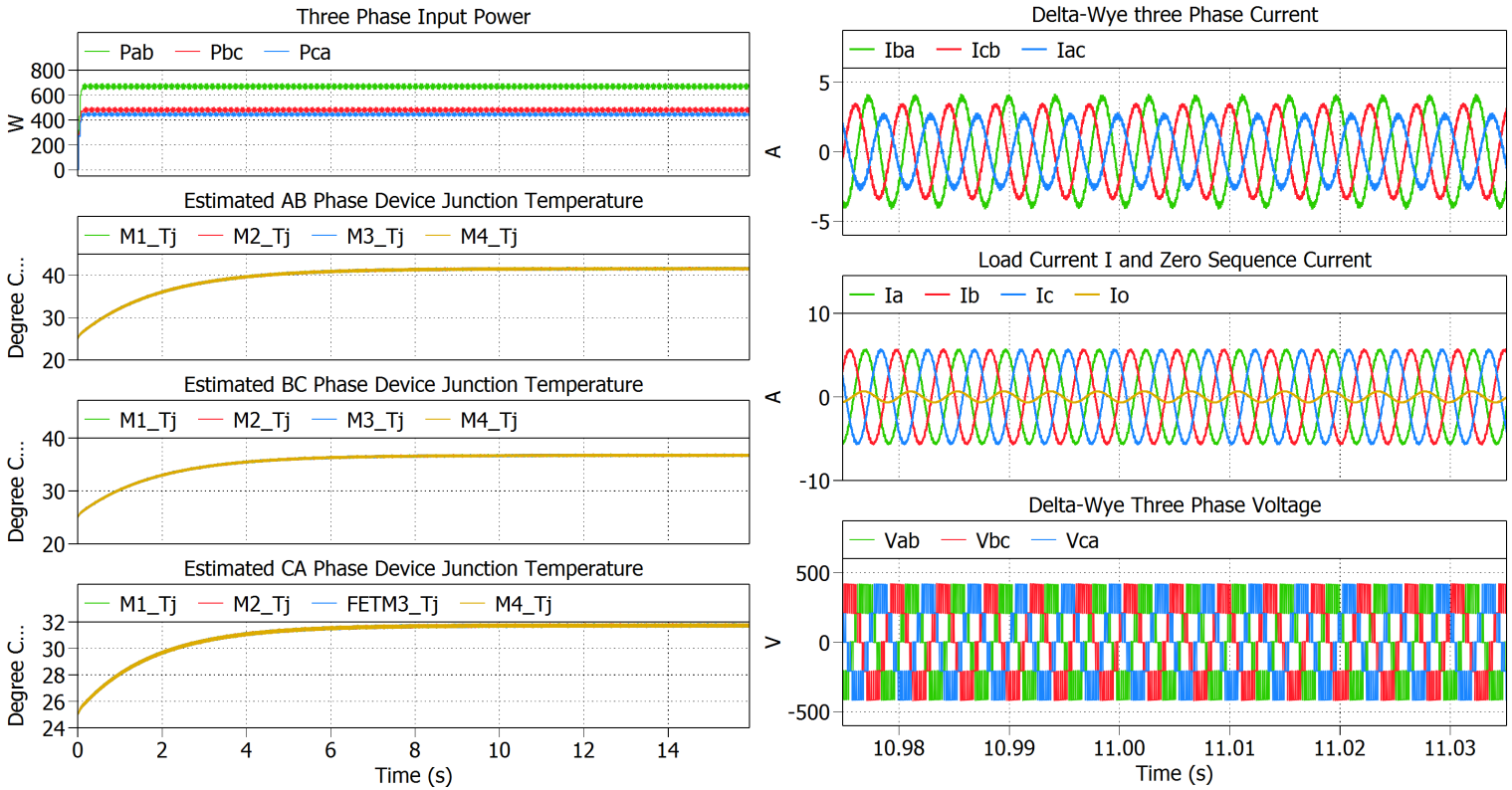


Fig. 5.10 Performance of a 5-level Δ-Y connected three-phase power system with unbalanced power generation $P = 0.87P_{nom} = 1.56$ kW, λ_{ba}=1, λ_{cb}=0.9, λ_{ac}=0.7, and $R = 33.5\ \Omega$.

5.5.3 Δ-Y three-phase system $R = 11\ \Omega$ (B)

In this case, the Δ-Y connected three-phase system with reduced load resistance ($R = 11\ \Omega$ and $L = 10\ mH$) to that in the Y-Y configuration is simulated. By doing so, identical phase cluster currents of the two configurations can be achieved and compared. Both the electrical and thermal performances of the balanced and unbalanced cases follow a similar trend to that in group A as explained in Section 5.5.2. Nevertheless, clearer observations of device temperature variations can be obtained due to the enlarged current.

5.5.3.1 Case 1: Balanced operation ($\lambda_{ba} = \lambda_{cb} = \lambda_{ac} = 1$)

In the nominal operation condition, the three-phase and load currents $I_{ba,cb,ac}$ and $I_{a,b,c}$ feature symmetrically, with RMS values of 4.2 A and 7.3 A, respectively, as illustrated in Fig. 5.11. The phase voltages $V_{ab,bc,ca}$ are also balanced, with almost 0 A ZSC I_o. Moreover, identical junction temperatures of all three-phase devices with values of 75 °C can be seen due to the enlarged phase current.

5.5.3.2 Case 2: Unbalanced three-phase power generation ($\lambda_{ba} = 1, \lambda_{cb} = 0.9, \lambda_{ac} = 0.7$)

Nonidentical three-phase currents $I_{ba,cb,ac}$ can be obtained as depicted in Fig. 5.12, for which the RMS values are 4.67 A, 4.15 A, and 3.1 A, respectively. Resulting from the increased three-phase current due to reduced load resistance and also the deviation, the thermal performance of devices among the three-phase varies significantly. The devices in phase AC have the lowest temperature of 47.5 °C, while those in phase BC are 73 °C, and those in phase AB show the highest temperature with 95 °C. Similarly, the three-phase load currents $I_{a,b,c}$ are regulated and symmetric with ZSI, with an RMS value of 6.8 A. The RMS value of ZSC to cope with the imbalance is about 0.87 A.

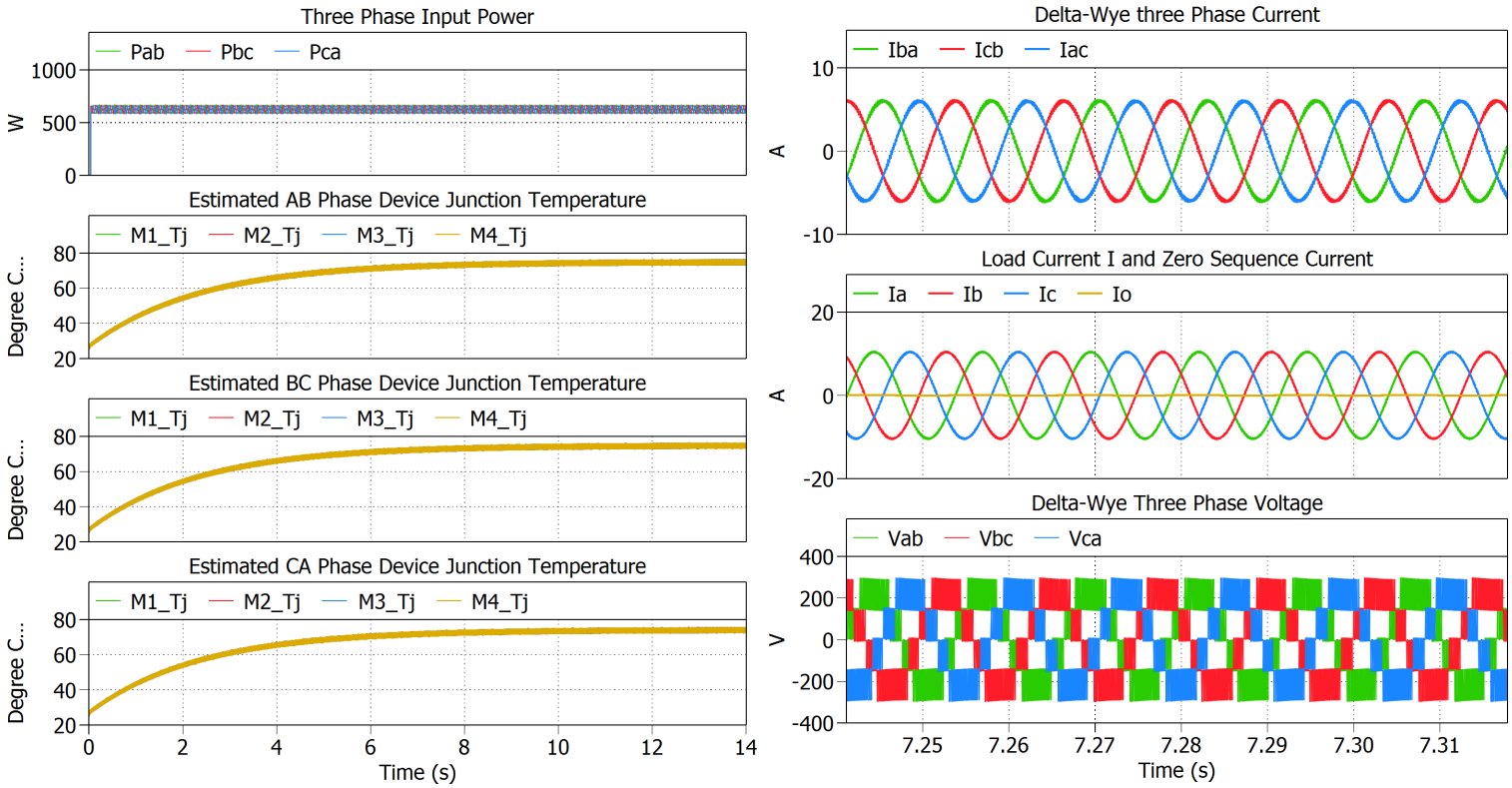


Fig. 5.11 Performance of a 5-level Δ-Y connected three-phase power system with balanced power generation $P = P_{nom} = 1.8$ kW, $\lambda_{ab} = \lambda_{bc} = \lambda_{ca} = 1$ and $R = 11\ \Omega$.

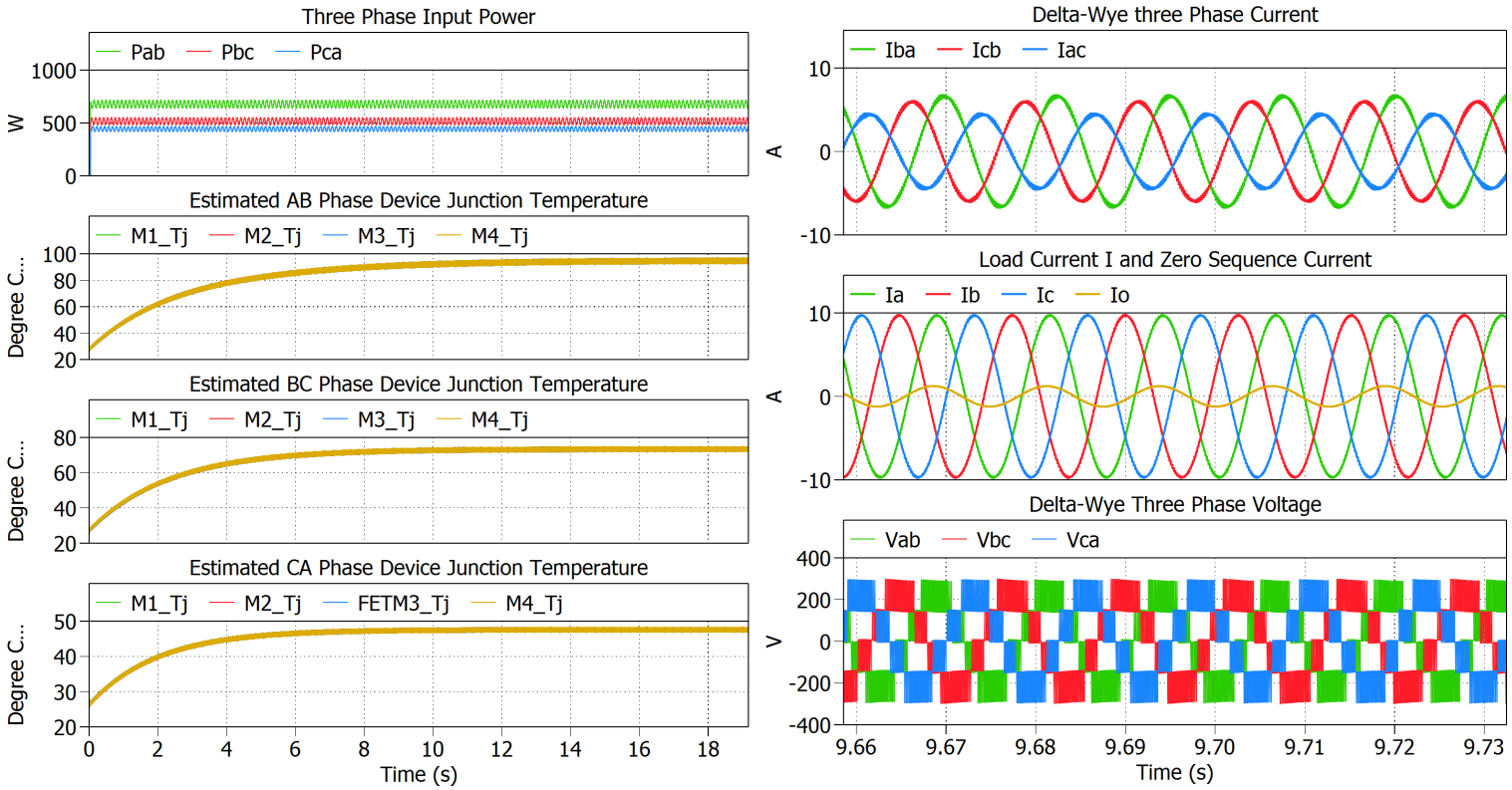


Fig. 5.12 Performance of a 5-level Δ-Y connected three-phase power system with unbalanced power generation $P = 0.87P_{nom} = 1.56$ kW, λ_{ba}=1, λ_{cb}=0.9, λ_{ac}=0.7, and $R = 11\ \Omega$.

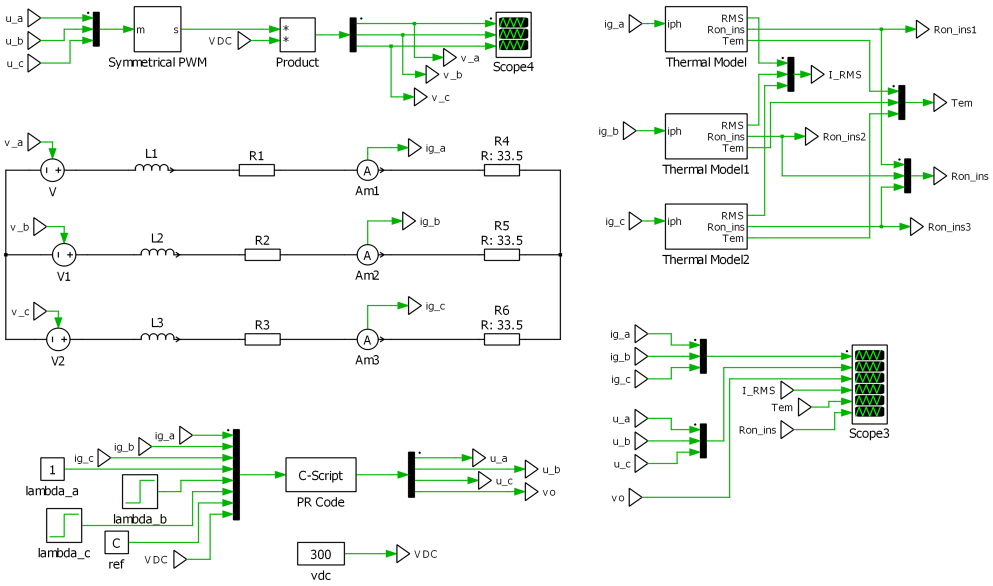
5.5.4 Averaged Thermal Model of Y-Y Connected Three-Phase System

In this section, a simple averaged thermal models which follows the same principle as proposed in Section 2.5 is presented for the Y-Y connected three-phase system as an illustration example. Similarly, the model is to tackle the long simulation time issue exists in the switching model. As any increase in the number of HB submodules and/or operation frequency of the switching three-phase systems will lead to a further increase in the simulation time, while the averaged model does not have this issue.

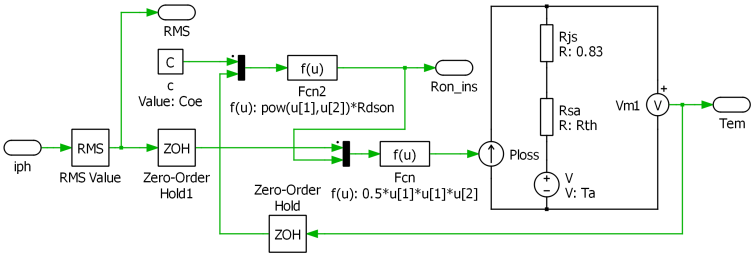
An overview of the electrical model of Y-Y three-phase can be obtained as depicted in Fig. 5.13a and the detail circuits adopted in the thermal model is given in Fig. 5.13b. The electrical model follows the existing large-signal averaged model of a three-phase system. The voltage source $v_{a,b,c}$ are the output of CHB converter voltages, and L_{1-3} and R_{1-6} represent three-phase R-L loads. A PR controller is employed to cope with the power imbalance issue among the three-phase.

Regarding the thermal model, as the input and output share the same phase currents, which can be input into the thermal model to calculate the corresponding temperatures of device in a phase. The phase RMS values are extracted first, and following the equation (2.14), the conduction losses of a power MOSFETs can be calculated. Note that, only the conduction losses are considered there, as they are the dominant contributor. R_{js} is an estimated thermal resistance, which is compose of the junction-to-case and case-to-heat sink thermal resistances. The values are according to the datasheet. The R_{sa} is the general heat sink thermal to ambient thermal resistance, and T_a is the ambient temperature.

Note that the model presented here is not a complete ETAM. Although the devices in a phase share the same averaged losses in the 50 Hz period, their averaged losses and $R_{ds,on}$ in one switching period differ from one to another due to the complicated and non-identical switching pattern. Future works on building the feedback loop from the thermal domain to the



(a)



(b)

Fig. 5.13 (a) Overview of the ETAM of Y-Y three-phase system. (b) Thermal model.

electrical domain should be conducted. Here, to facilitate the fast evaluation of temperatures and lifetimes of devices in each phase, only averaged thermal model is adopted.

To verify the proposed fast temperature estimation model of the Y-Y three-phase system, simulation is carried with the same operation conditions and parameters as described in Section 5.5.1. Almost identical performances of three-phase currents, v_o and also device temperatures as compared to that in the switching three-phase system can be observed when changing from nominal to unbalanced operation condition. The phase RMS values, v_o and three-phase device temperatures change from 4.2 A to 3.9 A, 0 V to 40 V and about 74.5 °C to 65 °C respectively. Due to the instantaneous calculation of the RMS currents, it requires

1 cycle time of the sinusoidal wave which is 0.02 s to reach the steady state when changes operation condition. The estimated device temperature and instantaneous $R_{ds,on}$ of a device in a phase follows the growing trend of the corresponding phase RMS value. Therefore, almost identical thermal performances and estimated $R_{ds,on}$ values can be observed of the three devices. Besides, the varied $R_{ds,on}$ under different operation conditions has stated the importance of the ETAM, as the value increases 44% and 39% respectively as compared to its original value. It also indicates the enhanced estimation accuracy of the temperature and lifetime of a device.

The simulation speed increases dramatically, with the propose d model, 1 s simulation can be finished within 20 s, while for the switching model, it requires about 300 s. In addition, with the model, the temperature of device reaches steady state quickly when the operation condition changes, indicating it is a good candidate in reliability assessment.

Although the Y-Y and Δ-Y CHB converter-based three-phase systems are complicated, as investigated in Section 5.5, the same thermal performances are shared by power devices in Y-Y configuration and in each phase of Δ-Y connection respectively regardless of the power condition when with the ZSI. Therefore, it is adequate to implement lifetime evaluation on one power device and one device per phase in the Y-Y and Δ-Y configurations respectively. Moreover, it is also feasible for this model to take the device's aging impacts into account and to adopt the proposed rainflow counting algorithm to facilitate the system lifetime evaluation by following the works presented in Chapters 3 and 4.

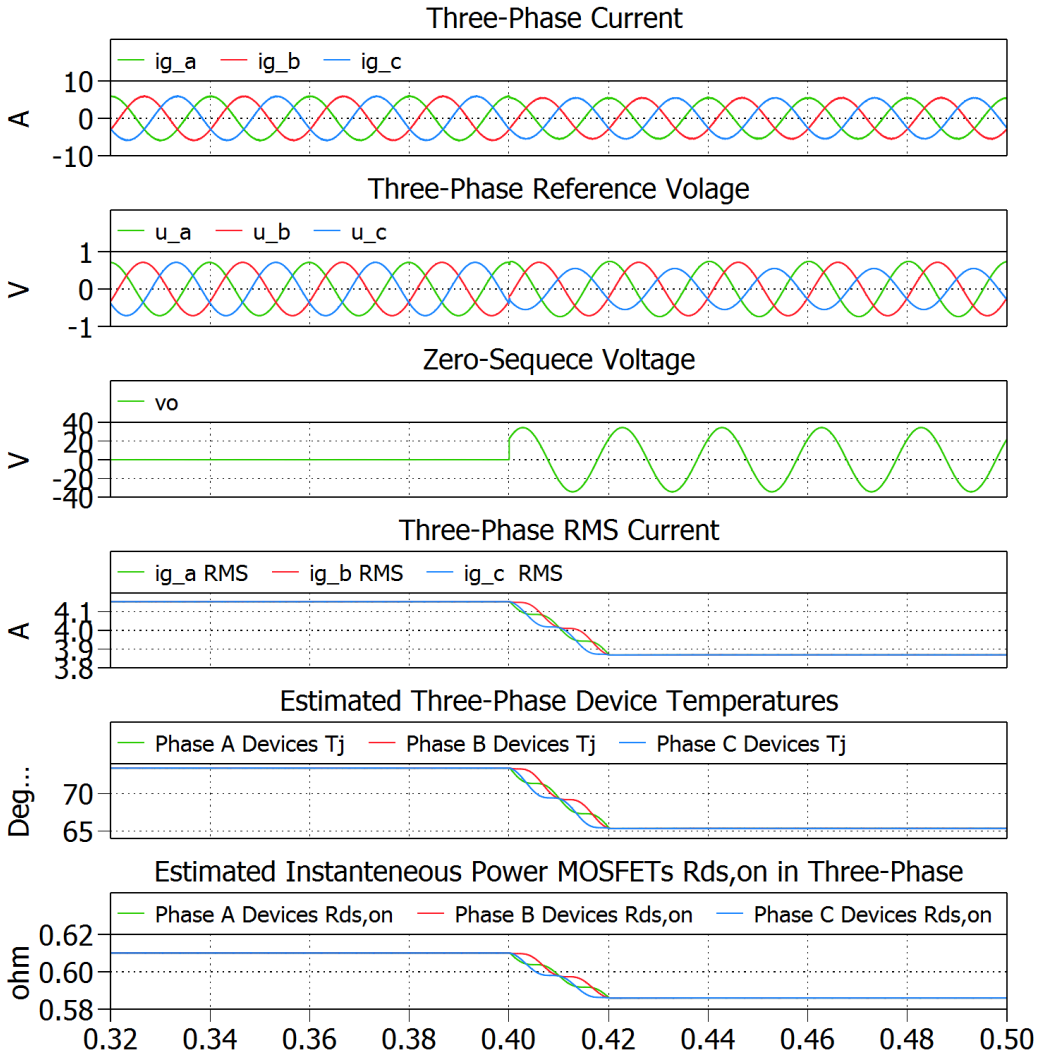


Fig. 5.14 Simulated results of the proposed ETAM of CHB converter-based Y-Y connected three-phase system.

5.5.5 Impact of ZSV and ZSC injections on reliability of Y-Y and Δ-Y systems

In this section, the reliability of Y-Y and Δ-Y systems are compared and discussed with the injected ZSV and ZSC. The device lifetime can be calculated by the widely accepted modified Coffin-Manson law in (1.4). The device number of cycles to fail N_f under certain stress can be determined. The parameters and empirical coefficients are dependent on the specific MOSFET model. For IRFP340, the parameters δ and A_1 are -5.2776 and 4.9283×10^{13}, respectively, according to [73].

Taking the load variation from balanced ($\lambda_a = \lambda_b = \lambda_c = 1/\ \lambda_{ab} = \lambda_{bc} = \lambda_{ca} = 1$) to an unbalanced situation ($\lambda_a = 1,\ \lambda_b = 0.9,\ \lambda_c = 0.7/\lambda_{ab} = 1,\ \lambda_{bc} = 0.9,\ \lambda_{ca} = 0.7$)) as the dominant operation condition, the corresponding N_f and in this variation are calculated. The stress undertaken on the devices in this transition is also evaluated. Since only one switching of operation condition is existing, a half thermal cycle is identified. Therefore, the generated stress during this action can be simply calculated as $1/(2N_f)$. With long varying loads, the stress of each cycle needs to be calculated and accumulated. Once it reaches 1, it is identified as a faulty device.

In Tables 5.4 and 5.5, summaries of thermal performances and resultant failure cycles and resultant stress on the device by changing the operation from Case 1 to 2 for Y-Y and Δ-Y (A) three-phase systems which with the same load, and Y-Y and Δ-Y (B) three-phase systems which with the same phase current are given and compared respectively.

Conclusions can be drawn from the tables and are as follows:

1. For the devices in Y-Y configuration, identical thermal performances of all three-phase can be observed regardless of the balancing of the system, as the ZSV regulates the imbalance by injecting the voltage instead of current. Therefore, the same stresses are suffered by devices when changing operation conditions. As a result, they potentially will fail at the same time.

2. In Table 5.4, with the same load, the Δ-Y three-phase system has longer lifespan compared to the Y-Y configuration, due to the intrinsic characteristic that the phase current of Δ-Y is $1/\sqrt{3}$ smaller than that in Y-Y. Therefore, devices in this configuration are subject to less thermal stress.

3. In both Tables 5.4 and 5.5, devices in the Δ-Y three-phase system suffer different thermal stresses with the ZSC when operating in the unbalanced condition. Unbalanced thermal distribution clearly will lead to an unequalled device lifetime expectation among these three phases.

4. In both Tables 5.4 and 5.5, devices in phase AB are overstressed in the unbalanced case as compared to the rated balanced case due to the ZSI. And the severity of the overstress is dependent on the system power rate and also the unbalancing ratio.

5. In the Δ-Y system, although the phase AB suffers the highest temperature, the phase CA is the one with the highest stress. The dominant term in N_f is the temperature fluctuation ΔT_j. Although phase BC produces less stress, the lifetime of whole three-phase system depends on the weakest point, which in this case is phase CA.

6. In Table 5.5, with the same phase cluster current, the Δ-Y three-phase system has lower lifespan as compared to the Y-Y configuration.

The reasons for conclusions 3-6 are due to that with the Y connection in the load end, when the system operates in an unbalanced condition, the reduced balanced three-phase load current is determined by the averaged power ratio $\bar{\lambda}$. This can be found in (5.14) below, where P_{nom} and R are fixed terms, taking the Y-Y configuration as the illustration example. ZSV is injected to facilitate the load currents reaching the averaged condition. As phase currents are identical with the load currents, the phase currents will also be regulated to the averaged current value. Conversely, in the Δ-Y configuration, the phase with lower power ratio than the averaged power ratio has a smaller current amount than the averaged load

current. This will lead to a higher temperature variation when the operation changes from case 1 to 2 than that in Y-Y. Therefore, more stresses are taken by the devices in that phase. Consequently, shorter lifespans are expected in that phase. In addition, with the ZSC, the phase that has a higher power ratio potentially will be overstressed.

$$I_{load} = \frac{\bar{\lambda} P_{nom}}{\sqrt{3} V_{LL}} \tag{5.14}$$

where $\bar{\lambda}$ is the averaged power ratio of the three phases, and V_{LL} is the load line-to-line voltage:

$$\bar{\lambda} = \frac{\lambda_a + \lambda_b + \lambda_c}{3} \tag{5.15}$$

$$V_{LL} = \sqrt{3} I_{load} R \tag{5.16}$$

In summary, the results presented here give an insight into the different stress distribution modes of these two configurations when operating under power imbalance situations and are established on the prerequisite that this load variation is the dominant operation condition. The lifetime of a Y-Y connected three-phase system is less complicated to estimate than that in a Δ-Y system. In addition, it is necessary to take environment and loading mission profiles into consideration when estimating the lifetimes of Δ-Y configurations particularly in applications such as wind or solar power converter systems, as they are the determinants of unbalanced power generation among phases. Therefore, the Δ-Y system requires more careful consideration in reliability assessments and lifetime evaluation when power imbalance is encountered.

Table 5.4 A summary of thermal performances and resultant failure cycles of the device by shifting the operation from Case 1 to 2 for Y-Y and Δ-Y (A) three-phase systems with the same load.

Power Ratio	Per Phase Temperature of Y-Y			Per Phase Temperature of Δ-Y		
	A	B	C	AB	BC	CA
Case 1 Balanced Condition	75 °C	75 °C	75 °C	37.7 °C	37.7 °C	37.7 °C
Case 2 Unbalanced Condition	65 °C	65 °C	65 °C	41.7 °C	36.5 °C	31.8 °C
Mean Temperature T_m	70 °C	70 °C	70 °C	39.7 °C	37.1 °C	34.7 °C
Temperature Variation ΔT_j	10 °C	10 °C	10 °C	4 °C	1.2 °C	5.9 °C
Number of Cycles to Fail N_f	2.79 E9	2.79 E9	2.79 E9	442 E9	259.9 E12	59.3 E9
Generated stress $(1/(2N_f))$	179E-12	179E-12	179E-12	1.13 E-12	1.9 E-15	8.4 E-12

Table 5.5 A summary of thermal performances and resultant failure cycles of the device by shifting the operation from Case 1 to 2 for Y-Y and Δ-Y (B) three-phase systems with the same phase current.

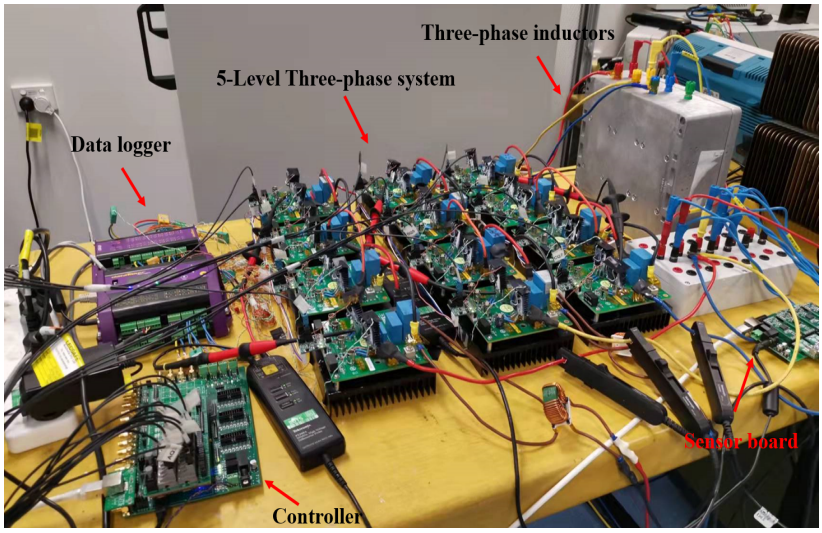
Power Ratio	Per Phase Temperature of Y-Y			Per Phase Temperature of Δ-Y		
	A	B	C	AB	BC	CA
Case 1 Balanced Condition	75 °C	75 °C	75 °C	75 °C	75 °C	75 °C
Case 2 Unbalanced Condition	65 °C	65 °C	65 °C	95 °C	73 °C	47.5 °C
Mean Temperature T_m	70 °C	70 °C	70 °C	85 °C	74 °C	61.25 °C
Temperature Variation ΔT_j	10 °C	10 °C	10 °C	20 °C	2 °C	27.5 °C
Number of cycles to fail N_f	2.79 E9	2.79 E9	2.79 E9	65.1 E6	13.2 E12	14.2 E6
Generated stress $(1/(2N_f))$	179E-12	179E-12	179E-12	7.7E-9	37.7E-15	35E-9

5.6 Experimental Results

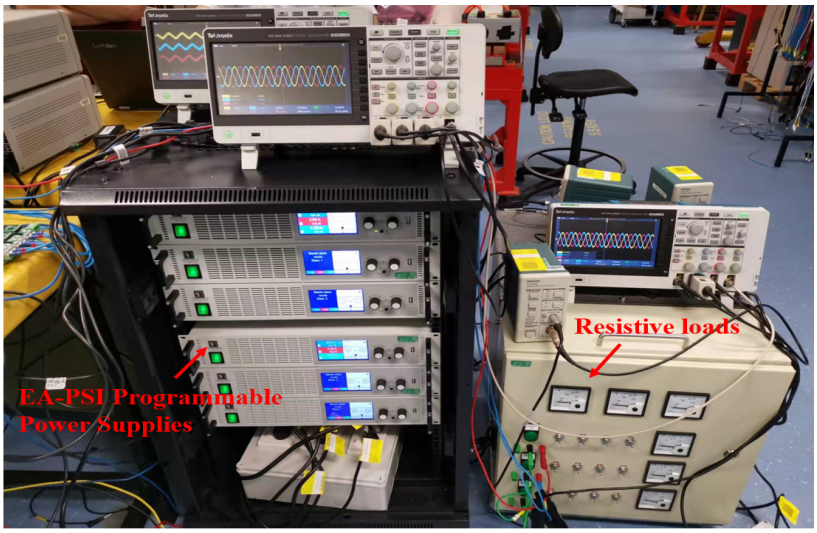
Due to the limitations of the selected power MOSFETs, experiments on down-scaled 600 W five-level CHB-based Y- and Δ-connected three-phase systems with the same load are carried out to verify the idea. Both nominal operation condition, and unbalanced operation condition are studied. To observe the electrical and thermal performances clearly, the unbalanced condition with two phases drops to 0.7 and 0.5 of their rated values are given. The schematic diagram of these two configurations and the experimental platform are shown in Figs. 5.1 and 5.15 respectively. The complete 5-level CHB converter three-phase prototype is shown in Fig. 5.15a, where the submodules adopted are modified from the CREE KIT8020-CRD-8FF1217P-1 half bridge module. The parameters of the experiment are shown in Tables 1.1 and 5.6. The electrical and thermal performances are captured and analysed. Regarding the system control, phase-shifted modulation is adopted, and the balancing of three phases are implemented by the TI microcontroller F28379D LaunchPad.

Table 5.6 Parameters in Experiment

Parameter	Y-Y	Δ-Y
HB module input power V_{dc}	70V	110 V
Carrier frequency	20 kHz	20 kHz
Three-phase nominal power	600 W	600 W
Filter inductance	-	10 mH
Load resistance	30 Ω	30 Ω
Load inductance	10 mH	3.3 mH
Heat sink thermal resistance R_{th}	20.5 Ω	20.5 Ω



(a)



(b)

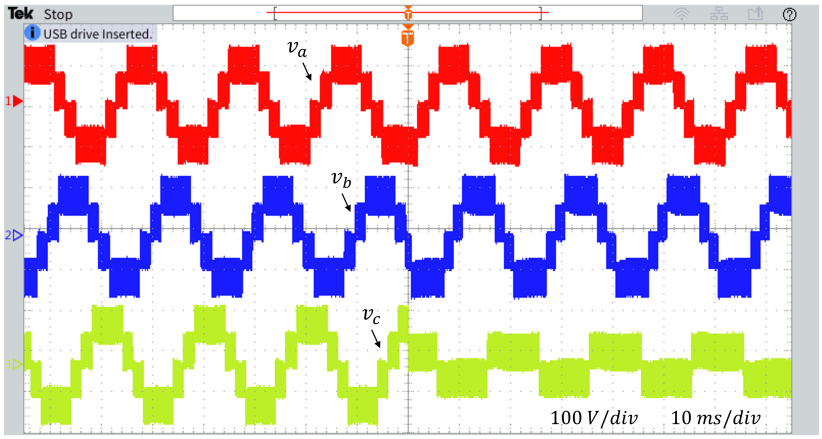
Fig. 5.15 Experimental setups (a) 5-level CHB three-phase system prototype. (b) Programmable DC power supplies and resistive loads.

5.6.1 Experimental results of Y-Y three-phase system under balanced and unbalanced operation conditions

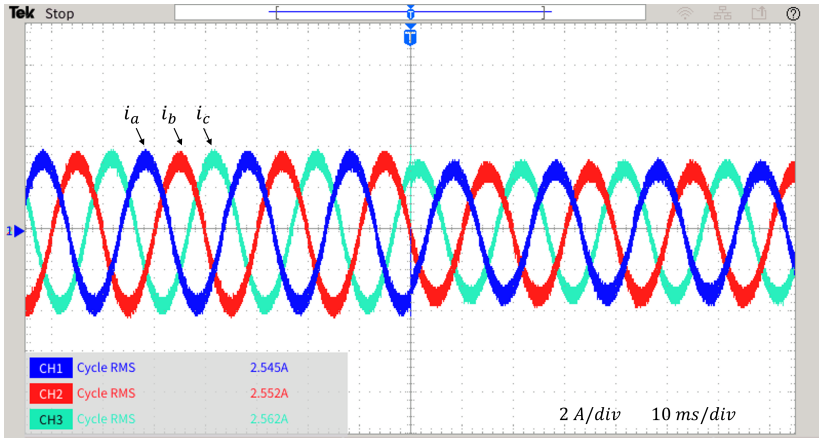
5.6.1.1 Electrical performance

The three-phase CHB converter output voltages v_a, v_b, v_c and phase currents i_a, i_b, i_c, together with the three-phase load currents i_{la}, i_{lb}, i_{lc} are measured to analyse electrical performance under nominal operation ($\lambda_a = \lambda_b = \lambda_c = 1$) and unbalanced operation ($\lambda_a = 1, \lambda_b = 0.7, \lambda_c = 0.5$).

Fig. 5.16a shows the transition of the CHB converter output voltages from nominal to unbalanced operation conditions. The phase C converter output voltage v_c becomes 3-level due to the lowered power generation of this phase, as can be clearly observed. In addition, slightly increased output voltages in both phase A v_a and B v_b due to the injected ZSV can also be seen by comparing balanced operation and unbalanced operations. In the meantime, both the three-phase phase i_a, i_b, i_c and load current i_{la}, i_{lb}, i_{lc} are still symmetric and balanced in these two scenarios, as illustrated in Figs. 5.16b and 5.16c, respectively. The ZSV is injected instead of ZSC to handle the power imbalances among the three-phase. The average RMS value from 2.5 V drops to 2.15A for both due to the overall reduced power generation. Small difference appears among three-phase load current may be due to the mismatch of the inductance and resistance among the three-phase.



(a)



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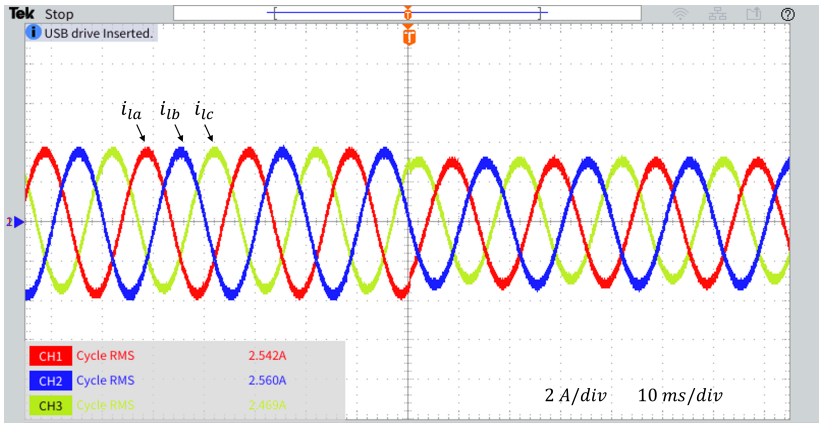


(c)

Fig. 5.16 Transition waveforms of a CHB-based 5-level three-phase Y-Y connected power system (a) CHB converter three-phase output voltages. (b) CHB converter three-phase currents. (c) Load three-phase currents.

5.6.1.2 Thermal performances

The temperature data points of all 24 power MOSFETs in the three-phase system are captured and plotted in Fig. 5.17. Due to the sensitivity of the measurement point of the MOSFETs, their individual heat sink temperatures are measured. For comparison purposes, the representative simulated thermal result of the system is also plotted in this figure, since all devices in this configuration share the same growing trend. To save the simulation time, instead of using a 20 kHz operation frequency, the system operates at 2 kHz is simulated. This results slightly underestimation of the switching losses, nevertheless, conduction losses are still the dominant losses. In the figure, the left and bottom axes are set for the measured results while the opposite ones are for the simulated results. As can be seen in Fig. 5.17, the temperature of power MOSFETs in all three phases drops from an averaged value of 60.5 °C to about 52.5 °C when changing from the rated operation condition to unbalanced condition. This follows the same decreasing trend with the three-phase currents of the CHB converter, demonstrating that, the ZSV has little impact on the device thermal performance. Note that in the ideal scenario, the temperature of all power devices should be identical, as the phase-shifted modulation scheme is employed. In other words, the same power losses are shared by the devices. The measured errors are about 6 °C, and mismatches are possibly due to thermocouple sensing errors, device manufacturing process variations, etc., while the high temperature further increases the difference. Nevertheless, the captured results reflect a genuine relationship between the three-phase currents and the temperature under study. In addition, small mismatches between simulated results and measured ones can be observed possibly due to the lack of considering the heat sink thermal capacitances in the simulation, reduced operation frequency, and experimental measurement errors.

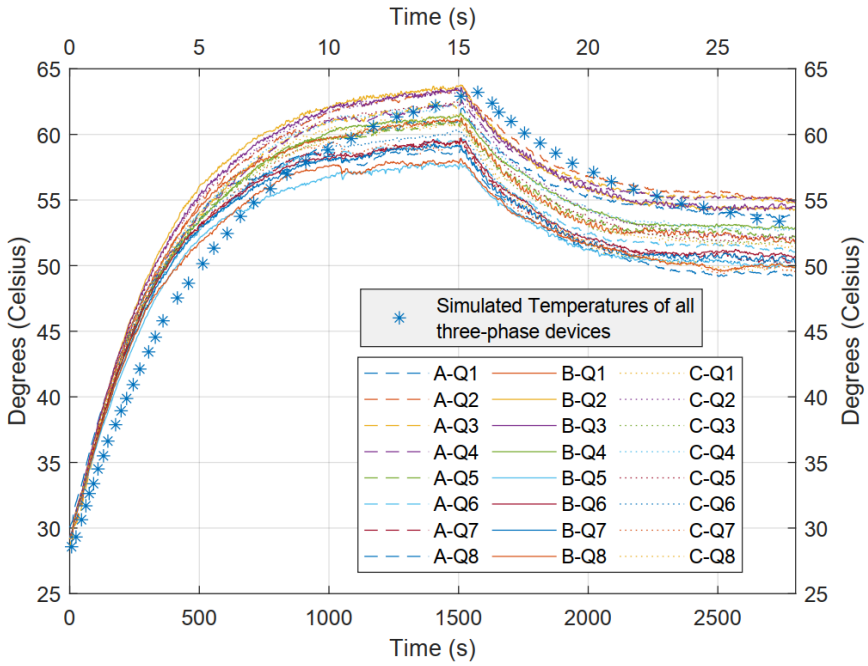


Fig. 5.17 Simulated and experimental thermal performances of power MOSFETs under rated and unbalanced situations.

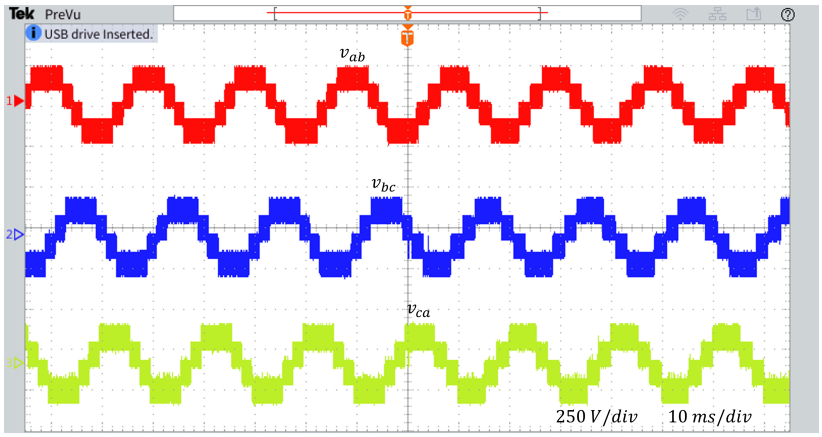
5.6.2 Experimental results of Δ-Y three-phase under balanced and unbalanced operation conditions

5.6.2.1 Electrical performance

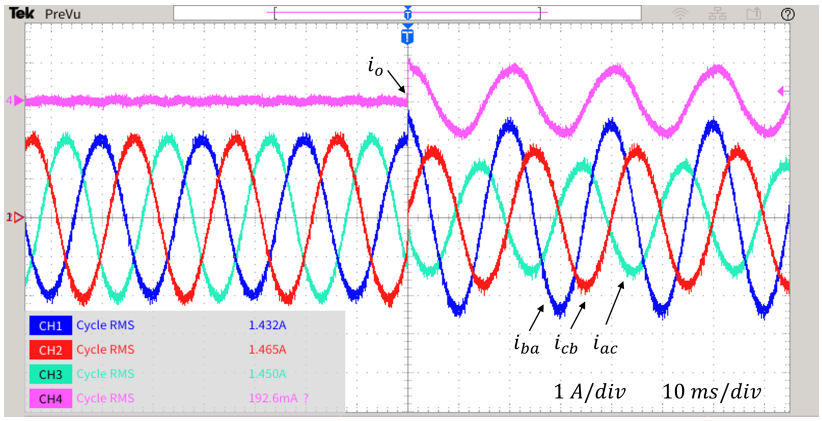
Similarly, the three-phase CHB converter output voltages v_{ab}, v_{bc}, v_{ca} and phase currents i_{ba}, i_{cb}, i_{ac}, together with the three-phase load currents i_{la}, i_{lb}, i_{lc} are measured to analyse electrical performance under nominal operation ($\lambda_{ab} = \lambda_{bc} = \lambda_{ca} = 1$) and unbalanced operation ($\lambda_{ab} = 1, \lambda_{bc} = 0.7, \lambda_{ca} = 0.5$).

Unlike the Y-Y configuration, the three-phase CHB converter output voltages v_{ab}, v_{bc}, v_{ca} of the Δ-Y configuration still exhibit the same number of voltage levels as can be observed in Fig. 5.18a. This is due to the ZSC are injected instead of ZSV to cope with the three-phase power imbalance. On the contrary, the CHB converter three-phase currents i_{ba}, i_{cb}, i_{ac}, are no longer symmetrical with the injected ZSC i_o in the unbalanced operation condition as depicted in Fig. 5.18b. As shown in the figure, i_o becomes a 50 Hz sine wave with RMS

value of 0.588 A to cope with the imbalance as compared to that in the nominal case which is almost 0 A. The currents i_{cb} and i_{ac} are reduced to 1.22 A and 0.97 A, respectively from the 1.45 A rated condition. These are mainly due to the reduced power generation in phases BC and CA. Moreover, with the injected ZSC to the phase AB, which produces the rated power in that phase, an overstress in i_{ba} with an RMS value of 1.7 A can be observed. Nevertheless, the three-phase load currents are still symmetrical and balanced sinusoidal waveforms with an average RMS value of 2.5 A and 2.15 A in these two operation conditions, respectively, as shown in Fig. 5.18c.



(a)



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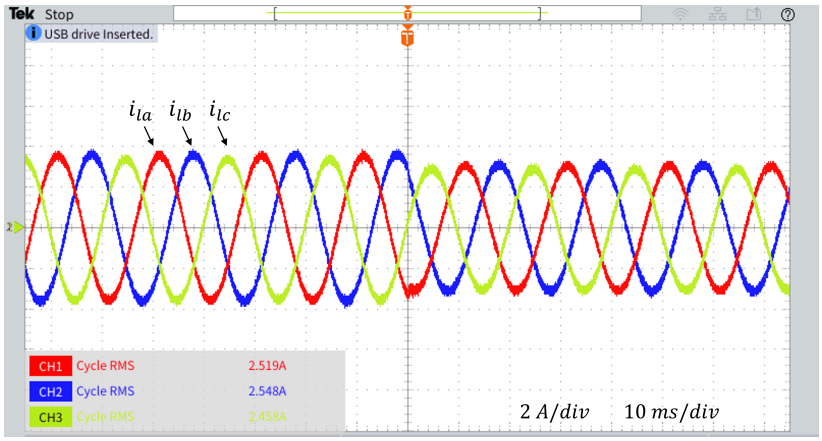


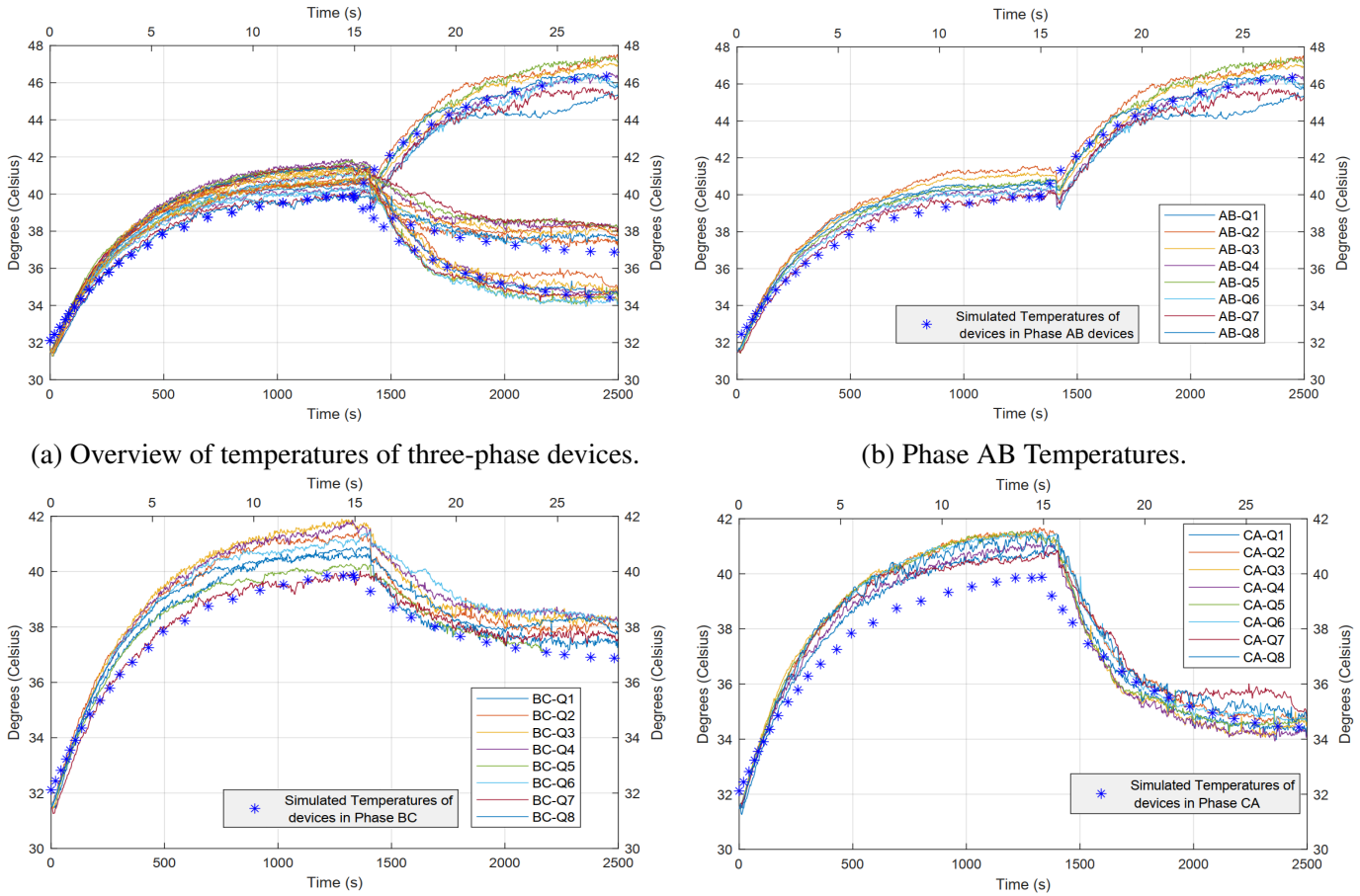
(c)

Fig. 5.18 Transition waveforms of a CHB-based 5-level three-phase Δ-Y connected power system (a) CHB converter three-phase output voltages. (b) CHB converter three-phase currents. (c) Load three-phase currents.

5.6.2.2 Thermal performance

Similarly, the temperature data points of all power MOSFETs in the Δ-connected CHB three-phase system under nominal and unbalanced conditions are captured and plotted in Fig. 5.19. Simulated results of this system at 2 kHz are also plotted for comparison. The reason for adopting the lowered frequency, the corresponding impacts, figure axes settings, and also the discussion on the mismatch between simulated and experimental results are the same as explained in Section 5.6.1.2.

As can be seen in Fig. 5.19, the temperature of the power MOSFETs in the nominal situation are identical with an average value of 41 °C. As compared to the Y-Y connection, the Δ three-phase temperatures are much lower due to the characteristics of the Δ- configuration, in which the phase output voltage and current are $\sqrt{3}$ and $1/\sqrt{3}$ respectively than those of the Y-connection. However, the CHB converter three-phase temperatures deviate from one to another after the transition, with devices in phase AB increases to 47 °C, and phase BC and CA decrease to 38 °C and 34.5 °C, respectively. The temperature follows the trend of the unbalanced three-phase current i_{ba}, i_{cb}, i_{ac}, demonstrating that, the ZSC has great impact on the device's thermal performance. Not only the phenomenon that the device in phase AB is overstressed can be observed, but also the nonidentical thermal stresses distribution among three phases are found. These should be carefully considered in the three-phase system lifespan evaluation. The measured errors in this case are about 2-3 °C, and mismatches are lower than in the Y-Y configuration due to the lowered current in three-phases, and hence more uniformed performances.



(a) Overview of temperatures of three-phase devices.

(b) Phase AB Temperatures.

(c) Phase BC Temperatures.

(d) Phase CA Temperatures.

Fig. 5.19 Simulated and measured thermal performances of Δ-connected three-phase under nominal and unbalanced operation conditions.

5.7 Conclusion

In this chapter, a comparison of the thermal and lifetime aspects of both balanced and unbalanced power generation of each phase in Y-Y and Δ-Y three-phase systems has been presented. The methodology to calculate the ZSV/ZSC is revisited first to cope with the unbalanced three-phase power together with control implementation explanations. Simulation of these two systems under different cases are carried out in PLECS®. The thermal performance of devices are evaluated by the thermal model provided by the software, and also by the behaviour averaged model which is constructed following the same principle as explained in Chapter 2. Experiments are also implemented to verify the idea. Based on the simulation and also experimental results, it is possible to conclude that with the injected ZSV to the unbalanced Y-Y three-phase system, the module temperature of each phase remains identical with a reduced value as compared to the rated case. Hence, it is expected that the three-phase modules will have similar lifetimes independent of the power imbalance level. Conversely, with the Δ-Y connection, power imbalances lead to unbalanced thermal stress distribution among the three phases. This will potentially lead to different lifetime expectations of modules among the three-phase. Hence, the Δ-Y system request more careful consideration in reliability assessment and lifetime evaluation when operating under power imbalance conditions.

Chapter 6

Conclusions and Future Prospects

6.1 Conclusion

Motivated by the requirement of high power density power supplies with reliable operation, this thesis implemented a series of thermally related investigations, such as electro-thermal modelling techniques, device lifetime prediction, and reliability assessment on three-phase applications.

Chapter 1 gave a brief background on future power supply needs and the requirement for safe operation of power systems. The introduction section explained how thermal performance affects the electrical parameters of both semiconductors and passive components. A brief introduction to lifetime estimation methodology was also presented.

Chapter 2 elaborated electro-thermal modelling techniques for power devices with both a switching and an averaged boost converter as shown in Figs. 2.1 and 2.11 respectively. Fairly accurate electrical and thermal results are achieved by both the proposed models, and simulation results show better agreement with the experimental results as compared to the conventional electrical model due to the introduced thermal impacts. In addition, the proposed ETAM is highly time-efficient and tackles the low simulation speed issue in the

ETM at high operation frequency. Both of these models are data-driven and possess ease of construction, allowing users to easily build their own models.

Chapter 3 proposed a MOSFET model which integrates the ETAM, aging and lifetime evaluation functions as illustrated in Fig. 3.1. With the proposed model, simultaneous in-the-loop monitoring of electrical and thermal performances, stress accumulation, degradation and lifetime consumption is possible. The estimated lifetimes with and without inducing aging effects are equivalent to 9.67 and 13 years, respectively, which verifies the importance of considering aging in lifetime evaluation. Another benefit of the model is the time efficiency due to the ETAM, allowing a 120 Ks simulation to be completed in around 46 s. Therefore, the proposed model is a good candidate for long-term device lifetime evaluation.

Chapter 4 presented an easy implementation of the rainflow counting algorithm in LTspice® as depicted in Fig. 4.3, aimed at providing a high counting accuracy method to assist in lifetime estimation. The work eliminates the necessity of multi-domain models and stages in the estimation process when adopting the conventional rainflow counting method. Instantaneous electrical and thermal performances, and accumulated stress of the device can also be monitored. The lifetime of an operating MOSFET in a boost converter is estimated, and compared with the simulated results from MATLAB and half-cycle counting methods. It is found that the proposed method has an improved counting accuracy with 3%-4% errors as compared to the half-cycle counting method, which has errors of 16.3%-31.6% under different load conditions. Moreover, a further refinement of the accuracy to 1.3%-2% can be achieved by adding an extra comparison round.

Chapter 5 gave reliability assessments of 5-level CHB converter-based Y- and Δ-connected three-phase systems, particularly when they face unbalanced three-phase power generation operation conditions. ZSV and ZSC are injected into the two systems, respectively, to cope with the power imbalance, and the corresponding electrical and thermal performances are discussed based on ETM, and with the impact on the lifespan of each phase. It is found

that although the Δ-connection has better balancing capability than the Y configuration, an unbalanced stress distribution among phases is occurring. Moreover, overstressing may occur in phases in some situations. Conversely, the Y configuration does not have this issue. Consequently, there is a trade-off between electrical and thermal operations when selecting a configuration to deal with power imbalances.

6.2 Future Work

- **Thermal coupling issues**: The works presented in chapter 2 Sections 2.3 and 2.5 give relatively comprehensive electro-thermal modelling methodologies for both active and passive power components. However, only the self-heating effects of devices are considered. One potential avenue for future work is to take thermal coupling issues into account. Recent studies investigating thermal coupling focus on the conduction coupling of MOSFETs/IGBTs in the same heat sink or in a power module, and the convection and radiation impacts are usually neglected. While the conduction coupling is the dominant effect, convectional coupling among devices should be considered, from the point of view of the design of a whole converter, especially for future converter/inverter design which is required to have high power density. This is not only for a better thermal management, but also in terms of size and efficiency optimization in the converter/inverter design phase.

- **Active thermal control schemes or power management strategies**: Another potential future line of work that can be developed is the active thermal control schemes for improving the reliability of power converters/inverters, and/or prolonging device lifetimes. Although the ETM and ETAM proposed in chapter 2 Sections 2.3 and 2.5 are based on the SPICE simulator, these models fully utilize mathematical equations which can be similarly adopted in the controller. By sensing the required current and

voltage of the converter/inverter, and applying to the state observer, the temperature of components can be estimated. In addition, with the comprehensive MOSFET model proposed in chapter 3 Section 3.3 the state of health of a device can be evaluated further. Based on these considerations, active thermal control schemes and/or power management strategies can be developed to reduce the power losses of components or converter/inverter, and/or to reschedule the power routing and therefore redistribute the losses, hence to prolong the device lifetime and improve reliability. The findings of different thermal stresses suffered in unbalanced Y- and Δ-connected CHB converter based three-phase systems in chapter 5 Section 5.5 can also give some guidance.

- **Digital-twin**: Another future avenue of research is to develop a digital-twin, which is a digital replication of the physical converter/inverter in the controller. The work presented in chapters 2-3 Sections 2.3, 2.5, 3.3, 4.4 and 5.5 assists users to predict the actual values of parameters, and the lifetime of devices/components in simulation, while the digital-twin helps in identifying their real-time values. Hence, an online monitoring platform of power electronics system can be built by the digital-twin. Similarly, the parametric drift can effectively help users to identify the state of health of a device, to schedule maintenance, and hence to avoid any downtime of the power converter/inverter.

6.3 Publications

6.3.1 Journals

1. T. Cheng, D. D.-C. Lu and Y. P. Siwakoti, “A MOSFET SPICE Model With Integrated Electro-Thermal Averaged Modeling, Aging, and Lifetime Estimation,” *IEEE Access*, vol. 9, pp. 5545-5554, 2021.

2. T. Cheng, D. D.-C. Lu and Y. P. Siwakoti, “Circuit-Based Rainflow Counting Algorithm in Application of Power Device Lifetime Estimation.” *Energies*, vol 15, pp. 5159, 2022.

6.3.2 Journals Under Preparation

1. T. Cheng, R. P. Aguilera, D. D.-C. Lu and Y. P. Siwakoti, "Evaluation of The lifetime of Three Phase Systems With Zero Sequence Injection." in preparation.

6.3.3 Conference Papers

1. T. Cheng, D. D.-C. Lu and Y. Siwakoti, "Electro-Thermal Modeling of a Boost Converter Considering Device Self-heating," in *2019 IEEE 4th International Future Energy Electronics Conference (IFEEC)*, 2019, pp. 1-6.

2. T. Cheng, D. D.-C. Lu and Y. Siwakoti, "Electro-Thermal Average Modeling of a Boost Converter Considering Device Self-heating." in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 2854-2859.

3. T. Cheng, R. P. Aguilera, D. D. -C. Lu and Y. P. Siwakoti, "Evaluation of Thermal Performance of Three-Phase Systems With Zero Sequence Injection," *2021 IEEE Southern Power Electronics Conference (SPEC)*, 2021, pp. 1-6.

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